



# THE DATASHEET OF FSA636UCX



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# Ultra Small, Low Power, 4 Data Lane, 2:1 Switch for MIPI, SuperSpeed USB, PCIe and DisplayPort

## Product Preview FSA636

### Description

The FSA636 may be configured as a four data lane MIPI D-PHY, V2.1 switch or a three data lane MIPI C-PHY, V1.2 switch. This single pole, double throw (SPDT) switch is optimized for switching between both high speed and low power MIPI sources. The FSA636 is designed for the MIPI specification and allows connection to a CSI or DSI module. It may also be used for any high speed switching application with amplitudes of 2 V or less and is capable of a total data throughput of up to 23.9 Gbps.

### Features

- Switch Type: SPDT (10x)
- Signal Type:
  - ◆ MIPI D-PHY V2.1
  - ◆ MIPI C-PHY V1.2
  - ◆ SuperSpeed USB
  - ◆ PCIe 2.0
  - ◆ DisplayPort HBR
- Input Signal: 0 V to 2 V
- $V_{CC}$ : 1.5 to 5.0 V
- $R_{ON}$ : 6  $\Omega$  Typical HS/LP MIPI
- $\Delta R_{ON}$ : 0.1  $\Omega$  Typical
- $R_{ON\_FLAT}$ : 0.9  $\Omega$  Typical
- $I_{CCZ}$ : 1.0  $\mu$ A Maximum
- $I_{CC}$ : 30  $\mu$ A Maximum
- $O_{IRR}$ : -24 dB Typical
- Bandwidth: 4 GHz Typical
- Xtalk: -30 dB Typical
- $C_{ON}$ : 1.5 pF Typical
- Skew: 6 ps Typical

### Applications

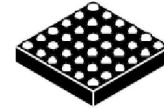
- Cellular Phones, Smart Phones
- Cameras
- Tablets
- Laptops
- Displays

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WLCSP36 2.06x2.06x0.432  
CASE 567XU

### MARKING DIAGRAMS



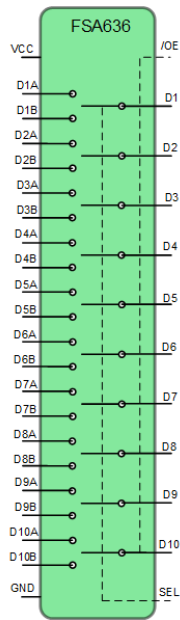
|    |                        |
|----|------------------------|
| VR | = Specific Device Code |
| KK | = Assembly Lot         |
| X  | = Year                 |
| Y  | = Work Week            |
| Z  | = Assembly Location    |

### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

# FSA636

## PIN DESCRIPTIONS



| PIN NAME | DESCRIPTION      |       |          |
|----------|------------------|-------|----------|
| Dn       | Common Data Path |       |          |
| DnA      | Data Path A      |       |          |
| DnB      | Data Path B      |       |          |
| /OE      | Output Enable    |       |          |
| SEL      | Control Pin      | SEL=0 | Dn = DnA |
|          |                  | SEL=1 | Dn = DnB |
| VCC      | Power            |       |          |
| GND      | Ground           |       |          |

Figure 1. Analog Symbol

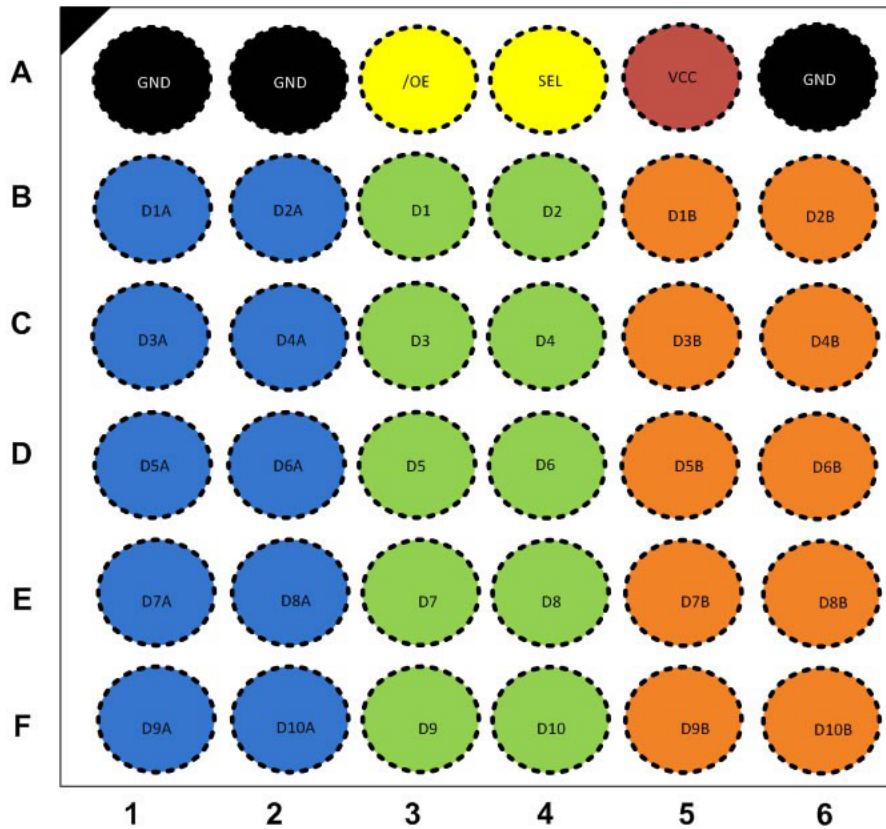


Figure 2. Top Through View

# FSA636

## BALL-TO-PIN MAPPINGS

| Ball | Pin Name | Ball | Pin Name | Ball | Pin Name |
|------|----------|------|----------|------|----------|
| A1   | GND      | C1   | D3A      | E1   | D7A      |
| A2   | GND      | C2   | D4A      | E2   | D8A      |
| A3   | /OE      | C3   | D3       | E3   | D7       |
| A4   | SEL      | C4   | D4       | E4   | D8       |
| A5   | Vcc      | C5   | D3B      | E5   | D7B      |
| A6   | GND      | C6   | D4B      | E6   | D8B      |
| B1   | D1A      | D1   | D5A      | F1   | D9A      |
| B2   | D2A      | D2   | D6A      | F2   | D10A     |
| B3   | D1       | D3   | D5       | F3   | D9       |
| B4   | D2       | D4   | D6       | F4   | D10      |
| B5   | D1B      | D5   | D5B      | F5   | D9B      |
| B6   | D2B      | D6   | D6B      | F6   | D10B     |

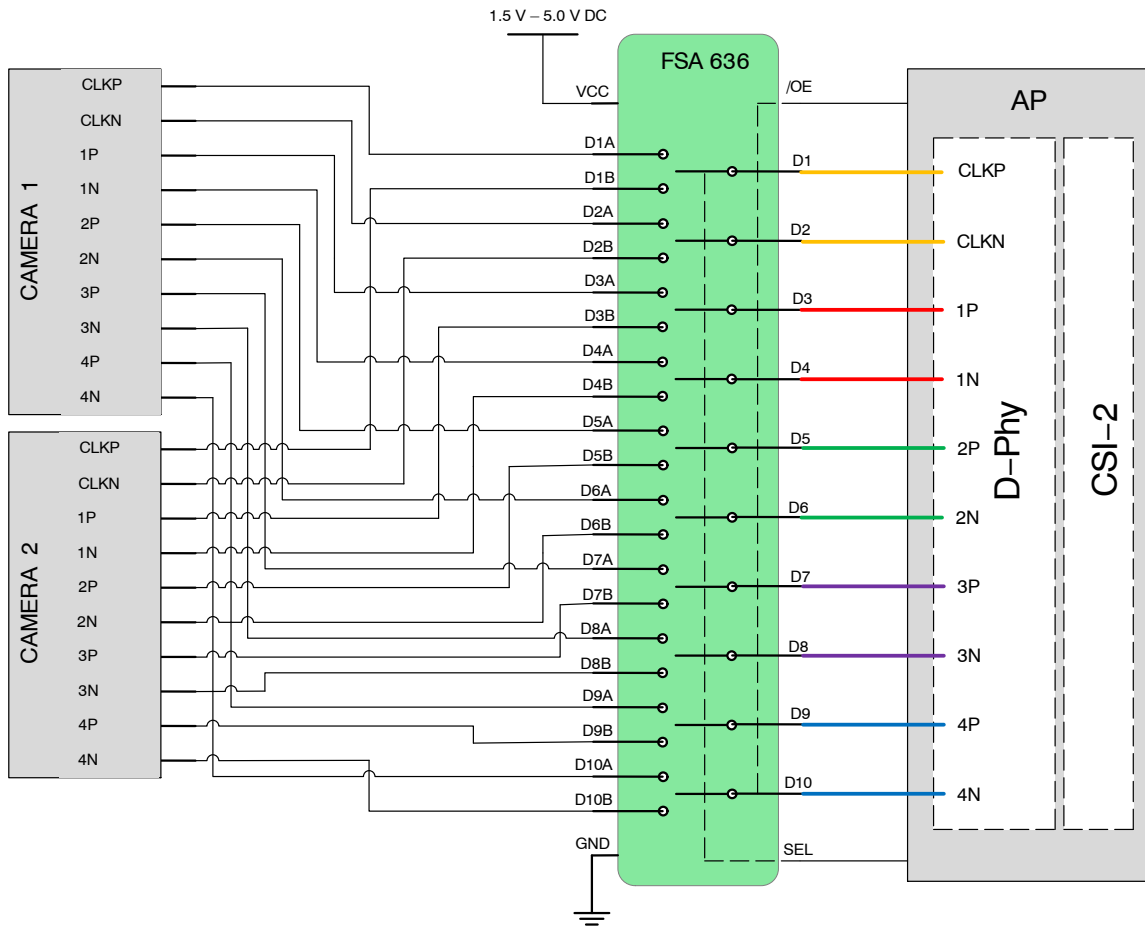


Figure 3. Suggested Configuration for 4 Lane D-PHY

# FSA636

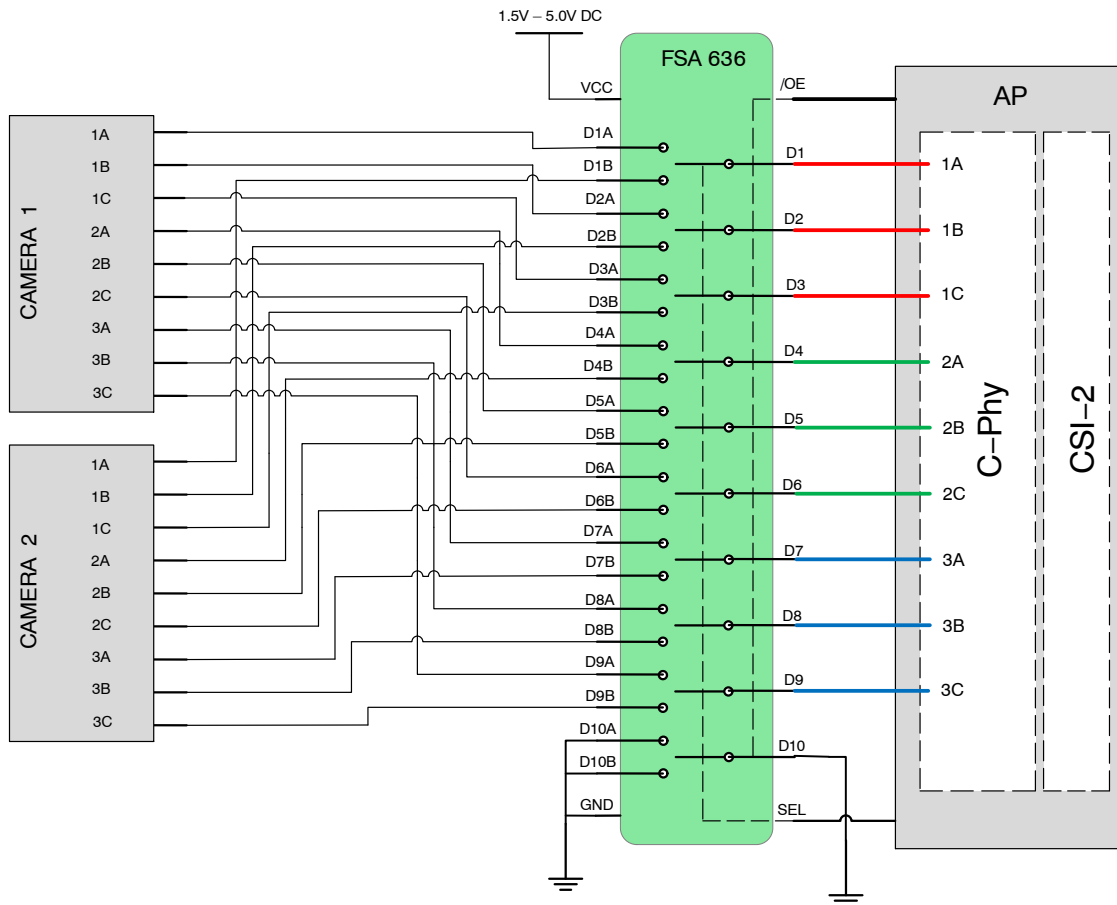


Figure 4. Suggested Configuration for 3 Lane C-PHY

## TRUTH TABLE

| SEL  | /OE  | Function                 |
|------|------|--------------------------|
| LOW  | LOW  | Dn = DnA                 |
| HIGH | LOW  | Dn = DnB                 |
| X    | HIGH | All Ports High Impedance |

## ABSOLUTE MAXIMUM RATINGS

| Symbol             | Parameter                                | Min      | Max             | Unit |
|--------------------|--|----------|-----------------|------|
| V <sub>CC</sub>    | Supply Voltage                           | -0.5     | 6.0             | V    |
| V <sub>CNTRL</sub> | DC Input Voltage (/OE, SEL) (Note 1)     | -0.5     | V <sub>CC</sub> | V    |
| V <sub>SW</sub>    | DC Switch I/O Voltage (Note 1, 2)        | -0.3     | 2.1             | V    |
| I <sub>IK</sub>    | DC Input Diode Current                   | -50      |                 | mA   |
| I <sub>OUT</sub>   | DC Output Current                        |          | 25              | mA   |
| T <sub>STG</sub>   | Storage Temperature                      | -65      | +150            | °C   |
| ESD                | Human Body Model, JEDEC: JESD22-A114     | All Pins | 2.0             | kV   |
|                    | Charged Device Model, JEDEC: JESD22-C101 |          | 0.5             |      |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.
2. V<sub>SW</sub> refers to analog data switch paths.

# FSA636

## RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter                                 | Min     | Max             | Unit  |   |
|-------------------|---|---------|-----------------|-------|---|
| V <sub>CC</sub>   | Supply Voltage                            | 1.5     | 5.0             | V     |   |
| V <sub>CTRL</sub> | Control Input Voltage (SEL, /OE) (Note 3) | 0       | V <sub>CC</sub> | V     |   |
| V <sub>SW</sub>   | Switch I/O Voltage (Dn, DAn, DBn)         | HS Mode | 0               | 0.425 | V |
|                   |   | LP Mode | -0.05           | 2.0   | V |
| T <sub>A</sub>    | Operating Temperature                     | -40     | +85             | °C    |   |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. The control inputs must be held HIGH or LOW; they must not float.

## ELECTRICAL SPECIFICATION TABLE

Typical values are at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 3.3 V unless otherwise specified.

| Symbol  | Parameter   | Conditions  | Min  | Typ | Max  | Units |
|---|---|---|------|-----|------|-------|
| <b>DC ELECTRICAL PARAMETERS</b>                 |   |   |      |     |      |       |
| V <sub>IK</sub>                                 | Clamp Diode Voltage (/OE, SEL)                                  | I <sub>IN</sub> = -18 mA, V <sub>CC</sub> = 1.5 V   | -1.2 |     | -0.6 | V     |
| V <sub>IH</sub>                                 | Input Voltage High (/OE, SEL)                                   | V <sub>CC</sub> = 1.5 V to 5.0 V  | 1.3  |     |      | V     |
| V <sub>IL</sub>                                 | Input Voltage Low (/OE, SEL)                                    | V <sub>CC</sub> = 1.5 V to 5.0 V  |      |     | 0.5  | V     |
| I <sub>IN</sub>                                 | Control Input Leakage (SEL, /OE)                                | V <sub>CTRL</sub> = 0 to V <sub>CC</sub>  | -0.5 |     | 0.5  | μA    |
| I <sub>NO(OFF)</sub> ,<br>I <sub>INC(OFF)</sub> | Off Leakage Current of Port Dn, DnA, DnB                        | V <sub>SW</sub> = 0.0 ⇐ DATA ⇐ 2.0 V, V <sub>CC</sub> = 5 V   | -0.5 |     | 0.5  | μA    |
| I <sub>A(ON)</sub>                              | On Leakage Current of Common Ports (Dn)                         | V <sub>SW</sub> = 0.0 ⇐ DATA ⇐ 2.0 V, V <sub>CC</sub> = 5 V   | -0.5 |     | 0.5  | μA    |
| I <sub>OFF</sub>                                | Power-Off Leakage Current                                       | V <sub>SW</sub> = 0 V or 2.0 V; V <sub>CC</sub> = 0 V   | -0.5 |     | 0.5  | μA    |
| I <sub>OZ</sub>                                 | Off-State Leakage   | V <sub>SW</sub> = 0.0 ⇐ DATA ⇐ 2.0 V, /OE = High, V <sub>CC</sub> = 5 V   | -0.5 |     | 0.5  | μA    |
| R <sub>ON_MIPI_HS</sub>                         | Switch On Resistance for HS MIPI Applications                   | I <sub>ON</sub> = -8 mA, /OE = 0 V, SEL = V <sub>CC</sub> or 0 V, DnA or DnB = 0.2 V, V <sub>CC</sub> = 1.5 V to 5.0 V                              |      | 6   | 9    | Ω     |
| R <sub>ON_MIPI_LP</sub>                         | Switch On Resistance for LP MIPI Applications                   | I <sub>ON</sub> = -8 mA, /OE = 0 V, SEL = V <sub>CC</sub> or 0 V, DnA or DnB = 1.2 V, V <sub>CC</sub> = 1.5 V to 5.0 V                              |      | 6   | 9    | Ω     |
| ΔR <sub>ON_MIPI_HS</sub>                        | On Resistance Matching Between HS MIPI Channels (Note 4)        | I <sub>ON</sub> = -8 mA, /OE = 0 V, SEL = V <sub>CC</sub> or 0 V, DnA or DnB = 0.2 V, V <sub>CC</sub> = 1.5 V to 5.0 V                              |      | 0.1 | 0.25 | Ω     |
| ΔR <sub>ON_MIPI_LP</sub>                        | On Resistance Matching Between LP MIPI Channels (Note 4)        | I <sub>ON</sub> = -8 mA, /OE = 0 V, SEL = V <sub>CC</sub> or 0 V, DnA or DnB = 1.2 V, V <sub>CC</sub> = 1.5 V to 5.0 V                              |      | 0.1 | 0.25 | Ω     |
| R <sub>ON_FLAT_MIPI_HS</sub>                    | On Resistance Flatness for HS MIPI Signals (Note 4)             | I <sub>ON</sub> = -8 mA, /OE = 0 V, SEL = V <sub>CC</sub> or 0 V, DnA or DnB = 0 V to 0.3 V, V <sub>CC</sub> = 1.5 V to 5.0 V                       |      | 0.9 |      | Ω     |
| R <sub>ON_FLAT_MIPI_LP</sub>                    | On Resistance Flatness for LP MIPI Signals (Note 4)             | I <sub>ON</sub> = -8 mA, /OE = 0 V, SEL = V <sub>CC</sub> or 0 V, DnA or DnB = 0V to 1.2 V, V <sub>CC</sub> = 1.5 V to 5.0 V                        |      | 0.9 |      | Ω     |
| I <sub>CCZ</sub>                                | Quiescent Hi-Z Supply Current                                   | V <sub>IN</sub> = 0 V or V <sub>CC</sub> , V <sub>SEL</sub> = 0 V or V <sub>CC</sub> , I <sub>OUT</sub> = 0 A, V <sub>CC</sub> = 5.0 V, /OE = 5.0 V |      |     | 1    | μA    |
| I <sub>CC</sub>                                 | Quiescent Supply Current  | V <sub>IN</sub> = 0 or V <sub>CC</sub> , I <sub>OUT</sub> = 0 A, V <sub>CC</sub> = 5.0 V, /OE = 0 V   |      |     | 30   | μA    |
| I <sub>CCCT</sub>                               | Increase in ICC Current Per Control Voltage and V <sub>CC</sub> | V <sub>SEL</sub> = 1.5 V, /OE = 5.0 V, V <sub>CC</sub> = 5.0 V  |      | 1   | 4    | μA    |

# FSA636

**ELECTRICAL SPECIFICATION TABLE** Typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V}$  unless otherwise specified.

| Symbol                          | Parameter  | Conditions  | Min | Typ  | Max  | Units         |
|---------------------------------|--|---|-----|------|------|---------------|
| <b>AC ELECTRICAL PARAMETERS</b> |  |   |     |      |      |               |
| tINIT                           | Initialization Time VCC to Output (Note 4)               | RL = 50 $\Omega$ , CL = 0 pF, VSW = 0.6 V                         |     | 60   | 150  | $\mu\text{s}$ |
| tEN                             | Enable Turn-On Time, /OE to Output                       | RL = 50 $\Omega$ , CL = 0 pF, VSW = 0.6 V                         |     | 60   | 150  | $\mu\text{s}$ |
| tDIS                            | Disable Turn-Off Time, /OE to Output                     | RL = 50 $\Omega$ , CL = 0 pF, VSW = 0.6 V                         |     | 25   | 250  | ns            |
| tON                             | Turn-On Time, SEL to Output                              | RL = 50 $\Omega$ , CL = 0 pF, VSW = 0.6 V, SEL H to L, SEL L to H |     | 350  | 1100 | ns            |
| tOFF                            | Turn-Off Time SEL to Output                              | RL = 50 $\Omega$ , CL = 0 pF, VSW = 0.6 V, SEL H to L, SEL L to H |     | 125  | 1100 | ns            |
| tBBM                            | Break-Before-Make Time (Note 4)                          | RL = 50 $\Omega$ , CL = 0 pF, VSW = 0.6 V, 50%DnA/B to 50%DnB/A   |     | 150  |      | ns            |
| tPD                             | Propagation Delay (Note 4)                               | RL = 50 $\Omega$ , CL = 0 pF                                      |     | TBD  |      | ps            |
| OIRR                            | Off Isolation for MIPI (Note 4)                          | RL = 50 $\Omega$ , f = 2250 MHz, /OE = VCC, VSW = 200 mVpp        |     | -24  |      | dB            |
| XTALK                           | Crosstalk for MIPI (Note 4)                              | RL = 50 $\Omega$ , f = 2250 MHz, VSW = 200 mVpp, SEL = H & L      |     | -30  |      | dB            |
| BW                              | Bandwidth at -3dB (Note 4)                               | RL = 50 $\Omega$ , CL = 0 pF, VSW = 200 mVpp                      |     | 4.0  |      | GHz           |
| IL                              | Insertion Loss at 750 MHz (Note 4)                       | RL = 50 $\Omega$ , CL = 0 pF, VSW = 200 mVpp                      |     | -0.7 |      | dB            |
| tSK(O)                          | Channel-to-Channel Single-Ended Skew (Note 4)            | RL = 50 $\Omega$ , CL = 0 pF, VSW = 0.3 V                         |     | 6    |      | ps            |
| tSK(P)                          | Skew of Opposite Transitions of the Same Output (Note 4) | RL = 50 $\Omega$ , CL = 0 pF, VSW = 0.3 V                         |     | 6    |      | ps            |

## CAPACITANCE

|      |  |                                      |  |     |  |    |
|------|--|--------------------------------------|--|-----|--|----|
| CIN  | Control Pin Input Capacitance (Note 5) | VCC = 0 V, f = 1 MHz                 |  | 2.1 |  | pF |
| CON  | On Capacitance (Note 5)                | VCC = 3.3 V, /OE = 0 V, f = 2250 MHz |  | 1.5 |  | pF |
| COFF | Off Capacitance (Note 5)               | VCC and /OE = 3.3 V, f = 2250 MHz    |  | 0.9 |  | pF |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES: Guarantee Levels:

- Guaranteed by Design. Characterized on the ATE or Bench.
- Guaranteed by Design and Characterization, not Production Tested

The table below pertains to the Packaging information on the following page

## ORDERING INFORMATION

| Part Number | Operating Temperature Range | Package   | Top Mark |
|-------------|-----------------------------|---|----------|
| FSA636UCX   | -40 to +85°C                | 36-Ball WLCSP, Non-JEDEC<br>2.06 x 2.06 mm, 0.35 mm Pitch | VR       |

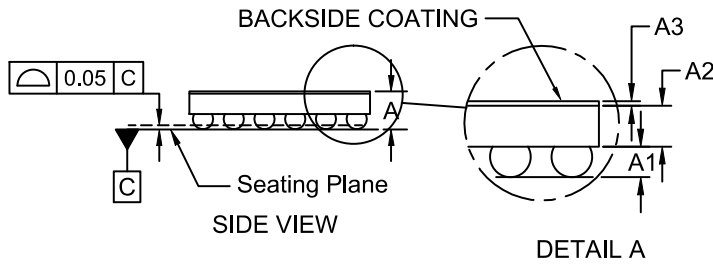
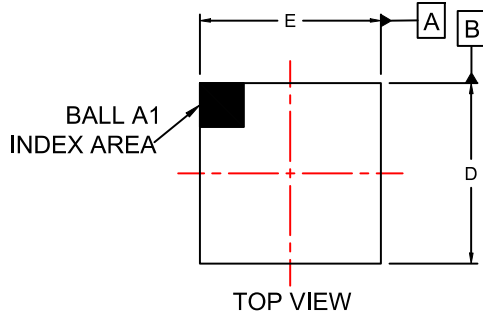
# FSA636

## PACKAGE DIMENSIONS

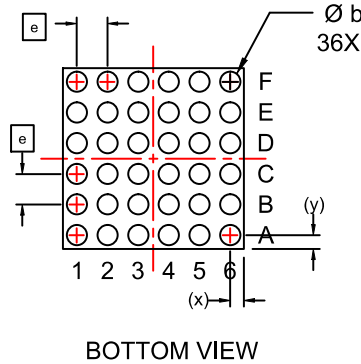


**WLCSP36 2.06x2.06x0.432**  
CASE 567XU  
ISSUE 0

DATE 26 APR 2019



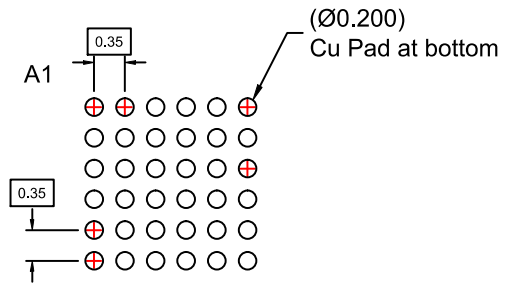
⊕ 0.005 (M) C A B



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS

| DIM | MILLIMETERS |       |       |
|-----|-------------|-------|-------|
|     | MIN.        | NOM.  | MAX.  |
| A   | 0.391       | 0.432 | 0.473 |
| A1  | 0.154       | 0.174 | 0.194 |
| A2  | 0.215       | 0.233 | 0.251 |
| A3  | 0.022       | 0.025 | 0.028 |
| b   | 0.211       | 0.231 | 0.251 |
| D   | 2.03        | 2.06  | 2.09  |
| E   | 2.03        | 2.06  | 2.09  |
| e   | 0.35 BSC    |       |       |
| x   | 0.140       | 0.155 | 0.170 |
| y   | 0.140       | 0.155 | 0.170 |



### RECOMMENDED MOUNTING FOOTPRINT\* (NSMD PAD TYPE)

\*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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