THE DATASHEET OF

DS21Q41BT

www.win-source.net 0086-755-83957316

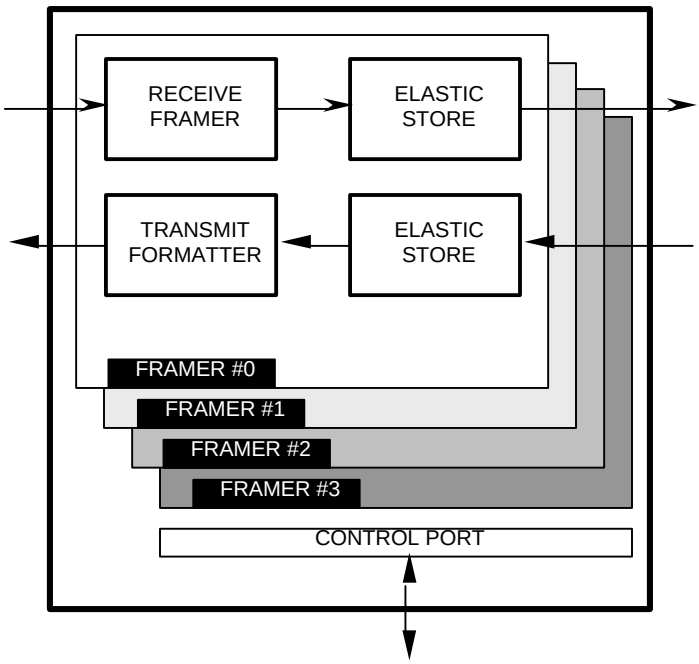
DS21Q41B
Quad T1 Framer

www.dalsemi.com

FEATURES

- Four T1 DS1/ISDN-PRI framing transceivers
- All four framers are fully independent
- Frames to D4, ESF, and SLC-96 formats
- 8-bit parallel control port that can be connected to either multiplexed or non-multiplexed buses
- Each of the four framers contains dual two-frame elastic stores that can connect to asynchronous or synchronous backplanes up to 8.192 MHz
- Extracts and inserts robbed bit signaling
- Framer and payload loopbacks
- Large counters for BPVs, LCVs, EXZs, CRC6, PCVs, F-bit errors and the number of multiframes out of sync
- Contains ANSI 1s density monitor and enforcer
- CSU loop code generator and detector
- Programmable output clocks for Fractional T1, ISDN-PRI, Actual Size and per channel loopback applications
- Onboard FDL support circuitry
- Pin-compatible with DS21Q43 Quad E1 Framer
- 5V supply; low power CMOS
- Available in 128-pin TQFP
- Industrial (-40°C to +85°C) grade version available (DS21Q41BTN)

FUNCTIONAL DIAGRAM



ACTUAL SIZE

DESCRIPTION

The DS21Q41B combines four of the popular DS2141A T1 Controllers onto a single monolithic die. The "B" designation denotes that some new features are available in the Quad version that were not available in the single T1 device. The added features in the DS21Q41B are listed in Section 1. The DS21Q41B offers a substantial space savings to applications that require more than one T1 framer on a card. The Quad version is only slightly bigger than the single T1 device. All four framers in the DS21Q41B are totally independent; they do not share a common framing synchronizer. Also, the transmit and receive sides of each framer are totally independent. The dual two-frame elastic stores contained in each of the four framers can be independently enabled and disabled as required. The DS21Q41B meets all of the latest specifications including ANSI T1.403 (and the emerging T1.403-199X), ANSI T1.231-1993, AT&T TR62411, AT&T TR54016, ITU G.704 and G.706.

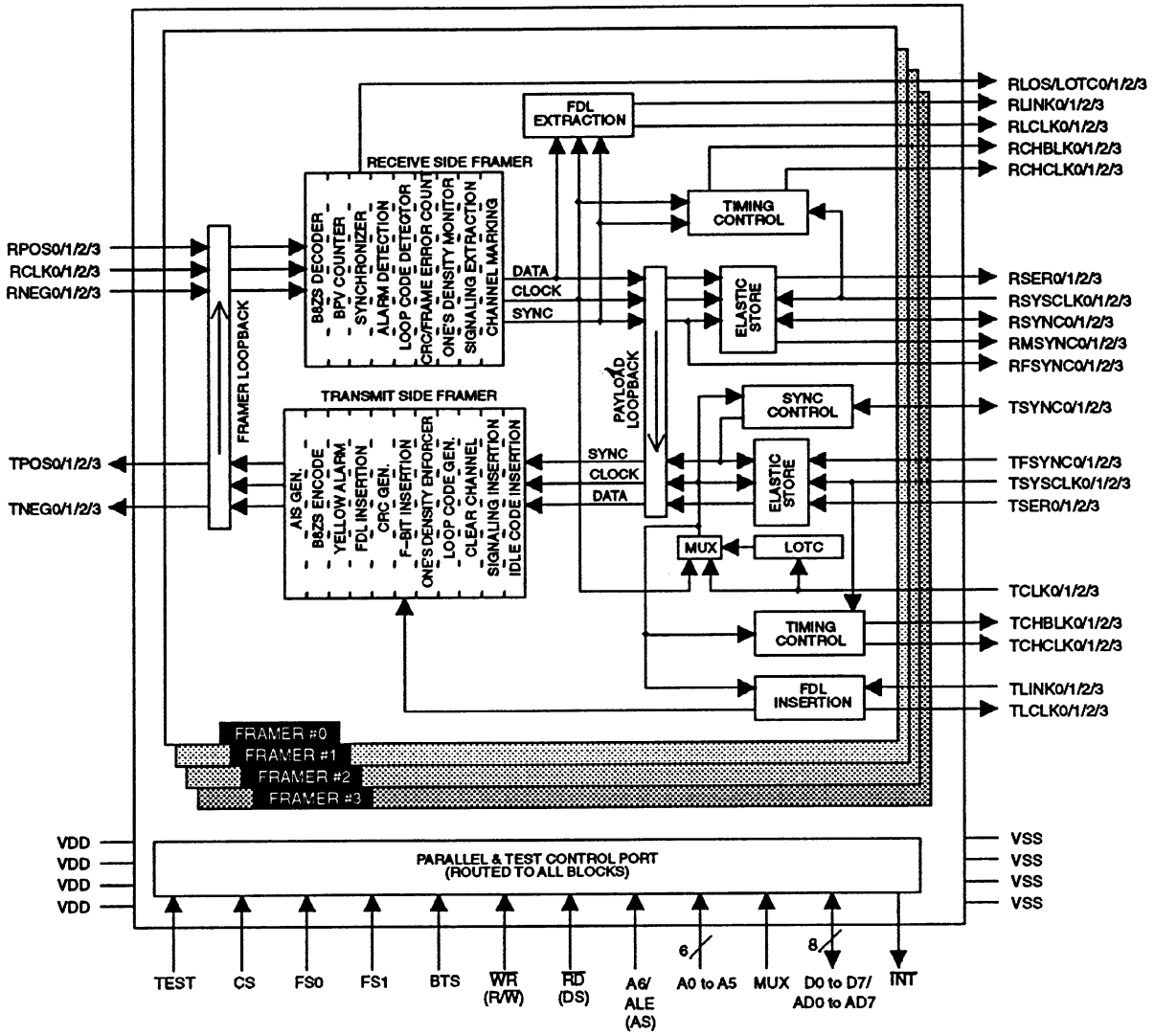
1.0 INTRODUCTION

The DS21Q41B Quad T1 Framer is made up of five main parts: framer #0, framer #1, framer #2, framer #3, and the control port which is shared by all four framers. See the Block Diagram in Figure 1-1. Each of the four framers within the DS21Q41B maintain the same register structure that appeared in the DS2141A. The two framer select inputs (FS0 and FS1) are used to determine which framer within the DS21Q41B is being accessed. In this manner, software written for the DS2141A can also be used with only slight modifications, in the DS21Q41B.

Several new features have been added to the framers in the DS21Q41B over the DS2141A. Below is short list of the new features. More details can be found in Sections 2 through 12.

ADDED FEATURE	SECTION
Non-multiplexed parallel control port operation	2
ANSI ones density monitor (transmit and receive sides) and enforcer (transmit side only)	3 and 4
CSU loop code generator	3
Elastic store reset and minimum delay mode	3 and 10
Divide RSYNC output by two for D4 to ESF conversion applications	3
TCLK keep alive	3
Indications of transmit side elastic store slip direction	4
Ability to decouple the receive and transmit elastic stores	10
Counting of excessive 0s (EXZs)	5

DS21Q41B BLOCK DIAGRAM Figure 1-1



TRANSMIT PIN LIST Table 1-1

PIN	SYMBOL	TYPE	DESCRIPTION
19	TCLK0	I	Transmit Clock for Framer 0
53	TCLK1	I	Transmit Clock for Framer 1
87	TCLK2	I	Transmit Clock for Framer 2
113	TCLK3	I	Transmit Clock for Framer 3
126	TSER0	I	Transmit Serial Data for Framer 0
32	TSER1	I	Transmit Serial Data for Framer 1
66	TSER2	I	Transmit Serial Data for Framer 2
92	TSER3	I	Transmit Serial Data for Framer 3
128	TCHCLK0	O	Transmit Channel Clock from Framer 0
34	TCHCLK1	O	Transmit Channel Clock from Framer 1
68	TCHCLK2	O	Transmit Channel Clock from Framer 2
94	TCHCLK3	O	Transmit Channel Clock from Framer 3
1	TCHBLK0	O	Transmit Channel Block from Framer 0
35	TCHBLK1	O	Transmit Channel Block from Framer 1
69	TCHBLK2	O	Transmit Channel Block from Framer 2
95	TCHBLK3	O	Transmit Channel Block from Framer 3
20	TLCLK0	O	Transmit Link Clock from Framer 0
54	TLCLK1	O	Transmit Link Clock from Framer 1
88	TLCLK2	O	Transmit Link Clock from Framer 2
114	TLCLK3	O	Transmit Link Clock from Framer 3
22	TLINK0	I	Transmit Link Data for Framer 0
56	TLINK1	I	Transmit Link Data for Framer 1
90	TLINK2	I	Transmit Link Data for Framer 2
116	TLINK3	I	Transmit Link Data for Framer 3
2	TPOS0	O	Transmit Bipolar Data from Framer 0
36	TPOS1	O	Transmit Bipolar Data from Framer 1
70	TPOS2	O	Transmit Bipolar Data from Framer 2
96	TPOS3	O	Transmit Bipolar Data from Framer 3
3	TNEG0	O	Transmit Bipolar Data from Framer 0
37	TNEG1	O	Transmit Bipolar Data from Framer 1
71	TNEG2	O	Transmit Bipolar Data from Framer 2
97	TNEG3	O	Transmit Bipolar Data from Framer 3
21	TSYNC0	I/O	Transmit Sync for Framer 0
55	TSYNC1	I/O	Transmit Sync for Framer 1
89	TSYNC2	I/O	Transmit Sync for Framer 2
115	TSYNC3	I/O	Transmit Sync for Framer 3

127	TFSYNC0	I	Transmit Sync for Elastic Store in Framer 0
33	TFSYNC1	I	Transmit Sync for Elastic Store in Framer 1
67	TFSYNC2	I	Transmit Sync for Elastic Store in Framer 2
93	TFSYNC3	I	Transmit Sync for Elastic Store in Framer 3
125	TSYSCLK0	I	Transmit System Clock for Elastic Store in Framer 0
31	TSYSCLK1	I	Transmit System Clock for Elastic Store in Framer 1
65	TSYSCLK2	I	Transmit System Clock for Elastic Store in Framer 2
91	TSYSCLK3	I	Transmit System Clock for Elastic Store in Framer 3

RECEIVE PIN LIST Table 1-2

PIN	SYMBOL	TYPE	DESCRIPTION
6	RCLK0	I	Receive Clock for Framer 0
40	RCLK1	I	Receive Clock for Framer 1
74	RCLK2	I	Receive Clock for Framer 2
100	RCLK3	I	Receive Clock for Framer 3
13	RSER0	O	Receive Serial Data from Framer 0
49	RSER1	O	Receive Serial Data from Framer 1
83	RSER2	O	Receive Serial Data from Framer 2
107	RSER3	O	Receive Serial Data from Framer 3
9	RCHCLK0	O	Receive Channel Clock from Framer 0
43	RCHCLK1	O	Receive Channel Clock from Framer 1
77	RCHCLK2	O	Receive Channel Clock from Framer 2
103	RCHCLK3	O	Receive Channel Clock from Framer 3
10	RCHBLK0	O	Receive Channel Block from Framer 0
44	RCHBLK1	O	Receive Channel Block from Framer 1
80	RCHBLK2	O	Receive Channel Block from Framer 2
104	RCHBLK3	O	Receive Channel Block from Framer 3
5	RLCLK0	O	Receive Link Clock from Framer 0
39	RLCLK1	O	Receive Link Clock from Framer 1
73	RLCLK2	O	Receive Link Clock from Framer 2
99	RLCLK3	O	Receive Link Clock from Framer 3
4	RLINK0	O	Receive Link Data from Framer 0
38	RLINK1	O	Receive Link Data from Framer 1
72	RLINK2	O	Receive Link Data from Framer 2
98	RLINK3	O	Receive Link Data from Framer 3
8	RPOS0	I	Receive Bipolar Data for Framer 0
42	RPOS1	I	Receive Bipolar Data for Framer 1
76	RPOS2	I	Receive Bipolar Data for Framer 2

102	RPOS3	I	Receive Bipolar Data for Framer 3
7	RNEG0	I	Receive Bipolar Data for Framer 0
41	RNEG1	I	Receive Bipolar Data for Framer 1
75	RNEG2	I	Receive Bipolar Data for Framer 2
101	RNEG3	I	Receive Bipolar Data for Framer 3
12	RSYNC0	I/O	Receive Sync for Framer 0
48	RSYNC1	I/O	Receive Sync for Framer 1
82	RSYNC2	I/O	Receive Sync for Framer 2
106	RSYNC3	I/O	Receive Sync for Framer 3
17	RFSYNC0	O	Receive Frame Sync from Framer 0
51	RFSYNC1	O	Receive Frame Sync from Framer 1
85	RFSYNC2	O	Receive Frame Sync from Framer 2
109	RFSYNC3	O	Receive Frame Sync from Framer 3
16	RMSYNC0	O	Receive Multiframe Sync from Framer 0
50	RMSYNC1	O	Receive Multiframe Sync from Framer 1
84	RMSYNC2	O	Receive Multiframe Sync from Framer 2
108	RMSYNC3	O	Receive Multiframe Sync from Framer 3
11	RSYSCLK0	I	Receive System Clock for Elastic Store in Framer 0
45	RSYSCLK1	I	Receive System Clock for Elastic Store in Framer 1
81	RSYSCLK2	I	Receive System Clock for Elastic Store in Framer 2
105	RSYSCLK3	I	Receive System Clock for Elastic Store in Framer 3
18	RLOS/LOTC0	O	Receive Loss of Sync/Loss of Transmit Clock from Framer 0
52	RLOS/LOTC1	O	Receive Loss of Sync/Loss of Transmit Clock from Framer 1
86	RLOS/LOTC2	O	Receive Loss of Sync/Loss of Transmit Clock from Framer 2
112	RLOS/LOTC3	O	Receive Loss of Sync/Loss of Transmit Clock from Framer 3

CONTROL PORT/TEST/SUPPLY PIN LIST Table 1-3

PIN	SYMBOL	TYPE	DESCRIPTION
57	TEST	I	3-State Control for all Output and I/O Pins
60	CS	I	Chip Select
58	FS0	I	Framer Select 0 for Parallel Control Port
59	FS1	I	Framer Select 1 for Parallel Control Port
61	BTS	I	Bus Type Select for Parallel Control Port
63	$\overline{WR}$ (R/$\overline{W}$)	I	Write Input (Read/Write)
62	$\overline{RD}$ (DS)	I	Read Input (Data Strobe)
23	A0	I	Address Bus Bit 0; LS
24	A1	I	Address Bus Bit 1
25	A2	I	Address Bus Bit 2
26	A3	I	Address Bus Bit 3
27	A4	I	Address Bus Bit 4
28	A5	I	Address Bus Bit 5
29	A6 or ALE (AS)	I	Address Bus Bit 6; MSB or Address Latch Enable (Address Strobe)
30	$\overline{INT}$	O	Receive Alarm Interrupt for all Four Framers
64	MUX	I	Non-Multiplexed or Multiplexed Bus Select
117	D0 or AD0	I/O	Data Bus Bit 0 or Address/Data Bus Bit 0; LSB
118	D1 or AD1	I/O	Data Bus Bit 1 or Address/Data Bus Bit 1
119	D2 or AD2	I/O	Data Bus Bit 2 or Address/Data Bus Bit 2
120	D3 or AD3	I/O	Data Bus Bit 3 or Address/Data Bus Bit 3
121	D4 or AD4	I/O	Data Bus Bit 4 or Address/Data Bus Bit 4
122	D5 or AD5	I/O	Data Bus Bit 5 or Address/Data Bus Bit 5
123	D6 or AD6	I/O	Data Bus Bit 6 or Address/Data Bus Bit 6
124	D7 or AD7	I/O	Data Bus Bit 7 or Address/Data Bus Bit 7; MSB
15	V_{DD}	-	Positive Supply Voltage
47	V_{DD}	-	Positive Supply Voltage
79	V_{DD}	-	Positive Supply Voltage
111	V_{DD}	-	Positive Supply Voltage
14	V_{SS}	-	Signal Ground
46	V_{SS}	-	Signal Ground
78	V_{SS}	-	Signal Ground
110	V_{SS}	-	Signal Ground

DS21Q41B PIN DESCRIPTION Table 1-4

Transmit Clock [TCLK]. 1.544 MHz primary clock. Used to clock data through the transmit side formatter.

Transmit Serial Data [TSER]. Transmit NRZ serial data. Sampled on the falling edge of TCLK when the transmit side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled.

Transmit Channel Clock [TCHCLK]. 192 kHz clock which pulses high during the LSB of each channel. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for parallel to serial conversion of channel data, locating robbed-bit signaling bits, and for blocking clocks in DDS applications. See Section 12 for timing details.

Transmit Bipolar Data [TPOS and TNEG]. Updated on rising edge of TCLK. Can be programmed to output NRZ data on TPOS via the TCR1.7 control bit.

Transmit Channel Block [TCHBLK]. A user programmable output that can be forced high or low during any of the 24 T1 channels. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used such as Fractional T1, 384k bps service, 768k bps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications and for per-channel loopback. See Section 12 for timing details.

Transmit System Clock [TSYSCLK]. 1.544 MHz or 2.048 MHz clock. Only used when the transmit side elastic store function is enabled. Should be tied low in applications that do not use the transmit side elastic store.

Transmit Link Clock [TLCLK]. 4 kHz or 2 kHz (ZBTSI) demand clock for the TLINK input. See Section 12 for timing details.

Transmit Link Data [TLINK]. If enabled via TCR1.2, this pin will be sampled during the F-bit time on the falling edge of TCLK for data insertion into either the FDL stream (ESF) or the Fs bit position (D4) or the Z-bit position (ZBTSI). See Section 12 for timing details.

Transmit Sync [TSYNC]. A pulse at this pin will establish either frame or multiframe boundaries for the DS21Q41B. Via TCR2.2, the DS21Q41B can be programmed to output either a frame or multiframe pulse at this pin. If this pin is set to output pulses at frame boundaries, it can also be set via TCR2.4 to output double-wide pulses at signaling frames. See Section 12 for timing details.

Transmit Frame Sync [TFSYNC]. 8 kHz pulse. Only used when the transmit side elastic store is enabled. A pulse at this pin will establish frame boundaries for the DS21Q41B. Should be tied low in applications that do not use the transmit side elastic store. See Section 12 for timing details.

Receive Link Data [RLINK]. Updated with either FDL data (ESF) or Fs bits (D4) or Z bits (ZBTSI) one RCLK before the start of a frame. See Section 12 for timing details.

Receive Link Clock [RLCLK]. 4 kHz or 2 kHz (ZBTSI) demand clock for the RLINK input. See Section 12 for timing details.

Receive Clock [RCLK]. 1.544 MHz primary clock. Used to clock data through the receive side of the framer.

Receive Channel Clock [RCHCLK]. 192 kHz clock which pulses high during the LSB of each channel. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYSCLK when the receive side elastic store is enabled. Useful for parallel to serial conversion of channel data, locating robbed-bit signaling bits, and for blocking clocks in DDS applications. See Section 12 for timing details.

Receive Channel Block [RCHBLK]. A user programmable output that can be forced high or low during any of the 24 T1 channels. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYSCLK when the receive side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used such as Fractional T1, 384k bps service, 768k bps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications and for per-channel loopback. See Section 12 for timing details.

Receive Serial Data [RSER]. Received NRZ serial data. Updated on rising edges of RCLK when the receive side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive side elastic store is enabled.

Receive Sync [RSYNC]. An extracted pulse, one RCLK wide, is output at this pin which identifies either frame (RCR2.4=0) or multiframe boundaries (RCR2.4=1). If set to output frame boundaries, then via RCR2.5, RSYNC can also be set to output double-wide pulses on signaling frames. If the receive side elastic store is enabled, then this pin can be enabled to be an input at which a frame boundary pulse is applied. See Section 12 for timing details.

Receive Frame Sync (RFSYNC). An extracted 8 kHz pulse, one RCLK wide, is output at this pin which identifies frame boundaries. See Section 12 for timing details.

Receive Multiframe Sync [RMSYNC]. Only used when the receive side elastic store is enabled. An extracted pulse, one RSYSCLK wide, is output at this pin which identifies multiframe boundaries. If the receive side elastic store is disabled, then this output should be ignored. See Section 12 for timing details.

Receive Bipolar Data Inputs [RPOS and RNEG]. Sampled on falling edge of RCLK. Tie together to receive NRZ data and disable bipolar violation monitoring circuitry.

Receive System Clock [RSYSCLK]. 1.544 MHz or 2.048 MHz clock. Only used when the elastic store function is enabled. Should be tied low in applications that do not use the elastic store. Allowing this pin to float can cause the device to 3-state its outputs.

Receive Loss of Sync/Loss of Transmit Clock [RLOS/LOTC]. A dual function output. If CCR1.6=0, then this pin will toggle high when the synchronizer is searching for the T1 frame and multiframe. If CCR1.6=1, then this pin will toggle high if the TCLK pin has not been toggled for 5 μs.

Receive Alarm Interrupt [$\overline{\text{INT}}$]. Flags host controller during conditions defined in the Status Registers of the four framers. User can poll the Interrupt Status Register (ISR) to determine which status register in which framer is active (if any). Active low, open drain output.

3-State Control [Test]. Set high to 3-state all output and I/O pins (including the parallel control port). Set low for normal operation. Useful in board-level testing.

Bus Operation [MUX]. Set low to select non-multiplexed bus operation. Set high to select multiplexed bus operation.

Data Bus [D0 to D7] or Address/Data Bus [AD0 to AD7]. In non-multiplexed bus operation (MUX=0), serves as the data bus. In multiplexed bus operation (MUX=1), serves as an 8-bit multiplexed address/data bus.

Address Bus [A0 to A5]. In non-multiplexed bus operation (MUX=0), serves as the address bus. In multiplexed bus operation (MUX=1), these pins are not used and should be tied low.

Bus Type Select [BTS]. Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the $\overline{RD}$ (DS), ALE(AS), and $\overline{WR}$ (R/$\overline{W}$) pins. If BTS=1, then these pins assume the function listed in parentheses ().

Read Input [$\overline{RD}$] (Data Strobe [DS]).

Framer Selects [FS0 and FS1]. Selects which of the four framers to be accessed.

Chip Selects [$\overline{CS}$]. Must be low to read or write to any of the four framers.

A6 or Address Latch Enable [ALE] (Address Strobe [AS]). In non-multiplexed bus operation (MUX=0), serves as the upper address bit. In multiplexed bus operation (MUX=1), serves to demultiplex the bus on a positive-going edge.

Write Input [$\overline{WR}$] (Read/Write [R/$\overline{W}$]).

Positive Supply [V_{DD}]. 5.0 volts ±0.5 volts.

Signal Ground [V_{SS}]. 0.0 volts.

DS21Q41B REGISTER MAP Table 1-5

ADDRESS	R/W	REGISTER NAME
20	R/W	Status Register 1
21	R/W	Status Register 2
22	R/W	Receive Information Register 1
23	R	Line Code Violation Count Register 1
24	R	Line Code Violation Count Register 2
25	R	Path Code Violation Count Register 1(1)
26	R	Path Code Violation Count Register 2
27	R	Multiframe Out of Sync Count Register 2
28	R	Receive FDL Register
29	R/W	Receive FDL Match Register 1
2A	R/W	Receive FDL Match Register 2
2B	R/W	Receive Control Register 1
2C	R/W	Receive Control Register 2
2D	R/W	Receive Mark Register 1
2E	R/W	Receive Mark Register 2
2F	R/W	Receive Mark Register 3
30	R/W	Common Control Register 3
31	R/W	Receive Information Register 2
32	R/W	Transmit Channel Blocking Register 1
33	R/W	Transmit Channel Blocking Register 2
34	R/W	Transmit Channel Blocking Register 3
35	R/W	Transmit Control Register 1
36	R/W	Transmit Control Register 2
37	R/W	Common Control Register 1
38	R/W	Common Control Register 2
39	R/W	Transmit Transparency Register 1
3A	R/W	Transmit Transparency Register 2
3B	R/W	Transmit Transparency Register 3
3C	R/W	Transmit Idle Register 1
3D	R/W	Transmit Idle Register 2
3E	R/W	Transmit Idle Register 3
3F	R/W	Transmit Idle Definition Register
60	R	Receive Signaling Register 1
61	R	Receive Signaling Register 2
62	R	Receive Signaling Register 3
63	R	Receive Signaling Register 4

ADDRESS	R/W	REGISTER NAME
64	R	Receive Signaling Register 5
65	R	Receive Signaling Register 6
66	R	Receive Signaling Register 7
67	R	Receive Signaling Register 8
68	R	Receive Signaling Register 9
69	R	Receive Signaling Register 10
6A	R	Receive Signaling Register 11
6B	R	Receive Signaling Register 12
6C	R/W	Receive Channel Blocking Register 1
6D	R/W	Receive Channel Blocking Register 2
6E	R/W	Receive Channel Blocking Register 3
6F	R/W	Interrupt Mast Register 2
70	R/W	Transmit Signaling Register 1
71	R/W	Transmit Signaling Register 2
72	R/W	Transmit Signaling Register 3
73	R/W	Transmit Signaling Register 4
74	R/W	Transmit Signaling Register 5
75	R/W	Transmit Signaling Register 6
76	R/W	Transmit Signaling Register 7
77	R/W	Transmit Signaling Register 8
78	R/W	Transmit Signaling Register 9
79	R/W	Transmit Signaling Register 10
7A	R/W	Transmit Signaling Register 11
7B	R/W	Transmit Signaling Register 12
7C	R/W	Test Register(2)
7D	R/W	Test Register(2)
7E	R/W	Transmit FDL Register
7F	R/W	Interrupt Mask Register 1

NOTES:

1. Address 25 also contains Multiframe Out of Sync Count Register 1.
2. The Test Registers are used only by the factory; these registers must be cleared (set to all 0s) on power-up initialization to insure proper operation.
3. Any unused register address will allow the status of the interrupts to appear on the bus.

DS21Q41B FRAMER DECODE Table 1-6

FS1	FS0	FRAMER ACCESSED
0	0	#0
0	1	#1
1	0	#2
1	1	#3

2.0 PARALLEL PORT

The DS21Q41B is controlled via either a non-mutliplexed (MUX=0) or multiplexed (MUX=1) by an external microcontroller or microprocessor. The DS21Q41B can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parenthesis (). See the timing diagrams in the A.C. Electrical Characteristics for more details.

3.0 CONTROL REGISTERS

The operation of each framer within the DS21Q41B is configured via a set of seven registers. Typically, the control registers are only accessed when the system is first powered up. Once the DS21Q41B has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two Receive Control Registers (RCR1 and RCR2), two Transmit Control Registers (TCR1 and TCR2), and three Common Control Registers (CCR1, CCR2, and CCR3).

RCR1: RECEIVE CONTROL REGISTER 1 (Address=2B Hex)

(MSB)							(LSB)
LCVCRF	ARC	OOF1	OOF2	SYNCC	CYNCT	SYNCE	RESYNC

SYMBOL	POSITION	NAME AND DESCRIPTION
LCVCRF	RCR1.7	**Line Code Violation Count Register Function Select.** 0=do not count excessive 0s 1=count excessive 0s
ARC	RCR1.6	**Auto Resync Criteria.** 0=Resync on OOF or RCL event 1=Resync on OOF only
OOF1	RCR1.5	**Out Of Frame Select 1.** 0=2/4 frame bits in error 1=2/5 frame bits in error
OOF2	RCR1.4	**Out Of Frame Select 2.** 0=follow RCR1.5 1=2/6 frame bits in error
SYNCC	RCR1.3	**Sync Criteria. In D4 Framing Mode.** 0=search for Ft pattern, then search for Fs pattern 1=cross couple Ft and Fs pattern **In ESF Framing Mode.** 0=search for FPS pattern only 1=search for FPS and verify with CRC6
SYNCT	RCR1.2	**Sync Time.** 0=qualify 10 bits 1=qualify 24 bits
SYNCE	RCR1.1	**Sync Enable.** 0=auto resync enabled 1=auto resync disabled
RESYNC	RCR1.0	**Resync.** When toggled from low to high, a resynchronization of the receive side framer is initiated. Must be cleared and set again for a subsequent resync.

RCR2: RECEIVE CONTROL REGISTER 2 (Address=2C Hex)

(MSB)							(LSB)
RCS	ZBTSI	RSDW	RSM	RSIO	D4YM	FSBE	MOSCRF

SYMBOL	POSITION	NAME AND DESCRIPTION
RCS	RCR2.7	**Receive Code Select.** 0=idle code (7F Hex) 1=digital milliwatt code (1E/0B/0B/1E/9E/8B/8B/9E Hex)
ZBTSI	RCR2.6	**ZBTSI Enable.** 0=ZBTSI disabled 1=ZBTSI enabled
RSDW	RCR2.5	**RSYNC Double-Wide.** 0=do not pulse double-wide in signaling frames 1=do pulse double-wide in signaling frames (note: this bit must be set to 0 when RCR2.4=1 or when RCR2.3=1)
RSM	RCR2.4	**RSYNC Mode Select.** 0=frame mode (see the timing in Section 12) 1=multiframe mode (see the timing in Section 12)
RSIO	RCR2.3	**RSYNC I/O Select.** 0=RSYNC is an output 1=RSYNC is an input (only valid if elastic store enabled) (note: this bit must be set to 0 when CCR1.2=0)
D4YM	RCR2.2	**D4 Yellow Alarm Select.** 0=0s in bit 2 of all channels 1=a one in the S-bit position of frame 12
FSBE	RCR2.1	**PCVCR Fs Bit Error Report Enable.** 0=do not report bit errors in Fsbit position; only Ft bit position 1=report bit errors in Fs bit position as well as Ft bit position
MOSCRF	RCR2.0	**Multiframe Out of Sync Count Register Function Select.** 0=count errors in the framing bit position 1=count the number of multiframes out of sync

TCR1: TRANSMIT CONTROL REGISTER 1 (Address=35 Hex)

(MSB)							(LSB)
LOTCMC	TFPT	TCPT	RBSE	GB7S	TLINK	TBL	TYEL

SYMBOL	POSITION	NAME AND DESCRIPTION
LOTCMC	TCR1.7	**Loss Of Transmit Clock Mux Control.** Determines whether the transmit side formatter should switch to the ever present RCLK if the TCLK input should fail to transition (see Figure 1-1 for details). 0=do not switch to RCLK if TCLK stops 1=switch to RCLK if TCLK stops
TFPT	TCR1.6	**Transmit Framing Pass Through.** (see note below) 0=Ft or FPS bits sourced internally 1=Ft or FPS bits sampled at TSER during F-bit time
TCPT	TCR1.5	**Transmit CRC Pass Through.** (see note below) 0=source CRC6 bits internally 1=CRC6 bits sampled at TSER during F-bit time
RBSE	TCR1.4	**Robbed Bit Signaling Enable.** (see note below) 0=no signaling is inserted in any channel 1=signaling is inserted in all channels (the TTR registers can be used to block insertion on a channel by channel basis)
GB7S	TCR1.3	**Global Bit 7 Stuffing.** (see note below) 0=allow the TTR registers to determine which channels containing all 0s are to be Bit 7 stuffed 1=force Bit 7 stuffing in all 0-byte channels regardless of how the TTR registers are programmed
TLINK	TCR1.2	**TLINK Select.** (see note below) 0=source FDL or Fs bits from TFDL register 1=source FDL or Fs bits from the TLINK pin
TBL	TCR1.1	**Transmit Blue Alarm.** (see note below) 0=transmit data normally 1=transmit an unframed all ones code at TPOS and TNEG
TYEL	TCR1.0	**Transmit Yellow Alarm.** (see note below) 0=do not transmit yellow alarm 1=transmit yellow alarm

Note: for a detailed description of how the bits in TCR1 affect the transmit side formatter of the DS21Q41, please see Figure 12-9.

TCR2: TRANSMIT CONTROL REGISTER 2 (Address=36 Hex)

(MSB)							(LSB)
TEST1	TEST0	ZBTSI	TSDW	TSM	TSIO	D4YM	B7ZS

SYMBOL	POSITION	NAME AND DESCRIPTION
TEST1	TCR2.7	**Test Mode Bit 1 for Output Pins.** See Table 3-1.
TEST0	TCR2.6	**Test Mode Bit 0 for Output Pins.** See Table 3-1.
ZBTSI	TCR2.5	**ZBTSI Enable.** 0=ZBTSI disabled 1=ZBTSI enabled
TSDW	TCR2.4	**TSYNC Double-Wide.** (Note: this bit must be set to 0 when TCR2.3=1 or when TCR2.2=0) 0=do not pulse double-wide in signaling frames 1=do pulse double-wide in signaling frames
TSM	TCR2.3	**TSYNC Mode Select.** 0=frame mode (see the timing in Section 12) 1=multiframe mode (see the timing in Section 12)
TSIO	TCR2.2	**TSYNC I/O Select.** 0=TSYNC is an input 1=TSYNC is an output
D4YM	TCR2.1	**D4 Yellow Alarm Select.** 0=0s in bit 2 of all channels 1=a 1 in the S-bit position of frame 12
B7ZS	TCR2.0	**Bit 7 0 Suppression Enable.** 0=no stuffing occurs 1=Bit 7 force to a 1 in channels with all 0s

OUTPUT PIN TEST MODES Table 3-1

TEST1	TEST0	EFFECT ON OUTPUT PINS
0	0	Operate normally
0	1	Force all output pins 3-state (including all I/O pins and parallel port pins)
1	0	Force all output pins low (including all I/O pins except parallel port pins)
1	1	Force all output pins high (including all I/O pins except parallel port pins)

CCR1: COMMON CONTROL REGISTER 1 (Address=37 Hex)

(MSB)							(LSB)
TESE	ODF	RSAO	TSCLKM	RSCLKM	RESE	PLB	FLB

SYMBOL	POSITION	NAME AND DESCRIPTION
TESE	CCR1.7	**Transmit Elastic Store Enable.** 0=elastic store is bypassed 1=elastic store is enabled
ODF	CCR1.6	**Output Data Format.** 0=bipolar data at TPOS and TNEG 1=NRZ data at TPOS; TNEG=0
RSAO	CCR1.5	**Receive Signaling All ones.** 0=allow robbed signaling bits to appear at RSER 1=force all robbed signaling bits at RSER to 1
TSCLKM	CCR1.4	**TSYSCLK Mode Select.** 0=if TSYSCLK is 1.544 MHz 1=if TSYSCLK is 2.048 MHz
RSCLKM	CCR1.3	**RSYSCLK Mode Select.** 0=if RSYSCLK is 1.544 MHz 1=if RSYSCLK is 2.048 MHz
RESE	CCR1.2	**Receive Elastic Store Enable.** 0=elastic store is bypassed 1=elastic store is enabled
PLB	CCR1.1	**Payload Loopback.** 0=loopback disabled 1=loopback enabled
FLB	CCR1.0	**Framer Loopback.** 0=loopback disabled 1=loopback enabled

PAYLOAD LOOPBACK

When CCR1.1 is set to a one, the DS21Q41B will be forced into Payload LoopBack (PLB). Normally, this loopback is only enabled when ESF framing is being performed. In a PLB situation, the DS21Q41B will loop the 192 bits of payload data (with BPVs corrected) from the receive section back to the transmit section. The FPS framing pattern, CRC6 calculation, and the FDL bits are not looped back; they are reinserted by the DS21Q41B. When PLB is enabled, the following will occur:

1. Data will be transmitted from the TPOS and TNEG pins synchronous with RCLK instead of TCLK.
2. All of the receive side signals will continue to operate normally.
3. The TCHCLK and TCHBLK signals are forced low.
4. Data at the TSER pin is ignored.
5. The TLCLK signal will become synchronous with RCLK instead of TCLK.

FRAMER LOOPBACK

When CCR1.0 is set to a 1, the DS21Q41B will enter a Framer LoopBack (FLB) mode. This loopback is useful in testing and debugging applications. In FLB, the DS21Q41B will loop data from the transmit side back to the receive side. When FLB is enabled, the following will occur:

1. An unframed all 1s code will be transmitted at TPOS and TNEG.
2. Data at RPOS and RNEG will be ignored.
3. All receive side signals will take on timing synchronous with TCLK instead of RCLK.

CCR2: COMMON CONTROL REGISTER 2 (Address=38 Hex)

(MSB)							**(LSB)**
TFM	TB8ZS	TSLC96	TFDL	RFM	RB8ZS	RSLC96	RFDL

SYMBOL	POSITION	NAME AND DESCRIPTION
TFM	CCR2.7	**Transmit Frame Mode Select.** 0=D4 framing mode 1=ESF framing mode
TB8ZS	CCR2.6	**Transmit B8ZS Enable.** 0=B8ZS disabled 1=B8ZS enabled
TSLC96	CCR2.5	**Transmit SLC-96/Fs Bit Insertion Enable.** 0=SLC-96 disabled 1=SLC-96 enabled
TFDL	CCR2.4	**Transmit 0 Stuffer Enable.** 0=0 stuffer disabled 1=0 stuffer enabled
RFM	CCR2.3	**Receive Frame Mode Select.** 0=D4 framing mode 1=ESF framing mode
RB8ZS	CCR2.2	**Receive B8ZS Enable.** 0=B8ZS disabled 1=B8ZS enabled
RSLC96	CCR2.1	**Receive SLC-96 Enable.** 0=SLC-96 disabled 1=SLC-96 enabled
RFDL	CCR2.0	**Receive 0 Destuffer Enable.** 0=0 destuffer disabled 1=0 destuffer enabled

CCR3: COMMON CONTROL REGISTER 3 (Address=30 Hex)

(MSB)							(LSB)
ESMDM	ESR	RLOS	RSMS	PDE	TLD	TLU	-

SYMBOL	POSITION	NAME AND DESCRIPTION
ESMDM	CCR3.7	**Elastic Store Minimum Delay Mode.** See Section 10.3 for details. 0=elastic stores operate at full two-frame depth 1=elastic stores operate at 32-bit depth
ESR	CCR3.6	**Elastic Store Reset.** Setting this bit from a 0 to a 1 will force the elastic stores to a known depth. Should be toggled after RSYSCLK and TSYSCLK have been applied and are stable. Must be cleared and set again for a subsequent reset.
RLOS	CCR3.5	**Function of the RLOS/LOTC Output.** 0=Receive Loss of Sync (RLOS) 1=Loss of Transmit Clock (LOTC)
RSMS	CCR3.4	**RSYNC Multiframe Skip Control.** Useful in framing format conversions from D4 to ESF. 0=RSYNC will output a pulse at every multiframe 1=RSYNC will output a pulse at every other multiframe note: for this bit to have any affect, the RSYNC must be set to output multiframe pulses (RCR2.4=1 and RCR2.3=0).
PDE	CCR3.3	**Pulse Density Enforcer Enable.** 0=disable transmit pulse density enforcer 1=enable transmit pulse density enforcer
TLD	CCR3.2	**Transmit Loop Down Code (001).** 0=transmit data normally 1=replace normal transmitted data with loop down code
TLU	CCR3.1	**Transmit Loop Up Code (00001).** 0=transmit data normally 1=replace normal transmitted data with loop up code
-	CCR3.0	**Not Assigned.** Must be set to 0 when written

LOOP CODE GENERATION

When either the CCR3.1 or CCR3.2 bits are set to one, the DS21Q41B will replace the normal transmitted payload with either the Loop Up or Loop Down code respectively. The DS21Q41B will overwrite the repeating loop code pattern with the framing bits. The SCT will continue to transmit the loop codes as long as either bit is set. It is an illegal state to have both CCR3.1 and CCR3.2 set to 1 at the same time.

PULSE DENSITY ENFORCER

The DS21Q41B always examines both the transmit and receive data streams for violations of the following rules which are required by ANSI T1.403-1989: - no more than 15 consecutive 0s - at least N ones in each and every time window of 8 x (N +1) bits where N=1 through 23. Violations for the transmit and receive data streams are reported in the RIR2.2 and RIR2.1 bits, respectively.

When the CCR3.3 is set to 1, the DS21Q41B will force the transmitted stream to meet this requirement no matter the content of the transmitted stream. When running B8ZS, the CCR3.3 bit should be set to 0 since B8ZS encoded data streams cannot violate the pulse density requirements.

POWER-UP SEQUENCE

On power-up, after the supplies are stable, the DS21Q41B should be configured for operation by writing to all of the internal registers (this includes setting the Test Registers to 00Hex) since the contents of the internal registers cannot be predicted on power-up. Finally, after the TSYSCLK and RSYSCLK inputs are stable, the ESR bit should be toggled from a 0 to a 1 (this step can be skipped if the elastic stores are disabled).

4.0 STATUS AND INFORMATION REGISTERS

There is a set of four registers that contain information on the current real time status of the DS21Q41B, Status Register 1 (SR1), Status Register 2 (SR2), Receive Information Register 1 (RIR1), and Receive Information Register 2 (RIR2). When a particular event has occurred (or is occurring), the appropriate bit in one of these four registers will be set to a 1. All of the bits in these registers operate in a latched fashion. This means that if an event occurs and a bit is set to a 1 in any of the registers, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again or if the alarm(s) is still present.

The user will always precede a read of these registers with a write. The byte written to the register will inform the DS21Q41B which bits the user wishes to read and have cleared. The user will write a byte to one of these four registers, with a 1 in the bit positions he or she wishes to read and a 0 in the bit positions he or she does not wish to obtain the latest information on. When a 1 is written to a bit location, the read register will be updated with current value and it will be cleared. When a 0 is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically AND'ed with the mask byte that was just written and this value should be written back into the same register to insure that the bit does indeed clear. This second write is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. The write-read-write scheme is unique to the four status registers and it allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS21Q41B with higher-order software languages.

The SR1 and SR2 registers have the unique ability to initiate a hardware interrupt via the $\overline{\text{INT}}$ output pin. All four framers within the DS21Q41B share the $\overline{\text{INT}}$ output. Each of the alarms and events in the SR1 and SR2 can be either masked or unmasked from the interrupt pins via the Interrupt Mask Register 1 (IMR1) and Interrupt Mask Register 2 (IMR2) respectively. The user can determine which framer has active interrupts by polling the Interrupt Status Register (ISR).

ISR: INTERRUPT STATUS REGISTER (any unused address)

(MSB)							(LSB)
F3SR2	F3SR1	F2SR2	F2SR1	F1SR2	F1SR1	F0SR2	F0SR1

SYMBOL	POSITION	NAME AND DESCRIPTION
F3SR2	ISR.7	**Status of Interrupt for SR2 in Framer 3.** 1=interrupt active.
F3SR1	ISR.6	**Status of Interrupt for SR1 in Framer 3.** 1=interrupt active.
F2SR2	ISR.5	**Status of Interrupt for SR2 in Framer 2.** 1=interrupt active.
F2SR1	ISR.4	**Status of Interrupt for SR1 in Framer 2.** 1=interrupt active.
F1SR2	ISR.3	**Status of Interrupt for SR2 in Framer 1.** 1=interrupt active.
F1SR1	ISR.2	**Status of Interrupt for SR1 in Framer 1.** 1=interrupt active.
F0SR2	ISR.1	**Status of Interrupt for SR2 in Framer 0.** 1=interrupt active.
F0SR1	ISR.0	**Status of Interrupt for SR1 in Framer 0.** 1=interrupt active.

RIR1: RECEIVE INFORMATION REGISTER 1 (Address=22 Hex)

(MSB)							(LSB)
COFA	8ZD	16ZD	RESF	RESE	SEFE	B8ZS	FBE

SYMBOL	POSITION	NAME AND DESCRIPTION
COFA	RIR1.7	**Change of Frame Alignment.** Set when the last resync resulted in a change of frame or multiframe alignment.
8ZD	RIR1.6	**Eight 0 Detect.** Set when a string of at least eight consecutive 0s (regardless of the length of the string) have been received at RPOS and RNEG.
16ZD	RIR1.5	**Sixteen 0 Detect.** Set when a string of at least 16 consecutive 0s (regardless of the length of the string) have been received at RPOS and RNEG.
RESF	RIR1.4	**Receive Elastic Store Full.** Set when the receive elastic store buffer fills and a frame is deleted.
RESE	RIR1.3	**Receive Elastic Store Empty.** Set when the receive elastic store buffer empties and a frame is repeated.
SEFE	RIR1.2	**Severely Errored Framing Event.** Set when 2 out of 6 framing bits (Ft or FPS) are received in error.
B8ZS	RIR1.1	**B8ZS Code Word Detect.** Set when a B8ZS code word is detected at RPOS and RNEG independent of whether the B8ZS mode is selected or not via CCR2.6. Useful for automatically setting the line coding.
FBE	RIR1.0	**Frame Bit Error.** Set when a Ft (D4) or FPS (ESF) framing bit is received in error.

RIR2: RECEIVE INFORMATION REGISTER 2 (Address=31 Hex)

(MSB)							(LSB)
RLOSC	RCLC	TESF	TESE	TSLIP	RBLC	RPDV	TPDV

SYMBOL	POSITION	NAME AND DESCRIPTION
RLOSC	RIR2.7	**Receive Loss of Sync Clear.** Set when the framer achieves synchronization; will remain set until read.
RCLC	RIR2.6	**Receive Carrier Loss Clear.** Set when the carrier signal is restored; will remain set until read.
TESF	RIR2.5	**Transmit Elastic Store Full.** Set when the transmit elastic store buffer fills and a frame is deleted.
TESE	RIR2.4	**Transmit Elastic Store Empty.** Set when the transmit elastic store buffer empties and a frame is repeated.
TSLIP	RIR2.3	**Transmit Elastic Store Slip Occurrence.** Set when the transmit elastic store has either repeated or deleted a frame.
TBLC	RIR2.2	**Receive Blue Alarm Clear.** Set when the Blue Alarm (AIS) is no longer detected; will remain set until read.
RPDV	RIR2.1	**Receive Pulse Density Violation.** Set when the receive data stream does not meet the ANSI T1.403 requirements for pulse density.
TPDV	RIR2.0	**Transmit Pulse Density Violation.** Set when the transmit data stream does not meet the ANSI T1.403 requirements for pulse density.

SR1: STATUS REGISTER 1 (Address=20 Hex)

(MSB)							(LSB)
LUP	LDN	LOTC	RSLIP	RBL	RYEL	RCL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
LUP	SR1.7	**Loop Up Code Detected.** Set when the repeating ...00001... loop up code is being received.
LDN	SR1.6	**Loop Down Code Detected.** Set when the repeating ...001... loop down code is being received.
LOTC	SR1.5	**Loss of Transmit Clock.** Set when the TCLK pin has not transitioned for one channel time (or 5.2 µs). Will force the RLOS/LOTC pin high if enabled via CCR1.6. Also will force transmit side formatter to switch to RCLK if so enabled via TCR1.7. Based on RCLK.
RSLIP	SR1.4	**Receive Elastic Store Slip Occurrence.** Set when the receive elastic store has either repeated or deleted a frame.
RBL	SR1.3	**Receive Blue Alarm.** Set when an unframed all ones code is received at RPOS and RNEG.
RYEL	SR1.2	**Receive Yellow Alarm.** Set when a yellow alarm is received at RPOS and RNEG.
RCL	SR1.1	**Receive Carrier Loss.** Set when 192 consecutive 0s have been detected at RPOS and RNEG.
RLOS	SR1.0	**Receive Loss of Sync.** Set when the device is not synchronized to the receive T1 stream.

DS21Q41B ALARM SET & CLEAR CRITERIA Table 4-2

ALARM	SET CRITERIA	CLEAR CRITERIA
Blue Alarm (AIS) (see note 1 below)	when over a 3 ms window, five or less 0s are received	when over a 3 ms window, six or more 0s are received
Yellow Alarm (RAI) 1. D4 bit 2 mode (RCR2.2=0)	when bit 2 of 256 consecutive channels is set to 0 for at least 254 occurrences	when bit 2 of 256 consecutive channels is set to 0 for less than 254 occurrences
2. D4 12th F-bit mode (RCR2.2=1; this mode is also referred to as the "Japanese Yellow Alarm")	when the 12th framing bit is set to one for two consecutive occurrences	when the 12th framing bit is set to 0 for two consecutive occurrences
3. ESF mode	when 16 consecutive patterns of 00FF appear in the FDL	when 14 or less patterns of 00FF hex out of 16 possible appear in the FDL
Red Alarm (RCL) (this alarm is also referred to as Loss of Signal)	when 192 consecutive 0s are received	when 14 or more ones out of 112 possible bit positions are received starting with the first one received

NOTES:

1. The definition of Blue Alarm (or Alarm Indication Signal) is an unframed all 1s signal. Blue alarm detectors should be able to operate properly in the presence of a 10-3 error rate and they should not falsely trigger on a framed all 1s signal. The blue alarm criteria in the DS21Q41B has been set to achieve this performance. It is recommended that the RBL bit be qualified with the RLOS bit.

2. ANSI specifications use a different nomenclature than the DS21Q41B does; the following terms are equivalent:

   RBL=AIS
   RCL=LOS
   RLOS=LOF
   RYEL=RAI

LOOP UP/DOWN CODE DETECTION

Bits SR1.7 and SR1.6 will indicate when either the standard “loop up” or “loop down” codes are being received by the DS21Q41B. When a loop up code has been received for 5 seconds, the CPE is expected to loop the recovered data (without correcting BPVs) back to the source. The loop down code indicates that the loopback should be discontinued. See the AT&T publication TR 62411 for more details. The DS21Q41B will detect the loop up/down codes in both framed and unframed circumstances with bit error rates as high as 10**-2. The loop code detector has a nominal integration period of 48 ms. Hence, after about 48 ms of receiving either code, the proper status bit will be set to a 1. After this initial indication, it is recommend that the software poll the DS21Q41B every 100 ms to 500 ms until 5 seconds has elapsed to insure that the code is continuously present.

SR2: STATUS REGISTER 2 (Address=21 Hex)

(MSB)							(LSB)
RMF	TMF	SEC	RFDL	TFDL	RMTCH	RAF	LORC

SYMBOL	POSITION	NAME AND DESCRIPTION
RMF	SR2.7	**Receive Multiframe**. Set on receive multiframe boundaries.
TMF	SR2.6	**Transmit Multiframe.** Set on transmit multiframe boundaries.
SEC	SR2.5	**1-Second Timer.** Set on increments of 1 second based on RCLK; will be set in increments of 999 ms, 999 ms, and 1002 ms every 3 seconds.
RFDL	SR2.4	**Receive FDL Buffer Full.** Set when the receive FDL buffer (RFDL) fills to capacity (8 bits).
TFDL	SR2.3	**Transmit FDL Buffer Empty.** Set when the transmit FDL buffer (TFDL) empties.
RMTCH	SR2.2	**Receive FDL Match Occurrence.** Set when the RFDL matches either RFDLM1 or RFDLM2.
RAF	SR2.1	**Receive FDL Abort.** Set when eight consecutive 1s are received in the FDL.
LORC	SR2.0	**Loss of Receive Clock.** Set when the RCLK pin has not transitioned for at least 2 μs (3 μs ± 1 μs).

IMR1: INTERRUPT MASK REGISTER (Address=7F Hex)

(MSB)							(LSB)
LUP	LDN	LOTC	SLIP	RBL	RYEL	RCL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
LUP	IMR1.7	**Loop Up Code Detected.** 0=interrupt masked 1=interrupt enabled
LDN	IMR1.6	**Loop Down Code Detected.** 0=interrupt masked 1=interrupt enabled
LOTC	IMR1.5	**Loss of Transmit Clock.** 0=interrupt masked 1=interrupt enabled
SLIP	IMR1.4	**Elastic Store Slip Occurrence.** 0=interrupt masked 1=interrupt enabled
RBL	IMR1.3	**Receive Blue Alarm.** 0=interrupt masked 1=interrupt enabled
RYEL	IMR1.2	**Receive Yellow Alarm.** 0=interrupt masked 1=interrupt enabled
RCL	IMR1.1	**Receive Carrier Loss.** 0=interrupt masked 1=interrupt enabled
RLOS	IMR1.0	**Receive Loss of Sync.** 0=interrupt masked 1=interrupt enabled

IMR2: INTERRUPT MASK REGISTER 2 (Address=6F Hex)

(MSB)							(LSB)
RMF	TMF	SEC	RFDL	TFDL	RMTCH	RAF	LORC

SYMBOL	POSITION	NAME AND DESCRIPTION
RMF	IMR2.7	**Receive Multiframe.** 0=interrupt masked 1=interrupt enabled
TMF	IMR2.6	**Transmit Multiframe.** 0=interrupt masked 1=interrupt enabled
SEC	IMR2.5	**One Second Timer.** 0=interrupt masked 1=interrupt enabled
RFDL	IMR2.4	**Receive FDL Buffer Full.** 0=interrupt masked 1=interrupt enabled
TFDL	IMR2.3	**Transmit FDL Buffer Empty.** 0=interrupt masked 1=interrupt enabled
RMTCH	IMR2.2	**Receive FDL Match Occurrence.** 0=interrupt masked 1=interrupt enabled
RAF	IMR2.1	**Receive FDL Abort.** 0=interrupt masked 1=interrupt enabled
LORC	IMR2.0	**Loss of Receive Clock.** 0=interrupt masked 1=interrupt enabled

5.0 ERROR COUNT REGISTERS

There are a set of three counters in the DS21Q41B that record bipolar violations, excessive 0s, errors in the CRC6 code words, framing bit errors, and number of multiframes that the device is out of receive synchronization. Each of these three counters are automatically updated on 1-second boundaries as determined by the one second timer in Status Register 2 (SR2.5). Hence, these registers contain performance data from the previous second. The user can use the interrupt from the 1-second timer to determine when to read these registers. The user has a full second to read the counters before the data is lost. All three counters will saturate at their respective maximum counts and they will not rollover (note: only the Line Code Violation Count Register has the potential to overflow).

5.1 Line Code Violation Count Register (LCVCR)

Line Code Violation Count Register 1 High (LCVCR1) is the most significant word and LCVCR2 is the least significant word of a 16-bit counter that records code violations (CVs). CVs are defined as Bipolar Violations (BPVs) or excessive 0s. See Table 5-1 for details of exactly what the LCVCRs count. If the B8ZS mode is set for the receive side via CCR2.2, then B8ZS code words are not counted. This counter is always enabled; it is not disabled during receive loss of synchronization (RLOS=1) conditions.

LCVCR1: LINE CODE VIOLATION COUNT REGISTER 1 (Address=23 Hex)
LCVCR2: LINE CODE VIOLATION COUNT REGISTER 2 (Address=24 Hex)

(MSB)							(LSB)	
LCV15	LCV14	LCV13	LCV12	LCV11	LCV10	LCV9	LCV8	LCVCR1
LCV7	LCV6	LCV5	LCV4	LCV3	LCV2	LCV1	LCV0	LCVCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
CV16	LCVCR1.7	MSB of the 16-bit code violation count
CV0	LCVCR2.0	LSB of the 16-bit code violation count

LINE CODE VIOLATION COUNTING ARRANGEMENTS Table 5-1

COUNT EXCESSIVE 0S? (RCR1.7)	B8ZS ENABLED? (CCR2.2)	WHAT IS COUNTED IN THE LCVCRs
no	no	BPVs
yes	no	BPVs + 16 consecutive 0s
no	yes	BPVs (B8ZS code words not counted)
yes	yes	BPVs + 8 consecutive 0s

5.2 Path Code Violation Count Register (PCVCR)

When the receive side of the DS21Q41B is set to operate in the ESF framing mode (CCR2.3=1), PCVCR will automatically be set as a 12-bit counter that will record errors in the CRC6 code words. When set to operate in the D4 framing mode (CCR2.3=0), PCVCR will automatically count errors in the Ft framing bit position. Via the RCR2.1 bit, the DS21Q41B can be programmed to also report errors in the Fs framing bit position. The PCVCR will be disabled during receive loss of synchronization (RLOS=1) conditions. See Table 5-2 for a detailed description of exactly what errors the PCVCR counts.

PCVCR1: PATH VIOLATION COUNT REGISTER 1 (Address=25 Hex)
PCVCR2: PATH VIOLATION COUNT REGISTER 2 (Address=26 Hex)

(MSB)							(LSB)	
(note 1)	(note 1)	(note 1)	(note 1)	CRC/FB11	CRC/FB10	CRC/FB9	CRC/FB8	PCVCR1
CRC/FB7	CRC/FB6	CRC/FB5	CRC/FB4	CRC/FB3	CRC/FB2	CRC/FB1	CRC/FB0	PCVCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
CRC/FB11	PCVCR1.3	MSB of the 12-bit CRC6 error or frame bit error count (note 2)
CRC/FB0	PCVCR2.0	LSB of the 12-bit CRC6 error or frame bit error count (note 2)

NOTES:

1. The upper nibble of the counter at address 25 is used by the Multiframes Out of Sync Count Register.
2. PCVCR counts either errors in CRC code words (in the ESF framing mode; CCR2.3=1) or errors in the framing bit position (in the D4 framing mode; CCR2.3=0).

PATH CODE VIOLATION COUNTING ARRANGEMENTS Table 5-2

FRAMING MODE (CCR2.3)	COUNT Fs ERRORS? (RCR2.1)	WHAT IS COUNTED IN THE PCVCRs
D4	no	errors in the Ft pattern
D4	yes	errors in both the Ft and Fs patterns
ESF	don't care	errors in the CRC6 code words

5.3 Multiframes Out of Sync Count Register (MOSCR)

Normally the MOSCR is used to count the number of multiframes that the receive synchronizer is out of sync (RCR2.0=1). This number is useful in ESF applications needing to measure the parameters Loss Of Frame Count (LOFC) and ESF Error Events as described in AT&T publication TR54016. When the MOSCR is operated in this mode, it is not disabled during receive loss of synchronization (RLOS=1) conditions. The MOSCR has alternate operating mode whereby it will count either errors in the Ft framing pattern (in the D4 mode) or errors in the FPS framing pattern (in the ESF mode). When the MOSCR is operated in this mode, it is disabled during receive loss of synchronization (RLOS=1) conditions. See Table 5-3 for a detailed description of what the MOSCR is capable of counting.

MOSCR1:
MULTIFRAMES OUT OF SYNC COUNT REGISTER 1 (Address=25 Hex)
MOSCR2:
MULTIFRAMES OUT OF SYNC COUNT REGISTER 2 (Address=27 Hex)

(MSB)							(LSB)	
MOS/FB11	MOS/FB10	MOS/FB9	MOS/FB8	(note 1)	(note 1)	(note 1)	(note 1)	MOSCR1
MOS/FB7	MOS/FB6	MOS/FB5	MOS/FB4	MOS/FB3	MOS/FB2	MOS/FB1	MOS/FB0	MOSCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
MOS/FB11	MOSCR1.7	MSB of the 12-Bit multiframes out of sync or F-bit error count (note 2)
MOS/FB0	MOSCR2.0	LSB of the 12-bit multiframes out of sync or F-bit error count (note 2)

NOTES:
1. The lower nibble of the counter at address 25 is used by the Path Code Violation Count Register.
2. MOSCR counts either errors in framing bit position (RCR2.0=0) or the number of multiframes out of sync (RCR2.0=1).

MULTIFRAMES OUT OF SYNC COUNTING ARRANGEMENTS Table 5-3

FRAMING MODE (CCR2.3)	COUNT MOS OR F-BIT ERRORS? (RCR2.0)	WHAT IS COUNTED IN THE MOSCRs
D4	MOS	number of multiframes out of sync
D4	F-BIT	errors in the Ft pattern
ESF	MOS	number of multiframes out of sync
ESF	F-BIT	errors in the FPS pattern

6.0 FDL/Fs EXTRACTION AND INSERTION
The DS21Q41B has the ability to extract/insert data from/into the Facility Data Link (FDL) in the ESF framing mode and from/into Fs bit position in the D4 framing mode. Since SLC-96 utilizes the Fs bit position, this capability can also be used in SLC-96 applications. The operation of the receive and transmit sections will be discussed separately. Contact the factory for a copy of C language source code for implementing the FDL on the DS21Q41B.

6.1 Receive Section
In the receive section, the recovered FDL bits or Fs bits are shifted bit-by-bit into the Receive FDL register (RFDL). Since the RFDL is 8 bits in length, it will fill up every 2 ms (8 times 250 µs). The DS21Q41B will signal an external microcontroller that the buffer has filled via the SR2.4 bit. If enabled via IMR2.4, the $\overline{\text{INT}}$ pin will toggle low indicating that the buffer has filled and needs to be read. The user has 2 ms to read this data before it is lost. If the byte in the RFDL matches either of the bytes programmed into the RFDLM1 or RFDLM2 registers, then the SR2.2 bit will be set to a 1 and the $\overline{\text{INT}}$ pin will toggled low if enabled via IMR2.2. This feature allows an external microcontroller to ignore the FDL or Fs pattern until an important event occurs.

The DS21Q41B also contains a 0 destuffer which is controlled via the CCR2.0 bit. In both ANSI T1.403 and TR54016, communications on the FDL follows a subset of a LAPD protocol. The LAPD protocol states that no more than five 1s should be transmitted in a row so that the data does not resemble an opening or closing flag (01111110) or an abort signal (11111111). If enabled via CCR2.0, the DS21Q41B will automatically look for five 1s in a row, followed by a 0. If it finds such a pattern, it will automatically remove the 0. If the 0 destuffer sees six or more 1s in a row followed by a 0, the 0 is not removed. The CCR2.0 bit should always be set to a 1 when the DS21Q41B is extracting the FDL. More on how to use the DS21Q41B in FDL applications is covered in a separate Application Note.

RFDL: RECEIVE FDL REGISTER (Address=28 Hex)

(MSB)							**(LSB)**
RFDL7	RFDL6	RFDL5	RFDL4	RFDL3	RFDL2	RFDL1	RFDL0

SYMBOL	POSITION	NAME AND DESCRIPTION
RFDL7	RFDL.7	MSB of the received FDL code
RFDL0	RFDL.0	LSB of the received FDL code

The Receive FDL Register (RFDL) reports the incoming Facility Data Link (FDL) or the incoming Fs bits. The LSB is received first.

RFDLM1: RECEIVE FDL MATCH REGISTER 1 (Address=29 Hex)
RFDLM2: RECEIVE FDL MATCH REGISTER 2 (Address=2A Hex)

(MSB)							**(LSB)**
RFDL7	RFDL6	RFDL5	RFDL4	RFDL3	RFDL2	RFDL1	RFDL0

SYMBOL	POSITION	NAME AND DESCRIPTION
RFDL7	RFDL.7	MSB of the FDL match code
RFDL0	RFDL.0	LSB of the FDL match code

When the byte in the Receive FDL Register matches either of the two Receive FDL Match Registers (RFDLM1/RFDLM2), RSR2.2 will be set to a 1 and the $\overline{\text{INT}}$ will go active if enabled via IMR2.2.

6.2 Transmit Section

The transmit section will shift out into the T1 data stream, either the FDL (in the ESF framing mode) or the Fs bits (in the D4 framing mode) contained in the Transmit FDL register (TFDL). When a new value is written to the TFDL, it will be multiplexed serially (LSB first) into the proper position in the outgoing T1 data stream. After the full 8 bits have been shifted out, the DS21Q41B will signal the host microcontroller that the buffer is empty and that more data is needed by setting the SR2.3 bit to a 1. The $\overline{\text{INT}}$ will also toggle low if enabled via IMR2.3. The user has 2 ms (1.5 ms in SLC-96 applications) to update the TFDL with a new value. If the TFDL is not updated, the old value in the TFDL will be transmitted once again.

The DS21Q41B also contains a 0 stuffer which is controlled via the CCR2.4 bit. In both ANSI T1.403 and TR54016, communications on the FDL follows a subset of a LAPD protocol. The LAPD protocol

states that no more than five 1s should be transmitted in a row so that the data does not resemble an opening or closing flag (01111110) or an abort signal (11111111). If enabled via CCR2.4, the DS21Q41B will automatically look for five 1s in a row.

If it finds such a pattern, it will automatically insert a 0 after the five ones. The CCR2.4 bit should always be set to a 1 when the DS21Q41B is inserting the FDL. More on how to use the DS21Q41B in FDL applications is covered in a separate Application Note.

TFDL: TRANSMIT FDL REGISTER (Address=7E Hex)

(MSB)							**(LSB)**
TFDL7	TFDL6	TFDL5	TFDL4	TFDL3	TFDL2	TFDL1	TFDL0

SYMBOL	POSITION	NAME AND DESCRIPTION
TFDL7	TFDL.7	MSB of the FDL code to be transmitted
TFDL0	TFDL.0	LSB of the FDL code to be transmitted

The Transmit FDL Register (TFDL) contains the Facility Data Link (FDL) information that is to be inserted on a byte basis into the outgoing T1 data stream. The LSB is transmitted first.

7.0 SIGNALING OPERATION

The robbed bit signaling bits in embedded in the T1 stream can be extracted from the receive stream and inserted into the transmit stream by the DS21Q41B. There is a set of 12 registers for the receive side (RS1 to RS12) and 12 registers on the transmit side (TS1 to TS12). The signaling registers are detailed below. The CCR1.5 bit is used to control the robbed signaling bits as they appear at RSER. If CCR1.5 is set to 0, then the robbed signaling bits will appear at RSER in their proper position as they are received. If CCR1.5 is set to a 1, then the robbed signaling bit positions will be forced to a 1 at RSER.

RS1 TO RS12: RECEIVE SIGNALING REGISTERS (Address=60 to 6B Hex)

(MSB)							(LSB)	
A(8)	A(7)	A(6)	A(5)	A(4)	A(3)	A(2)	A(1)	RS1 (60)
A(16)	A(15)	A(14)	A(13)	A(12)	A(11)	A(10)	A(9)	RS2 (61)
A(24)	A(23)	A(22)	A(21)	A(20)	A(19)	A(18)	A(17)	RS3 (62)
B(8)	B(7)	B(6)	B(5)	B(4)	B(3)	B(2)	B(1)	RS4 (63)
B(16)	B(15)	B(14)	B(13)	B(12)	B(11)	B(10)	B(9)	RS5 (64)
B(24)	B(23)	B(22)	B(21)	B(20)	B(19)	B(18)	B(17)	RS6 (65)
A/C(8)	A/C(7)	A/C(6)	A/C(5)	A/C(4)	A/C(3)	A/C(2)	A/C(1)	RS7 (66)
A/C(16)	A/C(15)	A/C(14)	A/C(13)	A/C(12)	A/C(11)	A/C(10)	A/C(9)	RS8 (67)
A/C(24)	A/C(23)	A/C(22)	A/C(21)	A/C(20)	A/C(19)	A/C(18)	A/C(17)	RS9 (68)
B/D(8)	B/D(7)	B/D(6)	B/D(5)	B/D(4)	B/D(3)	B/D(2)	B/D(1)	RS10 (69)
B/D(16)	B/D(15)	B/D(14)	B/D(13)	B/D(12)	B/D(11)	B/D(10)	B/D(9)	RS11 (6A)
B/D(24)	B/D(23)	B/D(22)	B/D(21)	B/D(20)	B/D(19)	B/D(18)	B/D(17)	RS12 (6B)

SYMBOL	POSITION	NAME AND DESCRIPTION
D(24)	RS12.7	Signaling Bit D in Channel 24
A(1)	RS1.0	Signaling Bit A in Channel 1

Each Receive Signaling Register (RS1 to RS12) reports the incoming robbed bit signaling from eight DS0 channels. In the ESF framing mode, there can be up to four signaling bits per channel (A, B, C, and D). In the D4 framing mode, there are only two signaling bits per channel (A and B). In the D4 framing mode, the DS21Q41B will replace the C and D signaling bit positions with the A and B signaling bits from the previous multiframe. Hence, whether the DS21Q41B is operated in either framing mode, the user needs only to retrieve the signaling bits every 3 ms. The bits in the Receive Signaling Registers are updated on multiframe boundaries in both framing modes so the user can utilize the Receive Multiframe Interrupt in the Receive Status Register 2 (SR2.7) to know when to retrieve the signaling bits. The Receive Signaling Registers are frozen and not updated during a loss of sync condition (SR1.0=1). They will contain the most recent signaling information before the “OOF” occurred.

TS1 TO TS12: TRANSMIT SIGNALING REGISTERS (Address=70 to 7B Hex)

(MSB)							(LSB)	
A(8)	A(7)	A(6)	A(5)	A(4)	A(3)	A(2)	A(1)	TS1 (70)
A(16)	A(15)	A(14)	A(13)	A(12)	A(11)	A(10)	A(9)	TS2 (71)
A(24)	A(23)	A(22)	A(21)	A(20)	A(19)	A(18)	A(17)	TS3 (72)
B(8)	B(7)	B(6)	B(5)	B(4)	B(3)	B(2)	B(1)	TS4 (73)
B(16)	B(15)	B(14)	B(13)	B(12)	B(11)	B(10)	B(9)	TS5 (74)
B(24)	B(23)	B(22)	B(21)	B(20)	B(19)	B(18)	B(17)	TS6 (75)
A/C(8)	A/C(7)	A/C(6)	A/C(5)	A/C(4)	A/C(3)	A/C(2)	A/C(1)	TS7 (76)
A/C(16)	A/C(15)	A/C(14)	A/C(13)	A/C(12)	A/C(11)	A/C(10)	A/C(9)	TS8 (77)
A/C(24)	A/C(23)	A/C(22)	A/C(21)	A/C(20)	A/C(19)	A/C(18)	A/C(17)	TS9 (78)
B/D(8)	B/D(7)	B/D(6)	B/D(5)	B/D(4)	B/D(3)	B/D(2)	B/D(1)	TS10 (79)
B/D(16)	B/D(15)	B/D(14)	B/D(13)	B/D(12)	B/D(11)	B/D(10)	B/D(9)	TS11 (7A)
B/D(24)	B/D(23)	B/D(22)	B/D(21)	B/D(20)	B/D(19)	B/D(18)	B/D(17)	TS12 (7B)

SYMBOL	POSITION	NAME AND DESCRIPTION
D(24)	TS12.7	Signaling Bit D in Channel 24
A(1)	TS1.0	Signaling Bit A in Channel 1

Each Transmit Signaling Register (TS1 to TS12) contains the Robbed Bit signaling for eight DS0 channels that will be inserted into the outgoing stream if enabled to do so via TCR1.4. In the ESF framing mode, there can be up to four signaling bits per channel (A, B, C, and D). On multiframe boundaries, the DS21Q41B will load the values present in the Transmit Signaling Register into an outgoing signaling shift register that is internal to the device. The user can utilize the Transmit Multiframe Interrupt in Status Register 2 (SR2.6) to know when to update the signaling bits. In the ESF framing mode, the interrupt will come every 3 ms and the user has a full 3 ms to update the TSRs. In the D4 framing mode, there are only two framing bits per channel (A and B). However in the D4 framing mode, the DS21Q41B uses the C and D-bit positions as the A and B bit positions for the next multiframe. The DS21Q41B will load the values in the TSRs into the outgoing shift register every other D4 multiframe.

8.0 SPECIAL TRANSMIT SIDE REGISTERS

There is a set of seven registers in the DS21Q41B that can be used to custom tailor the data that is to be transmitted onto the T1 line, on a channel by channel basis. Each of the 24 T1 channels can be either forced to be transparent or to have a user defined idle code inserted into them. Each of these special registers is defined below.

TTR1/TTR2/TTR3: TRANSMIT TRANSPARENCY REGISTERS (Address=39 to 3B Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TTR1 (29)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TTR2 (3A)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TTR3 (3B)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TTR3.7	**Transmit Transparency Registers.** 0=this DS0 channel is not transparent
CH1	TTR1.0	1=this DS0 channel is transparent

Each of the bit positions in the Transmit Transparency Registers (TTR1/TTR2/TTR3) represent a DS0 channel in the outgoing frame. When these bits are set to a 1, the corresponding channel is transparent (or clear). If a DS0 is programmed to be clear, no robbed bit signaling will be inserted nor will the channel have Bit 7 stuffing performed. However, in the D4 framing mode, bit 2 will be overwritten by a 0 when a Yellow Alarm is transmitted. Also the user has the option to prevent the TTR registers from determining which channels are to have Bit 7 stuffing performed. If the TCR2.0 and TCR1.3 bits are set to 1, then all 24 T1 channels will have Bit 7 stuffing performed on them regardless of how the TTR registers are programmed. In this manner, the TTR registers are only affecting which channels are to have robbed bit signaling inserted into them. Please see Figure 13-9 for more details.

TIR1/TIR2/TIR3: TRANSMIT IDLE REGISTERS (Address=3C to 3E Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TIR1 (3C)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TIR2 (3D)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TIR3 (3E)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TIR3.7	**Transmit Idle Registers.** 0=do not insert the Idle Code into this DS0 channel
CH1	TIR1.0	1=insert the Idle Code into this channel

TIDR: TRANSMIT IDLE DEFINITION REGISTER (Address=3F Hex)

(MSB)							(LSB)
TIDR7	TIDR6	TIDR5	TIDR4	TIDR3	TIDR2	TIDR1	TIDR0

SYMBOL	POSITION	NAME AND DESCRIPTION
TIDR7	TIDR.7	MSB of the Idle Code
TIDR0	TIDR.0	LSB of the Idle Code

Each of the bit positions in the Transmit Idle Registers (TIR1/TIR2/TIR3) represent a DS0 channel in the outgoing frame. When these bits are set to a 1, the corresponding channel will transmit the Idle Code contained in the Transmit Idle Definition Register (TIDR). Robbed bit signaling and Bit 7 stuffing will occur over the programmed Idle Code unless the DS0 channel is made transparent by the Transmit Transparency Registers.

9.0 CLOCK BLOCKING REGISTERS

The Receive Channel Blocking Registers (RCBR1/RCBR2/RCBR3) and the Transmit Channel Blocking Registers (TCBR1/TCBR2/TCBR3) control the RCHBLK and TCHBLK pins respectively. The RCHBLK and TCHCLK pins are user-programmable outputs that can be forced either high or low during individual channels. These outputs can be used to block clocks to a USART or LAPD controller in Fractional T1 or ISDN-PRI applications. When the appropriate bits are set to a 1, the RCHBLK and TCHCLK pins will be held high during the entire corresponding channel time. See the timing in Section 12 for an example.

RCBR1/RCBR2/RCBR3:
RECEIVE CHANNEL BLOCKING REGISTERS (Address=6C to 6E Hex)

(MSB) **(LSB)**

CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RCBR1 (6C)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RCBR2 (6D)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RCBR3 (6E)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	RCBR3.7	**Receive Channel Blocking Registers.** 0=force the RCHBLK pin to remain low during this channel time
CH1	RCBR1.0	1=force the RCHBLK pin high during this channel time

TCBR1/TCBR2/TCBR3:
TRANSMIT CHANNEL BLOCKING REGISTERS (Address=32 to 34 Hex)

(MSB) **(LSB)**

CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TCBR1 (32)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TCBR2 (33)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TCBR3 (34)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TCBR3.7	**Transmit Channel Blocking Registers.** 0=force the TCHBLK pin to remain low during this channel time
CH1	TCBR1.0	1=force the TCHBLK pin high during this channel time

10.0 ELASTIC STORES OPERATION

Each framer within the DS21Q41B contains dual two-frame (386 bits) elastic stores, one for the receive direction, and one for the transmit direction. These elastic stores have two main purposes. First, they can be used to rate convert the T1 data stream to 2.048 Mbps (or a multiple of 2.048 Mbps) which is the E1 rate. Secondly, they can be used to absorb the differences in frequency and phase between the T1 data stream and an asynchronous (i.e., not frequency locked) backplane clock (which can be 1.544 MHz or 2.048 MHz). Both elastic stores contain full controlled slip capability which is necessary for this second purpose. The receive side elastic store can be enabled via CCR1.2 and the transmit side elastic store is enabled via CCR1.7. The elastic stores can be forced to a known depth via the Elastic Store Reset bit (CCR3.6). Toggling the CCR3.6 bit forces the read and write pointers into opposite frames. Both elastic stores within the DS21Q41B are fully independent and no restrictions apply to the sourcing of the various clocks that are applied to them. The transmit side elastic store can be enabled whether the receive elastic store is enabled or disabled and vice versa. Also, each elastic store can interface to either a 1.544 MHz or 2.048 MHz backplane without regard to the backplane rate the other elastic store is interfacing.

10.1 Receive Side

If the receive side elastic store is enabled (CCR1.2=1), then the user must provide either a 1.544 MHz (CCR1.3=0) or 2.048 MHz (CCR1.3=1) clock at the RSYSCLK pin. The user has the option of either providing a frame sync at the RSYNC pin (RCR2.3=1) or having the RSYNC pin provide a pulse on frame boundaries (RCR2.3=0). If the user wishes to obtain pulses at the frame boundary, then RCR2.4 must be set to 0, and if the user wishes to have pulses occur at the multiframe boundary, then RCR2.4 must be set to 1. The DS21Q41B will always indicate frame boundaries via the RFSYNC output whether the elastic store is enabled or not. If the elastic store is enabled, then multiframe boundaries will be indicated via the RMSYNC output. If the user selects to apply a 2.048 MHz clock to the SYSCLK pin, then the data output at RSER will be forced to all 1s every fourth channel and the F-bit will be deleted. Hence channels 1, 5, 9, 13, 17, 21, 25, and 29 (timeslots 0, 4, 8, 12, 16, 20, 24, and 28) will be forced to a 1. Also, in 2.048 MHz applications, the RCHBLK output will be forced high during the same channels as the RSER pin. See Section 12 for more details. This is useful in T1 to CEPT (E1) conversion applications. If the 386-bit elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties, then a full frame of data (193 bits) will be repeated at RSER and the SR1.4 and RIR1.3 bits will be set to a 1. If the buffer fills, then a full frame of data will be deleted and the SR1.4 and RIR1.4 bits will be set to a 1.

10.2 Transmit Side

The operation of the transmit elastic store is very similar to the receive side. The transmit side elastic store is enabled via CCR1.7. A 1.544 MHz (CCR1.4=0) or 2.048 MHz (CCR1.4=1) clock can be applied to the TSYSCLK input. If the user selects to apply a 2.048 MHz clock to the TSYSCLK pin, then the data output at TSER will be ignored every fourth channel. Hence channels 1, 5, 9, 13, 17, 21, 25, and 29 (timeslots 0, 4, 8, 12, 16, 20, 24, and 28) will be ignored. The user must supply a 8 kHz frame sync pulse to the TFSYNC input. Also, in 2.048 MHz applications the TCHBLK output will be forced high during the channels ignored by the DS21Q41B. See Section 12 for more details. Controlled slips in the transmit elastic store are reported in the RIR2.3 bit and the direction of the slip is reported in the RIR2.5 and RIR2.4 bits.

10.3 Minimum Delay Synchronous SYSCLK Mode

In applications where the DS21Q41B is connected to backplanes that are frequency locked to the recovered T1 clock (i.e., the RCLK output), the full two-frame depth of the onboard elastic stores is really not needed. In fact, in some delay sensitive applications, the normal two-frame depth may be excessive. If the CCR3.7 bit is set to 1, then the receive elastic store (and also the transmit elastic store if it is enabled) will be forced to a maximum depth of 32 bits instead of the normal 386 bits. In this mode, RSYSCLK

and TSYSCLK must be tied together and they must be frequency locked to RCLK. All of the slip contention logic in the DS21Q41B is disabled (since slips cannot occur). Also, since the buffer depth is no longer two frames deep, the DS21Q41B must be set up to source either a frame pulse at the RSYNC pin and this output must be tied to the TFSYNC input. On power-up after the RSYSCLK and TSYSCLK signals have locked to the RCLK signal, the elastic store reset bit (CCR3.6) should be toggled from a 0 to a 1 to insure proper operation.

11.0 RECEIVE MARK REGISTERS

The DS21Q41B has the ability to replace the incoming data, on a channel-by-channel basis with either an idle code (7F Hex) or the digital milliwatt code which is a 8-byte repeating pattern that represents a 1 kHz sine wave (1E/0B/0B/1E/9E/8B/8B/9E). The RCR2.7 bit will determine which code is used. Each bit in the RMRs, represents a particular channel. If a bit is set to a one, then the receive data in that channel will be replaced with one of the two codes. If a bit is set to 0, no replacement occurs.

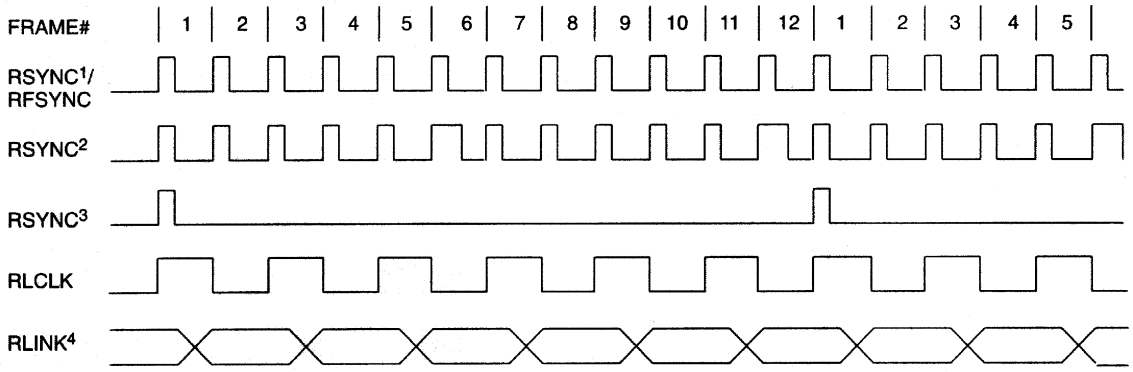
RMR1/RMR2/RMR3: RECEIVE MARK REGISTERS (Address=2D to 2F Hex)

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RMR1 (2D)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RMR2 (2E)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RMR3 (2F)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	RCBR3.7	**Receive Channel Blocking Registers.** 0=do not affect the receive data associated with this channel
CH1	RCBR1.0	1=replace the receive data associated with this channel with either the idle code or the digital milliwatt code (depends on the (RCR2.7 bit)

12.0 TIMING DIAGRAMS

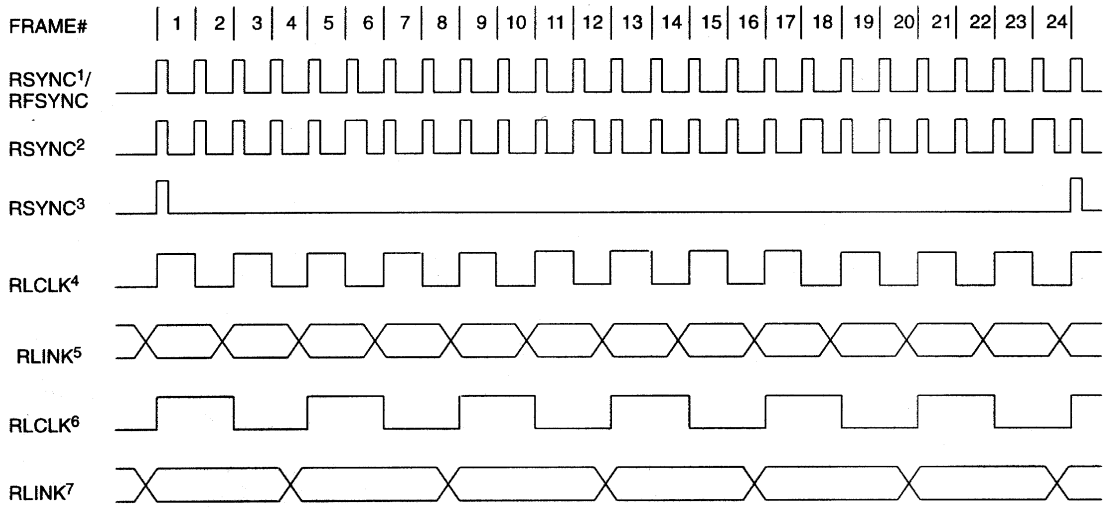
RECEIVE SIDE D4 TIMING Figure 12-1



NOTES:

1. RSYNC in the frame mode (RCR2.4=0) and double-wide frame sync is not enabled (RCR2.5=0).
2. RSYNC in the frame mode (RCR2.4=0) and double-wide frame sync is enabled (RCR2.5=1).
3. RSYNC in the multiframe mode (RCR2.4=1).
4. RLINK data (S-bit) is updated one bit prior to even frames and held for two frames.
5. RLINK and RLCLK are not synchronous with RSYNC when the receive side elastic store is enabled.

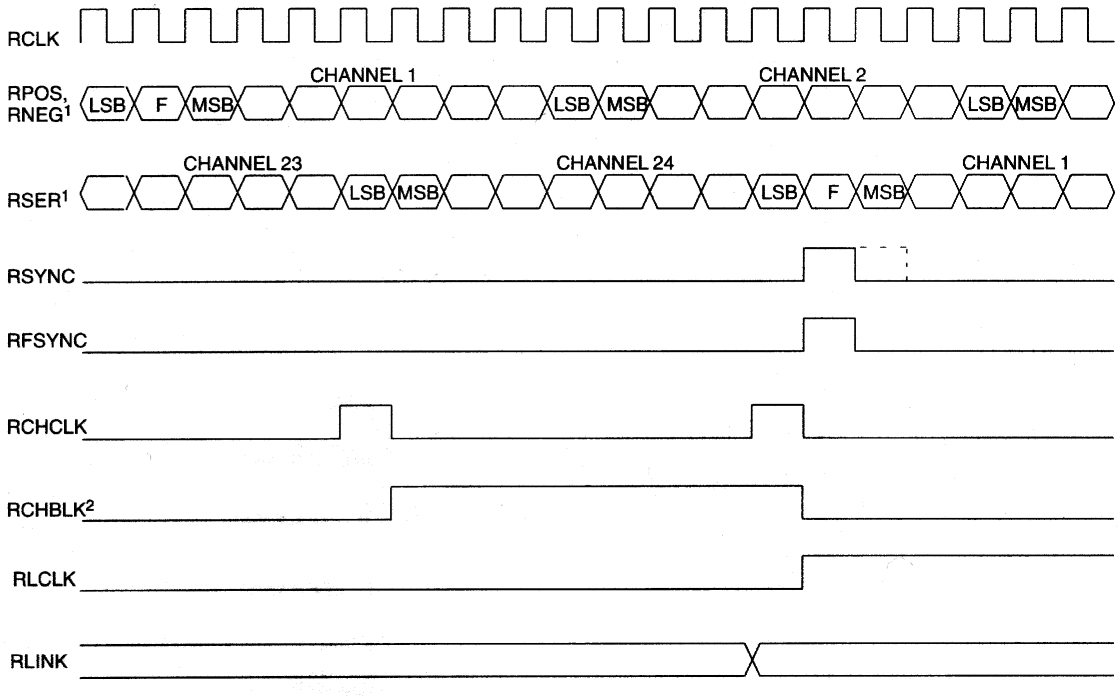
RECEIVE SIDE ESF TIMING Figure 12-2



NOTES:

1. RSYNC in the frame mode (RCR2.4=0) and double-wide frame sync is not enabled (RCR2.5=0).
2. RSYNC in the frame mode (RCR2.4=0) and double-wide frame sync is enabled (RCR2.5=1).
3. RSYNC in the multiframe mode (RCR2.4=1).
4. ZBTSI mode disabled (RCR2.6=0).
5. RLINK data (FDL bits) is updated 1 bit-time before odd frames and held for two frames.
6. ZBTSI mode is enabled (RCR2.6=1).
7. RLINK data (Z-bits) is updated 1 bit-time before odd frame and held for four frames.
8. RLINK and RLCLK are not synchronous with RSYNC when the receive side elastic store is enabled.

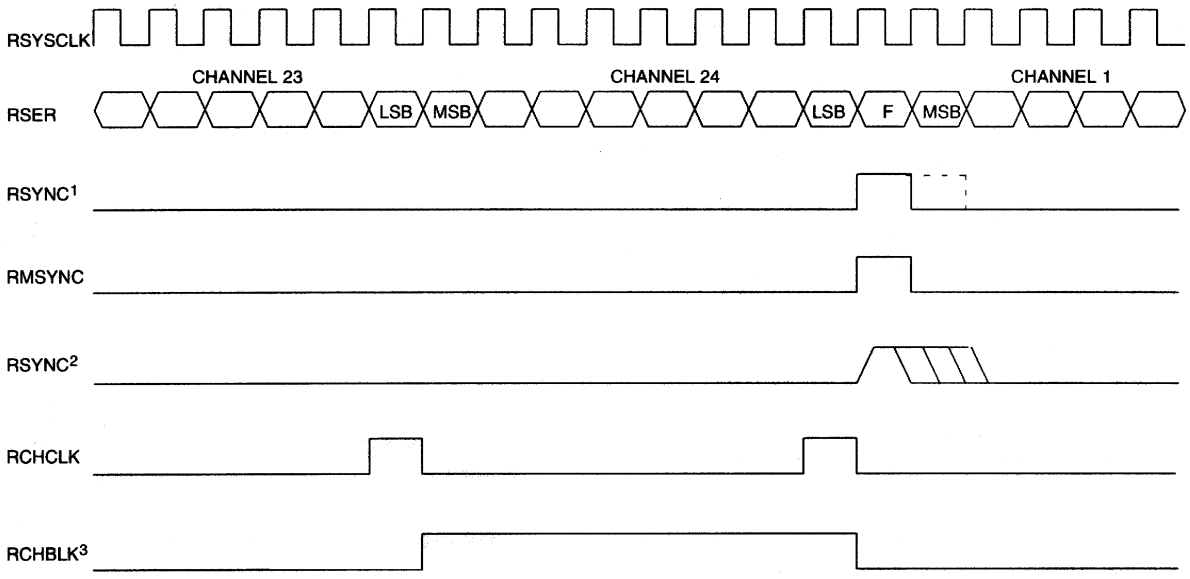
RECEIVE SIDE BOUNDARY TIMING (WITH ELASTIC STORE DISABLED) Figure 12-3



NOTES:

1. There is a 13 RCLK delay from RPOS/RNEG to RSER.
2. RCHBLK is programmed to block channel 24.
3. Boundary timing shown is for the ESF framing mode.

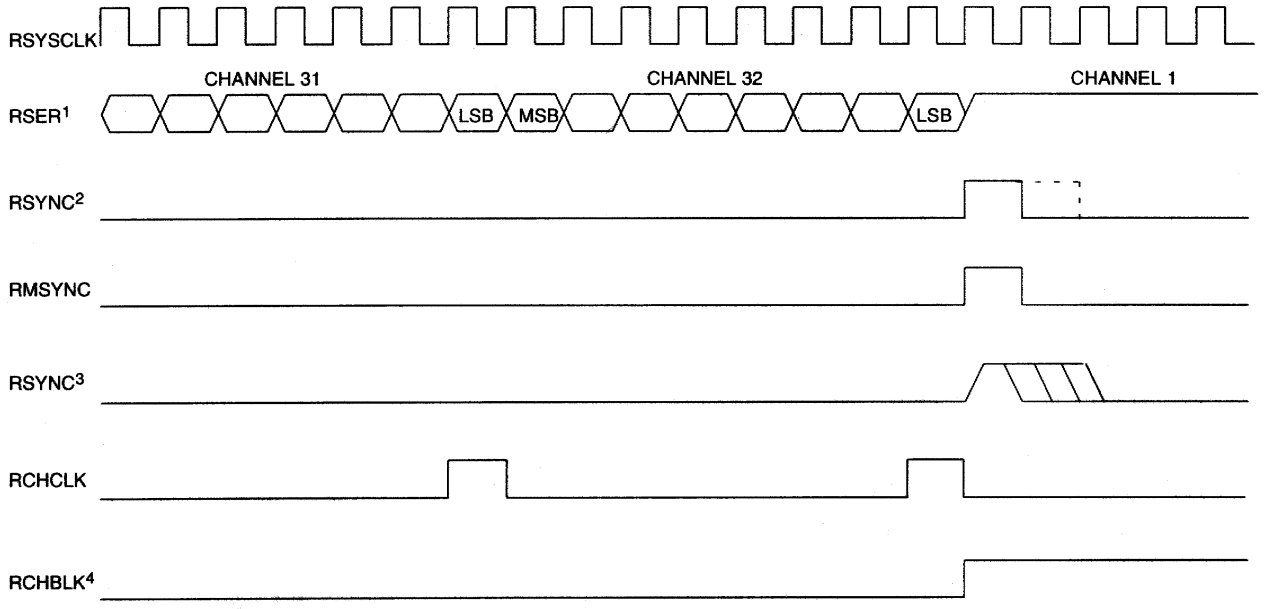
RECEIVE SIDE 1.544 MHz BOUNDARY TIMING (WITH ELASTIC STORE ENABLED) Figure 12-4



NOTES:

1. RSYNC is in the output mode (RCR2.3=0).
2. RSYNC is in the input mode (RCR2.3=1).
3. RCHBLK is programmed to block channel 24.

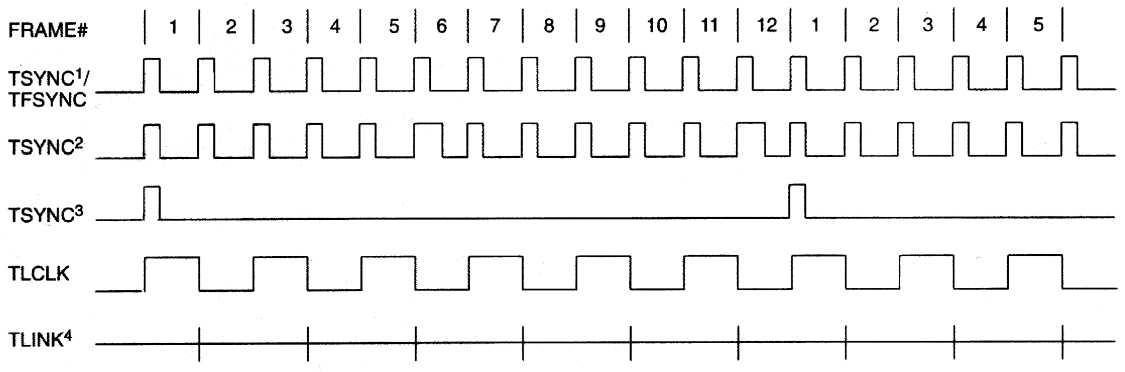
RECEIVE SIDE 2.048 MHz BOUNDARY TIMING (WITH ELASTIC STORE ENABLED) Figure 12-5



NOTES:

1. RSER data in channels 1, 5, 9, 13, 17, 21, 25, and 29 are forced to 1.
2. RSYNC is in the output mode (RCR2.3=0).
3. RSYNC is in the input mode (RCR2.3=1).
4. RCHBLK is forced to 1 in the same channels as RSER (see Note 1).

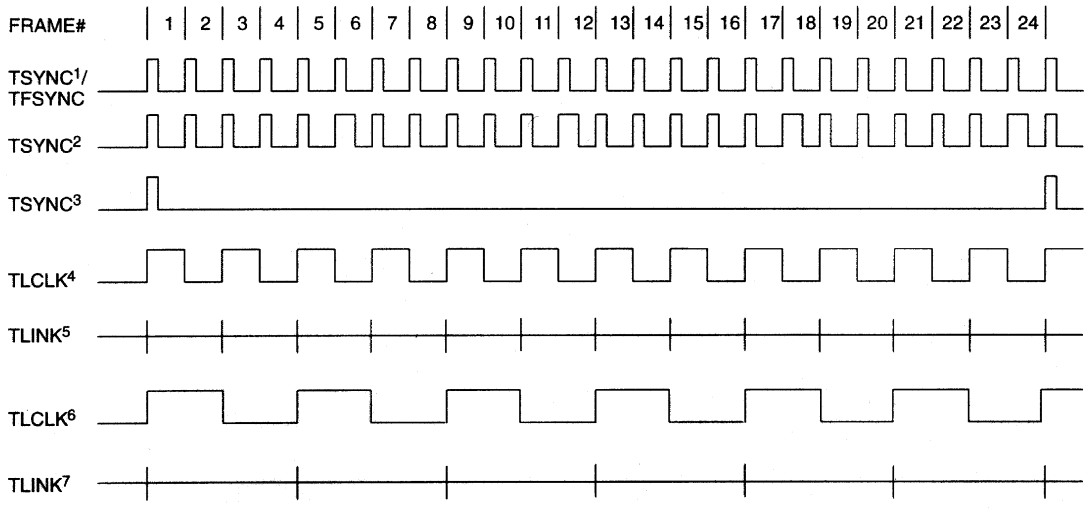
TRANSMIT SIDE D4 TIMING Figure 12-6



NOTES:

1. TSYNC in the frame mode (TCR2.3=0) and double-wide frame sync is not enabled (TCR2.4=0).
2. TSYNC in the frame mode (TCR2.3=0) and double-wide frame sync is enabled (TCR2.4=1).
3. TSYNC in the multiframe mode (TCR2.3=1).
4. TLINK data (S-bit) is sampled during the F-bit position of even frames for insertion into the outgoing T1 stream when enabled via TCR1.2.
5. TLINK and TLCLK are not synchronous with TFSYNC.

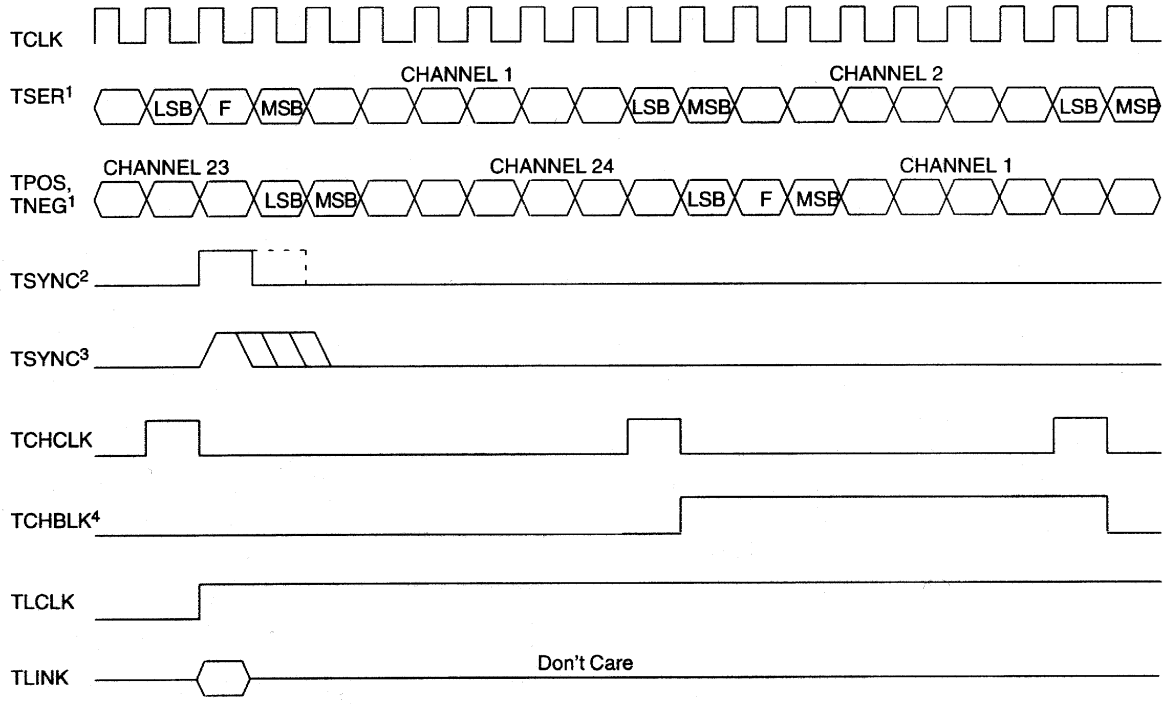
TRANSMIT SIDE ESF TIMING Figure 12-7



NOTES:

1. TSYNC in the frame mode (TCR2.3=0) and double-wide frame sync is not enabled (TCR2.4=0).
2. TSYNC in the frame mode (TCR2.3=0) and double-wide frame sync is enabled (TCR2.4=1).
3. TSYNC in the multiframe mode (TCR2.4=1).
4. ZBTSI mode disabled (TCR2.5=0).
5. TLINK data (FDL bits) is sampled during the F-bit time of odd frame and inserted into the outgoing T1 stream if enabled via TCR1.2.
6. ZBTSI mode is enabled (TCR2.5=1).
7. TLINK data (Z-bits) is sampled during the F-bit time of frame 1, 5, 9, 13, 17, and 21 and inserted into the outgoing stream if enabled via TCR1.2.
8. TLINK and TLCLK are not synchronous with TFSYNC.

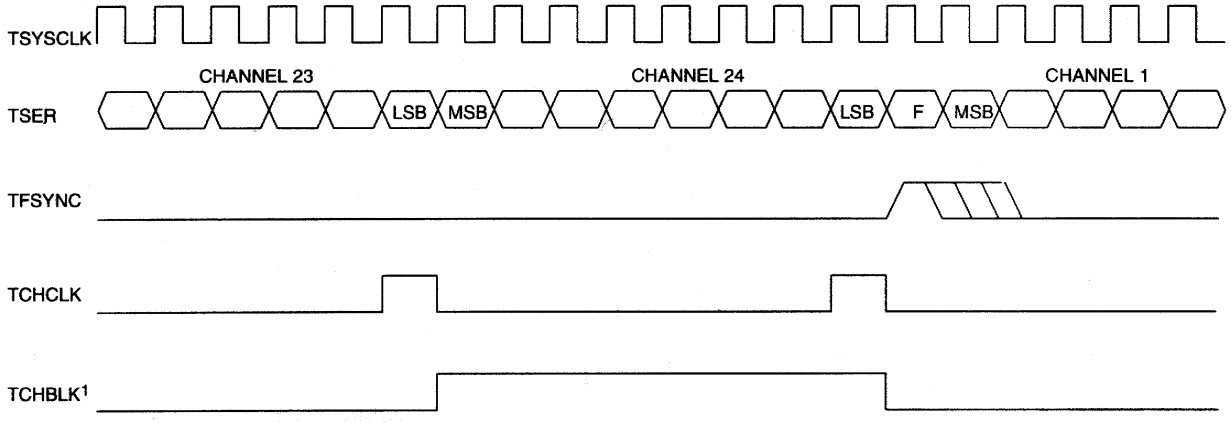
TRANSMIT SIDE BOUNDARY TIMING (WITH ELASTIC STORE DISABLED) Figure 12-8



NOTES:

1. There is a 10 TCLK delay from TSER to TPOS/TNEG.
2. TSYNC is in the output mode (TCR2.0=1).
3. TSYNC is in the input mode (TCR2.0=0).
4. TCHBLK is programmed to block channel 2.

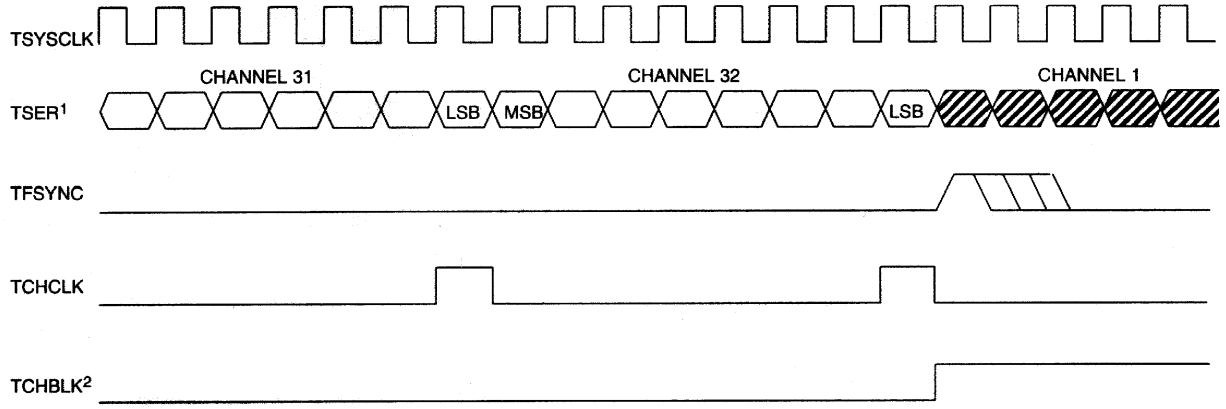
TRANSMIT SIDE 1.544 MHz BOUNDARY TIMING (WITH ELASTIC STORE ENABLED) Figure 12-9



NOTE:

1. TCHBLK is programmed to block channel 24.

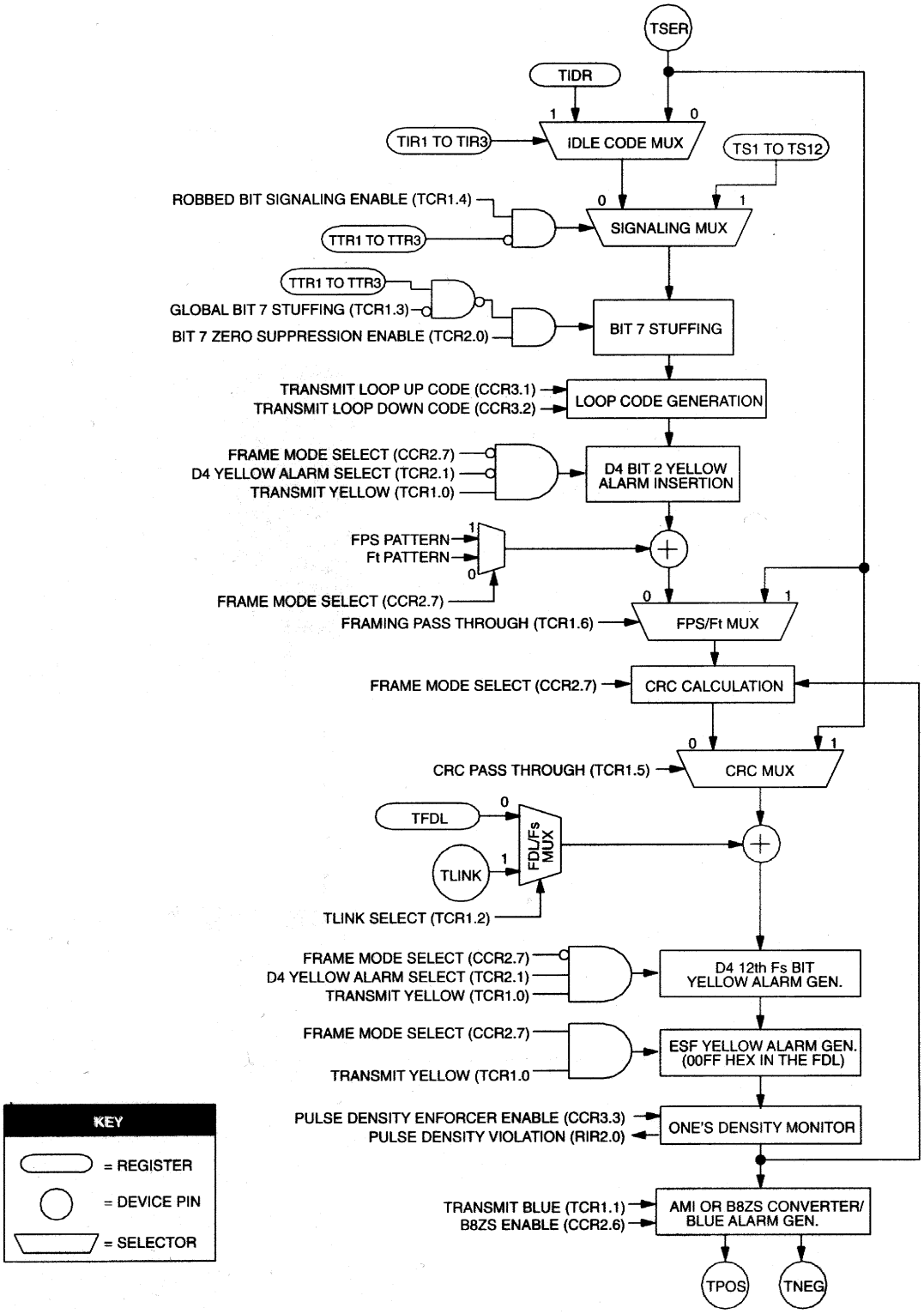
TRANSMIT SIDE 2.048 MHz BOUNDARY TIMING (WITH ELASTIC STORE ENABLED) Figure 12-10



NOTES:

1. TSER data in channels 1, 5, 9, 13, 17, 21, 25, and 29 is ignored.
2. TCHBLK is forced to 1 in the same channels as TSER (see Note 1).

DS21Q41B TRANSMIT DATA FLOW Figure 12-11



13.0 AC AND DC CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C for DS21Q41BT
Operating Temperature	-40°C to +85°C for DS21Q41BTN
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATION CONDITIONS

(0°C to 70°C for DS21Q41BT; -40°C to +85°C for DS21Q41BTN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{DD}+0.3	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.50		5.50	V	1

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5		pF	
Output Capacitance	C_{OUT}		7		pF	

DC CHARACTERISTICS

(0°C to 70°C; V_{DD}=5V ± 10% for DS21Q41BT; -40°C to +85°C; V_{DD}=5V ± 10% for DS21Q41BTN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current @ 5V	I_{DD}		30		mA	1
Input Leakage	I_{IL}	-1.0		+1.0	µA	2
Output Leakage	I_{LO}			1.0	µA	3
Output Current (2.4V)	I_{OH}	-1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

1. TCLK = RCLK = TSYSCLK = RSYSCLK = 1.544 MHz ; outputs open circuited.

2. $0.0V < V_{IN} < V_{DD}$.

3. Applies to $\overline{INT}$ when 3-stated.

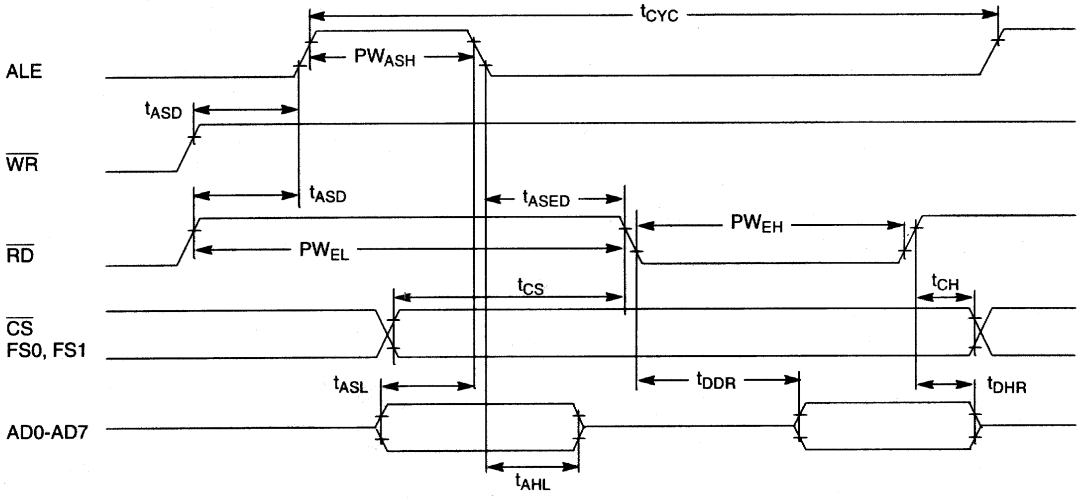
AC CHARACTERISTICS - MULTIPLEXED PARALLEL PORT (MUX=1)

(0°C to 70°C; V_{DD}=5V ± 10% for DS21Q41BT; -40°C to +85°C; V_{DD}=5V ± 10% for DS21Q41BTN)

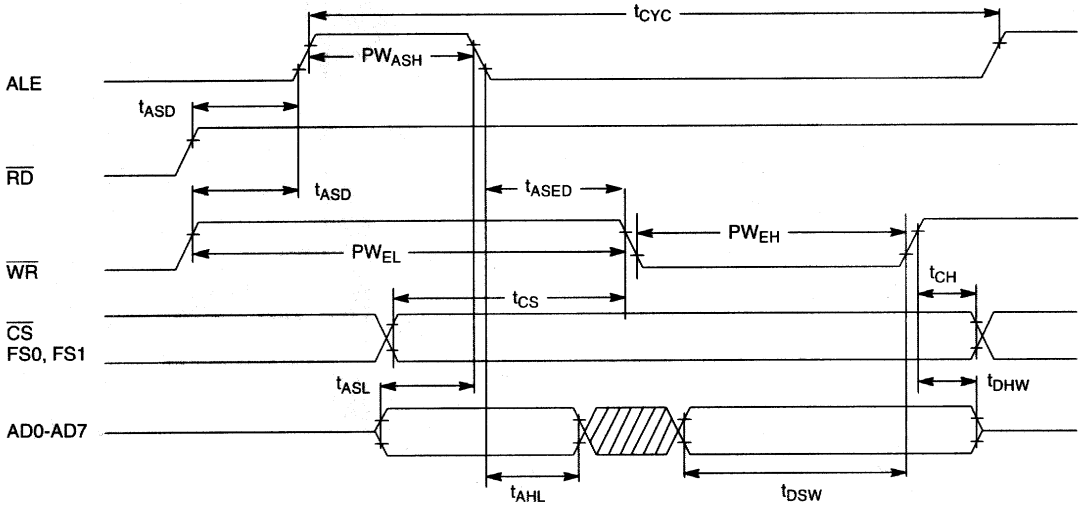
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	200			ns	
Pulse Width, DS Low or $\overline{RD}$ High	PW_{EL}	100			ns	
Pulse Width, DS High or $\overline{RD}$ Low	PW_{EH}	100			ns	
Input Rise/Fall Times	t_R, t_F			20	ns	
R/$\overline{W}$ Hold Time	t_{RWH}	10			ns	
R/$\overline{W}$ Setup Time Before DS High	t_{RWS}	50			ns	
$\overline{CS}$, FS0, FS1 Setup Time before DS, $\overline{WR}$ or $\overline{RD}$ Active	t_{CS}	20			ns	
$\overline{CS}$, FS0, FS1 Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		50	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid to AS or ALE Fall	t_{ASL}	15			ns	
Muxed Address Hold Time	t_{AHL}	10			ns	
Delay Time DS, $\overline{WR}$ or $\overline{RD}$ to AS or ALE Rise	t_{ASD}	20			ns	
Pulse Width AS or ALE High	PW_{ASH}	30			ns	
Delay Time, AS or ALE to DS, $\overline{WR}$ or $\overline{RD}$	t_{ASED}	10			ns	
Output Data Delay Time from DS or $\overline{RD}$	t_{DDR}	20		80	ns	
Data Setup Time	t_{DSW}	50			ns	

See Figures 13-1 to 13-3 for details.

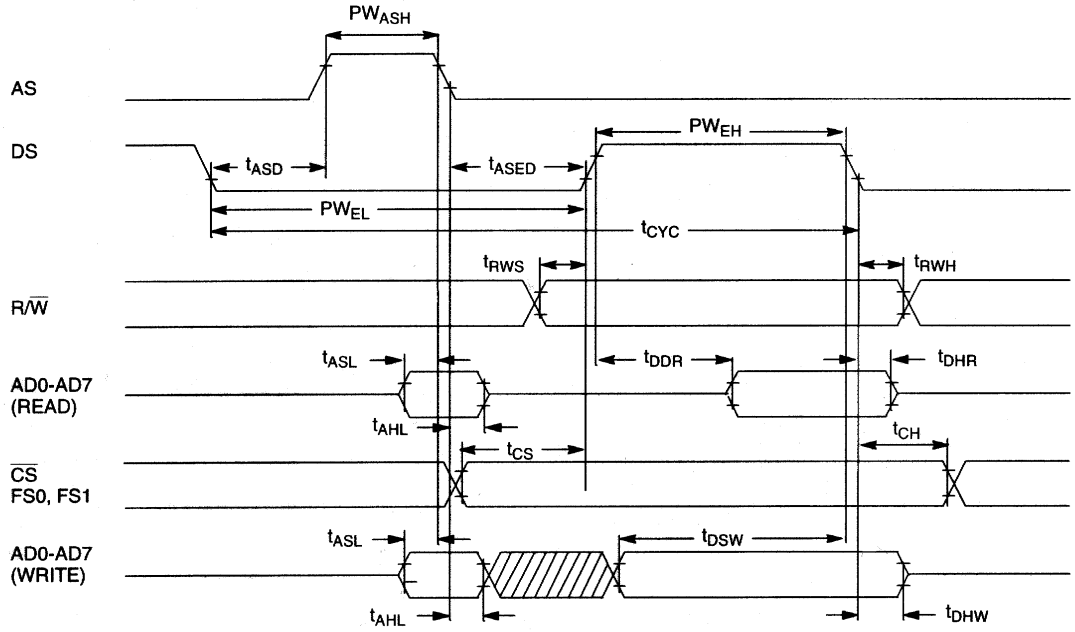
INTEL BUS READ AC TIMING (BTS=0/MUX=1) Figure 13-1



INTEL BUS WRITE AC TIMING (BTS=0/MUX=1) Figure 13-2



MOTOROLA BUS AC TIMING (BTS=1/MUX=1) Figure 13-3



AC CHARACTERISTICS - RECEIVE SIDE

(0°C to 70°C; V_{DD}=5V ± 10% for DS21Q41BT; -40°C to +85°C; V_{DD}=5V ± 10% for DS21Q41BTN)

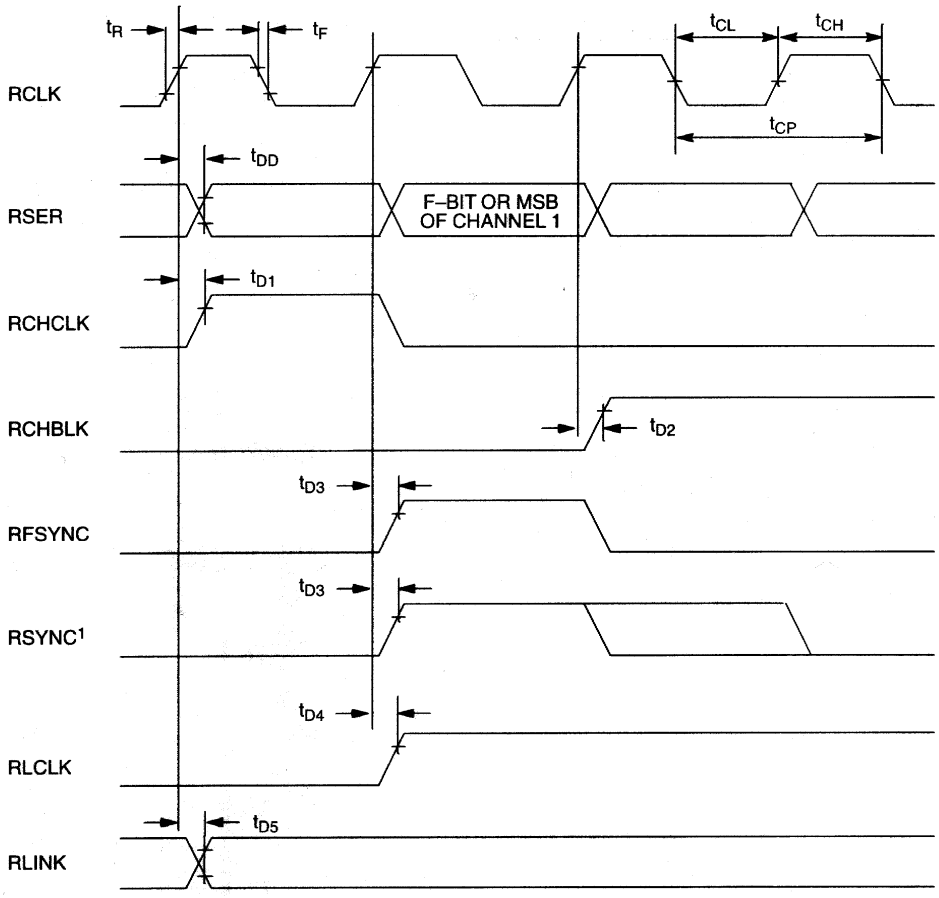
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t_{CP}		648		ns	
RCLK Pulse Width	t_{CH} t_{CL}	75 75			ns ns	
RSYSCLK Period	t_{SP} t_{SP}		648 488		ns ns	1 2
RSYSCLK Pulse Width	t_{SH} t_{SL}	50 50			ns	
RSYNC Set Up to RSYSCLK Falling or RPOS/RNEG Set Up to RCLK Falling	t_{SU}	20			ns	
RSYNC Pulse Width	t_{PW}	50			ns	3
RPOS/RNEG Hold from RCLK Falling	t_{HD}	20			ns	
RCLK and RSYSCLK Rise and Fall Times	t_R, t_F			25	ns	
Delay RCLK or RSYSCLK to RSER Valid	t_{DD}			75	ns	
Delay RCLK or RSYSCLK to RCHCLK	t_{D1}			75	ns	
Delay RCLK or RSYSCLK to RCHBLK	t_{D2}			75	ns	
Delay RCLK to RFSYNC or RSYNC or Delay RSYSCLK to RMSYNC or RSYNC	t_{D3}			75	ns	
Delay RCLK to RLCLK	t_{D4}			75	ns	
Delay RCLK to RLINK Valid	t_{D5}			75	ns	

See Figures 13-4 to 13-6 for details.

NOTES:

1. RSYSCLK=1.544 MHz.
2. RSYSCLK=2.048 MHz.
3. RSYNC in input mode.

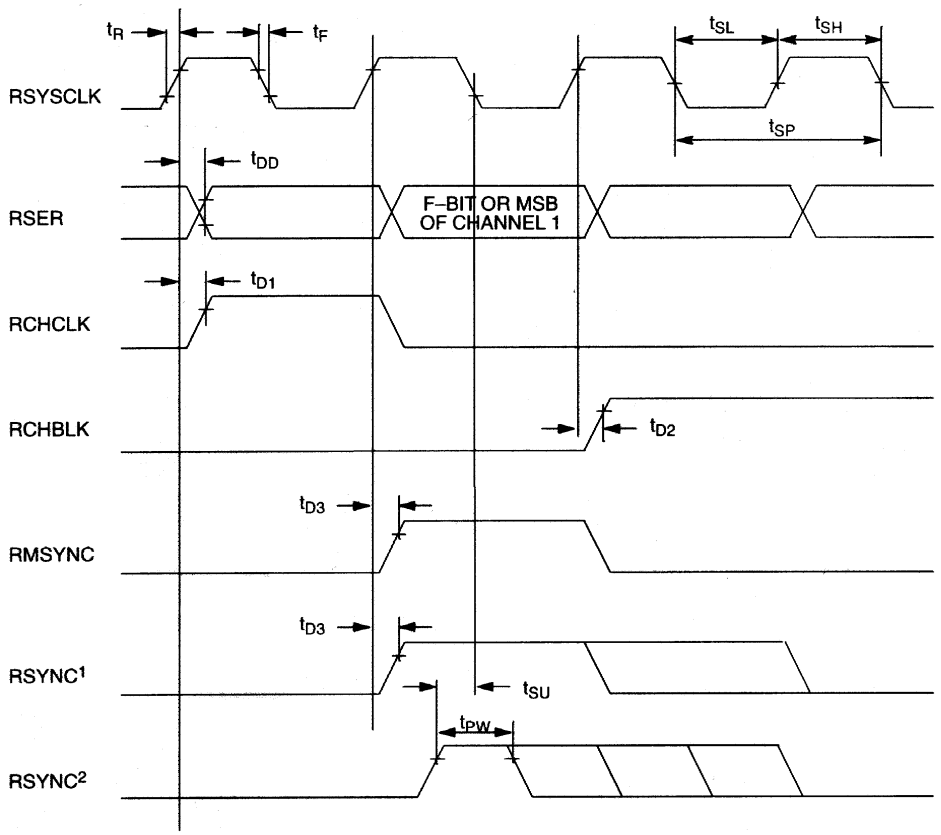
RECEIVE SIDE AC TIMING Figure 13-4



NOTE:

1. RSYNC is in the output mode (RCR2.3=0).

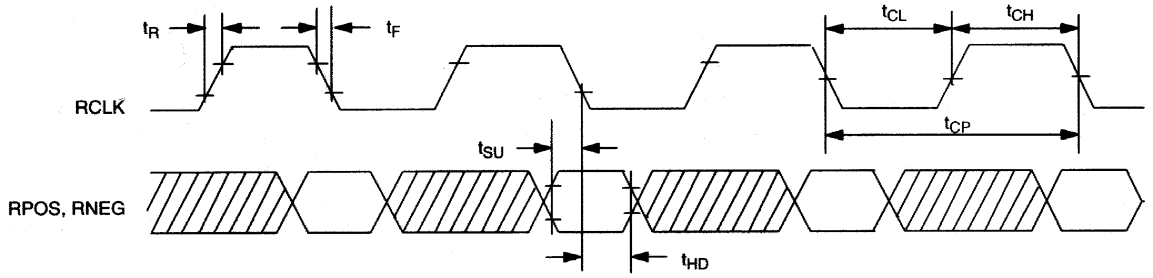
RECEIVE SYSTEM SIDE AC TIMING Figure 13-5



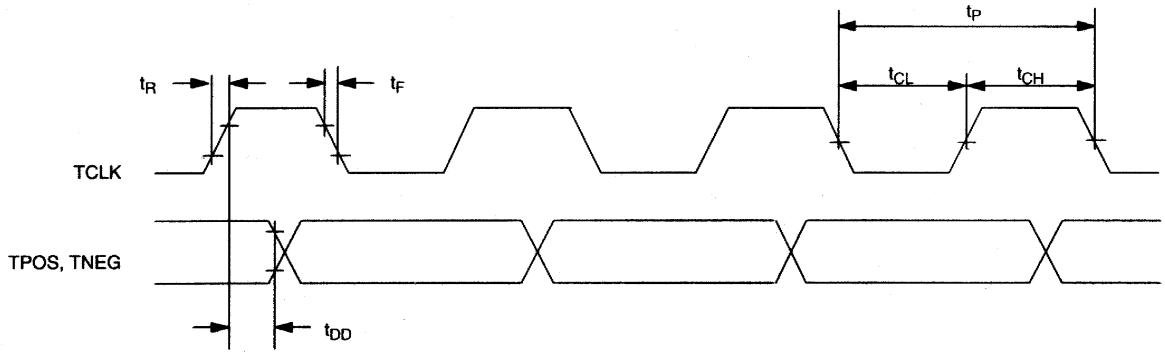
NOTES:

1. RSYNC is in the output mode (RCR 2.3 = 0).
2. RSYNC is in the input mode (RCR 2.3 = 1).

RECEIVE LINE INTERFACE AC TIMING Figure 13-6



TRANSMIT LINE INTERFACE SIDE AC TIMING Figure 13-7



AC CHARACTERISTICS - TRANSMIT SIDE

(0°C to 70°C; V_{DD}=5V ± 10% for DS21Q41BT; -40°C to +85°C; V_{DD}=5V ± 10% for DS21Q41BTN)

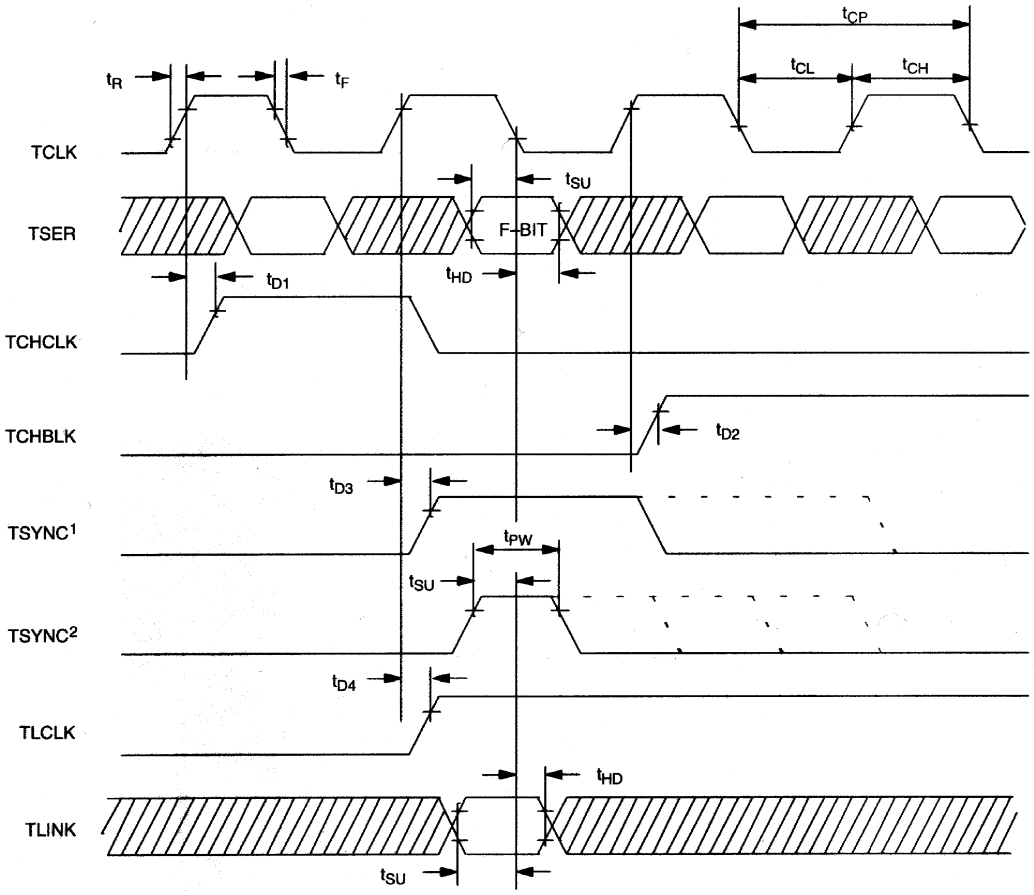
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t_{CP}		648		ns	
TCLK Pulse Width	t_{CH} t_{CL}	75 75			ns ns	
TSYSCLK Period	t_{SP} t_{SP}		648 488		ns ns	1 2
TSYSCLK Pulse Width	t_{SH} t_{SL}	50 50			ns ns	
TSER, TSYNC and TLINK Set Up to TCLK Falling or TSER, TFSYNC Set Up to TSYSCLK Falling	t_{SU}	20			ns	
TSYNC, TFSYNC Pulse Width	t_{PW}	50			ns	3
TSER, TSYNC and TLINK Hold from TCLK Falling or TSER	t_{HD}	20			ns	
TCLK or TSYSCLK Rise and Fall Times	t_R, t_F			25	ns	
Delay TCLK to TPOS/TNEG Valid	t_{DD}			75	ns	
Delay TCLK to TCHCLK or TSYSCLK to TCHCLK	t_{D1}			75	ns	
Delay TCLK to TCHBLK or TSYSCLK to TCHBLK	t_{D2}			75	ns	
Delay TCLK to TSYNC	t_{D3}			75	ns	
Delay TCLK to TLCLK	t_{D4}			75	ns	

See Figures 13-7 to 13-9 for details.

NOTES:

1. TSYSCLK = 1.544 MHz.
2. TSYSCLK = 2.048 MHz.
3. TSYNC in input mode.

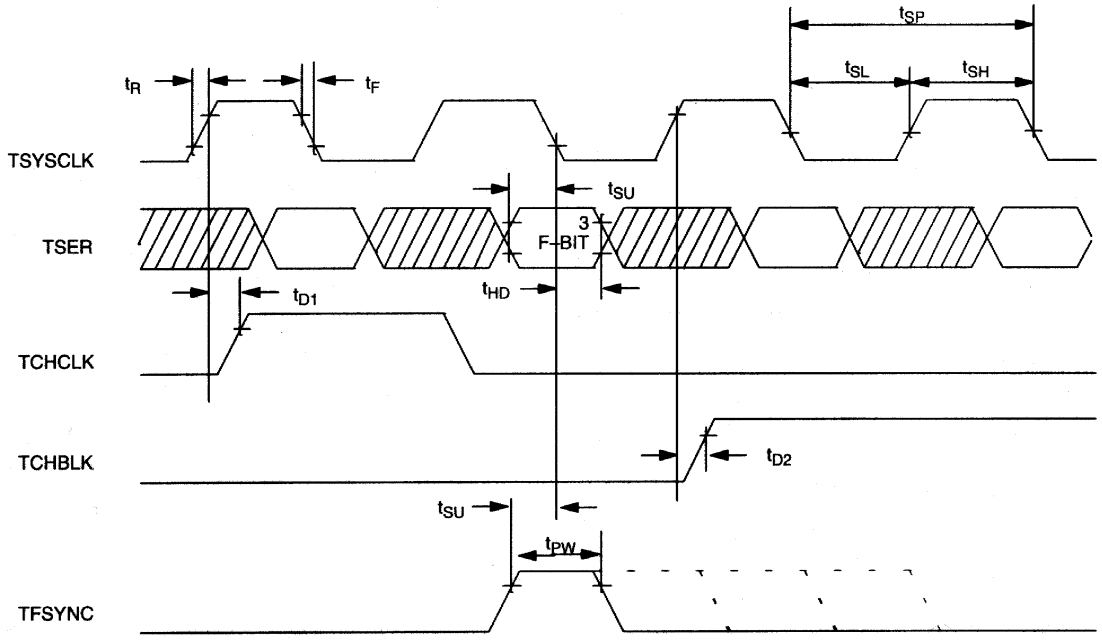
TRANSMIT SIDE AC TIMING Figure 13-8



NOTES:

1. TSYNC is in the output mode (TCR2.2=1).
2. TSYNC is in the input mode (TCR2.2=0).
3. TSER is sampled on the falling edge of TCLK when the transmit side elastic store is disabled.
4. TCHCLK and TCHBLK are synchronous with TCLK when the transmit side elastic store is disabled.

TRANSMIT SYSTEM SIDE AC TIMING Figure 13-9



NOTES:

1. TSER is only sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled.
2. TCHCLK and TCHBLK are synchronous with TSYSCLK when the transmit side elastic store is enabled.
3. MSB of channel 1 when TSYSCLK is in 2.048 mode.

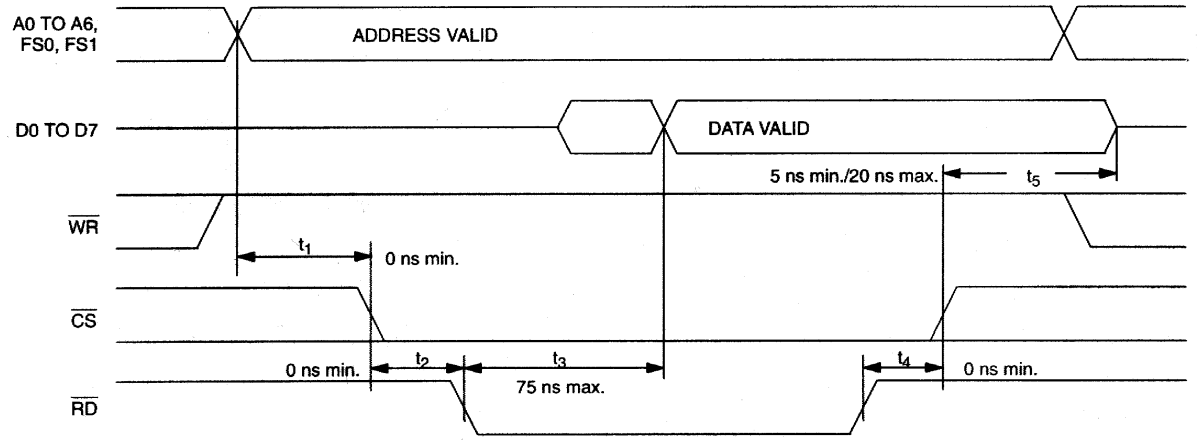
AC CHARACTERISTICS - NON-MULTIPLEXED PARALLEL PORT (MUX=0)

(0°C to 70°C; V_{DD}=5V ± 10% for DS21Q41BT; -40°C to +85°C; V_{DD}=5V ± 10% for DS21Q41BTN)

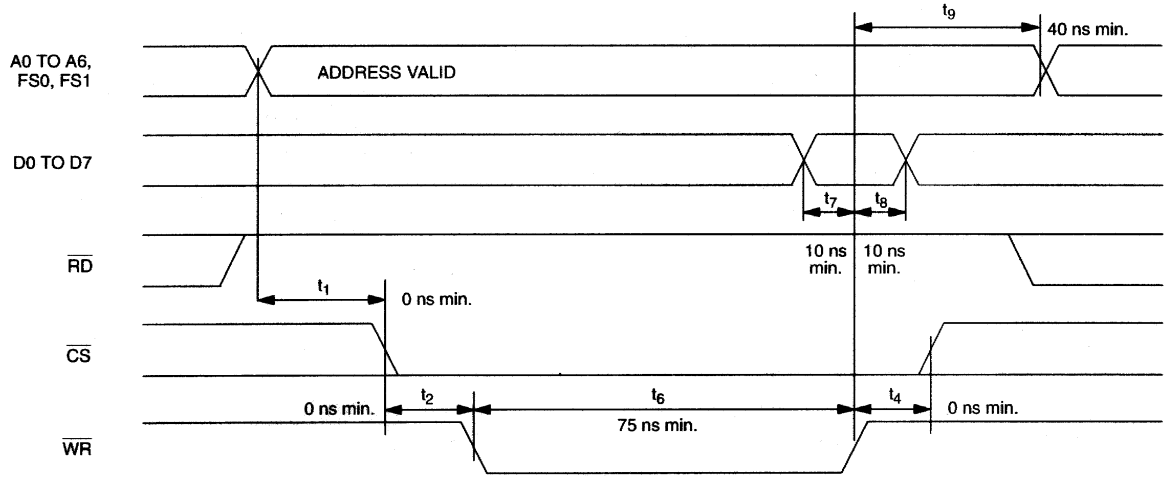
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Set Up Time for A0 to A6, FS0, FS1 Valid to CS Active	t_1	0			ns	
Set Up Time for CS Active to either RD, WR, or DS Active	t_2	0			ns	
Delay Time from either RD or DS Active to Data Valid	t_3			75	ns	
Hold Time from either RD, WR, or DS Inactive to CS Inactive	t_4	0			ns	
Hold Time from CS Inactive to Data Bus 3-State	t_5	5		20	ns	
Wait Time from either WR or DS Active to Latch Data	t_6	75			ns	
Data Set Up Time to either WR or DS Inactive	t_7	10			ns	
Data Hold Time from either WR or DS Inactive	t_8	10			ns	
Address Hold Time	t_9	40			ns	

See Figures 13-10 to 13-13 for details.

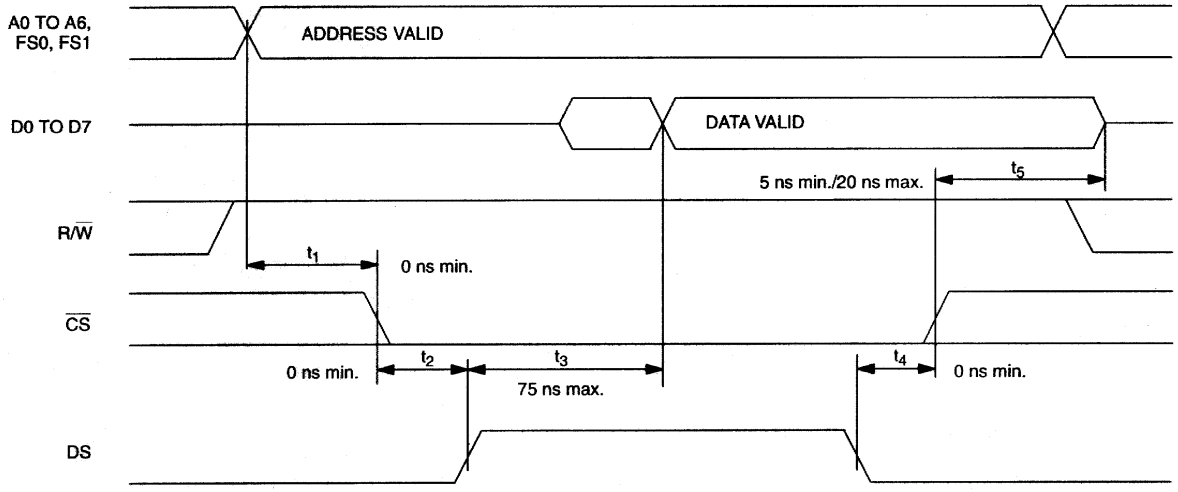
INTEL BUS READ AC TIMING (BTS=0/MUX=0) Figure 13-10



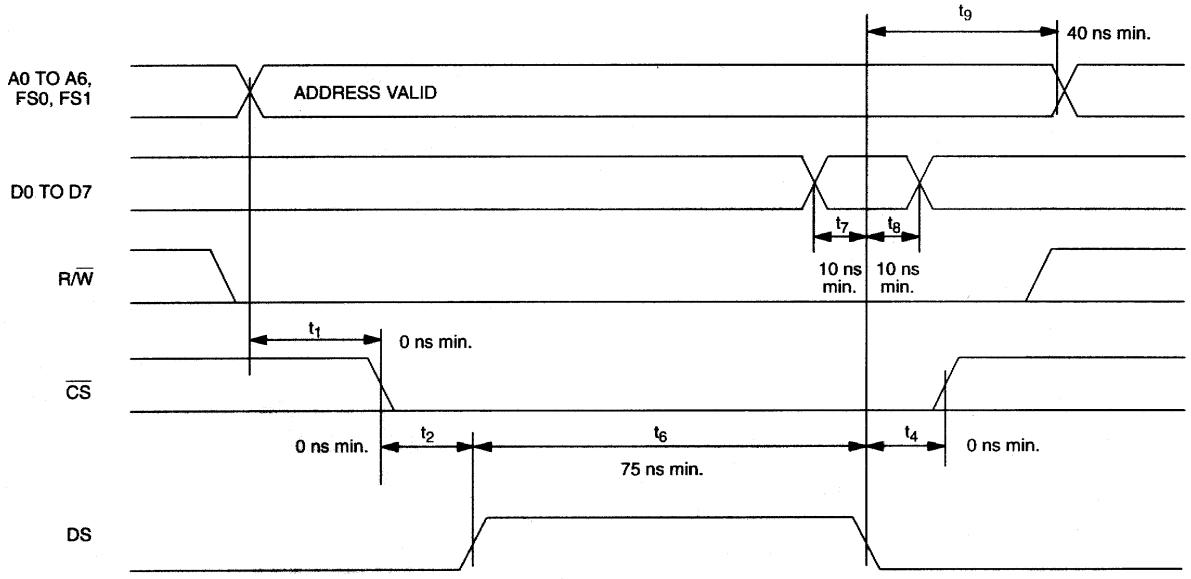
INTEL BUS WRITE AC TIMING (BTS=0/MUX=0) Figure 13-11



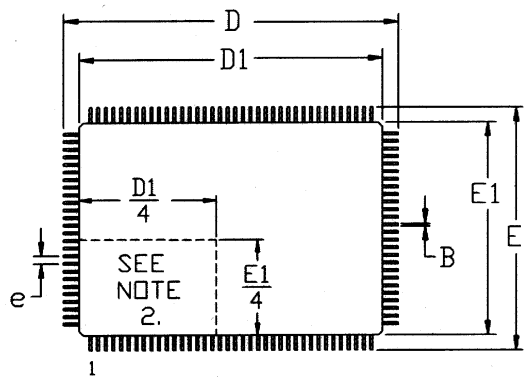
MOTOROLA BUS READ AC TIMING (BTS=1/MUX=0) Figure 13-12



MOTOROLA BUS WRITE AC TIMING (BTS=1/MUX=0) Figure 13-13

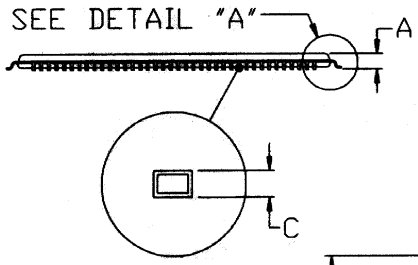


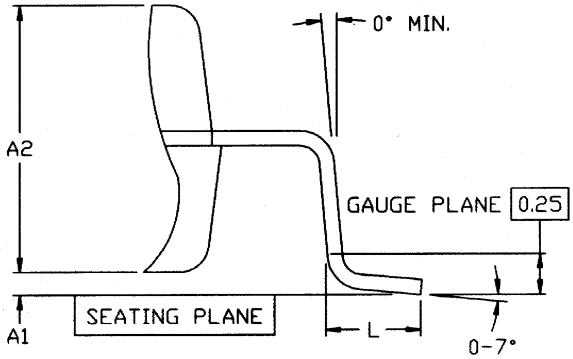
DS21Q41B 128-PIN TQFP



NOTES:

1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE.
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE B DIMENSION; PROTRUSION NOT TO BE LOCATED ON LOWER RADIUS OR FOOT OF LEAD.





DETAIL A

DIMENSIONS ARE IN MILLIMETERS

PKG	128-PIN	
DIM	MIN	MAX
A	-	1.60
A1	0.05	-
A2	1.35	1.45
B	0.17	0.27
C	0.09	0.20
D	21.80	22.20
D1	20.00 BSC	
E	15.80	16.20
E1	14.00 BSC	
e	0.50 BSC	
L	0.45	0.75

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- Alternative Solution
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