



THE DATASHEET OF DS2182Q



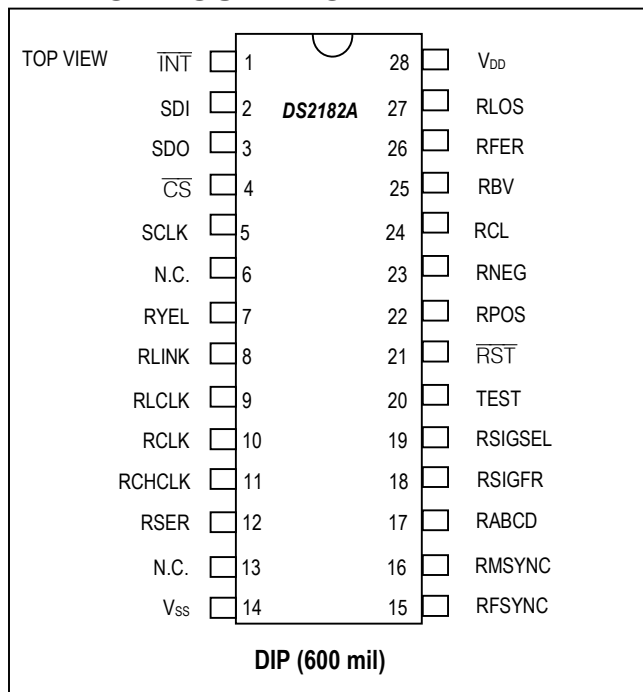
GENERAL DESCRIPTION

The DS2182A T1 line monitor chip is a monolithic CMOS device designed to monitor real-time performance on T1 lines. The DS2182A frames to the data on the line, counts errors, and supplies detailed information about the status and condition of the line. Large on-board counters allow the accumulation of errors for extended periods, which permits a single CPU to monitor many T1 lines. Output clocks that are synchronized to the incoming data stream are provided for easy extraction of S-bits, FDL bits, signaling bits, and channel data. The DS2182A meets the requirements of ANSI T1.231.

ORDERING INFORMATION

| PART | TEMP RANGE | PIN-PACKAGE |
|----------|----------------|-------------|
| DS2182 | 0°C to +70°C | 28 DIP |
| DS2182N | -40°C to +85°C | 28 DIP |
| DS2182Q | 0°C to +70°C | 28 PLCC |
| DS2182QN | -40°C to +85°C | 28 PLCC |

PIN CONFIGURATION



FEATURES

- Performs Framing and Monitoring Functions
- Supports Superframe and Extended Superframe Formats
- Four On-Board Error Counters:
 - 16-Bit Bipolar Violation
 - 8-Bit CRC
 - 8-Bit OOF
 - 8-Bit Frame Bit Error
- Indication of the Following:
 - Yellow and Blue Alarms
 - Incoming B8ZS Codewords
 - 8 and 16 Zero Strings
 - Change-of-Frame Alignment
 - Loss of Sync
 - Carrier Loss
- Simple Serial Interface Used for Configuration, Control, and Status Monitoring
- Burst Mode Allows Quick Access to Counters for Status Updates
- Automatic Counter Reset Feature
- Single 5V Supply; Low-Power CMOS Technology
- Available in 28-Pin DIP and 28-Pin PLCC
- Upward-Compatible from the Original DS2182

The DS2182A includes the following changes from the original DS2182:

- Ability to Count Excessive Zeros
- Severely Errored-Framing-Event Indication
- Updated AIS Detection
- Updated RCL Detection
- AIS and RCL Alarm Clear Indications

Note: Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.

Table 1. Pin Description

| PIN | NAME | TYPE | FUNCTION |
|-------|-------------------------|------|--|
| 1 | $\overline{\text{INT}}$ | O | Receive Alarm Interrupt. Flags host controller during alarm conditions. Active low; open-drain output. |
| 2 | SDI | I | Serial Data In. Data for on-board registers. Sampled on rising edge of SCLK. |
| 3 | SDO | O | Serial Data Out. Control and status information from on-board registers. Updated on falling edge of SCLK; tri-stated during serial port write or when CS is high. |
| 4 | $\overline{\text{CS}}$ | I | Chip Select. Must be low to read or write the serial port. |
| 5 | SCLK | I | Serial Data Clock. Used to read or write the serial port registers. |
| 6, 13 | N.C. | — | No Connect. No internal connection. This pin can be connected to either V_{SS} or V_{DD} , or it can be floated. |
| 7 | RYEL | O | Receive Yellow Alarm. Transitions high when a yellow alarm detected; goes low when the alarm clears. |
| 8 | RLINK | O | Receive Link Data. Updated with extracted FDL data one RCLK before start of odd frames (193E) and held until next update. Updated with extracted S-bit data one RCLK before start of even frames (193S) and held until next update. |
| 9 | RLCLK | O | Receive Link Clock. 4kHz demand clock for RLINK |
| 10 | RCLK | I | Receive Clock. 1.544MHz primary clock |
| 11 | RCHCLK | O | Receive Channel Clock. 192kHz clock; identifies timeslot (channel) boundaries |
| 12 | RSER | O | Receive Serial Data. Received NRZ serial data; updated on rising edges of RCLK |
| 15 | RFSYNC | O | Receive Frame Sync. Extracted 8kHz clock, one RCLK wide; F-bit position in each frame |
| 16 | RMSYNC | O | Receive Multiframe Sync. Extracted multiframe sync; positive-going edge indicates start of multiframe; 50% duty cycle |
| 17 | RABCD | O | Receive ABCD Signaling. Extracted signaling data output; valid for each channel in signaling frames. In non-signaling frames, RABCD outputs the LSB of each channel word. |
| 18 | RSIGFR | O | Receive Signaling Frame. High during signaling frames; low during non-signaling frames (and during resync) |
| 19 | RSIGSEL | O | Receive Signaling Select. In 193E framing, a .667kHz clock that identifies signaling frames A and C; a 1.33kHz clock in 193S |
| 21 | $\overline{\text{RST}}$ | I | Reset. A high-low transition clears all internal registers and resets counters. A high-low-high transition initiates a resync. |
| 22 | RPOS | I | Receive Bipolar Data Inputs. Sampled on falling of RCLK. Connect together to receive NRZ data and disable bipolar violation monitoring circuitry. |
| 23 | RNEG | | |
| 24 | RCL | O | Receive Carrier Loss. High if 192 consecutive 0's appear at RPOS and RNEG; goes low upon seeing 12.5% 1's density. |
| 25 | RBV | O | Receive Bipolar Violation. High during accused bit time at RSER. If bipolar violation detected, low otherwise. |
| 26 | RFER | O | Receive Frame Error. High during F-bit time when FT or FS errors occur (193S), or when FPS or CRC errors occur (193E). Low during resync. |
| 27 | RLOS | O | Receive Loss-of-Sync. Indicates sync status; high when internal resync is in progress, low otherwise. |

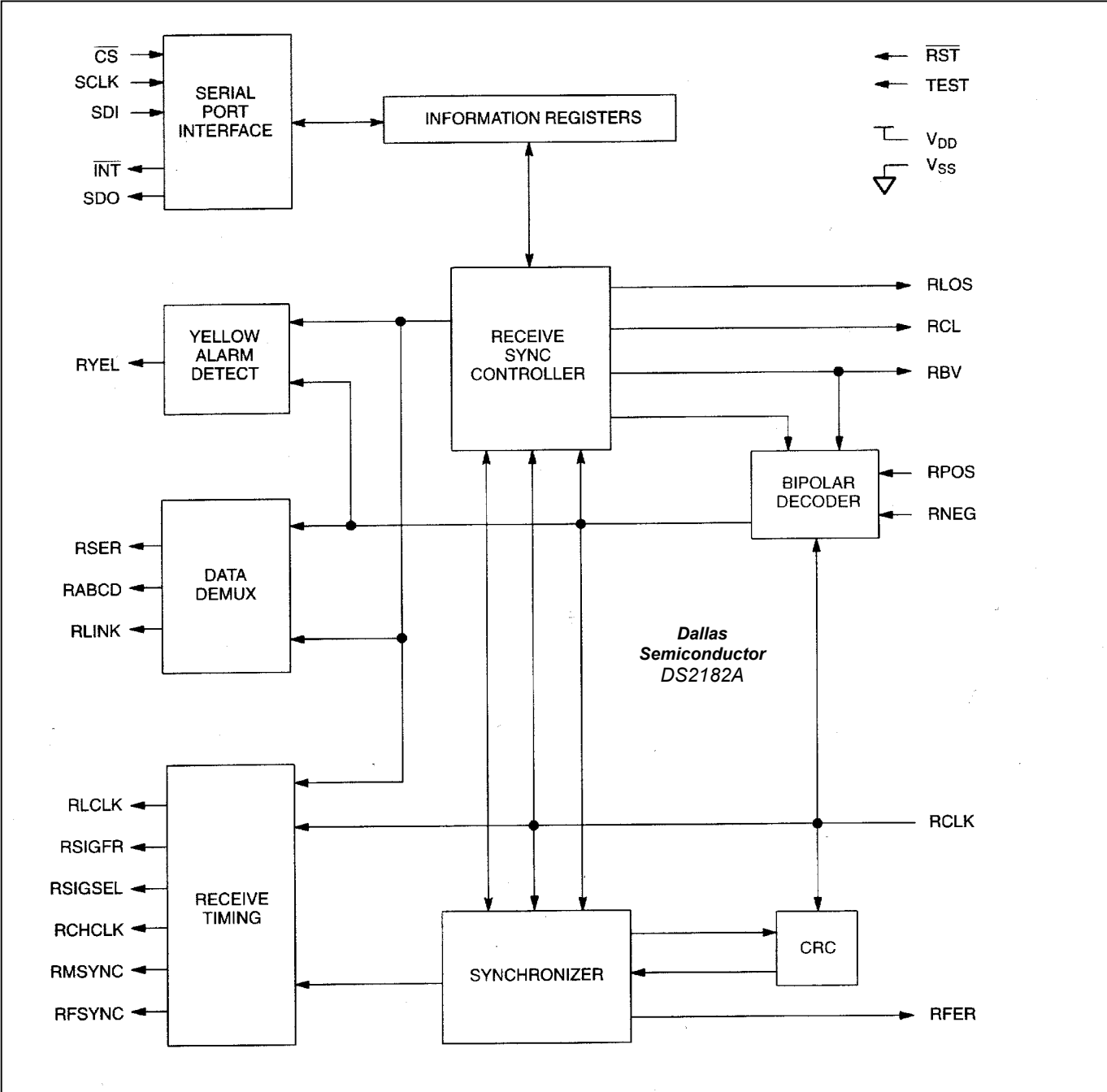
Table 2. Power and Test Pin Description

| PIN | NAME | TYPE | FUNCTION |
|-----|-----------------|------|--|
| 14 | V _{SS} | — | Signal Ground. 0V |
| 20 | TEST | I | Test Mode. Connect to V _{SS} for normal operation. |
| 28 | V _{DD} | — | Positive Supply. 5.0V |

Table 3. Register Summary

| REGISTER | ADDRESS | FUNCTION |
|----------|---------|--|
| BVCR2 | 0000 | Bipolar Violation Count Register 2. LSW of a 16-bit presettable counter that records individual bipolar violations. |
| BVCR1 | 0001 | Bipolar Violation Count Register 1. MSW of a 16-bit presettable counter that records individual bipolar violations. |
| CRCCR | 0010 | CRC Error Count Register. 8-bit presettable counter that records CRC6 errored words in the 193E frame mode. |
| OOFCR | 0011 | OOFCR Count Register. 8-bit presettable counter that records OOF events. OOF events are defined by RCR1.5 and RCR1.6. |
| FEER | 0100 | Frame Error Count Register. 8-bit presettable counter that records individual bit errors in the framing pattern. |
| RSR1 | 0101 | Receive Status Register 1. Reports alarm conditions. |
| RIMR1 | 0110 | Receive Interrupt Mask Register 1. Allows masking of individual alarm-generated interrupts from RSR1. |
| RSR2 | 0111 | Receive Status Register 2. Reports alarm conditions. |
| RIMR2 | 1000 | Receive Interrupt Mask Register 2. Allows masking of individual alarm-generated interrupts from RSR2. |
| RCR1 | 1001 | Receive Control Register 1. Programs device operating characteristics. |
| RCR2 | 1010 | Receive Control Register 2. Programs device operating characteristics. |

Figure 1. Block Diagram



SERIAL PORT INTERFACE

The port pins of the DS2182A serve as a microprocessor/microcontroller-compatible serial port. Eleven on-board registers allow the user to update operational characteristics and monitor device status through a host controller, minimizing hardware interfaces. The port on the DS2182A can be read from or written to at any time. Serial port reads and writes are independent of T1 line timing signals RCLK, RPOS, and RNEG. However, RCLK is needed to clear RSR1 and RSR2 after reads.

ADDRESS/COMMAND

Reading or writing the control, configuration, or status registers requires writing one address/command byte prior to transferring register data. The first bit written (LSB) of the address/command word specifies register read or write. The following four bits identify the register address. The next two bits are reserved and must be set to 0 for proper operation. The last bit of the address/ command word enables burst mode when set. The burst mode causes all registers to be consecutively read or written to. Data is read and written to the DS2182A LSB first.

CHIP SELECT AND CLOCK CONTROL

All data transfers are initiated by driving the \overline{CS} input low. Input data is latched on the rising edge of SCLK and must be valid during the previous low period of SCLK to prevent momentary corruption of register data during writes. Data is output on the falling edge of SCLK and held to the next falling edge. All data transfers are terminated if the \overline{CS} input transitions high. Port control logic is disabled and SDO is tri-stated when \overline{CS} is high.

DATA I/O

Following the eight SCLK cycles that input an address/command byte to write, a data byte is strobed into the addressed register on the rising edge of the next eight SCLK cycles. Following an address/command word to read, contents of the selected register are output on the falling edges of the next eight SCLK cycles. The SDO pin is tri-stated during device write and can be connected to SDI in applications where the host processor has a bidirectional I/O pin.

BURST MODE

The burst mode allows all on-board registers to be consecutively written to or read by the host processor. A burst read is used to poll all registers. RSR1 and RSR2 contents are unaffected. This feature minimizes device initialization time on system power-up or reset. Burst mode is initiated when ACB.7 is set and the address is 0000. A burst is terminated by a low-high transition on \overline{CS} .

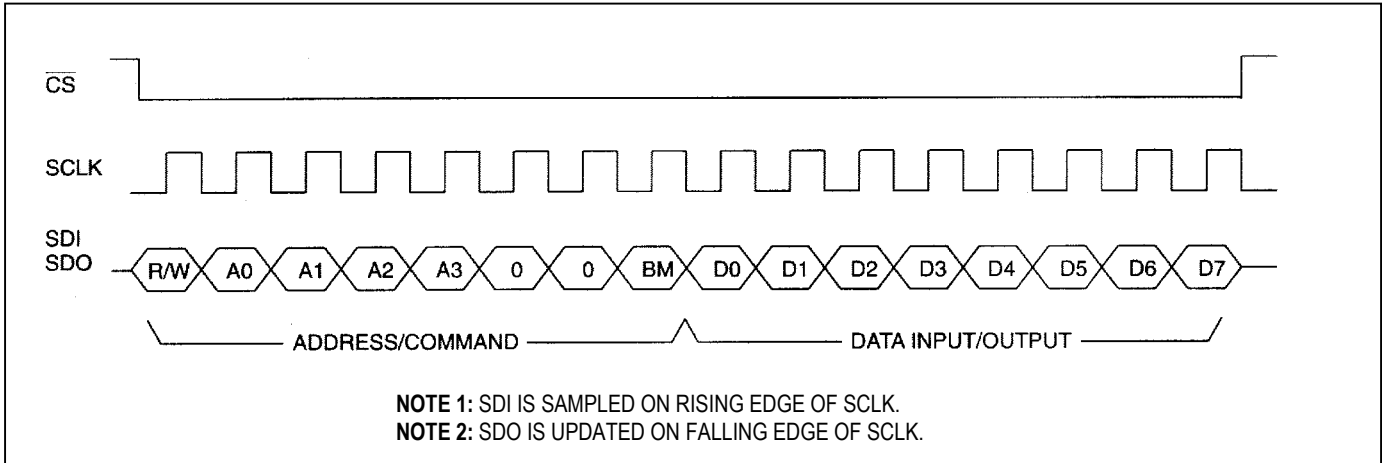
ACB: Address Command Byte

MSB

LSB

| | | | | | | | |
|----|---|---|------|------|------|------|-------------------|
| BM | — | — | ADD3 | ADD2 | ADD1 | ADD0 | R/ \overline{W} |
|----|---|---|------|------|------|------|-------------------|

| NAME | POSITION | FUNCTION |
|-------------------|----------|---|
| BM | ACB.7 | Burst Mode. If set (and register address is 0000), burst read or write is enabled. |
| — | ACB.6 | Reserved; must be 0 for operation |
| — | ACB.5 | Reserved; must be 0 for operation |
| ADD3 | ACB.4 | MSB of register address |
| ADD0 | ACB.1 | LSB of register address |
| R/ \overline{W} | ACB.0 | Read/Write Select 0 = write addressed register 1 = read addressed register |

Figure 2. Serial Port Read/Write

OPERATION OF THE COUNTERS

All four of the counters in the DS2182A can be preset by the user to establish an event-count interrupt threshold. The counters count up from the preset value until they reach saturation. At saturation, each additional event occurrence sets the appropriate bit in RSR2 and generates an interrupt if enabled by RIMR2.

The DS2182A contains an auto-counter reset feature in the burst read mode. If RCR1.4 is set, then the user can burst read the four counters (five registers), and all four counters are automatically reset to 0 after the read takes place. Since the burst mode can be terminated at any time by taking \overline{CS} high, the user has the option of reading all of the registers or only the counters. If RCR1.4 is set, then any read of the registers, burst mode or not, clears the count in all four counters. If the user wishes to read the port and not clear the counters, then RCR1.4 must be cleared first.

The counter registers can be read or written to at any time with the serial port, which operates totally asynchronously with the monitoring of the T1 line. Reading a register does not affect the count as long as RCR1.4 is cleared. The dual buffer architecture of the DS2182A ensures that no error events are missed while the serial port is being accessed for reads.

BVCR1: Bipolar Violation Count Register 1; BVCR2: Bipolar Violation Counter Register 2

MSB

LSB

| | | | | | | | |
|-----|-----|-----|-----|-----|-----|-----|-----|
| BV7 | BV6 | BV5 | BV4 | BV3 | BV2 | BV1 | BV0 |
|-----|-----|-----|-----|-----|-----|-----|-----|

| NAME | POSITION | FUNCTION |
|------|----------|--------------------------------|
| BV7 | BVCR.7 | MSB of bipolar violation count |
| BV0 | BVCR.0 | LSB of bipolar violation count |

Bipolar violation count register 1 (BVCR1) is the most significant word and BVCR2 is the least significant word of a presettable 16-bit counter that records individual bipolar violations. If the B8ZS mode is enabled (RCR2.2 = 1), then B8ZS codewords are not counted. The BVCR can also be programmed to count excessive 0's by setting the RCR2.5 bit. In this mode, the BVCR counts occurrences of eight consecutive 0's when B8ZS is enabled or 16 consecutive 0's when B8ZS is disabled. This counter increments at all times and is not disabled by a loss-of-sync condition (RLOS = 1). The counter saturates at 65,535 and generates an interrupt for each occurrence after saturation if RIMR2.0 is set.

Note: To properly preset the bipolar violation count register, BVCR2 must be written to before BVCR1 is written to.

CRCCR: CRC Count Register 2**MSB****LSB**

| | | | | | | | |
|------|------|------|------|------|------|------|------|
| CRC7 | CRC6 | CRC5 | CRC4 | CRC3 | CRC2 | CRC1 | CRC0 |
|------|------|------|------|------|------|------|------|

| NAME | POSITION | FUNCTION |
|------|----------|-------------------------------------|
| CRC7 | CRCCR.7 | MSB of CRC6 word error count |
| CRC0 | CRCCR.0 | LSB of CRC6 word error count |

The CRC count register (CRCCR) is an 8-bit presettable counter that records word errors in the cyclic redundancy check (CRC). This 8-bit binary counter saturates at 255 and generates an interrupt for each occurrence after saturation if RIMR2.1 is set. The count in this register is only valid in the 193E-framing mode (RCR2.4 = 1), and is reset and disabled in the 193S-framing mode (RCR2.4 = 0). The count is disabled during a loss-of-sync condition (RLOS = 1).

OOF CR: OOF Count Register**MSB****LSB**

| | | | | | | | |
|------|------|------|------|------|------|------|------|
| OOF7 | OOF6 | OOF5 | OOF4 | OOF3 | OOF2 | OOF1 | OOF0 |
|------|------|------|------|------|------|------|------|

| NAME | POSITION | FUNCTION |
|------|----------|----------------------------------|
| OOF7 | OOF CR.7 | MSB of OOF event count |
| OOF0 | OOF CR.0 | LSB of OOF of event count |

The OOF count register (OOF CR) is an 8-bit presettable counter that records out-of-frame (OOF) events. OOF events are defined by RCR1.5 and RCR1.6. This 8-bit counter saturates at 255 and generates an interrupt for each occurrence after saturation if RIMR2.2 is set. The count is disabled during a loss-of-sync condition (RLOS = 1).

FE CR: Frame Error Count Register**MSB****LSB**

| | | | | | | | |
|-----|-----|-----|-----|-----|-----|-----|-----|
| FE7 | FE6 | FE5 | FE4 | FE3 | FE2 | FE1 | FE0 |
|-----|-----|-----|-----|-----|-----|-----|-----|

| NAME | POSITION | FUNCTION |
|------|----------|---------------------------------|
| FE7 | FE CR.7 | MSB of frame error count |
| FE0 | FE CR.0 | LSB of frame error count |

The frame error count register (FE CR) is an 8-bit presettable counter that records individual frame-bit errors. In the 193E mode (RCR2.4 = 1), the FE CR records bit errors in the FPS framing pattern (001011). In the 193S mode (RCR2.4 = 0), the FE CR records bit errors in both the FT (101010) and FS (001110) framing patterns if RCR1.3 is set. If RCR1.3 is cleared, then the FE CR only records bit errors in the FT pattern. This 8-bit counter saturates at 255 and generates an interrupt for each occurrence after saturation if RIMR2.3 is set. The count is disabled during a loss-of-sync condition (RLOS = 1).

RSR1: Receive Status Register 1**MSB****LSB**

| | | | | | | | |
|-----|------|-----|------|------|-------|-----|------|
| 8ZD | 16ZD | RCL | RYEL | RLOS | B8ZSD | RBL | COFA |
|-----|------|-----|------|------|-------|-----|------|

| NAME | POSITION | FUNCTION |
|-------|----------|---|
| 8ZD | RSR1.7 | 8 Zero Detect. Set when a string of eight consecutive 0's has been received at RPOS and RNEG. |
| 16ZD | RSR1.6 | 16 Zero Detect. Set when a string of 16 consecutive 0's has been received at RPOS and RNEG. |
| RCL | RSR1.5 | Receive Carrier Loss. Set when a string of 192 consecutive 0's has been received at RPOS and RNEG. Cleared when 14 or more 1's out of 112 possible bit positions are received. |
| RYEL | RSR1.4 | Receive Yellow Alarm. Set when yellow alarm is detected. The format of yellow alarm is determined by RCR2.3 and RCR2.4. |
| RLOS | RSR1.3 | Receive Loss-of-Sync. Set when resync is in progress. |
| B8ZSD | RSR1.2 | B8ZS Codeword Detect. Set when a B8ZS codeword is received at RPOS and RNEG independent of whether the B8ZS mode is enabled or not (RCR2.2). |
| RBL | RSR1.1 | Receive Blue Alarm. Set when over a 3ms window, five or fewer 0's are received. Cleared when over a 3ms window, six or more 0's are received. |
| COFA | RSR1.0 | Change-of-Frame Alignment. Set when the last resync resulted in a change-of-frame or multiframe alignment. |

Note: Alarm 8ZD and 16ZD are cleared on the next occurrence of a 1 at RPOS and RNEG.

RECEIVE STATUS REGISTERS

The receive status registers (RSR1 and RSR2) can be used in either a polled or an interrupt configuration. In a polled configuration, the user reads the RSR at regular intervals to check for alarms. In an interrupt configuration, the user monitors the $\overline{\text{INT}}$ pin. When the $\overline{\text{INT}}$ pin goes low, an alarm condition has occurred and has been reported in one of the RSRs. The processor can then read the RSRs to find which bits have been set. All the bits in the receive status registers operate in a latched fashion. That is, once set, they remain set until read. The bits in the RSR are cleared when read unless the read was performed in the burst mode or the alarm condition still exists.

Yellow Alarm

193S Bit 2

If RCR2.4 = 0 and RCR2.3 = 0, then the DS2182A examines bit 2 of all incoming channels for the presence of a yellow alarm. If bit 2 is set to 0 in 256 consecutive channels, then the reception of a yellow alarm is declared. The alarm is considered cleared when the first channel with bit 2 set to a 1 is received.

193S S-Bit

If RCR2.4 = 0 and RCR2.3 = 1, then the DS2182A examines the S-bit position of frame 12 for the presence of a yellow alarm. The DS2182A declares the presence of a yellow alarm on the first occurrence of the S-bit in frame 12 being set to 1. The alarm is considered cleared when this S-bit returns to 0.

193E FDL

If RCR2.4 = 1, then the DS2182A examines the FDL for a repeating 00FF pattern. If this pattern is received in the FDL 16 consecutive times without error, then a yellow alarm is declared. The alarm is considered cleared as soon as any pattern other than 00FF is received.

RIMR1: Receive Interrupt Mask Register 1**MSB****LSB**

| | | | | | | | |
|-----|------|-----|------|------|-------|-----|------|
| 8ZD | 16ZD | RCL | RYEL | RLOS | B8ZSD | RBL | COFA |
|-----|------|-----|------|------|-------|-----|------|

| NAME | POSITION | FUNCTION |
|-------------|-----------------|--|
| 8ZD | RIMR1.7 | 8 Zero Detect Mask 1 = interrupt enabled 0 = interrupt masked |
| 16ZD | RIMR1.6 | 16 Zero Detect Mask 1 = interrupt enabled 0 = interrupt masked |
| RCL | RIMR1.5 | Receive Carrier Loss Mask 1 = interrupt enabled 0 = interrupt masked |
| RYEL | RIMR1.4 | Receive Yellow Alarm Mask 1 = interrupt enabled 0 = interrupt masked |
| RLOS | RIMR1.3 | Receive Loss-of-Sync Mask 1 = interrupt enabled 0 = interrupt masked |
| B8ZSD | RIMR1.2 | B8ZS Codeword Detect Mask 1 = interrupt enabled 0 = interrupt masked |
| RBL | RIMR1.1 | Receive Blue Alarm Mask 1 = interrupt enabled 0 = interrupt masked |
| COFA | RIMR1.0 | Change-of-Frame Alignment Mask 1 = interrupt enabled 0 = interrupt masked |

RSR2: Receive Status Register 2**MSB****LSB**

| | | | | | | | |
|------|------|------|------|------|-------|-------|-------|
| SEFE | RCLC | RBLC | FERR | FECS | OOFCS | CRCCS | BPVCS |
|------|------|------|------|------|-------|-------|-------|

| NAME | POSITION | FUNCTION |
|-------|----------|--|
| SEFE | RSR2.7 | Severely Errored Framing Event. Set when two out of six framing bits (Ft or FPS) are received in error. |
| RCLC | RSR2.6 | Receive Carrier Loss Clear. Set when the carrier signal is restored; remains set until read. |
| RBLC | RSR2.5 | Receive Blue Alarm Clear. Set when the Blue Alarm (AIS) is no longer detected; remains set until read. |
| FERR | RSR2.4 | Frame Bit Error. Set when FT (193S) or FPS (193E) bit errors occur. |
| FECS | RSR2.3 | Frame Error-Count Saturation. Set on the next frame error event after the 8-bit frame error-count register (FECE) saturates at 255. |
| OOFCS | RSR2.2 | Out-of-Frame Count Saturation. Set on the next OOF event after the 8-bit OOF Count Register (OOFCE) saturates at 255. |
| CRCCS | RSR2.1 | CRC Count Saturation. Set on the next CRC error event after the 8-bit CRC Count Register (CRCE) saturates at 255. |
| BPVCS | RSR2.0 | Bipolar Violation Count Saturation. Set on the next BPV error event after the 16-bit Bipolar Violation Count Register (BVCE) saturates at 65,535. |

RIMR2: Receive Interrupt Mask Register 2**MSB****LSB**

| | | | | | | | |
|------|------|------|------|------|-------|-------|-------|
| SEFE | RCLC | RBLC | FERR | FECS | OOFCS | CRCCS | BPVCS |
|------|------|------|------|------|-------|-------|-------|

| NAME | POSITION | FUNCTION |
|-------|----------|---|
| SEFE | RIMR2.7 | Severely Errored Framing-Event Mask 0 = interrupt masked 1 = interrupt enabled |
| RCLC | RIMR2.6 | Receive Carrier Loss Clear Mask 0 = interrupt masked 1 = interrupt enabled |
| RBLC | RIMR2.5 | Receive Blue Alarm Clear Mask 0 = interrupt masked 1 = interrupt enabled |
| FERR | RIMR2.4 | Frame Bit Error Mask 1 = interrupt enabled 0 = interrupt masked |
| FECS | RIMR2.3 | Frame Error-Count Saturation Mask 1 = interrupt enabled 0 = interrupt masked |
| OOFCS | RIMR2.2 | Out-of-Frame Count Saturation Mask 1 = interrupt enabled 0 = interrupt masked |
| CRCCS | RIMR2.1 | CRC Count Saturation Mask 1 = interrupt enabled 0 = interrupt masked |
| BPVCS | RIMR2.0 | Bipolar Violation Count Saturation Mask 1 = interrupt enabled 0 = interrupt masked |

RCR1: Receive Control Register 1**MSB****LSB**

| | | | | | | | |
|-----|------|------|-----|-------|-------|-------|--------|
| ARC | OOF1 | OOF2 | ACR | SYNCC | SYNCT | SYNCE | RESYNC |
|-----|------|------|-----|-------|-------|-------|--------|

| NAME | POSITION | FUNCTION |
|--------|----------|--|
| ARC | RCR1.7 | Auto Resync Criteria 1 = resync on OOF event only 0 = resync on OOF event or Receive Carrier Loss (RCL) |
| OOF1 | RCR1.6 | Out-of-Frame 1. OOF event description. Valid when RCR1.5 is cleared. 1 = 2 out of 5 frame bits (FT or FPS) in error 0 = 2 out of 4 frame bits (FT or FPS) in error |
| OOF2 | RCR1.5 | Out-of-Frame 2. OOF event description. 1 = 2 out of 6 frame bits (FT or FPS) in error 0 = follow OOF event described in RCR1.6 |
| ACR | RCR1.4 | Auto Counter Reset. When set, all four of the counters are reset to 0 when read. |
| SYNCC | RCR1.3 | Sync Criteria. Determines the type of algorithm used by the receive synchronizer; differs for each frame mode. 193S Framing (RCR2.4 = 0) 0 = synchronize to frame boundaries using FT pattern, then search for multiframe by using FS 1 = cross couple FT and FS patterns in sync algorithm 193E Framing (RCR2.4 = 1) 0 = normal sync (uses FPS only) 1 = validate new alignment with CRC before declaring sync |
| SYNCT | RCR1.2 | Sync Time 1 = validate 24 consecutive F-bits before declaring sync 0 = validate 10 consecutive F-bits before declaring sync |
| SYNCE | RCR1.1 | Sync Enable. If clear, the DS2182A automatically begins a resync if the conditions described in RCR1.7 are met. If set, no auto resync occurs. |
| RESYNC | RCR1.0 | Resync. When toggled low to high, the DS2182A initiates a resync immediately. The bit must be cleared and set again for subsequent resyncs. |

SYNCHRONIZER

The heart of the monitor is the receive synchronizer. This circuit serves two purposes: it monitors the incoming data stream for loss-of-frame or multiframe alignment, and it searches for a new frame alignment pattern when sync loss is detected. When sync loss is detected, the synchronizer begins an off-line search for the new alignment. All output timing signals remain at the old alignment with the exception of RSIGFR, which is forced low during resync. When one and only one candidate is qualified, the output timing moves to the new alignment at the beginning of the next multiframe. One frame later, RLOS transitions low, indicating valid sync and the resumption of the normal sync-monitoring mode. Several bits in the RCR1 allow tailoring of the resync algorithm by the user. These bits are described below.

Sync Criteria (RCR1.3)

193E

Bit RCR1.3 determines which sync algorithm is used when resync is in progress (RLOS = 1). In 193E framing, when RCR1.3 = 0, the synchronizer locks only to the FPS pattern and moves to the new frame and multiframe alignment after the framing candidate is qualified. RLOS goes low one frame after the move to the new alignment. When RCR1.3 = 1, the new alignment is further tested by a CRC6 code match. RLOS transitions low after a CRC6 match occurs. If no CRC6 match occurs in three attempts (three multiframes), the algorithm resets and a new search for the FPS pattern begins. It takes 9ms for the synchronizer to check the first CRC6 code after the new FPS alignment has been loaded. Each additional CRC6 test takes 3ms. Regardless of the state of RCR1.3, if more than one candidate exists after 24ms, the synchronizer begins eliminating emulators by testing their CRC6 codes in order to find the true framing candidate.

193S

In 193S framing, when RCR1.3 = 1, the synchronizer crosschecks the FT pattern with the FS pattern to help eliminate false-framing candidates such as digital milliwatts. The FS patterns are compared to the repeating pattern ...001111000111000...(001111x0 if RCR2.3 = 1). In this mode, FT and FS must be correctly identified by the synchronizer before sync is declared. Clearing RCR1.3 causes the synchronizer to search for the FT pattern (101010...) without cross-coupling the FS pattern. Frame sync is established using the FT information, while multiframe sync is established only if valid FS information is present. If no valid FS pattern is identified, the synchronizer moves to the FT alignment, RLOS goes low, and a false multiframe position can be indicated by RMSYNC. RFER indicates when the received S-bit pattern does not match the assumed internal multiframe alignment. This mode is used in applications where nonstandard S-bit patterns exist. In such applications, multiframe alignment information can be decoded externally by using the S-bits present at RLINK.

Sync Time (RCR1.2)

Bit RCR1.2 determines the number of consecutive framing pattern bits to be qualified before SYNC is declared. If RCR1.2 = 1, the algorithm validates 24 bits; if RCR1.2 = 0, 10 bits are validated. Validating 24 bits results in superior false-framing protection while 10-bit testing minimizes reframe time. In either case, the synchronizer only establishes resync when one and only one candidate is found (Table 4).

Table 4. Average Reframe Time

| FRAME MODE | RCR1.2 = 0 | | | RCR1.2 = 1 | | |
|------------|------------|--------|-------|------------|--------|--------|
| | MIN | AVG | MAX | MIN | AVG | MAX |
| 193S | 3.0ms | 3.75ms | 4.5ms | 6.5ms | 7.25ms | 8.0ms |
| 193E | 6.0ms | 7.5ms | 9.0ms | 13.0ms | 14.5ms | 16.0ms |

Note: Average reframe time is defined here as the average time it takes from the start of resync (rising edge of RLOS) to the actual loading of the new alignment (on a multiframe edge) into the output receive timing.

Sync Enable (RCR1.1)

When RCR1.1 is cleared, the receiver initiates automatic resync if an OOF event occurs or if carrier loss (192 consecutive 0's) occurs (depends on RCR1.7). When RCR1.1 is set, the automatic resync circuitry is disabled. In this case, resync can only be initiated by setting RCR1.0 to 1 or externally transitioning \overline{RST} from low to high. Note that using \overline{RST} to initiate a resync resets the output timing while \overline{RST} is low; use of RCR1.1 does not affect the output timing until the new alignment is located.

Resync (RCR1.0)

A 0-to-1 transition of RCR1.0 causes the synchronizer to search for the framing pattern sequence immediately, regardless of the internal sync status. To initiate another resync command, this bit must be cleared and then set again.

RCR2: Receive Control Register 2

MSB

LSB

| | | | | | | | |
|---|---|-------|----|-------|------|---|---|
| — | — | BVCRF | FM | SFYEL | B8ZS | — | — |
|---|---|-------|----|-------|------|---|---|

| NAME | POSITION | FUNCTION |
|-------|----------|--|
| — | RCR2.7 | Reserved ; must be 0 for proper operation |
| — | RCR2.6 | Reserved ; must be 0 for proper operation |
| BVCRF | RCR2.5 | Bipolar Violation Count Register Function Select 0 = do not count excessive 0's 1 = count excessive 0's |
| FM | RCR2.4 | Frame Mode 1 = Extended Superframe (193E, 24 frames per Superframe) 0 = Superframe (193S or D4, 12 frames per Superframe) |
| SFYEL | RCR2.3 | SF Yellow Mode Select 1 = 1 in the S-bit position of frame 12 0 = 0 in bit 2 of all channels |
| B8ZS | RCR2.2 | Bipolar Eight-Zero Substitution 1 = B8ZS enabled 0 = B8ZS disabled |
| — | RCR2.1 | Reserved ; must be 0 for proper operation |
| — | RCR2.10 | Reserved ; must be 0 for proper operation |

Figure 3. 193S Receive Multiframe Timing

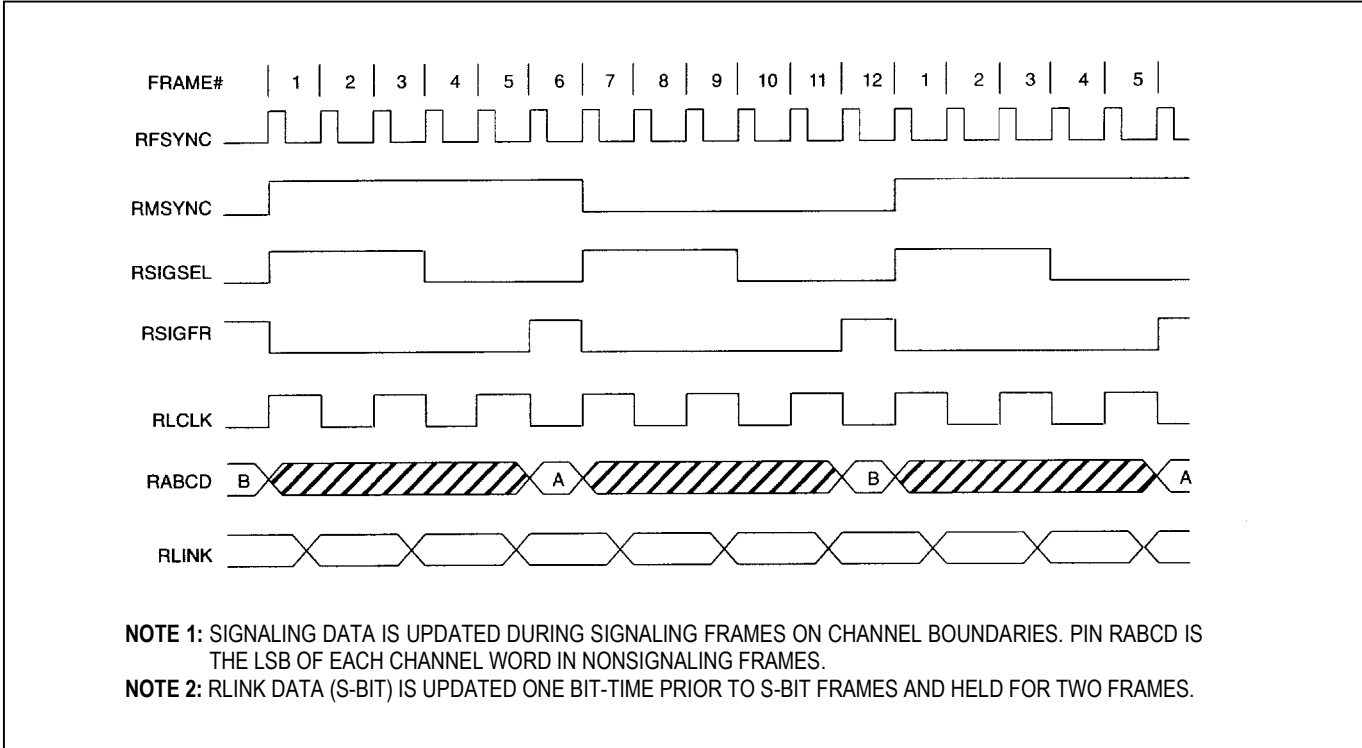


Figure 4. 193E Receive Multiframe Timing

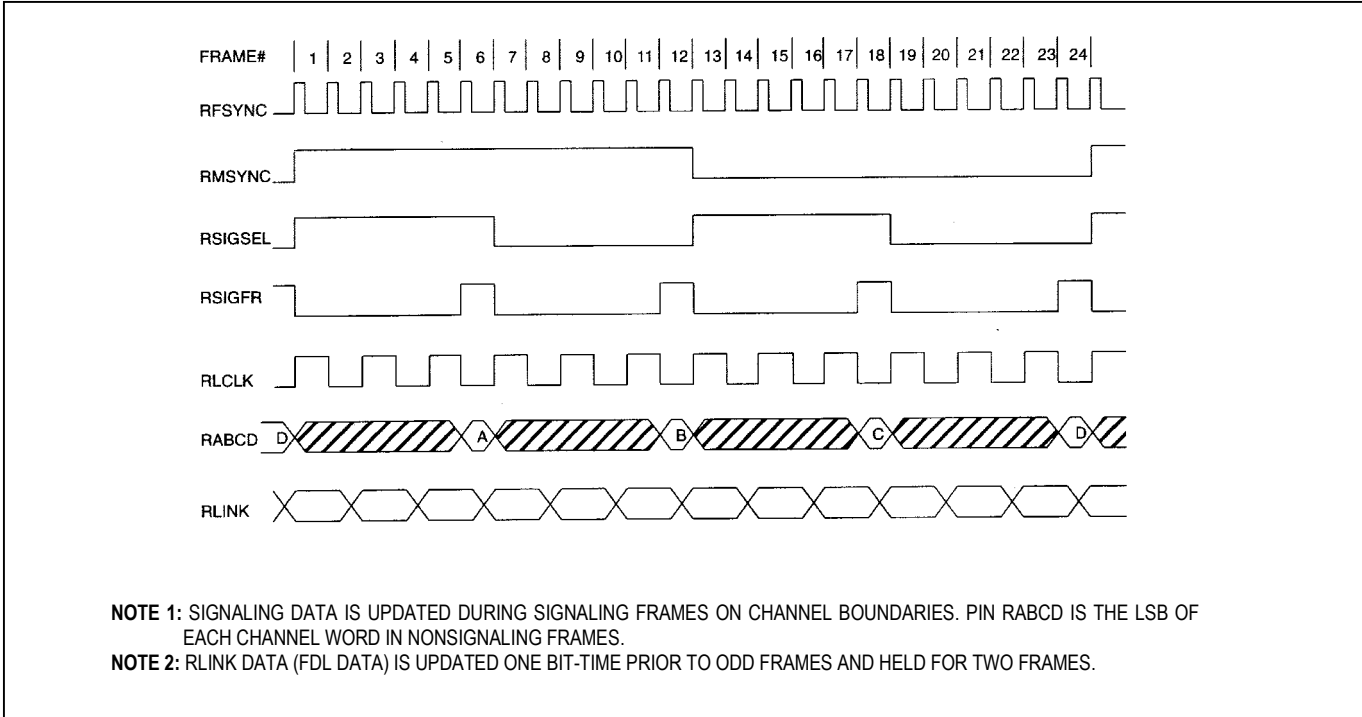
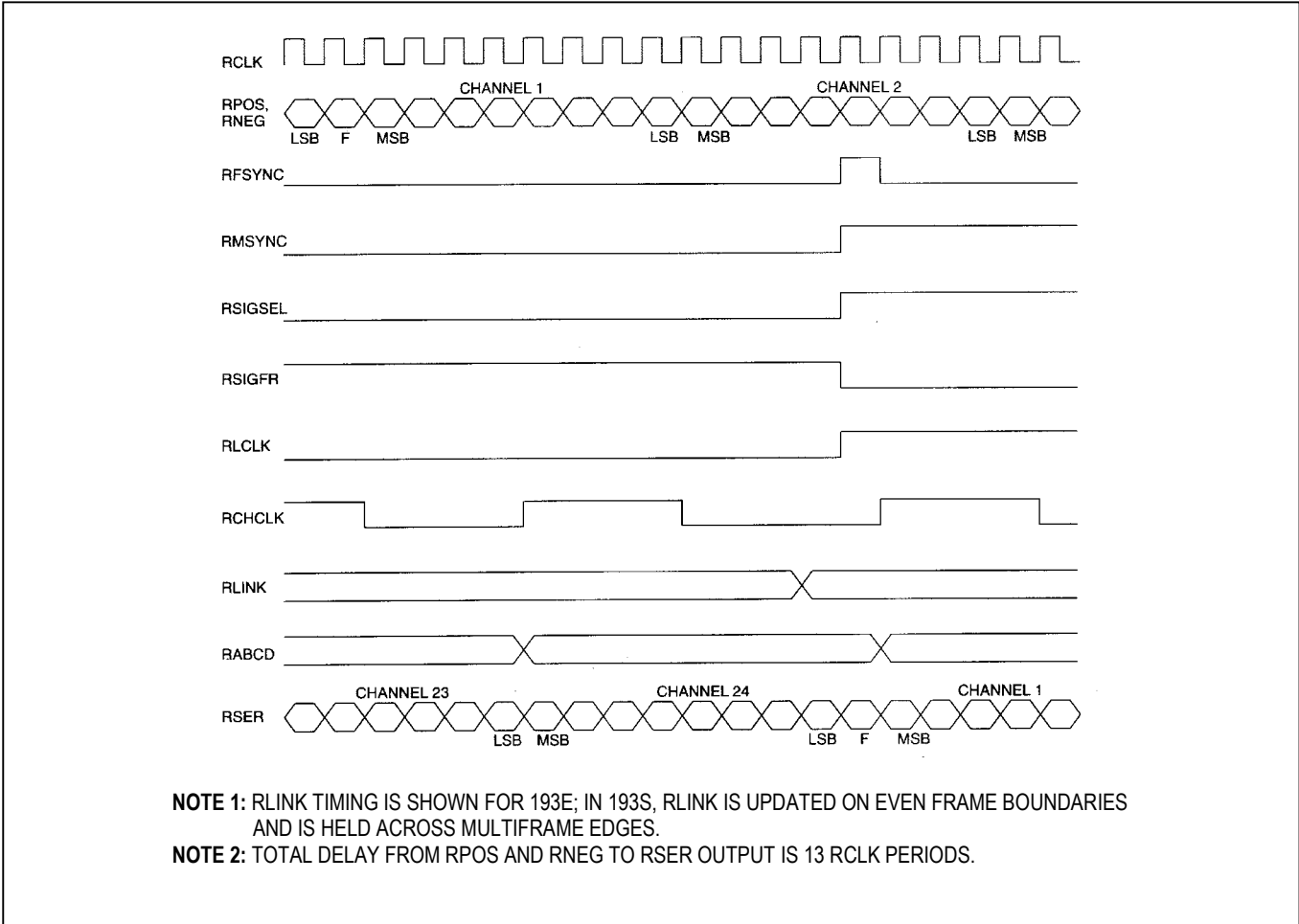


Figure 5. Receive Multiframed Boundary Timing



ALARM OUTPUTS

The transceiver also provides direct alarm outputs for applications when additional decoding and demuxing are required to supplement the on-board alarm logic.

RLOS Output

The receive loss-of-sync output indicates the status of the receiver synchronizer circuitry. When high, an off-line resynchronization is in progress and a high-low transition indicates that resync is complete. The RLOS bit (RSR1.3) is a latched version of the RLOS output. If the auto-resync mode is selected (RCR1.1 = 0), RLOS is a real-time indication of a carrier loss or OOF event occurrence.

RYEL Output

The yellow alarm output transitions high when a yellow alarm is detected. A high-low transition indicates the alarm condition has been cleared. The RYEL bit (RSR1.4) is a latched version of the RYEL output.

RBV Output

The bipolar violation output transitions high when the accused bit emerges at RSER. RBV goes low at the next bit time if no additional violations are detected.

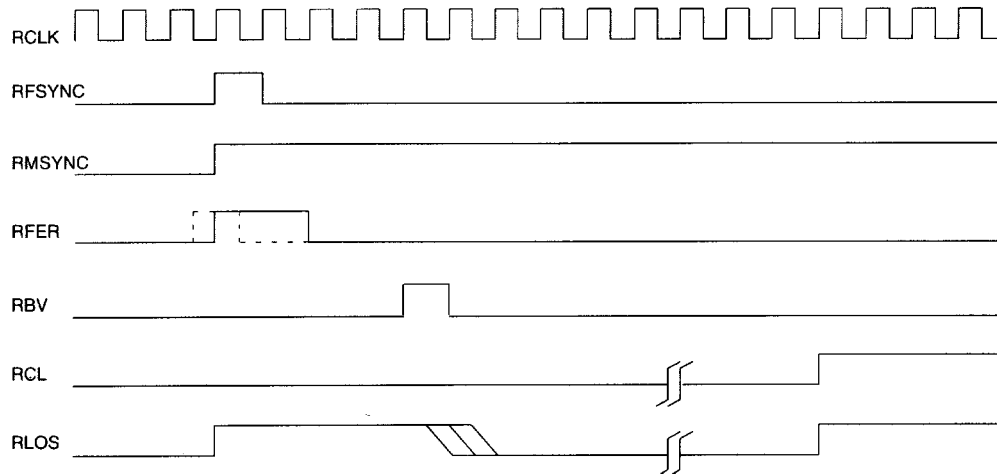
RFER Output

The receive frame-error output transitions high at the F-bit time and is held high for 2-bit periods when a frame bit error occurs. In 193S, framing FT and FS patterns are tested. The FPS pattern is tested in 193E framing. Additionally, in 193E framing, RFER reports CRC6 codeword errors by a low-high-low transition (1-bit period-wide) one-half RCLK period before a low-high transition on RMSYNC ([Figure 6](#)).

Reset ($\overline{\text{RST}}$)

A high-low transition on $\overline{\text{RST}}$ clears all registers and forces an immediate resync when $\overline{\text{RST}}$ returns high. $\overline{\text{RST}}$ must be held low on system power-up to ensure proper initialization of the counters and registers. Following reset, the host processor should restore all control modes by writing appropriate registers with control data.

Figure 6. Alarm Output Timing



- NOTE 1:** RFER TRANSITIONS HIGH DURING F-BIT TIME IF RECEIVED FRAMING PATTERN BIT IS IN ERROR. (FRAME 12 F-BITS IN 193S ARE IGNORED IF RCR2.3 = 1.) ALSO, IN 193E, RFER TRANSITIONS HIGH ONE-HALF BIT-TIME BEFORE RISING EDGE OF RMSYNC TO INDICATE A CRC6 ERROR FOR THE PREVIOUS MULTIFRAME.
- NOTE 2:** RBV INDICATES RECEIVED BIPOLAR VIOLATION AND TRANSITIONS HIGH WHEN ACCUSED BIT EMERGES FROM RSER. IF B8ZS IS ENABLED, RBV DOES NOT REPORT THE ZERO REPLACEMENT CODE.
- NOTE 3:** RCL TRANSITIONS HIGH WHEN 192 CONSECUTIVE BITS ARE 0; RCL TRANSITIONS LOW UPON RECEPTION OF 12.5% 1'S DENSITY.
- NOTE 4:** RLOS TRANSITIONS HIGH DURING F-BIT TIME THAT CAUSED AN OOF EVENT IF AUTO-RESYNC IS ENABLED (RCR1.1 = 0). RESYNC ALSO OCCURS WHEN LOSS-OF-CARRIER IS DETECTED (RCL = 1) IF RCR1.7 = 0. WHEN RCR1.1 = 1, RLOS REMAINS LOW UNTIL RESYNC OCCURS, REGARDLESS OF OOF OR CARRIER LOSS FLAGS. IN THIS SITUATION, RESYNC IS INITIATED ONLY WHEN RCR1.0 TRANSITIONS LOW-TO-HIGH OR THE $\overline{\text{RST}}$ PIN TRANSITIONS HIGH-LOW-HIGH.

ABSOLUTE MAXIMUM RATINGS

| | |
|--|--------------------------|
| Voltage Range on Any Pin Relative to Ground..... | -0.1V to +7.0V |
| Operating Temperature Range..... | 0°C to +70°C |
| Storage Temperature Range..... | -55°C to +125°C |
| Soldering Temperature..... | See IPC/JEDEC J-STD-020A |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device.

RECOMMENDED DC OPERATING CONDITIONS

($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---------------|----------|------|-----|----------------|-------|-------|
| Input Logic 1 | V_{IH} | 2.0 | | $V_{CC} + 0.3$ | V | 1 |
| Input Logic 0 | V_{IL} | -0.3 | | +0.8 | V | |
| Supply | V_{DD} | 4.50 | | 5.50 | V | |

DC ELECTRICAL CHARACTERISTICS

($V_{DD} = 5V \pm 10\%$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$.)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|-----------------------|----------|------|-----|------|---------------|-------|
| Supply Current | I_{DD} | | 3 | | mA | 2, 3 |
| Input Leakage | I_L | -1.0 | | +1.0 | μA | 4 |
| Output Current (2.4V) | I_{OH} | -1.0 | | | mA | 5 |
| Output Current (0.4V) | I_{OL} | +4.0 | | | mA | 6 |
| Output Leakage | I_{LO} | -1.0 | | +1.0 | μA | 7 |

CAPACITANCE

($T_A = +25^\circ\text{C}$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|--------------------|-----------|-----|-----|-----|-------|-------|
| Input Capacitance | C_{IN} | | | 5 | pF | |
| Output Capacitance | C_{OUT} | | | 7 | pF | |

Note 1: RCLK, SCLK, and RST $V_{IH(MIN)} = 2.4V$.

Note 2: RCLK = 1.544MHz

Note 3: Outputs open.

Note 4: $0V < V_{IN} < V_{DD}$

Note 5: All outputs except \overline{INT} , which is open-collector.

Note 6: All outputs.

Note 7: Applies to SDO when tri-stated.

CHARACTERISTICS—SERIAL PORT(V_{DD} = 5V ±10%, T_A = 0°C to +70°C.) (Notes 1 and 2) (See [Figure 7](#) and [Figure 8](#))

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|--------------------------------------|---------------------------------|-----|-----|-----|-------|
| SDI to SCLK Setup | t _{DC} | 50 | | | ns |
| SCLK to SDI Hold | t _{CHD} | 50 | | | ns |
| SDI to SCLK Falling Edge | t _{CD} | 50 | | | ns |
| SCLK Low Time | t _{CL} | 250 | | | ns |
| SCLK High Time | t _{CH} | 250 | | | ns |
| SCLK Rise and Fall Times | t _R , t _F | | | 100 | ns |
| $\overline{\text{CS}}$ to SCLK Setup | t _{CC} | 50 | | | ns |
| SCLK to $\overline{\text{CS}}$ Hold | t _{CCH} | 50 | | | ns |
| $\overline{\text{CS}}$ Inactive Time | t _{CWH} | 2.5 | | | μs |
| SCLK to SDO Valid | t _{CDV} | | | 200 | ns |
| $\overline{\text{CS}}$ to SDO High-Z | t _{CDZ} | | | 75 | ns |

Note 1: Measured at V_{IH} = 2.0 or V_{IL} = 0.8 and 10ns maximum rise and fall time.**Note 2:** Output load capacitance = 100pF.

AC ELECTRICAL CHARACTERISTICS—RECEIVE(V_{DD} = 5.0V ±10%, T_A = 0°C to +70°C) (Notes 1 and 2) (See [Figure 9](#))

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---------------------------------|-----|-----|-----|-------|
| Propagation Delay RCLK to RMSYNC, RFSYNC, RSISEL, RSIGFR, RLCLK, RCHCLK | t _{PRS} | | | 75 | ns |
| Propagation Delay RCLK to RSER, RABCD, RLINK | t _{PRD} | | | 75 | ns |
| Transition Time, All Outputs | t _{TTR} | | | 20 | ns |
| RCLK Period | t _P | | 648 | | ns |
| RCLK Pulse Width | t _R , t _F | | 324 | | ns |
| RCLK Rise and Fall Times | t _{CCH} | | 20 | | ns |
| RPOS, RNEG Setup to RCLK Falling | t _{SRD} | 50 | | | ns |
| RPOS, RNEG Hold to RCLK Falling | t _{HRD} | 50 | | | ns |
| Propagation Delay RCLK to RLOS, RYEL, RBV, RCL, RFER | t _{PRA} | | | 75 | ns |
| Minimum $\overline{\text{RST}}$ Pulse Width | t _{RST} | 1 | | | μs |

Note 1: Measured at V_{IH} = 2.0 or V_{IL} = 0.8 and 10ns maximum rise and fall time.**Note 2:** Output load capacitance = 100pF.

Figure 7. Serial Port Write AC Timing Diagram

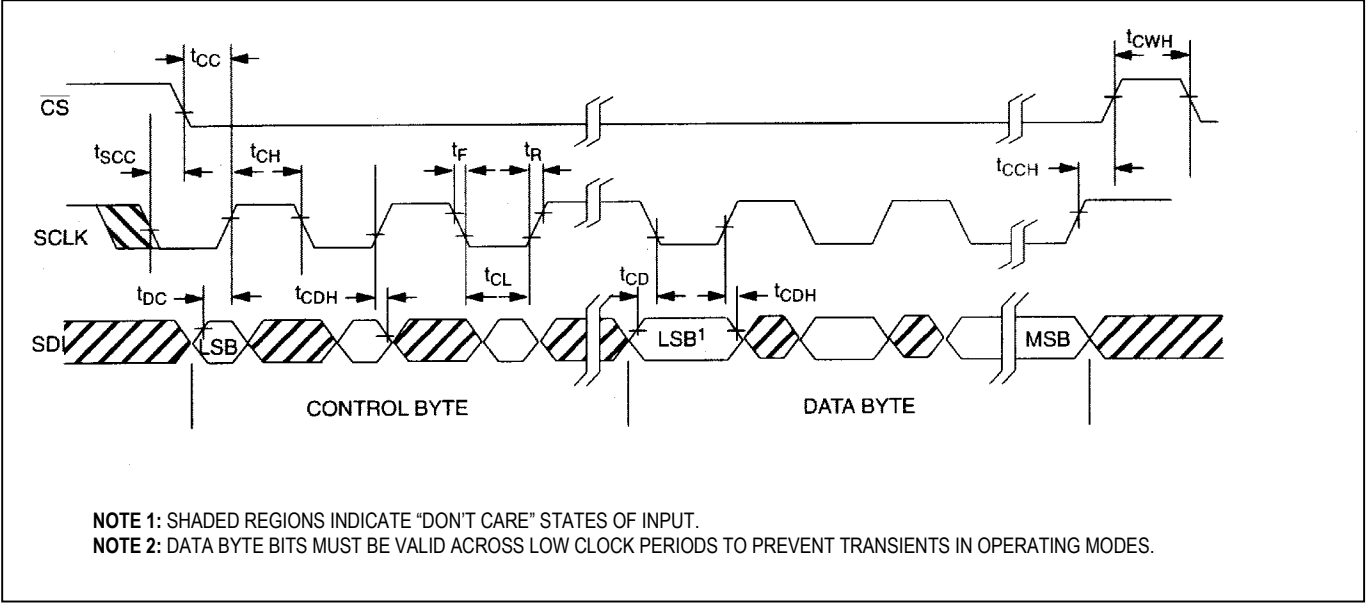


Figure 8. Serial Port Read AC Timing Diagram

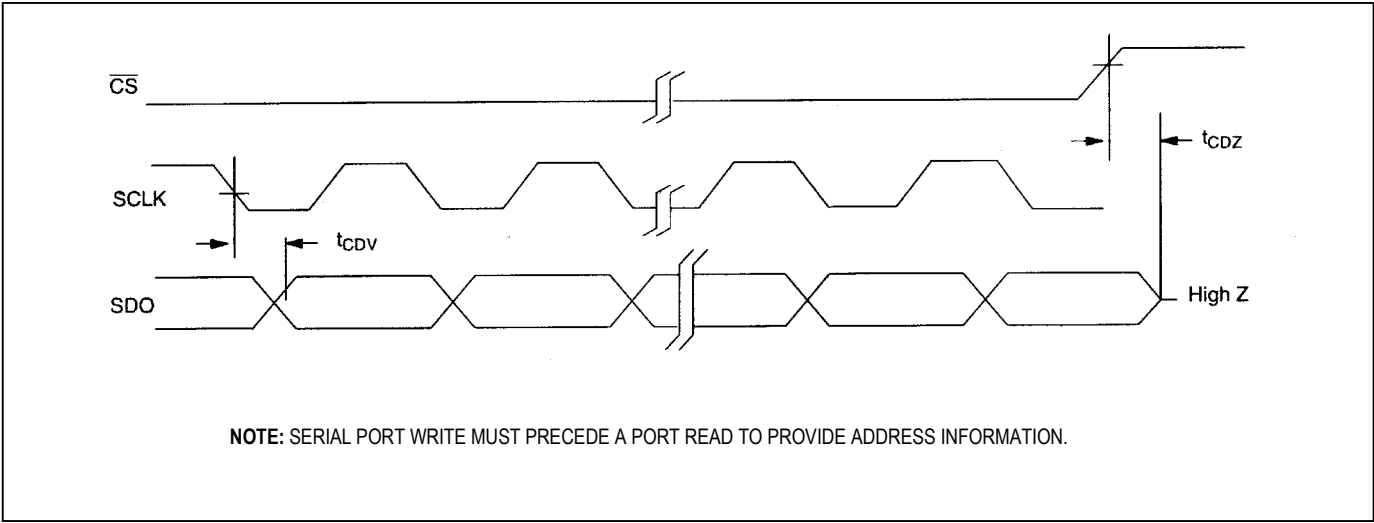
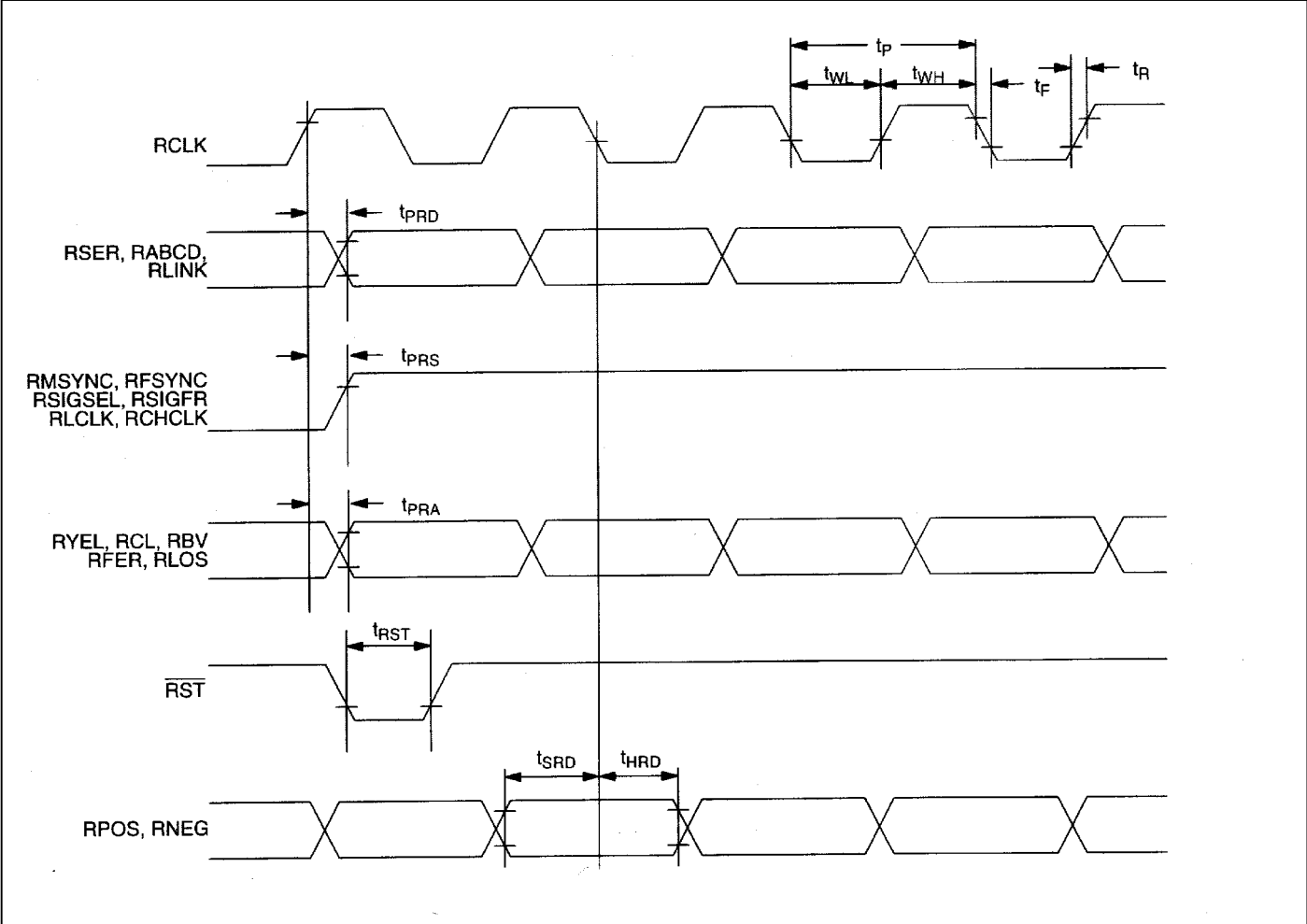


Figure 9. Receive AC Timing Diagram

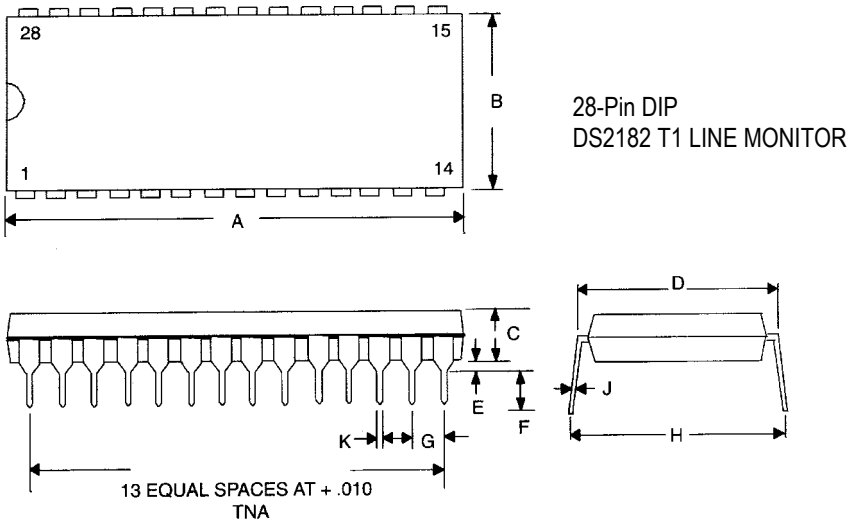


REVISION HISTORY

| DATE | DESCRIPTION |
|--------|---|
| 092299 | Original release. |
| 080802 | Changed typo in <i>Pin Description</i> for ESIGRF to RSIGFR. Added Note 1 to Input Logic 1, V_{IH} spec in the <i>Recommended DC Operating Characteristics</i> table. [Note 1: RCLK, SCLK, and RST $V_{IH (MIN)} = 2.4V$.] Note was added to match the device characterization. No changes were made to fit, form, or function of production units. |
| 120103 | Changed ordering information. |

PACKAGE INFORMATION

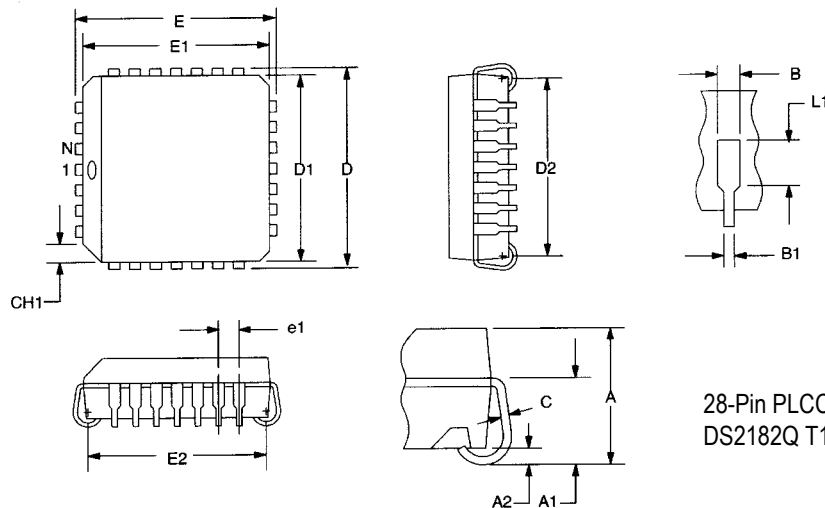
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/DallasPackInfo.)



| DIM | INCHES | |
|-----|--------|-------|
| | MIN | MAX |
| A | 1.445 | 1.470 |
| B | 0.530 | 0.550 |
| C | 0.140 | 0.160 |
| D | 0.600 | 0.625 |
| E | 0.015 | 0.040 |
| F | 0.120 | 0.145 |
| G | 0.090 | 0.110 |
| H | 0.600 | 0.680 |
| J | 0.008 | 0.012 |
| K | 0.015 | 0.022 |

PACKAGE INFORMATION (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/DallasPackInfo.)



28-Pin PLCC
DS2182Q T1 LINE MONITOR

| DIM | INCHES | |
|----------|-----------|-------|
| | MIN | MAX |
| A | 0.165 | 0.180 |
| A1 | 0.090 | 0.120 |
| A2 | 0.020 | — |
| B | 0.026 | 0.033 |
| B1 | 0.013 | 0.021 |
| C | 0.009 | 0.012 |
| D | 0.485 | 0.495 |
| D1 | 0.450 | 0.456 |
| D2 | 0.390 | 0.430 |
| E | 0.485 | 0.495 |
| E1 | 0.450 | 0.456 |
| E2 | 0.390 | 0.430 |
| L1 | 0.060 | — |
| N | 28 | — |
| e1 | 0.050 BSC | |
| CH1 | 0.042 | 0.048 |



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