



# 45 $\mu\text{V}$ Offset, 0.4 $\mu\text{V}/^\circ\text{C}$ , Zero-Drift Operational Amplifier

## NCS21871, NCV21871, NCS21872, NCV21872, NCS21874, NCV21874

The NCS21871, NCS21872 and NCS21874 family of zero-drift op amps feature offset voltage as low as 45  $\mu\text{V}$  over the 1.8 V to 5.5 V supply voltage range. The zero-drift architecture reduces the offset drift to as low as 0.4  $\mu\text{V}/^\circ\text{C}$  and enables high precision measurements over both time and temperature. This family has low power consumption over a wide dynamic range and is available in space saving packages. These features make it well suited for signal conditioning circuits in portable, industrial, automotive, medical and consumer markets.

### Features

- Gain-Bandwidth Product: 270 kHz to 350 kHz
- Low Supply Current: 17  $\mu\text{A}$  (typ at 3.3 V)
- Low Offset Voltage: 45  $\mu\text{V}$  max
- Low Offset Drift: 0.4  $\mu\text{V}/^\circ\text{C}$  max
- Wide Supply Range: 1.8 V to 5.5 V
- Wide Temperature Range:  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$
- Rail-to-Rail Input and Output
- Available in Single, Dual and Quad Packages
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

### Applications

- Automotive
- Battery Powered/ Portable Application
- Sensor Signal Conditioning
- Low Voltage Current Sensing
- Filter Circuits
- Bridge Circuits
- Medical Instrumentation



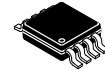
SOT23-5  
 SN SUFFIX  
 CASE 483



SC70-5  
 SQ SUFFIX  
 CASE 419A



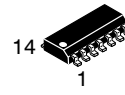
UDFN8  
 MU SUFFIX  
 CASE 517AW



MSOP-8  
 DM SUFFIX  
 CASE 846A-02



SOIC-8  
 D SUFFIX  
 CASE 751



SOIC-14  
 D SUFFIX  
 CASE 751A



TSSOP-14 WB  
 DT SUFFIX  
 CASE 948G



ECP5  
 FCT SUFFIX  
 CASE 971BE

### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 2 of this data sheet.

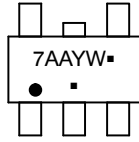
### ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

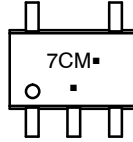
NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 3.

DEVICE MARKING INFORMATION

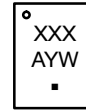
Single Channel Configuration  
NCS21871, NCV21871



TSOP-5/SOT23-5  
CASE 483

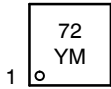


SC70-5  
CASE 419A

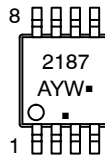


ECP5  
CASE 971BE

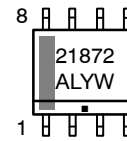
Dual Channel Configuration  
NCS21872, NCV21872



UDFN8, 2x2, 0.5P  
CASE 517AW

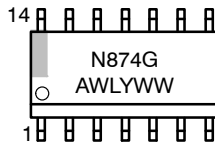


Micro8/MSOP8  
CASE 846A-02

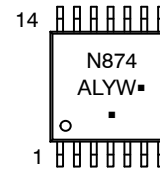


SOIC-8  
CASE 751

Quad Channel Configuration  
NCS21874, NCV21874



SOIC-14  
CASE 751A



TSSOP-14 WB  
CASE 948G

N874 = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
M = Date Code  
G or ■ = Pb-Free Package

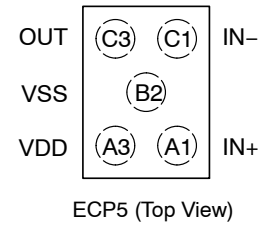
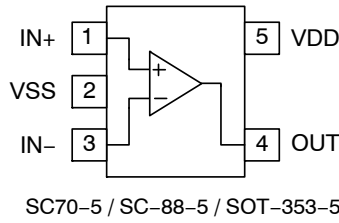
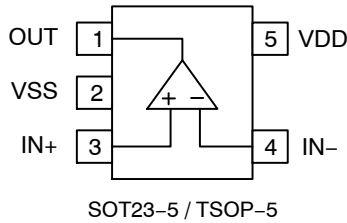
N874 = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
■ = Pb-Free Package

(Note: Microdot may be in either location)

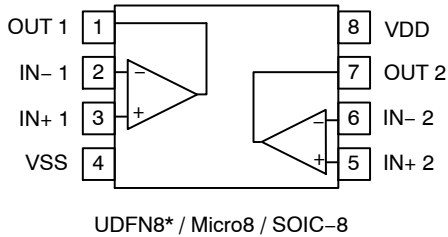
# NCS21871, NCV21871, NCS21872, NCV21872, NCS21874, NCV21874

## PIN CONNECTIONS

### Single Channel Configuration NCS21871, NCV21871

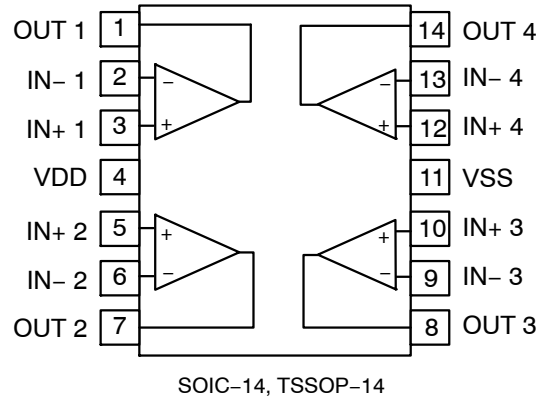


### Dual Channel Configuration NCS21872, NCV21872



\*The exposed pad of the UDFN8 package can be floated or connected to VSS.

### Quad Channel Configuration NCS21874, NCV21874



## ORDERING INFORMATION

Device Part Number	Temperature	Channels	Package	Shipping †
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### COMMERCIAL AND INDUSTRIAL

NCS21871SN2T1G	-40°C to 125°C	Single	SOT23-5 / TSOP-5	3000 / Tape & Reel
NCS21871SQ3T2G			SC70-5 / SC-88-5 / SOT-353-5	
NCS21872DMR2G		Dual	MICRO-8	4000 / Tape & Reel
NCS21872DR2G			SOIC-8	3000 / Tape & Reel
NCS21874DR2G		Quad	SOIC-14	2500 / Tape & Reel
NCS21874DTBR2G			TSSOP-14	

### AUTOMOTIVE

NCV21871SN2T1G	-40°C to 125°C	Single	SOT23-5 / TSOP-5	3000 / Tape & Reel
NCV21871SQ3T2G			SC70-5 / SC-88-5 / SOT-353-5	
NCV21872DMR2G		Dual	MICRO-8	4000 / Tape & Reel
NCV21872DR2G			SOIC-8	3000 / Tape & Reel
NCV21874DR2G		Quad	SOIC-14	2500 / Tape & Reel
NCV21874DTBR2G			TSSOP-14	

### DISCONTINUED (Note 1)

NCS21871FCTTAG	-40°C to 125°C	Single	ECP5	3000 / Tape & Reel
NCS21872MUTBG	-40°C to 125°C	Dual	UDFN-8	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

1. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on [www.onsemi.com](http://www.onsemi.com).

# NCS21871, NCV21871, NCS21872, NCV21872, NCS21874, NCV21874

**ABSOLUTE MAXIMUM RATING** Over operating free-air temperature, unless otherwise stated.

Parameter	Rating	Unit
Supply Voltage	6	V

## INPUT AND OUTPUT PINS

Input Voltage (Note 2)	(VSS) – 0.3 to (VDD) + 0.3	V
Input Current (Note 2)	±10	mA
Output Short Circuit Current (Note 3)	Continuous	

## TEMPERATURE

Operating Temperature Range	–40 to +125	°C
Storage Temperature Range	–65 to +150	°C
Junction Temperature	+150	°C

## ESD RATINGS (Note 4)

Human Body Model (HBM)	±4000	V
Charged Device Model (CDM)	±2000	V

## OTHER RATINGS

Latch-up Current (Note 5)	100	mA
MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less
- Short-circuit to ground.
- This device series incorporates ESD protection and is tested by the following methods:  
ESD Human Body Model tested per JEDEC standard JS-001 (AEC-Q100-002)  
ESD Charged Device Model tested per JEDEC standard JESD22-C101 (AEC-Q100-011)
- Latch-up Current tested per JEDEC standard: JESD78.

## THERMAL INFORMATION (Note 6)

Symbol	Parameter	Package	Value	Unit
$\theta_{JA}$	Thermal Resistance, Junction to Ambient	SOT23-5 / TSOP5	290	°C/W
		SC70-5 / SC-88-5 / SOT-353-5	290	
		ECP5	157	
		Micro8 / MSOP8	298	
		SOIC-8	250	
		UDFN8	228	
		SOIC-14	216	
		TSSOP-14	155	

- As mounted on an 80x80x1.5 mm FR4 PCB with 650 mm<sup>2</sup> and 2 oz (0.07 mm) thick copper heat spreader. Following JEDEC JESD/EIA 51.1, 51.2, 51.3 test guidelines

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Range	Unit
V <sub>S</sub>	Supply Voltage (V <sub>DD</sub> – V <sub>SS</sub> )	1.8 to 5.5	V
T <sub>A</sub>	Specified Operating Temperature Range	–40 to 125	°C
V <sub>CM</sub>	Input Common Mode Voltage Range	V <sub>SS</sub> -0.1 to V <sub>DD</sub> +0.1	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# NCS21871, NCV21871, NCS21872, NCV21872, NCS21874, NCV21874

## ELECTRICAL CHARACTERISTICS: $V_S = 1.8\text{ V to }5.5\text{ V}$

At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to midsupply,  $V_{CM} = V_{OUT} = \text{midsupply}$ , unless otherwise noted.

**Boldface** limits apply over the specified operating temperature range, guaranteed by characterization and/or design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>INPUT CHARACTERISTICS</b>							
$V_{OS}$	Offset Voltage	$V_S = +5\text{ V}$	-	6	45	$\mu\text{V}$	
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift vs Temp	$V_S = 5\text{ V}$	-	<b>0.1</b>	<b>0.4</b>	$\mu\text{V}/^\circ\text{C}$	
$\Delta V_{OS}/\Delta V_S$	Offset Voltage Drift vs Supply	$T_A = +25^\circ\text{C}$	-	0.4	8	$\mu\text{V}/\text{V}$	
		Full temperature range	-		<b>12.6</b>		
$I_{IB}$	Input Bias Current (Note 7)	$T_A = +25^\circ\text{C}$	-	$\pm 60$	$\pm 400$	$\text{pA}$	
		Full temperature range	-	<b><math>\pm 400</math></b>			
$I_{OS}$	Input Offset Current (Note 7)	$T_A = +25^\circ\text{C}$	-	$\pm 50$	$\pm 800$	$\text{pA}$	
CMRR	Common Mode Rejection Ratio (Note 8)	$V_S = 1.8\text{ V}$	-	111	-	dB	
		$V_S = 3.3\text{ V}$	-	118	-		
		$V_S = 5.0\text{ V}$	102	123	-		
		$V_S = 5.5\text{ V}$	-	127	-		
$C_{IN}$	Input Capacitance	Differential	-	4.1	-	$\text{pF}$	
		Common Mode	-	7.9	-		
<b>OUTPUT CHARACTERISTICS</b>							
$A_{VOL}$	Open Loop Voltage Gain (Note 7)	$V_{SS} + 100\text{ mV} < V_O < V_{DD} - 100\text{ mV}$	<b>106</b>	145	-	dB	
$Z_{out-OL}$	Open Loop Output Impedance		See Figure 18			$\Omega$	
$V_{OH}$	Output Voltage High, Referenced to $V_{DD}$	$T_A = +25^\circ\text{C}$	-	10	80	mV	
		Full temperature range	-	-	<b>80</b>		
$V_{OL}$	Output Voltage Low, Referenced to $V_{SS}$	$T_A = +25^\circ\text{C}$	-	10	80	mV	
		Full temperature range	-	-	<b>80</b>		
$I_O$		Sinking Current	-	11	-	mA	
		Sourcing Current	-	5.0	-		
$C_L$	Capacitive Load Drive		See Figure 14				
<b>NOISE PERFORMANCE</b>							
$e_N$	Voltage Noise Density	$f_{IN} = 1\text{ kHz}$	-	62	-	$\text{nV} / \sqrt{\text{Hz}}$	
$e_{P-P}$	Voltage Noise	$f_{IN} = 0.1\text{ Hz to }10\text{ Hz}$	-	1.1	-	$\mu\text{V}_{PP}$	
		$f_{IN} = 0.01\text{ Hz to }1\text{ Hz}$	-	0.5	-		
$i_N$	Current Noise Density	$f_{IN} = 10\text{ Hz}$	-	350	-	$\text{fA} / \sqrt{\text{Hz}}$	
	Channel Separation	NCS21872, NCS21874	-	135	-	dB	
<b>DYNAMIC PERFORMANCE</b>							
GBWP	Gain Bandwidth Product	$C_L = 100\text{ pF}$	NCS21871, NCS21874	-	350	-	kHz
			NCS21872	-	270	-	
$A_M$	Gain Margin	$C_L = 100\text{ pF}$	-	18	-	dB	
$\phi_M$	Phase Margin	$C_L = 100\text{ pF}$	-	55	-	$^\circ$	
SR	Slew Rate	$G = 1, V_{DD} = 5.5\text{ V}$	-	0.1	-	$\text{V}/\mu\text{s}$	
		$G = 1, V_{DD} = 1.8\text{ V}$	-	0.05	-		
<b>POWER SUPPLY</b>							
PSRR	Power Supply Rejection Ratio	$T_A = +25^\circ\text{C}$	106	130	-	dB	
		Full temperature range	<b>98</b>	-	-		
$t_{ON}$	Turn-on Time	$V_S = 5\text{ V}$	-	100	-	$\mu\text{s}$	

# NCS21871, NCV21871, NCS21872, NCV21872, NCS21874, NCV21874

**ELECTRICAL CHARACTERISTICS:**  $V_S = 1.8\text{ V to }5.5\text{ V}$

At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to midsupply,  $V_{CM} = V_{OUT} = \text{midsupply}$ , unless otherwise noted.

**Boldface** limits apply over the specified operating temperature range, guaranteed by characterization and/or design. (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>POWER SUPPLY</b>						
$I_Q$	Quiescent Current (Note 9)	$1.8\text{ V} \leq V_S \leq 3.3\text{ V}$	-	20	40	$\mu\text{A}$
			-	-	<b>40</b>	
		$3.3\text{ V} < V_S \leq 5.5\text{ V}$	-	28	45	
			-	-	<b>45</b>	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- 7. Guaranteed by characterization and/or design
- 8. Specified over the full common mode range:  $V_{SS} - 0.1 < V_{CM} < V_{DD} + 0.1$
- 9. No load, per channel

TYPICAL CHARACTERISTICS

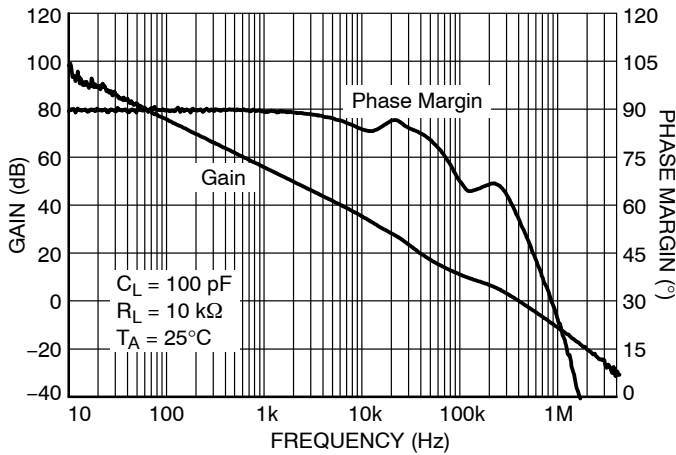


Figure 1. Open Loop Gain and Phase Margin vs. Frequency

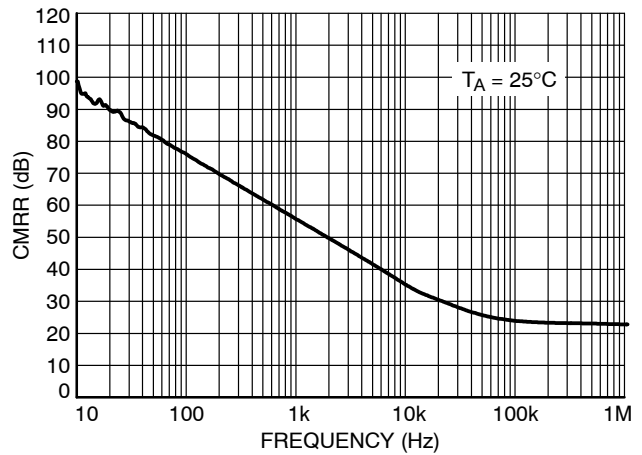


Figure 2. CMRR vs. Frequency

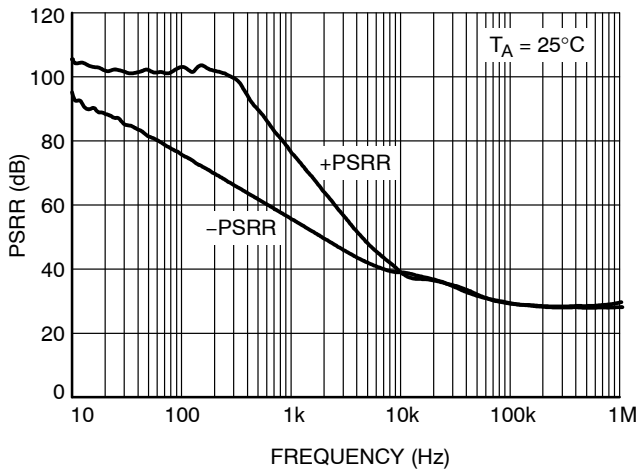


Figure 3. PSRR vs. Frequency

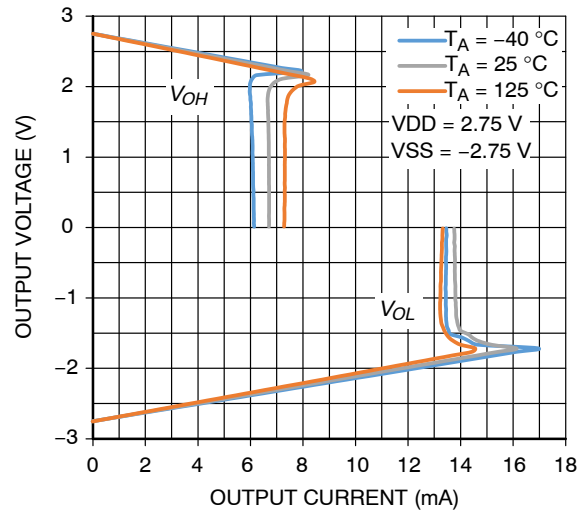


Figure 4. Output Voltage Swing vs. Output Current at  $V_S = 5.5\text{ V}$

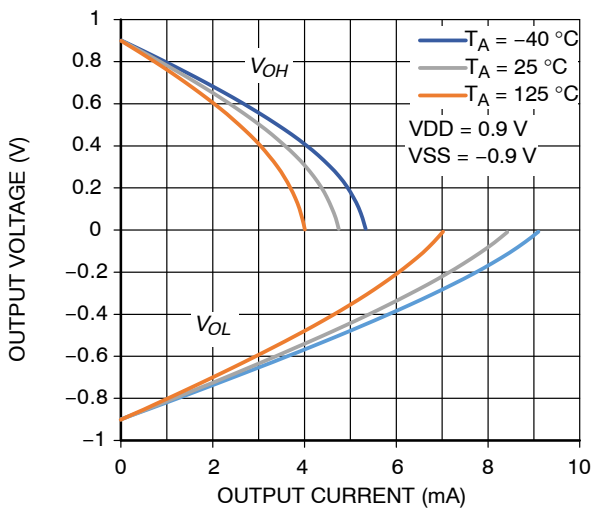


Figure 5. Output Voltage Swing vs. Output Current at  $V_S = 1.8\text{ V}$

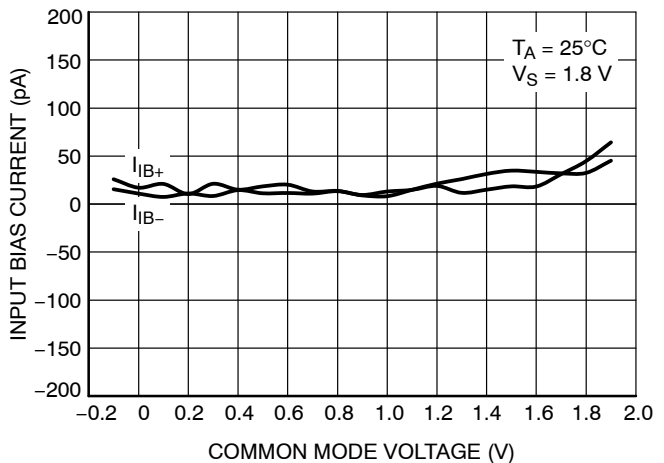


Figure 6. Input Bias Current vs. Common Mode Voltage

TYPICAL CHARACTERISTICS (continued)

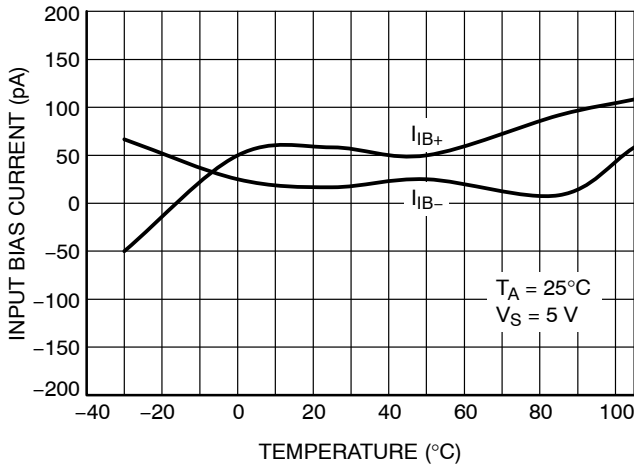


Figure 7. Input Bias Current vs. Temperature

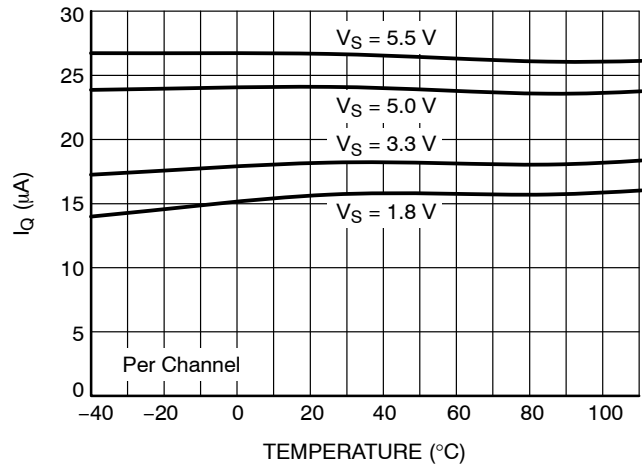


Figure 8. Quiescent Current vs. Temperature

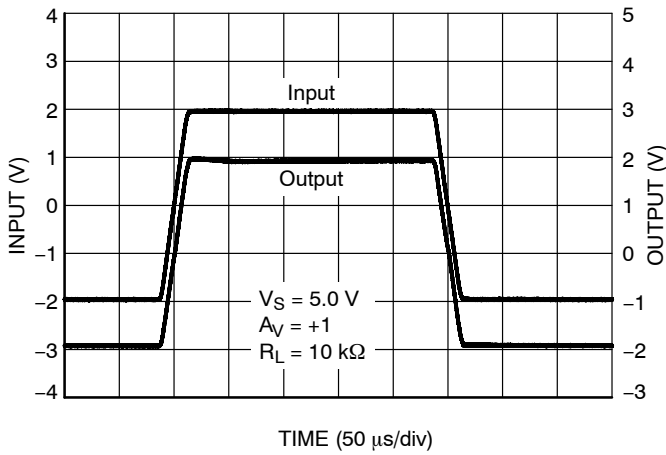


Figure 9. Large Signal Step Response

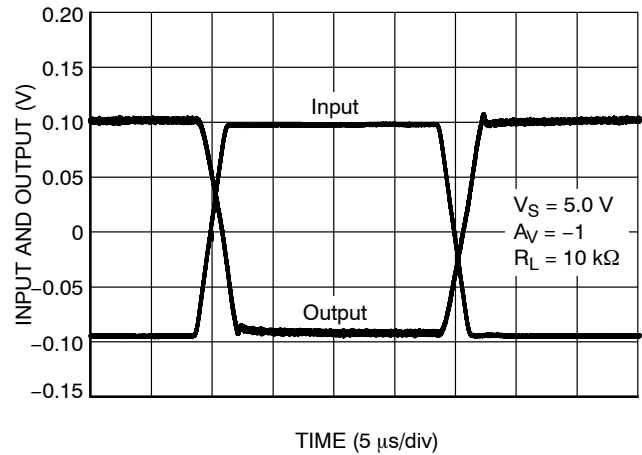


Figure 10. Small Signal Step Response

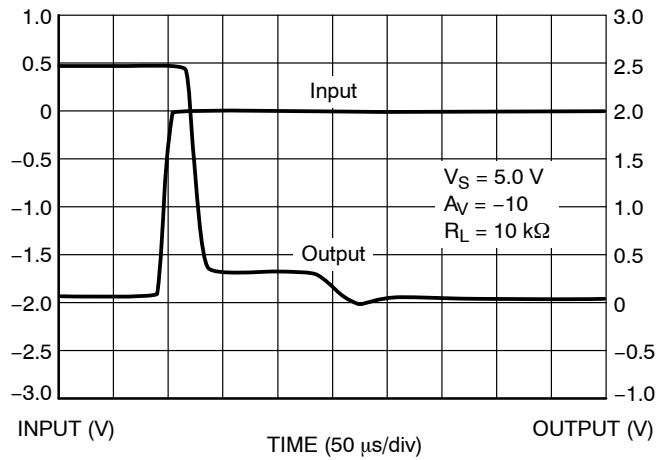


Figure 11. Positive Overtolerance Recovery

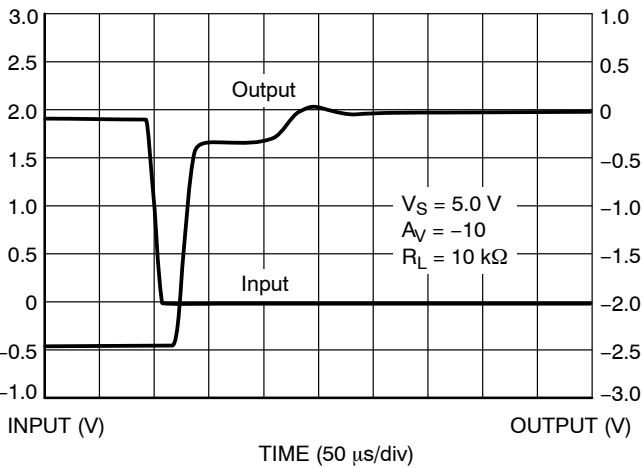


Figure 12. Negative Overtolerance Recovery

TYPICAL CHARACTERISTICS (continued)

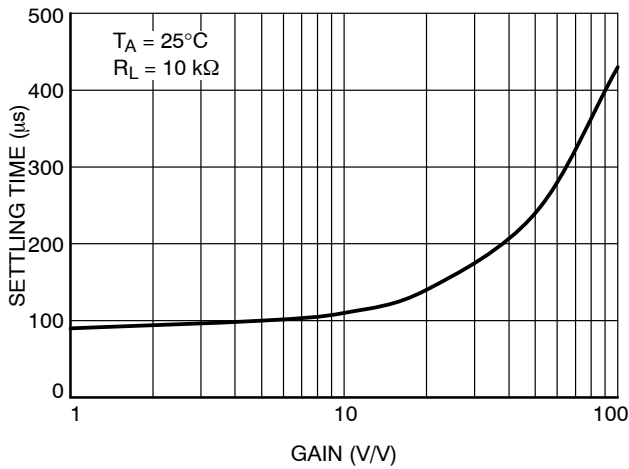


Figure 13. Setting Time to 0.1% vs. Closed-Loop Gain

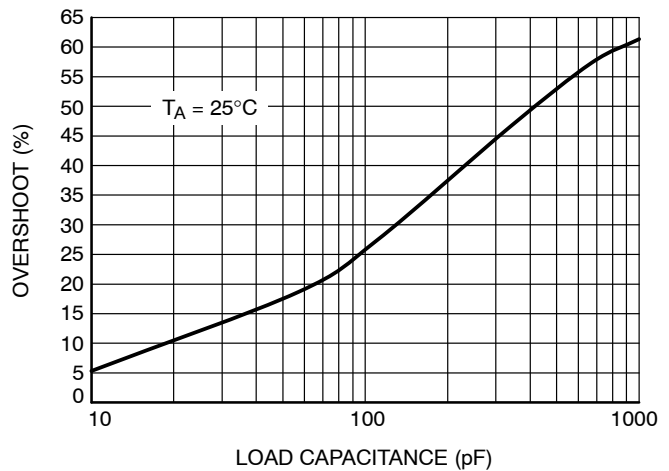


Figure 14. Small-Signal Overshoot vs. Load Capacitance

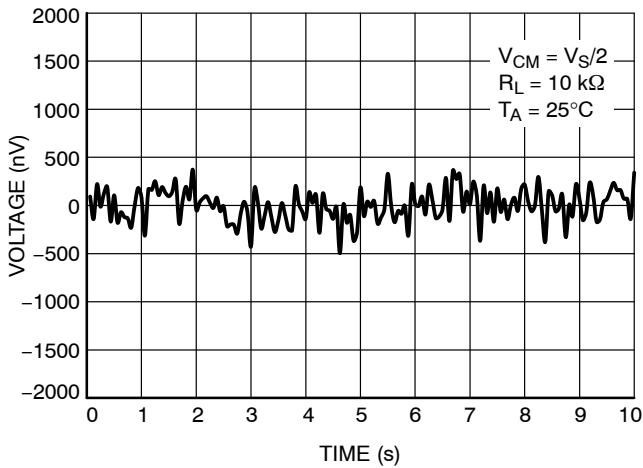


Figure 15. 0.1 Hz to 10 Hz Noise

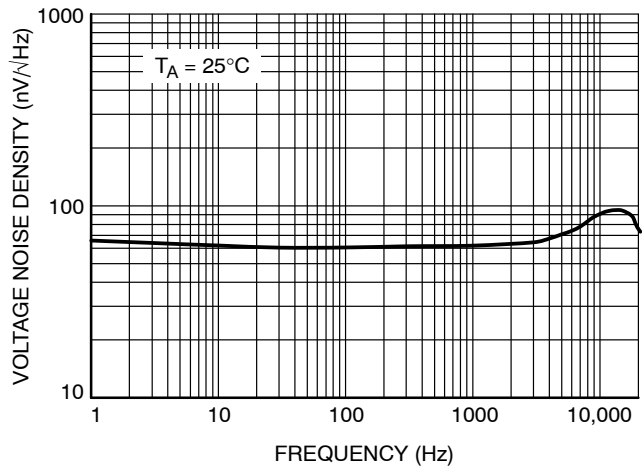


Figure 16. Voltage Noise Density vs. Frequency

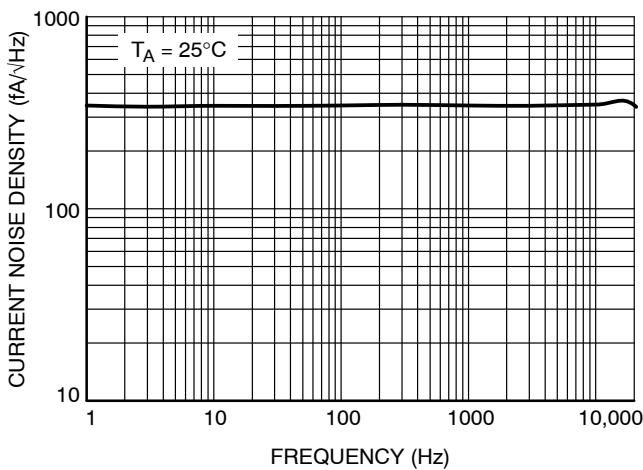


Figure 17. Current Noise Density vs. Frequency

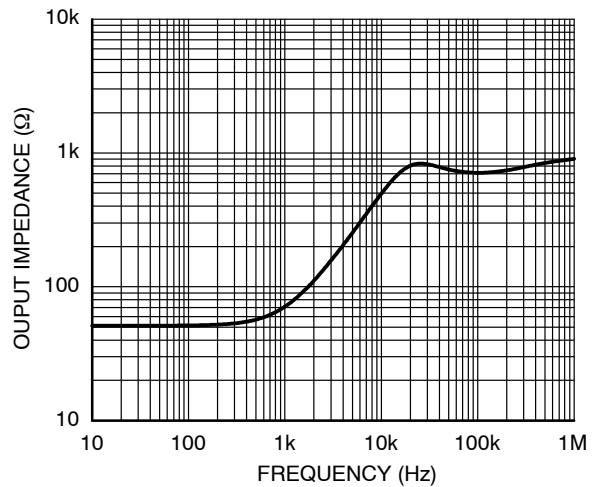


Figure 18. Open Loop Output Impedance vs. Frequency

APPLICATIONS INFORMATION

OVERVIEW

The NCS21871, NCS21872, and NCS21874 precision op amps provide low offset voltage and zero drift over temperature. The input common mode voltage range extends 100 mV beyond the supply rails to allow for sensing near ground or VDD. These features make the NCS21871 series well-suited for applications where precision is required, such as current sensing and interfacing with sensors.

The NCS21871 series of precision op amps uses a chopper-stabilized architecture, which provides the advantage of minimizing offset voltage drift over temperature and time. The simplified block diagram is shown in Figure 19. Unlike the classical chopper architecture, the chopper stabilized architecture has two signal paths.

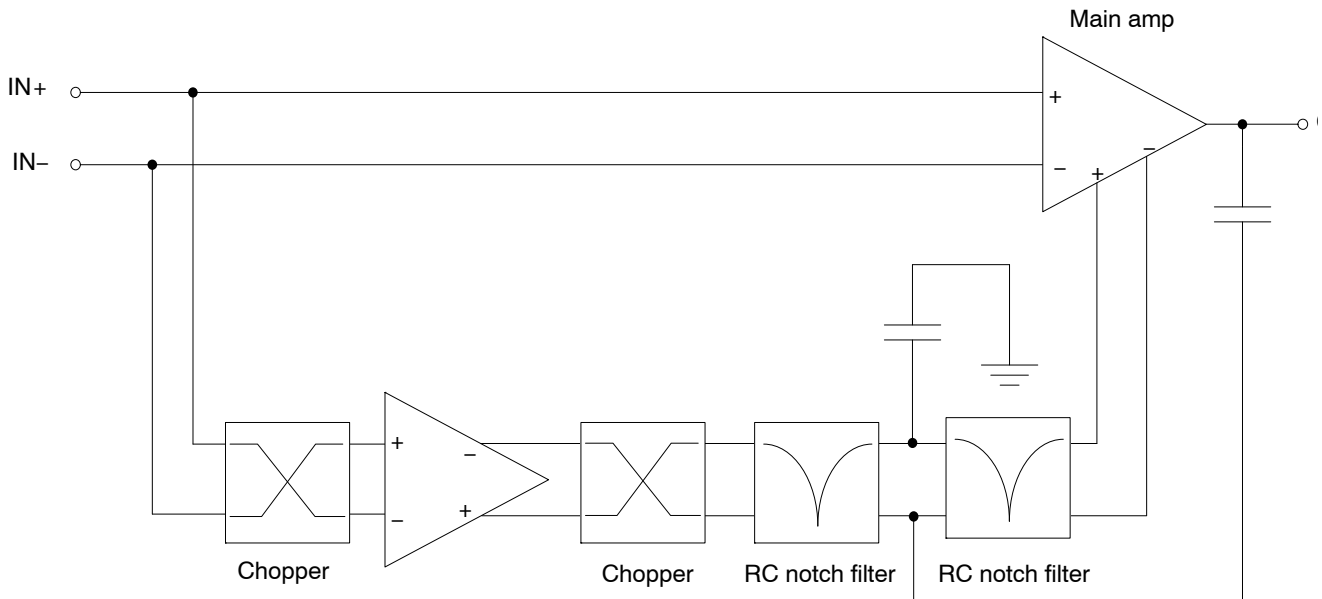


Figure 19. Simplified NCS21871 Block Diagram

In Figure 19, the lower signal path is where the chopper samples the input offset voltage, which is then used to correct the offset at the output. The offset correction occurs at a frequency of 125 kHz. The chopper-stabilized architecture is optimized for best performance at frequencies up to the related Nyquist frequency (1/2 of the offset correction frequency). As the signal frequency exceeds the Nyquist frequency, 62.5 kHz, aliasing may occur at the output. This is an inherent limitation of all chopper and chopper-stabilized architectures. Nevertheless, the NCS21871 op amps have minimal aliasing up to 125 kHz and low aliasing up to 190 kHz when compared to competitor parts from other manufacturers.

onsemi’s patented approach utilizes two cascaded, symmetrical, RC notch filters tuned to the chopper frequency and its fifth harmonic to reduce aliasing effects.

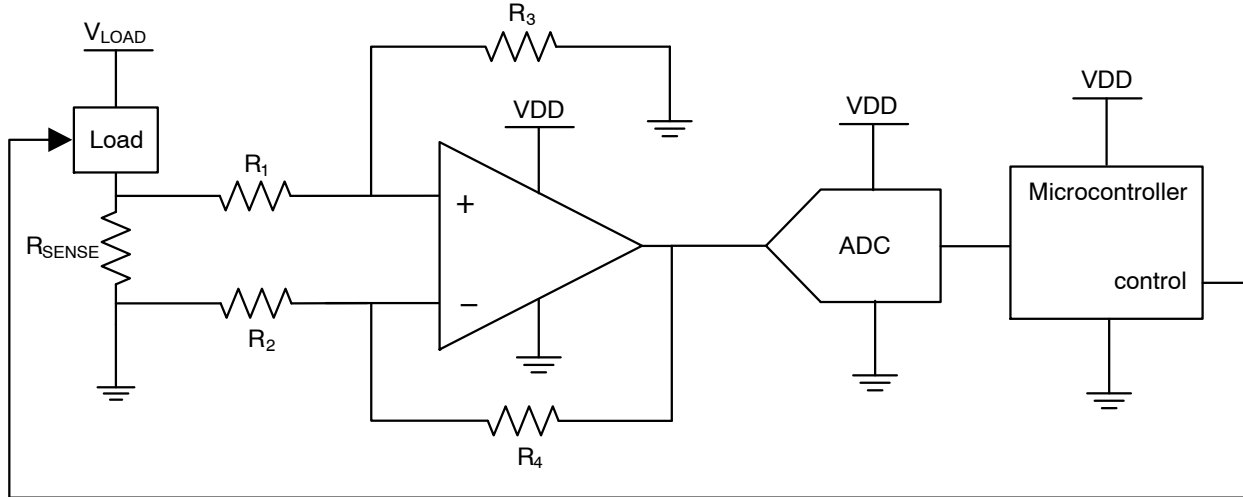
The chopper-stabilized architecture also benefits from the feed-forward path, which is shown as the upper signal path of the block diagram in Figure 19. This is the high speed signal path that extends the gain bandwidth up to 350 kHz. Not only does this help retain high frequency components of the input signal, but it also improves the loop gain at low frequencies. This is especially useful for low-side current sensing and sensor interface applications where the signal is low frequency and the differential voltage is relatively small.

**APPLICATION CIRCUITS**

**Low-Side Current Sensing**

Low-side current sensing is used to monitor the current through a load. This method can be used to detect over-current conditions and is often used in feedback control, as shown in Figure 20. A sense resistor is placed in series with the load to ground. Typically, the value of the

sense resistor is less than 100 mΩ to reduce power loss across the resistor. The op amp amplifies the voltage drop across the sense resistor with a gain set by external resistors R1, R2, R3, and R4 (where R1 = R2, R3 = R4). Precision resistors are required for high accuracy, and the gain is set to utilize the full scale of the ADC for the highest resolution.

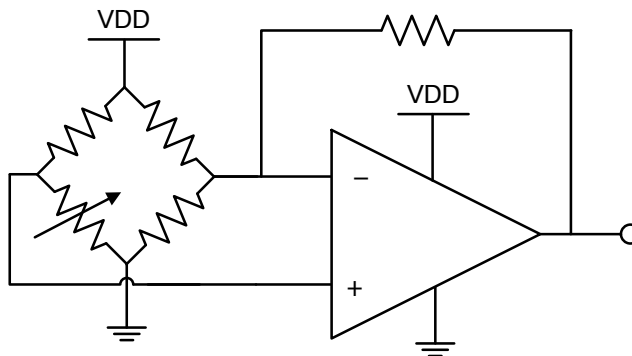


**Figure 20. Low-Side Current Sensing**

**Differential Amplifier for Bridged Circuits**

Sensors to measure strain, pressure, and temperature are often configured in a Wheatstone bridge circuit as shown in Figure 21. In the measurement, the voltage change that is

produced is relatively small and needs to be amplified before going into an ADC. Precision amplifiers are recommended in these types of applications due to their high gain, low noise, and low offset voltage.



**Figure 21. Bridge Circuit Amplification**

**EMI Susceptibility and Input Filtering**

Op amps have varying amounts of EMI susceptibility. Semiconductor junctions can pick up and rectify EMI signals, creating an EMI-induced voltage offset at the output, adding another component to the total error. Input pins are the most sensitive to EMI. The NCS21871 op amp family integrates low-pass filters to decrease sensitivity to EMI.

**General Layout Guidelines**

To ensure optimum device performance, it is important to follow good PCB design practices. Place 0.1 μF decoupling capacitors as close as possible to the supply pins. Keep traces short, utilize a ground plane, choose surface-mount components, and place components as close as possible to the device pins. These techniques will reduce susceptibility to electromagnetic interference (EMI). Thermoelectric effects can create an additional temperature dependent offset voltage at the input pins. To reduce these effects, use metals with low thermoelectric-coefficients and prevent temperature gradients from heat sources or cooling fans.

**UDFN8 Package Guidelines**

The UDFN8 package has an exposed leadframe die pad on the underside of the package. This pad should be soldered to the PCB, as shown in the recommended soldering footprint in the Package Dimensions section of this datasheet. The center pad can be electrically connected to VSS or it may be left floating. When connected to VSS, the center pad acts as a heat sink, improving the thermal resistance of the part.

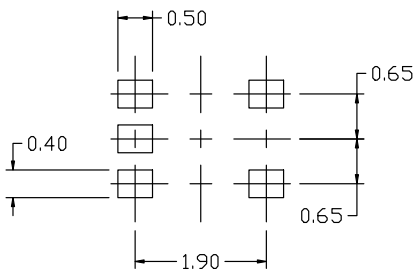
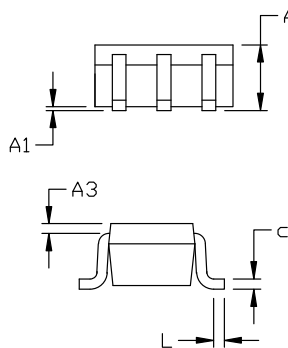
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

## SC-88A (SC-70-5/SOT-353) CASE 419A-02 ISSUE M

DATE 11 APR 2023



### RECOMMENDED MOUNTING FOOTPRINT

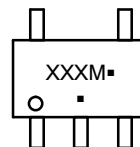
\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30

### GENERIC MARKING DIAGRAM\*



\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### STYLE 1:

- PIN 1. BASE
- EMITTER
- BASE
- COLLECTOR
- COLLECTOR

#### STYLE 2:

- PIN 1. ANODE
- EMITTER
- BASE
- COLLECTOR
- CATHODE

#### STYLE 3:

- PIN 1. ANODE 1
- N/C
- ANODE 2
- CATHODE 2
- CATHODE 1

#### STYLE 4:

- PIN 1. SOURCE 1
- DRAIN 1/2
- SOURCE 1
- GATE 1
- GATE 2

#### STYLE 5:

- PIN 1. CATHODE
- COMMON ANODE
- CATHODE 2
- CATHODE 3
- CATHODE 4

#### STYLE 6:

- PIN 1. EMITTER 2
- BASE 2
- EMITTER 1
- COLLECTOR
- COLLECTOR 2/BASE 1

#### STYLE 7:

- PIN 1. BASE
- EMITTER
- BASE
- COLLECTOR
- COLLECTOR

#### STYLE 8:

- PIN 1. CATHODE
- COLLECTOR
- N/C
- BASE
- EMITTER

#### STYLE 9:

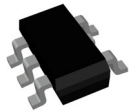
- PIN 1. ANODE
- CATHODE
- ANODE
- ANODE
- ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

<b>DOCUMENT NUMBER:</b>	<b>98ASB42984B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SC-88A (SC-70-5/SOT-353)</b>	<b>PAGE 1 OF 1</b>

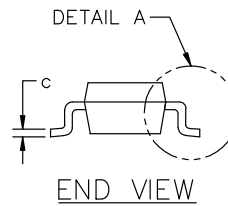
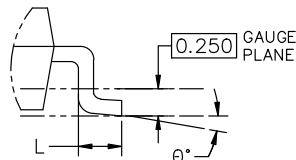
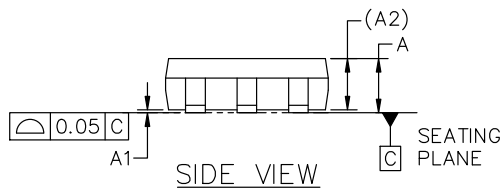
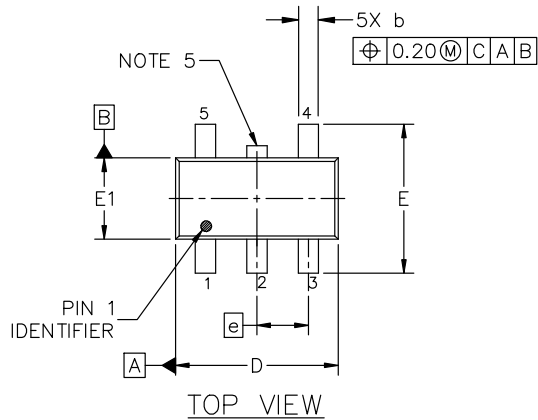
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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



## TSOP-5 3.00x1.50x0.95, 0.95P CASE 483 ISSUE P

DATE 01 APR 2024

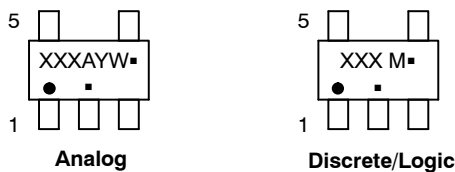


NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2	0.950 REF.		
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e	0.950 BSC		
L	0.200	0.400	0.600
θ	0°	5°	10°

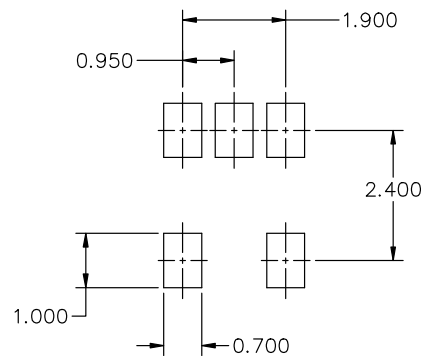
### GENERIC MARKING DIAGRAM\*



- XXX = Specific Device Code    XXX = Specific Device Code  
 A = Assembly Location        M = Date Code  
 Y = Year                            ▪ = Pb-Free Package  
 W = Work Week

▪ = Pb-Free Package  
(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



\* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

<b>DOCUMENT NUMBER:</b>	<b>98ARB18753C</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>TSOP-5 3.00x1.50x0.95, 0.95P</b>	<b>PAGE 1 OF 1</b>

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

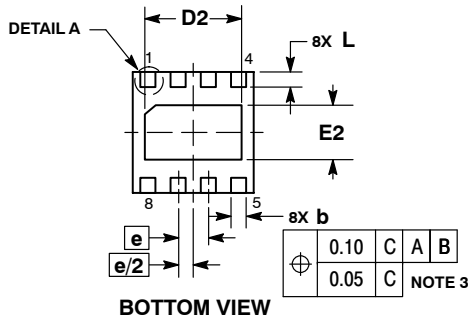
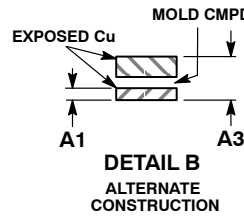
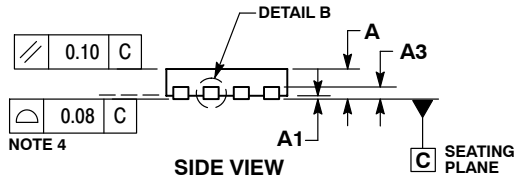
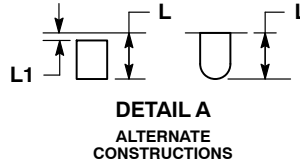
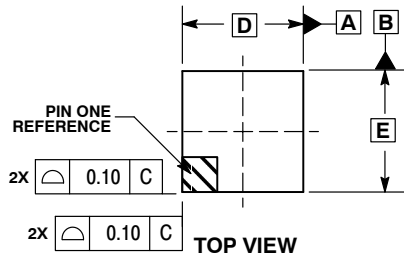
ON Semiconductor®



SCALE 2:1

UDFN8, 2x2  
CASE 517AW  
ISSUE A

DATE 13 NOV 2015

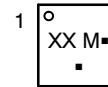


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICE OPN CONTAINING W OPTION, DETAIL B ALTERNATE CONSTRUCTION IS NOT APPLICABLE.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.18	0.30
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.80	1.00
e	0.50 BSC	
L	0.20	0.45
L1	---	0.15

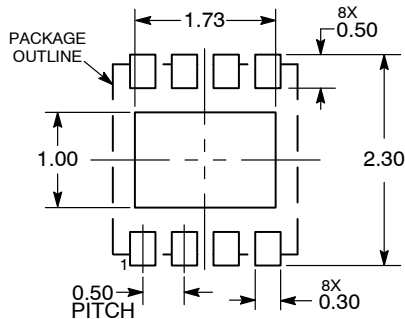
GENERIC MARKING DIAGRAM\*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)  
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	UDFN8, 2X2	PAGE 1 OF 1

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011

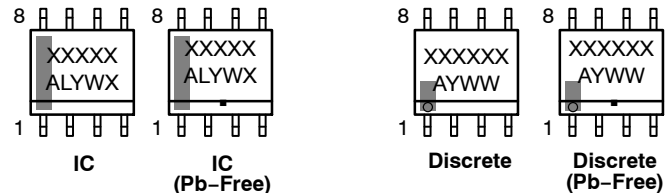
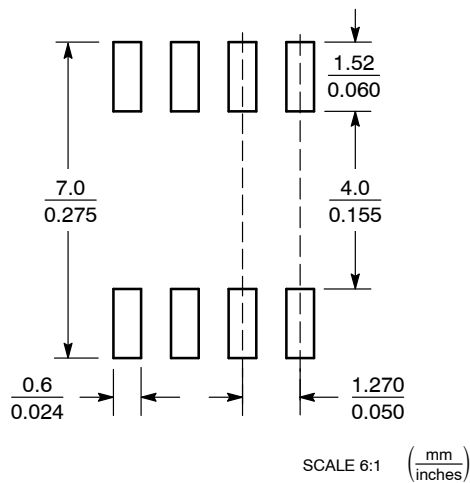


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

## GENERIC MARKING DIAGRAM\*

### SOLDERING FOOTPRINT\*



XXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |  |   |   |   |
|--|---|---|---|
| <p><b>STYLE 1:</b><br/> PIN 1. EMITTER<br/> 2. COLLECTOR<br/> 3. COLLECTOR<br/> 4. EMITTER<br/> 5. EMITTER<br/> 6. BASE<br/> 7. BASE<br/> 8. EMITTER</p>   | <p><b>STYLE 2:</b><br/> PIN 1. COLLECTOR, DIE, #1<br/> 2. COLLECTOR, #1<br/> 3. COLLECTOR, #2<br/> 4. COLLECTOR, #2<br/> 5. BASE, #2<br/> 6. EMITTER, #2<br/> 7. BASE, #1<br/> 8. EMITTER, #1</p>               | <p><b>STYLE 3:</b><br/> PIN 1. DRAIN, DIE #1<br/> 2. DRAIN, #1<br/> 3. DRAIN, #2<br/> 4. DRAIN, #2<br/> 5. GATE, #2<br/> 6. SOURCE, #2<br/> 7. GATE, #1<br/> 8. SOURCE, #1</p>                            | <p><b>STYLE 4:</b><br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. ANODE<br/> 4. ANODE<br/> 5. ANODE<br/> 6. ANODE<br/> 7. ANODE<br/> 8. COMMON CATHODE</p>   |
| <p><b>STYLE 5:</b><br/> PIN 1. DRAIN<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. DRAIN<br/> 5. GATE<br/> 6. GATE<br/> 7. SOURCE<br/> 8. SOURCE</p>   | <p><b>STYLE 6:</b><br/> PIN 1. SOURCE<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. SOURCE<br/> 5. SOURCE<br/> 6. GATE<br/> 7. GATE<br/> 8. SOURCE</p>  | <p><b>STYLE 7:</b><br/> PIN 1. INPUT<br/> 2. EXTERNAL BYPASS<br/> 3. THIRD STAGE SOURCE<br/> 4. GROUND<br/> 5. DRAIN<br/> 6. GATE 3<br/> 7. SECOND STAGE Vd<br/> 8. FIRST STAGE Vd</p>                    | <p><b>STYLE 8:</b><br/> PIN 1. COLLECTOR, DIE #1<br/> 2. BASE, #1<br/> 3. BASE, #2<br/> 4. COLLECTOR, #2<br/> 5. COLLECTOR, #2<br/> 6. EMITTER, #2<br/> 7. EMITTER, #1<br/> 8. COLLECTOR, #1</p>                              |
| <p><b>STYLE 9:</b><br/> PIN 1. EMITTER, COMMON<br/> 2. COLLECTOR, DIE #1<br/> 3. COLLECTOR, DIE #2<br/> 4. EMITTER, COMMON<br/> 5. EMITTER, COMMON<br/> 6. BASE, DIE #2<br/> 7. BASE, DIE #1<br/> 8. EMITTER, COMMON</p> | <p><b>STYLE 10:</b><br/> PIN 1. GROUND<br/> 2. BIAS 1<br/> 3. OUTPUT<br/> 4. GROUND<br/> 5. GROUND<br/> 6. BIAS 2<br/> 7. INPUT<br/> 8. GROUND</p>  | <p><b>STYLE 11:</b><br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. DRAIN 2<br/> 7. DRAIN 1<br/> 8. DRAIN 1</p>   | <p><b>STYLE 12:</b><br/> PIN 1. SOURCE<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p><b>STYLE 13:</b><br/> PIN 1. N.C.<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>  | <p><b>STYLE 14:</b><br/> PIN 1. N-SOURCE<br/> 2. N-GATE<br/> 3. P-SOURCE<br/> 4. P-GATE<br/> 5. P-DRAIN<br/> 6. P-DRAIN<br/> 7. N-DRAIN<br/> 8. N-DRAIN</p>   | <p><b>STYLE 15:</b><br/> PIN 1. ANODE 1<br/> 2. ANODE 1<br/> 3. ANODE 1<br/> 4. ANODE 1<br/> 5. CATHODE, COMMON<br/> 6. CATHODE, COMMON<br/> 7. CATHODE, COMMON<br/> 8. CATHODE, COMMON</p>               | <p><b>STYLE 16:</b><br/> PIN 1. EMITTER, DIE #1<br/> 2. BASE, DIE #1<br/> 3. EMITTER, DIE #2<br/> 4. BASE, DIE #2<br/> 5. COLLECTOR, DIE #2<br/> 6. COLLECTOR, DIE #2<br/> 7. COLLECTOR, DIE #1<br/> 8. COLLECTOR, DIE #1</p> |
| <p><b>STYLE 17:</b><br/> PIN 1. VCC<br/> 2. V2OUT<br/> 3. V1OUT<br/> 4. TXE<br/> 5. RXE<br/> 6. VEE<br/> 7. GND<br/> 8. ACC</p>  | <p><b>STYLE 18:</b><br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. CATHODE<br/> 8. CATHODE</p>   | <p><b>STYLE 19:</b><br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. MIRROR 2<br/> 7. DRAIN 1<br/> 8. MIRROR 1</p>   | <p><b>STYLE 20:</b><br/> PIN 1. SOURCE (N)<br/> 2. GATE (N)<br/> 3. SOURCE (P)<br/> 4. GATE (P)<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p><b>STYLE 21:</b><br/> PIN 1. CATHODE 1<br/> 2. CATHODE 2<br/> 3. CATHODE 3<br/> 4. CATHODE 4<br/> 5. CATHODE 5<br/> 6. COMMON ANODE<br/> 7. COMMON ANODE<br/> 8. CATHODE 6</p>  | <p><b>STYLE 22:</b><br/> PIN 1. I/O LINE 1<br/> 2. COMMON CATHODE/VCC<br/> 3. COMMON CATHODE/VCC<br/> 4. I/O LINE 3<br/> 5. COMMON ANODE/GND<br/> 6. I/O LINE 4<br/> 7. I/O LINE 5<br/> 8. COMMON ANODE/GND</p> | <p><b>STYLE 23:</b><br/> PIN 1. LINE 1 IN<br/> 2. COMMON ANODE/GND<br/> 3. COMMON ANODE/GND<br/> 4. LINE 2 IN<br/> 5. LINE 2 OUT<br/> 6. COMMON ANODE/GND<br/> 7. COMMON ANODE/GND<br/> 8. LINE 1 OUT</p> | <p><b>STYLE 24:</b><br/> PIN 1. BASE<br/> 2. EMITTER<br/> 3. COLLECTOR/ANODE<br/> 4. COLLECTOR/ANODE<br/> 5. CATHODE<br/> 6. CATHODE<br/> 7. COLLECTOR/ANODE<br/> 8. COLLECTOR/ANODE</p>                                      |
| <p><b>STYLE 25:</b><br/> PIN 1. VIN<br/> 2. N/C<br/> 3. REXT<br/> 4. GND<br/> 5. IOUT<br/> 6. IOUT<br/> 7. IOUT<br/> 8. IOUT</p>   | <p><b>STYLE 26:</b><br/> PIN 1. GND<br/> 2. dv/dt<br/> 3. ENABLE<br/> 4. ILIMIT<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. VCC</p>  | <p><b>STYLE 27:</b><br/> PIN 1. ILIMIT<br/> 2. OVLO<br/> 3. UVLO<br/> 4. INPUT+<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. DRAIN</p>  | <p><b>STYLE 28:</b><br/> PIN 1. SW_TO_GND<br/> 2. DASIC_OFF<br/> 3. DASIC_SW_DET<br/> 4. GND<br/> 5. V_MON<br/> 6. VBULK<br/> 7. VBULK<br/> 8. VIN</p>  |
| <p><b>STYLE 29:</b><br/> PIN 1. BASE, DIE #1<br/> 2. EMITTER, #1<br/> 3. BASE, #2<br/> 4. EMITTER, #2<br/> 5. COLLECTOR, #2<br/> 6. COLLECTOR, #2<br/> 7. COLLECTOR, #1<br/> 8. COLLECTOR, #1</p>                        | <p><b>STYLE 30:</b><br/> PIN 1. DRAIN 1<br/> 2. DRAIN 1<br/> 3. GATE 2<br/> 4. SOURCE 2<br/> 5. SOURCE 1/DRAIN 2<br/> 6. SOURCE 1/DRAIN 2<br/> 7. SOURCE 1/DRAIN 2<br/> 8. GATE 1</p>                           |   |   |

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<b>DESCRIPTION:</b>	<b>SOIC-8 NB</b>	<b>PAGE 2 OF 2</b>

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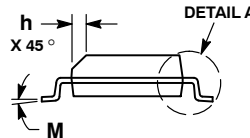
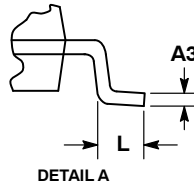
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	SOIC-14 NB	PAGE 1 OF 2

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**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

DATE 03 FEB 2016

STYLE 1:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 2:  
 CANCELLED

STYLE 3:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON CATHODE

STYLE 4:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 5:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 6:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

STYLE 7:  
 PIN 1. ANODE/CATHODE  
 2. COMMON ANODE  
 3. COMMON CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. COMMON CATHODE  
 12. COMMON ANODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

STYLE 8:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

### Micro8 CASE 846A-02 ISSUE K

DATE 16 JUL 2020



TOP VIEW

NOTE 3



SIDE VIEW



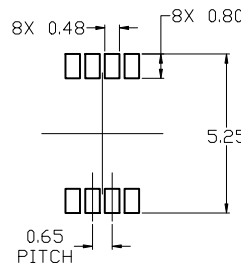
END VIEW

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

$\phi 0.08$  (0.003) M C B S A S

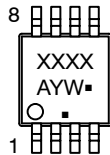
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
<i>b</i>	0.25	0.33	0.40
<i>c</i>	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
<i>e</i>	0.65 BSC		
H <sub>E</sub>	4.75	4.90	5.05
L	0.40	0.55	0.70



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

### GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**STYLE 1:**

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

**STYLE 2:**

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

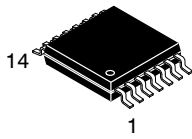
**STYLE 3:**

1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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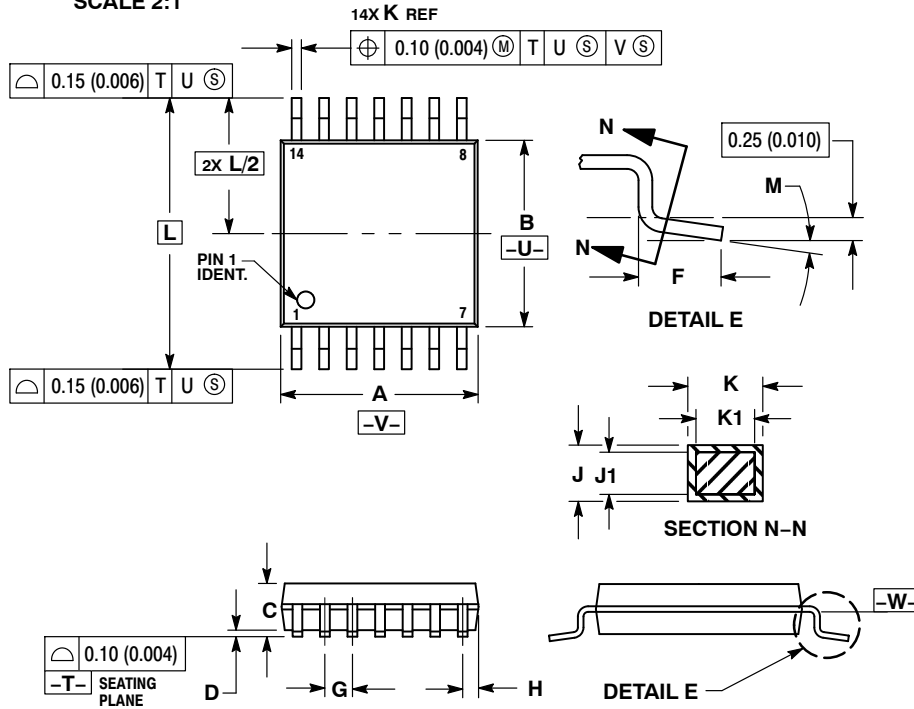
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**TSSOP-14 WB**  
CASE 948G  
ISSUE C

DATE 17 FEB 2016

SCALE 2:1

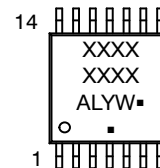


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**GENERIC MARKING DIAGRAM\***

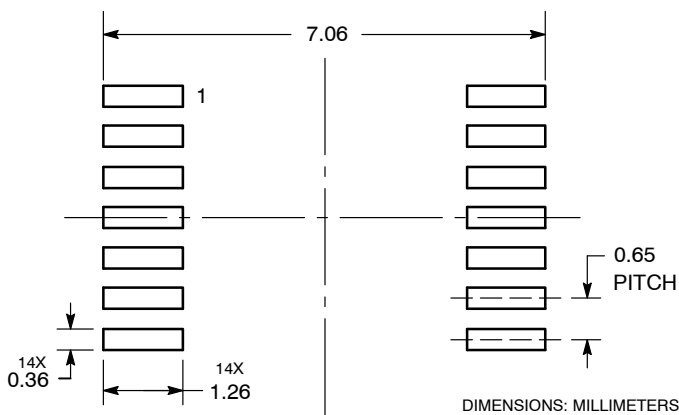


- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**SOLDERING FOOTPRINT**



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