WINSOURCE ELECTRONICS

THE DATASHEET OF

DS1996L-F5

DS1996
64Kb Memory iButton

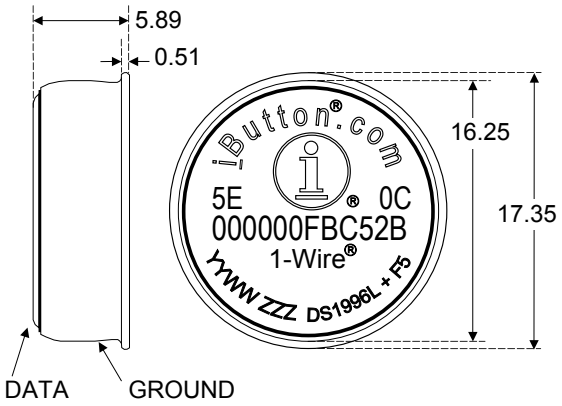
SPECIAL FEATURES

- 65,536 bits of read/write nonvolatile memory
- Overdrive mode boosts communication speed to 142 kbits per second
- 256-bit scratchpad ensures integrity of data transfer
- Memory partitioned into 256-bit pages for packetizing data
- Data integrity assured with strict read/write protocols
- Operating temperature range from -40°C to +70°C
- Over 10 years of data retention

COMMON iButton FEATURES

- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number 8-bit CRC tester) assures absolute traceability because no two parts are alike
- Multidrop controller for MicroLAN
- Digital identification and information by momentary contact
- Chip-based data carrier compactly stores information
- Data can be accessed while affixed to object
- Economically communicates to bus master with a single digital signal at 16.3 kbits per second
- Standard 16 mm diameter and 1-Wire® protocol ensure compatibility with iButton® family
- Button shape is self-aligning with cup-shaped probes

F5 MICROCAN



All dimensions are shown in millimeters

- Durable stainless steel case engraved with registration number withstands harsh environments
- Easily affixed with self-stick adhesive backing, latched by its flange, or locked with a ring pressed onto its rim
- Presence detector acknowledges when reader first applies voltage

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS1996L-F5+	-40°C to +70°C	F5 MicroCan

+Denotes a lead(Pb)-free/RoHS-compliant package.

EXAMPLES OF ACCESSORIES

DS9096P	Self-Stick Adhesive Pad
DS9101	Multi-Purpose Clip
DS9093RA	Mounting Lock Ring
DS9093F	Snap-In Fob
DS9092	iButton Probe

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-4896; Rev 8/09

iButton DESCRIPTION

The DS1996 Memory iButton is a rugged read/write data carrier that acts as a localized database that can be easily accessed with minimal hardware. The nonvolatile memory offers a simple solution to storing and retrieving vital information pertaining to the object to which the iButton is attached. Data is transferred serially via the 1-Wire protocol which requires only a single data lead and a ground return. The scratchpad is an additional page that acts as a buffer when writing to memory. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to memory. This process ensures data integrity when modifying the memory. A 48-bit serial number is factory lasered into each DS1996 to provide a guaranteed unique identity which allows for absolute traceability. The durable MicroCan package is highly resistant to environmental hazards such as dirt, moisture, and shock. Its compact button-shaped profile is self-aligning with mating receptacles, allowing the DS1996 to be easily used by human operators. Accessories permit the DS1996 to be mounted on almost any surface including plastic key fobs, photo-ID badges and printed circuit boards. Applications include access control, work-in-progress tracking, electronic travelers, storage of calibration constants, and debit tokens.

OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS1996. The DS1996 has three main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad and 3) 65536-bit SRAM. The hierarchal structure of the 1-Wire protocol is shown in Figure 2. The bus master must first provide one of the six ROM Function Commands, 1)Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, 5) Overdrive-Skip ROM or Overdrive-Match ROM. Upon completion of an overdrive ROM command byte executed at regular speed, the device will enter Overdrive mode where all subsequent communication occurs at a higher speed. The protocol required for these ROM Function Commands is described in Figure 9. After a ROM Function Command is successfully executed, the memory functions become accessible and the master may provide any one of the four memory function commands. The protocol for these memory function commands is described in Figure 7. All data read and written least significant bit first.

PARASITE POWER

The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry ”steals” power whenever the data line is high. The data line will provide sufficient power as long as the specified timing and voltage requirements are met. The advantages of parasite power are two-fold: 1) by parasiting off this input, battery power is not consumed for 1-Wire ROM function commands, and 2) if the battery is exhausted for any reason, the ROM may still be read normally. The remaining circuitry of the DS1996 is solely operated by battery energy.

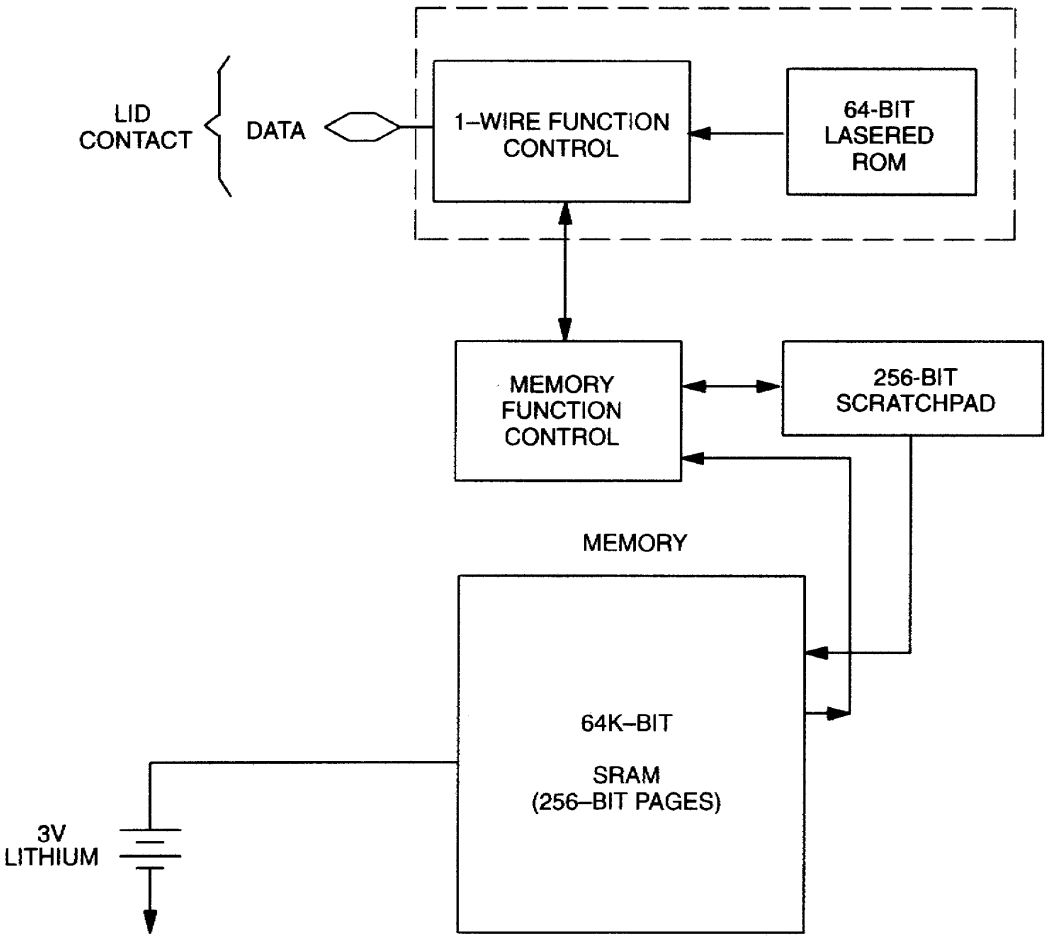
64-BIT LASERED ROM

Each DS1996 contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits. (Figure 3.)

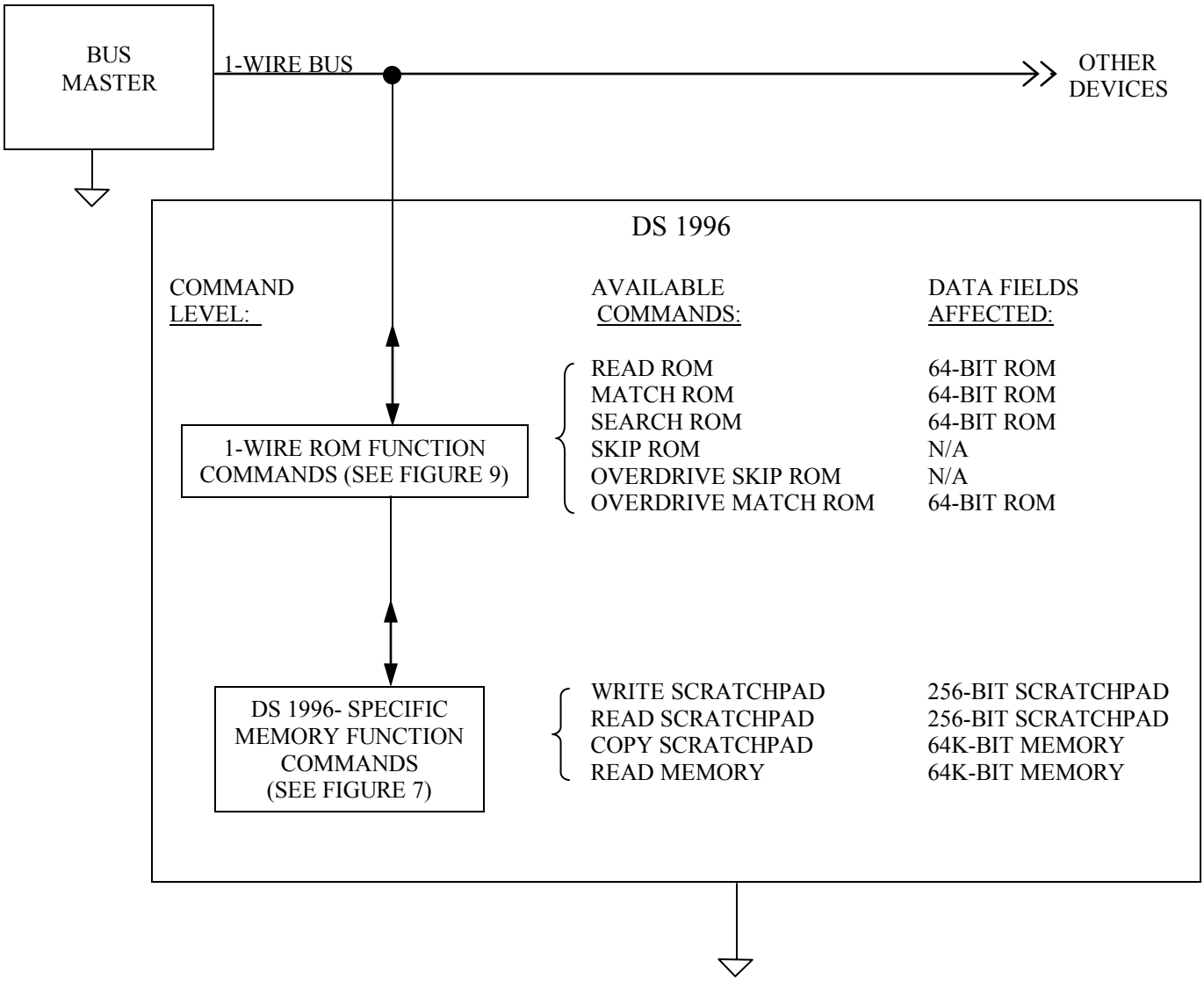
The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in the Book of DS19xx iButton Standards.

The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, 1 bit at a time is shifted in. After the 8^{th} bit of the family code has been entered, then the serial number is entered. After the 48^{th} bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of CRC should return the shift register to all zeros.

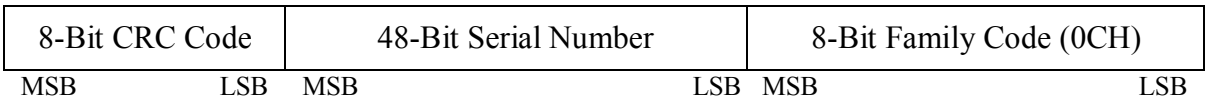
DS1996 BLOCK DIAGRAM Figure 1



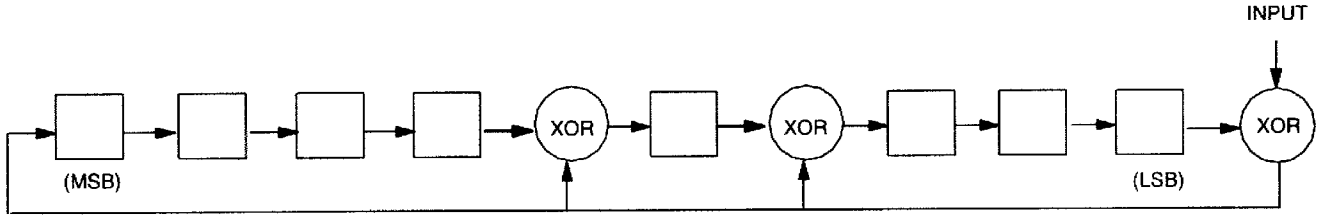
HIERARCHICAL STRUCTURE FOR 1-WIRE PROTOCOL Figure 2



64-BIT LASERED ROM Figure 3



1-WIRE CRC GENERATOR Figure 4



MEMORY

The memory map in Figure 5 shows a 32-byte page called the scratchpad and additional 32-byte pages called memory. The DS1996 contains 256 pages which comprise the 65536-bit SRAM. The scratchpad is an additional page that acts as a buffer when writing to memory.

ADDRESS REGISTERS AND TRANSFER STATUS

Because of the serial data transfer, the DS1996 employs three address registers, called TA1, TA2 and E/S (Figure 6). Registers TA1 and TA2 must be loaded with the target address to which the data will be written or from which data will be sent to the master upon a Read command. Register E/S acts like a byte counter and Transfer Status register. It is used to verify data integrity with Write commands. Therefore, the master only has read access to this register. The lower 5 bits of the E/S register indicate the address of the last byte that has been written to the scratchpad. This address is called Ending Offset. Bit 5 of the E/S register, called PF or ”partial byte flag,” is set if the number of data bits sent by the master is not an integer multiple of 8. Bit 6, OF or ”Overflow,” is set if more bits are sent by the master than can be stored in the scratchpad. Note that the lowest 5 bits of the target address also determine the address within the scratchpad, where intermediate storage of data will begin. This address is called byte offset. If the target address for a Write command is 13CH for example, then the scratchpad will store incoming data beginning at the byte offset 1CH and will be full after only 4 bytes. The corresponding ending offset in this example is 1FH. For best economy of speed and efficiency, the target address for writing should point to the beginning of a new page, i.e., the byte offset will be 0. Thus the full 32-byte capacity of the scratchpad is available, resulting also in the ending offset of 1FH. However, it is possible to write one or several contiguous bytes somewhere within a page. The ending offset together with the Partial and Overflow Flag is mainly a means to support the master checking the data integrity after a Write command. The highest valued bit of the E/S register, called AA or Authorization Accepted, acts as a flag to indicate that the data stored in the scratchpad has already been copied to the target memory address. Writing data to the scratchpad clears this flag.

WRITING WITH VERIFICATION

To write data to the DS1996, the scratchpad has to be used as intermediate storage. First the master issues the Write Scratchpad command to specify the desired target address, followed by the data to be written to the scratchpad. In the next step, the master sends the Read Scratchpad command to read the scratchpad and to verify data integrity. As preamble to the scratchpad data, the DS1996 sends the requested target address TA1 and TA2 and the contents of the E/S register. If one of the flags OF or PF is set, data did not arrive correctly in the scratchpad. The master does not need to continue reading; it can start a new trial to write data to the scratchpad. Similarly, a set AA flag indicates that the Write command was not recognized by the iButton. If everything went correctly, all three flags are cleared and the ending offset indicates the address of the last byte written to the scratchpad. Now the master can continue verifying every data bit. After the master has verified the data, it has to send the Copy Scratchpad command. This command must be followed exactly by the data of the three address registers TA1, TA2 and E/S as the master has read them verifying the scratchpad. As soon as the iButton has received these bytes, it will copy the data to the requested location beginning at the target address.

MEMORY FUNCTION COMMANDS

The “Memory Function Flow Chart” (Figure 7) describes the protocols necessary for accessing the memory. An example follows the flowchart. The communication between master and DS1996 takes place either at regular speed (default, OD=0) or at Overdrive Speed (OD=1). If not explicitly set into the Overdrive Mode the DS1996 assumes regular speed.

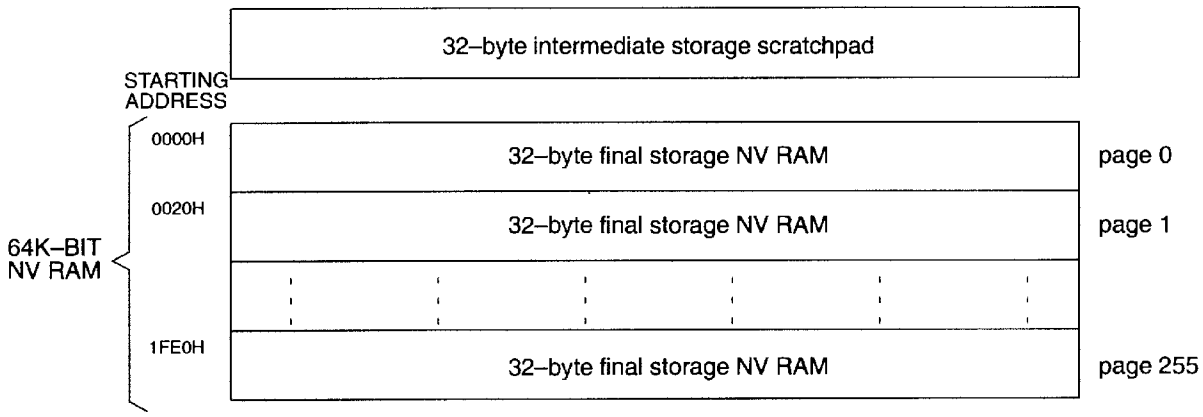
Write Scratchpad Command [0FH]

After issuing the write scratchpad command, the master must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data will be written to the scratchpad starting at the byte offset (T4:T0). The ending offset (E4: E0) will be the byte offset at which the bus master has stopped writing data.

Read Scratchpad Command [AAH]

This command is used to verify scratchpad data and target address. After issuing the read scratchpad command, the master begins reading. The first 2 bytes will be the target address. The next byte will be the ending offset/data status byte (E/S) followed by the scratchpad data beginning at the byte offset (T4: T0). The master may read data until the end of the scratchpad after which the data read will be all logic 1's.

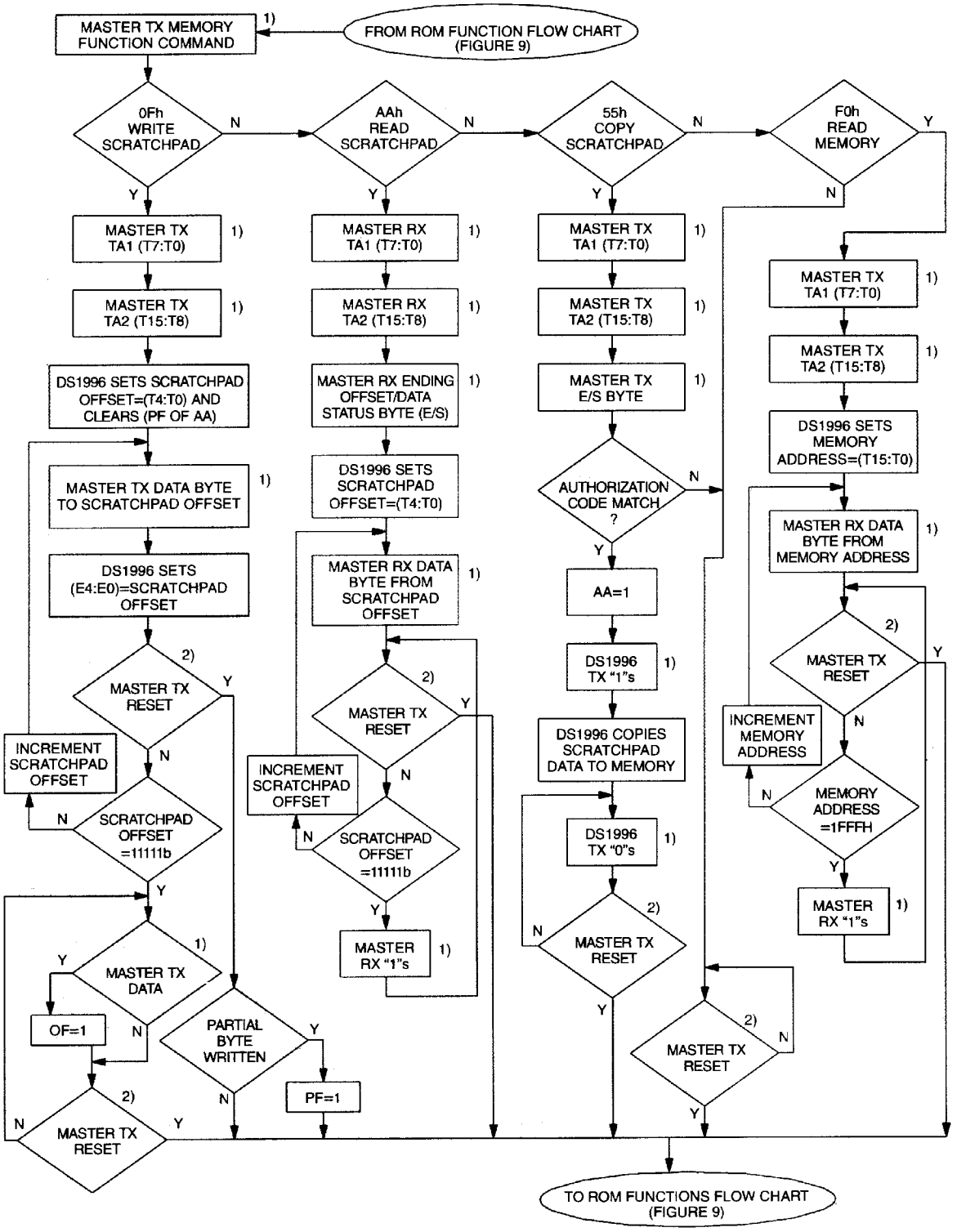
DS1996 MEMORY MAP Figure 5



ADDRESS REGISTERS Figure 6

	7	6	5	4	3	2	1	0
TARGET ADDRESS (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
ENDING ADDRESS WITH DATA STATUS (E/S) (READ ONLY)	AA	OF	PF	E4	E3	E2	E1	E0

MEMORY FUNCTION FLOW CHART Figure 7



1) TO BE TRANSMITTED OR RECEIVED AT OVERDRIVE SPEED IF OD=1
2) RESET PULSE TO BE TRANSMITTED AT OVERDRIVE SPEED IF OD=1;
RESET PULSE TO BE TRANSMITTED AT REGULAR SPEED IF OD=0
OR IF THE DS1996 IS TO BE RESET FROM OVERDRIVE SPEED TO REGULAR SPEED

MEMORY FUNCTION EXAMPLES

Example: Write two data bytes to memory locations 0026h and 0027h (the seventh and 8th bytes of page 1). Read entire memory.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480-960 µs)
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	0Fh	Issue “write scratchpad” command
TX	26h	TA1, beginning offset=6
TX	00h	TA2, address=0026h
TX	<2 data bytes>	Write 2 bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	AAh	Issue “read scratchpad” command
RX	26h	Read TA1, beginning offset=6
RX	00h	Read TA2, address=0026h
RX	07h	Read E/S, ending offset=7, flags=0
RX	<2 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	55h	Issue “copy scratchpad” command
TX	26h	TA1 } AUTHORIZATION CODE
TX	00h	TA2 } AUTHORIZATION CODE
TX	07h	E/S } AUTHORIZATION CODE
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	F0h	Issue “read memory” command
TX	00h	TA1, beginning offset=0
TX	00h	TA2, address=0000h
RX	<8192 bytes>	Read entire memory
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

Copy Scratchpad [55H]

This command is used to copy data from the scratchpad to memory. After issuing the copy scratchpad command, the master must provide a 3-byte authorization pattern which is obtained by reading the scratchpad for verification. This pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the AA (Authorization Accepted) flag will be set and the copy will begin. A logic 0 will be transmitted after the data has been copied until a reset pulse is issued by the master. Any attempt to reset the part will be ignored while the copy is in progress. Copy typically takes 30 µs.

The data to be copied is determined by the three address registers. The scratchpad data from the beginning offset through the ending offset, will be copied to memory, starting at the target address. Anywhere from 1 to 32 bytes may be copied to memory with this command. Whole bytes are copied even if only partially written. The AA flag will be cleared only by executing a write scratchpad command.

Read Memory [F0H]

The read memory command may be used to read the entire memory. After issuing the command, the master must provide the 2-byte target address. After the 2 bytes, the master reads data beginning from the target address and may continue until the end of memory, at which point logic 1's will be read. It is important to realize that the target address registers will contain the address provided. The ending offset/data status byte is unaffected.

The hardware of the DS1996 provides a means to accomplish error-free writing to the memory section. To safeguard reading data in the 1-Wire environment and to simultaneously speed up data transfers, it is recommended to packetize data into data packets of the size of one memory page each. Such a packet would typically store a 16-bit CRC with each page of data to ensure rapid, error-free data transfers that eliminate having to read a page multiple times to determine if the received data is correct or not. (See the Book of DS19xx iButton Standards, Chapter 7 for the recommended file structure to be used with the 1-Wire environment.)

1-WIRE BUS SYSTEM

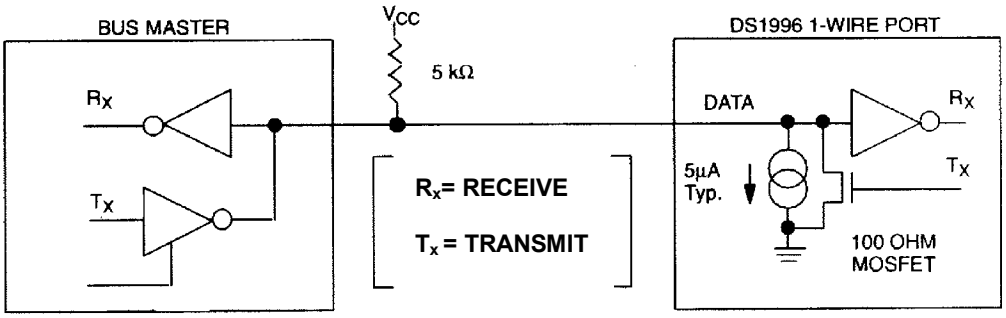
The 1-Wire bus is a system which has a single bus master and one or more slaves. In all instances the DS1996 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). A 1-Wire protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master. For a more detailed protocol description, refer to Chapter 4 of the Book of DS19xx iButton Standards.

HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open drain connection or 3-state outputs. The 1-Wire port of the DS1996 is open drain with an internal circuit equivalent to that shown in Figure 8. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. At regular speed the 1-Wire bus has a maximum data rate of 16.3 kbits per second. The speed can be boosted to 142 kbits per second by activating the Overdrive Mode. The 1-Wire bus requires a pullup resistor of approximately 5 kΩ.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16 µs (Overdrive Speed) or more than 120 µs (regular speed), one or more of the devices on the bus may be reset.

HARDWARE CONFIGURATION Figure 8



TRANSACTION SEQUENCE

The protocol for accessing the DS1996 via the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS1996 is on the bus and is ready to operate. For more details, see the ”1-Wire Signaling” section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the six ROM function commands. All ROM function commands are 8 bits long. A list of these commands follows (refer to flowchart in Figure 9).

Read ROM [33H]

This command allows the bus master to read the DS1996’s 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS1996 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The resultant family code and 48-bit serial number will usually result in a mismatch of the CRC.

Match ROM [55H]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS1996 on a multidrop bus. Only the DS1996 that exactly matches the 64-bit ROM sequence will respond to the subsequent memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCH]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns will produce a wired–AND result).

Search ROM [F0H]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The search ROM process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the Book of DS19xx iButton Standards for a comprehensive discussion of a search ROM, including an actual example.

Overdrive Skip ROM [3CH]

On a single-drop bus this command can save time by allowing the bus master to access the memory functions without providing the 64-bit ROM code. Unlike the normal Skip ROM command the Overdrive Skip ROM sets the DS1996 in the Overdrive Mode (OD=1). All communication following this command has to occur at Overdrive Speed until a reset pulse of minimum 480 µs duration resets all devices on the bus to regular speed (OD=0).

When issued on a multidrop bus this command will set all Overdrive-capable devices into Overdrive mode. To subsequently address a specific Overdrive-capable device, a reset pulse at Overdrive speed has to be issued followed by a Match ROM or Search ROM command sequence. This will shorten the time for the search process. If more than one slave supporting Overdrive is present on the bus and the Overdrive Skip ROM command is followed by a read command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns will produce a wired-AND result).

Overdrive Match ROM [69H]

The Overdrive Match ROM command, followed by a 64-bit ROM sequence transmitted at Overdrive Speed, allows the bus master to address a specific DS1996 on a multidrop bus and to simultaneously set it in Overdrive Mode. Only the DS1996 that exactly matches the 64-bit ROM sequence will respond to the subsequent memory function command. Slaves already in Overdrive mode from a previous Overdrive Skip or Match command will remain in Overdrive mode. All other slaves that do not match the 64-bit ROM sequence or do not support Overdrive will return to or remain at regular speed and wait for a reset pulse of minimum 480 µs duration. The Overdrive Match ROM command can be used with a single or multiple devices on the bus.

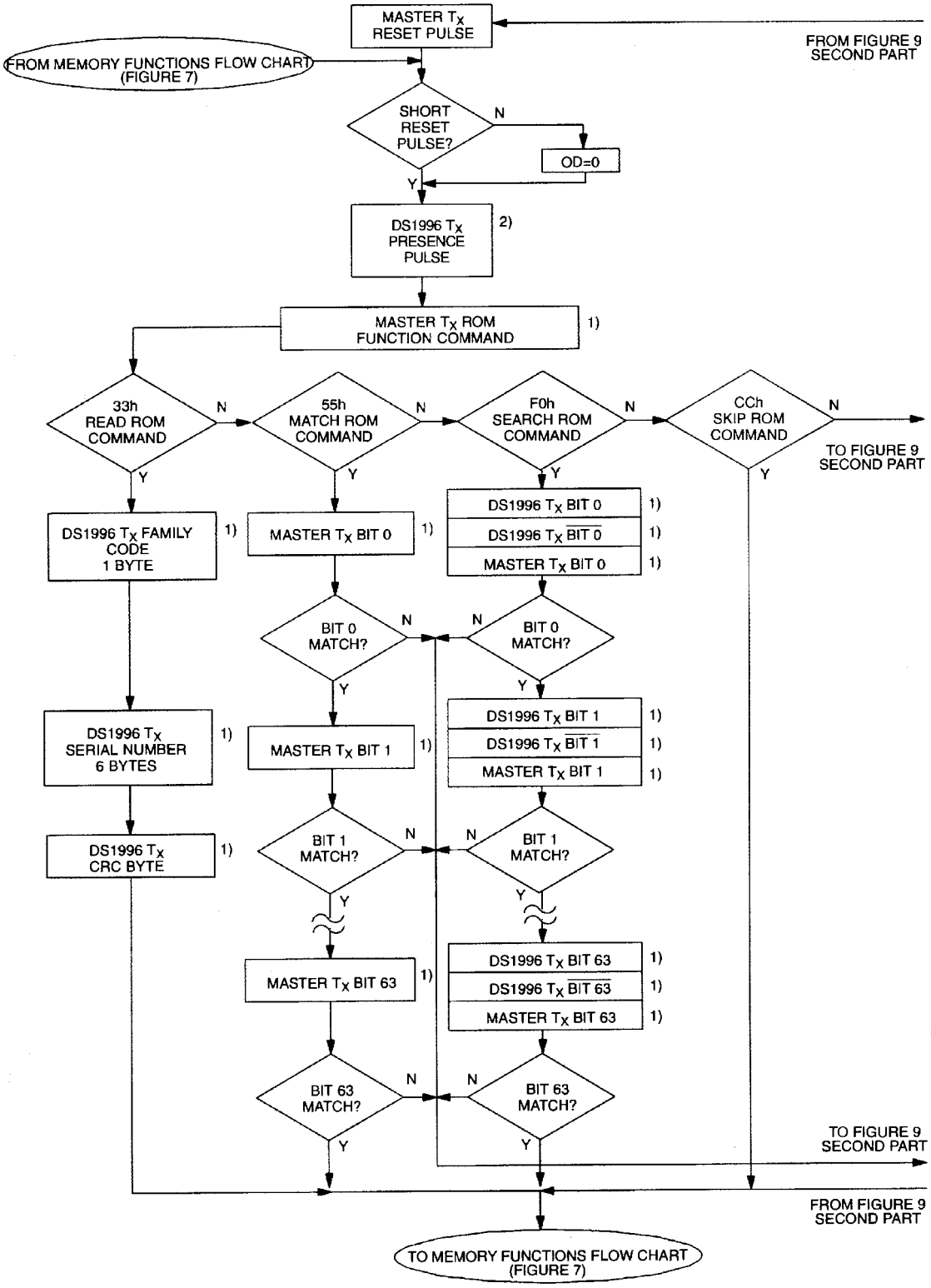
1-WIRE SIGNALING

The DS1996 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1 and Read Data. All these signals except presence pulse are initiated by the bus master. The DS1996 can communicate at two different speeds, regular speed and Overdrive speed. If not explicitly set into the overdrive mode, the DS1996 will communicate at regular speed. While in Overdrive Mode the fast timing applies to all wave forms.

The initialization sequence required to begin any communication with the DS1996 is shown in Figure 10. A reset pulse followed by a presence pulse indicates the DS1996 is ready to send or receive data given the correct ROM command and memory function command. The bus master transmits (TX) a reset pulse (t_{RSTL}, minimum 480 µs at regular speed, 48 µs at Overdrive speed). The bus master then releases the line and goes into receive mode (RX). The 1-Wire bus is pulled to a high state via the pullup resistor. After detecting the rising edge on the data contact, the DS1996 waits (t_{PDH}, 15-60 µs at regular speed, 2-6 µs at Overdrive speed) and then transmits the presence pulse (t_{PDL}, 60-240 µs at regular speed, 8-24 µs at Overdrive speed).

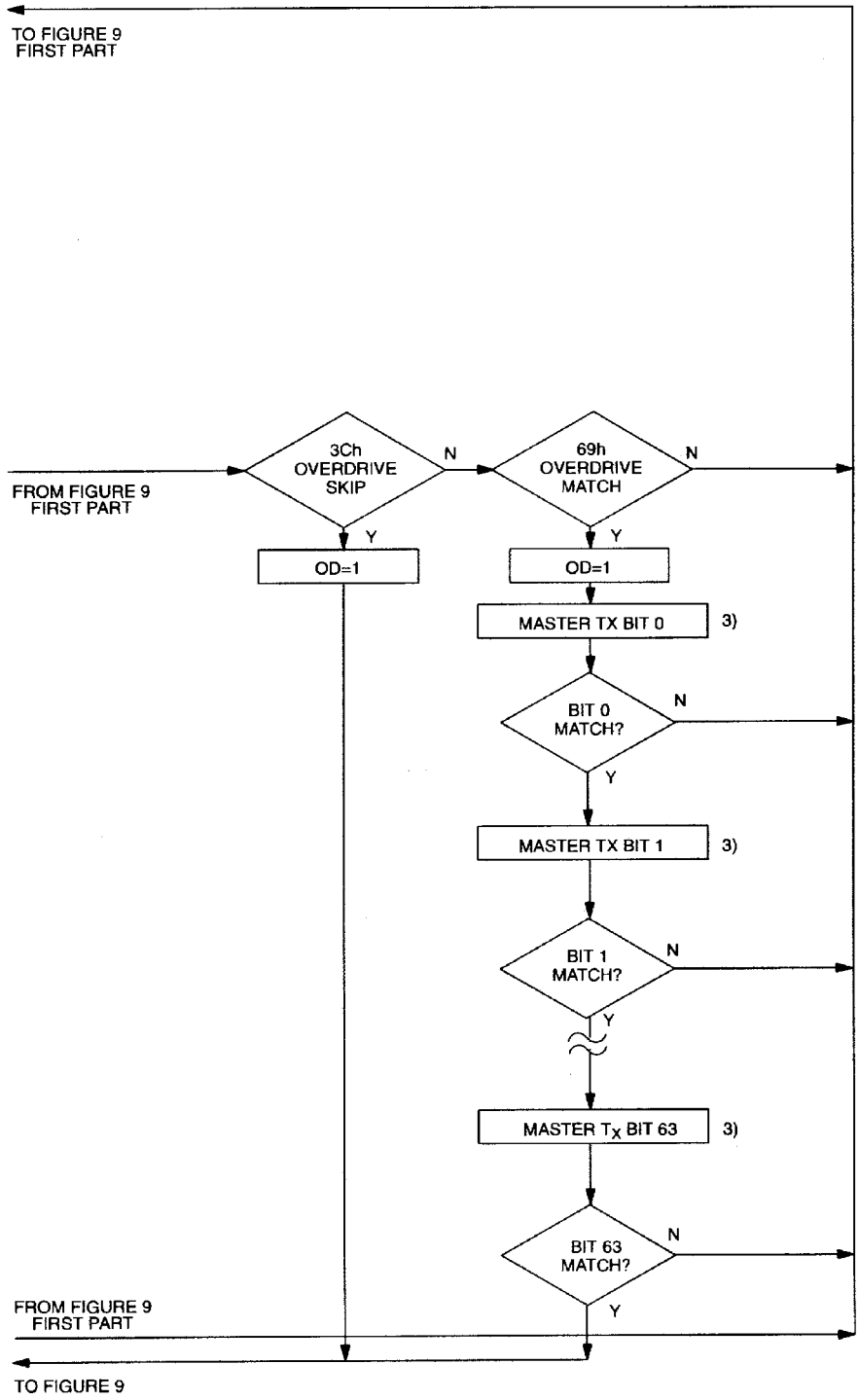
A Reset Pulse of 480 µs or longer will exit the Overdrive Mode returning the device to regular speed. If the DS1996 is in Overdrive Mode and the Reset Pulse is no longer than 80 µs the device will remain in Overdrive Mode.

ROM FUNCTIONS FLOW CHART Figure 9



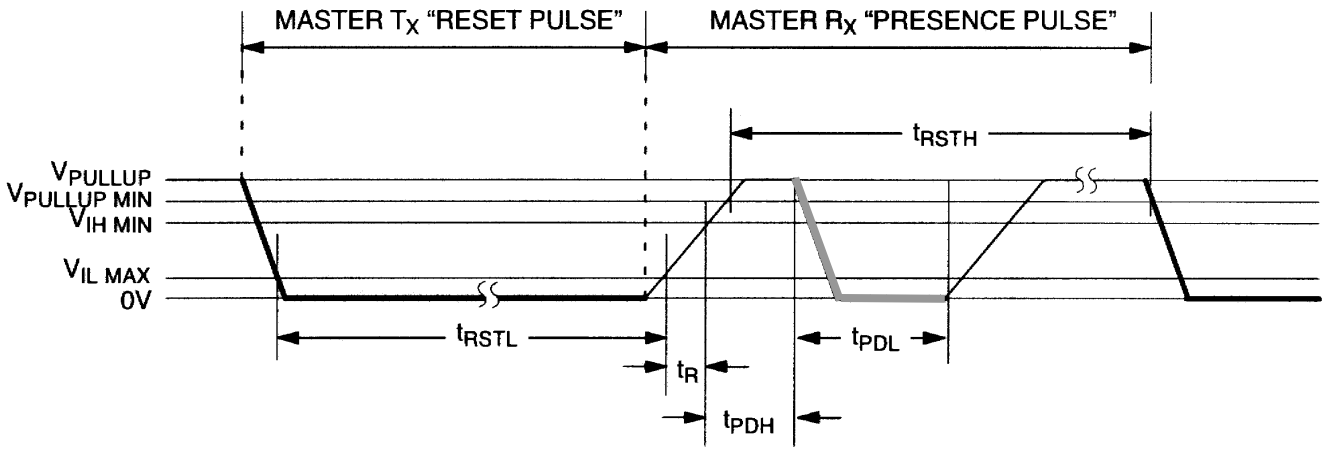
1) TO BE TRANSMITTED OR RECEIVED AT OVERDRIVE SPEED IF OD=1
2) THE PRESENCE PULSE WILL BE SHORT IF OD=1

ROM FUNCTIONS FLOW CHART Figure 9 (cont'd)



3) ALWAYS TO BE TRANSMITTED AT OVERDRIVE SPEED

INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 10



RESISTOR
MASTER
DS1996

Regular Speed	Overdrive Speed
480 µs ≤ t_{RSTL} < ∞ *	48 µs ≤ t_{RSTL} < 80 µs
480 µs ≤ t_{RSTH} < ∞ (includes recovery time)	48 µs ≤ t_{RSTH} < ∞
15 µs ≤ t_{PDH} < 60 µs	2 µs ≤ t_{PDH} < 6 µs
60 µs ≤ t_{PDL} < 240 µs	7 µs ≤ t_{PDL} < 24 µs

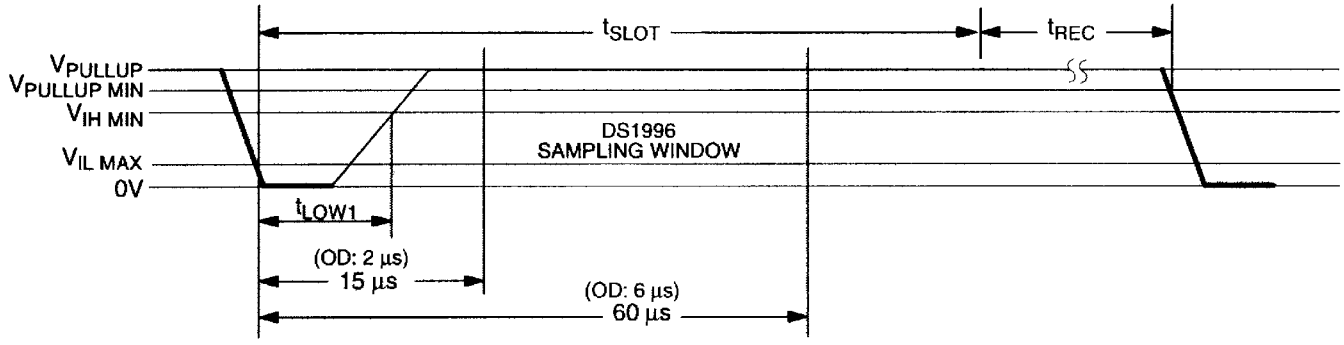
* In order not to mask interrupt signaling by other devices on the 1-Wire bus, t_{RSTL} + t_R should always be less than 960 µs.

READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 11. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS1996 to the master by triggering a delay circuit in the DS1996. During write time slots, the delay circuit determines when the DS1996 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS1996 will hold the data line low overriding the 1 generated by the master. If the data bit is a "1", the iButton will leave the read data time slot unchanged.

READ/WRITE TIMING DIAGRAM Figure 11

Write-One Time Slot

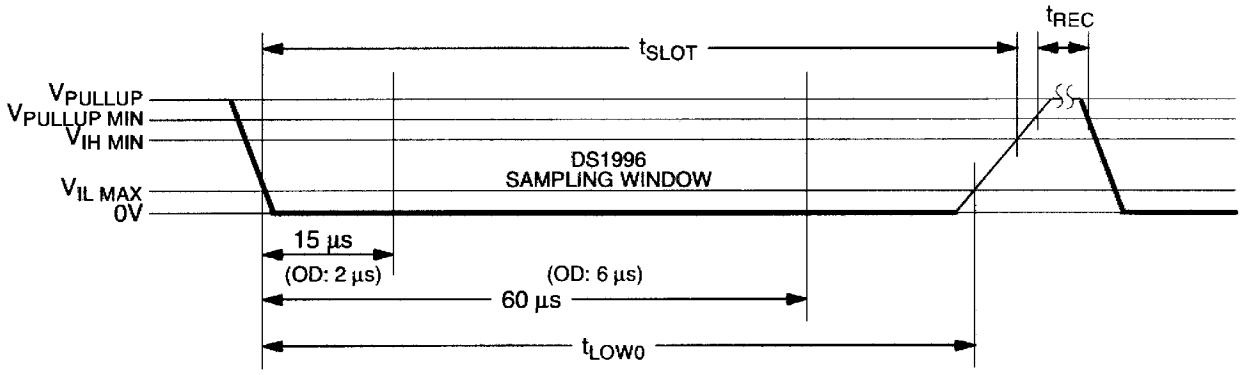


RESISTOR
MASTER

Regular Speed	Overdrive Speed
60 µs ≤ t_{SLOT} < 120 µs	6 µs ≤ t_{SLOT} < 16 µs
1 µs ≤ t_{LOW1} < 15 µs	1 µs ≤ t_{LOW1} < 2 µs
1 µs ≤ t_{REC} < ∞	1 µs ≤ t_{REC} < ∞

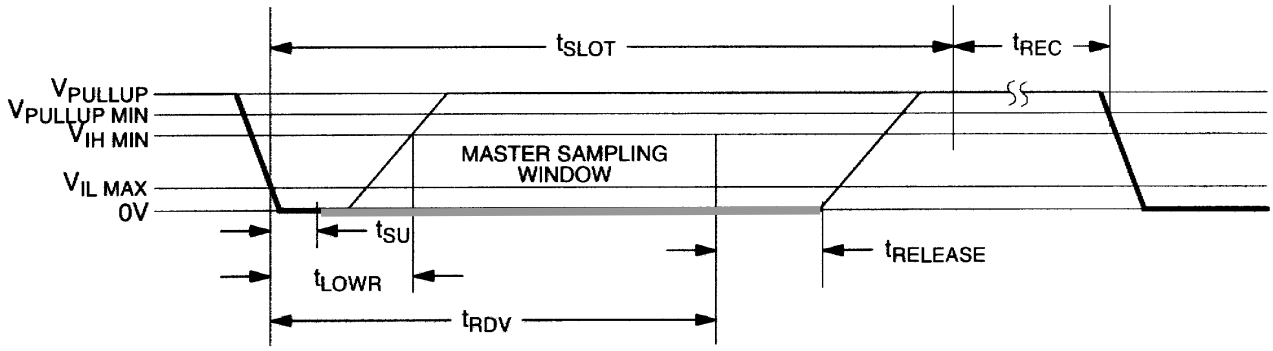
READ/WRITE TIMING DIAGRAM Figure 11 (cont'd)

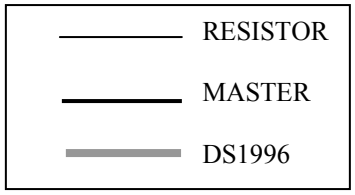
Write-Zero Time Slot



Regular Speed	Overdrive Speed
$60\ \mu s \le t_{LOW0} < t_{SLOT} < 120\ \mu s$	$6\ \mu s \le t_{LOW0} < t_{SLOT} < 16\ \mu s$
$1\ \mu s \le t_{REC} < \infty$	$1\ \mu s \le t_{REC} < \infty$

Read-Data Time Slot





Regular Speed	Overdrive Speed
$60\ \mu s \le t_{SLOT} < 120\ \mu s$	$6\ \mu s \le t_{SLOT} < 16\ \mu s$
$1\ \mu s \le t_{LOWR} < 15\ \mu s$	$1\ \mu s \le t_{LOWR} < 2\ \mu s$
$0 \le t_{RELEASE} < 45\ \mu s$	$0 \le t_{RELEASE} < 4\ \mu s$
$1\ \mu s \le t_{REC} < \infty$	$1\ \mu s \le t_{REC} < \infty$
$t_{RDV} = 15\ \mu s$	$t_{RDV} = 2\ \mu s$
$t_{SU} < 1\ \mu s$	$t_{SU} < 1\ \mu s$

PHYSICAL SPECIFICATIONS

Size	See mechanical drawing
Weight	3.3 grams (F5 package)
Humidity	90% RH at 50°C
Altitude	10,000 feet
Expected Service Life	10 years at 25°C

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	-40°C to +70°C
Storage Temperature	-40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (V_{PUP}=2.8V to 6.0V, -40°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1, 7
Logic 0	V_{IL}	-0.3		+0.3	V	1
Output Logic Low @ 4 mA	V_{OL}			0.4	V	1
Input Load Current	I_L		5		µA	2

CAPACITANCE (T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
I/O (1-Wire)	$C_{IN/OUT}$		100	800	pF	5

AC ELECTRICAL CHARACTERISTICS: REGULAR SPEED (-40°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Data Valid	t_{RDV}		exactly 15		µs	
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	4
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	3
Reset Time Low	t_{RSTL}	480			µs	6
Presence Detect High	t_{PDH}	15		60	µs	
Presence Detect Low	t_{PDL}	60		240	µs	

AC ELECTRICAL CHARACTERISTICS: OVERDRIVE SPEED (-40°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	6		16	µs	
Write 1 Low Time	t_{LOW1}	1		2	µs	
Write 0 Low Time	t_{LOW0}	6		16	µs	
Read Data Valid	t_{RDV}		exactly 2		µs	
Release Time	$t_{RELEASE}$	0	1.5	4	µs	
Read Data Setup	t_{SU}			1	µs	4
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	48			µs	3
Reset Time Low	t_{RSTL}	48		80	µs	
Presence Detect High	t_{PDH}	2		6	µs	
Presence Detect Low	t_{PDL}	7		24	µs	

NOTES:

1. All voltages are referenced to ground.

2. Input load is to ground.

3. An additional reset or communication sequence cannot begin until the reset high time has expired.

4. Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge.

5. Capacitance on the data contact could be 800 pF when power is first applied. If a 5 kΩ resistor is used to pullup the data line to V_{CC}, 5 ms after power has been applied, the parasite capacitance will not affect normal communications.

6. The reset low time (t_{RSTL}) should be restricted to a maximum of 960 µs, to allow interrupt signaling, otherwise, it could mask or conceal interrupt pulses.

7. V_{IH} is a function of the external pullup resistor and the V_{CC} power supply.

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
070808	Updated the *Ordering Information* table to only show the lead-free version (DS1996-F5+).	1
	Updated the F5 MicroCan marking to match PCN H020201.	1
	Updated the wording in the *Parasite Power* section.	2
	Changed the $t_{PDL(MIN)}$ spec from 8µs to 7µs in Figure 10 and in the *AC Electrical Characteristics: Overdrive Speed* table.	15, 18
	In the *DC Electrical Characteristics* table, removed the V_{OH} spec and changed the $V_{IL(MAX)}$ spec from 0.8V to 0.3V.	17
8/09	Removed the UL#913 bullet in the *Common iButton Features* section.	1

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