



**THE DATASHEET OF  
ADS7028IRTER**



# ADS7028 Small, 8-Channel, 12-Bit ADC with SPI Interface, GPIOs, and CRC

## 1 Features

- Small package size:
  - WQFN 3 mm × 3 mm
- 8 channels configurable as any combination of:
  - Up to 8 analog inputs, digital inputs, or digital outputs
- GPIOs for I/O expansion:
  - Open-drain, push-pull digital outputs
- Analog watchdog:
  - Programmable thresholds per channel
  - Event counter for transient rejection
- Wide operating ranges:
  - AVDD: 2.35 V to 5.5 V
  - DVDD: 1.65 V to 5.5 V
  - –40°C to +85°C temperature range
- Enhanced-SPI digital interface:
  - High-speed, 60-MHz interface
  - Achieve full throughput with >13.5-MHz SPI
- CRC for read/write operation:
  - CRC on data read/write
  - CRC on power-up configuration
- Programmable averaging filters
- Root-mean-square module:
  - 16-bit true RMS output
  - Programmable RMS time window
- Zero-crossing-detect module:
  - ZCD output corresponding to analog input
  - Built-in transient rejection and hysteresis
  - Digitally adjustable detection threshold

## 2 Applications

- [Refrigerator and freezer](#)
- [Rack server](#)
- [Mixed module \(AI, AO, DI, DO\)](#)
- [AC drive power stage module](#)

## 3 Description

The ADS7028 is an easy-to-use, 8-channel, multiplexed, 12-bit, 1-MSPS, successive approximation register analog-to-digital converter (SAR ADC). The eight channels can be independently configured as either analog inputs, digital inputs, or digital outputs. The device has an internal oscillator for the ADC conversion process.

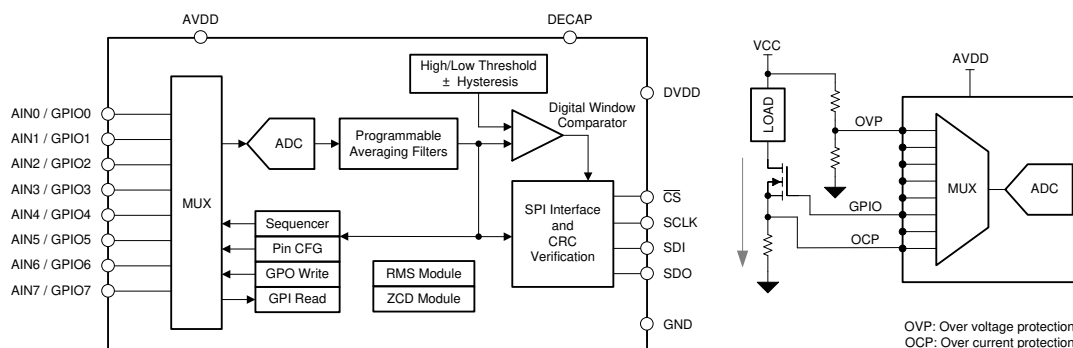
The ADS7028 communicates through an SPI-compatible interface and operates in either autonomous or single-shot conversion mode. The ADS7028 implements the analog watchdog function by event-triggered interrupts per channel using a digital window comparator with programmable high and low thresholds, hysteresis, and an event counter. The ADS7028 has a built-in cyclic redundancy check (CRC) for data read/write operations and the power-up configuration. The ADS7028 features a root-mean-square (RMS) module that computes a 16-bit true RMS result for any analog input channel. The integrated zero-crossing-detect (ZCD) module allows for transient rejection and hysteresis near the configurable threshold crossings.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS7028	WQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

## ADS7028 Block Diagram and Applications



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## 4 Revision History

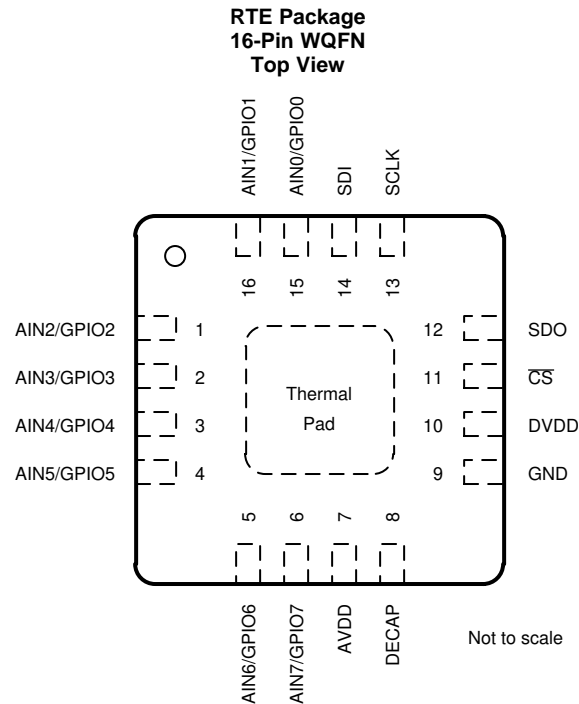
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2019) to Revision A	Page
• Changed device status from advance information to production data .....	<b>1</b>

## 5 Device Comparison Table

PART NUMBER	DESCRIPTION	CRC MODULE	ZERO-CROSSING-DETECT (ZCD) MODULE	ROOT-MEAN-SQUARE (RMS) MODULE
ADS7028	8-channel, 12-bit ADC with SPI interface and GPIOs	Yes	Yes	Yes
ADS7038		Yes	No	No
ADS7038-Q1		Yes	No	No

## 6 Pin Configuration and Functions



### Pin Functions

PIN		FUNCTION <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
AIN0/GPIO0	15	AI, DI, DO	Channel 0; can be configured as either an analog input (default), digital input, or digital output.
AIN1/GPIO1	16	AI, DI, DO	Channel 1; can be configured as either an analog input (default), digital input, or digital output.
AIN2/GPIO2	1	AI, DI, DO	Channel 2; can be configured as either an analog input (default), digital input, or digital output.
AIN3/GPIO3	2	AI, DI, DO	Channel 3; can be configured as either an analog input (default), digital input, or digital output.
AIN4/GPIO4	3	AI, DI, DO	Channel 4; can be configured as either an analog input (default), digital input, or digital output.
AIN5/GPIO5	4	AI, DI, DO	Channel 5; can be configured as either an analog input (default), digital input, or digital output.
AIN6/GPIO6	5	AI, DI, DO	Channel 6; can be configured as either an analog input (default), digital input, or digital output.
AIN7/GPIO7	6	AI, DI, DO	Channel 7; can be configured as either an analog input (default), digital input, or digital output.
AVDD	7	Supply	Analog supply input, also used as the reference voltage to the ADC; connect a 1- $\mu$ F decoupling capacitor to GND.
$\overline{\text{CS}}$	11	DI	Chip-select input pin; active low. The device takes control of the data bus when $\overline{\text{CS}}$ is low. The device starts converting the active input channel on the rising edge of $\overline{\text{CS}}$ . SDO goes hi-Z when $\overline{\text{CS}}$ is high.
DECAP	8	Supply	Connect a 1- $\mu$ F decoupling capacitor to GND for the internal power supply.
DVDD	10	Supply	Digital I/O supply voltage; connect a 1- $\mu$ F decoupling capacitor to GND.
GND	9	Supply	Ground for the power supply; all analog and digital signals are referred to this pin voltage.
SCLK	13	DI	Serial clock for the SPI interface.
SDI	14	DI	Serial data in for the device.
SDO	12	DO	Serial data out for the device.
Thermal pad	—	Supply	Exposed thermal pad; connect to GND.

(1) AI = analog input, DI = digital input, and DO = digital output.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

Over operating ambient temperature range (unless otherwise noted)<sup>(1)</sup>.

	MIN	MAX	UNIT
DVDD to GND	-0.3	5.5	V
AVDD to GND	-0.3	5.5	V
AINx / GPOx <sup>(2)</sup> to GND	GND - 0.3	AVDD + 0.3	V
Digital input to GND	GND - 0.3	5.5	V
Current through any pin except supply pins <sup>(3)</sup>	-10	10	mA
Junction temperature, T <sub>J</sub>	-40	125	°C
Storage temperature, T <sub>stg</sub>	-60	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) AINx / GPIOx refers to pins 1, 2, 3, 4, 5, 6, 15, and 16.
- (3) Pin current must be limited to 10 mA or less.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLY</b>						
AVDD	Analog supply voltage		2.35	3.3	5.5	V
DVDD	Digital supply voltage		1.65	3.3	5.5	V
<b>ANALOG INPUTS</b>						
FSR	Full-scale input range	AIN <sub>x</sub> - GND	0		AVDD	V
V <sub>IN</sub>	Absolute input voltage	AIN <sub>x</sub> - GND	-0.1		AVDD + 0.1	V
<b>TEMPERATURE RANGE</b>						
T <sub>A</sub>	Ambient temperature		-40	25	85	°C

- (1) AINx refers to AIN0, AIN1, AIN2, AIN3, AIN4, AIN5, AIN6, and AIN7.

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ADS7028	UNIT
		RTE (WQFN)	
		16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	49.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	53.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	24.7	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.3	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	24.7	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	9.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

At AVDD = 2.35 V to 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T<sub>A</sub> = –40°C to +85°C; typical values at T<sub>A</sub> = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ANALOG INPUTS</b>						
C <sub>SH</sub>	Sampling capacitance			12		pF
<b>DC PERFORMANCE</b>						
	Resolution	No missing codes		12		bits
DNL	Differential nonlinearity		–0.75	±0.3	0.75	LSB
INL	Integral nonlinearity		–1.3	±0.5	1.3	LSB
V <sub>(OS)</sub>	Input offset error	Post offset calibration	–2	±0.3	2	LSB
	Input offset thermal drift	Post offset calibration		±1		ppm/°C
G <sub>E</sub>	Gain error		–0.075	±0.05	0.075	%FSR
	Gain error thermal drift			±1		ppm/°C
<b>AC PERFORMANCE</b>						
SINAD	Signal-to-noise + distortion ratio	AVDD = 5 V, f <sub>IN</sub> = 2 kHz	70.2	72.9		dB
		AVDD = 3 V, f <sub>IN</sub> = 2 kHz	70.2	72.7		
SNR	Signal-to-noise ratio	AVDD = 5 V, f <sub>IN</sub> = 2 kHz	71.2	73.1		dB
		AVDD = 3 V, f <sub>IN</sub> = 2 kHz	70.5	72.9		
THD	Total harmonic distortion	f <sub>IN</sub> = 2 kHz		–87.5		dB
SFDR	Spurious-free dynamic range	f <sub>IN</sub> = 2 kHz		91		dB
	Isolation crosstalk	f <sub>IN</sub> = 100 kHz		–100		dB
<b>DECAP Pin</b>						
	Decoupling capacitor on DECAP pin		0.22	1	4.7	μF
<b>SPI INTERFACE (<math>\overline{\text{CS}}</math>, SCLK, SDI, SDO)</b>						
V <sub>IH</sub>	Input high logic level		0.7 x DVDD		5.5	V
V <sub>IL</sub>	Input low logic level		–0.3		0.3 x DVDD	V
V <sub>OH</sub>	Output high logic level	Source current = 2 mA, DVDD > 2 V	0.8 x DVDD		DVDD	V
		Source current = 2 mA, DVDD ≤ 2 V	0.7 x DVDD		DVDD	
V <sub>OL</sub>	Output low logic level	Sink current = 2 mA, DVDD > 2 V	0		0.4	V
		Sink current = 2 mA, DVDD ≤ 2 V	0		0.2 x DVDD	
<b>GPIOs</b>						
V <sub>IH</sub>	Input high logic level		0.7 x AVDD		AVDD + 0.3	V
V <sub>IL</sub>	Input low logic level		–0.3		0.3 x AVDD	V
	Input leakage current	GPIO configured as input		10	100	nA
V <sub>OH</sub>	Output high logic level	GPO_DRIVE_CFG = push-pull, I <sub>SOURCE</sub> = 2 mA	0.8 x AVDD		AVDD	V
V <sub>OL</sub>	Output low logic level	I <sub>SINK</sub> = 2 mA	0		0.2 x AVDD	V
I <sub>OH</sub>	Output high source current	V <sub>OH</sub> > 0.7 x AVDD			5	mA
I <sub>OL</sub>	Output low sink current	V <sub>OL</sub> < 0.3 x AVDD			5	mA
<b>POWER-SUPPLY CURRENTS</b>						
I <sub>AVDD</sub>	Analog supply current	Full throughput, AVDD = 5 V		600	660	μA
		Full throughput, AVDD = 3 V		560	610	
		No conversion, AVDD = 5 V		7	15	

## 7.6 Timing Requirements

At AVDD = 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T<sub>A</sub> = –40°C to +85°C; typical values at T<sub>A</sub> = 25°C.

		MIN	MAX	UNIT
<b>CONVERSION CYCLE</b>				
f <sub>CYCLE</sub>	Sampling frequency		1000	kSPS
t <sub>CYCLE</sub>	ADC cycle-time period	1 / f <sub>CYCLE</sub>		s
t <sub>ACQ</sub>	Acquisition time	400		ns
t <sub>QT_ACQ</sub>	Quiet acquisition time	10		ns
t <sub>D_CNVCAP</sub>	Quiet conversion time	10		ns
t <sub>WH_CSZ</sub>	Pulse duration: $\overline{CS}$ high	200		ns
t <sub>WL_CSZ</sub>	Pulse duration: $\overline{CS}$ low	200		ns
<b>SPI INTERFACE TIMINGS</b>				
f <sub>CLK</sub>	Maximum SCLK frequency		60	MHz
t <sub>CLK</sub>	Minimum SCLK time period	16.67		ns
t <sub>PH_CK</sub>	SCLK high time	0.45	0.55	t <sub>CLK</sub>
t <sub>PL_CK</sub>	SCLK low time	0.45	0.55	t <sub>CLK</sub>
t <sub>SU_CSCK</sub>	Setup time: $\overline{CS}$ falling to the first SCLK capture edge	3.5		ns
t <sub>SU_CKDI</sub>	Setup time: SDI data valid to the SCLK capture edge	1.5		ns
t <sub>HT_CKDI</sub>	Hold time: SCLK capture edge to data valid on SDI	2		ns
t <sub>D_CKCS</sub>	Delay time: last SCLK falling to $\overline{CS}$ rising	6		ns

## 7.7 Switching Characteristics

At AVDD = 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T<sub>A</sub> = –40°C to +85°C; typical values at T<sub>A</sub> = 25°C.

PARAMETER	Test Conditions	MIN	MAX	UNIT	
<b>CONVERSION CYCLE</b>					
t <sub>CONV</sub>	ADC conversion time		600	ns	
<b>RESET and ALERT</b>					
t <sub>PU</sub>	Power-up time for device	AVDD ≥ 2.35 V, C <sub>DECAP</sub> = 1 μF	5	ms	
t <sub>RST</sub>	Delay time; RST bit = 1b to device reset complete <sup>(1)</sup>		5	ms	
t <sub>ALERT_HI</sub>	ALERT high period	ALERT_LOGIC[1:0] = 1x	50	150	ns
t <sub>ALERT_LO</sub>	ALERT low period	ALERT_LOGIC[1:0] = 1x	50	150	ns
<b>SPI INTERFACE TIMINGS</b>					
t <sub>DEN_CSDO</sub>	Delay time: $\overline{CS}$ falling to data enable		15	ns	
t <sub>DZ_CSDO</sub>	Delay time: $\overline{CS}$ rising to SDO going Hi-Z		15	ns	
t <sub>D_CKDO</sub>	Delay time: SCLK launch edge to (next) data valid on SDO		16	ns	

(1) RST bit is automatically reset to 0b after t<sub>RST</sub>.

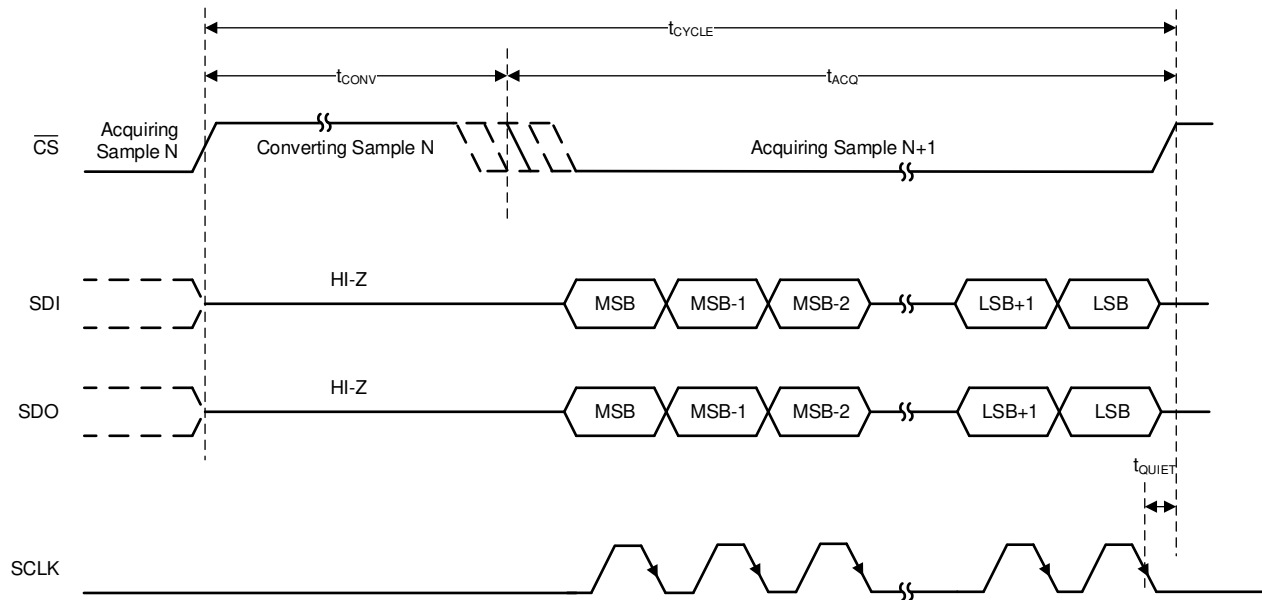
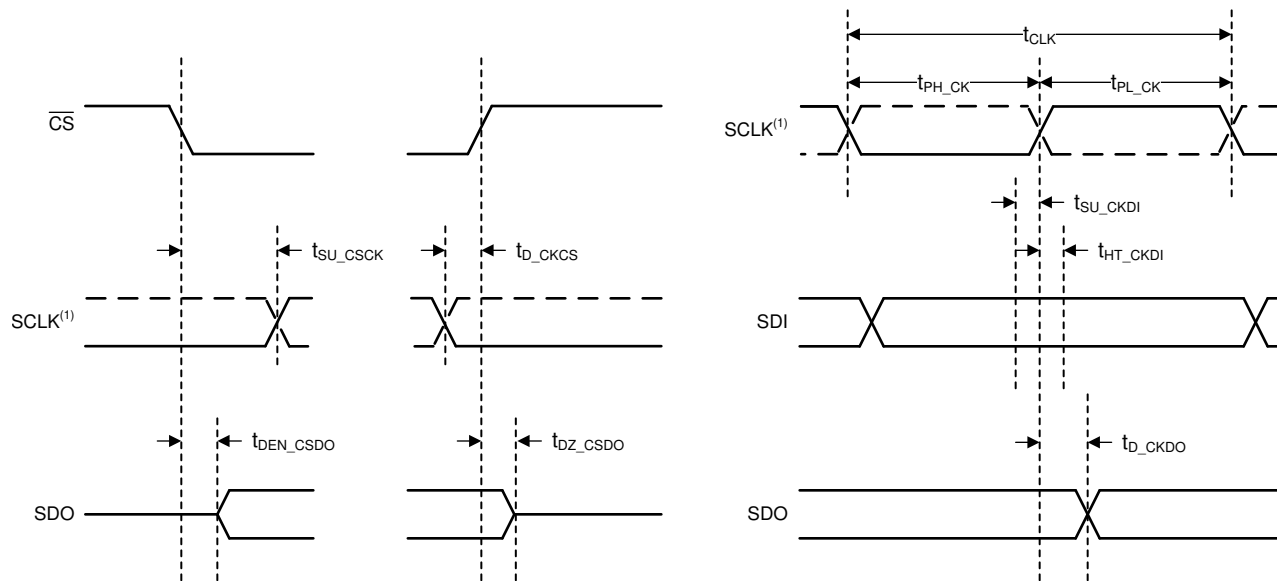


Figure 1. Conversion Cycle Timing

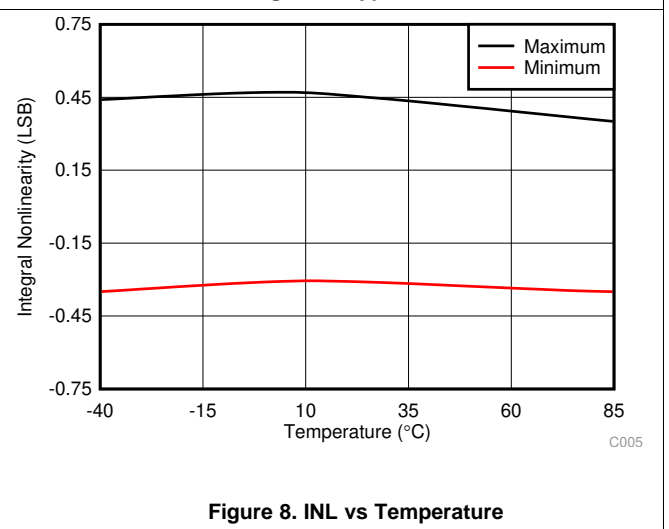
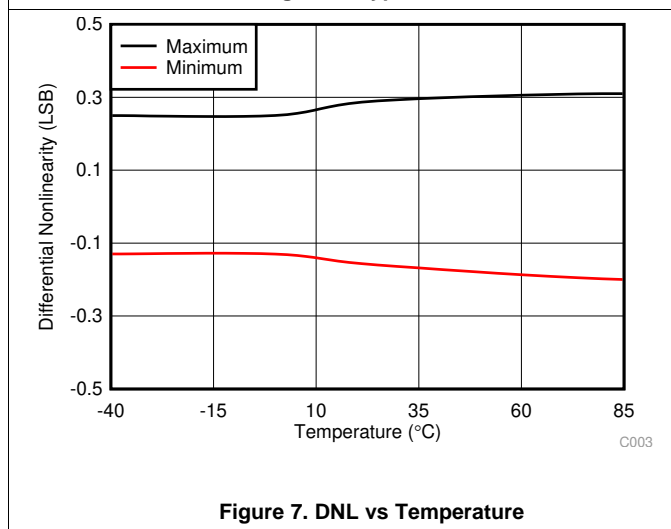
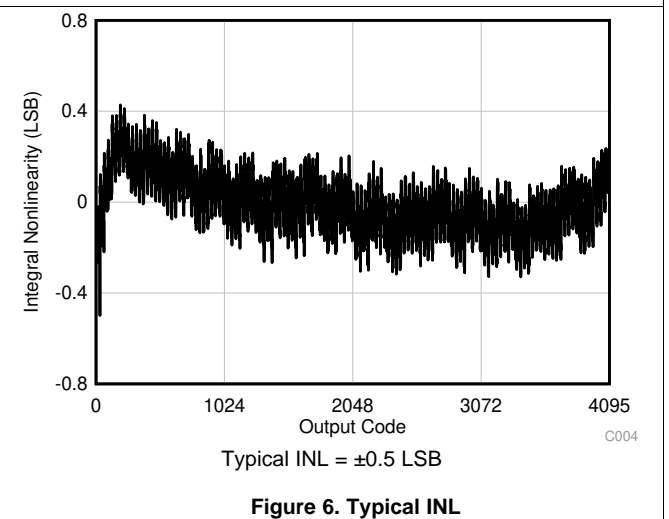
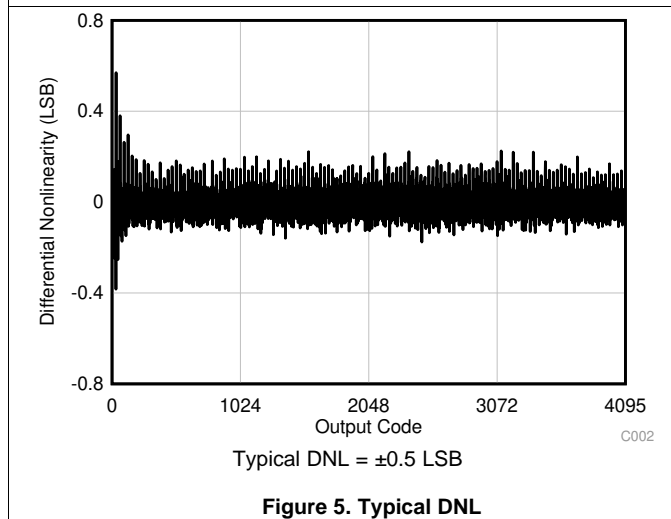
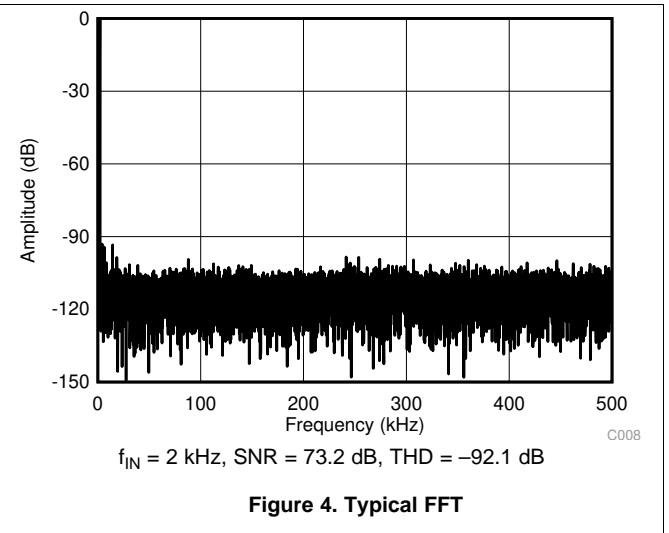
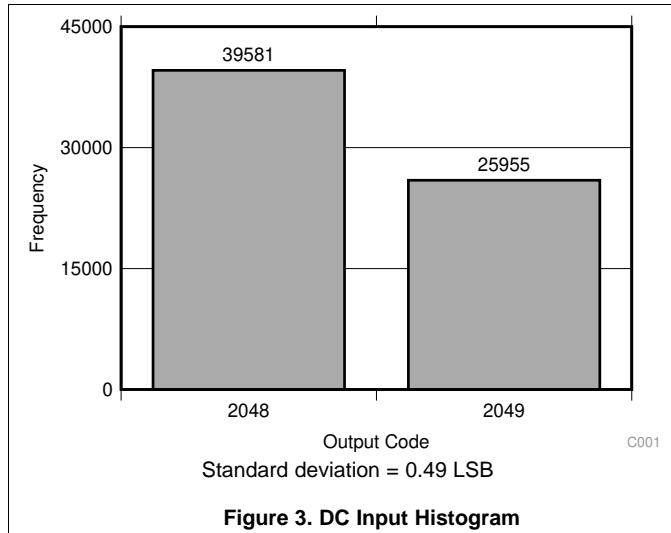


(1) The SCLK polarity, launch edge, and capture edge depend on the SPI protocol selected.

Figure 2. SPI-Compatible Serial Interface Timing

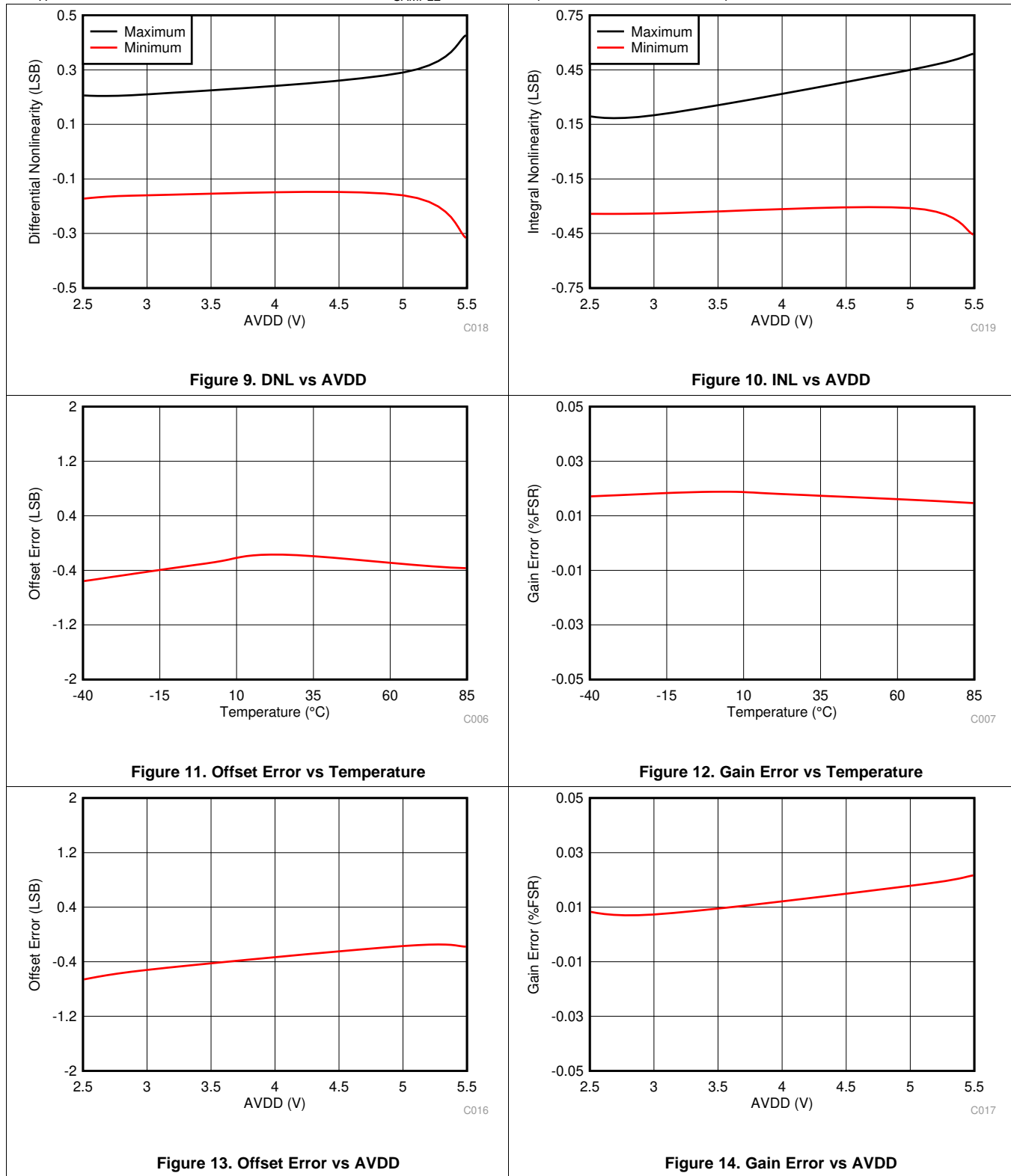
### 7.8 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 1.8\text{ V}$ , and  $f_{\text{SAMPLE}} = 1\text{ MSPS}$  (unless otherwise noted).



### Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 1.8\text{ V}$ , and  $f_{\text{SAMPLE}} = 1\text{ MSPS}$  (unless otherwise noted).



Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 1.8\text{ V}$ , and  $f_{\text{SAMPLE}} = 1\text{ MSPS}$  (unless otherwise noted).

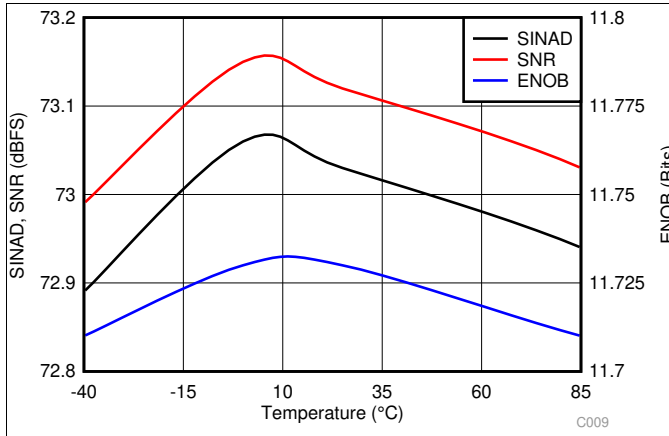


Figure 15. Noise Performance vs Temperature

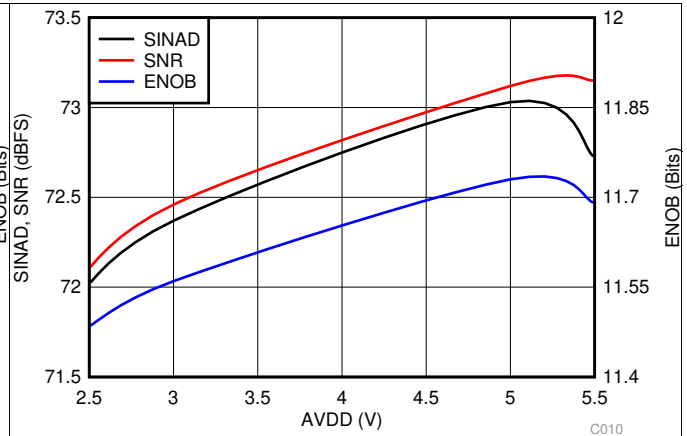


Figure 16. Noise Performance vs AVDD

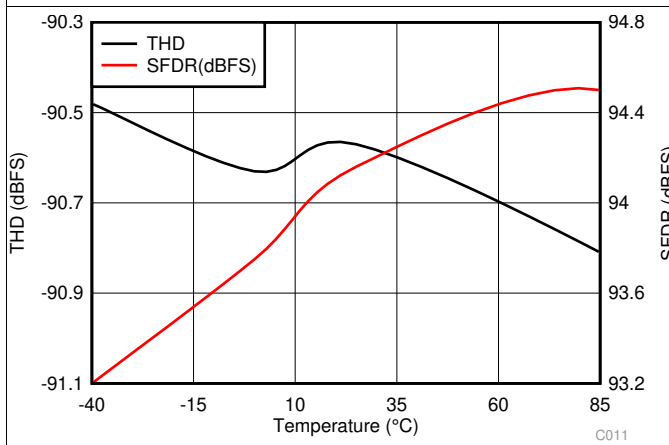


Figure 17. Distortion Performance vs Temperature

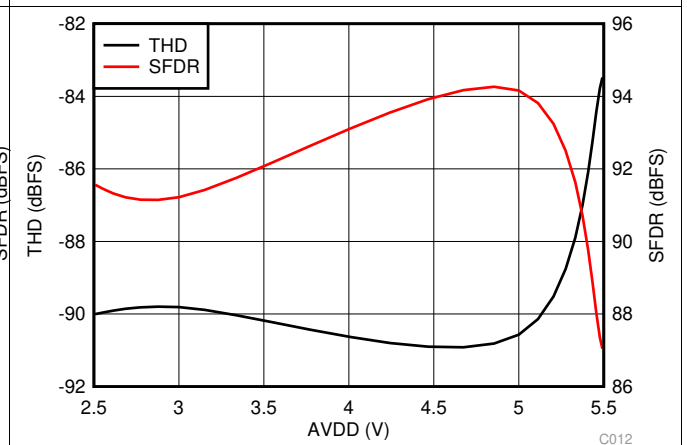


Figure 18. Distortion Performance vs AVDD

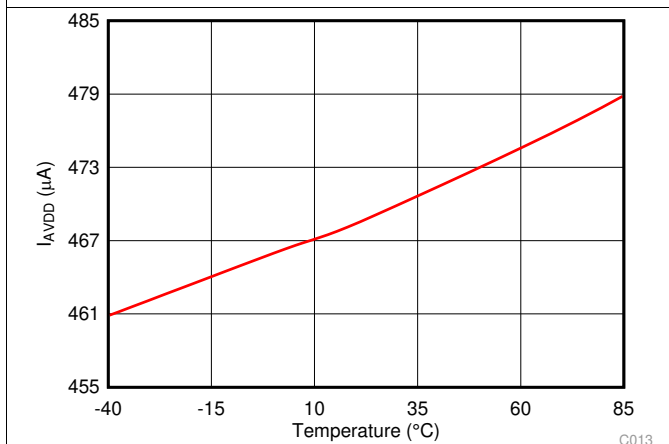


Figure 19. Analog Supply Current vs Temperature

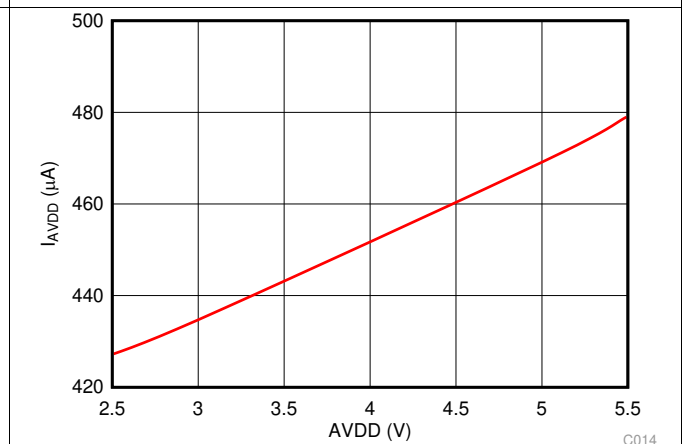
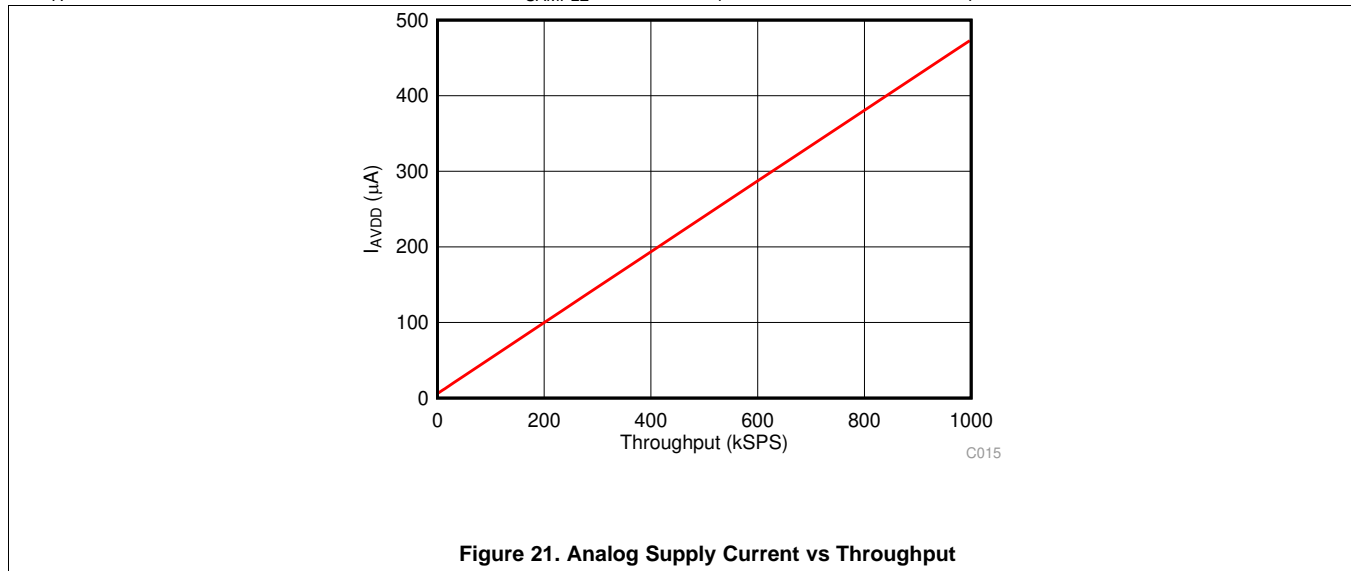


Figure 20. Analog Supply Current vs AVDD

**Typical Characteristics (continued)**

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 1.8\text{ V}$ , and  $f_{\text{SAMPLE}} = 1\text{ MSPS}$  (unless otherwise noted).



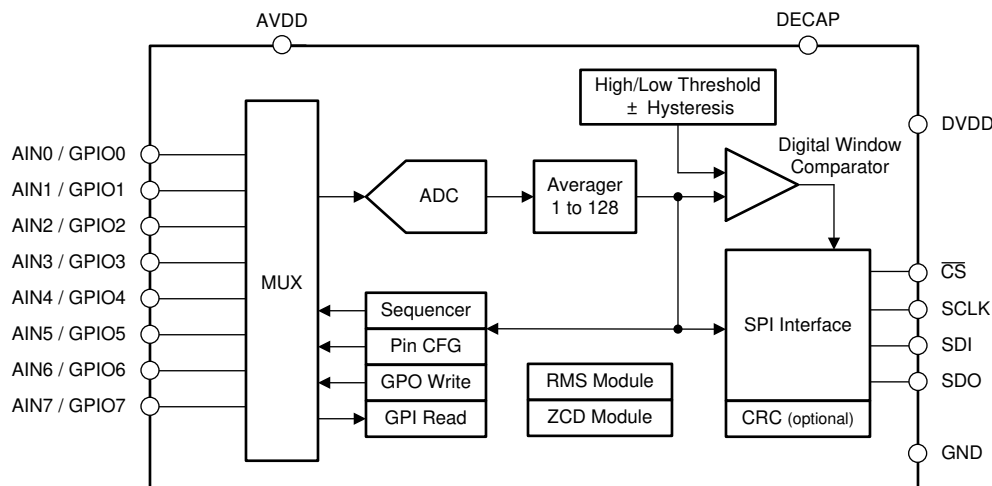
## 8 Detailed Description

### 8.1 Overview

The ADS7028 is a small, eight-channel, multiplexed, 12-bit, 1-MSPS, analog-to-digital converter (ADC) with an enhanced-SPI serial interface. The eight channels of the ADS7028 can be individually configured as either analog inputs, digital inputs, or digital outputs. The device includes a digital comparator which can be used to interrupt the host when a programmed high or low threshold is crossed on any input channel. The device uses an internal oscillator for conversion. The ADC can be used in manual mode for reading ADC data over the SPI interface or in autonomous mode for monitoring the analog inputs without an active SPI interface.

The device features a programmable averaging filter that outputs a 16-bit result for enhanced resolution. The root-mean-square (RMS) module computes a 16-bit true RMS result of any analog input channel over a configurable time window. The zero-crossing-detect (ZCD) module can be used to generate a digital output corresponding to the programmable threshold crossings of any analog input channel.

### 8.2 Functional Block Diagram

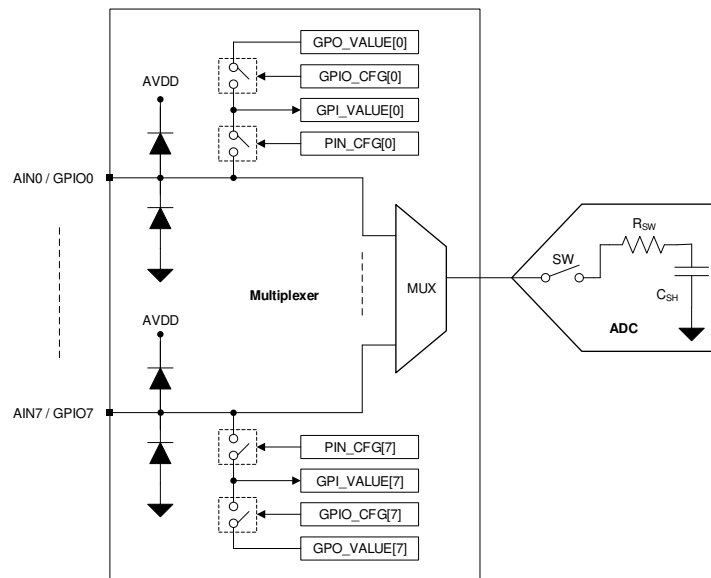


## 8.3 Feature Description

### 8.3.1 Multiplexer and ADC

The eight channels of the multiplexer can be independently configured as ADC inputs or general-purpose inputs/outputs (GPIOs). [Figure 22](#) shows that each input pin has ESD protection diodes to AVDD and GND. On power-up or after device reset, all eight multiplexer channels are configured as analog inputs.

[Figure 22](#) shows an equivalent circuit for pins configured as analog inputs. The ADC sampling switch is represented by ideal switch (SW) in series with the resistor  $R_{SW}$  (typically 150  $\Omega$ ) and the sampling capacitor,  $C_{SH}$  (typically 12 pF).



**Figure 22. Analog Inputs, GPIOs, and ADC Connections**

During acquisition, the SW switch is closed to allow the signal on the selected analog input channel to charge the internal sampling capacitor. During conversion, the SW switch is opened to disconnect the analog input channel from the sampling capacitor.

The multiplexer channels can be configured as GPIOs in the PIN\_CFG register. The direction of a GPIO (either as an input or an output) can be set in the GPIO\_CFG register. The logic level on the channels configured as digital inputs can be read from the GPI\_VALUE register. The digital outputs can be accessed by writing to the GPO\_VALUE register. The digital outputs can be configured as either open-drain or push-pull in the GPO\_DRIVE\_CFG register.

### 8.3.2 Reference

The device uses the analog supply voltage (AVDD) as a reference for the analog-to-digital conversion process. TI recommends connecting a 1- $\mu$ F, low-equivalent series resistance (ESR) ceramic decoupling capacitor between the AVDD and GND pins.

### 8.3.3 ADC Transfer Function

The ADC output is in straight binary format. [Equation 1](#) computes the ADC resolution:

$$1 \text{ LSB} = V_{REF} / 2^N$$

where:

- $V_{REF} = AVDD$
- $N = 12$

(1)

## Feature Description (continued)

Figure 23 and Table 1 detail the transfer characteristics for the device.

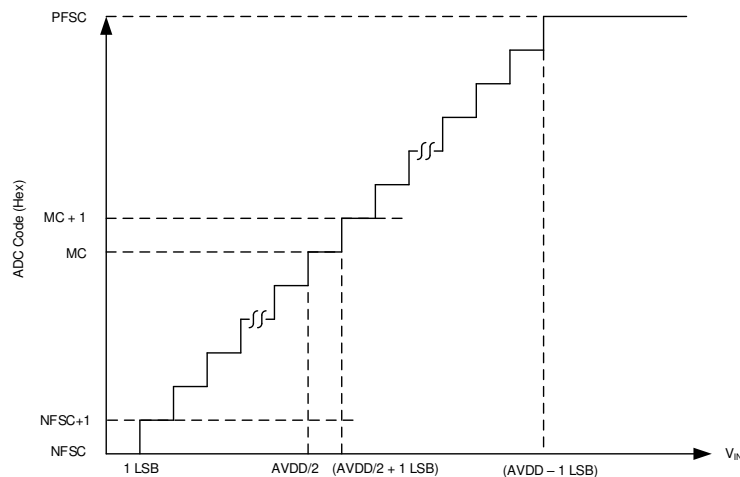


Figure 23. Ideal Transfer Characteristics

Table 1. Transfer Characteristics

INPUT VOLTAGE FOR SINGLE-ENDED INPUT	CODE	DESCRIPTION	IDEAL OUTPUT CODE
$\leq 1$ LSB	NFSC	Negative full-scale code	000
1 LSB to 2 LSBs	NFSC + 1	—	001
$(AVDD / 2)$ to $(AVDD / 2) + 1$ LSB	MC	Mid code	800
$(AVDD / 2) + 1$ LSB to $(AVDD / 2) + 2$ LSB	MC + 1	—	801
$\geq AVDD - 1$ LSB	PFSC	Positive full-scale code	FFF

### 8.3.4 ADC Offset Calibration

The variation in ADC offset error resulting from changes in temperature or AVDD can be calibrated by setting the CAL bit in the GENERAL\_CFG register. The CAL bit is reset to 0 after calibration. The host can poll the CAL bit to check the ADC offset calibration completion status.

### 8.3.5 Programmable Averaging Filter

The ADS7028 features a built-in oversampling (OSR) function that can be used to average several samples. The averaging filter can be enabled by programming the OSR[2:0] bits in the OSR\_CFG register. The averaging filter configuration is common to all analog input channels. Figure 24 shows that the averaging filter module output is 16 bits long. In manual conversion mode and auto-sequence mode, only the first conversion for the selected analog input channel must be initiated by the host; see the *Manual Mode* and *Auto-Sequence Mode* sections. As shown in Figure 24, any remaining conversions for the selected averaging factor are generated internally. The time required to complete the averaging operation is determined by the sampling speed and number of samples to be averaged. As shown in Figure 24, the 16-bit result can be read out after the averaging operation completes.

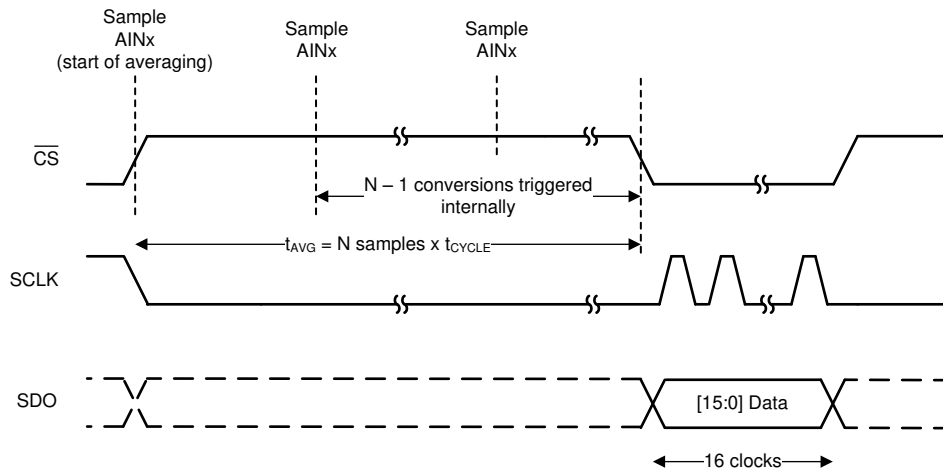


Figure 24. Averaging Example

In autonomous mode of operation, samples from analog input channels that are enabled in the AUTO\_SEQ\_CH\_SEL register are averaged sequentially. The digital window comparator compares the top 12 bits of the 16-bit average result with the thresholds.

Equation 2 provides the LSB value of the 16-bit average result.

$$1 \text{ LSB} = \frac{AVDD}{2^{16}} \tag{2}$$

### 8.3.6 CRC on Data Interface

The ADS7028 features a cyclic redundancy check (CRC) module for checking the integrity of the data bits exchanged over the SPI interface. The CRC module is bidirectional, which appends an 8-bit CRC to every byte read from the device and also evaluates the CRC of every incoming byte over the SPI interface. The CRC module uses the CRC-8-CCITT polynomial ( $x^8 + x^2 + x + 1$ ) for CRC computation.

To enable the CRC module, set the CRC\_EN bit in the GENERAL\_CFG register. Table 2 shows the different ways that a CRC error that occurs when configuring the ADS7028 can be detected.

Table 2. Configuring Notifications when CRC Error is Detected

CRC ERROR NOTIFICATION	CONFIGURATION	DESCRIPTION
ALERT	ALERT_CRCIN = 1b	ALERT (internal signal) is asserted if a CRC error is detected
Status flags	APPEND_STATUS = 10b	4-bit status flags are appended to the ADC data. See the <i>Output Data Format</i> section for details.
Register read	—	Read the CRCERR_IN bit to check if a CRC error was detected.

When the ADS7028 detects a CRC error on the SPI interface, the erroneous data are ignored and the CRCERR\_IN bit is set. Additional notifications can be enabled as described in [Table 2](#). Further register writes are disabled until the CRCERR\_IN bit is cleared by writing 1b to this bit. When using autonomous conversion mode, further conversions can be disabled on a CRC error on the SPI interface by setting CONV\_ON\_ERR = 1b.

### 8.3.7 General-Purpose I/Os

The eight channels of the ADS7028 can be independently configured as analog inputs, digital inputs, or digital outputs. [Table 3](#) describes how the PIN\_CFG and GPIO\_CFG registers can be used to configure the device channels.

**Table 3. Configuring Channels as Analog Inputs or GPIOs**

PIN_CFG[7:0]	GPIO_CFG[7:0]	GPO_DRIVE_CFG[7:0]	CHANNEL CONFIGURATION
0	x	x	Analog input (default)
1	0	x	Digital input
1	1	0	Digital output; open-drain driver
1	1	1	Digital output; push-pull driver

Digital outputs can be configured to logic 1 or 0 by writing to the GPO\_VALUE register. Reading the GPI\_VALUE register returns the logic level for all channels configured as digital inputs or digital outputs. The GPI\_VALUE register can be read to detect a failure in external components, such as a floating pullup resistor or a low-impedance pulldown resistor, that prevents digital outputs being set to the desired logic level.

### 8.3.8 Oscillator and Timing Control

The device uses an internal oscillator for conversion. When using the averaging module, the host initiates the first conversion and subsequent conversions are generated internally by the device. Also, in autonomous mode of operation, the start of the conversion signal is generated by the device. [Table 4](#) describes how the sampling rate can be controlled by the OSC\_SEL and CLK\_DIV[3:0] register fields when the device generates the start of the conversion.

**Table 4. Configuring Sampling Rate for Internal Conversion Start Control**

CLK_DIV[3:0]	OSC_SEL = 0		OSC_SEL = 1	
	SAMPLING FREQUENCY, $f_{\text{CYCLE}}$ (kSPS)	CYCLE TIME, $t_{\text{CYCLE}}$ ( $\mu\text{s}$ )	SAMPLING FREQUENCY, $f_{\text{CYCLE}}$ (kSPS)	CYCLE TIME, $t_{\text{CYCLE}}$ ( $\mu\text{s}$ )
0000b	1000	1	31.25	32
0001b	666.7	1.5	20.83	48
0010b	500	2	15.63	64
0011b	333.3	3	10.42	96
0100b	250	4	7.81	128
0101b	166.7	6	5.21	192
0110b	125	8	3.91	256
0111b	83	12	2.60	384
1000b	62.5	16	1.95	512
1001b	41.7	24	1.3	768
1010b	31.3	32	0.98	1024
1011b	20.8	48	0.65	1536
1100b	15.6	64	0.49	2048
1101b	10.4	96	0.33	3072
1110b	7.8	128	0.24	4096
1111b	5.2	192	0.16	6144

The conversion time of the device, given by  $t_{CONV}$  in the *Switching Characteristics* table, is independent of the OSC\_SEL and CLK\_DIV[3:0] configuration.

### 8.3.9 Output Data Format

Figure 25 depicts various SPI frames for reading data. The data output is MSB aligned. If averaging is enabled the output data from the ADC are 16 bits long, otherwise the output data are 12 bits long. Optionally, a 4-bit channel ID or status flags can be appended at the end of the output data by configuring the APPEND\_STATUS[1:0] field.

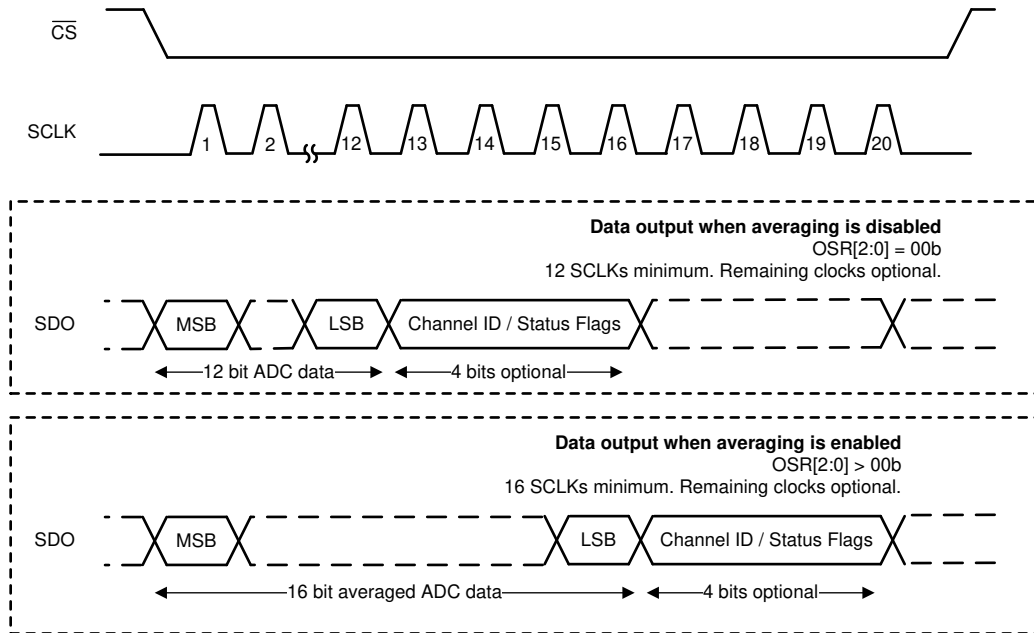


Figure 25. SPI Frames for Reading Data

### 8.3.10 Zero-Crossing-Detect Module

The zero-crossing-detect (ZCD) module generates a digital output corresponding to the designated analog input signal crossing a configured threshold. Figure 26 shows the digital output corresponding to the threshold crossings of an analog input. In order to detect the threshold crossings on a particular analog input, configure the 4-bit channel ID in the ZCD\_CHID register. The threshold crossing to be detected can be configured in the corresponding HIGH\_TH register. The output of the ZCD module can be connected to any digital output by configuring the ZCD\_TRIG\_EN and GPO\_VALUE\_ZCD registers.

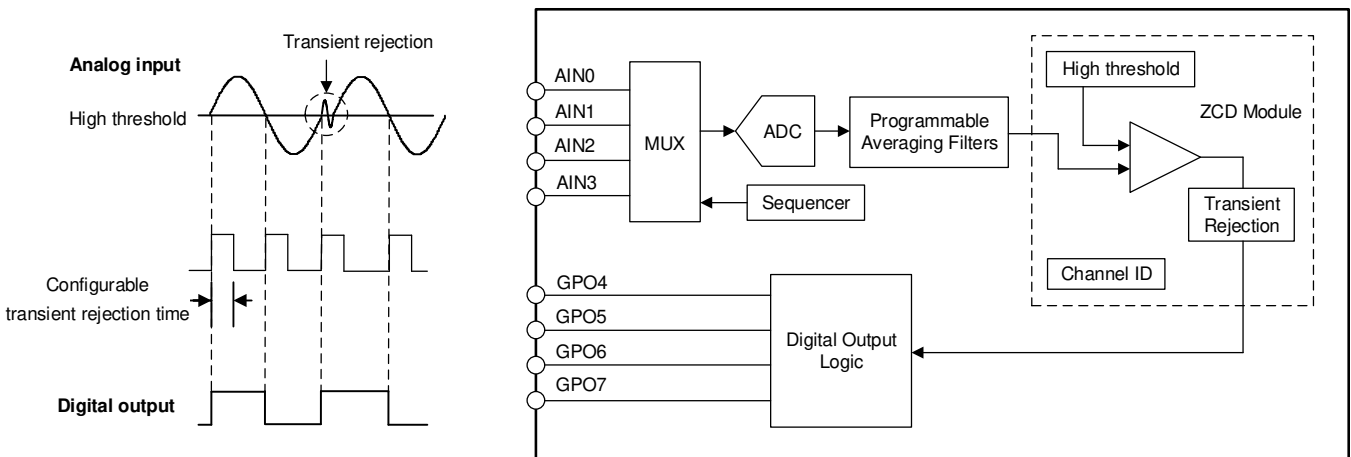


Figure 26. ZCD Module Operation and Block Diagram

The ADC conversion result of the selected analog input channel is compared with the digital threshold that then sets the digital output accordingly. Transients near zero crossings can be rejected, as calculated in Equation 3, by configuring the ZCD\_BLANKING register.

$$\text{transient rejection time} = \text{MULT\_EN} \times \text{ZCD\_BLANKING}[6:0] \times \frac{1}{\text{sampling rate for ZCD channel}} \text{seconds} \quad (3)$$

### 8.3.11 Digital Window Comparator

The internal digital window comparator (DWC) is available in both conversion modes (manual and autonomous). The DWC outputs an internal ALERT signal. The internal ALERT signal can be output on any one of the digital output channels by configuring the ALERT\_PIN register. Figure 27 provides a block diagram for the digital window comparator.

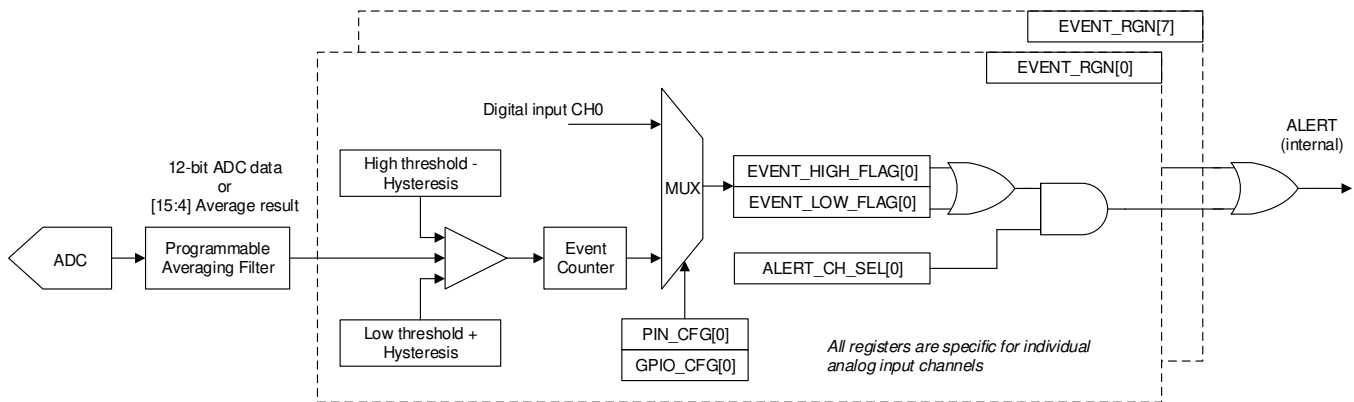
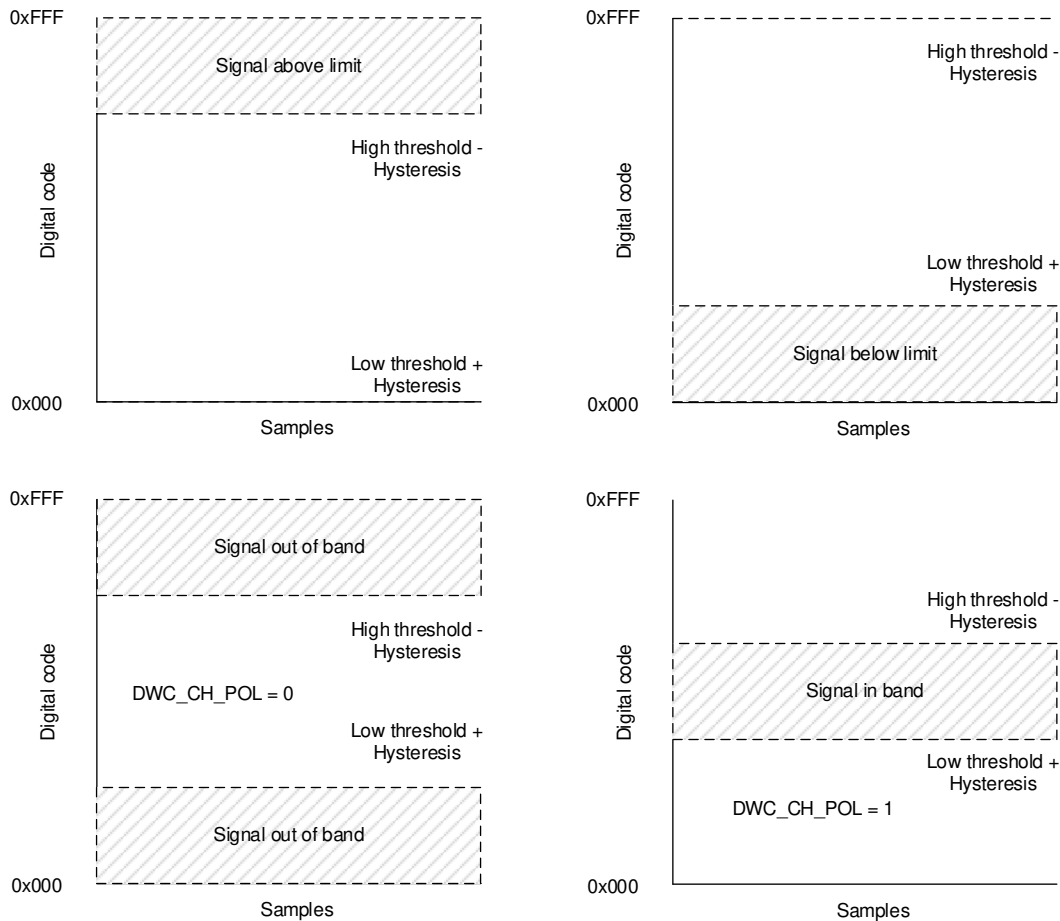


Figure 27. Digital Window Comparator Block Diagram

The low-side threshold, high-side threshold, event counter, and hysteresis parameters are independently programmable for each input channel. Figure 28 illustrates that the window comparator can monitor events for every analog input channel.



**Figure 28. Event Monitoring with the Window Comparator**

To enable the digital window comparator, set the `DWC_EN` bit in the `GENERAL_CFG` register. By default, hysteresis = 0, high threshold = 0xFFF, and low threshold = 0x000. For detecting when a signal is in-band, the `EVENT_RGN` register must be configured. In each of the cases shown in Figure 28, either or both `ALERT_HIGH_FLAG` and `ALERT_LOW_FLAG` can be set. The programmable event counter counts consecutive threshold violations before alert flags are set. The event count can be set to a higher value to avoid transients in the input signal setting the alert flags.

In order to assert the `ALERT` signal (internal) when the alert flag is set for a particular analog input channel, set the corresponding bit in the `DWC_CH_SEL` register. Alert flags are set, irrespective of the `DWC_CH_SEL` configuration, if `DWC_EN` = 1 and high or low thresholds are exceeded.

### 8.3.11.1 Interrupts from Digital Inputs

Table 5 shows that rising edge or falling edge events can be detected on channels configured as digital inputs.

**Table 5. Configuring Interrupts from Digital Inputs**

PIN_CFG[7:0]	GPIO_CFG[7:0]	EVENT_RGN[7:0]	EVENT DESCRIPTION
1	0	0	<code>ALERT_HIGH_FLAG</code> is set on the rising edge on the digital input channel
1	0	1	<code>ALERT_LOW_FLAG</code> is set on the falling edge on the digital input channel

### 8.3.11.2 Triggering Digital Outputs with Alert and ZCD

Figure 29 shows that digital outputs can be updated in response to alerts from individual channels or synchronous to the zero-crossing-detect signal.

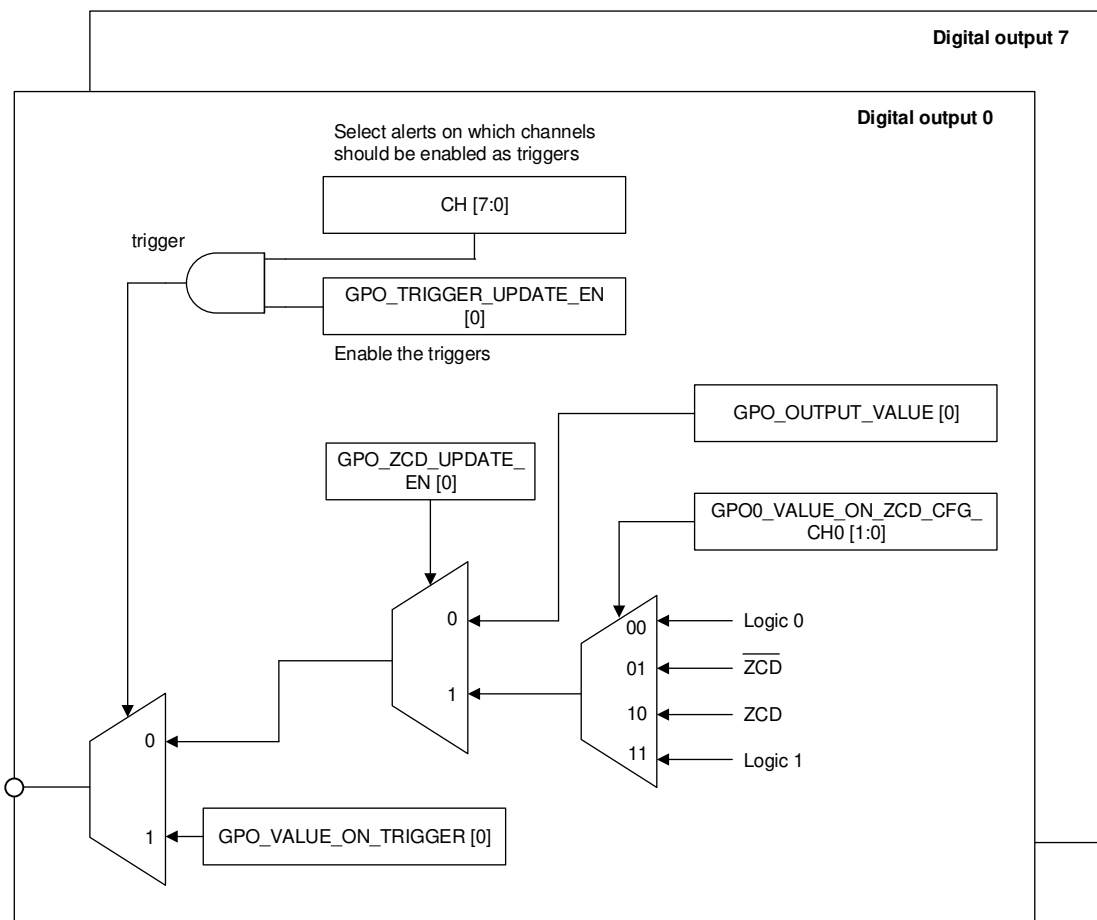


Figure 29. Block Diagram of the Digital Output Logic

#### 8.3.11.2.1 Triggering Digital Outputs on Alerts

Any given digital output can be updated in response to an alert condition on one or more analog inputs and digital inputs. To update the digital output in response to alert conditions, configure the trigger and the value to be launched when the trigger occurs.

##### 8.3.11.2.1.1 Trigger

The following events can act as triggers for updating the value on the digital output:

- An alert on one or more analog input channels. The digital window comparator must be enabled for these channels.
- An alert on one or more digital input channels. The digital window comparator must be enabled for these channels.

Configure the GPOx\_TRIG\_EVENT\_SEL register to select which channels, analog inputs, or digital inputs can trigger an update on the digital output pin. After configuring the triggers for updating a digital output, the logic can be enabled by configuring the corresponding bit in the GPO\_TRIGGER\_UPDATE\_EN register.

##### 8.3.11.2.1.2 Output Value

The digital outputs can be set to logic 1 or logic 0 in response to triggers. The value to be updated on the digital output when a trigger event occurs can be configured in the GPO\_VALUE\_ON\_TRIGGER register.

### 8.3.11.2.2 Changing Digital Outputs Synchronous to ZCD

Individual digital outputs can be set to either logic 0, logic 1, ZCD, or  $\overline{\text{ZCD}}$  synchronous to the zero-crossing-detect signal. This function can be enabled for individual digital outputs by configuring the GPO\_VALUE\_ON\_ZCD\_CFG\_CHx field and setting the corresponding bit in the GPO\_ZCD\_UPDATE\_EN [7:0] register. See the [Zero-Crossing-Detect Module](#) section for details about the operation of ZCD module and [Figure 29](#) for a block diagram detailing controlling the digital outputs with the ZCD signal.

### 8.3.12 Root-Mean-Square Module

In the ADS7028, any one analog input channel can be selected for computing the RMS result. The RMS result is computed over a block of samples from the selected channel and result can be read from the RMS\_RESULT\_LSB and RMS\_RESULT\_MSB registers. As shown in [Equation 4](#), compute the RMS result with the 16-bit square root mean of the accumulated result of the squares of the ADC conversion data.

$$\text{RMS} = \sqrt{\underbrace{\left(\frac{D_1^2 + D_2^2 + D_3^2 + \dots + D_N^2}{N}\right)}_{\text{AC component}}} - b \times \underbrace{\left(\frac{D_1 + D_2 + D_3 + \dots + D_N}{N}\right)^2}_{\text{DC component}} \text{ LSB} \quad (4)$$

In [Equation 4](#), D is the data corresponding to the analog input channel selected for RMS measurement and N is the number of samples over which RMS is computed. The DC offset must be subtracted from the AC component because the analog input signal to the ADC is unipolar. DC subtraction can be enabled or disabled, given by b in [Equation 4](#), by configuring the DC\_SUB field. When DC subtraction is enabled, the DC input voltage must be within  $\pm 5\%$  tolerance of the mid-scale voltage, for example  $(0.5 \times \text{AVDD}) \pm 5\%$ .

The size of a 1-LSB RMS result is given in [Equation 5](#) and the RMS result is 16 bits long.

$$1 \text{ LSB} = \text{AVDD} / 2^{16} \quad (5)$$

The procedure for using the RMS module is outlined in the steps below:

1. Select the channel for RMS computation using the RMS\_CHID field in the RMS\_CFG register.
2. Define the time over which RMS is to be computed by configuring the RMS\_SAMPLES field.
3. Start RMS computation by setting RMS\_EN = 1 in the GENERAL\_CFG register.
4. The RMS result is ready when the sample size defined by RMS\_SAMPLES has been converted on the analog input channel selected for RMS computation.
5. To monitor for completion of the RMS computation, poll the RMS\_DONE bit in the SYSTEM\_STATUS register. The ALERT pin can also be used for requesting an interrupt by configuring the ALERT\_RMS bit in the ALERT\_MAP register.
6. For starting a new RMS measurement, write 1 to the RMS\_EN bit in the GENERAL\_CFG register.

### 8.3.13 Minimum, Maximum, and Latest Data Registers

The ADS7028 can record the minimum, maximum, and latest code (statistics registers) for every analog input channel. To enable or re-enable recording statistics, set the STATS\_EN bit in the GENERAL\_CFG register. Writing 1 to the STATS\_EN bit reinitializes the statistics module. Afterwards, results from new conversions are recorded in the statistics registers. Previous values can be read from the statistics registers until a new conversion result is available. Before reading the statistics registers, set STATS\_EN = 0 to prevent any updates to this block of registers.

### 8.3.14 Device Programming

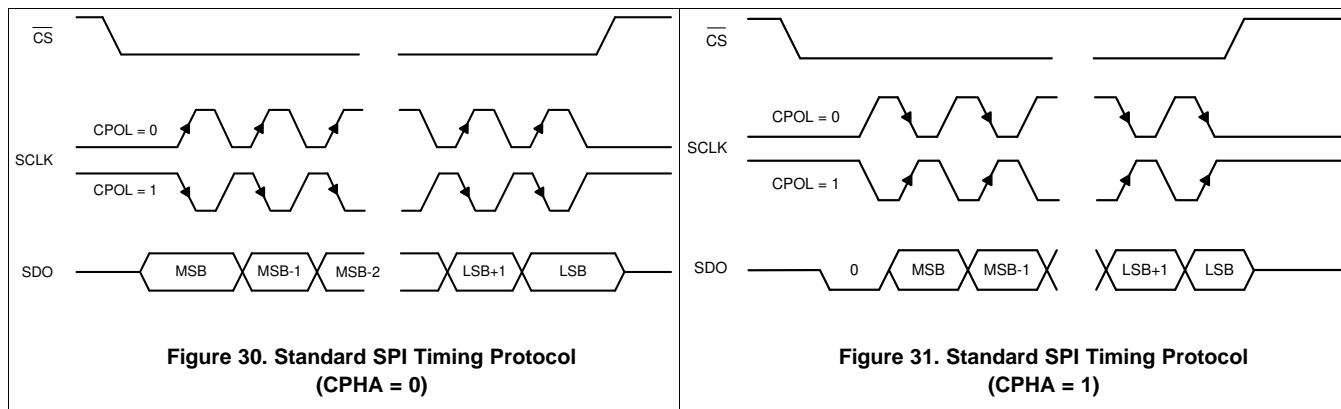
#### 8.3.14.1 Enhanced-SPI Interface

The device features an enhanced-SPI interface that allows the host controller to operate at slower SCLK speeds and still achieve full throughput. As described in Table 6, the host controller can use any of the four SPI-compatible protocols (SPI-00, SPI-01, SPI-10, or SPI-11) to access the device.

**Table 6. SPI Protocols for Configuring the Device**

PROTOCOL	SCLK POLARITY (At the $\overline{CS}$ Falling Edge)	SCLK PHASE (Capture Edge)	CPOL_CPHA[1:0]	DIAGRAM
SPI-00	Low	Rising	00b	Figure 30
SPI-01	Low	Falling	01b	Figure 31
SPI-10	High	Falling	10b	Figure 30
SPI-11	High	Rising	11b	Figure 31

On power-up or after coming out of any asynchronous reset, the device supports the SPI-00 protocol for data read and data write operations. To select a different SPI-compatible protocol, program the CPOL\_CPHA[1:0] field. This first write operation must adhere to the SPI-00 protocol. Any subsequent data transfer frames must adhere to the newly-selected protocol.



#### 8.3.14.2 Register Read/Write Operation

The device supports the commands listed in Table 7 to access the internal configuration registers.

**Table 7. Opcodes for Commands**

OPCODE	COMMAND DESCRIPTION
0000 0000b	No operation
0001 0000b	Single register read
0000 1000b	Single register write
0001 1000b	Set bit
0010 0000b	Clear bit

### 8.3.14.2.1 Register Write

A 24-bit SPI frame is required for writing data to configuration registers. The 24-bit data on SDI, as shown in Figure 32, consists of an 8-bit write command (0000 1000b), an 8-bit register address, and 8-bit data. The write command is decoded on the  $\overline{CS}$  rising edge and the specified register is updated with the 8-bit data specified during the register write operation.

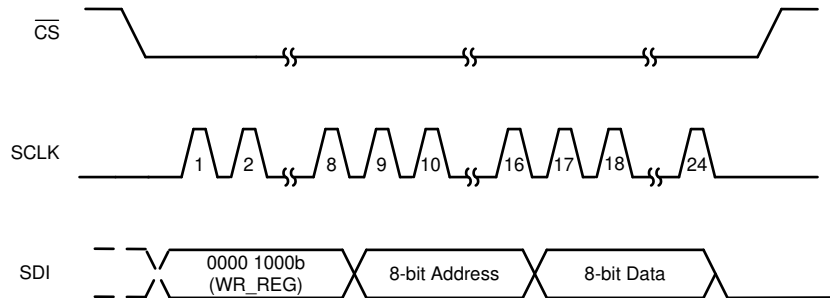


Figure 32. Register Write Operation

### 8.3.14.2.2 Register Read

Register read operation consists of two SPI frames: the first SPI frame initiates a register read and the second SPI frame reads data from the register address provided in the first frame. As shown in Figure 33, the 8-bit register address and the 8-bit dummy data are sent over the SDI pin during the first 24-bit frame with the read command (0001 0000b). On the rising edge of  $\overline{CS}$ , the read command is decoded and the requested register data are available for reading during the next frame. During the second frame, the first eight bits on SDO correspond to the requested register read. During the second frame, SDI can be used to initiate another operation or can be set to 0.

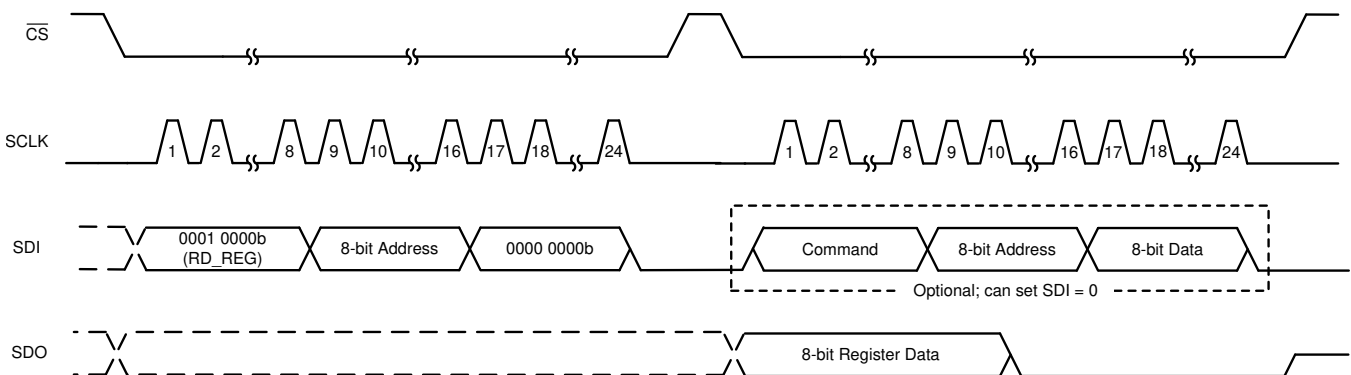


Figure 33. Register Read Operation

## 8.4 Device Functional Modes

Table 8 lists the functional modes supported by the ADS7028.

Table 8. Functional Modes

FUNCTIONAL MODE	CONVERSION CONTROL	MUX CONTROL	CONV_MODE[1:0]	SEQ_MODE[1:0]
Manual	$\overline{CS}$ rising edge	Register write to MANUAL_CHID	00b	00b
On-the-fly	$\overline{CS}$ rising edge	First 5 bits after the $\overline{CS}$ falling edge	00b	10b
Auto-sequence	$\overline{CS}$ rising edge	Channel sequencer	00b	01b
Autonomous	Internal to the device	Channel sequencer	01b	01b

The device powers up in manual mode and can be configured into either of these modes by writing the configuration registers for the desired mode.

### 8.4.1 Device Power-Up and Reset

On power-up, the BOR bit is set indicating a power-cycle or reset event. The device can be reset by setting the RST bit or by recycling the power on the AVDD pin.

### 8.4.2 Manual Mode

Manual mode allows the external host processor to directly select the analog input channel. Figure 34 shows the steps for operating the device in manual mode.

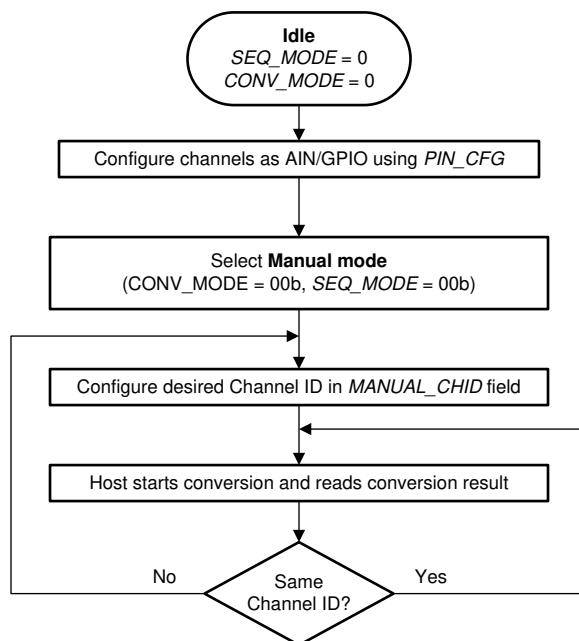


Figure 34. Device Operation in Manual Mode

In manual mode, the command to switch to a new channel (indicated by cycle N in Figure 35) is decoded by the device on the  $\overline{CS}$  rising edge. The  $\overline{CS}$  rising edge is also the start of the conversion signal, and therefore the device samples the previously selected MUX channel in cycle N+1. The newly selected analog input channel data are available in cycle N+2. For switching the analog input channel, a register write to the MANUAL\_CHID field requires 24 clocks; see the Register Write section for more details. After a channel is selected, the number of clocks required for reading the output data depends on the device output data frame size; see the Output Data Format section for more details.

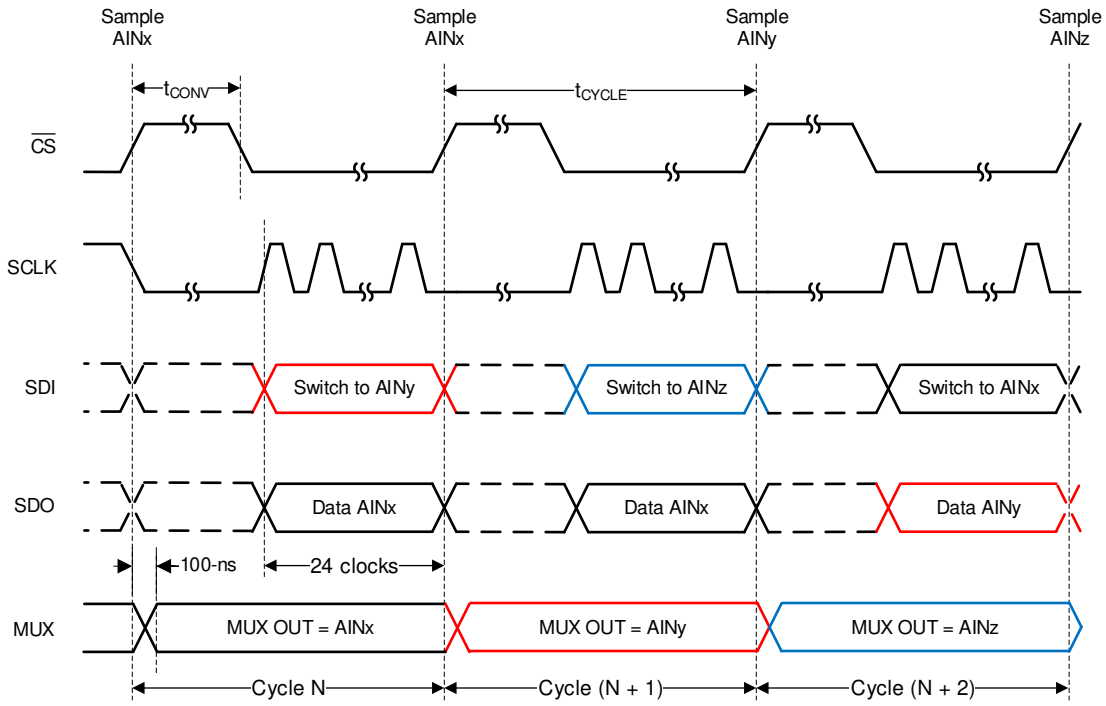


Figure 35. Starting Conversions and Reading Data in Manual Mode

### 8.4.3 On-the-Fly Mode

In the on-the-fly mode of operation, the analog input channel is selected, as shown in Figure 36, using the first five bits on SDI without waiting for the  $\overline{CS}$  rising edge. Thus, the ADC samples the newly selected channel on the  $\overline{CS}$  edge and there is no latency between the channel selection and the ADC output data.

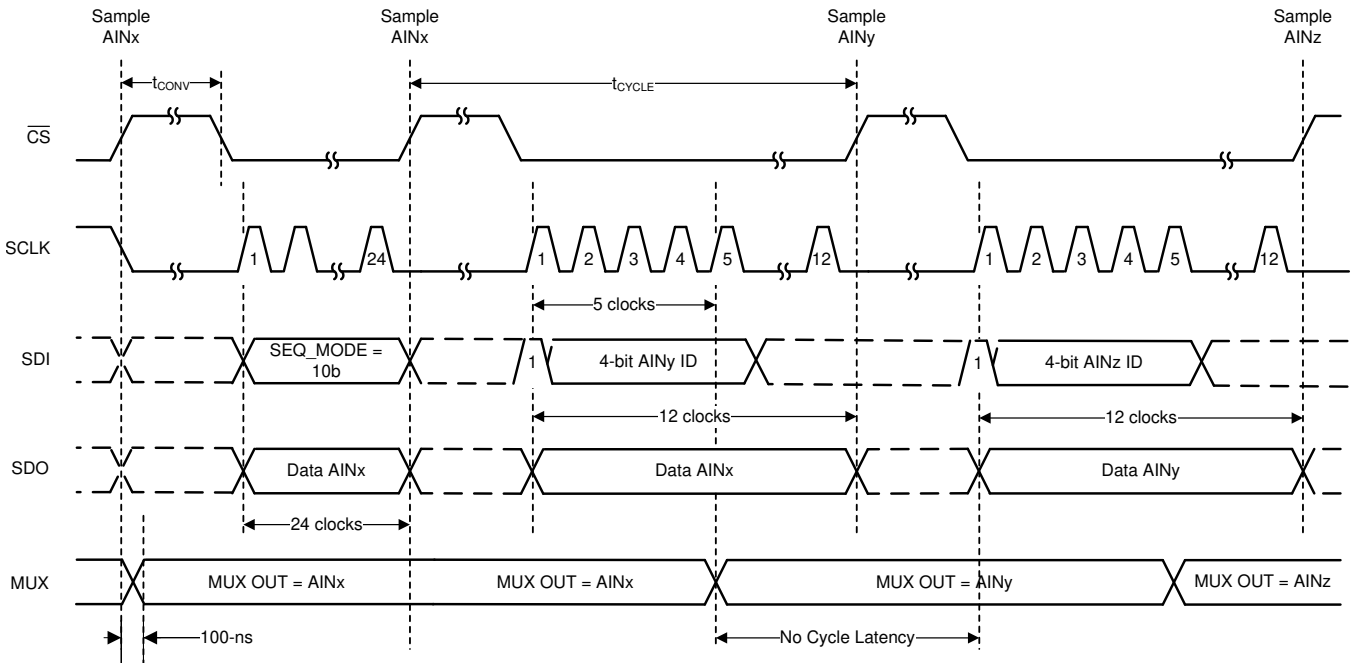


Figure 36. Starting Conversions and Reading Data in On-the-Fly Mode

The number of clocks required for reading the output data depends on the device output data frame size; see the [Output Data Format](#) section for more details.

#### 8.4.4 Auto-Sequence Mode

In auto-sequence mode, the internal channel sequencer switches the multiplexer to the next analog input channel after every conversion. The desired analog input channels can be configured for sequencing in the AUTO\_SEQ\_CHSEL register. To enable the channel sequencer, set SEQ\_START = 1b. After every conversion, the channel sequencer switches the multiplexer to the next analog input in ascending order. To stop the channel sequencer from selecting channels, set SEQ\_START = 0b.

In the example shown in [Figure 37](#), AIN2 and AIN6 are enabled for sequencing in AUTO\_SEQ\_CHSEL. The channel sequencer loops through AIN2 and AIN6 and repeats until SEQ\_START is set to 0b. The number of clocks required for reading the output data depends on the device output data frame size; see the [Output Data Format](#) section for more details.

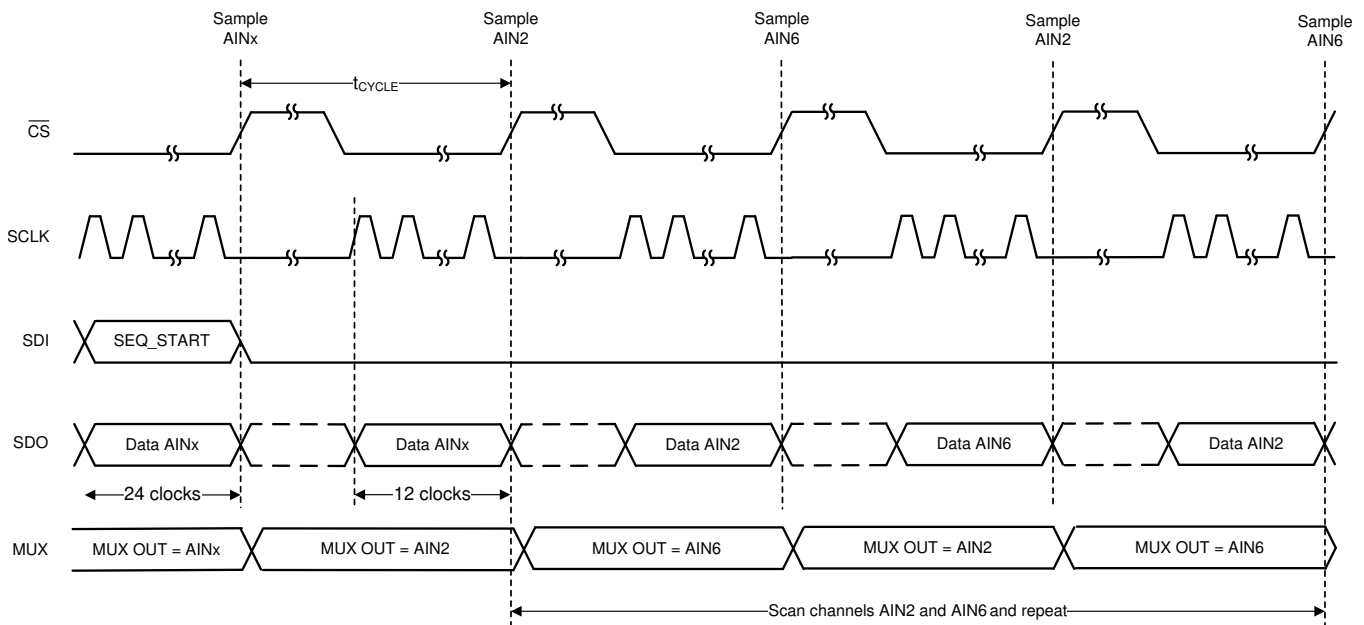


Figure 37. Starting Conversions and Reading Data in Auto-Sequence Mode

#### 8.4.5 Autonomous Mode

In autonomous mode, the device can be programmed to monitor the voltage applied on the analog input pins of the device and generate an ALERT signal internal to the device when the programmable high or low threshold values are crossed. The internal ALERT signal can be mapped to any one digital output channel by configuring the channel ID in the ALERT\_PIN[3:0] register field. In autonomous mode, the device generates the start of conversion using the internal oscillator. The first start of conversion must be provided by the host and the device generates the subsequent start of conversions.

Figure 38 shows the steps for configuring the functional mode to autonomous mode. Abort the on-going sequence by setting the SEQ\_START to 0b before changing the functional mode or configuration of device.

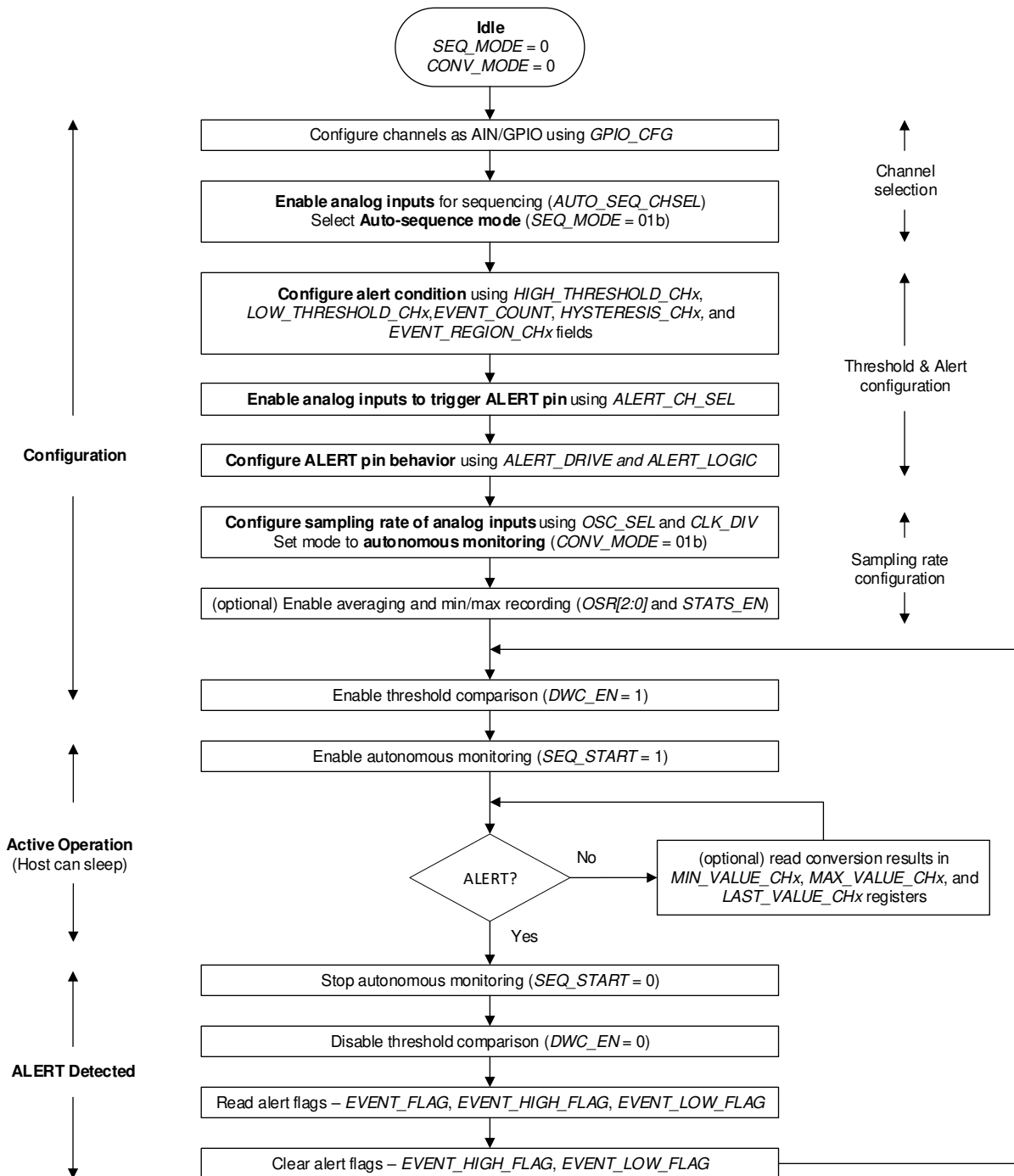


Figure 38. Configuring the Device in Autonomous Mode

## 8.5 ADS7028 Registers

Table 9 lists the ADS7028 registers. All register offset addresses not listed in Table 9 should be considered as reserved locations and the register contents should not be modified.

**Table 9. ADS7028 Registers**

Address	Acronym	Register Name	Section
0x0	SYSTEM_STATUS	SYSTEM_STATUS Register (Address = 0x0) [reset = 0x81]	
0x1	GENERAL_CFG	GENERAL_CFG Register (Address = 0x1) [reset = 0x0]	
0x2	DATA_CFG	DATA_CFG Register (Address = 0x2) [reset = 0x0]	
0x3	OSR_CFG	OSR_CFG Register (Address = 0x3) [reset = 0x0]	
0x4	OPMODE_CFG	OPMODE_CFG Register (Address = 0x4) [reset = 0x0]	
0x5	PIN_CFG	PIN_CFG Register (Address = 0x5) [reset = 0x0]	
0x7	GPIO_CFG	GPIO_CFG Register (Address = 0x7) [reset = 0x0]	
0x9	GPO_DRIVE_CFG	GPO_DRIVE_CFG Register (Address = 0x9) [reset = 0x0]	
0xB	GPO_VALUE	GPO_VALUE Register (Address = 0xB) [reset = 0x0]	
0xD	GPI_VALUE	GPI_VALUE Register (Address = 0xD) [reset = 0x0]	
0xF	ZCD_BLANKING_CFG	ZCD_BLANKING_CFG Register (Address = 0xF) [reset = 0x0]	
0x10	SEQUENCE_CFG	SEQUENCE_CFG Register (Address = 0x10) [reset = 0x0]	
0x11	CHANNEL_SEL	CHANNEL_SEL Register (Address = 0x11) [reset = 0x0]	
0x12	AUTO_SEQ_CH_SEL	AUTO_SEQ_CH_SEL Register (Address = 0x12) [reset = 0x0]	
0x14	ALERT_CH_SEL	ALERT_CH_SEL Register (Address = 0x14) [reset = 0x0]	
0x16	ALERT_MAP	ALERT_MAP Register (Address = 0x16) [reset = 0x0]	
0x17	ALERT_PIN_CFG	ALERT_PIN_CFG Register (Address = 0x17) [reset = 0x0]	
0x18	EVENT_FLAG	EVENT_FLAG Register (Address = 0x18) [reset = 0x0]	
0x1A	EVENT_HIGH_FLAG	EVENT_HIGH_FLAG Register (Address = 0x1A) [reset = 0x0]	
0x1C	EVENT_LOW_FLAG	EVENT_LOW_FLAG Register (Address = 0x1C) [reset = 0x0]	
0x1E	EVENT_RGN	EVENT_RGN Register (Address = 0x1E) [reset = 0x0]	
0x20	HYSTERESIS_CH0	HYSTERESIS_CH0 Register (Address = 0x20) [reset = 0xF0]	
0x21	HIGH_TH_CH0	HIGH_TH_CH0 Register (Address = 0x21) [reset = 0xFF]	
0x22	EVENT_COUNT_CH0	EVENT_COUNT_CH0 Register (Address = 0x22) [reset = 0x0]	
0x23	LOW_TH_CH0	LOW_TH_CH0 Register (Address = 0x23) [reset = 0x0]	
0x24	HYSTERESIS_CH1	HYSTERESIS_CH1 Register (Address = 0x24) [reset = 0xF0]	
0x25	HIGH_TH_CH1	HIGH_TH_CH1 Register (Address = 0x25) [reset = 0xFF]	
0x26	EVENT_COUNT_CH1	EVENT_COUNT_CH1 Register (Address = 0x26) [reset = 0x0]	
0x27	LOW_TH_CH1	LOW_TH_CH1 Register (Address = 0x27) [reset = 0x0]	
0x28	HYSTERESIS_CH2	HYSTERESIS_CH2 Register (Address = 0x28) [reset = 0xF0]	
0x29	HIGH_TH_CH2	HIGH_TH_CH2 Register (Address = 0x29) [reset = 0xFF]	
0x2A	EVENT_COUNT_CH2	EVENT_COUNT_CH2 Register (Address = 0x2A) [reset = 0x0]	
0x2B	LOW_TH_CH2	LOW_TH_CH2 Register (Address = 0x2B) [reset = 0x0]	
0x2C	HYSTERESIS_CH3	HYSTERESIS_CH3 Register (Address = 0x2C) [reset = 0xF0]	
0x2D	HIGH_TH_CH3	HIGH_TH_CH3 Register (Address = 0x2D) [reset = 0xFF]	
0x2E	EVENT_COUNT_CH3	EVENT_COUNT_CH3 Register (Address = 0x2E) [reset = 0x0]	
0x2F	LOW_TH_CH3	LOW_TH_CH3 Register (Address = 0x2F) [reset = 0x0]	
0x30	HYSTERESIS_CH4	HYSTERESIS_CH4 Register (Address = 0x30) [reset = 0xF0]	
0x31	HIGH_TH_CH4	HIGH_TH_CH4 Register (Address = 0x31) [reset = 0xFF]	
0x32	EVENT_COUNT_CH4	EVENT_COUNT_CH4 Register (Address = 0x32) [reset = 0x0]	
0x33	LOW_TH_CH4	LOW_TH_CH4 Register (Address = 0x33) [reset = 0x0]	
0x34	HYSTERESIS_CH5	HYSTERESIS_CH5 Register (Address = 0x34) [reset = 0xF0]	
0x35	HIGH_TH_CH5	HIGH_TH_CH5 Register (Address = 0x35) [reset = 0xFF]	

**Table 9. ADS7028 Registers (continued)**

Address	Acronym	Register Name	Section
0x36	EVENT_COUNT_CH5	EVENT_COUNT_CH5 Register (Address = 0x36) [reset = 0x0]	
0x37	LOW_TH_CH5	LOW_TH_CH5 Register (Address = 0x37) [reset = 0x0]	
0x38	HYSTERESIS_CH6	HYSTERESIS_CH6 Register (Address = 0x38) [reset = 0xF0]	
0x39	HIGH_TH_CH6	HIGH_TH_CH6 Register (Address = 0x39) [reset = 0xFF]	
0x3A	EVENT_COUNT_CH6	EVENT_COUNT_CH6 Register (Address = 0x3A) [reset = 0x0]	
0x3B	LOW_TH_CH6	LOW_TH_CH6 Register (Address = 0x3B) [reset = 0x0]	
0x3C	HYSTERESIS_CH7	HYSTERESIS_CH7 Register (Address = 0x3C) [reset = 0xF0]	
0x3D	HIGH_TH_CH7	HIGH_TH_CH7 Register (Address = 0x3D) [reset = 0xFF]	
0x3E	EVENT_COUNT_CH7	EVENT_COUNT_CH7 Register (Address = 0x3E) [reset = 0x0]	
0x3F	LOW_TH_CH7	LOW_TH_CH7 Register (Address = 0x3F) [reset = 0x0]	
0x60	MAX_CH0_LSB	MAX_CH0_LSB Register (Address = 0x60) [reset = 0x0]	
0x61	MAX_CH0_MSB	MAX_CH0_MSB Register (Address = 0x61) [reset = 0x0]	
0x62	MAX_CH1_LSB	MAX_CH1_LSB Register (Address = 0x62) [reset = 0x0]	
0x63	MAX_CH1_MSB	MAX_CH1_MSB Register (Address = 0x63) [reset = 0x0]	
0x64	MAX_CH2_LSB	MAX_CH2_LSB Register (Address = 0x64) [reset = 0x0]	
0x65	MAX_CH2_MSB	MAX_CH2_MSB Register (Address = 0x65) [reset = 0x0]	
0x66	MAX_CH3_LSB	MAX_CH3_LSB Register (Address = 0x66) [reset = 0x0]	
0x67	MAX_CH3_MSB	MAX_CH3_MSB Register (Address = 0x67) [reset = 0x0]	
0x68	MAX_CH4_LSB	MAX_CH4_LSB Register (Address = 0x68) [reset = 0x0]	
0x69	MAX_CH4_MSB	MAX_CH4_MSB Register (Address = 0x69) [reset = 0x0]	
0x6A	MAX_CH5_LSB	MAX_CH5_LSB Register (Address = 0x6A) [reset = 0x0]	
0x6B	MAX_CH5_MSB	MAX_CH5_MSB Register (Address = 0x6B) [reset = 0x0]	
0x6C	MAX_CH6_LSB	MAX_CH6_LSB Register (Address = 0x6C) [reset = 0x0]	
0x6D	MAX_CH6_MSB	MAX_CH6_MSB Register (Address = 0x6D) [reset = 0x0]	
0x6E	MAX_CH7_LSB	MAX_CH7_LSB Register (Address = 0x6E) [reset = 0x0]	
0x6F	MAX_CH7_MSB	MAX_CH7_MSB Register (Address = 0x6F) [reset = 0x0]	
0x80	MIN_CH0_LSB	MIN_CH0_LSB Register (Address = 0x80) [reset = 0xFF]	
0x81	MIN_CH0_MSB	MIN_CH0_MSB Register (Address = 0x81) [reset = 0xFF]	
0x82	MIN_CH1_LSB	MIN_CH1_LSB Register (Address = 0x82) [reset = 0xFF]	
0x83	MIN_CH1_MSB	MIN_CH1_MSB Register (Address = 0x83) [reset = 0xFF]	
0x84	MIN_CH2_LSB	MIN_CH2_LSB Register (Address = 0x84) [reset = 0xFF]	
0x85	MIN_CH2_MSB	MIN_CH2_MSB Register (Address = 0x85) [reset = 0xFF]	
0x86	MIN_CH3_LSB	MIN_CH3_LSB Register (Address = 0x86) [reset = 0xFF]	
0x87	MIN_CH3_MSB	MIN_CH3_MSB Register (Address = 0x87) [reset = 0xFF]	
0x88	MIN_CH4_LSB	MIN_CH4_LSB Register (Address = 0x88) [reset = 0xFF]	
0x89	MIN_CH4_MSB	MIN_CH4_MSB Register (Address = 0x89) [reset = 0xFF]	
0x8A	MIN_CH5_LSB	MIN_CH5_LSB Register (Address = 0x8A) [reset = 0xFF]	
0x8B	MIN_CH5_MSB	MIN_CH5_MSB Register (Address = 0x8B) [reset = 0xFF]	
0x8C	MIN_CH6_LSB	MIN_CH6_LSB Register (Address = 0x8C) [reset = 0xFF]	
0x8D	MIN_CH6_MSB	MIN_CH6_MSB Register (Address = 0x8D) [reset = 0xFF]	
0x8E	MIN_CH7_LSB	MIN_CH7_LSB Register (Address = 0x8E) [reset = 0xFF]	
0x8F	MIN_CH7_MSB	MIN_CH7_MSB Register (Address = 0x8F) [reset = 0xFF]	
0xA0	RECENT_CH0_LSB	RECENT_CH0_LSB Register (Address = 0xA0) [reset = 0x0]	
0xA1	RECENT_CH0_MSB	RECENT_CH0_MSB Register (Address = 0xA1) [reset = 0x0]	
0xA2	RECENT_CH1_LSB	RECENT_CH1_LSB Register (Address = 0xA2) [reset = 0x0]	
0xA3	RECENT_CH1_MSB	RECENT_CH1_MSB Register (Address = 0xA3) [reset = 0x0]	
0xA4	RECENT_CH2_LSB	RECENT_CH2_LSB Register (Address = 0xA4) [reset = 0x0]	

**Table 9. ADS7028 Registers (continued)**

Address	Acronym	Register Name	Section
0xA5	RECENT_CH2_MSB	RECENT_CH2_MSB Register (Address = 0xA5) [reset = 0x0]	
0xA6	RECENT_CH3_LSB	RECENT_CH3_LSB Register (Address = 0xA6) [reset = 0x0]	
0xA7	RECENT_CH3_MSB	RECENT_CH3_MSB Register (Address = 0xA7) [reset = 0x0]	
0xA8	RECENT_CH4_LSB	RECENT_CH4_LSB Register (Address = 0xA8) [reset = 0x0]	
0xA9	RECENT_CH4_MSB	RECENT_CH4_MSB Register (Address = 0xA9) [reset = 0x0]	
0xAA	RECENT_CH5_LSB	RECENT_CH5_LSB Register (Address = 0xAA) [reset = 0x0]	
0xAB	RECENT_CH5_MSB	RECENT_CH5_MSB Register (Address = 0xAB) [reset = 0x0]	
0xAC	RECENT_CH6_LSB	RECENT_CH6_LSB Register (Address = 0xAC) [reset = 0x0]	
0xAD	RECENT_CH6_MSB	RECENT_CH6_MSB Register (Address = 0xAD) [reset = 0x0]	
0xAE	RECENT_CH7_LSB	RECENT_CH7_LSB Register (Address = 0xAE) [reset = 0x0]	
0xAF	RECENT_CH7_MSB	RECENT_CH7_MSB Register (Address = 0xAF) [reset = 0x0]	
0xC0	RMS_CFG	RMS_CFG Register (Address = 0xC0) [reset = 0x0]	
0xC1	RMS_LSB	RMS_LSB Register (Address = 0xC1) [reset = 0x0]	
0xC2	RMS_MSB	RMS_MSB Register (Address = 0xC2) [reset = 0x0]	
0xC3	GPO0_TRIG_EVENT_SEL	GPO0_TRIG_EVENT_SEL Register (Address = 0xC3) [reset = 0x2]	
0xC5	GPO1_TRIG_EVENT_SEL	GPO1_TRIG_EVENT_SEL Register (Address = 0xC5) [reset = 0x1]	
0xC7	GPO2_TRIG_EVENT_SEL	GPO2_TRIG_EVENT_SEL Register (Address = 0xC7) [reset = 0x8]	
0xC9	GPO3_TRIG_EVENT_SEL	GPO3_TRIG_EVENT_SEL Register (Address = 0xC9) [reset = 0x4]	
0xCB	GPO4_TRIG_EVENT_SEL	GPO4_TRIG_EVENT_SEL Register (Address = 0xCB) [reset = 0x20]	
0xCD	GPO5_TRIG_EVENT_SEL	GPO5_TRIG_EVENT_SEL Register (Address = 0xCD) [reset = 0x10]	
0xCF	GPO6_TRIG_EVENT_SEL	GPO6_TRIG_EVENT_SEL Register (Address = 0xCF) [reset = 0x80]	
0xD1	GPO7_TRIG_EVENT_SEL	GPO7_TRIG_EVENT_SEL Register (Address = 0xD1) [reset = 0x40]	
0xE3	GPO_VALUE_ZCD_CFG_CH0_CH3	GPO_VALUE_ZCD_CFG_CH0_CH3 Register (Address = 0xE3) [reset = 0x0]	
0xE4	GPO_VALUE_ZCD_CFG_CH4_CH7	GPO_VALUE_ZCD_CFG_CH4_CH7 Register (Address = 0xE4) [reset = 0x0]	
0xE7	GPO_ZCD_UPDATE_EN	GPO_ZCD_UPDATE_EN Register (Address = 0xE7) [reset = 0x0]	
0xE9	GPO_TRIGGER_CFG	GPO_TRIGGER_CFG Register (Address = 0xE9) [reset = 0x0]	
0xEB	GPO_VALUE_TRIG	GPO_VALUE_TRIG Register (Address = 0xEB) [reset = 0x0]	

Complex bit access types are encoded to fit into small table cells. [Table 10](#) shows the codes that are used for access types in this section.

**Table 10. ADS7028 Access Type Codes**

Access Type	Code	Description
<b>Read Type</b>		
R	R	Read
<b>Write Type</b>		
W	W	Write
<b>Reset or Default Value</b>		
-n		Value after reset or the default value
<b>Register Array Variables</b>		

**Table 10. ADS7028 Access Type Codes (continued)**

Access Type	Code	Description
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

**8.5.1 SYSTEM\_STATUS Register (Address = 0x0) [reset = 0x81]**

SYSTEM\_STATUS is shown in [Figure 39](#) and described in [Table 11](#).

Return to the [Summary Table](#).

**Figure 39. SYSTEM\_STATUS Register**

7	6	5	4	3	2	1	0
RSVD	SEQ_STATUS	RESERVED	RMS_DONE	OSR_DONE	CRC_ERR_FUSE	CRC_ERR_IN	BOR
R-1b	R-0b	R-0b	R/W-0b	R/W-0b	R-0b	R/W-0b	R/W-1b

**Table 11. SYSTEM\_STATUS Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	RSVD	R	1b	Reads return 1b.
6	SEQ_STATUS	R	0b	Status of the channel sequencer. 0b = Sequence stopped. 1b = Sequence in progress.
5	RESERVED	R	0b	Reserved. Reads return 0.
4	RMS_DONE	R/W	0b	RMS computation status. Clear this bit by writing 1b to this bit. 0b = RMS operation in progress or not started; RMS result not ready. 1b = RMS computation complete; RMS result ready.
3	OSR_DONE	R/W	0b	Averaging status. Clear this bit by writing 1b to this bit. 0b = Averaging in progress or not started; average result is not ready. 1b = Averaging complete; average result is ready.
2	CRC_ERR_FUSE	R	0b	Device power-up configuration CRC check status. To re-evaluate this bit, software reset the device or power cycle AVDD. 0b = No problems detected in power-up configuration. 1b = Device configuration not loaded correctly.
1	CRC_ERR_IN	R/W	0b	Status of CRC check on incoming data. Write 1b to clear this error flag. 0b = No CRC error. 1b = CRC error detected. All register writes, except to addresses 0x00 and 0x01, are blocked.
0	BOR	R/W	1b	Brown out reset indicator. This bit is set if brown out condition occurs or device is power cycled. Write 1b to this bit to clear the flag. 0b = No brown out from the last time this bit was cleared. 1b = Brown out condition detected or device power cycled.

### 8.5.2 GENERAL\_CFG Register (Address = 0x1) [reset = 0x0]

GENERAL\_CFG is shown in [Figure 40](#) and described in [Table 12](#).

Return to the [Summary Table](#).

**Figure 40. GENERAL\_CFG Register**

7	6	5	4	3	2	1	0
RMS_EN	CRC_EN	STATS_EN	DWC_EN	RESERVED	CH_RST	CAL	RST
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R-0b	R/W-0b	R/W-0b	W-0b

**Table 12. GENERAL\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	RMS_EN	R/W	0b	Enable or disable the RMS module. 0b = RMS module disabled. 1b = RMS module enabled; writing 1b to this bit clears RMS_RESULT registers and initiates new RMS computation.
6	CRC_EN	R/W	0b	Enable or disable CRC on device interface. 0b = CRC module disabled. 1b = CRC appended to data output. CRC check is enabled on incoming data.
5	STATS_EN	R/W	0b	Enable or disable the statistics module to update minimum, maximum, and latest output code registers. 0b = Statistics registers are not updated. 1b = Clear statistics registers and continue updating with new conversion results.
4	DWC_EN	R/W	0b	Enable or disable the digital window comparator. 0b = Reset or disable digital window comparator. 1b = Enable digital window comparator.
3	RESERVED	R	0b	Reserved. Reads return 0.
2	CH_RST	R/W	0b	Force all channels to be analog inputs. 0b = Normal operation. 1b = All channels are set as analog inputs irrespective of configuration in other registers.
1	CAL	R/W	0b	Calibrate ADC offset. 0b = Normal operation. 1b = ADC offset is calibrated. After calibration is complete, this bit is set to 0b.
0	RST	W	0b	Software reset all registers to default values. 0b = Normal operation. 1b = Device is reset. After reset is complete, this bit is set to 0b and BOR bit is set to 1b.

### 8.5.3 DATA\_CFG Register (Address = 0x2) [reset = 0x0]

DATA\_CFG is shown in [Figure 41](#) and described in [Table 13](#).

Return to the [Summary Table](#).

**Figure 41. DATA\_CFG Register**

7	6	5	4	3	2	1	0
FIX_PAT	RESERVED	APPEND_STATUS[1:0]		RESERVED	CPOL_CPHA[1:0]		
R/W-0b	R-0b	R/W-0b		R-0b	R/W-0b		

**Table 13. DATA\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	FIX_PAT	R/W	0b	Device outputs fixed data bits, which can be helpful for debugging communication with the device. 0b = Normal operation. 1b = Device outputs fixed code 0xA5A repetitively when reading ADC data.
6	RESERVED	R	0b	Reserved. Reads return 0.
5-4	APPEND_STATUS[1:0]	R/W	0b	Append 4-bit channel ID or status flags to output data. 0b = Channel ID and status flags are not appended to ADC data. 1b = 4-bit channel ID is appended to ADC data. 10b = 4-bit status flags are appended to ADC data. 11b = Reserved.
3-2	RESERVED	R	0b	Reserved. Reads return 0.
1-0	CPOL_CPHA[1:0]	R/W	0b	This field sets the polarity and phase of SPI communication. 0b = CPOL = 0, CPHA = 0. 1b = CPOL = 0, CPHA = 1. 10b = CPOL = 1, CPHA = 0. 11b = CPOL = 1, CPHA = 1.

**8.5.4 OSR\_CFG Register (Address = 0x3) [reset = 0x0]**

OSR\_CFG is shown in [Figure 42](#) and described in [Table 14](#).

Return to the [Summary Table](#).

**Figure 42. OSR\_CFG Register**

7	6	5	4	3	2	1	0
RESERVED					OSR[2:0]		
R-0b					R/W-0b		

**Table 14. OSR\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0b	Reserved. Reads return 0.
2-0	OSR[2:0]	R/W	0b	Selects the number of ADC output samples to average. 0b = No averaging 1b = 2 samples 10b = 4 samples 11b = 8 samples 100b = 16 samples 101b = 32 samples 110b = 64 samples 111b = 128 samples

**8.5.5 OPMODE\_CFG Register (Address = 0x4) [reset = 0x0]**

OPMODE\_CFG is shown in [Figure 43](#) and described in [Table 15](#).

Return to the [Summary Table](#).

**Figure 43. OPMODE\_CFG Register**

7	6	5	4	3	2	1	0
CONV_ON_ER R	CONV_MODE[1:0]		OSC_SEL	CLK_DIV[3:0]			
R/W-0b	R/W-0b		R/W-0b	R/W-0b			

**Table 15. OPMODE\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	CONV_ON_ERR	R/W	0b	Control continuation of autonomous modes if CRC error is detected on communication interface. 0b = If CRC error is detected, device continues channel sequencing and pin configuration is retained. See the CRC_ERR_IN bit for more details. 1b = If CRC error is detected, device changes all channels to analog inputs and channel sequencing is paused until CRC_ERR_IN bit is set to 0b. After clearing CRC_ERR_IN flag, device resumes channel sequencing and pin configuration is restored.
6-5	CONV_MODE[1:0]	R/W	0b	These bits set the mode of conversion of the ADC. 0b = Manual mode; conversions are initiated by the host. 1b = Autonomous mode; conversions are initiated by the internal state machine.
4	OSC_SEL	R/W	0b	Selects the oscillator for internal timing generation. 0b = High-speed oscillator. 1b = Low-power oscillator.
3-0	CLK_DIV[3:0]	R/W	0b	Sampling speed control in autonomous monitoring mode (CONV_MODE = 01b). See the section on oscillator and timing control for details.

### 8.5.6 PIN\_CFG Register (Address = 0x5) [reset = 0x0]

PIN\_CFG is shown in [Figure 44](#) and described in [Table 16](#).

Return to the [Summary Table](#).

**Figure 44. PIN\_CFG Register**

7	6	5	4	3	2	1	0
PIN_CFG[7:0]							
R/W-0b							

**Table 16. PIN\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	PIN_CFG[7:0]	R/W	0b	Configure device channels AIN / GPIO [7:0] as analog inputs or GPIOs. 0b = Channel is configured as analog input. 1b = Channel is configured as GPIO.

### 8.5.7 GPIO\_CFG Register (Address = 0x7) [reset = 0x0]

GPIO\_CFG is shown in [Figure 45](#) and described in [Table 17](#).

Return to the [Summary Table](#).

**Figure 45. GPIO\_CFG Register**

7	6	5	4	3	2	1	0
GPIO_CFG[7:0]							
R/W-0b							

**Table 17. GPIO\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPIO_CFG[7:0]	R/W	0b	Configure GPIO[7:0] as either digital inputs or digital outputs. 0b = GPIO is configured as digital input. 1b = GPIO is configured as digital output.

### 8.5.8 GPO\_DRIVE\_CFG Register (Address = 0x9) [reset = 0x0]

GPO\_DRIVE\_CFG is shown in [Figure 46](#) and described in [Table 18](#).

Return to the [Summary Table](#).

**Figure 46. GPO\_DRIVE\_CFG Register**

7	6	5	4	3	2	1	0
GPO_DRIVE_CFG[7:0]							
R/W-0b							

**Table 18. GPO\_DRIVE\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO_DRIVE_CFG[7:0]	R/W	0b	Configure digital outputs GPO[7:0] as open-drain or push-pull outputs. 0b = Digital output is open-drain; connect external pullup resistor. 1b = Push-pull driver is used for digital output.

### 8.5.9 GPO\_VALUE Register (Address = 0xB) [reset = 0x0]

GPO\_VALUE is shown in [Figure 47](#) and described in [Table 19](#).

Return to the [Summary Table](#).

**Figure 47. GPO\_VALUE Register**

7	6	5	4	3	2	1	0
GPO_VALUE[7:0]							
R/W-0b							

**Table 19. GPO\_VALUE Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO_VALUE[7:0]	R/W	0b	Logic level to be set on digital outputs GPO[7:0]. 0b = Digital output set to logic 0. 1b = Digital output set to logic 1.

### 8.5.10 GPI\_VALUE Register (Address = 0xD) [reset = 0x0]

GPI\_VALUE is shown in [Figure 48](#) and described in [Table 20](#).

Return to the [Summary Table](#).

**Figure 48. GPI\_VALUE Register**

7	6	5	4	3	2	1	0
GPI_VALUE[7:0]							
R-0b							

**Table 20. GPI\_VALUE Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPI_VALUE[7:0]	R	0b	Readback the logic level on GPIO[7:0]. 0b = GPIO is at logic 0. 1b = GPIO is at logic 1.

### 8.5.11 ZCD\_BLANKING\_CFG Register (Address = 0xF) [reset = 0x0]

ZCD\_BLANKING\_CFG is shown in [Figure 49](#) and described in [Table 21](#).

Return to the [Summary Table](#).

**Figure 49. ZCD\_BLANKING\_CFG Register**

7	6	5	4	3	2	1	0
MULT_EN		ZCD_BLANKING[6:0]					
R/W-0b		R/W-0b					

**Table 21. ZCD\_BLANKING\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	MULT_EN	R/W	0b	Multiplier enable bit for the ZCD_BLANKING field. 0b = Blanking count = ZCD_BLANKING 1b = Blanking count = ZCD_BLANKING x 8
6-0	ZCD_BLANKING[6:0]	R/W	0b	This field defines the number of analog conversions, of the ZCD channel, which must be ignored before generating next ZCD event. The counting starts from ZCD event detection.

### 8.5.12 SEQUENCE\_CFG Register (Address = 0x10) [reset = 0x0]

SEQUENCE\_CFG is shown in [Figure 50](#) and described in [Table 22](#).

Return to the [Summary Table](#).

**Figure 50. SEQUENCE\_CFG Register**

7	6	5	4	3	2	1	0
RESERVED			SEQ_START	RESERVED		SEQ_MODE[1:0]	
R-0b			R/W-0b	R-0b		R/W-0b	

**Table 22. SEQUENCE\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0b	Reserved. Reads return 0.
4	SEQ_START	R/W	0b	Control for start of channel sequence when using channel sequencer (SEQ_MODE = 01b). 0b = Stop channel sequencing. 1b = Start channel sequencing in ascending order for channels enabled in AUTO_SEQ_CHSEL register.
3-2	RESERVED	R	0b	Reserved. Reads return 0.
1-0	SEQ_MODE[1:0]	R/W	0b	Selects the mode of scanning of analog input channels. 0b = Manual sequence mode; channel selected by MANUAL_CHID field. 1b = Auto sequence mode; channel selected by internal channel sequencer. 10b = On-the-fly sequence mode. 11b = Reserved.

### 8.5.13 CHANNEL\_SEL Register (Address = 0x11) [reset = 0x0]

CHANNEL\_SEL is shown in [Figure 51](#) and described in [Table 23](#).

Return to the [Summary Table](#).

**Figure 51. CHANNEL\_SEL Register**

7	6	5	4	3	2	1	0
ZCD_CHID[3:0]				MANUAL_CHID[3:0]			
R/W-0b				R/W-0b			

**Table 23. CHANNEL\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	ZCD_CHID[3:0]	R/W	0b	Input channel to treat as ZCD input. If the selected channel is configured as an analog input, internally generated ZCD signal is used (setup thresholds accordingly). If the selected channel is a digital input, the digital signal on this channel is directly used as ZCD signal.
3-0	MANUAL_CHID[3:0]	R/W	0b	In manual mode (SEQ_MODE = 00b), this field contains the 4-bit channel ID of the analog input channel for next ADC conversion. For valid ADC data, the selected channel must not be configured as GPIO in PIN_CFG register. 0b = AIN0 1b = AIN1 10b = AIN2 11b = AIN3 100b = AIN4 101b = AIN5 110b = AIN6 111b = AIN7 1000b = Reserved.

**8.5.14 AUTO\_SEQ\_CH\_SEL Register (Address = 0x12) [reset = 0x0]**

AUTO\_SEQ\_CH\_SEL is shown in [Figure 52](#) and described in [Table 24](#).

Return to the [Summary Table](#).

**Figure 52. AUTO\_SEQ\_CH\_SEL Register**

7	6	5	4	3	2	1	0
AUTO_SEQ_CH_SEL[7:0]							
R/W-0b							

**Table 24. AUTO\_SEQ\_CH\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	AUTO_SEQ_CH_SEL[7:0]	R/W	0b	Select analog input channels AIN[7:0] in for auto sequencing mode. 0b = Analog input channel is not enabled in scanning sequence. 1b = Analog input channel is enabled in scanning sequence.

**8.5.15 ALERT\_CH\_SEL Register (Address = 0x14) [reset = 0x0]**

ALERT\_CH\_SEL is shown in [Figure 53](#) and described in [Table 25](#).

Return to the [Summary Table](#).

**Figure 53. ALERT\_CH\_SEL Register**

7	6	5	4	3	2	1	0
ALERT_CH_SEL[7:0]							
R/W-0b							

**Table 25. ALERT\_CH\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	ALERT_CH_SEL[7:0]	R/W	0b	Select channels for which the alert flags can assert the ALERT signal. 0b = Alert flags for this channel do not assert the ALERT signal. 1b = Alert flags for this channel assert the ALERT signal.

### 8.5.16 ALERT\_MAP Register (Address = 0x16) [reset = 0x0]

ALERT\_MAP is shown in [Figure 54](#) and described in [Table 26](#).

Return to the [Summary Table](#).

**Figure 54. ALERT\_MAP Register**

7	6	5	4	3	2	1	0
RESERVED						ALERT_RMS	ALERT_CRCIN
R-0b						R/W-0b	R/W-0b

**Table 26. ALERT\_MAP Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0b	Reserved. Reads return 0.
1	ALERT_RMS	R/W	0b	Enable or disable asserting ALERT signal based on RMS computation status (RMS_DONE = 1b). 0b = ALERT signal is not asserted when RMS_DONE = 1b. 1b = ALERT signal is asserted when RMS_DONE = 1b. Clear RMS_DONE flag to deassert the ALERT signal.
0	ALERT_CRCIN	R/W	0b	Enable or disable the alert notification for CRC error on input data (CRCERR_IN = 1b). 0b = ALERT signal is not asserted when CRCERR_IN = 1b. 1b = ALERT signal is asserted when CRCERR_IN = 1b. Clear CRCERR_IN for deasserting the ALERT signal.

### 8.5.17 ALERT\_PIN\_CFG Register (Address = 0x17) [reset = 0x0]

ALERT\_PIN\_CFG is shown in [Figure 55](#) and described in [Table 27](#).

Return to the [Summary Table](#).

**Figure 55. ALERT\_PIN\_CFG Register**

7	6	5	4	3	2	1	0
ALERT_PIN[3:0]				RESERVED		ALERT_LOGIC[1:0]	
R/W-0b				R-0b		R/W-0b	

**Table 27. ALERT\_PIN\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	ALERT_PIN[3:0]	R/W	0b	Internal ALERT output of the digital window comparator will be output on this channel. This channel must be configured as digital output.
3-2	RESERVED	R	0b	Reserved. Reads return 0.
1-0	ALERT_LOGIC[1:0]	R/W	0b	Configure how ALERT signal is asserted. 0b = Active low. 1b = Active high. 10b = Pulsed low (one logic low pulse once per alert flag). 11b = Pulsed high (one logic high pulse once per alert flag).

### 8.5.18 EVENT\_FLAG Register (Address = 0x18) [reset = 0x0]

EVENT\_FLAG is shown in [Figure 56](#) and described in [Table 28](#).

Return to the [Summary Table](#).

**Figure 56. EVENT\_FLAG Register**

7	6	5	4	3	2	1	0
EVENT_FLAG[7:0]							
R-0b							

**Table 28. EVENT\_FLAG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	EVENT_FLAG[7:0]	R	0b	Alert flags indicating digital window comparator status for AIN/GPIO[7:0]. Clear individual bits of EVENT_HIGH_FLAG or EVENT_LOW_FLAG registers to clear the corresponding alert flag. 0b = Event condition not detected. 1b = Event condition detected.

### 8.5.19 EVENT\_HIGH\_FLAG Register (Address = 0x1A) [reset = 0x0]

EVENT\_HIGH\_FLAG is shown in [Figure 57](#) and described in [Table 29](#).

Return to the [Summary Table](#).

**Figure 57. EVENT\_HIGH\_FLAG Register**

7	6	5	4	3	2	1	0
EVENT_HIGH_FLAG[7:0]							
R/W-0b							

**Table 29. EVENT\_HIGH\_FLAG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	EVENT_HIGH_FLAG[7:0]	R/W	0b	Alert flag corresponding to high threshold of analog input or rising edge of digital input on CH[7:0]. Write 1b to clear this flag. 0b = No alert condition detected. 1b = Either high threshold was exceeded (analog input) or rising edge was detected (digital input).

### 8.5.20 EVENT\_LOW\_FLAG Register (Address = 0x1C) [reset = 0x0]

EVENT\_LOW\_FLAG is shown in [Figure 58](#) and described in [Table 30](#).

Return to the [Summary Table](#).

**Figure 58. EVENT\_LOW\_FLAG Register**

7	6	5	4	3	2	1	0
EVENT_LOW_FLAG[7:0]							
R/W-0b							

**Table 30. EVENT\_LOW\_FLAG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	EVENT_LOW_FLAG[7:0]	R/W	0b	Alert flag corresponding to low threshold of analog input or falling edge of digital input on CH[7:0]. Write 1b to clear this flag. 0b = No Event condition detected. 1b = Either low threshold was exceeded (analog input) or falling edge was detected (digital input).

### 8.5.21 EVENT\_RGN Register (Address = 0x1E) [reset = 0x0]

EVENT\_RGN is shown in [Figure 59](#) and described in [Table 31](#).

Return to the [Summary Table](#).

**Figure 59. EVENT\_RGN Register**

7	6	5	4	3	2	1	0
EVENT_RGN[7:0]							
R/W-0b							

**Table 31. EVENT\_RGN Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	EVENT_RGN[7:0]	R/W	0b	Choice of region used in monitoring analog/digital inputs CH[7:0]. 0b = Alert flag is set if: (conversion result andlt low threshold) or (conversion result andgt high threshold). For digital inputs, rising edge sets the alert flag. 1b = Alert flag is set if: (low threshold andgt conversion result andlt high threshold). For digital inputs, falling edge sets the alert flag.

### 8.5.22 HYSTERESIS\_CH0 Register (Address = 0x20) [reset = 0xF0]

HYSTERESIS\_CH0 is shown in [Figure 60](#) and described in [Table 32](#).

Return to the [Summary Table](#).

**Figure 60. HYSTERESIS\_CH0 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH0_LSB[3:0]				HYSTERESIS_CH0[3:0]			
R/W-1111b				R/W-0b			

**Table 32. HYSTERESIS\_CH0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH0_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH0[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteresis is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

### 8.5.23 HIGH\_TH\_CH0 Register (Address = 0x21) [reset = 0xFF]

HIGH\_TH\_CH0 is shown in [Figure 61](#) and described in [Table 33](#).

Return to the [Summary Table](#).

**Figure 61. HIGH\_TH\_CH0 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH0_MSB[7:0]							
R/W-11111111b							

**Table 33. HIGH\_TH\_CH0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH0_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

### 8.5.24 EVENT\_COUNT\_CH0 Register (Address = 0x22) [reset = 0x0]

EVENT\_COUNT\_CH0 is shown in [Figure 62](#) and described in [Table 34](#).

Return to the [Summary Table](#).

**Figure 62. EVENT\_COUNT\_CH0 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH0_LSB[3:0]				EVENT_COUNT_CH0[3:0]			
R/W-0b				R/W-0b			

**Table 34. EVENT\_COUNT\_CH0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH0_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH0[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples exceeding either high or low threshold before setting alert flag.

**8.5.25 LOW\_TH\_CH0 Register (Address = 0x23) [reset = 0x0]**

LOW\_TH\_CH0 is shown in [Figure 63](#) and described in [Table 35](#).

Return to the [Summary Table](#).

**Figure 63. LOW\_TH\_CH0 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH0_MSB[7:0]							
R/W-0b							

**Table 35. LOW\_TH\_CH0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH0_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.5.26 HYSTERESIS\_CH1 Register (Address = 0x24) [reset = 0xF0]**

HYSTERESIS\_CH1 is shown in [Figure 64](#) and described in [Table 36](#).

Return to the [Summary Table](#).

**Figure 64. HYSTERESIS\_CH1 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH1_LSB[3:0]				HYSTERESIS_CH1[3:0]			
R/W-1111b				R/W-0b			

**Table 36. HYSTERESIS\_CH1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH1_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH1[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteresis is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

**8.5.27 HIGH\_TH\_CH1 Register (Address = 0x25) [reset = 0xFF]**

HIGH\_TH\_CH1 is shown in [Figure 65](#) and described in [Table 37](#).

Return to the [Summary Table](#).

**Figure 65. HIGH\_TH\_CH1 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH1_MSB[7:0]							
R/W-11111111b							

**Table 37. HIGH\_TH\_CH1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH1_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

### 8.5.28 EVENT\_COUNT\_CH1 Register (Address = 0x26) [reset = 0x0]

EVENT\_COUNT\_CH1 is shown in [Figure 66](#) and described in [Table 38](#).

Return to the [Summary Table](#).

**Figure 66. EVENT\_COUNT\_CH1 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH1_LSB[3:0]				EVENT_COUNT_CH1[3:0]			
R/W-0b				R/W-0b			

**Table 38. EVENT\_COUNT\_CH1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH1_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH1[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples exceeding either high or low threshold before setting alert flag.

### 8.5.29 LOW\_TH\_CH1 Register (Address = 0x27) [reset = 0x0]

LOW\_TH\_CH1 is shown in [Figure 67](#) and described in [Table 39](#).

Return to the [Summary Table](#).

**Figure 67. LOW\_TH\_CH1 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH1_MSB[7:0]							
R/W-0b							

**Table 39. LOW\_TH\_CH1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH1_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

### 8.5.30 HYSTERESIS\_CH2 Register (Address = 0x28) [reset = 0xF0]

HYSTERESIS\_CH2 is shown in [Figure 68](#) and described in [Table 40](#).

Return to the [Summary Table](#).

**Figure 68. HYSTERESIS\_CH2 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH2_LSB[3:0]				HYSTERESIS_CH2[3:0]			
R/W-1111b				R/W-0b			

**Table 40. HYSTERESIS\_CH2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH2_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH2[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteresis is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

**8.5.31 HIGH\_TH\_CH2 Register (Address = 0x29) [reset = 0xFF]**

HIGH\_TH\_CH2 is shown in [Figure 69](#) and described in [Table 41](#).

Return to the [Summary Table](#).

**Figure 69. HIGH\_TH\_CH2 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH2_MSB[7:0]							
R/W-1111111b							

**Table 41. HIGH\_TH\_CH2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH2_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.5.32 EVENT\_COUNT\_CH2 Register (Address = 0x2A) [reset = 0x0]**

EVENT\_COUNT\_CH2 is shown in [Figure 70](#) and described in [Table 42](#).

Return to the [Summary Table](#).

**Figure 70. EVENT\_COUNT\_CH2 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH2_LSB[3:0]				EVENT_COUNT_CH2[3:0]			
R/W-0b				R/W-0b			

**Table 42. EVENT\_COUNT\_CH2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH2_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH2[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples exceeding either high or low threshold before setting alert flag.

**8.5.33 LOW\_TH\_CH2 Register (Address = 0x2B) [reset = 0x0]**

LOW\_TH\_CH2 is shown in [Figure 71](#) and described in [Table 43](#).

Return to the [Summary Table](#).

**Figure 71. LOW\_TH\_CH2 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH2_MSB[7:0]							
R/W-0b							

**Table 43. LOW\_TH\_CH2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH2_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.5.34 HYSTERESIS\_CH3 Register (Address = 0x2C) [reset = 0xF0]**

HYSTERESIS\_CH3 is shown in [Figure 72](#) and described in [Table 44](#).

Return to the [Summary Table](#).

**Figure 72. HYSTERESIS\_CH3 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH3_LSB[3:0]				HYSTERESIS_CH3[3:0]			
R/W-1111b				R/W-0b			

**Table 44. HYSTERESIS\_CH3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH3_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH3[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteresis is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

**8.5.35 HIGH\_TH\_CH3 Register (Address = 0x2D) [reset = 0xFF]**

HIGH\_TH\_CH3 is shown in [Figure 73](#) and described in [Table 45](#).

Return to the [Summary Table](#).

**Figure 73. HIGH\_TH\_CH3 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH3_MSB[7:0]							
R/W-11111111b							

**Table 45. HIGH\_TH\_CH3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH3_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.5.36 EVENT\_COUNT\_CH3 Register (Address = 0x2E) [reset = 0x0]**

EVENT\_COUNT\_CH3 is shown in [Figure 74](#) and described in [Table 46](#).

Return to the [Summary Table](#).

**Figure 74. EVENT\_COUNT\_CH3 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH3_LSB[3:0]				EVENT_COUNT_CH3[3:0]			
R/W-0b				R/W-0b			

**Table 46. EVENT\_COUNT\_CH3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH3_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.

**Table 46. EVENT\_COUNT\_CH3 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
3-0	EVENT_COUNT_CH3[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples exceeding either high or low threshold before setting alert flag.

**8.5.37 LOW\_TH\_CH3 Register (Address = 0x2F) [reset = 0x0]**

LOW\_TH\_CH3 is shown in [Figure 75](#) and described in [Table 47](#).

Return to the [Summary Table](#).

**Figure 75. LOW\_TH\_CH3 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH3_MSB[7:0]							
R/W-0b							

**Table 47. LOW\_TH\_CH3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH3_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.5.38 HYSTERESIS\_CH4 Register (Address = 0x30) [reset = 0xF0]**

HYSTERESIS\_CH4 is shown in [Figure 76](#) and described in [Table 48](#).

Return to the [Summary Table](#).

**Figure 76. HYSTERESIS\_CH4 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH4_LSB[3:0]				HYSTERESIS_CH4[3:0]			
R/W-1111b				R/W-0b			

**Table 48. HYSTERESIS\_CH4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH4_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH4[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteresis is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

**8.5.39 HIGH\_TH\_CH4 Register (Address = 0x31) [reset = 0xFF]**

HIGH\_TH\_CH4 is shown in [Figure 77](#) and described in [Table 49](#).

Return to the [Summary Table](#).

**Figure 77. HIGH\_TH\_CH4 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH4_MSB[7:0]							
R/W-11111111b							

**Table 49. HIGH\_TH\_CH4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH4_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

### 8.5.40 EVENT\_COUNT\_CH4 Register (Address = 0x32) [reset = 0x0]

EVENT\_COUNT\_CH4 is shown in [Figure 78](#) and described in [Table 50](#).

Return to the [Summary Table](#).

**Figure 78. EVENT\_COUNT\_CH4 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH4_LSB[3:0]				EVENT_COUNT_CH4[3:0]			
R/W-0b				R/W-0b			

**Table 50. EVENT\_COUNT\_CH4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH4_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH4[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples exceeding either high or low threshold before setting alert flag.

### 8.5.41 LOW\_TH\_CH4 Register (Address = 0x33) [reset = 0x0]

LOW\_TH\_CH4 is shown in [Figure 79](#) and described in [Table 51](#).

Return to the [Summary Table](#).

**Figure 79. LOW\_TH\_CH4 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH4_MSB[7:0]							
R/W-0b							

**Table 51. LOW\_TH\_CH4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH4_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

### 8.5.42 HYSTERESIS\_CH5 Register (Address = 0x34) [reset = 0xF0]

HYSTERESIS\_CH5 is shown in [Figure 80](#) and described in [Table 52](#).

Return to the [Summary Table](#).

**Figure 80. HYSTERESIS\_CH5 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH5_LSB[3:0]				HYSTERESIS_CH5[3:0]			
R/W-1111b				R/W-0b			

**Table 52. HYSTERESIS\_CH5 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH5_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH5[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteresis is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

### 8.5.43 HIGH\_TH\_CH5 Register (Address = 0x35) [reset = 0xFF]

HIGH\_TH\_CH5 is shown in [Figure 81](#) and described in [Table 53](#).

Return to the [Summary Table](#).

**Figure 81. HIGH\_TH\_CH5 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH5_MSB[7:0]							
R/W-1111111b							

**Table 53. HIGH\_TH\_CH5 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH5_MSB[7:0]	R/W	1111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.5.44 EVENT\_COUNT\_CH5 Register (Address = 0x36) [reset = 0x0]**

EVENT\_COUNT\_CH5 is shown in [Figure 82](#) and described in [Table 54](#).

Return to the [Summary Table](#).

**Figure 82. EVENT\_COUNT\_CH5 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH5_LSB[3:0]				EVENT_COUNT_CH5[3:0]			
R/W-0b				R/W-0b			

**Table 54. EVENT\_COUNT\_CH5 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH5_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH5[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples exceeding either high or low threshold before setting alert flag.

**8.5.45 LOW\_TH\_CH5 Register (Address = 0x37) [reset = 0x0]**

LOW\_TH\_CH5 is shown in [Figure 83](#) and described in [Table 55](#).

Return to the [Summary Table](#).

**Figure 83. LOW\_TH\_CH5 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH5_MSB[7:0]							
R/W-0b							

**Table 55. LOW\_TH\_CH5 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH5_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.5.46 HYSTERESIS\_CH6 Register (Address = 0x38) [reset = 0xF0]**

HYSTERESIS\_CH6 is shown in [Figure 84](#) and described in [Table 56](#).

Return to the [Summary Table](#).

**Figure 84. HYSTERESIS\_CH6 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH6_LSB[3:0]				HYSTERESIS_CH6[3:0]			
R/W-1111b				R/W-0b			

**Table 56. HYSTERESIS\_CH6 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH6_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH6[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteresis is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

**8.5.47 HIGH\_TH\_CH6 Register (Address = 0x39) [reset = 0xFF]**

HIGH\_TH\_CH6 is shown in [Figure 85](#) and described in [Table 57](#).

Return to the [Summary Table](#).

**Figure 85. HIGH\_TH\_CH6 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH6_MSB[7:0]							
R/W-1111111b							

**Table 57. HIGH\_TH\_CH6 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH6_MSB[7:0]	R/W	1111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.5.48 EVENT\_COUNT\_CH6 Register (Address = 0x3A) [reset = 0x0]**

EVENT\_COUNT\_CH6 is shown in [Figure 86](#) and described in [Table 58](#).

Return to the [Summary Table](#).

**Figure 86. EVENT\_COUNT\_CH6 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH6_LSB[3:0]				EVENT_COUNT_CH6[3:0]			
R/W-0b				R/W-0b			

**Table 58. EVENT\_COUNT\_CH6 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH6_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH6[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples exceeding either high or low threshold before setting alert flag.

**8.5.49 LOW\_TH\_CH6 Register (Address = 0x3B) [reset = 0x0]**

LOW\_TH\_CH6 is shown in [Figure 87](#) and described in [Table 59](#).

Return to the [Summary Table](#).

**Figure 87. LOW\_TH\_CH6 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH6_MSB[7:0]							
R/W-0b							

**Table 59. LOW\_TH\_CH6 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH6_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.5.50 HYSTERESIS\_CH7 Register (Address = 0x3C) [reset = 0xF0]**

HYSTERESIS\_CH7 is shown in [Figure 88](#) and described in [Table 60](#).

Return to the [Summary Table](#).

**Figure 88. HYSTERESIS\_CH7 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH7_LSB[3:0]				HYSTERESIS_CH7[3:0]			
R/W-1111b				R/W-0b			

**Table 60. HYSTERESIS\_CH7 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH7_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH7[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteresis is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

**8.5.51 HIGH\_TH\_CH7 Register (Address = 0x3D) [reset = 0xFF]**

HIGH\_TH\_CH7 is shown in [Figure 89](#) and described in [Table 61](#).

Return to the [Summary Table](#).

**Figure 89. HIGH\_TH\_CH7 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH7_MSB[7:0]							
R/W-11111111b							

**Table 61. HIGH\_TH\_CH7 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH7_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.5.52 EVENT\_COUNT\_CH7 Register (Address = 0x3E) [reset = 0x0]**

EVENT\_COUNT\_CH7 is shown in [Figure 90](#) and described in [Table 62](#).

Return to the [Summary Table](#).

**Figure 90. EVENT\_COUNT\_CH7 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH7_LSB[3:0]				EVENT_COUNT_CH7[3:0]			
R/W-0b				R/W-0b			

**Table 62. EVENT\_COUNT\_CH7 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH7_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.

**Table 62. EVENT\_COUNT\_CH7 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
3-0	EVENT_COUNT_CH7[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples exceeding either high or low threshold before setting alert flag.

### 8.5.53 LOW\_TH\_CH7 Register (Address = 0x3F) [reset = 0x0]

LOW\_TH\_CH7 is shown in [Figure 91](#) and described in [Table 63](#).

Return to the [Summary Table](#).

**Figure 91. LOW\_TH\_CH7 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH7_MSB[7:0]							
R/W-0b							

**Table 63. LOW\_TH\_CH7 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH7_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

### 8.5.54 MAX\_CH0\_LSB Register (Address = 0x60) [reset = 0x0]

MAX\_CH0\_LSB is shown in [Figure 92](#) and described in [Table 64](#).

Return to the [Summary Table](#).

**Figure 92. MAX\_CH0\_LSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH0_LSB[7:0]							
R-0b							

**Table 64. MAX\_CH0\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH0_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

### 8.5.55 MAX\_CH0\_MSB Register (Address = 0x61) [reset = 0x0]

MAX\_CH0\_MSB is shown in [Figure 93](#) and described in [Table 65](#).

Return to the [Summary Table](#).

**Figure 93. MAX\_CH0\_MSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH0_MSB[7:0]							
R-0b							

**Table 65. MAX\_CH0\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH0_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

**8.5.56 MAX\_CH1\_LSB Register (Address = 0x62) [reset = 0x0]**

 MAX\_CH1\_LSB is shown in [Figure 94](#) and described in [Table 66](#).

 Return to the [Summary Table](#).

**Figure 94. MAX\_CH1\_LSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH1_LSB[7:0]							
R-0b							

**Table 66. MAX\_CH1\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH1_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

**8.5.57 MAX\_CH1\_MSB Register (Address = 0x63) [reset = 0x0]**

 MAX\_CH1\_MSB is shown in [Figure 95](#) and described in [Table 67](#).

 Return to the [Summary Table](#).

**Figure 95. MAX\_CH1\_MSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH1_MSB[7:0]							
R-0b							

**Table 67. MAX\_CH1\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH1_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

**8.5.58 MAX\_CH2\_LSB Register (Address = 0x64) [reset = 0x0]**

 MAX\_CH2\_LSB is shown in [Figure 96](#) and described in [Table 68](#).

 Return to the [Summary Table](#).

**Figure 96. MAX\_CH2\_LSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH2_LSB[7:0]							
R-0b							

**Table 68. MAX\_CH2\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH2_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

**8.5.59 MAX\_CH2\_MSB Register (Address = 0x65) [reset = 0x0]**

 MAX\_CH2\_MSB is shown in [Figure 97](#) and described in [Table 69](#).

 Return to the [Summary Table](#).

**Figure 97. MAX\_CH2\_MSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH2_MSB[7:0]							
R-0b							

**Table 69. MAX\_CH2\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH2_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

### 8.5.60 MAX\_CH3\_LSB Register (Address = 0x66) [reset = 0x0]

MAX\_CH3\_LSB is shown in [Figure 98](#) and described in [Table 70](#).

Return to the [Summary Table](#).

**Figure 98. MAX\_CH3\_LSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH3_LSB[7:0]							
R-0b							

**Table 70. MAX\_CH3\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH3_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

### 8.5.61 MAX\_CH3\_MSB Register (Address = 0x67) [reset = 0x0]

MAX\_CH3\_MSB is shown in [Figure 99](#) and described in [Table 71](#).

Return to the [Summary Table](#).

**Figure 99. MAX\_CH3\_MSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH3_MSB[7:0]							
R-0b							

**Table 71. MAX\_CH3\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH3_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

### 8.5.62 MAX\_CH4\_LSB Register (Address = 0x68) [reset = 0x0]

MAX\_CH4\_LSB is shown in [Figure 100](#) and described in [Table 72](#).

Return to the [Summary Table](#).

**Figure 100. MAX\_CH4\_LSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH4_LSB[7:0]							
R-0b							

**Table 72. MAX\_CH4\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH4_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

**8.5.63 MAX\_CH4\_MSB Register (Address = 0x69) [reset = 0x0]**

 MAX\_CH4\_MSB is shown in [Figure 101](#) and described in [Table 73](#).

 Return to the [Summary Table](#).

**Figure 101. MAX\_CH4\_MSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH4_MSB[7:0]							
R-0b							

**Table 73. MAX\_CH4\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH4_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

**8.5.64 MAX\_CH5\_LSB Register (Address = 0x6A) [reset = 0x0]**

 MAX\_CH5\_LSB is shown in [Figure 102](#) and described in [Table 74](#).

 Return to the [Summary Table](#).

**Figure 102. MAX\_CH5\_LSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH5_LSB[7:0]							
R-0b							

**Table 74. MAX\_CH5\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH5_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

**8.5.65 MAX\_CH5\_MSB Register (Address = 0x6B) [reset = 0x0]**

 MAX\_CH5\_MSB is shown in [Figure 103](#) and described in [Table 75](#).

 Return to the [Summary Table](#).

**Figure 103. MAX\_CH5\_MSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH5_MSB[7:0]							
R-0b							

**Table 75. MAX\_CH5\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH5_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

### 8.5.66 MAX\_CH6\_LSB Register (Address = 0x6C) [reset = 0x0]

MAX\_CH6\_LSB is shown in [Figure 104](#) and described in [Table 76](#).

Return to the [Summary Table](#).

**Figure 104. MAX\_CH6\_LSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH6_LSB[7:0]							
R-0b							

**Table 76. MAX\_CH6\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH6_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

### 8.5.67 MAX\_CH6\_MSB Register (Address = 0x6D) [reset = 0x0]

MAX\_CH6\_MSB is shown in [Figure 105](#) and described in [Table 77](#).

Return to the [Summary Table](#).

**Figure 105. MAX\_CH6\_MSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH6_MSB[7:0]							
R-0b							

**Table 77. MAX\_CH6\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH6_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

### 8.5.68 MAX\_CH7\_LSB Register (Address = 0x6E) [reset = 0x0]

MAX\_CH7\_LSB is shown in [Figure 106](#) and described in [Table 78](#).

Return to the [Summary Table](#).

**Figure 106. MAX\_CH7\_LSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH7_LSB[7:0]							
R-0b							

**Table 78. MAX\_CH7\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH7_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

### 8.5.69 MAX\_CH7\_MSB Register (Address = 0x6F) [reset = 0x0]

MAX\_CH7\_MSB is shown in [Figure 107](#) and described in [Table 79](#).

Return to the [Summary Table](#).

**Figure 107. MAX\_CH7\_MSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH7_MSB[7:0]							
R-0b							

**Table 79. MAX\_CH7\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH7_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

**8.5.70 MIN\_CH0\_LSB Register (Address = 0x80) [reset = 0xFF]**

 MIN\_CH0\_LSB is shown in [Figure 108](#) and described in [Table 80](#).

 Return to the [Summary Table](#).

**Figure 108. MIN\_CH0\_LSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH0_LSB[7:0]							
R-11111111b							

**Table 80. MIN\_CH0\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH0_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

**8.5.71 MIN\_CH0\_MSB Register (Address = 0x81) [reset = 0xFF]**

 MIN\_CH0\_MSB is shown in [Figure 109](#) and described in [Table 81](#).

 Return to the [Summary Table](#).

**Figure 109. MIN\_CH0\_MSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH0_MSB[7:0]							
R-11111111b							

**Table 81. MIN\_CH0\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH0_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

**8.5.72 MIN\_CH1\_LSB Register (Address = 0x82) [reset = 0xFF]**

 MIN\_CH1\_LSB is shown in [Figure 110](#) and described in [Table 82](#).

 Return to the [Summary Table](#).

**Figure 110. MIN\_CH1\_LSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH1_LSB[7:0]							
R-11111111b							

**Table 82. MIN\_CH1\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH1_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

**8.5.73 MIN\_CH1\_MSB Register (Address = 0x83) [reset = 0xFF]**

MIN\_CH1\_MSB is shown in [Figure 111](#) and described in [Table 83](#).

Return to the [Summary Table](#).

**Figure 111. MIN\_CH1\_MSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH1_MSB[7:0]							
R-11111111b							

**Table 83. MIN\_CH1\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH1_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

**8.5.74 MIN\_CH2\_LSB Register (Address = 0x84) [reset = 0xFF]**

MIN\_CH2\_LSB is shown in [Figure 112](#) and described in [Table 84](#).

Return to the [Summary Table](#).

**Figure 112. MIN\_CH2\_LSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH2_LSB[7:0]							
R-11111111b							

**Table 84. MIN\_CH2\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH2_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

**8.5.75 MIN\_CH2\_MSB Register (Address = 0x85) [reset = 0xFF]**

MIN\_CH2\_MSB is shown in [Figure 113](#) and described in [Table 85](#).

Return to the [Summary Table](#).

**Figure 113. MIN\_CH2\_MSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH2_MSB[7:0]							
R-11111111b							

**Table 85. MIN\_CH2\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH2_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

**8.5.76 MIN\_CH3\_LSB Register (Address = 0x86) [reset = 0xFF]**

 MIN\_CH3\_LSB is shown in [Figure 114](#) and described in [Table 86](#).

 Return to the [Summary Table](#).

**Figure 114. MIN\_CH3\_LSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH3_LSB[7:0]							
R-11111111b							

**Table 86. MIN\_CH3\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH3_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

**8.5.77 MIN\_CH3\_MSB Register (Address = 0x87) [reset = 0xFF]**

 MIN\_CH3\_MSB is shown in [Figure 115](#) and described in [Table 87](#).

 Return to the [Summary Table](#).

**Figure 115. MIN\_CH3\_MSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH3_MSB[7:0]							
R-11111111b							

**Table 87. MIN\_CH3\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH3_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

**8.5.78 MIN\_CH4\_LSB Register (Address = 0x88) [reset = 0xFF]**

 MIN\_CH4\_LSB is shown in [Figure 116](#) and described in [Table 88](#).

 Return to the [Summary Table](#).

**Figure 116. MIN\_CH4\_LSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH4_LSB[7:0]							
R-11111111b							

**Table 88. MIN\_CH4\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH4_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

**8.5.79 MIN\_CH4\_MSB Register (Address = 0x89) [reset = 0xFF]**

 MIN\_CH4\_MSB is shown in [Figure 117](#) and described in [Table 89](#).

 Return to the [Summary Table](#).

**Figure 117. MIN\_CH4\_MSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH4_MSB[7:0]							
R-11111111b							

**Table 89. MIN\_CH4\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH4_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

**8.5.80 MIN\_CH5\_LSB Register (Address = 0x8A) [reset = 0xFF]**

MIN\_CH5\_LSB is shown in [Figure 118](#) and described in [Table 90](#).

Return to the [Summary Table](#).

**Figure 118. MIN\_CH5\_LSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH5_LSB[7:0]							
R-11111111b							

**Table 90. MIN\_CH5\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH5_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

**8.5.81 MIN\_CH5\_MSB Register (Address = 0x8B) [reset = 0xFF]**

MIN\_CH5\_MSB is shown in [Figure 119](#) and described in [Table 91](#).

Return to the [Summary Table](#).

**Figure 119. MIN\_CH5\_MSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH5_MSB[7:0]							
R-11111111b							

**Table 91. MIN\_CH5\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH5_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

**8.5.82 MIN\_CH6\_LSB Register (Address = 0x8C) [reset = 0xFF]**

MIN\_CH6\_LSB is shown in [Figure 120](#) and described in [Table 92](#).

Return to the [Summary Table](#).

**Figure 120. MIN\_CH6\_LSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH6_LSB[7:0]							
R-11111111b							

**Table 92. MIN\_CH6\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH6_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

**8.5.83 MIN\_CH6\_MSB Register (Address = 0x8D) [reset = 0xFF]**

 MIN\_CH6\_MSB is shown in [Figure 121](#) and described in [Table 93](#).

 Return to the [Summary Table](#).

**Figure 121. MIN\_CH6\_MSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH6_MSB[7:0]							
R-11111111b							

**Table 93. MIN\_CH6\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH6_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

**8.5.84 MIN\_CH7\_LSB Register (Address = 0x8E) [reset = 0xFF]**

 MIN\_CH7\_LSB is shown in [Figure 122](#) and described in [Table 94](#).

 Return to the [Summary Table](#).

**Figure 122. MIN\_CH7\_LSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH7_LSB[7:0]							
R-11111111b							

**Table 94. MIN\_CH7\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH7_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

**8.5.85 MIN\_CH7\_MSB Register (Address = 0x8F) [reset = 0xFF]**

 MIN\_CH7\_MSB is shown in [Figure 123](#) and described in [Table 95](#).

 Return to the [Summary Table](#).

**Figure 123. MIN\_CH7\_MSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH7_MSB[7:0]							
R-11111111b							

**Table 95. MIN\_CH7\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH7_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

**8.5.86 RECENT\_CH0\_LSB Register (Address = 0xA0) [reset = 0x0]**

RECENT\_CH0\_LSB is shown in [Figure 124](#) and described in [Table 96](#).

Return to the [Summary Table](#).

**Figure 124. RECENT\_CH0\_LSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH0_LSB[7:0]							
R-0b							

**Table 96. RECENT\_CH0\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH0_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

**8.5.87 RECENT\_CH0\_MSB Register (Address = 0xA1) [reset = 0x0]**

RECENT\_CH0\_MSB is shown in [Figure 125](#) and described in [Table 97](#).

Return to the [Summary Table](#).

**Figure 125. RECENT\_CH0\_MSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH0_MSB[7:0]							
R-0b							

**Table 97. RECENT\_CH0\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH0_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

**8.5.88 RECENT\_CH1\_LSB Register (Address = 0xA2) [reset = 0x0]**

RECENT\_CH1\_LSB is shown in [Figure 126](#) and described in [Table 98](#).

Return to the [Summary Table](#).

**Figure 126. RECENT\_CH1\_LSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH1_LSB[7:0]							
R-0b							

**Table 98. RECENT\_CH1\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH1_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

**8.5.89 RECENT\_CH1\_MSB Register (Address = 0xA3) [reset = 0x0]**

RECENT\_CH1\_MSB is shown in [Figure 127](#) and described in [Table 99](#).

Return to the [Summary Table](#).

**Figure 127. RECENT\_CH1\_MSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH1_MSB[7:0]							
R-0b							

**Table 99. RECENT\_CH1\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH1_MSB [7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

**8.5.90 RECENT\_CH2\_LSB Register (Address = 0xA4) [reset = 0x0]**

RECENT\_CH2\_LSB is shown in [Figure 128](#) and described in [Table 100](#).

Return to the [Summary Table](#).

**Figure 128. RECENT\_CH2\_LSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH2_LSB[7:0]							
R-0b							

**Table 100. RECENT\_CH2\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH2_LSB [7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

**8.5.91 RECENT\_CH2\_MSB Register (Address = 0xA5) [reset = 0x0]**

RECENT\_CH2\_MSB is shown in [Figure 129](#) and described in [Table 101](#).

Return to the [Summary Table](#).

**Figure 129. RECENT\_CH2\_MSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH2_MSB[7:0]							
R-0b							

**Table 101. RECENT\_CH2\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH2_MSB [7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

**8.5.92 RECENT\_CH3\_LSB Register (Address = 0xA6) [reset = 0x0]**

RECENT\_CH3\_LSB is shown in [Figure 130](#) and described in [Table 102](#).

Return to the [Summary Table](#).

**Figure 130. RECENT\_CH3\_LSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH3_LSB[7:0]							
R-0b							

**Table 102. RECENT\_CH3\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH3_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

**8.5.93 RECENT\_CH3\_MSB Register (Address = 0xA7) [reset = 0x0]**

RECENT\_CH3\_MSB is shown in [Figure 131](#) and described in [Table 103](#).

Return to the [Summary Table](#).

**Figure 131. RECENT\_CH3\_MSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH3_MSB[7:0]							
R-0b							

**Table 103. RECENT\_CH3\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH3_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

**8.5.94 RECENT\_CH4\_LSB Register (Address = 0xA8) [reset = 0x0]**

RECENT\_CH4\_LSB is shown in [Figure 132](#) and described in [Table 104](#).

Return to the [Summary Table](#).

**Figure 132. RECENT\_CH4\_LSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH4_LSB[7:0]							
R-0b							

**Table 104. RECENT\_CH4\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH4_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

**8.5.95 RECENT\_CH4\_MSB Register (Address = 0xA9) [reset = 0x0]**

RECENT\_CH4\_MSB is shown in [Figure 133](#) and described in [Table 105](#).

Return to the [Summary Table](#).

**Figure 133. RECENT\_CH4\_MSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH4_MSB[7:0]							
R-0b							

**Table 105. RECENT\_CH4\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH4_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

**8.5.96 RECENT\_CH5\_LSB Register (Address = 0xAA) [reset = 0x0]**

 RECENT\_CH5\_LSB is shown in [Figure 134](#) and described in [Table 106](#).

 Return to the [Summary Table](#).

**Figure 134. RECENT\_CH5\_LSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH5_LSB[7:0]							
R-0b							

**Table 106. RECENT\_CH5\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH5_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

**8.5.97 RECENT\_CH5\_MSB Register (Address = 0xAB) [reset = 0x0]**

 RECENT\_CH5\_MSB is shown in [Figure 135](#) and described in [Table 107](#).

 Return to the [Summary Table](#).

**Figure 135. RECENT\_CH5\_MSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH5_MSB[7:0]							
R-0b							

**Table 107. RECENT\_CH5\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH5_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

**8.5.98 RECENT\_CH6\_LSB Register (Address = 0xAC) [reset = 0x0]**

 RECENT\_CH6\_LSB is shown in [Figure 136](#) and described in [Table 108](#).

 Return to the [Summary Table](#).

**Figure 136. RECENT\_CH6\_LSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH6_LSB[7:0]							
R-0b							

**Table 108. RECENT\_CH6\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH6_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

**8.5.99 RECENT\_CH6\_MSB Register (Address = 0xAD) [reset = 0x0]**

 RECENT\_CH6\_MSB is shown in [Figure 137](#) and described in [Table 109](#).

 Return to the [Summary Table](#).

**Figure 137. RECENT\_CH6\_MSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH6_MSB[7:0]							
R-0b							

**Table 109. RECENT\_CH6\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH6_MSB [7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

**8.5.100 RECENT\_CH7\_LSB Register (Address = 0xAE) [reset = 0x0]**

RECENT\_CH7\_LSB is shown in [Figure 138](#) and described in [Table 110](#).

Return to the [Summary Table](#).

**Figure 138. RECENT\_CH7\_LSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH7_LSB[7:0]							
R-0b							

**Table 110. RECENT\_CH7\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH7_LSB [7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

**8.5.101 RECENT\_CH7\_MSB Register (Address = 0xAF) [reset = 0x0]**

RECENT\_CH7\_MSB is shown in [Figure 139](#) and described in [Table 111](#).

Return to the [Summary Table](#).

**Figure 139. RECENT\_CH7\_MSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH7_MSB[7:0]							
R-0b							

**Table 111. RECENT\_CH7\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH7_MSB [7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

**8.5.102 RMS\_CFG Register (Address = 0xC0) [reset = 0x0]**

RMS\_CFG is shown in [Figure 140](#) and described in [Table 112](#).

Return to the [Summary Table](#).

**Figure 140. RMS\_CFG Register**

7	6	5	4	3	2	1	0
RMS_CHID[3:0]			RESERVED	RMS_DC_SUB	RMS_SAMPLES[1:0]		
R/W-0b			R-0b	R/W-0b	R/W-0b		

**Table 112. RMS\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	RMS_CHID[3:0]	R/W	0b	Select analog input channel for RMS computation.
3	RESERVED	R	0b	Reserved. Reads return 0.
2	RMS_DC_SUB	R/W	0b	Subtract DC component from the RMS result. 0b = Do not subtract DC component. 1b = Subtract DC component.
1-0	RMS_SAMPLES[1:0]	R/W	0b	Number of samples for computing RMS result. 0b = 1024 1b = 4096 10b = 16384 11b = 65536

**8.5.103 RMS\_LSB Register (Address = 0xC1) [reset = 0x0]**

 RMS\_LSB is shown in [Figure 141](#) and described in [Table 113](#).

 Return to the [Summary Table](#).

**Figure 141. RMS\_LSB Register**

7	6	5	4	3	2	1	0
RMS_RESULT_LSB[7:0]							
R-0b							

**Table 113. RMS\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	RMS_RESULT_LSB[7:0]	R	0b	Lower 8-bits of RMS computation result.

**8.5.104 RMS\_MSB Register (Address = 0xC2) [reset = 0x0]**

 RMS\_MSB is shown in [Figure 142](#) and described in [Table 114](#).

 Return to the [Summary Table](#).

**Figure 142. RMS\_MSB Register**

7	6	5	4	3	2	1	0
RMS_RESULT_MSB[7:0]							
R-0b							

**Table 114. RMS\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	RMS_RESULT_MSB[7:0]	R	0b	Upper 8-bits of RMS result.

**8.5.105 GPO0\_TRIG\_EVENT\_SEL Register (Address = 0xC3) [reset = 0x2]**

 GPO0\_TRIG\_EVENT\_SEL is shown in [Figure 143](#) and described in [Table 115](#).

 Return to the [Summary Table](#).

**Figure 143. GPO0\_TRIG\_EVENT\_SEL Register**

7	6	5	4	3	2	1	0
GPO0_TRIG_EVENT_SEL[7:0]							
R/W-10b							

**Table 115. GPO0\_TRIG\_EVENT\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO0_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0] which can trigger an event based update on GPO0. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO0 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO0 output.

**8.5.106 GPO1\_TRIG\_EVENT\_SEL Register (Address = 0xC5) [reset = 0x1]**

GPO1\_TRIG\_EVENT\_SEL is shown in [Figure 144](#) and described in [Table 116](#).

Return to the [Summary Table](#).

**Figure 144. GPO1\_TRIG\_EVENT\_SEL Register**

7	6	5	4	3	2	1	0
GPO1_TRIG_EVENT_SEL[7:0]							
R/W-1b							

**Table 116. GPO1\_TRIG\_EVENT\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO1_TRIG_EVENT_SEL[7:0]	R/W	1b	Select the inputs AIN/GPIO[7:0] which can trigger an event based update on GPO1. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO1 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO1 output.

**8.5.107 GPO2\_TRIG\_EVENT\_SEL Register (Address = 0xC7) [reset = 0x8]**

GPO2\_TRIG\_EVENT\_SEL is shown in [Figure 145](#) and described in [Table 117](#).

Return to the [Summary Table](#).

**Figure 145. GPO2\_TRIG\_EVENT\_SEL Register**

7	6	5	4	3	2	1	0
GPO2_TRIG_EVENT_SEL[7:0]							
R/W-1000b							

**Table 117. GPO2\_TRIG\_EVENT\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO2_TRIG_EVENT_SEL[7:0]	R/W	1000b	Select the inputs AIN/GPIO[7:0] which can trigger an event based update on GPO2. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO2 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO2 output.

**8.5.108 GPO3\_TRIG\_EVENT\_SEL Register (Address = 0xC9) [reset = 0x4]**

GPO3\_TRIG\_EVENT\_SEL is shown in [Figure 146](#) and described in [Table 118](#).

Return to the [Summary Table](#).

**Figure 146. GPO3\_TRIG\_EVENT\_SEL Register**

7	6	5	4	3	2	1	0
GPO3_TRIG_EVENT_SEL[7:0]							
R/W-100b							

**Table 118. GPO3\_TRIG\_EVENT\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO3_TRIG_EVENT_SEL[7:0]	R/W	100b	Select the inputs AIN/GPIO[7:0] which can trigger an event based update on GPO3. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO3 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO3 output.

**8.5.109 GPO4\_TRIG\_EVENT\_SEL Register (Address = 0xCB) [reset = 0x20]**

 GPO4\_TRIG\_EVENT\_SEL is shown in [Figure 147](#) and described in [Table 119](#).

 Return to the [Summary Table](#).

**Figure 147. GPO4\_TRIG\_EVENT\_SEL Register**

7	6	5	4	3	2	1	0
GPO4_TRIG_EVENT_SEL[7:0]							
R/W-100000b							

**Table 119. GPO4\_TRIG\_EVENT\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO4_TRIG_EVENT_SEL[7:0]	R/W	100000b	Select the inputs AIN/GPIO[7:0] which can trigger an Event based update on GPO4. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO4 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO4 output.

**8.5.110 GPO5\_TRIG\_EVENT\_SEL Register (Address = 0xCD) [reset = 0x10]**

 GPO5\_TRIG\_EVENT\_SEL is shown in [Figure 148](#) and described in [Table 120](#).

 Return to the [Summary Table](#).

**Figure 148. GPO5\_TRIG\_EVENT\_SEL Register**

7	6	5	4	3	2	1	0
GPO5_TRIG_EVENT_SEL[7:0]							
R/W-10000b							

**Table 120. GPO5\_TRIG\_EVENT\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO5_TRIG_EVENT_SEL[7:0]	R/W	10000b	Select the inputs AIN/GPIO[7:0] which can trigger an Event based update on GPO5. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO5 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO5 output.

### 8.5.111 GPO6\_TRIG\_EVENT\_SEL Register (Address = 0xCF) [reset = 0x80]

GPO6\_TRIG\_EVENT\_SEL is shown in [Figure 149](#) and described in [Table 121](#).

Return to the [Summary Table](#).

**Figure 149. GPO6\_TRIG\_EVENT\_SEL Register**

7	6	5	4	3	2	1	0
GPO6_TRIG_EVENT_SEL[7:0]							
R/W-1000000b							

**Table 121. GPO6\_TRIG\_EVENT\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO6_TRIG_EVENT_SEL[7:0]	R/W	1000000b	Select the inputs AIN/GPIO[7:0] which can trigger an Event based update on GPO6. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO6 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO6 output.

### 8.5.112 GPO7\_TRIG\_EVENT\_SEL Register (Address = 0xD1) [reset = 0x40]

GPO7\_TRIG\_EVENT\_SEL is shown in [Figure 150](#) and described in [Table 122](#).

Return to the [Summary Table](#).

**Figure 150. GPO7\_TRIG\_EVENT\_SEL Register**

7	6	5	4	3	2	1	0
GPO7_TRIG_EVENT_SEL[7:0]							
R/W-1000000b							

**Table 122. GPO7\_TRIG\_EVENT\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO7_TRIG_EVENT_SEL[7:0]	R/W	1000000b	Select the inputs AIN/GPIO[7:0] which can trigger an Event based update on GPO7. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO7 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO7 output.

### 8.5.113 GPO\_VALUE\_ZCD\_CFG\_CH0\_CH3 Register (Address = 0xE3) [reset = 0x0]

GPO\_VALUE\_ZCD\_CFG\_CH0\_CH3 is shown in [Figure 151](#) and described in [Table 123](#).

Return to the [Summary Table](#).

**Figure 151. GPO\_VALUE\_ZCD\_CFG\_CH0\_CH3 Register**

7	6	5	4	3	2	1	0
GPO_VALUE_ZCD_CFG_CH3[1:0]	GPO_VALUE_ZCD_CFG_CH2[1:0]	GPO_VALUE_ZCD_CFG_CH1[1:0]	GPO_VALUE_ZCD_CFG_CH0[1:0]				
R/W-0b	R/W-0b	R/W-0b	R/W-0b				

**Table 123. GPO\_VALUE\_ZCD\_CFG\_CH0\_CH3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	GPO_VALUE_ZCD_CFG_CH3[1:0]	R/W	0b	Define the GPO value to be launched on ZCD rising and falling edges. 0b = Rising (0) and falling (0) -> logic 0 on both edges 1b = Rising (0) and falling (1) -> ZCD_bar 10b = Rising (1) and falling (0) -> ZCD 11b = Rising (1) and falling (1) -> logic 1 on both edges
5-4	GPO_VALUE_ZCD_CFG_CH2[1:0]	R/W	0b	Define the GPO value to be launched on ZCD rising and falling edges. 0b = Rising (0) and falling (0) -> logic 0 on both edges 1b = Rising (0) and falling (1) -> ZCD_bar 10b = Rising (1) and falling (0) -> ZCD 11b = Rising (1) and falling (1) -> logic 1 on both edges
3-2	GPO_VALUE_ZCD_CFG_CH1[1:0]	R/W	0b	Define the GPO value to be launched on ZCD rising and falling edges. 0b = Rising (0) and falling (0) -> logic 0 on both edges 1b = Rising (0) and falling (1) -> ZCD_bar 10b = Rising (1) and falling (0) -> ZCD 11b = Rising (1) and falling (1) -> logic 1 on both edges
1-0	GPO_VALUE_ZCD_CFG_CH0[1:0]	R/W	0b	Define the GPO value to be launched on ZCD rising and falling edges. 0b = Rising (0) and falling (0) -> logic 0 on both edges 1b = Rising (0) and falling (1) -> ZCD_bar 10b = Rising (1) and falling (0) -> ZCD 11b = Rising (1) and falling (1) -> logic 1 on both edges

**8.5.114 GPO\_VALUE\_ZCD\_CFG\_CH4\_CH7 Register (Address = 0xE4) [reset = 0x0]**

 GPO\_VALUE\_ZCD\_CFG\_CH4\_CH7 is shown in [Figure 152](#) and described in [Table 124](#).

 Return to the [Summary Table](#).

**Figure 152. GPO\_VALUE\_ZCD\_CFG\_CH4\_CH7 Register**

7	6	5	4	3	2	1	0
GPO_VALUE_ZCD_CFG_CH7[1:0]	GPO_VALUE_ZCD_CFG_CH6[1:0]	GPO_VALUE_ZCD_CFG_CH5[1:0]	GPO_VALUE_ZCD_CFG_CH4[1:0]	GPO_VALUE_ZCD_CFG_CH3[1:0]	GPO_VALUE_ZCD_CFG_CH2[1:0]	GPO_VALUE_ZCD_CFG_CH1[1:0]	GPO_VALUE_ZCD_CFG_CH0[1:0]
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

**Table 124. GPO\_VALUE\_ZCD\_CFG\_CH4\_CH7 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	GPO_VALUE_ZCD_CFG_CH7[1:0]	R/W	0b	Define the GPO value to be launched on ZCD rising and falling edges. 0b = Rising (0) and falling (0) -> logic 0 on both edges 1b = Rising (0) and falling (1) -> ZCD_bar 10b = Rising (1) and falling (0) -> ZCD 11b = Rising (1) and falling (1) -> logic 1 on both edges
5-4	GPO_VALUE_ZCD_CFG_CH6[1:0]	R/W	0b	Define the GPO value to be launched on ZCD rising and falling edges. 0b = Rising (0) and falling (0) -> logic 0 on both edges 1b = Rising (0) and falling (1) -> ZCD_bar 10b = Rising (1) and falling (0) -> ZCD 11b = Rising (1) and falling (1) -> logic 1 on both edges

**Table 124. GPO\_VALUE\_ZCD\_CFG\_CH4\_CH7 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
3-2	GPO_VALUE_ZCD_CFG_CH5[1:0]	R/W	0b	Define the GPO value to be launched on ZCD rising and falling edges. 0b = Rising (0) and falling (0) -> logic 0 on both edges 1b = Rising (0) and falling (1) -> ZCD_bar 10b = Rising (1) and falling (0) -> ZCD 11b = Rising (1) and falling (1) -> logic 1 on both edges
1-0	GPO_VALUE_ZCD_CFG_CH4[1:0]	R/W	0b	Define the GPO value to be launched on ZCD rising and falling edges. 0b = Rising (0) and falling (0) -> logic 0 on both edges 1b = Rising (0) and falling (1) -> ZCD_bar 10b = Rising (1) and falling (0) -> ZCD 11b = Rising (1) and falling (1) -> logic 1 on both edges

**8.5.115 GPO\_ZCD\_UPDATE\_EN Register (Address = 0xE7) [reset = 0x0]**

GPO\_ZCD\_UPDATE\_EN is shown in [Figure 153](#) and described in [Table 125](#).

Return to the [Summary Table](#).

**Figure 153. GPO\_ZCD\_UPDATE\_EN Register**

7	6	5	4	3	2	1	0
GPO_ZCD_UPDATE_EN[7:0]							
R/W-0b							

**Table 125. GPO\_ZCD\_UPDATE\_EN Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO_ZCD_UPDATE_EN[7:0]	R/W	0b	Update digital outputs GPO[7:0] synchronous to ZCD. 0b = Digital output not updated synchronous to ZCD. 1b = Digital output updated synchronous to ZCD. Configure GPO_VALUE_ON_ZCD_CFG register.

**8.5.116 GPO\_TRIGGER\_CFG Register (Address = 0xE9) [reset = 0x0]**

GPO\_TRIGGER\_CFG is shown in [Figure 154](#) and described in [Table 126](#).

Return to the [Summary Table](#).

**Figure 154. GPO\_TRIGGER\_CFG Register**

7	6	5	4	3	2	1	0
GPO_TRIGGER_UPDATE_EN[7:0]							
R/W-0b							

**Table 126. GPO\_TRIGGER\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO_TRIGGER_UPDATE_EN[7:0]	R/W	0b	Update digital outputs GPO[7:0] when corresponding trigger is set. . 0b = Digital output is not updated in response to alert flags. 1b = Digital output is updated when corresponding alert flags are set. Configure GPOx_TRIG_EVENT_SEL register to select which alert flags can trigger an update on the desired GPO.

**8.5.117 GPO\_VALUE\_TRIG Register (Address = 0xEB) [reset = 0x0]**

 GPO\_VALUE\_TRIG is shown in [Figure 155](#) and described in [Table 127](#).

 Return to the [Summary Table](#).

**Figure 155. GPO\_VALUE\_TRIG Register**

7	6	5	4	3	2	1	0
GPO_VALUE_ON_TRIGGER[7:0]							
R/W-0b							

**Table 127. GPO\_VALUE\_TRIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO_VALUE_ON_TRIGGER[7:0]	R/W	0b	Value to be set on digital outputs GPO[7:0] when corresponding trigger occurs. GPO update on alert flags must be enabled in corresponding bit in GPO_TRIGGER_CFG register. 0b = Digital output set to logic 0. 1b = Digital output set to logic 1.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register analog-to-digital converter (SAR ADC) are the input driver and the reference driver circuits. This section details some general principles for designing the input driver circuit, reference driver circuit, and provides some application circuits designed for the ADS7028.

### 9.2 Typical Applications

#### 9.2.1 Mixed-Channel Configuration

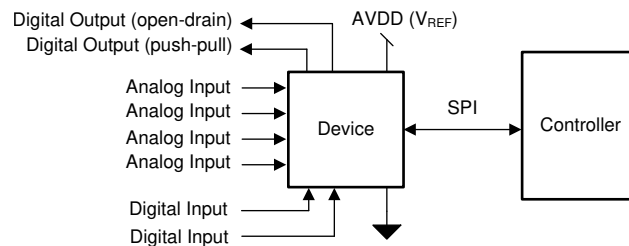


Figure 156. DAQ Circuit: Single-Supply DAQ

##### 9.2.1.1 Design Requirements

The goal of this application is to configure some channels of the ADS7028 as digital inputs, open-drain digital outputs, and push-pull digital outputs.

##### 9.2.1.2 Detailed Design Procedure

The ADS7028 can support GPIO functionality at each input pin. Any analog input pin can be independently configured as a digital input, a digital open-drain output, or a digital push-pull output through the PIN\_CFG and GPIO\_CFG registers; see [Table 3](#).

##### 9.2.1.2.1 Digital Input

The digital input functionality can be used to monitor a signal within the system. [Figure 157](#) illustrates that the state of the digital input can be read from the GPI\_VALUE register.

Typical Applications (continued)

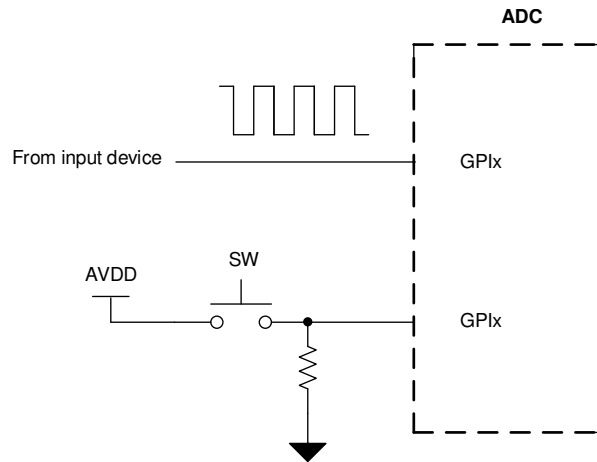


Figure 157. Digital Input

9.2.1.2.2 Digital Open-Drain Output

The channels of the ADS7028 can be configured as digital open-drain outputs supporting an output voltage up to 5.5 V. An open-drain output, as shown in Figure 158, consists of an internal FET (Q) connected to ground. The output is idle when not driven by the device, which means Q is off and the pullup resistor, R<sub>PULL\_UP</sub>, connects the GPOx node to the desired output voltage. The output voltage can range anywhere up to 5.5 V, depending on the external voltage that the GPIOx is pulled up to. When the device is driving the output, Q turns on, thus connecting the pullup resistor to ground and bringing the node voltage at GPOx low.

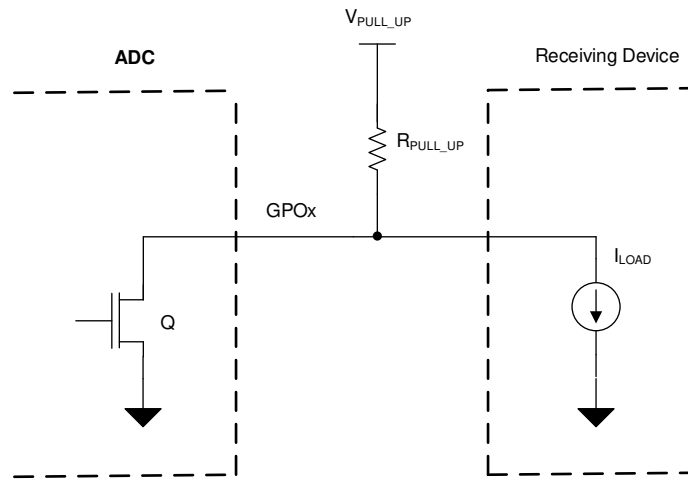


Figure 158. Digital Open-Drain Output

The minimum value of the pullup resistor, as calculated in Equation 6, is given by the ratio of V<sub>PULL\_UP</sub> and the maximum current supported by the device digital output (5 mA).

$$R_{MIN} = (V_{PULL\_UP} / 5 \text{ mA}) \tag{6}$$

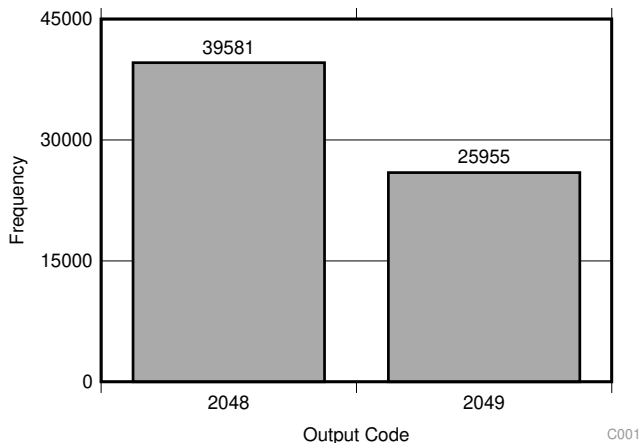
The maximum value of the pullup resistor, as calculated in Equation 7, depends on the minimum input current requirement, I<sub>LOAD</sub>, of the receiving device driven by this GPIO.

$$R_{MAX} = (V_{PULL\_UP} / I_{LOAD}) \tag{7}$$

Select R<sub>PULL\_UP</sub> such that R<sub>MIN</sub> < R<sub>PULL\_UP</sub> < R<sub>MAX</sub>.

## Typical Applications (continued)

### 9.2.1.3 Application Curve

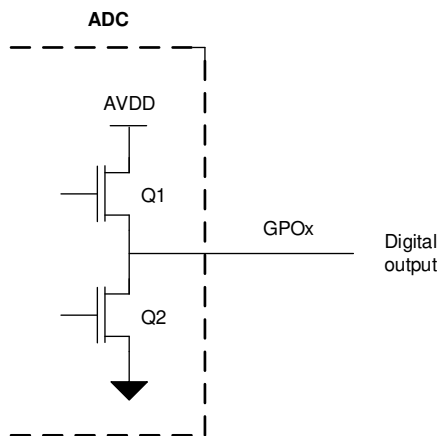


Standard deviation = 0.49 LSB

**Figure 159. DC Input Histogram**

### 9.2.2 Digital Push-Pull Output Configuration

The channels of the ADS7028 can be configured as digital push-pull outputs supporting an output voltage up to AVDD. As shown in Figure 160, a push-pull output consists of two mirrored opposite bipolar transistors, Q1 and Q2. The device can both source and sink current because only one transistor is on at a time (either Q2 is on and pulls the output low, or Q1 is on and sets the output high). A push-pull configuration always drives the line opposed to an open-drain output where the line is left floating.



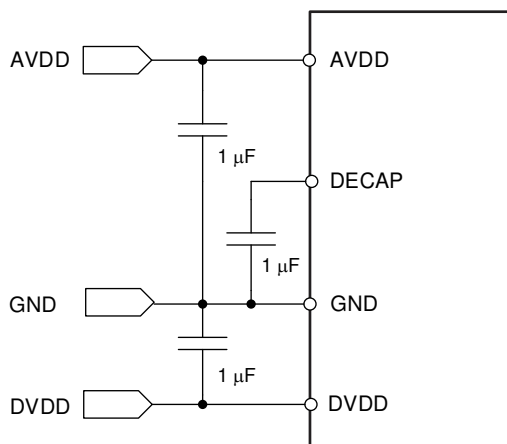
**Figure 160. Digital Push-Pull Output**

## 10 Power Supply Recommendations

### 10.1 AVDD and DVDD Supply Recommendations

The ADS7028 has two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. For supplies greater than 2.35 V, AVDD and DVDD can be shorted externally if single-supply operation is desired. The AVDD supply also defines the full-scale input range of the device. Decouple the AVDD and DVDD pins individually, as illustrated in [Figure 161](#), with 1- $\mu$ F ceramic decoupling capacitors. The minimum capacitor value required for AVDD and DVDD is 200 nF and 20 nF, respectively. If both supplies are powered from the same source, a minimum capacitor value of 220 nF is required for decoupling.

Connect 1- $\mu$ F ceramic decoupling capacitors between the DECAP and GND pins.



**Figure 161. Power-Supply Decoupling**

## 11 Layout

### 11.1 Layout Guidelines

Figure 162 shows a board layout example for the ADS7028. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the AVDD supply away from noise sources.

Use 1- $\mu$ F ceramic bypass capacitors in close proximity to the analog (AVDD) and digital (DVDD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect the GND pin to the ground plane using short, low-impedance paths. The AVDD supply voltage also functions as the reference voltage for the ADS7028. Place the decoupling capacitor for AVDD close to the device AVDD and GND pins and connect the decoupling capacitor to the device pins with thick copper tracks.

### 11.2 Layout Example

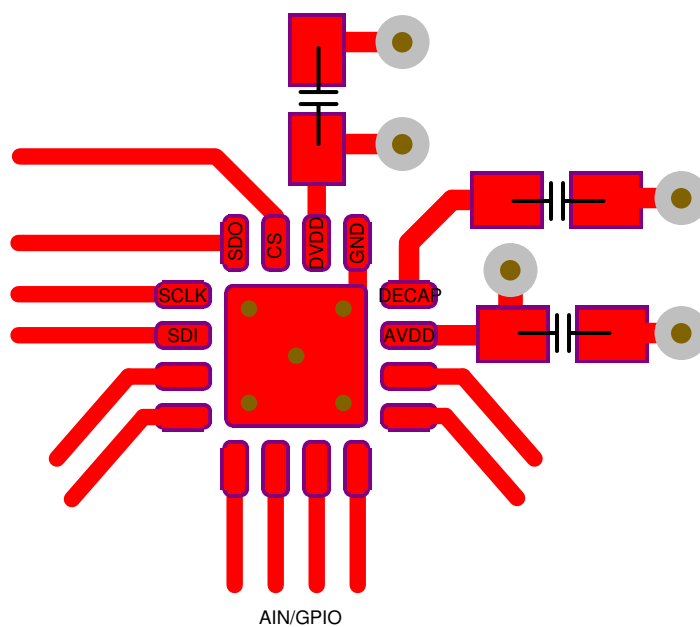


Figure 162. Example Layout

## 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 12.3 Trademarks

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

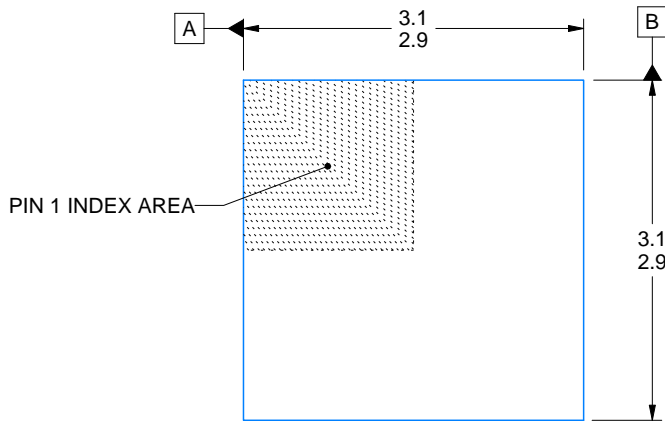
### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

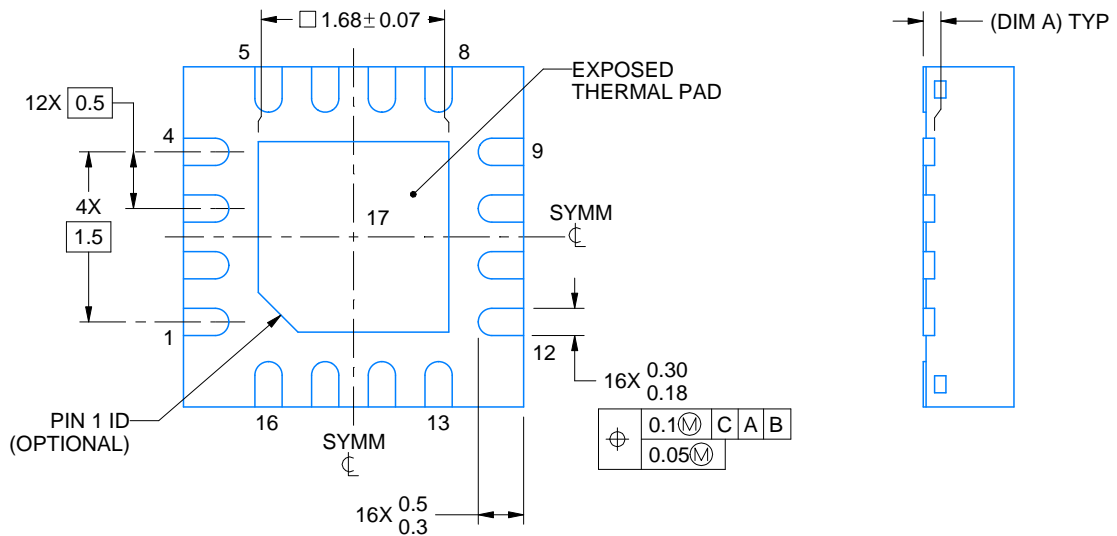
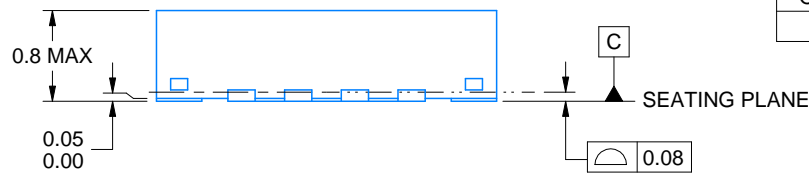
This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



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NOTES:

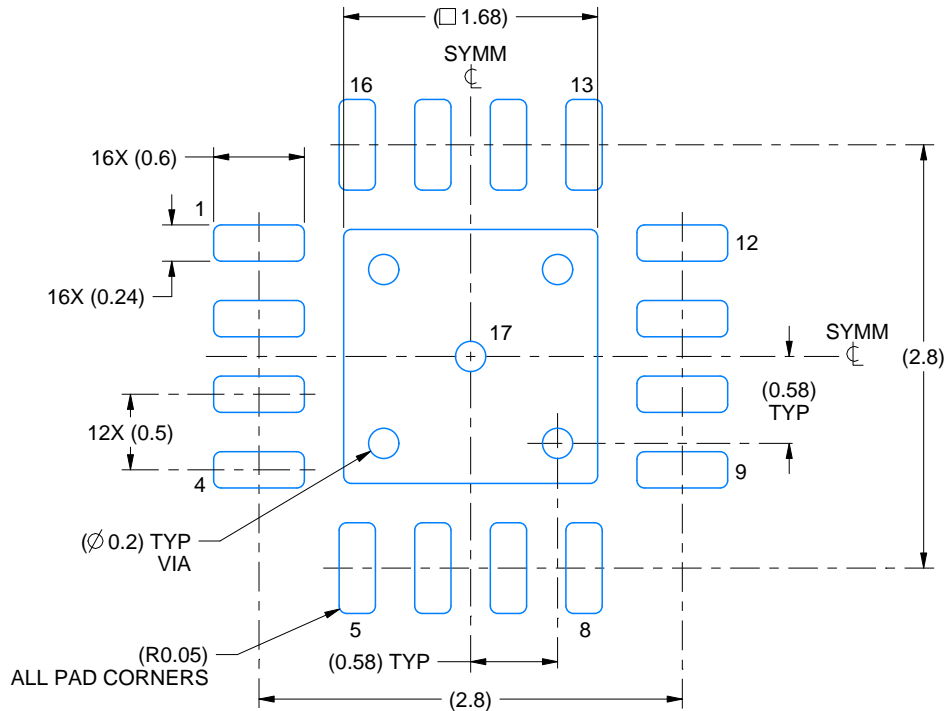
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

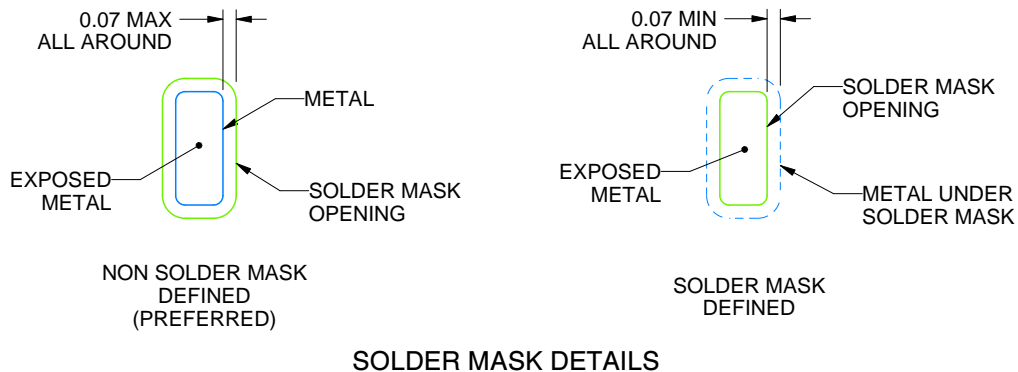
RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

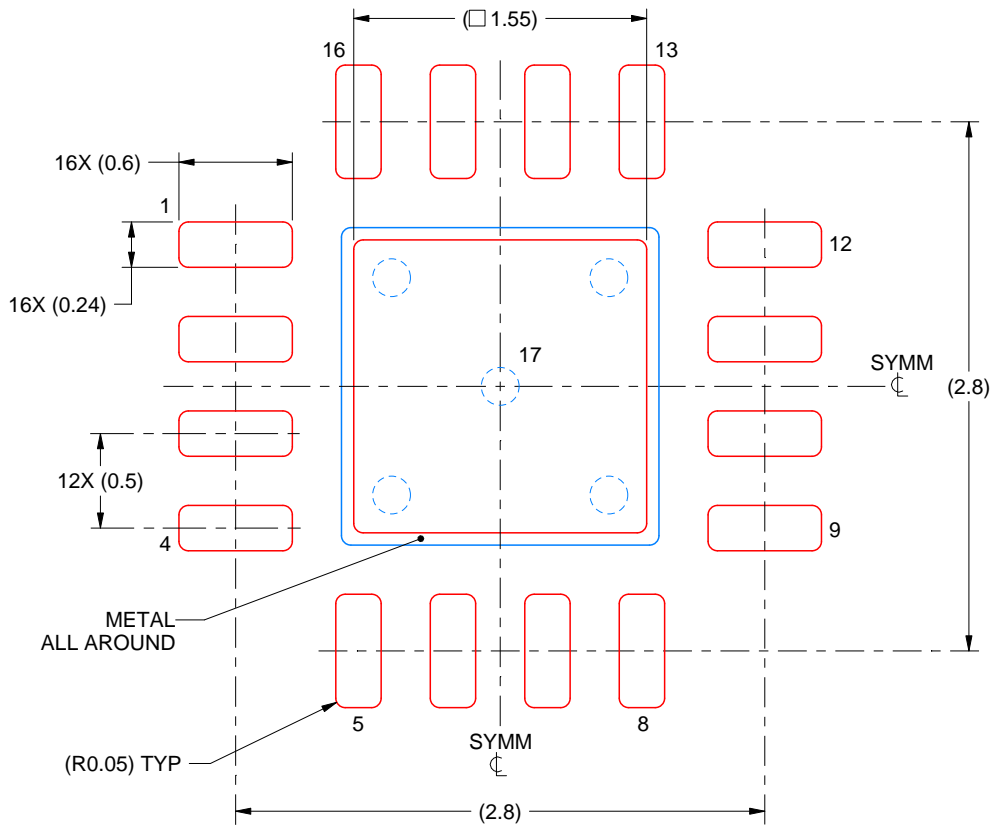
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:  
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7028IRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7028	<a href="#">Samples</a>
ADS7028IRTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7028	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

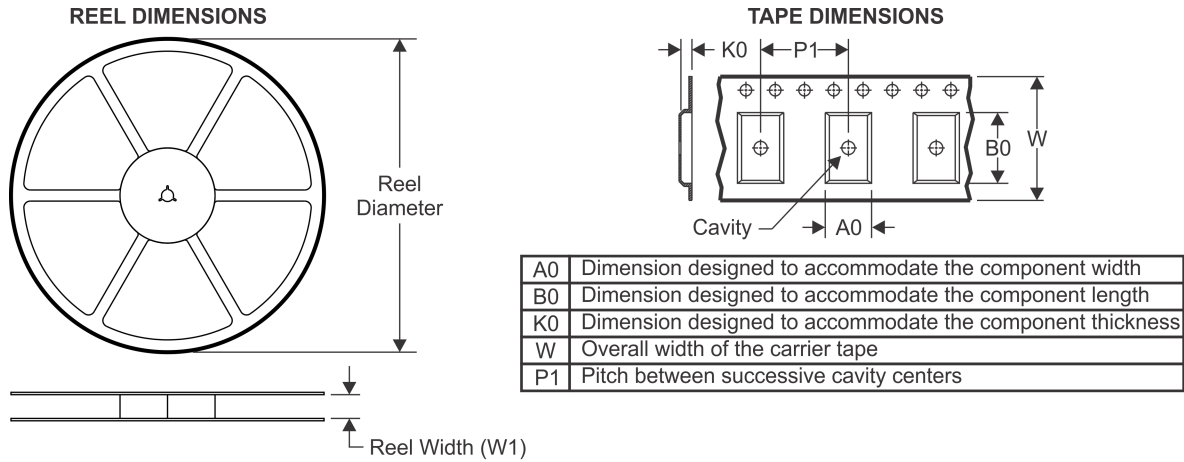
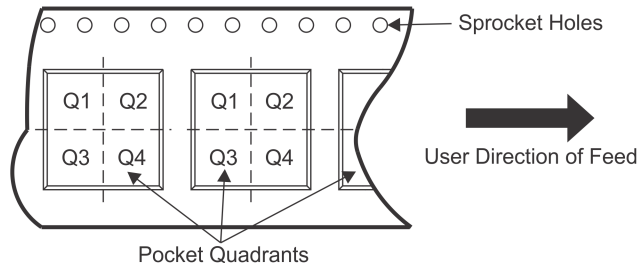
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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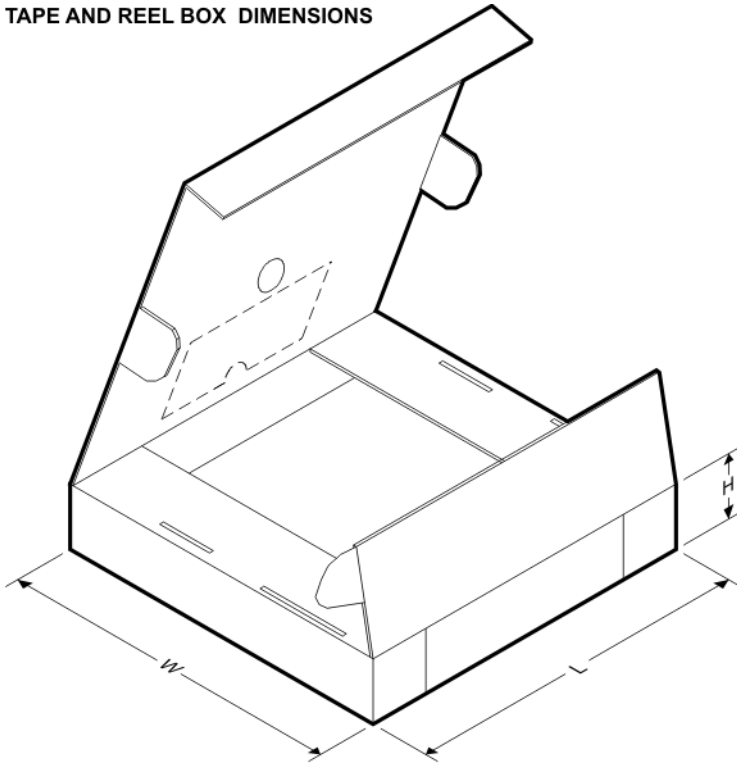
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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7028IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7028IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7028IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS7028IRTET	WQFN	RTE	16	250	210.0	185.0	35.0

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