



**THE DATASHEET OF  
9FG430AGILF**



# Four Output Differential Frequency Generator for PCIe Gen3 and QPI

9FG430

## General Description:

The 9FG430 is a Frequency Timing Generator that provides 4 HCSL differential output pairs. These outputs support PCI-Express Gen3, and QPI applications. The part supports Spread Spectrum and synthesizes several additional output frequencies from either a 14.31818 MHz crystal, a 25 MHz crystal or reference input clock. The 9FG430 also outputs a copy of the reference clock. Complete control of the device is available via strapping pins or via the SMBus interface.

## Recommended Application:

4 Output Differential Frequency Generator for PCIe Gen3 and QPI

## Output Features:

- 4 - 0.7V current mode differential HCSL output pairs
- 1 - 3.3V LVTTTL REF output

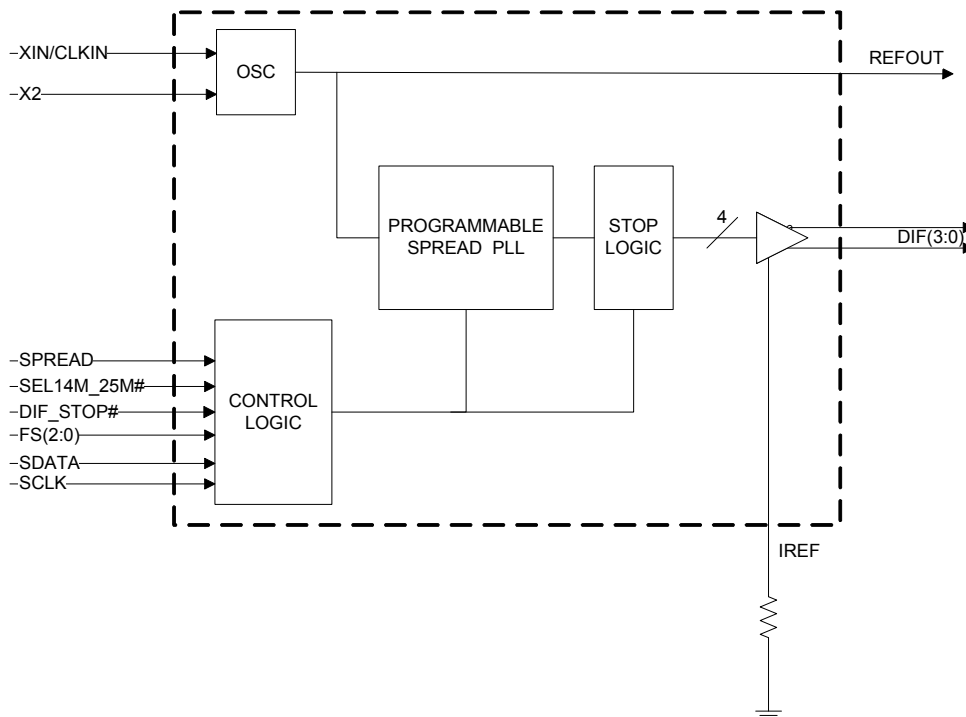
## Features/Benefits:

- Pin-to-Pin with 9FG104D/Easy upgrade to PCIe Gen3
- Generates common frequencies from 14.318 MHz or 25 MHz; single part supports multiple applications
- Provides copy of reference output; eliminates need for additional crystal or oscillator
- Unused outputs may be disabled in Hi-Z; save system power
- Device may be configured by SMBus and/or strap pins; can be used in systems without SMBus

## Key Specifications:

- Cycle-to-cycle jitter: < 50ps with 25MHz input
- Output-to-output skew: <50ps
- Phase jitter: PCIe Gen3 < 1ps rms
- Phase jitter: QPI 9.6GB/s < 0.2ps rms
- 10 ppm synthesis error with 25MHz input and Spread Off

## Functional Block Diagram



## Pin Configuration

|           |    |               |    |              |
|-----------|----|---------------|----|--------------|
| XIN/CLKIN | 1  | <b>9FG430</b> | 28 | VDDA         |
| X2        | 2  |               | 27 | GND          |
| VDD       | 3  |               | 26 | IREF         |
| GND       | 4  |               | 25 | vFS0         |
| REFOUT    | 5  |               | 24 | vFS1         |
| vFS2      | 6  |               | 23 | DIF_0        |
| DIF_3     | 7  |               | 22 | DIF_0#       |
| DIF_3#    | 8  |               | 21 | VDD          |
| VDD       | 9  |               | 20 | GND          |
| GND       | 10 |               | 19 | DIF_1        |
| DIF_2     | 11 |               | 18 | DIF_1#       |
| DIF_2#    | 12 |               | 17 | ^SEL14M_25M# |
| SDATA     | 13 |               | 16 | vSPREAD      |
| SCLK      | 14 |               | 15 | DIF_STOP#    |

^ indicates internal 120K pull up  
v indicates internal 120K pull down

## Power Groups

| Pin Number |       | Description                        |
|------------|-------|------------------------------------|
| VDD        | GND   |                                    |
| 3          | 4     | REFOUT, Digital Inputs             |
| 9,21       | 10,20 | DIF Outputs                        |
| 28         | 27    | IREF, Analog VDD, GND for PLL Core |

## Frequency Select Table

| SEL14M_25M#<br>(FS3) | FS2 | FS1 | FS0 | OUTPUT (MHz) |
|----------------------|-----|-----|-----|--------------|
| 0                    | 0   | 0   | 0   | 100.00       |
| 0                    | 0   | 0   | 1   | 125.00       |
| 0                    | 0   | 1   | 0   | 133.33       |
| 0                    | 0   | 1   | 1   | 166.67       |
| 0                    | 1   | 0   | 0   | 200.00       |
| 0                    | 1   | 0   | 1   | 266.67       |
| 0                    | 1   | 1   | 0   | 333.33       |
| 0                    | 1   | 1   | 1   | 400.00       |
| 1                    | 0   | 0   | 0   | 100.00       |
| 1                    | 0   | 0   | 1   | 125.00       |
| 1                    | 0   | 1   | 0   | 133.33       |
| 1                    | 0   | 1   | 1   | 166.67       |
| 1                    | 1   | 0   | 0   | 200.00       |
| 1                    | 1   | 0   | 1   | 266.67       |
| 1                    | 1   | 1   | 0   | 333.33       |
| 1                    | 1   | 1   | 1   | 400.00       |

## Pin Description

| PIN # | PIN NAME     | PIN TYPE | DESCRIPTION   |
|-------|--------------|----------|---|
| 1     | XIN/CLKIN    | IN       | Crystal input or Reference Clock input  |
| 2     | X2           | OUT      | Crystal output, Nominally 14.318MHz   |
| 3     | VDD          | PWR      | Power supply, nominal 3.3V  |
| 4     | GND          | PWR      | Ground pin.   |
| 5     | REFOUT       | OUT      | Reference Clock output  |
| 6     | vFS2         | IN       | Frequency select pin. This pin has an internal 120k pull down resistor  |
| 7     | DIF_3        | OUT      | 0.7V differential true clock output   |
| 8     | DIF_3#       | OUT      | 0.7V differential Complementary clock output  |
| 9     | VDD          | PWR      | Power supply, nominal 3.3V  |
| 10    | GND          | PWR      | Ground pin.   |
| 11    | DIF_2        | OUT      | 0.7V differential true clock output   |
| 12    | DIF_2#       | OUT      | 0.7V differential Complementary clock output  |
| 13    | SDATA        | I/O      | Data pin for SMBus circuitry, 5V tolerant.  |
| 14    | SCLK         | IN       | Clock pin of SMBus circuitry, 5V tolerant.  |
| 15    | DIF_STOP#    | IN       | Active low input to stop differential output clocks.  |
| 16    | vSPREAD      | IN       | Asynchronous, active high input to enable spread spectrum functionality. This pin has a 120Kohm pull down resistor.   |
| 17    | ^SEL14M_25M# | IN       | Select 14.31818 MHz or 25 Mhz input frequency. This pin has an internal 120kohm pull up resistor.<br>1 = 14.31818 MHz, 0 = 25 MHz   |
| 18    | DIF_1#       | OUT      | 0.7V differential Complementary clock output  |
| 19    | DIF_1        | OUT      | 0.7V differential true clock output   |
| 20    | GND          | PWR      | Ground pin.   |
| 21    | VDD          | PWR      | Power supply, nominal 3.3V  |
| 22    | DIF_0#       | OUT      | 0.7V differential Complementary clock output  |
| 23    | DIF_0        | OUT      | 0.7V differential true clock output   |
| 24    | vFS1         | IN       | Frequency select pin.   |
| 25    | vFS0         | IN       | Frequency select pin.   |
| 26    | IREF         | OUT      | This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet. |
| 27    | GND A        | PWR      | Ground pin for the PLL core.  |
| 28    | VDD A        | PWR      | 3.3V power for the PLL core.  |

### Note:

^ indicates internal 120K pull up

v indicates internal 120K pull down

**Electrical Characteristics - Absolute Maximum Ratings**

| PARAMETER                 | SYMBOL             | CONDITIONS                 | MIN     | TYP | MAX                   | UNITS | NOTES |
|---------------------------|--------------------|----------------------------|---------|-----|-----------------------|-------|-------|
| 3.3V Core Supply Voltage  | VDDA               |                            |         |     | 4.6                   | V     | 1,2   |
| 3.3V Logic Supply Voltage | VDD                |                            |         |     | 4.6                   | V     | 1,2   |
| Input Low Voltage         | V <sub>IL</sub>    |                            | GND-0.5 |     |                       | V     | 1     |
| Input High Voltage        | V <sub>IH</sub>    | Except for SMBus interface |         |     | V <sub>DD</sub> +0.5V | V     | 1     |
| Input High Voltage        | V <sub>IHSMB</sub> | SMBus clock and data pins  |         |     | 5.5V                  | V     | 1     |
| Storage Temperature       | T <sub>s</sub>     |                            | -65     |     | 150                   | °C    | 1     |
| Junction Temperature      | T <sub>j</sub>     |                            |         |     | 125                   | °C    | 1     |
| Input ESD protection      | ESD prot           | Human Body Model           | 2000    |     |                       | V     | 1     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Operation under these conditions is neither implied nor guaranteed.

**Electrical Characteristics - Input/Supply/Common Parameters**

TA = TCOM or TIND; Supply Voltage VDD = 3.3 V +/-5%; See Test Loads s for loading conditions.

| PARAMETER                     | SYMBOL              | CONDITIONS  | MIN       | TYP      | MAX                   | UNITS  | NOTES |
|-------------------------------|---------------------|---|-----------|----------|-----------------------|--------|-------|
| Ambient Operating Temperature | T <sub>COM</sub>    | Commercial range  | 0         |          | 70                    | °C     | 1     |
|                               | T <sub>IND</sub>    | Industrial range  | -40       |          | 85                    | °C     | 1     |
| Input High Voltage            | V <sub>IH</sub>     | Single-ended inputs, except SMBus, low threshold and tri-level inputs   | 2         |          | V <sub>DD</sub> + 0.3 | V      | 1     |
| Input Low Voltage             | V <sub>IL</sub>     | Single-ended inputs, except SMBus, low threshold and tri-level inputs   | GND - 0.3 |          | 0.8                   | V      | 1     |
| Input Current                 | I <sub>IN</sub>     | Single-ended inputs, V <sub>IN</sub> = GND, V <sub>IN</sub> = VDD   | -5        |          | 5                     | uA     | 1     |
|                               | I <sub>INP</sub>    | Single-ended inputs<br>V <sub>IN</sub> = 0 V; Inputs with internal pull-up resistors<br>V <sub>IN</sub> = VDD; Inputs with internal pull-down resistors | -200      |          | 200                   | uA     | 1     |
| Input Frequency               | F <sub>in</sub>     | SEL14M_25M# = 0   |           | 25       |                       | MHz    | 1     |
|                               |                     | SEL14M_25M# = 1   |           | 14.31818 |                       | MHz    | 1     |
| Pin Inductance                | L <sub>pin</sub>    |   |           |          | 7                     | nH     | 1     |
| Capacitance                   | C <sub>IN</sub>     | Logic Inputs, except DIF_IN   | 1.5       |          | 5                     | pF     | 1     |
|                               | C <sub>INXTAL</sub> | Crystal inputs  |           |          | 6                     | pF     | 1,4   |
|                               | C <sub>OUT</sub>    | Output pin capacitance  |           |          | 6                     | pF     | 1     |
| Clk Stabilization             | T <sub>STAB</sub>   | From V <sub>DD</sub> Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock   |           |          | 1.8                   | ms     | 1,2   |
| Input SS Modulation Frequency | f <sub>MODIN</sub>  | Allowable Frequency (Triangular Modulation)   | 30        |          | 33                    | kHz    | 1     |
| OE# Latency                   | t <sub>LATOE#</sub> | DIF start after OE# assertion<br>DIF stop after OE# deassertion   | 1         |          | 3                     | cycles | 1,3   |
| Tdrive_PD#                    | t <sub>DRVPD</sub>  | DIF output enable after PD# de-assertion  |           |          | 300                   | us     | 1,3   |
| Tfall                         | t <sub>F</sub>      | Fall time of control inputs   |           |          | 5                     | ns     | 1,2   |
| Trise                         | t <sub>R</sub>      | Rise time of control inputs   |           |          | 5                     | ns     | 1,2   |
| SMBus Input Low Voltage       | V <sub>ILSMB</sub>  |   |           |          | 0.8                   | V      | 1     |
| SMBus Input High Voltage      | V <sub>IHSMB</sub>  |   | 2.1       |          | V <sub>DD</sub> SMB   | V      | 1     |
| SMBus Output Low Voltage      | V <sub>OLSMB</sub>  | @ I <sub>PULLUP</sub>   |           |          | 0.4                   | V      | 1     |
| SMBus Sink Current            | I <sub>PULLUP</sub> | @ V <sub>OL</sub>   | 4         |          |                       | mA     | 1     |
| Nominal Bus Voltage           | V <sub>DD</sub> SMB | 3V to 5V +/- 10%  | 2.7       |          | 5.5                   | V      | 1     |
| SCLK/SDATA Rise Time          | t <sub>RSMB</sub>   | (Max VIL - 0.15) to (Min VIH + 0.15)  |           |          | 1000                  | ns     | 1     |
| SCLK/SDATA Fall Time          | t <sub>FSMB</sub>   | (Min VIH + 0.15) to (Max VIL - 0.15)  |           |          | 300                   | ns     | 1     |
| SMBus Operating Frequency     | f <sub>MAXSMB</sub> | Maximum SMBus operating frequency   |           |          | 100                   | kHz    | 1,5   |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Control input must be monotonic from 20% to 80% of input swing.

<sup>3</sup>Time from deassertion until outputs are >200 mV

<sup>4</sup>DIF\_IN input

<sup>5</sup>The differential input clock must be running for the SMBus to be active

**Electrical Characteristics - DIF 0.7V Current Mode Differential Outputs**

TA = TCOM or TIND; Supply Voltage VDD = 3.3 V +/-5%; See Test Loads s for loading conditions.

| PARAMETER              | SYMBOL           | CONDITIONS  | MIN  | TYP | MAX  | UNITS | NOTES   |
|------------------------|------------------|---|------|-----|------|-------|---------|
| Slew rate              | Trf              | Scope averaging on  | 1    |     | 4    | V/ns  | 1, 2, 3 |
| Slew rate matching     | $\Delta$ Trf     | Slew rate matching, Scope averaging on  |      |     | 20   | %     | 1, 2, 4 |
| Voltage High           | VHigh            | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660  |     | 850  | mV    | 1       |
| Voltage Low            | VLow             |   | -150 |     | 150  |       | 1       |
| Max Voltage            | Vmax             | Measurement on single ended signal using absolute value. (Scope averaging off)                        |      |     | 1150 | mV    | 1       |
| Min Voltage            | Vmin             |   | -300 |     |      |       | 1       |
| Vswing                 | Vswing           | Scope averaging off   | 300  |     |      | mV    | 1, 2    |
| Crossing Voltage (abs) | Vcross_abs       | Scope averaging off   | 250  |     | 550  | mV    | 1, 5    |
| Crossing Voltage (var) | $\Delta$ -Vcross | Scope averaging off   |      |     | 140  | mV    | 1, 6    |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production. IREF = VDD/(3xRR). For RR = 475 $\Omega$  (1%), IREF = 2.32mA. IOH = 6 x IREF and VOH = 0.7V @ ZO=50 $\Omega$  (100 $\Omega$  differential impedance).

<sup>2</sup> Measured from differential waveform

<sup>3</sup> Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

<sup>4</sup> Matching applies to rising edge rate of Clock / falling edge rate of Clock#. It is measured in a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope uses for the edge rate calculations.

<sup>5</sup> Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

<sup>6</sup> The total variation of all Vcross measurements in any particular system. Note that this is a subset of V\_cross\_min/max (V\_cross absolute) allowed. The intent is to limit Vcross induced modulation by setting V\_cross\_delta to be smaller than V\_cross absolute.

**Electrical Characteristics - Current Consumption**

TA = TCOM or TIND; Supply Voltage VDD = 3.3 V +/-5%, See Test Loads for loading

| PARAMETER                | SYMBOL     | CONDITIONS                              | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------|------------|---|-----|-----|-----|-------|-------|
| Operating Supply Current | IDD3.3     | VDD, All outputs active @100MHz         |     | 80  | 95  | mA    | 1     |
|                          | IDDA3.3OP  | VDDA, All outputs active @100MHz        |     | 25  | 30  | mA    | 1     |
|                          | IDD3.3     | VDD, All outputs active @400MHz         |     | 100 | 120 | mA    | 1     |
|                          | IDDA3.3OP  | VDDA, All outputs active @400MHz        |     | 25  | 30  | mA    | 1     |
| Powerdown Current        | IDD3.3PD   | VDD, All differential pairs driven      |     | 75  | 90  | mA    | 1     |
|                          | IDDA3.3PD  | VDDA, All differential pairs driven     |     | 25  | 30  | mA    | 1     |
|                          | IDD3.3PDZ  | VDD, All differential pairs tri-stated  |     | 25  | 30  | mA    | 1     |
|                          | IDDA3.3PDZ | VDDA, All differential pairs tri-stated |     | 25  | 30  | mA    | 1     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> IREF = VDD/(3xRR). For RR = 475 $\Omega$  (1%), IREF = 2.32mA. IOH = 6 x IREF and VOH = 0.7V @ ZO=50 $\Omega$ .

**Electrical Characteristics - Output Duty Cycle, Jitter, and Skew Characteristics**

TA = TCOM or TIND; Supply Voltage VDD = 3.3 V +/-5%, See Test Loads for loading

| PARAMETER              | SYMBOL    | CONDITIONS                        | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|-----------|-----------------------------------|-----|-----|-----|-------|-------|
| Duty Cycle             | tDC       | Measured differentially, PLL Mode | 45  |     | 55  | %     | 1     |
| Skew, Output to Output | tSK3      | VT = 50%                          |     |     | 50  | ps    | 1     |
| Jitter, Cycle to cycle | tjCyc-cyc | 25M input                         |     |     | 50  | ps    | 1,3   |
| Jitter, Cycle to cycle | tjCyc-cyc | 14.318M input                     |     |     | 60  | ps    | 1,3   |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> IREF = VDD/(3xRR). For RR = 475 $\Omega$  (1%), IREF = 2.32mA. IOH = 6 x IREF and VOH = 0.7V @ ZO=50 $\Omega$ .

<sup>3</sup> Measured from differential waveform

<sup>4</sup> Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

**Electrical Characteristics - Phase Jitter Parameters**TA = T<sub>COM</sub> or T<sub>IND</sub>; Supply Voltage VDD = 3.3 V +/-5%, See Test Loads for loading conditions

| PARAMETER                 | SYMBOL                  | CONDITIONS   | MIN | TYP | MAX | UNITS    | Notes     |
|---------------------------|-------------------------|--|-----|-----|-----|----------|-----------|
| Phase Jitter, PCI Express | t <sub>jphPCIeG1</sub>  | PCIe Gen 1   |     |     | 86  | ps (p-p) | 1,2,3,6   |
|                           | t <sub>jphPCIeG2</sub>  | PCIe Gen 2 Lo Band<br>10kHz < f < 1.5MHz               |     |     | 3   | ps (rms) | 1,2,6     |
|                           |                         | PCIe Gen 2 High Band<br>1.5MHz < f < Nyquist (50MHz)   |     |     | 3.1 | ps (rms) | 1,2,6     |
|                           | t <sub>jphPCIeG3</sub>  | PCIe Gen 3<br>(PLL BW of 2-4MHz, CDR = 10MHz)          |     |     | 1   | ps (rms) | 1,2,4,5,6 |
| Phase Jitter, QPI/SMI     | t <sub>jphQPI_SMI</sub> | QPI & SMI<br>(100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) |     |     | 0.5 | ps (rms) | 1,5,6     |
|                           |                         | QPI & SMI<br>(100MHz, 8.0Gb/s, 12UI)                   |     |     | 0.3 | ps (rms) | 1,5,6     |
|                           |                         | QPI & SMI<br>(100MHz, 9.6Gb/s, 12UI)                   |     |     | 0.2 | ps (rms) | 1,5,6     |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.<sup>2</sup> See <http://www.pcisiq.com> for complete specs<sup>3</sup> Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.<sup>4</sup> Subject to final radification by PCI SIG.<sup>5</sup> Calculated from Intel-supplied Clock Jitter Tool v 1.6.3<sup>6</sup> Applies to all differential outputs**Electrical Characteristics - REF-14.318/25 MHz**TA = T<sub>COM</sub> or T<sub>IND</sub>; Supply Voltage VDD = 3.3 V +/-5%, See Test Loads for loading

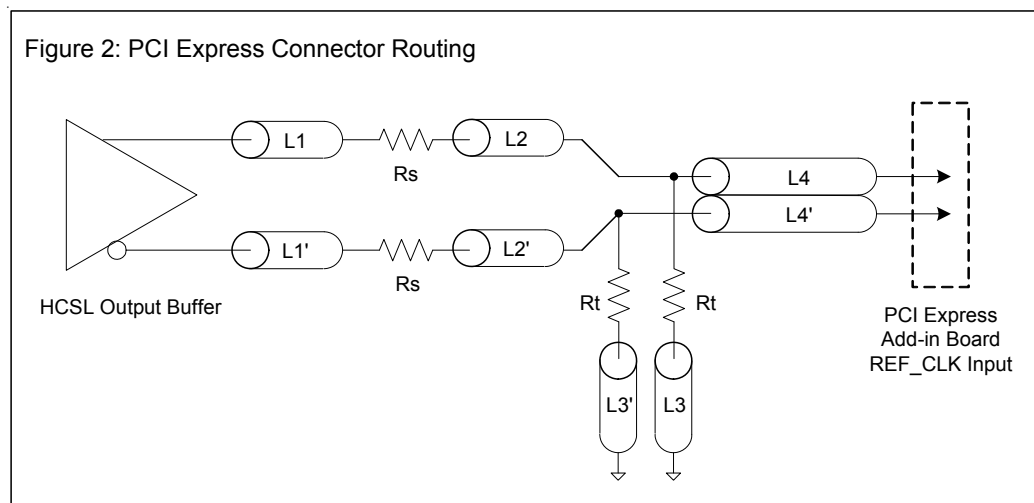
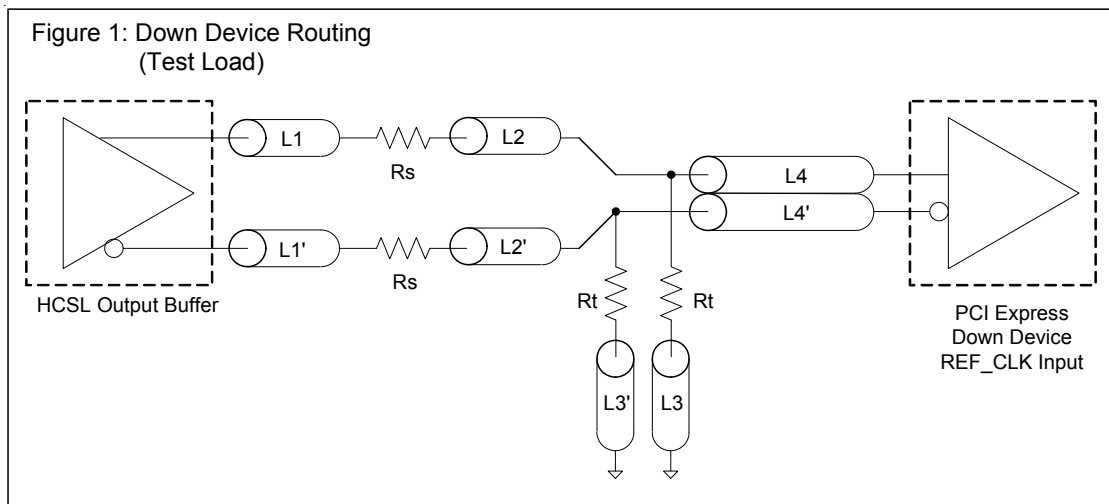
| PARAMETER           | SYMBOL               | CONDITIONS   | MIN | TYP     | MAX | UNITS | Notes |
|---------------------|----------------------|--|-----|---------|-----|-------|-------|
| Long Accuracy       | ppm                  | see T <sub>period</sub> min-max values                         |     | 0       |     | ppm   | 1     |
| Clock period        | T <sub>period</sub>  | 14.318MHz output nominal                                       |     | 69.8413 |     | ns    | 1,2   |
| Clock period        | T <sub>period</sub>  | 25.000MHz output nominal                                       |     | 40      |     | ns    | 1,2   |
| Output High Voltage | V <sub>OH</sub>      | I <sub>OH</sub> = -1 mA  | 2.4 |         |     | V     | 1     |
| Output Low Voltage  | V <sub>OL</sub>      | I <sub>OL</sub> = 1 mA   |     |         | 0.4 | V     | 1     |
| Output High Current | I <sub>OH</sub>      | V <sub>OH</sub> @ MIN = 1.0 V, V <sub>OH</sub> @ MAX = 3.135 V | -29 |         | -23 | mA    | 1     |
| Output Low Current  | I <sub>OL</sub>      | V <sub>OL</sub> @ MIN = 1.95 V, V <sub>OL</sub> @ MAX = 0.4 V  | 29  |         | 27  | mA    | 1     |
| Rise/Fall Time      | t <sub>rf1</sub>     | V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V               | 0.5 | 0.8     | 2   | ns    | 1     |
| Duty Cycle          | d <sub>t1</sub>      | V <sub>T</sub> = 1.5 V   | 45  |         | 55  | %     | 1     |
| Jitter              | t <sub>jcy-cyc</sub> | V <sub>T</sub> = 1.5 V   |     | 250     | 400 | ps    | 1     |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.<sup>2</sup> All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is at 14.31818 or 25.00 MHz

| Output Termination and Layout Information       |                    |      |        |
|---|--------------------|------|--------|
| Common Recommendations for Differential Routing | Dimension or Value | Unit | Figure |
| L1 length, route as non-coupled 50ohm trace     | 0.5 max            | inch | 1      |
| L2 length, route as non-coupled 50ohm trace     | 0.2 max            | inch | 1      |
| L3 length, route as non-coupled 50ohm trace     | 0.2 max            | inch | 1      |
| $R_s$   | 33                 | ohm  | 1      |
| $R_t$   | 49.9               | ohm  | 1      |

| Down Device Differential Routing                                 |                     |      |   |
|--|---------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 2 min to 16 max     | inch | 1 |
| L4 length, route as coupled stripline 100ohm differential trace  | 1.8 min to 14.4 max | inch | 1 |

| Differential Routing to PCI Express Connector                    |                       |      |   |
|--|-----------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 0.25 to 14 max        | inch | 2 |
| L4 length, route as coupled stripline 100ohm differential trace  | 0.225 min to 12.6 max | inch | 2 |

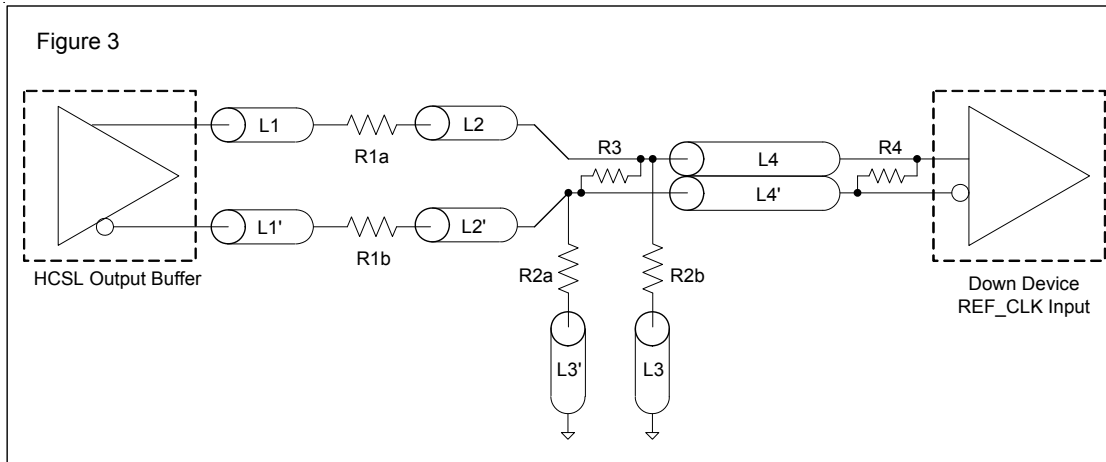


**Termination for LVDS and other Common Differential Signals (figure 3)**

| Vdiff | Vp-p  | Vcm  | R1 | R2   | R3   | R4  | Note                           |
|-------|-------|------|----|------|------|-----|--------------------------------|
| 0.45v | 0.22v | 1.08 | 33 | 150  | 100  | 100 |                                |
| 0.58  | 0.28  | 0.6  | 33 | 78.7 | 137  | 100 |                                |
| 0.80  | 0.40  | 0.6  | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60  | 0.3   | 1.2  | 33 | 174  | 140  | 100 | Standard LVDS                  |

R1a = R1b = R1

R2a = R2b = R2



**Termination for Cable AC Coupled Application (figure 4)**

| Component | Value       | Note |
|-----------|-------------|------|
| R5a, R5b  | 8.2K 5%     |      |
| R6a, R6b  | 1K 5%       |      |
| Cc        | 0.1 μF      |      |
| Vcm       | 0.350 volts |      |

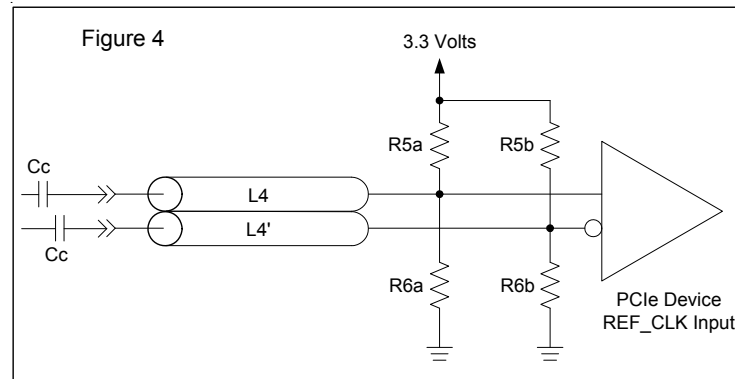
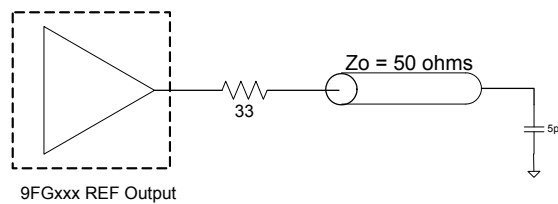


Figure 5. REF Output Test Load



## Differential Clock Tolerances x1 = 25MHz

## Clock Periods - Differential Outputs with Spread Spectrum Disabled

| SSC OFF<br>or SSC +/-<br>0.25%<br>Center<br>Spread | Synthesis<br>Error<br>(ppm) | Center<br>Freq.<br>MHz | Measurement Window           |                                      |                                      |                            |                                      |  |                                 | Units | Notes |
|--|-----------------------------|------------------------|------------------------------|--------------------------------------|--------------------------------------|----------------------------|--------------------------------------|--|---------------------------------|-------|-------|
|  |                             |                        | 1 Clock                      | 1us                                  | 0.1s                                 | 0.1s                       | 0.1s                                 | 1us                                      | 1 Clock                         |       |       |
|  |                             |                        | -c2c jitter<br>AbsPer<br>Min | -SSC<br>Short-Term<br>Average<br>Min | - ppm<br>Long-Term<br>Average<br>Min | 0 ppm<br>Period<br>Nominal | + ppm<br>Long-Term<br>Average<br>Max | +SSC<br>Short-<br>Term<br>Average<br>Max | +c2c<br>jitter<br>AbsPer<br>Max |       |       |
| DIF  | 0                           | 100.00                 | 9.95000                      |                                      | 10.00000                             | 10.00000                   | 10.00000                             |  | 10.05000                        | ns    | 1,2   |
|  | 0                           | 125.00                 | 7.95000                      |                                      | 8.00000                              | 8.00000                    | 8.00000                              |  | 8.05000                         | ns    | 1,2   |
|  | 0                           | 133.33                 | 7.45000                      |                                      | 7.50000                              | 7.50000                    | 7.50000                              |  | 7.55000                         | ns    | 1,2   |
|  | 10                          | 166.67                 | 5.94994                      |                                      | 5.99994                              | 6.00000                    | 6.00006                              |  | 6.05006                         | ns    | 1,2   |
|  | 0                           | 200.00                 | 4.95000                      |                                      | 5.00000                              | 5.00000                    | 5.00000                              |  | 5.05000                         | ns    | 1,2   |
|  | 6                           | 266.67                 | 3.69998                      |                                      | 3.74998                              | 3.75000                    | 3.75002                              |  | 3.80002                         | ns    | 1,2   |
|  | 10                          | 333.33                 | 2.94997                      |                                      | 2.99997                              | 3.00000                    | 3.00003                              |  | 3.05003                         | ns    | 1,2   |
| 0  | 400.00                      | 2.45000                |                              | 2.50000                              | 2.50000                              | 2.50000                    |                                      | 2.55000                                  | ns                              | 1,2   |       |

## Clock Periods - Differential Outputs with Spread Spectrum Enabled

| SSC ON<br>-0.5%<br>Down<br>Spread | Synthesis<br>Error<br>(ppm) | Center<br>Freq.<br>MHz | Measurement Window           |                                      |                                      |                            |                                      |  |                                 | Units | Notes |
|-----------------------------------|-----------------------------|------------------------|------------------------------|--------------------------------------|--------------------------------------|----------------------------|--------------------------------------|--|---------------------------------|-------|-------|
|                                   |                             |                        | 1 Clock                      | 1us                                  | 0.1s                                 | 0.1s                       | 0.1s                                 | 1us                                      | 1 Clock                         |       |       |
|                                   |                             |                        | -c2c jitter<br>AbsPer<br>Min | -SSC<br>Short-Term<br>Average<br>Min | - ppm<br>Long-Term<br>Average<br>Min | 0 ppm<br>Period<br>Nominal | + ppm<br>Long-Term<br>Average<br>Max | +SSC<br>Short-<br>Term<br>Average<br>Max | +c2c<br>jitter<br>AbsPer<br>Max |       |       |
| DIF                               | 96                          | 99.75                  | 9.94906                      | 9.99906                              | 10.02406                             | 10.02506                   | 10.02603                             | 10.05103                                 | 10.10103                        | ns    | 1,2   |
|                                   | 19                          | 124.69                 | 7.94925                      | 7.99925                              | 8.01925                              | 8.02005                    | 8.02020                              | 8.04020                                  | 8.09020                         | ns    | 1,2   |
|                                   | 96                          | 133.00                 | 7.44930                      | 7.49930                              | 7.51805                              | 7.51880                    | 7.51952                              | 7.53827                                  | 7.58827                         | ns    | 1,2   |
|                                   | 10                          | 166.25                 | 5.94943                      | 5.99943                              | 6.01443                              | 6.01504                    | 6.01510                              | 6.03010                                  | 6.08010                         | ns    | 1,2   |
|                                   | 96                          | 199.50                 | 4.94953                      | 4.99953                              | 5.01203                              | 5.01253                    | 5.01301                              | 5.02551                                  | 5.07551                         | ns    | 1,2   |
|                                   | -98                         | 266.00                 | 3.69965                      | 3.74965                              | 3.75902                              | 3.75940                    | 3.75903                              | 3.76841                                  | 3.81841                         | ns    | 1,2   |
|                                   | 10                          | 332.50                 | 2.94972                      | 2.99972                              | 3.00722                              | 3.00752                    | 3.00755                              | 3.01505                                  | 3.06505                         | ns    | 1,2   |
|                                   | 96                          | 399.00                 | 2.44977                      | 2.49977                              | 2.50602                              | 2.50627                    | 2.50651                              | 2.51276                                  | 2.56276                         | ns    | 1,2   |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.<sup>2</sup>All ppm specifications are guaranteed with the assumption that the REF output is tuned to the exact target XTAL frequency.

## Differential Clock Tolerances, x1 = 14.31818MHz

## Clock Periods - Differential Outputs with Spread Spectrum Disabled

| SSC OFF<br>or SSC +/-<br>0.25%<br>Center<br>Spread | Synthesis<br>Error<br>(ppm) | Center<br>Freq.<br>MHz | Measurement Window           |                                      |                                      |                            |                                      |  |                                 | Units | Notes |
|--|-----------------------------|------------------------|------------------------------|--------------------------------------|--------------------------------------|----------------------------|--------------------------------------|--|---------------------------------|-------|-------|
|  |                             |                        | 1 Clock                      | 1us                                  | 0.1s                                 | 0.1s                       | 0.1s                                 | 1us                                      | 1 Clock                         |       |       |
|  |                             |                        | -c2c jitter<br>AbsPer<br>Min | -SSC<br>Short-Term<br>Average<br>Min | - ppm<br>Long-Term<br>Average<br>Min | 0 ppm<br>Period<br>Nominal | + ppm<br>Long-Term<br>Average<br>Max | +SSC<br>Short-<br>Term<br>Average<br>Max | +c2c<br>jitter<br>AbsPer<br>Max |       |       |
| DIF  | 35                          | 100.00                 | 9.94965                      |                                      | 9.99965                              | 10.00000                   | 10.00035                             |  | 10.05035                        | ns    | 1,2   |
|  | -114                        | 125.00                 | 7.95091                      |                                      | 8.00091                              | 8.00000                    | 7.99909                              |  | 8.04909                         | ns    | 1,2   |
|  | 35                          | 133.33                 | 7.44974                      |                                      | 7.49974                              | 7.50000                    | 7.50026                              |  | 7.55026                         | ns    | 1,2   |
|  | -104                        | 166.67                 | 5.95062                      |                                      | 6.00062                              | 6.00000                    | 5.99937                              |  | 6.04937                         | ns    | 1,2   |
|  | 35                          | 200.00                 | 4.94983                      |                                      | 4.99983                              | 5.00000                    | 5.00018                              |  | 5.05018                         | ns    | 1,2   |
|  | 42                          | 266.67                 | 3.69984                      |                                      | 3.74984                              | 3.75000                    | 3.75016                              |  | 3.80016                         | ns    | 1,2   |
|  | -104                        | 333.33                 | 2.95031                      |                                      | 3.00031                              | 3.00000                    | 2.99969                              |  | 3.04969                         | ns    | 1,2   |
|  | 35                          | 400.00                 | 2.44991                      |                                      | 2.49991                              | 2.50000                    | 2.50009                              |  | 2.55009                         | ns    | 1,2   |

## Clock Periods - Differential Outputs with Spread Spectrum Enabled

| SSC ON<br>-0.5%<br>Down<br>Spread | Synthesis<br>Error<br>(ppm) | Center<br>Freq.<br>MHz | Measurement Window           |                                      |                                      |                            |                                      |  |                                 | Units | Notes |
|-----------------------------------|-----------------------------|------------------------|------------------------------|--------------------------------------|--------------------------------------|----------------------------|--------------------------------------|--|---------------------------------|-------|-------|
|                                   |                             |                        | 1 Clock                      | 1us                                  | 0.1s                                 | 0.1s                       | 0.1s                                 | 1us                                      | 1 Clock                         |       |       |
|                                   |                             |                        | -c2c jitter<br>AbsPer<br>Min | -SSC<br>Short-Term<br>Average<br>Min | - ppm<br>Long-Term<br>Average<br>Min | 0 ppm<br>Period<br>Nominal | + ppm<br>Long-Term<br>Average<br>Max | +SSC<br>Short-<br>Term<br>Average<br>Max | +c2c<br>jitter<br>AbsPer<br>Max |       |       |
| DIF                               | 199                         | 99.75                  | 9.94906                      | 9.99906                              | 10.02406                             | 10.02506                   | 10.02706                             | 10.05206                                 | 10.10206                        | ns    | 1,2   |
|                                   | -100                        | 124.69                 | 7.94925                      | 7.99925                              | 8.01925                              | 8.02005                    | 8.01925                              | 8.03925                                  | 8.08925                         | ns    | 1,2   |
|                                   | 199                         | 133.00                 | 7.44930                      | 7.49930                              | 7.51805                              | 7.51880                    | 7.52029                              | 7.53904                                  | 7.58904                         | ns    | 1,2   |
|                                   | 10                          | 166.25                 | 5.94943                      | 5.99943                              | 6.01443                              | 6.01504                    | 6.01510                              | 6.03010                                  | 6.08010                         | ns    | 1,2   |
|                                   | 199                         | 199.50                 | 4.94953                      | 4.99953                              | 5.01203                              | 5.01253                    | 5.01353                              | 5.02603                                  | 5.07603                         | ns    | 1,2   |
|                                   | -140                        | 266.00                 | 3.69965                      | 3.74965                              | 3.75902                              | 3.75940                    | 3.75887                              | 3.76825                                  | 3.81825                         | ns    | 1,2   |
|                                   | 10                          | 332.50                 | 2.94972                      | 2.99972                              | 3.00722                              | 3.00752                    | 3.00755                              | 3.01505                                  | 3.06505                         | ns    | 1,2   |
|                                   | 199                         | 399.00                 | 2.44977                      | 2.49977                              | 2.50602                              | 2.50627                    | 2.50676                              | 2.51301                                  | 2.56301                         | ns    | 1,2   |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.<sup>2</sup>All ppm specifications are guaranteed with the assumption that the REF output is tuned to the exact target XTAL frequency.

## General SMBus serial interface information for the 9FG430

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address  $DC_{(H)}$
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the data byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**  
(see Note 2)
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address  $DC_{(H)}$
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address  $DD_{(H)}$
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends **Byte N + X - 1**
- IDT clock sends **Byte 0 through byte X (if  $X_{(H)}$  was written to byte 8)**.
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Write Operation |           |                      |
|-----------------------------|-----------|----------------------|
| Controller (Host)           |           | IDT (Slave/Receiver) |
| T                           | starT bit |                      |
| Slave Address $DC_{(H)}$    |           |                      |
| WR                          | WRite     |                      |
|                             |           | ACK                  |
| Beginning Byte = N          |           |                      |
|                             |           | ACK                  |
| Data Byte Count = X         |           |                      |
|                             |           | ACK                  |
| Beginning Byte N            | X Byte    |                      |
| ◊                           |           | ACK                  |
| ◊                           |           | ◊                    |
| ◊                           |           | ◊                    |
| Byte N + X - 1              |           | ◊                    |
|                             |           | ACK                  |
| P                           | stoP bit  |                      |

| Index Block Read Operation |                 |                      |
|----------------------------|-----------------|----------------------|
| Controller (Host)          |                 | IDT (Slave/Receiver) |
| T                          | starT bit       |                      |
| Slave Address $DC_{(H)}$   |                 |                      |
| WR                         | WRite           |                      |
|                            |                 | ACK                  |
| Beginning Byte = N         |                 |                      |
|                            |                 | ACK                  |
| RT                         | Repeat starT    |                      |
| Slave Address $DD_{(H)}$   |                 |                      |
| RD                         | ReaD            |                      |
|                            |                 | ACK                  |
|                            |                 | Data Byte Count = X  |
| ACK                        |                 |                      |
| ACK                        |                 | Beginning Byte N     |
| ◊                          |                 | ◊                    |
| ◊                          |                 | ◊                    |
| ◊                          |                 | ◊                    |
|                            |                 | Byte N + X - 1       |
| N                          | Not acknowledge |                      |
| P                          | stoP bit        |                      |

**SMBus Table: Device Control Register, READ/WRITE ADDRESS (DC/DD)**

| Byte 0 | Pin # | Name  | Control Function           | Type | 0  | 1               | Default |
|--------|-------|---|----------------------------|------|--|-----------------|---------|
| Bit 7  | 17    |   | FS3 <sup>1</sup>           | RW   | See Frequency Selection Table,<br>Page 1 |                 | Pin 17  |
| Bit 6  | 6     |   | FS2 <sup>1</sup>           | RW   |  |                 | Pin 6   |
| Bit 5  | 24    |   | FS1 <sup>1</sup>           | RW   |  |                 | Pin 24  |
| Bit 4  | 25    |   | FS0 <sup>1</sup>           | RW   |  |                 | Pin 25  |
| Bit 3  | 16    |   | Spread Enable <sup>1</sup> | RW   | Off                                      | On              | Pin 16  |
| Bit 2  | -     | Enable Software Control of Frequency, Spread Enable (Spread Type always Software Control) |                            | RW   | Hardware Select                          | Software Select | 0       |
| Bit 1  |       |   | DIF_STOP# drive mode       | RW   | Driven                                   | Hi-Z            | 0       |
| Bit 0  |       |   | SPREAD TYPE                | RW   | Down                                     | Center          | 0       |

**Notes:**

1. These bits reflect the state of the corresponding pins at power up, but may be written to if Byte 0, bit 2 is set to '1'. FS3 is the SEL14M\_25M# pin.

**SMBus Table: Output Enable Register**

| Byte 1 | Pin # | Name     | Control Function | Type | 0       | 1      | Default |
|--------|-------|----------|------------------|------|---------|--------|---------|
| Bit 7  | -     | Reserved |                  |      |         |        | 1       |
| Bit 6  | -     | DIF_3 EN | Output Enable    | RW   | Disable | Enable | 1       |
| Bit 5  | -     | DIF_2 EN | Output Enable    | RW   | Disable | Enable | 1       |
| Bit 4  | -     | Reserved |                  |      |         |        | 1       |
| Bit 3  | -     | Reserved |                  |      |         |        | 1       |
| Bit 2  | -     | DIF_1 EN | Output Enable    | RW   | Disable | Enable | 1       |
| Bit 1  | -     | DIF_0 EN | Output Enable    | RW   | Disable | Enable | 1       |
| Bit 0  | -     | Reserved |                  |      |         |        | 1       |

**SMBus Table: Output Stop Control Register**

| Byte 2 | Pin # | Name          | Control Function      | Type | 0        | 1         | Default |
|--------|-------|---------------|-----------------------|------|----------|-----------|---------|
| Bit 7  | -     | Reserved      |                       |      |          |           | 0       |
| Bit 6  | -     | DIF_3 STOP EN | Free Run/ Stop Enable | RW   | Free-run | Stop-able | 0       |
| Bit 5  | -     | DIF_2 STOP EN | Free Run/ Stop Enable | RW   | Free-run | Stop-able | 0       |
| Bit 4  | -     | Reserved      |                       |      |          |           | 0       |
| Bit 3  | -     | Reserved      |                       |      |          |           | 0       |
| Bit 2  | -     | DIF_1 STOP EN | Free Run/ Stop Enable | RW   | Free-run | Stop-able | 0       |
| Bit 1  | -     | DIF_0 STOP EN | Free Run/ Stop Enable | RW   | Free-run | Stop-able | 0       |
| Bit 0  | -     | Reserved      |                       |      |          |           | 0       |

**SMBus Table: Frequency Select Readback Register**

| Byte 3 | Pin # | Name                              | Control Function | Type | 0  | 1  | Default |
|--------|-------|-----------------------------------|------------------|------|--|----|---------|
| Bit 7  | 27    | SEL14M_25M# <sup>1</sup><br>(FS3) | State of pin 17  | R    | See Frequency Selection Table,<br>Page 1 |    | Pin 17  |
| Bit 6  | 6     | FS2 <sup>1</sup>                  | State of pin 6   | R    |  |    | Pin 6   |
| Bit 5  | 44    | FS1 <sup>1</sup>                  | State of pin 24  | R    |  |    | Pin 24  |
| Bit 4  | 45    | FS0 <sup>1</sup>                  | State of pin 25  | R    |  |    | Pin 25  |
| Bit 3  | 16    | SPREAD <sup>1</sup>               | State of pin 26  | R    | Off                                      | On | Pin 16  |
| Bit 2  |       |                                   | Reserved         |      |  |    | 0       |
| Bit 1  |       |                                   | Reserved         |      |  |    | 0       |
| Bit 0  |       |                                   | Reserved         |      |  |    | 0       |

**Notes:**

1. These bits reflect the state of the corresponding pins, regardless of whether software programming is enabled or not.

**SMBus Table: Vendor & Revision ID Register**

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7  | -     | RID3 | REVISION ID      | R    | - | - | 0       |
| Bit 6  | -     | RID2 |                  | R    | - | - | 0       |
| Bit 5  | -     | RID1 |                  | R    | - | - | 0       |
| Bit 4  | -     | RID0 |                  | R    | - | - | 0       |
| Bit 3  | -     | VID3 | VENDOR ID        | R    | - | - | 0       |
| Bit 2  | -     | VID2 |                  | R    | - | - | 0       |
| Bit 1  | -     | VID1 |                  | R    | - | - | 0       |
| Bit 0  | -     | VID0 |                  | R    | - | - | 1       |

**SMBus Table: DEVICE ID**

| Byte 5 | Pin # | Name | Control Function   | Type | 0 | 1 | Default |
|--------|-------|------|--------------------|------|---|---|---------|
| Bit 7  | -     | DID7 | Device ID = 01 hex | R    | - | - | 0       |
| Bit 6  | -     | DID6 |                    | R    | - | - | 0       |
| Bit 5  | -     | DID5 |                    | R    | - | - | 0       |
| Bit 4  | -     | DID4 |                    | R    | - | - | 0       |
| Bit 3  | -     | DID3 |                    | R    | - | - | 0       |
| Bit 2  | -     | DID2 |                    | R    | - | - | 0       |
| Bit 1  | -     | DID1 |                    | R    | - | - | 0       |
| Bit 0  | -     | DID0 |                    | R    | - | - | 1       |

**SMBus Table: Byte Count Register**

| Byte 6 | Pin # | Name | Control Function  | Type | 0 | 1 | Default |
|--------|-------|------|---|------|---|---|---------|
| Bit 7  | -     | BC7  | Writing to this register will<br>configure how many bytes will<br>be read back, default is 07 = 7<br>bytes. | RW   | - | - | 0       |
| Bit 6  | -     | BC6  |   | RW   | - | - | 0       |
| Bit 5  | -     | BC5  |   | RW   | - | - | 0       |
| Bit 4  | -     | BC4  |   | RW   | - | - | 0       |
| Bit 3  | -     | BC3  |   | RW   | - | - | 0       |
| Bit 2  | -     | BC2  |   | RW   | - | - | 1       |
| Bit 1  | -     | BC1  |   | RW   | - | - | 1       |
| Bit 0  | -     | BC0  |   | RW   | - | - | 1       |

**SMBus Table: Reserved Register**

| Byte 7 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7  | -     |      | Reserved         |      |   |   | 0       |
| Bit 6  | -     |      | Reserved         |      |   |   | 0       |
| Bit 5  | -     |      | Reserved         |      |   |   | 0       |
| Bit 4  | -     |      | Reserved         |      |   |   | 0       |
| Bit 3  | -     |      | Reserved         |      |   |   | 0       |
| Bit 2  | -     |      | Reserved         |      |   |   | 0       |
| Bit 1  | -     |      | Reserved         |      |   |   | 0       |
| Bit 0  | -     |      | Reserved         |      |   |   | 0       |

**SMBus Table: Reserved Register**

| Byte 8 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7  | -     |      | Reserved         |      |   |   | 0       |
| Bit 6  | -     |      | Reserved         |      |   |   | 0       |
| Bit 5  | -     |      | Reserved         |      |   |   | 0       |
| Bit 4  | -     |      | Reserved         |      |   |   | 0       |
| Bit 3  | -     |      | Reserved         |      |   |   | 0       |
| Bit 2  | -     |      | Reserved         |      |   |   | 0       |
| Bit 1  | -     |      | Reserved         |      |   |   | 0       |
| Bit 0  | -     |      | Reserved         |      |   |   | 0       |

**SMBus Table: M/N Programming Enable**

| Byte 9 | Pin # | Name       | Control Function | Type | 0       | 1      | Default |
|--------|-------|------------|------------------|------|---------|--------|---------|
| Bit 7  | -     | M/N_Enable | M/N Prog. Enable | RW   | Disable | Enable | 0       |
| Bit 6  | -     |            | Reserved         |      |         |        | 1       |
| Bit 5  | 5     | REFOUT_En  | REFOUT Enable    | RW   | Disable | Enable | 1       |
| Bit 4  | -     |            | Reserved         |      |         |        | 0       |
| Bit 3  | -     |            | Reserved         |      |         |        | 0       |
| Bit 2  | -     |            | Reserved         |      |         |        | 0       |
| Bit 1  | -     |            | Reserved         |      |         |        | 0       |
| Bit 0  | -     |            | Reserved         |      |         |        | 0       |

**SMBus Table: PLL Frequency Control Register**

| Byte 10 | Pin # | Name       | Control Function                | Type | 0   | 1 | Default |
|---------|-------|------------|---------------------------------|------|---|---|---------|
| Bit 7   | -     | PLL N Div8 | N Divider Prog bit 8            | RW   | The decimal representation of M and N Divider in Byte 10 and 11 will configure the PLL VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = $f_{XTAL} \times [N_{Div}(9:0)+8] / [M_{Div}(5:0)+2]$ . The user does NOT need to program these registers for standard frequencies. |   | X       |
| Bit 6   | -     | PLL N Div9 | N Divider Prog bit 9            | RW   |   |   | X       |
| Bit 5   | -     | PLL M Div5 | M Divider Programming bit (5:0) | RW   |   |   | X       |
| Bit 4   | -     | PLL M Div4 |                                 | RW   |   |   | X       |
| Bit 3   | -     | PLL M Div3 |                                 | RW   |   |   | X       |
| Bit 2   | -     | PLL M Div2 |                                 | RW   |   |   | X       |
| Bit 1   | -     | PLL M Div1 |                                 | RW   |   |   | X       |
| Bit 0   | -     | PLL M Div0 |                                 | RW   |   |   | X       |

**SMBus Table: PLL Frequency Control Register**

| Byte 11 | Pin # | Name       | Control Function  | Type | 0   | 1 | Default |
|---------|-------|------------|---|------|---|---|---------|
| Bit 7   | -     | PLL N Div7 | N Divider Programming<br>Byte11 bit(7:0) and Byte10<br>bit(7:6) | RW   | The decimal representation of M<br>and N Divider in Byte 10 and 11 will<br>configure the PLL VCO frequency.<br>Default at power up = latch-in or<br>Byte 0 Rom table. VCO Frequency<br>= fXTAL x [NDiv(9:0)+8] /<br>[MDiv(5:0)+2]. The user does NOT<br>need to program these resgisters<br>for standard frequencies. |   | X       |
| Bit 6   | -     | PLL N Div6 |   | RW   |   |   | X       |
| Bit 5   | -     | PLL N Div5 |   | RW   |   |   | X       |
| Bit 4   | -     | PLL N Div4 |   | RW   |   |   | X       |
| Bit 3   | -     | PLL N Div3 |   | RW   |   |   | X       |
| Bit 2   | -     | PLL N Div2 |   | RW   |   |   | X       |
| Bit 1   | -     | PLL N Div1 |   | RW   |   |   | X       |
| Bit 0   | -     | PLL N Div0 |   | RW   |   |   | X       |

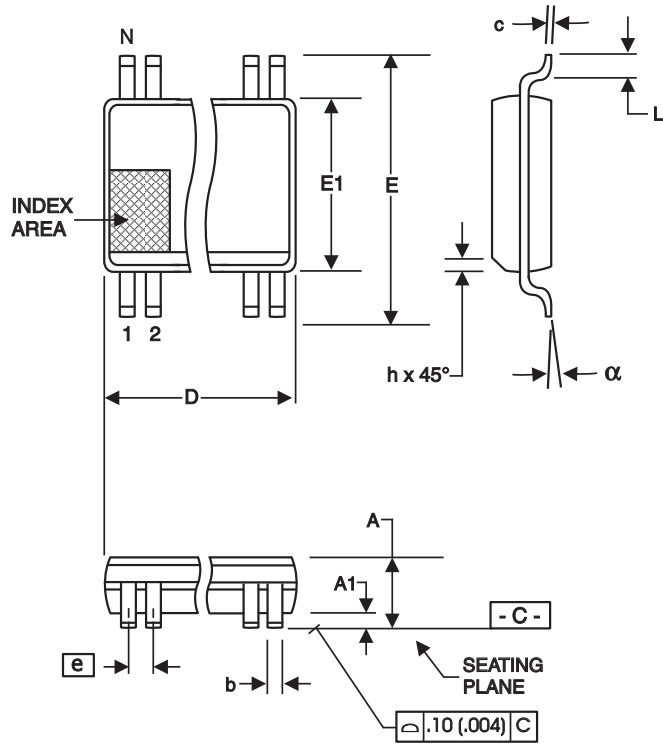
**SMBus Table: PLL Spread Spectrum Control Register**

| Byte 12 | Pin # | Name     | Control Function                        | Type | 0  | 1 | Default |
|---------|-------|----------|---|------|--|---|---------|
| Bit 7   | -     | PLL SSP7 | Spread Spectrum<br>Programming bit(7:0) | RW   | These Spread Spectrum bits in<br>Byte 12 and 13 will program the<br>spread percentage of PLL. The<br>user does not need to modify<br>these settings unless non-<br>standard spread amounts are<br>required. The part defaults to -<br>0.5% spread when spread is<br>enabled. |   | X       |
| Bit 6   | -     | PLL SSP6 |   | RW   |  |   | X       |
| Bit 5   | -     | PLL SSP5 |   | RW   |  |   | X       |
| Bit 4   | -     | PLL SSP4 |   | RW   |  |   | X       |
| Bit 3   | -     | PLL SSP3 |   | RW   |  |   | X       |
| Bit 2   | -     | PLL SSP2 |   | RW   |  |   | X       |
| Bit 1   | -     | PLL SSP1 |   | RW   |  |   | X       |
| Bit 0   | -     | PLL SSP0 |   | RW   |  |   | X       |

**SMBus Table: PLL Spread Spectrum Control Register**

| Byte 13 | Pin # | Name      | Control Function                         | Type | 0  | 1 | Default |
|---------|-------|-----------|--|------|--|---|---------|
| Bit 7   | -     |           | Reserved                                 |      |  |   | 0       |
| Bit 6   | -     | PLL SSP14 | Spread Spectrum<br>Programming bit(14:8) | RW   | These Spread Spectrum bits in<br>Byte 12 and 13 will program the<br>spread percentage of PLL. The<br>user does not need to modify<br>these settings unless non-<br>standard spread amounts are<br>required. The part defaults to -<br>0.5% spread when spread is<br>enabled. |   | X       |
| Bit 5   | -     | PLL SSP13 |  | RW   |  |   | X       |
| Bit 4   | -     | PLL SSP12 |  | RW   |  |   | X       |
| Bit 3   | -     | PLL SSP11 |  | RW   |  |   | X       |
| Bit 2   | -     | PLL SSP10 |  | RW   |  |   | X       |
| Bit 1   | -     | PLL SSP9  |  | RW   |  |   | X       |
| Bit 0   | -     | PLL SSP8  |  | RW   |  |   | X       |

### 28-Pin SSOP Package Drawing and Dimensions



209 mil SSOP

| SYMBOL   | In Millimeters<br>COMMON DIMENSIONS |      | In Inches<br>COMMON DIMENSIONS |      |
|----------|-------------------------------------|------|--------------------------------|------|
|          | MIN                                 | MAX  | MIN                            | MAX  |
| A        | --                                  | 2.00 | --                             | .079 |
| A1       | 0.05                                | --   | .002                           | --   |
| A2       | 1.65                                | 1.85 | .065                           | .073 |
| b        | 0.22                                | 0.38 | .009                           | .015 |
| c        | 0.09                                | 0.25 | .0035                          | .010 |
| D        | SEE VARIATIONS                      |      | SEE VARIATIONS                 |      |
| E        | 7.40                                | 8.20 | .291                           | .323 |
| E1       | 5.00                                | 5.60 | .197                           | .220 |
| e        | 0.65 BASIC                          |      | 0.0256 BASIC                   |      |
| L        | 0.55                                | 0.95 | .022                           | .037 |
| N        | SEE VARIATIONS                      |      | SEE VARIATIONS                 |      |
| $\alpha$ | 0°                                  | 8°   | 0°                             | 8°   |

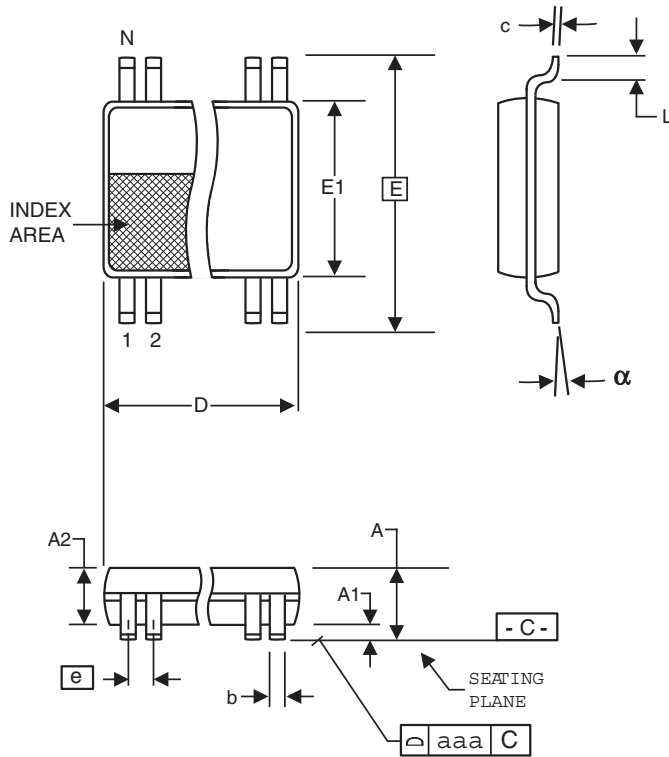
VARIATIONS

| N  | D mm. |       | D (inch) |      |
|----|-------|-------|----------|------|
|    | MIN   | MAX   | MIN      | MAX  |
| 28 | 9.90  | 10.50 | .390     | .413 |

Reference Doc.: JEDEC Publication 95, MO-150

10-0033

## 28-Pin TSSOP Package Drawing and Dimensions



4.40 mm. Body, 0.65 mm. Pitch TSSOP

(173 mil) (25.6 mil)

| SYMBOL   | In Millimeters    |      | In Inches         |      |
|----------|-------------------|------|-------------------|------|
|          | COMMON DIMENSIONS |      | COMMON DIMENSIONS |      |
|          | MIN               | MAX  | MIN               | MAX  |
| A        | --                | 1.20 | --                | .047 |
| A1       | 0.05              | 0.15 | .002              | .006 |
| A2       | 0.80              | 1.05 | .032              | .041 |
| b        | 0.19              | 0.30 | .007              | .012 |
| c        | 0.09              | 0.20 | .0035             | .008 |
| D        | SEE VARIATIONS    |      | SEE VARIATIONS    |      |
| E        | 6.40 BASIC        |      | 0.252 BASIC       |      |
| E1       | 4.30              | 4.50 | .169              | .177 |
| e        | 0.65 BASIC        |      | 0.0256 BASIC      |      |
| L        | 0.45              | 0.75 | .018              | .030 |
| N        | SEE VARIATIONS    |      | SEE VARIATIONS    |      |
| $\alpha$ | 0°                | 8°   | 0°                | 8°   |
| aaa      | --                | 0.10 | --                | .004 |

## VARIATIONS

| N  | D mm. |      | D (inch) |      |
|----|-------|------|----------|------|
|    | MIN   | MAX  | MIN      | MAX  |
| 28 | 9.60  | 9.80 | .378     | .386 |

Reference Doc.: JEDEC Publication 95, MO-153

10-0035

## Ordering Information

| Part / Order Number | Shipping Packaging | Package      | Temperature  |
|---------------------|--------------------|--------------|--------------|
| 9FG430AFLF          | Tubes              | 28-pin SSOP  | 0 to +70°C   |
| 9FG430AFLFT         | Tape and Reel      | 28-pin SSOP  | 0 to +70°C   |
| 9FG430AFILF         | Tubes              | 28-pin SSOP  | -40 to +85°C |
| 9FG430AFILFT        | Tape and Reel      | 28-pin SSOP  | -40 to +85°C |
| 9FG430AGLF          | Tubes              | 28-pin TSSOP | 0 to +70°C   |
| 9FG430AGLFT         | Tape and Reel      | 28-pin TSSOP | 0 to +70°C   |
| 9FG430AGILF         | Tubes              | 28-pin TSSOP | -40 to +85°C |
| 9FG430AGILFT        | Tape and Reel      | 28-pin TSSOP | -40 to +85°C |

“LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

“A” is the device revision designator (will not correlate with the datasheet revision).

**Revision History**

| <b>Rev.</b> | <b>Issue Date</b> | <b>Who</b> | <b>Description</b>  | <b>Page #</b> |
|-------------|-------------------|------------|---|---------------|
| 0.1         | 7/13/2010         | RDW        | New datasheet.  |               |
| A           | 7/13/2010         | RDW        | Release   |               |
| B           | 7/20/2010         | RDW        | 1. Added PPM tables to DS for both 25M and 14.318M inputs<br>2. Added Test load figures   |               |
| C           | 8/25/2010         | RDW        | 1. Updated/reformatted Electrical Tables<br>2. Corrected Features/Benefits and General Description<br>3. Updated pull up ^ and pull down v indicators.<br>4. Updated termination figures to include Fig. 5 for REF output, merged test load figures into these figures. | 1, Various    |
| D           | 4/4/2017          | RDW        | 1. Corrected Byte 5 Device ID from 43 hex to 01 hex   | 13            |

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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

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