THE DATASHEET OF

66AK2G12ABY100

66AK2G1x Multicore DSP+Arm KeyStone II System-on-Chip (SoC)

1 Device Overview

1.1 Features

Processor cores:

- Arm® Cortex®-A15 microprocessor unit (Arm A15) subsystem at up to 1000 MHz
  - Supports full Implementation of Armv7-A architecture instruction set
  - Integrated SIMDv2 (Arm® Neon™ Technology) and VFPv4 (Vector Floating Point)
  - 32KB of L1 program memory
  - 32KB of L1 data memory
  - 512KB of L2 memory
  - Error Correction Code (ECC) protection for L1 data memory ECC for L2 memory
  - Parity protection for L1 program memory
  - Global Timebase Counter (GTC)
    - 64-Bit free-running counter that provides timebase for Arm A15 internal timers
    - Compliant to Armv7 MPCore Architecture for Generic Timers
- C66x fixed- and floating-point VLIW DSP subsystem at up to 1000 MHz
  - Fully object-code compatible With C67x+ and C64x+ cores
  - 32KB of L1 program memory
  - 32KB of L1 data memory
  - 1024KB of L2 configurable as L2 RAM or cache
  - Error detection for L1 program memory
  - ECC for L1 data memory
  - ECC for L2 data memory

Industrial subsystem:

- Up to Two Programmable Real-Time Unit and Industrial Communication Subsystems (PRU-ICSS), each supports:
  - Two Programmable Real-Time Units (PRUs) with enhanced multiplier and accumulator, each PRU supports:
    - 16KB of program memory With ECC
    - 8KB of data memory With ECC
    - CRC32 and CRC16 hardware accelerator
    - 20 × enhanced GPIO
    - Serial Capture Unit (SCU), supporting direct connection, 16-bit parallel capture, 28-bit shift, MII_RT, EnDat 2.2 protocol and Sigma-Delta demodulation
    - Scratch pad and XFR direct connect
  - 64KB of general-purpose memory With ECC
  - One Ethernet MII_RT module with two MII ports configurable for connection with each PRU; supports multiple industrial communication protocols
  - Industrial Ethernet Peripheral (IEP) to manage and generate industrial Ethernet functions
  - Built-In Universal Asynchronous Receiver and Transmitter (UART) 16550, with a dedicated 192-MHz clock to support 12-Mbps PROFIBUS®
  - Built-In industrial Ethernet 64-Bit timer
  - Built-In enhanced capture module (eCAP)

Memory subsystem:

- Multicore Shared Memory Controller (MSMC) with 1024KB of shared L2 RAM
  - Provides high-performance interconnect to internal shared SRAM and DDR EMIF for both Arm A15 and C66x Access
  - Supports Arm I/O coherency where Arm A15 is cache coherent to other system masters accessing the MSMC-SRAM or DDR EMIF
  - Supports ECC on SRAM
- Up to 36-Bit DDR External Memory Interface (EMIF)
  - Supports DDR3L at up to 1066 MT/s
  - Supports 4-GB memory address range
  - Supports 32-Bit SDRAM data bus with 4-bit ECC
  - Supports 16-Bit and 32-Bit SDRAM data bus without ECC
- General-Purpose Memory Controller (GPMC)
  - Flexible 8- and 16-Bit asynchronous memory interface with up to four chip selects
  - Supports NOR, Muxed-NOR, SRAM
  - Supports general-purpose memory-port expansion with the following modes:
    - Asynchronous read and write access
    - Asynchronous read page access (4-, 8-, 16-Word16)
    - Synchronous read and write access
    - Synchronous read burst access without wrap capability (4-, 8-, 16-Word16)

Network Subsystem (NSS):

- Ethernet MAC (EMAC) subsystem
  - One-port Gigabit Ethernet: RMII, MII, RGMII
  - Supports 10-, 100-, 1000-Mbps full duplex
  - Supports 10-, 100-Mbps half duplex

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

  - Supports Ethernet Audio Video Bridging (eAVB)
  - Maximum frame size 2016 Bytes (2020 Bytes with VLAN)
  - Eight priority level QOS support (802.1p)
  - IEEE 1588v2 (2008 Annex D, Annex E, and Annex F) to facilitate Audio Video Bridging 802.1AS Precision Time Protocol (PTP)
  - CPTS module with timestamping support for IEEE 1588v2
  - DSCP priority mapping (IPv4 and IPv6)
  - MDIO module for PHY management
  - Enhanced statistics collection
- Navigator Subsystem (NAVSS)
  - Built-In packet DMA controller for optimized network processing
  - Built-In Queue Manager (QM) for optimized network processing
    - Supports up to 128 queues
    - 2048 buffers supported in internal queue RAM
- Crypto Engine (SA) supports:
  - Crypto Function Library for AES, DES, 3DES, SHA1, MD5, SHA2-224 and SHA2-256 Operations
  - Block data encryption supported through hardware cores
    - AES with 128-, 192-, and 256-Bit Key supports
    - DES and 3DES with 1, 2, or 3 Different Key support
  - Programmable Mode Control Engine (MCE)
  - Public Key Accelerator (PKA) with elliptic curve cryptography
  - Elliptic Curve Diffie–Hellman (ECDH) based key exchange and digital signature (ECDSA) applications
  - Authentication for SHA1, MD5, SHA2-224 and SHA2-256
  - Keyed HMAC operation through hardware core
  - True Random Number Generator (TRNG)

Display Subsystem:

- Supports one video pipe with in-loop scaling, color space
- Conversion and background color overlay
- Input data format: BITMAP, RGB16, RGB24, RGB32, ARGB16, ARGB32, YUV420, YUV422, and RGB565-A8
- Supported display interfaces:
  - MIPI® DPI 2.0 parallel interface
  - RFBI (MIPI-DBI 2.0) up to QVGA at 30fps
  - BT.656 4:2:2
  - BT.1120 4:2:2 up to 1920 × 1080 at 30fps
- In-loop scaling capability
- LCD interface supports:
  - Active Matrix (TFT)
  - Passive Matrix (STN)
  - Grayscale
  - TDM
  - AC Bias Control
  - Dither
  - CPR

Asynchronous Audio Sample Rate Converter (ASRC)

- High performance asynchronous sample rate converter with 140 dB Signal-to-Noise (SNR)
- Up to 8 stereo streams (16 audio channels)
- Automatically sensing / detection of input sample frequencies
- Attenuation of sampling clock jitter
- 16-, 18-, 20-, 24-Bit data input/output
- Audio sample rates from 8 kHz to 216 kHz
- Input/output sampling ratios from 16:1 to 1:16
- Group mode, where multiple ASRC blocks use the same timing loop for input or output
- Linear phase FIR filter
- Controllable soft mute
- Independent clock generator, and rate and stamp generator, for each input and output clock zone
- Separate DMA events for input and output, for each channel and group

High-speed serial interfaces:

- PCI Express® 2.0 port with integrated PHY:
  - Single lane Gen2-compliant port
  - Root Complex (RC) and End Point (EP) modes
- Up to two USB 2.0 High-Speed dual-role ports with Integrated PHYs, support:
  - Dual-role-device (DRD) Capability with:
    - USB 2.0 peripheral (or device) at HS (480Mbps) and FS (12Mbps) speeds
    - USB 2.0 host at HS (480Mbps), FS (12Mbps), and LS (1.5Mbps) speeds
    - USB 2.0 static peripheral and static host operations
  - xHCI controller with the following features:
    - Compatible to the xHCI specification (revision 1.1) in host mode
    - All modes of transfer (control, bulk, interrupt, and isochronous)
    - 15 transmit (TX), 15 receive (RX) endpoints (EPs), and one bidirectional endpoint (EP0)

Flash media interfaces:

- QSPI™ with XIP and up to four chip selects, supports:
  - Memory-mapped direct mode of operation for performing FLASH data transfers and executing code from FLASH memory (XIP)
  - Supports up to 96 MHz
  - Internal SRAM buffer with ECC

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  - High speed read data capture mechanism
- Two Multimedia Card (MMC) and Secure Digital (SD) ports
  - Supports JEDEC JESD84 v4.5-A441 and SD3.0 physical layer with SDA3.00 standards
  - MMC0 supports 3.3-V I/O for:
    - SD DS and HS mode
    - eMMC mode HS-SDR up to 48 MHz
  - MMC1 supports 1.8-V I/O modes for eMMC, including HS-SDR and DDR at up to 48 MHz with 4- and 8-Bit bus width

Audio peripherals:

- Three Multichannel Audio Serial Port (McASP) peripherals
  - Transmit and receive clocks up to 50 MHz
  - Two independent clock zones and independent transmit and receive clocks per McASP
  - Up to 16-, 10-, 6-serial data pins for McASP0, McASP1, and McASP2, respectively
  - Supports TDM, I2S, and similar formats
  - Supports DIT mode
  - Built-In FIFO buffers for optimized system traffic
- Multichannel Buffered Serial Port (McBSP)
  - Transmit and receive clocks up to 50 MHz
  - Two clock zones and two serial-data pins
  - Supports TDM, I2S, and similar formats

Real-time control interfaces:

- Six Enhanced High Resolution Pulse Width Modulation (eHRPWM) Modules, Each Counter supports:
  - Dedicated 16-Bit Time-Base with Period and Frequency Control
  - Two independent PWM outputs with single edge operation
  - Two independent PWM outputs with dual-edge symmetric operation
  - One independent PWM output with dual-edge asymmetric operation
- Two 32-Bit Enhanced Capture Modules (eCAP):
  - Supports one capture input or one auxiliary PWM output configuration options
  - 4-Event time-stamp registers (Each 32-Bits)
  - Interrupt on either of the four events
- Three 32-Bit Enhanced Quadrature Pulse Encoder Modules (eQEP), each supports:
  - Quadrature decoding
  - Position counter and control unit for position measurement
  - Unit time base for speed and frequency measurement

General connectivity:

- Two Controller Area Network (CAN) Ports
  - Supports CAN v2.0 Part A, B (ISO 11898-1) protocol
  - Bit rates up to 1 Mbps
  - Dual clock source
  - ECC protection for message RAM
- One Media Local Bus (MLB)
  - Supports both 3-pin (up to MOST50, 1024 × Fs) and 6-pin (up to MOST150, 2048 × Fs) versions of MediaLB® Physical layer specification v4.2
  - Supports all types of data transfer over 64 logical channels (synchronous stream, isochronous, asynchronous packet, control message)
  - Supports 3-wire MOST 150 protocol
- Three Inter-Integrated Circuit (I^2C) interfaces, each supports:
  - Standard (up to 100 kHz) and Fast (up to 400 kHz) modes
  - 7-Bit addressing mode
  - Supports EEPROM size up to 4Mbit
- Four Serial Peripheral Interfaces (SPI), each supports:
  - Operates at up to 50 MHz in master mode and 25 MHz in slave mode
  - Two chip selects
- Three UART interfaces
  - All UARTs are 16C750-compatible and operate at up to 3M baud
  - UART0 supports 8 pins with full modem control, with DSR, DTR, DCD, and RI signals
  - UART1 and UART2 are 4-pin interfaces
- General-Purpose I/O (GPIO)
  - Up to 212 GPIOs muxed with other interfaces
  - Can be configured as interrupt pins

Timers and miscellaneous modules:

- Seven 64-Bit timers:
  - Two 64-Bit timers dedicated to Arm A15 and DSP cores (one timer per core)
    - Watchdog and General-Purpose (GP)
  - Four 64-Bit timers are shared for general purposes
  - Each 64-Bit timer can be configured as two individual 32-Bit timers
  - One 64-Bit timer dedicated for PMMC
  - Two timers input/output pin pairs
- Interprocessor communication with:
  - Message manager to facilitate multiprocessor access to the PMMC:
    - Provides hardware acceleration for pushing and popping messages to/from logical queues
    - Supports up to 64 queues and 128 messages
  - Semaphore module with up to 64 independent semaphores and 16 masters (device cores)
- EDMA with 128 (2 × 64) channels and

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1024 (2 × 512) PaRAM entries

Keystone II System on Chip (SoC) architecture:

- Security
  - Supports General-Purpose (GP) and High-Secure (HS) devices
  - Supports secure boot
  - Supports customer secondary keys
  - 4KB of One-Time Programmable (OTP) ROM for customer keys
- Power management
  - Integrated Power Management Microcontroller (PMMC) technology
- Supports primary boot from UART, I^2C, SPI, GPMC, SD or eMMC, USB device firmware upgrade v1.1, PCIe®, and Ethernet interfaces
- Keystone II debug architecture with integrated Arm CoreSight™ support and trace capability

Operating Temperature (T_J):

- –40°C to 125°C (Industrial Extended)
- –40°C to 105°C (Extended)
- 0°C to 90°C (Commercial)

1.2 Applications

- Industrial Communications and Controls
- Home Audio
- Professional Audio
- Protection Relays
- Industrial Transport

1.3 Description

66AK2G1x is a family of heterogeneous multicore System-on-Chip (SoC) devices based on TI's field-proven Keystone II (KS2) architecture. These devices address applications that require both DSP and Arm performance, with integration of high-speed peripheral and memory interfaces, hardware acceleration for network and cryptography functions, and high-level operating systems (HLOS) support.

Similar to existing KS2-based SoC devices, the 66AK2G1x enables both the DSP and Arm cores to master all memory and peripherals in the system. This architecture facilitates maximum software flexibility where either DSP- or Arm-centric system designs can be achieved.

The 66AK2G1x significantly improves device reliability by extensively implementing error correction code (ECC) in processor cores, shared memory, embedded memory in modules, and external memory interfaces. Full analysis of soft error rate (SER) and power-on-hours (POH) shows that the designated 66AK2G1x parts satisfy a wide range of industrial requirements.

Accompanied by the new Processor SDK, the 66AK2G1x development platform enables unprecedented ease-of-use with main line open source Linux, Code Composer Studio™ (CCS) - Integrated Development Environment (IDE), a wide range of OS-independent device drivers, as well as TI-RTOS that enables seamless task management across processor cores. The device also features advanced debug and trace technology with the latest innovations from TI and Arm, such as system trace and seamless integration of the Arm CoreSight components.

Secure boot can also be made available for anticloning and illegal software update protection. For more information about secure boot, contact your TI sales representative.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
66AK2G12	FCBGA (625)	21.0 mm × 21.0 mm

(1) For more information, see Section 9, *Mechanical Packaging and Orderable Information*.

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1.4 Functional Block Diagram

Figure 1-1 is a block diagram of the device.

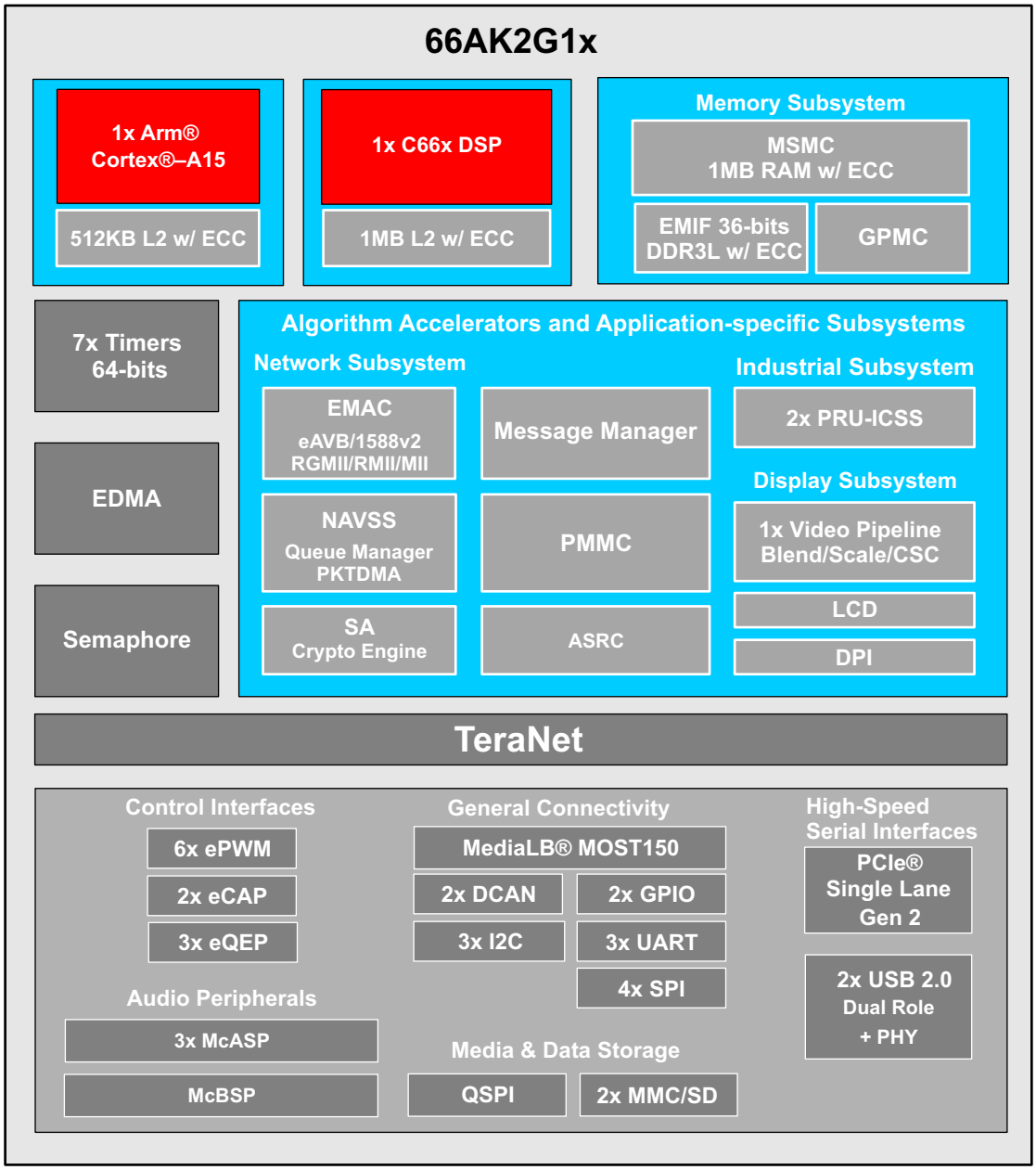

Figure 1-1. Functional Block Diagram

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2 Revision History

Changes from March 7, 2019 to December 15, 2019 (from E Revision (March 2019) to F Revision) **Page**

- **GLOBAL:** Removed all automotive references 1
- Updated Applications section 4
- Added reminders to disable unused pulls and RX pads in Section 4.2, *Pin Attributes* 40
- Updated Section 8.2, Tools and Software and Section 8.3, Documentation Support 224

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3 Device Comparison

Table 3-1 lists the features of the 66AK2G1x devices.

Table 3-1. Device Comparison

FEATURES	REFERENCE NAME	66AK2G12
PROCESSORS AND ACCELERATORS		
Speed Grades		See Table 5-1
Arm Cortex-A15 Microprocessor Subsystem	Arm A15	Yes
C66x VLIW Digital Signal Processor	C66x	Yes
Power Management Micro Controller	PMMC	Yes
Display Subsystem	DSS	Yes
PROGRAM AND DATA STORAGE		
Multicore Shared Memory Controller	MSMC	Up to 1MB (On-Chip Shared SRAM With ECC)
General-Purpose Memory Controller	GPMC	Up to 1GB
DDR External Memory Interface	EMIF	Up to 4GB (32-Bit data)
	SECDED/ECC	Yes
PERIPHERALS		
Dual Controller Area Network Interface	DCAN	2
Enhanced Direct Memory Access	EDMA	Yes
Network Subsystem	EMAC	RMII, MII, RGMII With eAVB
	NAVSS	PKTDMA and QM
	SA	Yes
General-Purpose I/O	GPIO	Up to 212
Inter-Integrated Circuit Interface	I2C	3
Message Manager	MSGMGR	Yes
Semaphore	SEM	Yes
Media Local Bus Subsystem	MLB	Yes (3-pin or 6-pin Modes)
Multichannel Buffered Serial Port	McBSP	Yes
Audio Asynchronous Sample Rate Converter	ASRC	Yes
Multichannel Audio Serial Port	McASP0	16 Serializers
	McASP1	10 Serializers
	McASP2	6 Serializers
MultiMedia Card, Secure Digital Interface (MMC/SD)	MMC0	eMMC, SD (3.3 V) - 8-bits
	MMC1	eMMC (1.8 V) - 8-bits
PCI Express 2.0 Port with Integrated PHY	PCIESS	Yes (Single-Lane Mode)
Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem	PRU-ICSS	2
Serial Peripheral Interface	SPI	4
Quad SPI	QSPI	Yes
General-Purpose Timers	TIMER_1 to TIMER_4	4
General-Purpose or Watchdog Timer Dedicated to Arm	TIMER_5	1
General-Purpose or Watchdog Timer Dedicated to DSP	TIMER_0	1
Dedicated to PMMC Timer	TIMER_6	1
Enhanced PWM Module	ePWM	6
Enhanced Capture Module	eCAP	2
Enhanced Quadrature Encoder Pulse Module	eQEP	3
Universal Asynchronous Receiver and Transmitter	UART	3

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Table 3-1. Device Comparison (continued)

FEATURES	REFERENCE NAME	66AK2G12
Universal Serial Bus (USB2.0) High Speed Dual-Role-Device (DRD) Ports with PHY	USB	2

3.1 Related Products

Digital Signal Processors DSPs bring computing performance, real-time processing, and power efficiency to diverse applications ranging from sensors to servers. Our product range spans high-performance real-time needs, to power-efficient processors with industry-leading lowest active power needs. Choose one of the following scalable solutions.

C6000 Multicore DSP + Arm SoC TI DSP + Arm processors include a wide range of device choices that deliver the highest performance at the lowest power levels and costs. TI DSP + Arm solutions range from single core Arm9 + C674x DSP to quad-core Arm Cortex-A15 + 8xC66x DSP cores.

66AK2x Multicore DSP + Arm Processors

Companion Products for 66AKG0x/66AKG1x Review products that are frequently purchased or used in conjunction with this product.

Reference Designs for 66AKG0x/66AKG1x TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump-start your system design, all TI Designs include schematic or block diagrams, BOMs and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

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4 Terminal Configuration and Functions

NOTE

The terms 'ball', 'pin', and 'terminal' are used interchangeably throughout the document. An attempt is made to use 'ball' only when referring to the physical package.

4.1 Pin Diagram

Figure 4-1 shows the ball locations for the 625 plastic ball grid array (FCBGA) package that are used in conjunction with Table 4-1 through Table 4-27 to locate signal names and ball grid numbers.

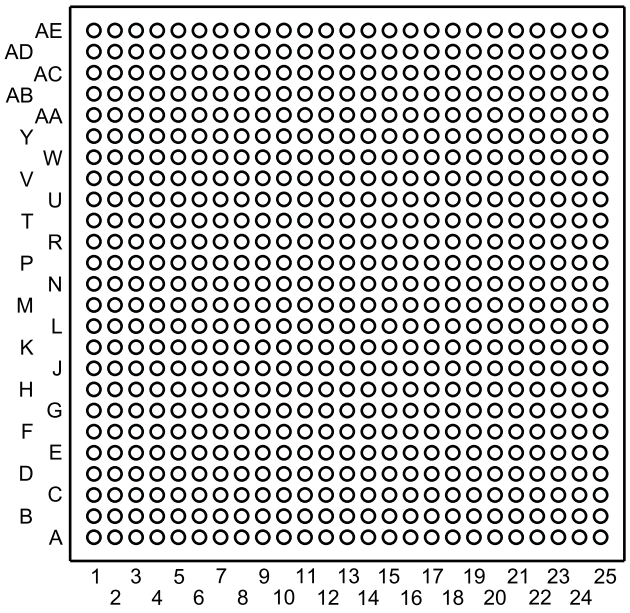

Figure 4-1. ABY FCBGA-N625 Package (Bottom View)

4.2 Pin Attributes

Table 4-1 describes the terminal characteristics and the signals multiplexed on each ball.

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Table 4-1. Pin Attributes

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
C17	AUDOSC_IN	AUDOSC_IN	0	I			0	1.8 V	DVDD18		Analog		
A17	AUDOSC_OUT	AUDOSC_OUT	0	O			0	1.8 V	DVDD18		Analog		
N6	AVDDA_ARMPLL	AVDDA_ARMPLL		PWR									
W20	AVDDA_DDRPLL	AVDDA_DDRPLL		PWR									
N20	AVDDA_DSSPLL	AVDDA_DSSPLL		PWR									
G8	AVDDA_ICSSPLL	AVDDA_ICSSPLL		PWR									
M19	AVDDA_MAINPLL	AVDDA_MAINPLL		PWR									
G14	AVDDA_NSSPLL	AVDDA_NSSPLL		PWR									
G10	AVDDA_UARTPLL	AVDDA_UARTPLL		PWR									
Y3	BOOTCOMPLETE	BOOTCOMPLETE	0	OZ	PD	PD	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	
L21	CPTS_REFCLK_N	CPTS_REFCLK_N	0	I			0	1.8 V	DVDD18		LVDS		
K21	CPTS_REFCLK_P	CPTS_REFCLK_P	0	I			0	1.8 V	DVDD18		LVDS		
J10, J14, J16, K11, K13, K15, K17, K9, L10, L12, L14, L16, L18, M11, M13, M15, M17, M9, N10, N12, N14, N16, P11, P13, P15, P17, P9, R10, R12, R14, R16, R18, R8, T11, T15, T17, T9, U16	CVDD	CVDD		PWR									
J12, M5, N18, N8, T13	CVDD1	CVDD1		PWR									
R5	DCAN0_RX	DCAN0_RX	0	I	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO1_57	3	IOZ									0
P5	DCAN0_TX	DCAN0_TX	0	OZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO1_56	3	IOZ									0
AC13	DDR3_CASn	DDR3_CASn	0	OZ	OFF	DRIVE 1 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
Y11	DDR3_CBDQM	DDR3_CBDQM	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AD12	DDR3_CBDQS_N	DDR3_CBDQS_N	0	IOZ	PU	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AE12	DDR3_CBDQS_P	DDR3_CBDQS_P	0	IOZ	PD	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AE13	DDR3_RASn	DDR3_RASn	0	OZ	OFF	DRIVE 1 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
Y18	DDR3_RESETn	DDR3_RESETn	0	OZ	OFF	DRIVE 0 (OFF)	0	1.35 V	DVDD_DDR		SSTL		
Y9	DDR3_VREFSSTL	DDR3_VREFSSTL	0	A			0	0.5 x DVDD_DDR	DVDD_DDR		Analog		
Y13	DDR3_WEn	DDR3_WEn	0	OZ	OFF	DRIVE 1 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
AC15	DDR3_A00	DDR3_A00	0	OZ	OFF	DRIVE 0 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
Y15	DDR3_A01	DDR3_A01	0	OZ	OFF	DRIVE 0 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AC16	DDR3_A02	DDR3_A02	0	OZ	OFF	DRIVE 0 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AA15	DDR3_A03	DDR3_A03	0	OZ	OFF	DRIVE 0 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AB16	DDR3_A04	DDR3_A04	0	OZ	OFF	DRIVE 0 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AE17	DDR3_A05	DDR3_A05	0	OZ	OFF	DRIVE 0 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AC14	DDR3_A06	DDR3_A06	0	OZ	OFF	DRIVE 0 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AB15	DDR3_A07	DDR3_A07	0	OZ	OFF	DRIVE 0 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AC17	DDR3_A08	DDR3_A08	0	OZ	OFF	DRIVE 0 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AB17	DDR3_A09	DDR3_A09	0	OZ	OFF	DRIVE 0 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AB14	DDR3_A10	DDR3_A10	0	OZ	OFF	DRIVE 0 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AA16	DDR3_A11	DDR3_A11	0	OZ	OFF	DRIVE 0 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AA17	DDR3_A12	DDR3_A12	0	OZ	OFF	DRIVE 0 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AA12	DDR3_A13	DDR3_A13	0	OZ	OFF	DRIVE 0 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
Y17	DDR3_A14	DDR3_A14	0	OZ	OFF	DRIVE 0 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
Y16	DDR3_A15	DDR3_A15	0	OZ	OFF	DRIVE 0 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AA14	DDR3_BA0	DDR3_BA0	0	OZ	OFF	DRIVE 0 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AB13	DDR3_BA1	DDR3_BA1	0	OZ	OFF	DRIVE 0 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AD17	DDR3_BA2	DDR3_BA2	0	OZ	OFF	DRIVE 0 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AA11	DDR3_CB00	DDR3_CB00	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AB11	DDR3_CB01	DDR3_CB01	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AC11	DDR3_CB02	DDR3_CB02	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AC12	DDR3_CB03	DDR3_CB03	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AD13	DDR3_CEn0	DDR3_CEn0	0	OZ	OFF	DRIVE 1 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
AB18	DDR3_CKE0	DDR3_CKE0	0	OZ	OFF	DRIVE 0 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AD15	DDR3_CLKOUT_N0	DDR3_CLKOUT_N0	0	OZ	OFF		0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AD16	DDR3_CLKOUT_N1	DDR3_CLKOUT_N1	0	OZ	OFF		0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AE15	DDR3_CLKOUT_P0	DDR3_CLKOUT_P0	0	OZ	OFF		0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AE16	DDR3_CLKOUT_P1	DDR3_CLKOUT_P1	0	OZ	OFF		0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AD2	DDR3_D00	DDR3_D00	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
Y4	DDR3_D01	DDR3_D01	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AC3	DDR3_D02	DDR3_D02	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AC2	DDR3_D03	DDR3_D03	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AE3	DDR3_D04	DDR3_D04	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AA4	DDR3_D05	DDR3_D05	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AD3	DDR3_D06	DDR3_D06	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AB3	DDR3_D07	DDR3_D07	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AA6	DDR3_D08	DDR3_D08	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
Y7	DDR3_D09	DDR3_D09	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
Y6	DDR3_D10	DDR3_D10	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AC5	DDR3_D11	DDR3_D11	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AB6	DDR3_D12	DDR3_D12	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
Y5	DDR3_D13	DDR3_D13	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AC4	DDR3_D14	DDR3_D14	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AB5	DDR3_D15	DDR3_D15	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AB7	DDR3_D16	DDR3_D16	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AB8	DDR3_D17	DDR3_D17	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AC7	DDR3_D18	DDR3_D18	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AA7	DDR3_D19	DDR3_D19	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AA8	DDR3_D20	DDR3_D20	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AC6	DDR3_D21	DDR3_D21	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AE7	DDR3_D22	DDR3_D22	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AD7	DDR3_D23	DDR3_D23	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AA10	DDR3_D24	DDR3_D24	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AE10	DDR3_D25	DDR3_D25	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AD10	DDR3_D26	DDR3_D26	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AC10	DDR3_D27	DDR3_D27	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AC9	DDR3_D28	DDR3_D28	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AB10	DDR3_D29	DDR3_D29	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AB9	DDR3_D30	DDR3_D30	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
Y8	DDR3_D31	DDR3_D31	0	IOZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AB4	DDR3_DQM0	DDR3_DQM0	0	OZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AA5	DDR3_DQM1	DDR3_DQM1	0	OZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AC8	DDR3_DQM2	DDR3_DQM2	0	OZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AA9	DDR3_DQM3	DDR3_DQM3	0	OZ	OFF	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AE2	DDR3_DQS0_N	DDR3_DQS0_N	0	IOZ	PU	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AD1	DDR3_DQS0_P	DDR3_DQS0_P	0	IOZ	PD	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AE4	DDR3_DQS1_N	DDR3_DQS1_N	0	IOZ	PU	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AD4	DDR3_DQS1_P	DDR3_DQS1_P	0	IOZ	PD	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AD6	DDR3_DQS2_N	DDR3_DQS2_N	0	IOZ	PU	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AE6	DDR3_DQS2_P	DDR3_DQS2_P	0	IOZ	PD	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AD9	DDR3_DQS3_N	DDR3_DQS3_N	0	IOZ	PU	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AE9	DDR3_DQS3_P	DDR3_DQS3_P	0	IOZ	PD	OFF	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
AA13	DDR3_ODT0	DDR3_ODT0	0	OZ	OFF	DRIVE 0 (OFF)	0	1.35 V	DVDD_DDR		SSTL	PU/PD	
W12	DDR3_RZQ0	DDR3_RZQ0	0	A			0		DVDD_DDR		Analog		
V9	DDR3_RZQ1	DDR3_RZQ1	0	A			0		DVDD_DDR		Analog		
AD24	DDR_CLK_N	DDR_CLK_N	0	I			0	1.8 V	DVDD18		LVDS		
AE24	DDR_CLK_P	DDR_CLK_P	0	I			0	1.8 V	DVDD18		LVDS		
V22	DSS_DATA0	DSS_DATA0	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPMC_A1	1	OZ									0
		GPIO0_53	3	IOZ									0
		DSS_RFBI_DATA0	5	IOZ									0
U21	DSS_DATA1	DSS_DATA1	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPMC_A2	1	OZ									0
		eQEP2_S	2	IOZ									0
		GPIO0_52	3	IOZ									0
		DSS_RFBI_DATA1	5	IOZ									0
W22	DSS_DATA2	DSS_DATA2	0	OZ	OFF	OFF	3	3.3 V	DVDD33	Yes	LVCMOS		0
		GPMC_A3	1	OZ									0
		eQEP2_I	2	IOZ									0
		GPIO0_51	3	IOZ									0
		DSS_RFBI_DATA2	5	IOZ									0
		MAINPLL_OD_SEL	Bootstrap	I									0

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
V23	DSS_DATA3	DSS_DATA3	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPMC_A4	1	OZ									0
		eQEP2_B	2	I									0
		GPIO0_50	3	IOZ									0
		DSS_RFBI_DATA3	5	IOZ									0
		BOOT_RSVD	Bootstrap	I									0
U23	DSS_DATA4	DSS_DATA4	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPMC_A5	1	OZ									0
		eQEP2_A	2	I									0
		GPIO0_49	3	IOZ									0
		DSS_RFBI_DATA4	5	IOZ									0
		NODDR	Bootstrap	I									0
V24	DSS_DATA5	DSS_DATA5	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPMC_A6	1	OZ									0
		eQEP1_S	2	IOZ									0
		GPIO0_48	3	IOZ									0
		DSS_RFBI_DATA5	5	IOZ									0
T21	DSS_DATA6	DSS_DATA6	0	OZ	OFF	OFF	3	3.3 V	DVDD33	Yes	LVCMOS		0
		GPMC_A7	1	OZ									0
		eQEP1_I	2	IOZ									0
		GPIO0_47	3	IOZ									0
		EMU19	4	IOZ									0
		DSS_RFBI_DATA6	5	IOZ									0
U22	DSS_DATA7	DSS_DATA7	0	OZ	OFF	OFF	3	3.3 V	DVDD33	Yes	LVCMOS		0
		GPMC_A8	1	OZ									0
		eQEP1_B	2	I									0
		GPIO0_46	3	IOZ									0
		EMU18	4	IOZ									0
		DSS_RFBI_DATA7	5	IOZ									0
T22	DSS_DATA8	DSS_DATA8	0	OZ	OFF	OFF	3	3.3 V	DVDD33	Yes	LVCMOS		0
		GPMC_A9	1	OZ									0
		eQEP1_A	2	I									0
		GPIO0_45	3	IOZ									0
		EMU17	4	IOZ									0
		DSS_RFBI_DATA8	5	IOZ									0
		BOOTMODE15	Bootstrap	I									0

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
R21	DSS_DATA9	DSS_DATA9	0	OZ	OFF	OFF	3	3.3 V	DVDD33	Yes	LVCMOS		0
		GPMC_A10	1	OZ									0
		eQEP0_S	2	IOZ									0
		GPIO0_44	3	IOZ									0
		EMU16	4	IOZ									0
		DSS_RFBI_DATA9	5	IOZ									0
		BOOTMODE14	Bootstrap	I									0
U24	DSS_DATA10	DSS_DATA10	0	OZ	OFF	OFF	3	3.3 V	DVDD33	Yes	LVCMOS		0
		GPMC_A11	1	OZ									0
		eQEP0_I	2	IOZ									0
		GPIO0_43	3	IOZ									0
		EMU15	4	IOZ									0
		DSS_RFBI_DATA10	5	IOZ									0
		BOOTMODE13	Bootstrap	I									0
V25	DSS_DATA11	DSS_DATA11	0	OZ	OFF	OFF	3	3.3 V	DVDD33	Yes	LVCMOS		0
		GPMC_A12	1	OZ									0
		eQEP0_B	2	I									0
		GPIO0_42	3	IOZ									0
		EMU14	4	IOZ									0
		DSS_RFBI_DATA11	5	IOZ									0
		BOOTMODE12	Bootstrap	I									0
T24	DSS_DATA12	DSS_DATA12	0	OZ	OFF	OFF	3	3.3 V	DVDD33	Yes	LVCMOS		0
		GPMC_A13	1	OZ									0
		eQEP0_A	2	I									0
		GPIO0_41	3	IOZ									0
		EMU13	4	IOZ									0
		DSS_RFBI_DATA12	5	IOZ									0
		BOOTMODE11	Bootstrap	I									0
P21	DSS_DATA13	DSS_DATA13	0	OZ	OFF	OFF	3	3.3 V	DVDD33	Yes	LVCMOS		0
		GPMC_A14	1	OZ									0
		eHRPWM_TZn2	2	I									0
		GPIO0_40	3	IOZ									0
		EMU12	4	IOZ									0
		DSS_RFBI_DATA13	5	IOZ									0
		BOOTMODE10	Bootstrap	I									0

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
U25	DSS_DATA14	DSS_DATA14	0	OZ	OFF	OFF	3	3.3 V	DVDD33	Yes	LVCMOS		0
		GPMC_A15	1	OZ									0
		eHRPWM2_B	2	IOZ									0
		GPIO0_39	3	IOZ									0
		EMU11	4	IOZ									0
		DSS_RFBI_DATA14	5	IOZ									0
		BOOTMODE09	Bootstrap	I									0
R22	DSS_DATA15	DSS_DATA15	0	OZ	OFF	OFF	3	3.3 V	DVDD33	Yes	LVCMOS		0
		GPMC_A16	1	OZ									0
		eHRPWM2_A	2	IOZ									0
		GPIO0_38	3	IOZ									0
		EMU10	4	IOZ									0
		DSS_RFBI_DATA15	5	IOZ									0
		BOOTMODE08	Bootstrap	I									0
P23	DSS_DATA16	DSS_DATA16	0	OZ	OFF	OFF	3	3.3 V	DVDD33	Yes	LVCMOS		0
		GPMC_A17	1	OZ									0
		eHRPWM_TZn1	2	I									0
		GPIO0_37	3	IOZ									0
		EMU09	4	IOZ									0
		DSS_RFBI_CSn0	5	OZ									0
		BOOTMODE07	Bootstrap	I									0
R24	DSS_DATA17	DSS_DATA17	0	OZ	OFF	OFF	3	3.3 V	DVDD33	Yes	LVCMOS		0
		GPMC_A18	1	OZ									0
		eHRPWM1_B	2	IOZ									0
		GPIO0_36	3	IOZ									0
		EMU08	4	IOZ									0
		DSS_RFBI_CSn1	5	OZ									0
		BOOTMODE06	Bootstrap	I									0
N22	DSS_DATA18	DSS_DATA18	0	OZ	OFF	OFF	3	3.3 V	DVDD33	Yes	LVCMOS		0
		GPMC_A19	1	OZ									0
		eHRPWM1_A	2	IOZ									0
		GPIO0_35	3	IOZ									0
		EMU07	4	IOZ									0
		DSS_RFBI_HSYNC1	5	I									0
		BOOTMODE05	Bootstrap	I									0

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
T25	DSS_DATA19	DSS_DATA19	0	OZ	OFF	OFF	3	3.3 V	DVDD33	Yes	LVCMOS		0
		GPMC_A20	1	OZ									0
		eHRPWM0_SYNCO	2	OZ									0
		GPIO0_34	3	IOZ									0
		EMU06	4	IOZ									0
		DSS_RFBI_TEVSYNC1	5	I									0
		BOOTMODE04	Bootstrap	I									0
N24	DSS_DATA20	DSS_DATA20	0	OZ	OFF	OFF	3	3.3 V	DVDD33	Yes	LVCMOS		0
		GPMC_A21	1	OZ									0
		eHRPWM0_SYNCI	2	I									0
		GPIO0_33	3	IOZ									0
		EMU05	4	IOZ									0
		BOOTMODE03	Bootstrap	I									0
P24	DSS_DATA21	DSS_DATA21	0	OZ	OFF	OFF	3	3.3 V	DVDD33	Yes	LVCMOS		0
		GPMC_A22	1	OZ									0
		eHRPWM_TZn0	2	I									0
		GPIO0_32	3	IOZ									0
		EMU04	4	IOZ									0
		BOOTMODE02	Bootstrap	I									0
P25	DSS_DATA22	DSS_DATA22	0	OZ	OFF	OFF	3	3.3 V	DVDD33	Yes	LVCMOS		0
		GPMC_A23	1	OZ									0
		eHRPWM0_B	2	IOZ									0
		GPIO0_31	3	IOZ									0
		EMU03	4	IOZ									0
		BOOTMODE01	Bootstrap	I									0
N23	DSS_DATA23	DSS_DATA23	0	OZ	OFF	OFF	3	3.3 V	DVDD33	Yes	LVCMOS		0
		GPMC_A24	1	OZ									0
		eHRPWM0_A	2	IOZ									0
		GPIO0_30	3	IOZ									0
		EMU02	4	IOZ									0
		BOOTMODE00	Bootstrap	I									0
M25	DSS_DE	DSS_DE	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPMC_A0	1	OZ									0
		PR1_EDIO_OUTVALID	2	OZ									0
		GPIO0_57	3	IOZ									0
		DSS_RFBI_WEn	5	OZ									0

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
L25	DSS_FID	DSS_FID	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_EDIO_OUTVALID	2	OZ									0
		GPIO0_58	3	IOZ									0
		DSS_RFBI_A0	5	OZ									0
P22	DSS_HSYNC	DSS_HSYNC	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPMC_A26	1	OZ									0
		PR1_eCAP0_eCAP_SYNCIN	2	I									0
		GPIO0_55	3	IOZ									0
		DSS_RFBI_HSYNC0	5	I									0
N25	DSS_PCLK	DSS_PCLK	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPMC_A27	1	OZ									0
		PR1_eCAP0_eCAP_SYNCOUT	2	OZ									0
		GPIO0_56	3	IOZ									0
		DSS_RFBI_REn	5	OZ									0
R25	DSS_VSYNC	DSS_VSYNC	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPMC_A25	1	OZ									0
		PR1_eCAP0_eCAP_CAPIN_APWM_O	2	IOZ									0
		GPIO0_54	3	IOZ									0
		DSS_RFBI_TEVSYNC0	5	I									0
F17, F19, G6, H5, J6, K19, L20, L6, M7, U18, U6, V19, W6	DVDD18	DVDD18		PWR									
AA23, E23, F11, F15, F21, F7, G12, G16, G20, H11, H13, H15, H9, J20, P19, P7, R20, R6, T19, T23, T7, U20, V21	DVDD33	DVDD33		PWR									
G18, H17	DVDD33_USB	DVDD33_USB		PWR									
AD11, AD18, AD5, AE14, AE8, U10, U12, U14, U8, V11, V13, V15, V17, V7, W16, W18	DVDD_DDR	DVDD_DDR		PWR									
W10, W14, W8	DVDD_DDRDLL	DVDD_DDRDLL		PWR									
A23	eHRPWM3_A	PR0_EDIO_DATA3	1	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_73	3	IOZ									0
		eHRPWM3_A	4	IOZ									0

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
B22	eHRPWM3_B	PR0_EDIO_DATA2	1	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_74	3	IOZ									0
		eHRPWM3_B	4	IOZ									0
C22	eHRPWM3_SYNCI	PR0_EDIO_DATA1	1	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_75	3	IOZ									0
		eHRPWM3_SYNCI	4	I									0
D23	eHRPWM3_SYNCO	PR0_EDIO_DATA0	1	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_76	3	IOZ									0
		eHRPWM3_SYNCO	4	OZ									0
M22	EMU00	EMU00	0	IOZ	PU	OFF	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	
L22	EMU01	EMU01	0	IOZ	PU	OFF	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	
AC21	GPMC_AD0	GPMC_AD0	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_00	3	IOZ									0
AE20	GPMC_AD1	GPMC_AD1	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_01	3	IOZ									0
AD22	GPMC_AD2	GPMC_AD2	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_02	3	IOZ									0
AD20	GPMC_AD3	GPMC_AD3	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_03	3	IOZ									0
AE21	GPMC_AD4	GPMC_AD4	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_04	3	IOZ									0
AE22	GPMC_AD5	GPMC_AD5	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_05	3	IOZ									0
AC20	GPMC_AD6	GPMC_AD6	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_06	3	IOZ									0
AD21	GPMC_AD7	GPMC_AD7	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_07	3	IOZ									0
AE23	GPMC_AD8	GPMC_AD8	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_08	3	IOZ									0
AB20	GPMC_AD9	GPMC_AD9	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_09	3	IOZ									0
AA20	GPMC_AD10	GPMC_AD10	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_10	3	IOZ									0
AD23	GPMC_AD11	GPMC_AD11	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_11	3	IOZ									0
AA21	GPMC_AD12	GPMC_AD12	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_12	3	IOZ									0

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
AB21	GPMC_AD13	GPMC_AD13	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_13	3	IOZ									0
AB22	GPMC_AD14	GPMC_AD14	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_14	3	IOZ									0
AA22	GPMC_AD15	GPMC_AD15	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_15	3	IOZ									0
AC23	GPMC_ADVn_ALE	GPMC_ADVn_ALE	0	OZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_17	3	IOZ									0
AC24	GPMC_BEn0_CLE	GPMC_BEn0_CLE	0	OZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_20	3	IOZ									0
AB24	GPMC_BEn1	GPMC_BEn1	0	OZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_21	3	IOZ									0
AB23	GPMC_CLK	GPMC_CLK	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_16	3	IOZ									0
AB25	GPMC_CSn0	GPMC_CSn0	0	OZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_26	3	IOZ									0
W24	GPMC_CSn1	GPMC_CSn1	0	OZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		MLB_DAT	2	IOZ									0
		GPIO0_27	3	IOZ									0
W23	GPMC_CSn2	GPMC_CSn2	0	OZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		TIMI1	2	I									0
		GPIO0_28	3	IOZ									0
Y25	GPMC_CSn3	GPMC_CSn3	0	OZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		TIMO1	2	OZ									0
		GPIO0_29	3	IOZ									0
AA25	GPMC_DIR	GPMC_DIR	0	OZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		MLB_SIG	2	IOZ									0
		GPIO0_25	3	IOZ									0
AC22	GPMC_OEn_REn	GPMC_OEn_REn	0	OZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_18	3	IOZ									0
Y24	GPMC_WAIT0	GPMC_WAIT0	0	I	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_22	3	IOZ									0
AA24	GPMC_WAIT1	GPMC_WAIT1	0	I	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		MLB_CLK	2	I									0
		GPIO0_23	3	IOZ									0
Y22	GPMC_WEn	GPMC_WEn	0	OZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_19	3	IOZ									0

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
W25	GPMC_WPn	GPMC_WPn	0	OZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_24	3	IOZ									0
U5	I2C0_SCL	I2C0_SCL	0	IOD	OFF	OFF	0	3.3 V	DVDD33		I2C OPEN DRAIN		
W5	I2C0_SDA	I2C0_SDA	0	IOD	OFF	OFF	0	3.3 V	DVDD33		I2C OPEN DRAIN		
V6	I2C1_SCL	I2C1_SCL	0	IOD	OFF	OFF	0	3.3 V	DVDD33		I2C OPEN DRAIN		
W4	I2C1_SDA	I2C1_SDA	0	IOD	OFF	OFF	0	3.3 V	DVDD33		I2C OPEN DRAIN		
V5	I2C2_SCL	I2C2_SCL	0	IOD	OFF	OFF	0	3.3 V	DVDD33		I2C OPEN DRAIN		
V4	I2C2_SDA	I2C2_SDA	0	IOD	OFF	OFF	0	3.3 V	DVDD33		I2C OPEN DRAIN		
J8, L8	LDO_PCIE_CAP	LDO_PCIE_CAP		CAP									
H19, J18	LDO_USB_CAP	LDO_USB_CAP		CAP									
V2	LRESETn	LRESETn	0	I	PU	PU	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	
V1	LRESETNMIENn	LRESETNMIENn	0	I	PU	PU	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	
U3	MDIO_CLK	MDIO_CLK	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_98	3	IOZ									0
V3	MDIO_DATA	MDIO_DATA	0	IOZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_97	3	IOZ									0
B25	MII_COL	MII_COL	0	I	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_83	3	IOZ									0
G22	MII_CRS	MII_CRS	0	I	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		RMII_CRS_DV	2	I									0
		GPIO0_84	3	IOZ									0
A22	MII_RXCLK	MII_RXCLK	0	I	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		RGMII_RXC	1	I									0
		GPIO0_72	3	IOZ									0
B24	MII_RXD0	MII_RXD0	0	I	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		RGMII_RXD0	1	I									0
		RMII_RXD0	2	I									0
		GPIO0_80	3	IOZ									0
C23	MII_RXD1	MII_RXD1	0	I	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		RGMII_RXD1	1	I									0
		RMII_RXD1	2	I									0
		GPIO0_79	3	IOZ									0

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
B23	MII_RXD2	MII_RXD2	0	I	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		RGMII_RXD2	1	I									0
		GPIO0_78	3	IOZ									0
F22	MII_RXD3	MII_RXD3	0	I	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		RGMII_RXD3	1	I									0
		GPIO0_77	3	IOZ									0
A24	MII_RXDV	MII_RXDV	0	I	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		RGMII_RXCTL	1	I									0
		GPIO0_81	3	IOZ									0
F23	MII_RXER	MII_RXER	0	I	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		RMII_RXER	2	I									0
		GPIO0_82	3	IOZ									0
C25	MII_TXCLK	MII_TXCLK	0	I	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		RGMII_TXC	1	IOZ									0
		GPIO0_85	3	IOZ									0
G23	MII_TXD0	MII_TXD0	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		RGMII_TXD0	1	OZ									0
		RMII_TXD0	2	OZ									0
		GPIO0_94	3	IOZ									0
G24	MII_TXD1	MII_TXD1	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		RGMII_TXD1	1	OZ									0
		RMII_TXD1	2	OZ									0
		GPIO0_93	3	IOZ									0
G25	MII_TXD2	MII_TXD2	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		RGMII_TXD2	1	OZ									0
		GPIO0_92	3	IOZ									0
D25	MII_TXD3	MII_TXD3	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		RGMII_TXD3	1	OZ									0
		GPIO0_91	3	IOZ									0
H25	MII_TXEN	MII_TXEN	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		RGMII_TXCTL	1	OZ									0
		RMII_TXEN	2	OZ									0
		GPIO0_95	3	IOZ									0
H24	MII_TXER	MII_TXER	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_eCAP0_eCAP_SYNCIN	2	I									0
		GPIO0_96	3	IOZ									0
		eHRPWM_TZn3	4	I									0

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
L23	MLBP_CLK_N	MLBP_CLK_N	0	I			0	1.8 V	DVDD18		MLB LVDS		
M23	MLBP_CLK_P	MLBP_CLK_P	0	I			0	1.8 V	DVDD18		MLB LVDS		
K22	MLBP_DAT_N	MLBP_DAT_N	0	IO			0	1.8 V	DVDD18		MLB LVDS		
K23	MLBP_DAT_P	MLBP_DAT_P	0	IO			0	1.8 V	DVDD18		MLB LVDS		
M24	MLBP_SIG_N	MLBP_SIG_N	0	IO			0	1.8 V	DVDD18		MLB LVDS		
L24	MLBP_SIG_P	MLBP_SIG_P	0	IO			0	1.8 V	DVDD18		MLB LVDS		
J4	MMC1_CLK	MMC1_CLK	0	IOZ	PU	PU	3	1.8 V	DVDD18	Yes	LVCMOS	PU/PD	0
		GPIO0_67	3	IOZ									0
J2	MMC1_CMD	MMC1_CMD	0	IOZ	PU	PU	3	1.8 V	DVDD18	Yes	LVCMOS	PU/PD	0
		GPIO0_68	3	IOZ									0
K2	MMC1_POW	MMC1_POW	0	OZ	PD	PD	3	1.8 V	DVDD18	Yes	LVCMOS	PU/PD	0
		GPIO0_71	3	IOZ									0
J3	MMC1_SDCD	MMC1_SDCD	0	I	PD	PD	3	1.8 V	DVDD18	Yes	LVCMOS	PU/PD	0
		GPIO0_69	3	IOZ									0
K3	MMC1_SDWP	MMC1_SDWP	0	I	PD	PD	3	1.8 V	DVDD18	Yes	LVCMOS	PU/PD	0
		GPIO0_70	3	IOZ									0
H3	MMC1_DAT0	MMC1_DAT0	0	IOZ	PU	PU	3	1.8 V	DVDD18	Yes	LVCMOS	PU/PD	0
		GPIO0_66	3	IOZ									0
F5	MMC1_DAT1	MMC1_DAT1	0	IOZ	PU	PU	3	1.8 V	DVDD18	Yes	LVCMOS	PU/PD	0
		GPIO0_65	3	IOZ									0
J5	MMC1_DAT2	MMC1_DAT2	0	IOZ	PU	PU	3	1.8 V	DVDD18	Yes	LVCMOS	PU/PD	0
		GPIO0_64	3	IOZ									0
H4	MMC1_DAT3	MMC1_DAT3	0	IOZ	PU	PU	3	1.8 V	DVDD18	Yes	LVCMOS	PU/PD	0
		GPIO0_63	3	IOZ									0
E3	MMC1_DAT4	MMC1_DAT4	0	IOZ	PU	PU	3	1.8 V	DVDD18	Yes	LVCMOS	PU/PD	0
		GPIO0_62	3	IOZ									0
G4	MMC1_DAT5	MMC1_DAT5	0	IOZ	PU	PU	3	1.8 V	DVDD18	Yes	LVCMOS	PU/PD	0
		GPIO0_61	3	IOZ									0
F4	MMC1_DAT6	MMC1_DAT6	0	IOZ	PU	PU	3	1.8 V	DVDD18	Yes	LVCMOS	PU/PD	0
		GPIO0_60	3	IOZ									0
G5	MMC1_DAT7	MMC1_DAT7	0	IOZ	PU	PU	3	1.8 V	DVDD18	Yes	LVCMOS	PU/PD	0
		GPIO0_59	3	IOZ									0
W1	NMIn	NMIn	0	I	PU	PU	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	
L1	OBSCLK_N	OBSCLK_N	0	O			0	1.8 V	DVDD18		LVDS		
K1	OBSCLK_P	OBSCLK_P	0	O			0	1.8 V	DVDD18		LVDS		
N5	OBSPLL_LOCK	OBSPLL_LOCK	0	OZ	PD	PD	0	1.8 V	DVDD18	Yes	LVCMOS	PU/PD	
F2	PCIE_CLK_N	PCIE_CLK_N	0	I			0	1.8 V	DVDD18 / VDDAHV		LVDS		

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
G2	PCIE_CLK_P	PCIE_CLK_P	0	I			0	1.8 V	DVDD18 / VDDAHV		LVDS		
H7	PCIE_REFRES	PCIE_REFRES	0	A			0	NA	n/a		Analog		
D1	PCIE_RXN0	PCIE_RXN0	0	I			0		DVDD18 / VDDAHV		CML		
E1	PCIE_RXP0	PCIE_RXP0	0	I			0		DVDD18 / VDDAHV		CML		
H1	PCIE_TXN0	PCIE_TXN0	0	O			0		DVDD18 / VDDAHV		CML		
G1	PCIE_TXP0	PCIE_TXP0	0	O			0		DVDD18 / VDDAHV		CML		
AA3	PORn	PORn	0	I			0	3.3 V	DVDD33	Yes	LVCMOS		
A10	PR0_MDIO_DATA	PR0_MDIO_DATA	0	IOZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO1_04	3	IOZ									0
		MCASP0_AXR3	4	IOZ									0
C10	PR0_MDIO_MDCLK	PR0_MDIO_MDCLK	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO1_05	3	IOZ									0
		MCASP0_AXR4	4	IOZ									0
E18	PR1_MDIO_DATA	PR1_MDIO_DATA	0	IOZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO1_46	3	IOZ									0
		eCAP0_IN_APWM0_OUT	4	IOZ									0
D18	PR1_MDIO_MDCLK	PR1_MDIO_MDCLK	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO1_47	3	IOZ									0
		eCAP1_IN_APWM1_OUT	4	IOZ									0
D3	PR0_PRU0_GPO0	PR0_PRU0_GPO0	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU0_GPI0	1	I									0
		GPIO0_108	3	IOZ									0
		MCASP2_AXR0	4	IOZ									0
A2	PR0_PRU0_GPO1	PR0_PRU0_GPO1	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU0_GPI1	1	I									0
		GPIO0_109	3	IOZ									0
		MCASP2_AXR1	4	IOZ									0
E4	PR0_PRU0_GPO2	PR0_PRU0_GPO2	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU0_GPI2	1	I									0
		GPIO0_110	3	IOZ									0
		MCASP2_AXR2	4	IOZ									0
B1	PR0_PRU0_GPO3	PR0_PRU0_GPO3	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU0_GPI3	1	I									0
		GPIO0_111	3	IOZ									0
		MCASP2_AXR3	4	IOZ									0

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
A3	PR0_PRU0_GPO4	PR0_PRU0_GPO4	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU0_GPI4	1	I									0
		GPIO0_112	3	IOZ									0
		MCASP2_AXR4	4	IOZ									0
E5	PR0_PRU0_GPO5	PR0_PRU0_GPO5	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU0_GPI5	1	I									0
		GPIO0_113	3	IOZ									0
		MCASP2_AXR5	4	IOZ									0
B2	PR0_PRU0_GPO6	PR0_PRU0_GPO6	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU0_GPI6	1	I									0
		GPIO0_114	3	IOZ									0
		MCASP2_ACLKR	4	IOZ									0
D4	PR0_PRU0_GPO7	PR0_PRU0_GPO7	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU0_GPI7	1	I									0
		GPIO0_115	3	IOZ									0
		MCASP2_AFSR	4	IOZ									0
E6	PR0_PRU0_GPO8	PR0_PRU0_GPO8	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU0_GPI8	1	I									0
		GPIO0_116	3	IOZ									0
		MCASP2_AHCLKR	4	IOZ									0
C2	PR0_PRU0_GPO9	PR0_PRU0_GPO9	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU0_GPI9	1	I									0
		XREFCLK	2	I									0
		GPIO0_117	3	IOZ									0
		MCASP2_AMUTE	4	IOZ									0
C3	PR0_PRU0_GPO10	PR0_PRU0_GPO10	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU0_GPI10	1	I									0
		GPIO0_118	3	IOZ									0
		MCASP2_AFSX	4	IOZ									0
D5	PR0_PRU0_GPO11	PR0_PRU0_GPO11	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU0_GPI11	1	I									0
		GPIO0_119	3	IOZ									0
		MCASP2_AHCLKX	4	IOZ									0
B3	PR0_PRU0_GPO12	PR0_PRU0_GPO12	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU0_GPI12	1	I									0
		GPIO0_120	3	IOZ									0
		MCASP2_ACLKX	4	IOZ									0

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
B4	PR0_PRU0_GPO13	PR0_PRU0_GPO13	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU0_GPI13	1	I									0
		GPIO0_121	3	IOZ									0
		MCASP1_ACLKR	4	IOZ									0
A4	PR0_PRU0_GPO14	PR0_PRU0_GPO14	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU0_GPI14	1	I									0
		GPIO0_122	3	IOZ									0
		MCASP1_AFSR	4	IOZ									0
E7	PR0_PRU0_GPO15	PR0_PRU0_GPO15	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU0_GPI15	1	I									0
		GPIO0_123	3	IOZ									0
		MCASP1_AHCLKR	4	IOZ									0
D6	PR0_PRU0_GPO16	PR0_PRU0_GPO16	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU0_GPI16	1	I									0
		GPIO0_124	3	IOZ									0
		MCASP1_ACLKX	4	IOZ									0
C4	PR0_PRU0_GPO17	PR0_PRU0_GPO17	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU0_GPI17	1	I									0
		PR1_UART0_RXD	2	I									0
		GPIO0_125	3	IOZ									0
		MCASP1_AFSX	4	IOZ									0
C5	PR0_PRU0_GPO18	PR0_PRU0_GPO18	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU0_GPI18	1	I									0
		PR0_EDC_LATCH0_IN	2	I									0
		GPIO0_126	3	IOZ									0
		MCASP1_AHCLKX	4	IOZ									0
A5	PR0_PRU0_GPO19	PR0_PRU0_GPO19	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU0_GPI19	1	I									0
		PR0_EDC_SYNC0_OUT	2	OZ									0
		GPIO0_127	3	IOZ									0
		MCASP1_AMUTE	4	IOZ									0
B5	PR0_PRU1_GPO0	PR0_PRU1_GPO0	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU1_GPI0	1	I									0
		GPIO0_128	3	IOZ									0
		MCASP1_AXR0	4	IOZ									0

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
B6	PR0_PRU1_GPO1	PR0_PRU1_GPO1	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU1_GPI1	1	I									0
		GPIO0_129	3	IOZ									0
		MCASP1_AXR1	4	IOZ									0
D7	PR0_PRU1_GPO2	PR0_PRU1_GPO2	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU1_GPI2	1	I									0
		GPIO0_130	3	IOZ									0
		MCASP1_AXR2	4	IOZ									0
A6	PR0_PRU1_GPO3	PR0_PRU1_GPO3	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU1_GPI3	1	I									0
		GPIO0_131	3	IOZ									0
		MCASP1_AXR3	4	IOZ									0
C6	PR0_PRU1_GPO4	PR0_PRU1_GPO4	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU1_GPI4	1	I									0
		GPIO0_132	3	IOZ									0
		MCASP1_AXR4	4	IOZ									0
E8	PR0_PRU1_GPO5	PR0_PRU1_GPO5	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU1_GPI5	1	I									0
		GPIO0_133	3	IOZ									0
		MCASP1_AXR5	4	IOZ									0
A7	PR0_PRU1_GPO6	PR0_PRU1_GPO6	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU1_GPI6	1	I									0
		GPIO0_134	3	IOZ									0
		MCASP1_AXR6	4	IOZ									0
D8	PR0_PRU1_GPO7	PR0_PRU1_GPO7	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU1_GPI7	1	I									0
		GPIO0_135	3	IOZ									0
		MCASP1_AXR7	4	IOZ									0
F9	PR0_PRU1_GPO8	PR0_PRU1_GPO8	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU1_GPI8	1	I									0
		GPIO0_136	3	IOZ									0
		MCASP1_AXR8	4	IOZ									0
B7	PR0_PRU1_GPO9	PR0_PRU1_GPO9	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU1_GPI9	1	I									0
		GPIO0_137	3	IOZ									0
		MCASP1_AXR9	4	IOZ									0

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
C7	PR0_PRU1_GPO10	PR0_PRU1_GPO10	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU1_GPI10	1	I									0
		GPIO0_138	3	IOZ									0
		MCASP0_AMUTE	4	IOZ									0
E9	PR0_PRU1_GPO11	PR0_PRU1_GPO11	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU1_GPI11	1	I									0
		GPIO0_139	3	IOZ									0
		MCASP0_ACLKR	4	IOZ									0
A8	PR0_PRU1_GPO12	PR0_PRU1_GPO12	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU1_GPI12	1	I									0
		GPIO0_140	3	IOZ									0
		MCASP0_AFSR	4	IOZ									0
B8	PR0_PRU1_GPO13	PR0_PRU1_GPO13	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU1_GPI13	1	I									0
		GPIO0_141	3	IOZ									0
		MCASP0_AHCLKR	4	IOZ									0
D9	PR0_PRU1_GPO14	PR0_PRU1_GPO14	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU1_GPI14	1	I									0
		GPIO0_142	3	IOZ									0
		MCASP0_ACLKX	4	IOZ									0
C8	PR0_PRU1_GPO15	PR0_PRU1_GPO15	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU1_GPI15	1	I									0
		GPIO0_143	3	IOZ									0
		MCASP0_AFSX	4	IOZ									0
C9	PR0_PRU1_GPO16	PR0_PRU1_GPO16	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU1_GPI16	1	I									0
		GPIO1_00	3	IOZ									0
		MCASP0_AHCLKX	4	IOZ									0
B9	PR0_PRU1_GPO17	PR0_PRU1_GPO17	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU1_GPI17	1	I									0
		PR1_UART0_TXD	2	OZ									0
		GPIO1_01	3	IOZ									0
		MCASP0_AXR0	4	IOZ									0

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
A9	PR0_PRU1_GPO18	PR0_PRU1_GPO18	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU1_GPI18	1	I									0
		PR0_EDC_LATCH1_IN	2	I									0
		GPIO1_02	3	IOZ									0
		MCASP0_AXR1	4	IOZ									0
B10	PR0_PRU1_GPO19	PR0_PRU1_GPO19	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_PRU1_GPI19	1	I									0
		PR0_EDC_SYNC1_OUT	2	OZ									0
		GPIO1_03	3	IOZ									0
		MCASP0_AXR2	4	IOZ									0
E10	PR1_PRU0_GPO0	PR1_PRU0_GPO0	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU0_GPI0	1	I									0
		GPIO1_06	3	IOZ									0
		MCASP0_AXR5	4	IOZ									0
D10	PR1_PRU0_GPO1	PR1_PRU0_GPO1	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU0_GPI1	1	I									0
		GPIO1_07	3	IOZ									0
		MCASP0_AXR6	4	IOZ									0
F10	PR1_PRU0_GPO2	PR1_PRU0_GPO2	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU0_GPI2	1	I									0
		GPIO1_08	3	IOZ									0
		MCASP0_AXR7	4	IOZ									0
C11	PR1_PRU0_GPO3	PR1_PRU0_GPO3	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU0_GPI3	1	I									0
		GPIO1_09	3	IOZ									0
		MCASP0_AXR8	4	IOZ									0
D11	PR1_PRU0_GPO4	PR1_PRU0_GPO4	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU0_GPI4	1	I									0
		MMC0_POW	2	OZ									0
		GPIO1_10	3	IOZ									0
		MCASP0_AXR9	4	IOZ									0
E11	PR1_PRU0_GPO5	PR1_PRU0_GPO5	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU0_GPI5	1	I									0
		MMC0_SDWP	2	I									0
		GPIO1_11	3	IOZ									0
		MCASP0_AXR10	4	IOZ									0

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
F12	PR1_PRU0_GPO6	PR1_PRU0_GPO6	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU0_GPI6	1	I									0
		MMC0_SDCD	2	I									0
		GPIO1_12	3	IOZ									0
		MCASP0_AXR11	4	IOZ									0
E12	PR1_PRU0_GPO7	PR1_PRU0_GPO7	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU0_GPI7	1	I									0
		MMC0_DAT7	2	IOZ									0
		GPIO1_13	3	IOZ									0
		MCASP0_AXR12	4	IOZ									0
C12	PR1_PRU0_GPO8	PR1_PRU0_GPO8	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU0_GPI8	1	I									0
		MMC0_DAT6	2	IOZ									0
		GPIO1_14	3	IOZ									0
		MCASP0_AXR13	4	IOZ									0
B11	PR1_PRU0_GPO9	PR1_PRU0_GPO9	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU0_GPI9	1	I									0
		MMC0_DAT5	2	IOZ									0
		GPIO1_15	3	IOZ									0
		MCASP0_AXR14	4	IOZ									0
B12	PR1_PRU0_GPO10	PR1_PRU0_GPO10	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU0_GPI10	1	I									0
		MMC0_DAT4	2	IOZ									0
		GPIO1_16	3	IOZ									0
		MCASP0_AXR15	4	IOZ									0
A12	PR1_PRU0_GPO11	PR1_PRU0_GPO11	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU0_GPI11	1	I									0
		MMC0_DAT3	2	IOZ									0
		GPIO1_17	3	IOZ									0
A11	PR1_PRU0_GPO12	PR1_PRU0_GPO12	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU0_GPI12	1	I									0
		MMC0_DAT2	2	IOZ									0
		GPIO1_18	3	IOZ									0
A13	PR1_PRU0_GPO13	PR1_PRU0_GPO13	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU0_GPI13	1	I									0
		MMC0_DAT1	2	IOZ									0
		GPIO1_19	3	IOZ									0

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
B13	PR1_PRU0_GPO14	PR1_PRU0_GPO14	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU0_GPI14	1	I									0
		MMC0_DAT0	2	IOZ									0
		GPIO1_20	3	IOZ									0
F13	PR1_PRU0_GPO15	PR1_PRU0_GPO15	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU0_GPI15	1	I									0
		MMC0_CLK	2	IOZ									0
		GPIO1_21	3	IOZ									0
C13	PR1_PRU0_GPO16	PR1_PRU0_GPO16	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU0_GPI16	1	I									0
		MMC0_CMD	2	IOZ									0
		GPIO1_22	3	IOZ									0
E13	PR1_PRU0_GPO17	PR1_PRU0_GPO17	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU0_GPI17	1	I									0
		GPIO1_23	3	IOZ									0
		eHRPWM_TZn4	4	I									0
		eHRPWM_SOCA	5	OZ									0
D12	PR1_PRU0_GPO18	PR1_PRU0_GPO18	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU0_GPI18	1	I									0
		PR1_EDC_LATCH0_IN	2	I									0
		GPIO1_24	3	IOZ									0
		eHRPWM4_A	4	IOZ									0
D13	PR1_PRU0_GPO19	PR1_PRU0_GPO19	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU0_GPI19	1	I									0
		PR1_EDC_SYNC0_OUT	2	OZ									0
		GPIO1_25	3	IOZ									0
		eHRPWM4_B	4	IOZ									0
A14	PR1_PRU1_GPO0	PR1_PRU1_GPO0	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU1_GPI0	1	I									0
		GPIO1_26	3	IOZ									0
B14	PR1_PRU1_GPO1	PR1_PRU1_GPO1	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU1_GPI1	1	I									0
		GPIO1_27	3	IOZ									0
C14	PR1_PRU1_GPO2	PR1_PRU1_GPO2	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU1_GPI2	1	I									0
		GPIO1_28	3	IOZ									0

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
E14	PR1_PRU1_GPO3	PR1_PRU1_GPO3	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU1_GPI3	1	I									0
		GPIO1_29	3	IOZ									0
D14	PR1_PRU1_GPO4	PR1_PRU1_GPO4	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU1_GPI4	1	I									0
		GPIO1_30	3	IOZ									0
A15	PR1_PRU1_GPO5	PR1_PRU1_GPO5	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU1_GPI5	1	I									0
		GPIO1_31	3	IOZ									0
F14	PR1_PRU1_GPO6	PR1_PRU1_GPO6	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU1_GPI6	1	I									0
		GPIO1_32	3	IOZ									0
B15	PR1_PRU1_GPO7	PR1_PRU1_GPO7	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU1_GPI7	1	I									0
		GPIO1_33	3	IOZ									0
C15	PR1_PRU1_GPO8	PR1_PRU1_GPO8	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU1_GPI8	1	I									0
		GPIO1_34	3	IOZ									0
D15	PR1_PRU1_GPO9	PR1_PRU1_GPO9	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU1_GPI9	1	I									0
		MCBSP_DR	2	I									0
		GPIO1_35	3	IOZ									0
A16	PR1_PRU1_GPO10	PR1_PRU1_GPO10	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU1_GPI10	1	I									0
		MCBSP_DX	2	OZ									0
		GPIO1_36	3	IOZ									0
E15	PR1_PRU1_GPO11	PR1_PRU1_GPO11	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU1_GPI11	1	I									0
		MCBSP_FSX	2	IOZ									0
		GPIO1_37	3	IOZ									0
B16	PR1_PRU1_GPO12	PR1_PRU1_GPO12	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU1_GPI12	1	I									0
		MCBSP_CLKX	2	IOZ									0
		GPIO1_38	3	IOZ									0

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
C16	PR1_PRU1_GPO13	PR1_PRU1_GPO13	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU1_GPI13	1	I									0
		MCBSP_FSR	2	IOZ									0
		GPIO1_39	3	IOZ									0
D17	PR1_PRU1_GPO14	PR1_PRU1_GPO14	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU1_GPI14	1	I									0
		MCBSP_CLKR	2	IOZ									0
		GPIO1_40	3	IOZ									0
C18	PR1_PRU1_GPO15	PR1_PRU1_GPO15	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU1_GPI15	1	I									0
		GPIO1_41	3	IOZ									0
D16	PR1_PRU1_GPO16	PR1_PRU1_GPO16	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU1_GPI16	1	I									0
		GPIO1_42	3	IOZ									0
F16	PR1_PRU1_GPO17	PR1_PRU1_GPO17	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU1_GPI17	1	I									0
		GPIO1_43	3	IOZ									0
		eHRPWM_TZn5	4	I									0
		eHRPWM_SOCB	5	OZ									0
E17	PR1_PRU1_GPO18	PR1_PRU1_GPO18	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU1_GPI18	1	I									0
		PR1_EDC_LATCH1_IN	2	I									0
		GPIO1_44	3	IOZ									0
		eHRPWM5_A	4	IOZ									0
E16	PR1_PRU1_GPO19	PR1_PRU1_GPO19	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_PRU1_GPI19	1	I									0
		PR1_EDC_SYNC1_OUT	2	OZ									0
		GPIO1_45	3	IOZ									0
		eHRPWM5_B	4	IOZ									0
K25	QSPI_CLK	QSPI_CLK	0	OZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO1_58	3	IOZ									0
J25	QSPI_CSn0	QSPI_CSn0	0	OZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO1_64	3	IOZ									0
H23	QSPI_CSn1	QSPI_CSn1	0	OZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		CLKOUT	1	OZ									0
		GPIO1_65	3	IOZ									0

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
H22	QSPI_CSn2	QSPI_CSn2	0	OZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		DCAN1_TX	1	OZ									0
		PR1_UART0_CTSN	2	I									0
		GPIO1_66	3	IOZ									0
		USB0_EXT_TRIGGER	4	I									0
H21	QSPI_CSn3	QSPI_CSn3	0	OZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	1
		DCAN1_RX	1	I									1
		PR1_UART0_RTSN	2	OZ									1
		GPIO1_67	3	IOZ									1
		USB1_EXT_TRIGGER	4	I									1
J23	QSPI_D0	QSPI_D0	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO1_60	3	IOZ									0
J22	QSPI_D1	QSPI_D1	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO1_61	3	IOZ									0
J21	QSPI_D2	QSPI_D2	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO1_62	3	IOZ									0
J24	QSPI_D3	QSPI_D3	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO1_63	3	IOZ									0
K24	QSPI_RCLK	QSPI_RCLK	0	I	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO1_59	3	IOZ									0
W2	RESETFULLn	RESETFULLn	0	I	PU	PU	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	
W3	RESETn	RESETn	0	I	PU	PU	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	
Y2	RESETSTATn	RESETSTATn	0	O	DRIVE 0 (OFF)	DRIVE 0 (OFF)	0	3.3 V	DVDD33	Yes	LVCMOS		
D24	RMII_REFCLK	RMII_REFCLK	0	IOZ	PD	PD	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_eCAP0_eCAP_SYNCOUT	2	OZ									0
M2	SPI0_CLK	SPI0_CLK	0	IOZ	PD	PD	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
N4	SPI0_SIMO	SPI0_SIMO	0	IOZ	PD	PD	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
M1	SPI0_SOMI	SPI0_SOMI	0	IOZ	PD	PD	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
N2	SPI1_CLK	SPI1_CLK	0	IOZ	PD	PD	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
P2	SPI1_SIMO	SPI1_SIMO	0	IOZ	PD	PD	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
N1	SPI1_SOMI	SPI1_SOMI	0	IOZ	PD	PD	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
R2	SPI2_CLK	SPI2_CLK	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_103	3	IOZ									0
R3	SPI2_SIMO	SPI2_SIMO	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_105	3	IOZ									0

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
R4	SPI2_SOMI	SPI2_SOMI	0	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_104	3	IOZ									0
E24	SPI3_CLK	SPI3_CLK	1	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_UART0_TXD	2	OZ									0
		GPIO0_88	3	IOZ									0
F24	SPI3_SIMO	SPI3_SIMO	1	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_UART0_RTSN	2	OZ									0
		GPIO0_90	3	IOZ									0
F25	SPI3_SOMI	SPI3_SOMI	1	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR0_UART0_CTSN	2	I									0
		GPIO0_89	3	IOZ									0
M3	SPI0_SCSn0	SPI0_SCSn0	0	IOZ	PU	PU	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	1
M4	SPI0_SCSn1	SPI0_SCSn1	0	IOZ	PU	PU	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_99	3	IOZ									0
P1	SPI1_SCSn0	SPI1_SCSn0	0	IOZ	PU	PU	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	1
N3	SPI1_SCSn1	SPI1_SCSn1	0	IOZ	PU	PU	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_100	3	IOZ									0
P3	SPI2_SCSn0	SPI2_SCSn0	0	IOZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_101	3	IOZ									0
P4	SPI2_SCSn1	SPI2_SCSn1	0	IOZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO0_102	3	IOZ									0
C24	SPI3_SCSn0	SPI3_SCSn0	1	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	1
		PR0_eCAP0_eCAP_CAPIN_APWM_O	2	IOZ									1
		GPIO0_86	3	IOZ									1
E25	SPI3_SCSn1	SPI3_SCSn1	1	IOZ	PD	PD	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	1
		PR0_UART0_RXD	2	I									1
		GPIO0_87	3	IOZ									1
M21	SYSCLKOUT	SYSCLKOUT	0	OZ	PD	PD	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	
R1	SYSCLKSEL	SYSCLKSEL	0	I			0	3.3 V	DVDD33	Yes	LVCMOS		
AC25	SYSCLK_N	SYSCLK_N	0	I			0	1.8 V	DVDD18		LVDS		
AD25	SYSCLK_P	SYSCLK_P	0	I			0	1.8 V	DVDD18		LVDS		
AC19	SYSOSC_IN	SYSOSC_IN	0	I			0	1.8 V	DVDD18		Analog		
AE19	SYSOSC_OUT	SYSOSC_OUT	0	O			0	1.8 V	DVDD18		Analog		
L3	TCK	TCK	0	I	PU	PU	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	
L5	TDI	TDI	0	I	PU	PU	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	
K5	TDO	TDO	0	OZ	PU	OFF	0	3.3 V	DVDD33		LVCMOS	PU/PD	
K4	TMS	TMS	0	I	PU	PU	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
L4	TRSTn	TRSTn	0	I	PD	PD	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	
T2	UART0_CTSn	UART0_CTSn	0	I	PU	PU	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		TIMI0	1	I									0
		GPIO0_106	3	IOZ									0
U1	UART0_RTSn	UART0_RTSn	0	OZ	PU	PU	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		TIMO0	1	OZ									0
		GPIO0_107	3	IOZ									0
T4	UART0_RXD	UART0_RXD	0	I	PU	PU	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	1
T1	UART0_TXD	UART0_TXD	0	OZ	PU	PU	0	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	
U2	UART1_CTSn	UART1_CTSn	0	I	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO1_50	3	IOZ									0
U4	UART1_RTSn	UART1_RTSn	0	OZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO1_51	3	IOZ									0
T3	UART1_RXD	UART1_RXD	0	I	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO1_48	3	IOZ									0
T5	UART1_TXD	UART1_TXD	0	OZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		GPIO1_49	3	IOZ									0
D22	UART2_CTSn	UART2_CTSn	0	I	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_EDIO_DATA1	1	IOZ									0
		UART0_DTRn	2	OZ									0
		GPIO1_54	3	IOZ									0
		CPTS_TS_SYNC	4	OZ									0
C21	UART2_RTSn	UART2_RTSn	0	OZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_EDIO_DATA0	1	IOZ									0
		UART0_RIN	2	I									0
		GPIO1_55	3	IOZ									0
		CPTS_TS_COMP	4	OZ									0
E21	UART2_RXD	UART2_RXD	0	I	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_EDIO_DATA3	1	IOZ									0
		UART0_DCDn	2	I									0
		GPIO1_52	3	IOZ									0
		CPTS_HW1_TSPUSH	4	I									0
D21	UART2_TXD	UART2_TXD	0	OZ	PU	PU	3	3.3 V	DVDD33	Yes	LVCMOS	PU/PD	0
		PR1_EDIO_DATA2	1	IOZ									0
		UART0_DSRn	2	I									0
		GPIO1_53	3	IOZ									0
		CPTS_HW2_TSPUSH	4	I									0

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
B18	USB0_DM	USB0_DM	0	IO			0		DVDD18 / DVDD33_USB		USB0_PHY		
A18	USB0_DP	USB0_DP	0	IO			0		DVDD18 / DVDD33_USB		USB0_PHY		
E19	USB0_DRVVBUS	USB0_DRVVBUS	0	OZ	PD	PD	0	3.3 V	DVDD33_USB	Yes	LVCMOS	PU/PD	
A19	USB0_ID	USB0_ID	0	A			0		DVDD18 / DVDD33_USB		USB0_PHY		
C19	USB0_TXRTUNE_RKELVIN	USB0_TXRTUNE_RKELVIN	0	A					DVDD18 / DVDD33_USB		USB0_PHY		
B19	USB0_VBUS	USB0_VBUS	0	A			0	5.0 V	n/a - Fail-safe		USB0_PHY		
D19	USB0_XO	USB0_XO	0	I			0	1.8 V	DVDD18 / DVDD33_USB		USB0_PHY		
A20	USB1_DM	USB1_DM	0	IO			0		DVDD18 / DVDD33_USB		USB1_PHY		
B20	USB1_DP	USB1_DP	0	IO			0		DVDD18 / DVDD33_USB		USB1_PHY		
B21	USB1_DRVVBUS	USB1_DRVVBUS	0	OZ	PD	PD	0	3.3 V	DVDD33_USB	Yes	LVCMOS	PU/PD	
E20	USB1_ID	USB1_ID	0	A			0		DVDD18 / DVDD33_USB		USB1_PHY		
D20	USB1_TXRTUNE_RKELVIN	USB1_TXRTUNE_RKELVIN	0	A					DVDD18 / DVDD33_USB		USB1_PHY		
A21	USB1_VBUS	USB1_VBUS	0	A			0	5.0 V	n/a - Fail-safe		USB1_PHY		
C20	USB1_XO	USB1_XO	0	I			0	1.8 V	DVDD18 / DVDD33_USB		USB1_PHY		
K7	VDDAHV	VDDAHV		PWR									
Y21	VPP	VPP		PWR									
W21	VPP2	VPP2		PWR									

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Table 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
A1, A25, AD14, AD8, AE1, AE11, AE18, AE25, AE5, C1, E2, E22, F1, F20, F3, F6, F8, G11, G13, G15, G17, G19, G21, G7, G9, H10, H12, H14, H16, H18, H20, H6, H8, J1, J11, J13, J15, J17, J19, J7, J9, K10, K12, K14, K16, K18, K20, K6, K8, L11, L13, L15, L17, L19, L7, L9, M10, M12, M14, M16, M18, M20, M6, M8, N11, N13, N15, N17, N19, N21, N7, N9, P10, P12, P14, P16, P18, P20, P6, P8, R11, R13, R15, R17, R19, R23, R7, R9, T10, T12, T14, T16, T18, T20, T6, T8, U11, U13, U15, U17, U19, U7, U9, V10, V12, V14, V16, V18, V20, V8, W11, W13, W15, W17, W7, W9, Y10, Y23	VSS	VSS		GND									
B17	VSS_OSC_AUDIO	VSS_OSC_AUDIO		GND									
AD19	VSS_OSC_SYS	VSS_OSC_SYS		GND									

The following list describes the table column headers:

1. **BALL NUMBER:** Ball numbers on the bottom side associated with each signal on the bottom.
2. **BALL NAME:** Mechanical name from package device (name is taken from muxmode 0).
3. **SIGNAL NAME:** Names of signals multiplexed on each ball (also notice that the name of the ball is the signal name in muxmode 0).

NOTE

Many device pins support multiple signal functions. Some signal functions are selected via a single layer of multiplexers associated with pins. Other signal functions are selected via two or more layers of multiplexers, where one layer is associated with the pins and other layers are associated with peripheral logic functions.

Table 4-1, *Pin Attributes* only describes signal multiplexing at the pins. For more information, related to signal multiplexing at the pins, see section *Pad Configuration Registers* in section *Control Module (BOOT_CFG)* of chapter *Device Configuration* of the Device TRM. Refer to the respective peripheral chapter of the Device TRM for information associated with peripheral signal multiplexing.

4. **MUXMODE:** Multiplexing mode number:
   a. MUXMODE 0 is the primary muxmode. The primary muxmode is not necessarily the default muxmode.

NOTE

The default muxmode is the mode at the release of the reset; also see the BALL RESET REL. MUXMODE column.

   b. MUXMODE 1 through 5 are possible muxmodes for alternate functions. On each pin, some muxmodes are effectively used for alternate functions, while some muxmodes are not used. Only MUXMODE values which correspond to defined functions should be used.
   c. Bootstrap are Special Configuration Pins, latched on rising edge of PORn / RESETFULLn. These are not programable MUXMODE.
   d. An empty box means Not Applicable.
5. **TYPE:** Signal type and direction:
   – I = Input
   – O = Output
   – IO = Input or Output
   – IOD = Input or Open-drain Output
   – IOZ = Input or Three-state Output
   – OZ = Three-state Output
   – A = Analog
   – PWR = Power
   – GND = Ground
   – CAP = LDO Capacitor.

NOTE

The RX buffer within the pad logic should be disabled on all pins that are not being used as an input. For more information, see the *Control Module (BOOT_CFG) / BOOT_CFG Functional Description / Pad Configuration Registers* section in the device TRM.

6. **BALL RESET STATE:** The state of the terminal at power-on reset:
   – DRIVE 0 (OFF): The buffer drives V_{OL} (pulldown or pullup resistor not activated).
   – DRIVE 1 (OFF): The buffer drives V_{OH} (pulldown or pullup resistor not activated).
   – OFF: High-impedance
   – PD: High-impedance with an active pulldown resistor
   – PU: High-impedance with an active pullup resistor

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– An empty box means Not Applicable.

NOTE

Designs that contain pullup or pulldown resistors, either on the board or in attached devices that oppose internal pullup or pulldown resistors, that are active while the device is held in reset, must not remain in reset for long periods of time.

7. **BALL RESET REL. STATE:** The state of the terminal at the deactivation of the rstoutn signal:
   – DRIVE 0 (OFF): The buffer drives V_{OL} (pulldown or pullup resistor not activated).
   – DRIVE 1 (OFF): The buffer drives V_{OH} (pulldown or pullup resistor not activated).
   – DRIVE CLK (OFF): The buffer drives a toggling clock (pulldown or pullup resistor not activated).
   – OFF: High-impedance
   – PD: High-impedance with an active pulldown resistor
   – PU: High-impedance with an active pullup resistor
   – An empty box means Not Applicable.

   For more information on the CORE_PWRON_RET_RST reset signal and its reset sources, see chapter *Device Configuration* of the Device TRM.
8. **BALL RESET REL. MUXMODE:** This muxmode is automatically configured at the release of the rstoutn signal.
   An empty box means Not Applicable.
9. **I/O VOLTAGE VALUE**: This column describes the IO voltage value (the corresponding power supply).
   An empty box means Not Applicable.
10. **POWER:** The voltage supply that powers the terminal IO buffers.
    An empty box means Not Applicable.
11. **HYS:** Indicates if the input buffer has hysteresis:
    – Yes: With hysteresis
    – No: Without hysteresis

    An empty box means No.

    For more information, see the hysteresis values in Section 5.7, *Electrical Characteristics*.
12. **BUFFER TYPE:** This column describes the associated output buffer type.

    An empty box means Not Applicable.

    For drive strength of the associated output buffer, refer to Section 5.7, *Electrical Characteristics*.
13. **PULL UP/DOWN TYPE:** Indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
    – PU: Internal pullup
    – PD: Internal pulldown
    – PU/PD: Internal pullup and pulldown
    – An empty box means No pull.

NOTE

Internal pullup or pulldown resistors must be disabled when opposed by an external pullup or pulldown resistor on the board or within an attached device.

14. **DSIS:** The deselected input state (DSIS) indicates the state driven on the peripheral input (logic "0", logic "1", or "PIN" level) when the peripheral pin function is not selected by any of the PINCNTLx registers:
    – 0: Logic 0 driven on the input signal port of the peripheral.
    – 1: Logic 1 driven on the input signal port of the peripheral.
    – An empty box means Not Applicable.

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NOTE

Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration.

NOTE

When a pad is set into a multiplexing mode that is not defined by pin multiplexing, behavior of that pad is undefined, this configuration shall be avoided.

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4.3 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

The following list describes the column headers:

1. **SIGNAL NAME:** The name of the signal passing through the pin.
2. **DESCRIPTION:** Description of the signal.
3. **PIN TYPE:** Signal direction and type:
   - I = Input
   - O = Output
   - IO = Input or Output
   - IOD = Input or Open-drain Output
   - IOZ = Input or Three-state Output
   - OZ = Three-state Output
   - A = Analog
   - PWR = Power
   - GND = Ground
   - CAP = LDO Capacitor
4. **ABY BALL:** Associated balls bottom.

   For more information on the I/O cell configurations, see section *Pad Configuration Registers* in section *Control Module (BOOT_CFG)* of chapter *Device Configuration* of the Device TRM.

4.3.1 DSS

Table 4-2. DSS Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
DSS_DATA0	DSS data output	OZ	V22
DSS_DATA1	DSS data output	OZ	U21
DSS_DATA2	DSS data output	OZ	W22
DSS_DATA3	DSS data output	OZ	V23
DSS_DATA4	DSS data output	OZ	U23
DSS_DATA5	DSS data output	OZ	V24
DSS_DATA6	DSS data output	OZ	T21
DSS_DATA7	DSS data output	OZ	U22
DSS_DATA8	DSS data output	OZ	T22
DSS_DATA9	DSS data output	OZ	R21
DSS_DATA10	DSS data output	OZ	U24
DSS_DATA11	DSS data output	OZ	V25
DSS_DATA12	DSS data output	OZ	T24
DSS_DATA13	DSS data output	OZ	P21
DSS_DATA14	DSS data output	OZ	U25
DSS_DATA15	DSS data output	OZ	R22
DSS_DATA16	DSS data output	OZ	P23
DSS_DATA17	DSS data output	OZ	R24
DSS_DATA18	DSS data output	OZ	N22
DSS_DATA19	DSS data output	OZ	T25
DSS_DATA20	DSS data output	OZ	N24
DSS_DATA21	DSS data output	OZ	P24
DSS_DATA22	DSS data output	OZ	P25
DSS_DATA23	DSS data output	OZ	N23

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Table 4-2. DSS Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
DSS_DE	DSS data enable output	OZ	M25
DSS_FID	DSS field ID output. This signal is not used for embedded sync modes	OZ	L25
DSS_HSYNC	DSS horizontal sync output. This signal is not used for embedded sync modes	OZ	P22
DSS_PCLK	DSS clock output	OZ	N25
DSS_VSYNC	DSS vertical sync output. This signal is not used for embedded sync modes	OZ	R25
DSS RFBI Mode			
DSS_RFBI_A0	RFBI A0 indicate the status of the data: command or data (Polarity is programmable)	OZ	L25
DSS_RFBI_CSn0	RFBI LCD chip select 0 (Polarity is programmable)	OZ	P23
DSS_RFBI_CSn1	RFBI LCD chip select 1 (Polarity is programmable)	OZ	R24
DSS_RFBI_DATA0	RFBI data read/write to LCD panel clock reference: asynchronous	IOZ	V22
DSS_RFBI_DATA1	RFBI data read/write to LCD panel lclock reference: asynchronous	IOZ	U21
DSS_RFBI_DATA2	RFBI data read/write to LCD panel clock reference: asynchronous	IOZ	W22
DSS_RFBI_DATA3	RFBI data read/write to LCD panel lclock reference: asynchronous	IOZ	V23
DSS_RFBI_DATA4	RFBI data read/write to LCD panel clock reference: asynchronous	IOZ	U23
DSS_RFBI_DATA5	RFBI data read/write to LCD panel lclock reference: asynchronous	IOZ	V24
DSS_RFBI_DATA6	RFBI data read/write to LCD panel clock reference: asynchronous	IOZ	T21
DSS_RFBI_DATA7	RFBI data read/write to LCD panel lclock reference: asynchronous	IOZ	U22
DSS_RFBI_DATA8	RFBI data read/write to LCD panel clock reference: asynchronous	IOZ	T22
DSS_RFBI_DATA9	RFBI data read/write to LCD panel lclock reference: asynchronous	IOZ	R21
DSS_RFBI_DATA10	RFBI data read/write to LCD panel clock reference: asynchronous	IOZ	U24
DSS_RFBI_DATA11	RFBI data read/write to LCD panel lclock reference: asynchronous	IOZ	V25
DSS_RFBI_DATA12	RFBI data read/write to LCD panel clock reference: asynchronous	IOZ	T24
DSS_RFBI_DATA13	RFBI data read/write to LCD panel lclock reference: asynchronous	IOZ	P21
DSS_RFBI_DATA14	RFBI data read/write to LCD panel clock reference: asynchronous	IOZ	U25
DSS_RFBI_DATA15	RFBI data read/write to LCD panel lclock reference: asynchronous	IOZ	R22
DSS_RFBI_HSYNC0	RFBI horizontal synchronization input 0 HSYNC pulse signals clock reference: asynchronous	I	P22
DSS_RFBI_HSYNC1	RFBI horizontal synchronization input 1 HSYNC pulse signals clock reference: asynchronous	I	N22
DSS_RFBI_REn	RFBI read enable (Polarity is programmable) indicate when a read is on going from the embedded emory in the LCD panel clock reference.	OZ	N25
DSS_RFBI_TEVSYNC0	RFBI vertical synchronization input 0 TE (Tearing Effect) pulse signal or the LCD panel VSYNC (Vertical Synchronization) clock reference: asynchronous	I	R25

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Table 4-2. DSS Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
DSS_RFBI_TEVSYNC1	RFBI vertical synchronization input 1 TE (Tearing Effect) pulse signal or the LCD panel VSYNC (Vertical Synchronization) clock reference: asynchronous	I	T25
DSS_RFBI_WEn	RFBI LCD write enable (Polarity is programmable)	OZ	M25

4.3.2 DDR EMIF

Table 4-3. DDR External Memory Interface Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
DDR3_A00	EMIF address bit 00 output	OZ	AC15
DDR3_A01	EMIF address bit 01 output	OZ	Y15
DDR3_A02	EMIF address bit 02 output	OZ	AC16
DDR3_A03	EMIF address bit 03 output	OZ	AA15
DDR3_A04	EMIF address bit 04 output	OZ	AB16
DDR3_A05	EMIF address bit 05 output	OZ	AE17
DDR3_A06	EMIF address bit 06 output	OZ	AC14
DDR3_A07	EMIF address bit 07 output	OZ	AB15
DDR3_A08	EMIF address bit 08 output	OZ	AC17
DDR3_A09	EMIF address bit 09 output	OZ	AB17
DDR3_A10	EMIF address bit 10 output	OZ	AB14
DDR3_A11	EMIF address bit 11 output	OZ	AA16
DDR3_A12	EMIF address bit 12 output	OZ	AA17
DDR3_A13	EMIF address bit 13 output	OZ	AA12
DDR3_A14	EMIF address bit 14 output	OZ	Y17
DDR3_A15	EMIF address bit 15 output	OZ	Y16
DDR3_BA0	EMIF bank address 0 output	OZ	AA14
DDR3_BA1	EMIF bank address 1 output	OZ	AB13
DDR3_BA2	EMIF bank address 2 output	OZ	AD17
DDR3_CASn	EMIF column address strobe output	OZ	AC13
DDR3_CB00	EMIF ECC check bit 00 input/output	IOZ	AA11
DDR3_CB01	EMIF ECC check bit 01 input/output	IOZ	AB11
DDR3_CB02	EMIF ECC check bit 02 input/output	IOZ	AC11
DDR3_CB03	EMIF ECC check bit 03 input/output	IOZ	AC12
DDR3_CBDQM	EMIF ECC check bits data mask output	OZ	Y11
DDR3_CBDQS_N	EMIF ECC check bit data strobe input/output (negative)	IOZ	AD12
DDR3_CBDQS_P	EMIF ECC check bit data strobe input/output (positive)	IOZ	AE12
DDR3_CEn0	EMIF chip enable 0 output (Active Low)	OZ	AD13
DDR3_CKE0	EMIF clock enable 0 output	OZ	AB18
DDR3_CLKOUT_N0	EMIF differential clock 0 output (negative)	OZ	AD15
DDR3_CLKOUT_P0	EMIF differential clock 0 output (positive)	OZ	AE15
DDR3_CLKOUT_N1	EMIF differential clock 1 output (negative)	OZ	AD16
DDR3_CLKOUT_P1	EMIF differential clock 1 output (positive)	OZ	AE16
DDR3_D00	EMIF data bit 00 input/output	IOZ	AD2
DDR3_D01	EMIF data bit 01 input/output	IOZ	Y4
DDR3_D02	EMIF data bit 02 input/output	IOZ	AC3
DDR3_D03	EMIF data bit 03 input/output	IOZ	AC2

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Table 4-3. DDR External Memory Interface Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
DDR3_D04	EMIF data bit 04 input/output	IOZ	AE3
DDR3_D05	EMIF data bit 05 input/output	IOZ	AA4
DDR3_D06	EMIF data bit 06 input/output	IOZ	AD3
DDR3_D07	EMIF data bit 07 input/output	IOZ	AB3
DDR3_D08	EMIF data bit 08 input/output	IOZ	AA6
DDR3_D09	EMIF data bit 09 input/output	IOZ	Y7
DDR3_D10	EMIF data bit 10 input/output	IOZ	Y6
DDR3_D11	EMIF data bit 11 input/output	IOZ	AC5
DDR3_D12	EMIF data bit 12 input/output	IOZ	AB6
DDR3_D13	EMIF data bit 13 input/output	IOZ	Y5
DDR3_D14	EMIF data bit 14 input/output	IOZ	AC4
DDR3_D15	EMIF data bit 15 input/output	IOZ	AB5
DDR3_D16	EMIF data bit 16 input/output	IOZ	AB7
DDR3_D17	EMIF data bit 17 input/output	IOZ	AB8
DDR3_D18	EMIF data bit 18 input/output	IOZ	AC7
DDR3_D19	EMIF data bit 19 input/output	IOZ	AA7
DDR3_D20	EMIF data bit 20 input/output	IOZ	AA8
DDR3_D21	EMIF data bit 21 input/output	IOZ	AC6
DDR3_D22	EMIF data bit 22 input/output	IOZ	AE7
DDR3_D23	EMIF data bit 23 input/output	IOZ	AD7
DDR3_D24	EMIF data bit 24 input/output	IOZ	AA10
DDR3_D25	EMIF data bit 25 input/output	IOZ	AE10
DDR3_D26	EMIF data bit 26 input/output	IOZ	AD10
DDR3_D27	EMIF data bit 27 input/output	IOZ	AC10
DDR3_D28	EMIF data bit 28 input/output	IOZ	AC9
DDR3_D29	EMIF data bit 29 input/output	IOZ	AB10
DDR3_D30	EMIF data bit 30 input/output	IOZ	AB9
DDR3_D31	EMIF data bit 31 input/output	IOZ	Y8
DDR3_DQM0	EMIF data mask 0 output for byte 0 of the 32-bit data bus	OZ	AB4
DDR3_DQM1	EMIF data mask 1 output for byte 1 of the 32-bit data bus	OZ	AA5
DDR3_DQM2	EMIF data mask 2 output for byte 2 of the 32-bit data bus	OZ	AC8
DDR3_DQM3	EMIF data mask 3 output for byte 3 of the 32-bit data bus	OZ	AA9
DDR3_DQS0_N	EMIF differential data strobe 0 negative input/output for byte 0 of the 32-bit data bus. This signal is a output to the DDR3L memory when writing and a input when reading.	IOZ	AE2
DDR3_DQS0_P	EMIF differential data strobe 0 positive input/output for byte 0 of the 32-bit data bus. This signal is a output to the DDR3L memory when writing and a input when reading.	IOZ	AD1
DDR3_DQS1_N	EMIF differential data strobe 1 negative input/output for byte 1 of the 32-bit data bus. This signal is a output to the DDR3L memory when writing and a input when reading.	IOZ	AE4
DDR3_DQS1_P	EMIF differential data strobe 1 positive input/output for byte 1 of the 32-bit data bus. This signal is a output to the DDR3L memory when writing and a input when reading.	IOZ	AD4
DDR3_DQS2_N	EMIF differential data strobe 2 negative input/output for byte 2 of the 32-bit data bus. This signal is a output to the DDR3L memory when writing and a input when reading.	IOZ	AD6
DDR3_DQS2_P	EMIF differential data strobe 2 positive input/output for byte 2 of the 32-bit data bus. This signal is a output to the DDR3L memory when writing and a input when reading.	IOZ	AE6

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Table 4-3. DDR External Memory Interface Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
DDR3_DQS3_N	EMIF differential data strobe 3 negative input/output for byte 3 of the 32-bit data bus. This signal is a output to the DDR3L memory when writing and a input when reading.	IOZ	AD9
DDR3_DQS3_P	EMIF differential data strobe 3 positive input/output for byte 3 of the 32-bit data bus. This signal is a output to the DDR3L memory when writing and a input when reading.	IOZ	AE9
DDR3_ODT0	EMIF on-die termination output for chip select 0	OZ	AA13
DDR3_RASn	EMIF row address strobe output	OZ	AE13
DDR3_RESETn	EMIF reset output (DDR3L-SDRAM only)	OZ	Y18
DDR3_RZQ0	EMIF calibration resistor. An external 240 Ω ±1% resistor must be connected between this pin and VSS.	A	W12
DDR3_RZQ1	EMIF calibration resistor. An external 240 Ω ±1% resistor must be connected between this pin and VSS.	A	V9
DDR3_WEn	EMIF write enable output	OZ	Y13
DDR_CLK_N	EMIF DPLL differential reference clock input (Negative)	I	AD24
DDR_CLK_P	EMIF DPLL differential reference clock input (Positive)	I	AE24

For more information, see section *DDR Extrenal Memory Interface (EMIF)* in chapter *Memory Subsystem* of the Device TRM.

4.3.3 GPMC

Table 4-4. GPMC Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
GPMC_A0	GPMC address 0. Only used to effectively address 8-bit data nonmultiplexed memories.	OZ	M25
GPMC_A1	GPMC address 1 in A/D nonmultiplexed mode and address 17 in A/D multiplexed mode	OZ	V22
GPMC_A2	GPMC address 2 in A/D nonmultiplexed mode and address 18 in A/D multiplexed mode	OZ	U21
GPMC_A3	GPMC address 3 in A/D nonmultiplexed mode and address 19 in A/D multiplexed mode	OZ	W22
GPMC_A4	GPMC address 4 in A/D nonmultiplexed mode and address 20 in A/D multiplexed mode	OZ	V23
GPMC_A5	GPMC address 5 in A/D nonmultiplexed mode and address 21 in A/D multiplexed mode	OZ	U23
GPMC_A6	GPMC address 6 in A/D nonmultiplexed mode and address 22 in A/D multiplexed mode	OZ	V24
GPMC_A7	GPMC address 7 in A/D nonmultiplexed mode and address 23 in A/D multiplexed mode	OZ	T21
GPMC_A8	GPMC address 8 in A/D nonmultiplexed mode and address 24 in A/D multiplexed mode	OZ	U22
GPMC_A9	GPMC address 9 in A/D nonmultiplexed mode and address 25 in A/D multiplexed mode	OZ	T22
GPMC_A10	GPMC address 10 in A/D nonmultiplexed mode and address 26 in A/D multiplexed mode	OZ	R21
GPMC_A11	GPMC address 11 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	OZ	U24
GPMC_A12	GPMC address 12 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	OZ	V25
GPMC_A13	GPMC address 13 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	OZ	T24

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Table 4-4. GPMC Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
GPMC_A14	GPMC address 14 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	OZ	P21
GPMC_A15	GPMC address 15 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	OZ	U25
GPMC_A16	GPMC address 16 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	OZ	R22
GPMC_A17	GPMC address 17 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	OZ	P23
GPMC_A18	GPMC address 18 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	OZ	R24
GPMC_A19	GPMC address 19 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	OZ	N22
GPMC_A20	GPMC address 20 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	OZ	T25
GPMC_A21	GPMC address 21 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	OZ	N24
GPMC_A22	GPMC address 22 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	OZ	P24
GPMC_A23	GPMC address 23 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	OZ	P25
GPMC_A24	GPMC address 24 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	OZ	N23
GPMC_A25	GPMC address 25 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	OZ	R25
GPMC_A26	GPMC address 26 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	OZ	P22
GPMC_A27	GPMC address 27 in A/D nonmultiplexed mode and address 27 in A/D multiplexed mode	OZ	N25
GPMC_AD0	GPMC data 0 in A/D nonmultiplexed mode and additionally address 1 in A/D multiplexed mode	IOZ	AC21
GPMC_AD1	GPMC data 1 in A/D nonmultiplexed mode and additionally address 2 in A/D multiplexed mode	IOZ	AE20
GPMC_AD2	GPMC data 2 in A/D nonmultiplexed mode and additionally address 3 in A/D multiplexed mode	IOZ	AD22
GPMC_AD3	GPMC data 3 in A/D nonmultiplexed mode and additionally address 4 in A/D multiplexed mode	IOZ	AD20
GPMC_AD4	GPMC data 4 in A/D nonmultiplexed mode and additionally address 5 in A/D multiplexed mode	IOZ	AE21
GPMC_AD5	GPMC data 5 in A/D nonmultiplexed mode and additionally address 6 in A/D multiplexed mode	IOZ	AE22
GPMC_AD6	GPMC data 6 in A/D nonmultiplexed mode and additionally address 7 in A/D multiplexed mode	IOZ	AC20
GPMC_AD7	GPMC data 7 in A/D nonmultiplexed mode and additionally address 8 in A/D multiplexed mode	IOZ	AD21
GPMC_AD8	GPMC data 8 in A/D nonmultiplexed mode and additionally address 9 in A/D multiplexed mode	IOZ	AE23
GPMC_AD9	GPMC data 9 in A/D nonmultiplexed mode and additionally address 10 in A/D multiplexed mode	IOZ	AB20
GPMC_AD10	GPMC data 10 in A/D nonmultiplexed mode and additionally address 11 in A/D multiplexed mode	IOZ	AA20
GPMC_AD11	GPMC data 11 in A/D nonmultiplexed mode and additionally address 12 in A/D multiplexed mode	IOZ	AD23
GPMC_AD12	GPMC data 12 in A/D nonmultiplexed mode and additionally address 13 in A/D multiplexed mode	IOZ	AA21

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Table 4-4. GPMC Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
GPMC_AD13	GPMC data 13 in A/D nonmultiplexed mode and additionally address 14 in A/D multiplexed mode	IOZ	AB21
GPMC_AD14	GPMC data 14 in A/D nonmultiplexed mode and additionally address 15 in A/D multiplexed mode	IOZ	AB22
GPMC_AD15	GPMC data 15 in A/D nonmultiplexed mode and additionally address 16 in A/D multiplexed mode	IOZ	AA22
GPMC_ADVn_ALE	GPMC address valid active low or address latch enable	OZ	AC23
GPMC_BEn1	GPMC upper-byte enable (Active Low)	OZ	AB24
GPMC_BEn0_CLE	GPMC lower-byte enable (Active Low)	OZ	AC24
GPMC_CLK(1)	GPMC clock output	IOZ	AB23
GPMC_CSn0	GPMC chip select 0 (Active Low)	OZ	AB25
GPMC_CSn1	GPMC chip select 1 (Active Low)	OZ	W24
GPMC_CSn2	GPMC chip select 2 (Active Low)	OZ	W23
GPMC_CSn3	GPMC chip select 3 (Active Low)	OZ	Y25
GPMC_DIR	GPMC direction	OZ	AA25
GPMC_OEn_REn	GPMC output enable (Active Low) or read enable	OZ	AC22
GPMC_WAIT0	GPMC external indication of wait 0	I	Y24
GPMC_WAIT1	GPMC external indication of wait 1	I	AA24
GPMC_WEn	GPMC write enable (Active Low)	OZ	Y22
GPMC_WPn	GPMC flash write protect (Active Low)	OZ	W25

(1) This clock signal is implemented as *pad loopback* inside the device — the output signal is looped back through the input buffer to serve as the internal reference signal. Series termination is required (as close as possible to device pin) to improve signal integrity of the clock input.

For more information, see section *General-Purpose Memory Controller (GPMC)* in chapter *Memory Subsystem* of the Device TRM.

4.3.4 Timers

Table 4-5. Timer Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
TIMI0	Timer input for TIMERS [4:0]	I	T2
TIMI1	Timer input for TIMERS [4:0]	I	W23
TIMO0	Timer output for TIMERS [4:0]	OZ	U1
TIMO1	Timer output for TIMERS [4:0]	OZ	Y25

For more information, see section *Timers* in chapter *Peripherals* of the Device TRM.

4.3.5 I2C

Table 4-6. I2C Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
I2C0_SCL(1)	I2C0 clock I/O	IOD	U5
I2C0_SDA	I2C0 data I/O	IOD	W5
I2C1_SCL(1)	I2C1 clock I/O	IOD	V6
I2C1_SDA	I2C1 data I/O	IOD	W4
I2C2_SCL(1)	I2C2 clock I/O	IOD	V5
I2C2_SDA	I2C2 data I/O	IOD	V4

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(1) This clock signal is implemented as pad loopback inside the device — the output signal is looped back through the input buffer to serve as the internal reference signal. Series termination is required (as close as possible to device pin) to improve signal integrity of the clock input.

For more information, see section *Inter-IC module (I2C)* in chapter *Peripherals* of the Device TRM.

4.3.6 UART

Table 4-7. UART Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
UART0_CTSn	UART0 clear to send (Active Low)	I	T2
UART0_DCDn	UART0 data carrier detect (Active Low)	I	E21
UART0_DSRn	UART0 data set ready (Active Low)	I	D21
UART0_DTRn	UART0 data terminal ready (Active Low)	OZ	D22
UART0_RIN	UART0 ring indicator input	I	C21
UART0_RTSn	UART0 request to send (Active Low)	OZ	U1
UART0_RXD	UART0 receive data input	I	T4
UART0_TXD	UART0 transmit data output	OZ	T1
UART1_CTSn	UART1 clear to send (Active Low)	I	U2
UART1_RTSn	UART1 request to send (Active Low)	OZ	U4
UART1_RXD	UART1 receive data input	I	T3
UART1_TXD	UART1 transmit data output	OZ	T5
UART2_CTSn	UART2 clear to send (Active Low)	I	D22
UART2_RTSn	UART2 request to send (Active Low)	OZ	C21
UART2_RXD	UART2 receive data input for UART mode	I	E21
UART2_TXD	UART2 transmit data output	OZ	D21

For more information, see section *Universal Asynchronous Receiver/Transmitter (UART)* in chapter *Peripherals* of the Device TRM.

4.3.7 SPI

Table 4-8. SPI Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
SPI0_CLK(1)	SPI clock I/O	IOZ	M2
SPI0_SCSn0	SPI chip select I/O (Active Low)	IOZ	M3
SPI0_SCSn1	SPI chip select I/O (Active Low)	IOZ	M4
SPI0_SIMO	SPI data output	IOZ	N4
SPI0_SOMI	SPI data input	IOZ	M1
SPI1_CLK(1)	SPI clock I/O	IOZ	N2
SPI1_SCSn0	SPI chip select I/O (Active Low)	IOZ	P1
SPI1_SCSn1	SPI chip select I/O (Active Low)	IOZ	N3
SPI1_SIMO	SPI data output	IOZ	P2
SPI1_SOMI	SPI data input	IOZ	N1
SPI2_CLK(1)	SPI clock I/O	IOZ	R2
SPI2_SCSn0	SPI chip select I/O (Active Low)	IOZ	P3
SPI2_SCSn1	SPI chip select I/O (Active Low)	IOZ	P4
SPI2_SIMO	SPI data output	IOZ	R3
SPI2_SOMI	SPI data input	IOZ	R4
SPI3_CLK(1)	SPI clock I/O	IOZ	E24

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Table 4-8. SPI Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
SPI3_SCSn0	SPI chip select I/O (Active Low)	IOZ	C24
SPI3_SCSn1	SPI chip select I/O (Active Low)	IOZ	E25
SPI3_SIMO	SPI data output	IOZ	F24
SPI3_SOMI	SPI data input	IOZ	F25

(1) This clock signal is implemented as *pad loopback* inside the device — the output signal is looped back through the input buffer to serve as the internal reference signal. Series termination is required (as close as possible to device pin) to improve signal integrity of the clock input.

For more information, see section *Serial Peripheral Interface (SPI)* in chapter *Peripherals* of the Device TRM.

4.3.8 QSPI

Table 4-9. QSPI Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
QSPI_CLK(1)	QSPI serial clock output	OZ	K25
QSPI_CSn0	QSPI chip select 0 (Active Low). This pin is used for QSPI boot modes.	OZ	J25
QSPI_CSn1	QSPI chip select 1 (Active Low)	OZ	H23
QSPI_CSn2	QSPI chip select 2 (Active Low)	OZ	H22
QSPI_CSn3	QSPI chip select 3 (Active Low)	OZ	H21
QSPI_D0	QSPI data 0. This pin is output data for all commands and writes. For dual read and quad read modes, it becomes input data pin during read phase.	IOZ	J23
QSPI_D1	QSPI data 1. Input read data in all modes.	IOZ	J22
QSPI_D2	QSPI data 2. This pin is used only in quad read mode as input data pin during read phase.	IOZ	J21
QSPI_D3	QSPI data 3. This pin is used only in quad read mode as input data pin during read phase.	IOZ	J24
QSPI_RCLK(1)	QSPI return clock input. Must be connected from QSPI_SCLK on PCB. Refer to PCB Guidelines for QSPI.	I	K24

(1) QSPI uses an external loopback clock strategy to support higher operating frequencies. QSPI_CLK is the clock source which must be connected to the clock input of all attached devices including QSPI_RCLK which is the clock input for this device. The QSPI clock PCB signal trace shall be designed using signal integrity analysis to insure impedance mismatches of this multi-point connection does not produce non-monotonic events while the clock transitions through the switching threshold of attached input buffers. If this occurs, the non-monotonic events may create internal clock glitches that cause unpredictable behavior of QSPI.

For more information, see section *Quad Serial Peripheral Interface (QSPI)* in chapter *Peripherals* of the Device TRM.

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4.3.9 McASP

Table 4-10. McASP Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
MCASP0_ACLKR(1)	McASP0 receive bit clock I/O	IOZ	E9
MCASP0_ACLKX(1)	McASP0 transmit bit clock I/O	IOZ	D9
MCASP0_AFSR	McASP0 receive frame sync I/O	IOZ	A8
MCASP0_AFSX	McASP0 transmit frame sync I/O	IOZ	C8
MCASP0_AHCLKR(1)	McASP0 receive high-frequency master clock I/O	IOZ	B8
MCASP0_AHCLKX(1)	McASP0 transmit high-frequency master clock output	OZ	C9
MCASP0_AMUTE	McASP0 mute	IOZ	C7
MCASP0_AXR0	McASP0 transmit and receive data I/O	IOZ	B9
MCASP0_AXR1	McASP0 transmit and receive data I/O	IOZ	A9
MCASP0_AXR2	McASP0 transmit and receive data I/O	IOZ	B10
MCASP0_AXR3	McASP0 transmit and receive data I/O	IOZ	A10
MCASP0_AXR4	McASP0 transmit and receive data I/O	IOZ	C10
MCASP0_AXR5	McASP0 transmit and receive data I/O	IOZ	E10
MCASP0_AXR6	McASP0 transmit and receive data I/O	IOZ	D10
MCASP0_AXR7	McASP0 transmit and receive data I/O	IOZ	F10
MCASP0_AXR8	McASP0 transmit and receive data I/O	IOZ	C11
MCASP0_AXR9	McASP0 transmit and receive data I/O	IOZ	D11
MCASP0_AXR10	McASP0 transmit and receive data I/O	IOZ	E11
MCASP0_AXR11	McASP0 transmit and receive data I/O	IOZ	F12
MCASP0_AXR12	McASP0 transmit and receive data I/O	IOZ	E12
MCASP0_AXR13	McASP0 transmit and receive data I/O	IOZ	C12
MCASP0_AXR14	McASP0 transmit and receive data I/O	IOZ	B11
MCASP0_AXR15	McASP0 transmit and receive data I/O	IOZ	B12
MCASP1_ACLKR(1)	McASP1 receive bit clock I/O	IOZ	B4
MCASP1_ACLKX(1)	McASP1 transmit bit clock I/O	IOZ	D6
MCASP1_AFSR	McASP1 receive frame sync I/O	IOZ	A4
MCASP1_AFSX	McASP1 transmit frame sync I/O	IOZ	C4
MCASP1_AHCLKR(1)	McASP1 receive high-frequency master clock I/O	IOZ	E7
MCASP1_AHCLKX(1)	McASP1 transmit high-frequency master clock output	OZ	C5
MCASP1_AMUTE	McASP1 mute	IOZ	A5
MCASP1_AXR0	McASP1 transmit and receive data I/O	IOZ	B5
MCASP1_AXR1	McASP1 transmit and receive data I/O	IOZ	B6
MCASP1_AXR2	McASP1 transmit and receive data I/O	IOZ	D7
MCASP1_AXR3	McASP1 transmit and receive data I/O	IOZ	A6
MCASP1_AXR4	McASP1 transmit and receive data I/O	IOZ	C6
MCASP1_AXR5	McASP1 transmit and receive data I/O	IOZ	E8
MCASP1_AXR6	McASP1 transmit and receive data I/O	IOZ	A7
MCASP1_AXR7	McASP1 transmit and receive data I/O	IOZ	D8
MCASP1_AXR8	McASP1 transmit and receive data I/O	IOZ	F9
MCASP1_AXR9	McASP1 transmit and receive data I/O	IOZ	B7
MCASP2_ACLKR(1)	McASP2 receive bit clock I/O	IOZ	B2
MCASP2_ACLKX(1)	McASP2 transmit bit clock I/O	IOZ	B3
MCASP2_AFSR	McASP2 receive frame sync I/O	IOZ	D4
MCASP2_AFSX	McASP2 transmit frame sync I/O	IOZ	C3
MCASP2_AHCLKR(1)	McASP2 receive high-frequency master clock I/O	IOZ	E6

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Table 4-10. McASP Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
MCASP2_AHCLKX(1)	McASP2 transmit high-frequency master clock output	OZ	D5
MCASP2_AMUTE	McASP2 mute	IOZ	C2
MCASP2_AXR0	McASP2 transmit and receive data I/O	IOZ	D3
MCASP2_AXR1	McASP2 transmit and receive data I/O	IOZ	A2
MCASP2_AXR2	McASP2 transmit and receive data I/O	IOZ	E4
MCASP2_AXR3	McASP2 transmit and receive data I/O	IOZ	B1
MCASP2_AXR4	McASP2 transmit and receive data I/O	IOZ	A3
MCASP2_AXR5	McASP2 transmit and receive data I/O	IOZ	E5

(1) This clock signal is implemented as *pad loopback* inside the device — the output signal is looped back through the input buffer to serve as the internal reference signal. Series termination is required (as close as possible to device pin) to improve signal integrity of the clock input.

For more information, see section *Multi-channel Audio Serial Port (McASP)* in chapter *Peripherals* of the Device TRM.

4.3.10 USB

Table 4-11. USB Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
USB0_DM	USB0 differential data signal pair (negative)	IO	B18
USB0_DP	USB0 differential data signal pair (positive)	IO	A18
USB0_DRVVBUS	USB0 drive VBUS output	OZ	E19
USB0_EXT_TRIGGER	USB0 external trigger Input	I	H22
USB0_ID	USB0 identify device, connection to resistor that determines mode of operation	A	A19
USB0_TXRTUNE_RKELVIN	USB0 Kelvin connection to termination calibration resistor (200 Ω ±1%)	A	C19
USB0_VBUS	USB0 VBUS comparator input	A	B19
USB0_XO	USB0 optional PHY reference clock input	I	D19
USB1_DM	USB1 differential data signal pair (negative)	IO	A20
USB1_DP	USB1 differential data signal pair (positive)	IO	B20
USB1_DRVVBUS	USB1 drive VBUS output	OZ	B21
USB1_EXT_TRIGGER	USB1 external trigger Input	I	H21
USB1_ID	USB1 identify device pin, determines mode of operation	A	E20
USB1_TXRTUNE_RKELVIN	USB1 Kelvin connection to termination calibration resistor (200 Ω ±1%)	A	D20
USB1_VBUS	USB1 VBUS comparator input	A	A21
USB1_XO	USB1 optional PHY reference clock input	I	C20

For more information, see section *Universal Serial Bus Subsystem (USB)* in chapter *Peripherals* of the Device TRM.

4.3.11 PCIESS

Table 4-12. PCIESS Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
PCIE_CLK_N	PCIe clock input (negative)	I	F2
PCIE_CLK_P	PCIe clock input (positive)	I	G2

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Table 4-12. PCIESS Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
PCIE_REFRES	PCIe SerDes reference resistor input (3 kΩ ±1%)	A	H7
PCIE_RXN0	PCIe receive data lane 0 (negative)	I	D1
PCIE_RXP0	PCIe receive data lane 0 (positive)	I	E1
PCIE_TXN0	PCIe transmit data lane 0 (negative)	O	H1
PCIE_TXP0	PCIe transmit data lane 0 (positive)	O	G1

For more information, see section *Peripheral Component Interconnect Express Subsystem (PCIe SS)* in chapter *Peripherals* of the Device TRM.

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4.3.12 DCAN

Table 4-13. DCAN Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
DCAN0_RX	DCAN0 receive data pin	I	R5
DCAN0_TX	DCAN0 transmit data pin	OZ	P5
DCAN1_RX	DCAN1 receive data pin	I	H21
DCAN1_TX	DCAN1 transmit data pin	OZ	H22

For more information, see section *Dual Controller Area Network (DCAN) Interface* in chapter *Peripherals* of the Device TRM.

4.3.13 EMAC

Table 4-14. EMAC Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
CPTS_HW1_TSPUSH	CPTS hardware time stamp push input 1	I	E21
CPTS_HW2_TSPUSH	CPTS hardware time stamp push input 2	I	D21
CPTS_TS_COMP	CPTS time stamp counter compare output	OZ	C21
CPTS_TS_SYNC	CPTS time stamp counter bit output	OZ	D22
MDIO_CLK	MDIO clock	OZ	U3
MDIO_DATA	MDIO data	IOZ	V3
MII_COL	MII collision detect (sense) input	I	B25
MII_CRS	MII carrier sense input	I	G22
MII_RXCLK	MII receive clock	I	A22
MII_RXD0	MII receive data 0	I	B24
MII_RXD1	MII receive data 1	I	C23
MII_RXD2	MII receive data 2	I	B23
MII_RXD3	MII receive data 3	I	F22
MII_RXDV	MII receive data valid input	I	A24
MII_RXER	MII receive data error input	I	F23
MII_TXCLK	MII transmit clock	I	C25
MII_TXD0	MII transmit data 0	OZ	G23
MII_TXD1	MII transmit data 1	OZ	G24
MII_TXD2	MII transmit data 2	OZ	G25
MII_TXD3	MII transmit data 3	OZ	D25
MII_TXEN	MII transmit data enable output	OZ	H25
MII_TXER	MII transmit data error output	OZ	H24
RGMII_RXC	RGMII receive clock	I	A22
RGMII_RXCTL	RGMII receive control	I	A24
RGMII_RXD0	RGMII receive data	I	B24
RGMII_RXD1	RGMII receive data	I	C23
RGMII_RXD2	RGMII receive data	I	B23
RGMII_RXD3	RGMII receive data	I	F22
RGMII_TXC	RGMII transmit clock	IOZ	C25
RGMII_TXCTL	RGMII transmit enable	OZ	H25
RGMII_TXD0	RGMII transmit data	OZ	G23
RGMII_TXD1	RGMII transmit data	OZ	G24
RGMII_TXD2	RGMII transmit data	OZ	G25

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Table 4-14. EMAC Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
RGMII_TXD3	RGMII transmit data	OZ	D25
RMII_CRS_DV	RMII carrier sense input	I	G22
RMII_REFCLK(1)	50-MHz RMII clock. Typically sourced from the CLKOUT pin	I	D24
RMII_RXD0	RMII receive data	I	B24
RMII_RXD1	RMII receive data	I	C23
RMII_RXER	RMII receive data error input	I	F23
RMII_TXD0	RMII transmit data	OZ	G23
RMII_TXD1	RMII transmit data	OZ	G24
RMII_TXEN	RMII transmit data enable output	OZ	H25

(1) RMII_REFCLK pad loopback is not supported on this device. An external 50 MHz clock source can be used to source RMII_REFCLK, or CLKOUT may be configured as a 50 MHz reference clock with an external connection to RMII_REFCLK. For either case, the RMII reference clock PCB signal trace is a multi-point connection which shall be designed using signal integrity analysis to insure impedance mismatches of this multi-point connection does not produce non-monotonic events while the clock transitions through the switching threshold of attached input buffers. If this occurs, the non-monotonic events may create internal clock glitches that cause unpredictable behavior of RMII.

For more information, see section *Networking Subsystem (NSS)*, *Gigabit Ethernet MAC (EMAC) Subsystem* in chapter *Peripherals* of the Device TRM.

4.3.14 MLB

Table 4-15. MLB Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
MLBP_CLK_N	Media Local Bus Subsystem (MLB) clock input differential pair (negative)	I	L23
MLBP_CLK_P	Media Local Bus Subsystem (MLB) clock input differential pair (positive)	I	M23
MLBP_DAT_N	Media Local Bus Subsystem (MLB) data input and output differential pair (negative)	IO	K22
MLBP_DAT_P	Media Local Bus Subsystem (MLB) data input and output differential pair (positive)	IO	K23
MLBP_SIG_N	Media Local Bus Subsystem (MLB) signal input and output differential pair (negative)	IO	M24
MLBP_SIG_P	Media Local Bus Subsystem (MLB) signal input and output differential pair (positive)	IO	L24
MLB_CLK	Media Local Bus Subsystem (MLB) clock input	I	AA24
MLB_DAT	Media Local Bus Subsystem (MLB) data input and output	IOZ	W24
MLB_SIG	Media Local Bus Subsystem (MLB) signal input and output	IOZ	AA25

For more information, see section *Media Local Bus (MLB)* in chapter *Peripherals* of the Device TRM.

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4.3.15 McBSP

Table 4-16. McBSP Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
MCBSP_CLKR(1)	McBSP received serial clock	IOZ	D17
MCBSP_CLKX(1)	McBSP transmitted serial clock	IOZ	B16
MCBSP_DR	McBSP received serial data	I	D15
MCBSP_DX	McBSP transmitted serial data	OZ	A16
MCBSP_FSR	McBSP received frame synchronization	IOZ	C16
MCBSP_FSX	McBSP transmitted frame synchronization	IOZ	E15

(1) This clock signal is implemented as pad loopback inside the device — the output signal is looped back through the input buffer to serve as the internal reference signal. Series termination is required (as close as possible to device pin) to improve signal integrity of the clock input.

For more information, see section *Multi-channel Buffered Serial Port (McBSP)* in chapter *Peripherals* of the Device TRM.

4.3.16 MMC/SD

Table 4-17. MMC/SD Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
MMC0_CLK(1)	MMC0 clock	IOZ	F13
MMC0_CMD	MMC0 command	IOZ	C13
MMC0_DAT0	MMC0 data bit 0	IOZ	B13
MMC0_DAT1	MMC0 data bit 1	IOZ	A13
MMC0_DAT2	MMC0 data bit 2	IOZ	A11
MMC0_DAT3	MMC0 data bit 3	IOZ	A12
MMC0_DAT4	MMC0 data bit 4	IOZ	B12
MMC0_DAT5	MMC0 data bit 5	IOZ	B11
MMC0_DAT6	MMC0 data bit 6	IOZ	C12
MMC0_DAT7	MMC0 data bit 7	IOZ	E12
MMC0_POW	MMC/SD cards on/off power supply control	OZ	D11
MMC0_SDCD	MMC0 card detect	I	F12
MMC0_SDWP	MMC0 write protect	I	E11
MMC1_CLK(1)	MMC1 clock	IOZ	J4
MMC1_CMD	MMC1 command	IOZ	J2
MMC1_DAT0	MMC1 data bit 0	IOZ	H3
MMC1_DAT1	MMC1 data bit 1	IOZ	F5
MMC1_DAT2	MMC1 data bit 2	IOZ	J5
MMC1_DAT3	MMC1 data bit 3	IOZ	H4
MMC1_DAT4	MMC1 data bit 4	IOZ	E3
MMC1_DAT5	MMC1 data bit 5	IOZ	G4
MMC1_DAT6	MMC1 data bit 6	IOZ	F4
MMC1_DAT7	MMC1 data bit 7	IOZ	G5
MMC1_POW	MMC/SD cards on/off power supply control	OZ	K2
MMC1_SDCD	MMC1 card detect	I	J3
MMC1_SDWP	MMC1 write protect	I	K3

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(1) This clock signal is implemented as *pad loopback* inside the device — the output signal is looped back through the input buffer to serve as the internal reference signal. Series termination is required (as closeas possible to device pin) to improve signal integrity of the clock input.

For more information, see section *Multimedia Card High Speed Interface (MMCHS)* in chapter *Peripherals* of the Device TRM.

4.3.17 GPIO

Table 4-18. GPIO Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
GPIO0_00	General-purpose input/output	IOZ	AC21
GPIO0_01	General-purpose input/output	IOZ	AE20
GPIO0_02	General-purpose input/output	IOZ	AD22
GPIO0_03	General-purpose input/output	IOZ	AD20
GPIO0_04	General-purpose input/output	IOZ	AE21
GPIO0_05	General-purpose input/output	IOZ	AE22
GPIO0_06	General-purpose input/output	IOZ	AC20
GPIO0_07	General-purpose input/output	IOZ	AD21
GPIO0_08	General-purpose input/output	IOZ	AE23
GPIO0_09	General-purpose input/output	IOZ	AB20
GPIO0_10	General-purpose input/output	IOZ	AA20
GPIO0_11	General-purpose input/output	IOZ	AD23
GPIO0_12	General-purpose input/output	IOZ	AA21
GPIO0_13	General-purpose input/output	IOZ	AB21
GPIO0_14	General-purpose input/output	IOZ	AB22
GPIO0_15	General-purpose input/output	IOZ	AA22
GPIO0_16	General-purpose input/output	IOZ	AB23
GPIO0_17	General-purpose input/output	IOZ	AC23
GPIO0_18	General-purpose input/output	IOZ	AC22
GPIO0_19	General-purpose input/output	IOZ	Y22
GPIO0_100	General-purpose input/output	IOZ	N3
GPIO0_101	General-purpose input/output	IOZ	P3
GPIO0_102	General-purpose input/output	IOZ	P4
GPIO0_103	General-purpose input/output	IOZ	R2
GPIO0_104	General-purpose input/output	IOZ	R4
GPIO0_105	General-purpose input/output	IOZ	R3
GPIO0_106	General-purpose input/output	IOZ	T2
GPIO0_107	General-purpose input/output	IOZ	U1
GPIO0_108	General-purpose input/output	IOZ	D3
GPIO0_109	General-purpose input/output	IOZ	A2
GPIO0_110	General-purpose input/output	IOZ	E4
GPIO0_111	General-purpose input/output	IOZ	B1
GPIO0_112	General-purpose input/output	IOZ	A3
GPIO0_113	General-purpose input/output	IOZ	E5
GPIO0_114	General-purpose input/output	IOZ	B2
GPIO0_115	General-purpose input/output	IOZ	D4
GPIO0_116	General-purpose input/output	IOZ	E6
GPIO0_117	General-purpose input/output	IOZ	C2
GPIO0_118	General-purpose input/output	IOZ	C3

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Table 4-18. GPIO Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
GPIO0_119	General-purpose input/output	IOZ	D5
GPIO0_120	General-purpose input/output	IOZ	B3
GPIO0_121	General-purpose input/output	IOZ	B4
GPIO0_122	General-purpose input/output	IOZ	A4
GPIO0_123	General-purpose input/output	IOZ	E7
GPIO0_124	General-purpose input/output	IOZ	D6
GPIO0_125	General-purpose input/output	IOZ	C4
GPIO0_126	General-purpose input/output	IOZ	C5
GPIO0_127	General-purpose input/output	IOZ	A5
GPIO0_128	General-purpose input/output	IOZ	B5
GPIO0_129	General-purpose input/output	IOZ	B6
GPIO0_130	General-purpose input/output	IOZ	D7
GPIO0_131	General-purpose input/output	IOZ	A6
GPIO0_132	General-purpose input/output	IOZ	C6
GPIO0_133	General-purpose input/output	IOZ	E8
GPIO0_134	General-purpose input/output	IOZ	A7
GPIO0_135	General-purpose input/output	IOZ	D8
GPIO0_136	General-purpose input/output	IOZ	F9
GPIO0_137	General-purpose input/output	IOZ	B7
GPIO0_138	General-purpose input/output	IOZ	C7
GPIO0_139	General-purpose input/output	IOZ	E9
GPIO0_140	General-purpose input/output	IOZ	A8
GPIO0_141	General-purpose input/output	IOZ	B8
GPIO0_142	General-purpose input/output	IOZ	D9
GPIO0_143	General-purpose input/output	IOZ	C8
GPIO0_20	General-purpose input/output	IOZ	AC24
GPIO0_21	General-purpose input/output	IOZ	AB24
GPIO0_22	General-purpose input/output	IOZ	Y24
GPIO0_23	General-purpose input/output	IOZ	AA24
GPIO0_24	General-purpose input/output	IOZ	W25
GPIO0_25	General-purpose input/output	IOZ	AA25
GPIO0_26	General-purpose input/output	IOZ	AB25
GPIO0_27	General-purpose input/output	IOZ	W24
GPIO0_28	General-purpose input/output	IOZ	W23
GPIO0_29	General-purpose input/output	IOZ	Y25
GPIO0_30	General-purpose input/output	IOZ	N23
GPIO0_31	General-purpose input/output	IOZ	P25
GPIO0_32	General-purpose input/output	IOZ	P24
GPIO0_33	General-purpose input/output	IOZ	N24
GPIO0_34	General-purpose input/output	IOZ	T25
GPIO0_35	General-purpose input/output	IOZ	N22
GPIO0_36	General-purpose input/output	IOZ	R24
GPIO0_37	General-purpose input/output	IOZ	P23
GPIO0_38	General-purpose input/output	IOZ	R22
GPIO0_39	General-purpose input/output	IOZ	U25
GPIO0_40	General-purpose input/output	IOZ	P21
GPIO0_41	General-purpose input/output	IOZ	T24

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Table 4-18. GPIO Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
GPIO0_42	General-purpose input/output	IOZ	V25
GPIO0_43	General-purpose input/output	IOZ	U24
GPIO0_44	General-purpose input/output	IOZ	R21
GPIO0_45	General-purpose input/output	IOZ	T22
GPIO0_46	General-purpose input/output	IOZ	U22
GPIO0_47	General-purpose input/output	IOZ	T21
GPIO0_48	General-purpose input/output	IOZ	V24
GPIO0_49	General-purpose input/output	IOZ	U23
GPIO0_50	General-purpose input/output	IOZ	V23
GPIO0_51	General-purpose input/output	IOZ	W22
GPIO0_52	General-purpose input/output	IOZ	U21
GPIO0_53	General-purpose input/output	IOZ	V22
GPIO0_54	General-purpose input/output	IOZ	R25
GPIO0_55	General-purpose input/output	IOZ	P22
GPIO0_56	General-purpose input/output	IOZ	N25
GPIO0_57	General-purpose input/output	IOZ	M25
GPIO0_58	General-purpose input/output	IOZ	L25
GPIO0_59	General-purpose input/output	IOZ	G5
GPIO0_60	General-purpose input/output	IOZ	F4
GPIO0_61	General-purpose input/output	IOZ	G4
GPIO0_62	General-purpose input/output	IOZ	E3
GPIO0_63	General-purpose input/output	IOZ	H4
GPIO0_64	General-purpose input/output	IOZ	J5
GPIO0_65	General-purpose input/output	IOZ	F5
GPIO0_66	General-purpose input/output	IOZ	H3
GPIO0_67	General-purpose input/output	IOZ	J4
GPIO0_68	General-purpose input/output	IOZ	J2
GPIO0_69	General-purpose input/output	IOZ	J3
GPIO0_70	General-purpose input/output	IOZ	K3
GPIO0_71	General-purpose input/output	IOZ	K2
GPIO0_72	General-purpose input/output	IOZ	A22
GPIO0_73	General-purpose input/output	IOZ	A23
GPIO0_74	General-purpose input/output	IOZ	B22
GPIO0_75	General-purpose input/output	IOZ	C22
GPIO0_76	General-purpose input/output	IOZ	D23
GPIO0_77	General-purpose input/output	IOZ	F22
GPIO0_78	General-purpose input/output	IOZ	B23
GPIO0_79	General-purpose input/output	IOZ	C23
GPIO0_80	General-purpose input/output	IOZ	B24
GPIO0_81	General-purpose input/output	IOZ	A24
GPIO0_82	General-purpose input/output	IOZ	F23
GPIO0_83	General-purpose input/output	IOZ	B25
GPIO0_84	General-purpose input/output	IOZ	G22
GPIO0_85	General-purpose input/output	IOZ	C25
GPIO0_86	General-purpose input/output	IOZ	C24
GPIO0_87	General-purpose input/output	IOZ	E25
GPIO0_88	General-purpose input/output	IOZ	E24

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Table 4-18. GPIO Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
GPIO0_89	General-purpose input/output	IOZ	F25
GPIO0_90	General-purpose input/output	IOZ	F24
GPIO0_91	General-purpose input/output	IOZ	D25
GPIO0_92	General-purpose input/output	IOZ	G25
GPIO0_93	General-purpose input/output	IOZ	G24
GPIO0_94	General-purpose input/output	IOZ	G23
GPIO0_95	General-purpose input/output	IOZ	H25
GPIO0_96	General-purpose input/output	IOZ	H24
GPIO0_97	General-purpose input/output	IOZ	V3
GPIO0_98	General-purpose input/output	IOZ	U3
GPIO0_99	General-purpose input/output	IOZ	M4
GPIO1_00	General-purpose input/output	IOZ	C9
GPIO1_01	General-purpose input/output	IOZ	B9
GPIO1_02	General-purpose input/output	IOZ	A9
GPIO1_03	General-purpose input/output	IOZ	B10
GPIO1_04	General-purpose input/output	IOZ	A10
GPIO1_05	General-purpose input/output	IOZ	C10
GPIO1_06	General-purpose input/output	IOZ	E10
GPIO1_07	General-purpose input/output	IOZ	D10
GPIO1_08	General-purpose input/output	IOZ	F10
GPIO1_09	General-purpose input/output	IOZ	C11
GPIO1_10	General-purpose input/output	IOZ	D11
GPIO1_11	General-purpose input/output	IOZ	E11
GPIO1_12	General-purpose input/output	IOZ	F12
GPIO1_13	General-purpose input/output	IOZ	E12
GPIO1_14	General-purpose input/output	IOZ	C12
GPIO1_15	General-purpose input/output	IOZ	B11
GPIO1_16	General-purpose input/output	IOZ	B12
GPIO1_17	General-purpose input/output	IOZ	A12
GPIO1_18	General-purpose input/output	IOZ	A11
GPIO1_19	General-purpose input/output	IOZ	A13
GPIO1_20	General-purpose input/output	IOZ	B13
GPIO1_21	General-purpose input/output	IOZ	F13
GPIO1_22	General-purpose input/output	IOZ	C13
GPIO1_23	General-purpose input/output	IOZ	E13
GPIO1_24	General-purpose input/output	IOZ	D12
GPIO1_25	General-purpose input/output	IOZ	D13
GPIO1_26	General-purpose input/output	IOZ	A14
GPIO1_27	General-purpose input/output	IOZ	B14
GPIO1_28	General-purpose input/output	IOZ	C14
GPIO1_29	General-purpose input/output	IOZ	E14
GPIO1_30	General-purpose input/output	IOZ	D14
GPIO1_31	General-purpose input/output	IOZ	A15
GPIO1_32	General-purpose input/output	IOZ	F14
GPIO1_33	General-purpose input/output	IOZ	B15
GPIO1_34	General-purpose input/output	IOZ	C15
GPIO1_35	General-purpose input/output	IOZ	D15

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Table 4-18. GPIO Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
GPIO1_36	General-purpose input/output	IOZ	A16
GPIO1_37	General-purpose input/output	IOZ	E15
GPIO1_38	General-purpose input/output	IOZ	B16
GPIO1_39	General-purpose input/output	IOZ	C16
GPIO1_40	General-purpose input/output	IOZ	D17
GPIO1_41	General-purpose input/output	IOZ	C18
GPIO1_42	General-purpose input/output	IOZ	D16
GPIO1_43	General-purpose input/output	IOZ	F16
GPIO1_44	General-purpose input/output	IOZ	E17
GPIO1_45	General-purpose input/output	IOZ	E16
GPIO1_46	General-purpose input/output	IOZ	E18
GPIO1_47	General-purpose input/output	IOZ	D18
GPIO1_48	General-purpose input/output	IOZ	T3
GPIO1_49	General-purpose input/output	IOZ	T5
GPIO1_50	General-purpose input/output	IOZ	U2
GPIO1_51	General-purpose input/output	IOZ	U4
GPIO1_52	General-purpose input/output	IOZ	E21
GPIO1_53	General-purpose input/output	IOZ	D21
GPIO1_54	General-purpose input/output	IOZ	D22
GPIO1_55	General-purpose input/output	IOZ	C21
GPIO1_56	General-purpose input/output	IOZ	P5
GPIO1_57	General-purpose input/output	IOZ	R5
GPIO1_58	General-purpose input/output	IOZ	K25
GPIO1_59	General-purpose input/output	IOZ	K24
GPIO1_60	General-purpose input/output	IOZ	J23
GPIO1_61	General-purpose input/output	IOZ	J22
GPIO1_62	General-purpose input/output	IOZ	J21
GPIO1_63	General-purpose input/output	IOZ	J24
GPIO1_64	General-purpose input/output	IOZ	J25
GPIO1_65	General-purpose input/output	IOZ	H23
GPIO1_66	General-purpose input/output	IOZ	H22
GPIO1_67	General-purpose input/output	IOZ	H21

For more information, see section *General-Purpose Interface (GPIO)* in chapter *Peripherals* of the Device TRM.

4.3.18 ePWM

Table 4-19. ePWM Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
eCAP0_IN_APWM0_OUT	eCAP0 capture input and PWM output	IOZ	E18
eCAP1_IN_APWM1_OUT	eCAP1 capture input and PWM output	IOZ	D18
eHRPWM0_A	eHRPWM0 output A	IOZ	N23
eHRPWM0_B	eHRPWM0 output B	IOZ	P25
eHRPWM0_SYNCI	eHRPWM0 sync input	I	N24
eHRPWM0_SYNCO	eHRPWM0 sync output	OZ	T25
eHRPWM1_A	eHRPWM1 output A	IOZ	N22

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Table 4-19. ePWM Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
eHRPWM1_B	eHRPWM1 output B	IOZ	R24
eHRPWM2_A	eHRPWM2 output A	IOZ	R22
eHRPWM2_B	eHRPWM2 output B	IOZ	U25
eHRPWM3_A	eHRPWM3 output A	IOZ	A23
eHRPWM3_B	eHRPWM3 output B	IOZ	B22
eHRPWM3_SYNCI	eHRPWM3 sync input	I	C22
eHRPWM3_SYNCO	eHRPWM3 sync output	OZ	D23
eHRPWM4_A	eHRPWM4 output A	IOZ	D12
eHRPWM4_B	eHRPWM4 output B	IOZ	D13
eHRPWM5_A	eHRPWM5 output A	IOZ	E17
eHRPWM5_B	eHRPWM5 output B	IOZ	E16
eHRPWM_SOCA	ePWM ADC output A	OZ	E13
eHRPWM_SOCB	ePWM ADC output B	OZ	F16
eHRPWM_TZn0	eHRPWM0 trip zone input (Active Low)	I	P24
eHRPWM_TZn1	eHRPWM1 trip zone input (Active Low)	I	P23
eHRPWM_TZn2	eHRPWM2 trip zone input (Active Low)	I	P21
eHRPWM_TZn3	eHRPWM3 trip zone input (Active Low)	I	H24
eHRPWM_TZn4	eHRPWM4 trip zone input (Active Low)	I	E13
eHRPWM_TZn5	eHRPWM5 trip zone input (Active Low)	I	F16
eQEP0_A	eQEP0 quadrature input A	I	T24
eQEP0_B	eQEP0 quadrature input B	I	V25
eQEP0_I	eQEP0 index input / output	IOZ	U24
eQEP0_S	eQEP0 strobe input / output	IOZ	R21
eQEP1_A	eQEP1 quadrature input A	I	T22
eQEP1_B	eQEP1 quadrature input B	I	U22
eQEP1_I	eQEP1 index input / output	IOZ	T21
eQEP1_S	eQEP1 strobe input / output	IOZ	V24
eQEP2_A	eQEP2 quadrature input A	I	U23
eQEP2_B	eQEP2 quadrature input B	I	V23
eQEP2_I	eQEP2 index input / output	IOZ	W22
eQEP2_S	eQEP2 strobe input / output	IOZ	U21

For more information, see section *Enhanced PWM (ePWM) Module* in chapter *Peripherals* of the Device TRM.

4.3.19 PRU-ICSS

Table 4-20. PRU-ICSS Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
PR0_eCAP0_eCAP_CAPIN_APWM_O	Capture input and PWM output	IOZ	C24
PR0_eCAP0_eCAP_SYNCIN	Capture sync input	I	H24
PR0_eCAP0_eCAP_SYNCOUT	Capture sync output	OZ	D24
PR0_EDC_LATCH0_IN	Latch input 0	I	C5
PR0_EDC_LATCH1_IN	Latch input 1	I	A9
PR0_EDC_SYNC0_OUT	SYNC 0 output	OZ	A5
PR0_EDC_SYNC1_OUT	SYNC 1 output	OZ	B10
PR0_EDIO_DATA0	Digital input	IOZ	D23

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Table 4-20. PRU-ICSS Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
PR0_EDIO_DATA1	Digital input	IOZ	C22
PR0_EDIO_DATA2	Digital input	IOZ	B22
PR0_EDIO_DATA3	Digital input	IOZ	A23
PR0_EDIO_OUTVALID	Digital out valid signal	OZ	L25
PR0_MDIO_DATA	MDIO data	IOZ	A10
PR0_MDIO_MDCLK	MDIO clock	OZ	C10
PR0_PRU0_GPI0	PRU0 general-purpose input	I	D3
PR0_PRU0_GPI1	PRU0 general-purpose input	I	A2
PR0_PRU0_GPI2	PRU0 general-purpose input	I	E4
PR0_PRU0_GPI3	PRU0 general-purpose input	I	B1
PR0_PRU0_GPI4	PRU0 general-purpose input	I	A3
PR0_PRU0_GPI5	PRU0 general-purpose input	I	E5
PR0_PRU0_GPI6	PRU0 general-purpose input	I	B2
PR0_PRU0_GPI7	PRU0 general-purpose input	I	D4
PR0_PRU0_GPI8	PRU0 general-purpose input	I	E6
PR0_PRU0_GPI9	PRU0 general-purpose input	I	C2
PR0_PRU0_GPI10	PRU0 general-purpose input	I	C3
PR0_PRU0_GPI11	PRU0 general-purpose input	I	D5
PR0_PRU0_GPI12	PRU0 general-purpose input	I	B3
PR0_PRU0_GPI13	PRU0 general-purpose input	I	B4
PR0_PRU0_GPI14	PRU0 general-purpose input	I	A4
PR0_PRU0_GPI15	PRU0 general-purpose input	I	E7
PR0_PRU0_GPI16	PRU0 general-purpose input	I	D6
PR0_PRU0_GPI17	PRU0 general-purpose input	I	C4
PR0_PRU0_GPI18	PRU0 general-purpose input	I	C5
PR0_PRU0_GPI19	PRU0 general-purpose input	I	A5
PR0_PRU0_GPO0	PRU0 general-purpose output	OZ	D3
PR0_PRU0_GPO1	PRU0 general-purpose output	OZ	A2
PR0_PRU0_GPO2	PRU0 general-purpose output	OZ	E4
PR0_PRU0_GPO3	PRU0 general-purpose output	OZ	B1
PR0_PRU0_GPO4	PRU0 general-purpose output	OZ	A3
PR0_PRU0_GPO5	PRU0 general-purpose output	OZ	E5
PR0_PRU0_GPO6	PRU0 general-purpose output	OZ	B2
PR0_PRU0_GPO7	PRU0 general-purpose output	OZ	D4
PR0_PRU0_GPO8	PRU0 general-purpose output	OZ	E6
PR0_PRU0_GPO9	PRU0 general-purpose output	OZ	C2
PR0_PRU0_GPO10	PRU0 general-purpose output	OZ	C3
PR0_PRU0_GPO11	PRU0 general-purpose output	OZ	D5
PR0_PRU0_GPO12	PRU0 general-purpose output	OZ	B3
PR0_PRU0_GPO13	PRU0 general-purpose output	OZ	B4
PR0_PRU0_GPO14	PRU0 general-purpose output	OZ	A4
PR0_PRU0_GPO15	PRU0 general-purpose output	OZ	E7
PR0_PRU0_GPO16	PRU0 general-purpose output	OZ	D6
PR0_PRU0_GPO17	PRU0 general-purpose output	OZ	C4
PR0_PRU0_GPO18	PRU0 general-purpose output	OZ	C5
PR0_PRU0_GPO19	PRU0 general-purpose output	OZ	A5
PR0_PRU1_GPI0	PRU1 general-purpose input	I	B5

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Table 4-20. PRU-ICSS Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
PR0_PRU1_GPI1	PRU1 general-purpose input	I	B6
PR0_PRU1_GPI2	PRU1 general-purpose input	I	D7
PR0_PRU1_GPI3	PRU1 general-purpose input	I	A6
PR0_PRU1_GPI4	PRU1 general-purpose input	I	C6
PR0_PRU1_GPI5	PRU1 general-purpose input	I	E8
PR0_PRU1_GPI6	PRU1 general-purpose input	I	A7
PR0_PRU1_GPI7	PRU1 general-purpose input	I	D8
PR0_PRU1_GPI8	PRU1 general-purpose input	I	F9
PR0_PRU1_GPI9	PRU1 general-purpose input	I	B7
PR0_PRU1_GPI10	PRU1 general-purpose input	I	C7
PR0_PRU1_GPI11	PRU1 general-purpose input	I	E9
PR0_PRU1_GPI12	PRU1 general-purpose input	I	A8
PR0_PRU1_GPI13	PRU1 general-purpose input	I	B8
PR0_PRU1_GPI14	PRU1 general-purpose input	I	D9
PR0_PRU1_GPI15	PRU1 general-purpose input	I	C8
PR0_PRU1_GPI16	PRU1 general-purpose input	I	C9
PR0_PRU1_GPI17	PRU1 general-purpose input	I	B9
PR0_PRU1_GPI18	PRU1 general-purpose input	I	A9
PR0_PRU1_GPI19	PRU1 general-purpose input	I	B10
PR0_PRU1_GPO0	PRU1 general-purpose output	OZ	B5
PR0_PRU1_GPO1	PRU1 general-purpose output	OZ	B6
PR0_PRU1_GPO2	PRU1 general-purpose output	OZ	D7
PR0_PRU1_GPO3	PRU1 general-purpose output	OZ	A6
PR0_PRU1_GPO4	PRU1 general-purpose output	OZ	C6
PR0_PRU1_GPO5	PRU1 general-purpose output	OZ	E8
PR0_PRU1_GPO6	PRU1 general-purpose output	OZ	A7
PR0_PRU1_GPO7	PRU1 general-purpose output	OZ	D8
PR0_PRU1_GPO8	PRU1 general-purpose output	OZ	F9
PR0_PRU1_GPO9	PRU1 general-purpose output	OZ	B7
PR0_PRU1_GPO10	PRU1 general-purpose output	OZ	C7
PR0_PRU1_GPO11	PRU1 general-purpose output	OZ	E9
PR0_PRU1_GPO12	PRU1 general-purpose output	OZ	A8
PR0_PRU1_GPO13	PRU1 general-purpose output	OZ	B8
PR0_PRU1_GPO14	PRU1 general-purpose output	OZ	D9
PR0_PRU1_GPO15	PRU1 general-purpose output	OZ	C8
PR0_PRU1_GPO16	PRU1 general-purpose output	OZ	C9
PR0_PRU1_GPO17	PRU1 general-purpose output	OZ	B9
PR0_PRU1_GPO18	PRU1 general-purpose output	OZ	A9
PR0_PRU1_GPO19	PRU1 general-purpose output	OZ	B10
PR0_UART0_CTSN	UART clear-to-send	I	F25
PR0_UART0_RTSN	UART ready-to-send	OZ	F24
PR0_UART0_RXD	UART receive data	I	E25
PR0_UART0_TXD	UART transmit data	OZ	E24
PR1_eCAP0_eCAP_CAPIN_APWM_O	Capture input and PWM output	IOZ	R25
PR1_eCAP0_eCAP_SYNCIN	Capture sync input	I	P22
PR1_eCAP0_eCAP_SYNCOUT	Cpature sync output	OZ	N25
PR1_EDC_LATCH0_IN	Latch input 0	I	D12

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Table 4-20. PRU-ICSS Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
PR1_EDC_LATCH1_IN	Latch input 1	I	E17
PR1_EDC_SYNC0_OUT	SYNC 0 output	OZ	D13
PR1_EDC_SYNC1_OUT	SYNC 1 output	OZ	E16
PR1_EDIO_DATA0	Digital input	IOZ	C21
PR1_EDIO_DATA1	Digital input	IOZ	D22
PR1_EDIO_DATA2	Digital input	IOZ	D21
PR1_EDIO_DATA3	Digital input	IOZ	E21
PR1_EDIO_OUTVALID	Digital out valid signal	OZ	M25
PR1_MDIO_DATA	MDIO data	IOZ	E18
PR1_MDIO_MDCLK	MDIO clock	OZ	D18
PR1_PRU0_GPI0	PRU0 general-purpose input	I	E10
PR1_PRU0_GPI1	PRU0 general-purpose input	I	D10
PR1_PRU0_GPI2	PRU0 general-purpose input	I	F10
PR1_PRU0_GPI3	PRU0 general-purpose input	I	C11
PR1_PRU0_GPI4	PRU0 general-purpose input	I	D11
PR1_PRU0_GPI5	PRU0 general-purpose input	I	E11
PR1_PRU0_GPI6	PRU0 general-purpose input	I	F12
PR1_PRU0_GPI7	PRU0 general-purpose input	I	E12
PR1_PRU0_GPI8	PRU0 general-purpose input	I	C12
PR1_PRU0_GPI9	PRU0 general-purpose input	I	B11
PR1_PRU0_GPI10	PRU0 general-purpose input	I	B12
PR1_PRU0_GPI11	PRU0 general-purpose input	I	A12
PR1_PRU0_GPI12	PRU0 general-purpose input	I	A11
PR1_PRU0_GPI13	PRU0 general-purpose input	I	A13
PR1_PRU0_GPI14	PRU0 general-purpose input	I	B13
PR1_PRU0_GPI15	PRU0 general-purpose input	I	F13
PR1_PRU0_GPI16	PRU0 general-purpose input	I	C13
PR1_PRU0_GPI17	PRU0 general-purpose input	I	E13
PR1_PRU0_GPI18	PRU0 general-purpose input	I	D12
PR1_PRU0_GPI19	PRU0 general-purpose input	I	D13
PR1_PRU0_GPO0	PRU0 general-purpose output	OZ	E10
PR1_PRU0_GPO1	PRU0 general-purpose output	OZ	D10
PR1_PRU0_GPO2	PRU0 general-purpose output	OZ	F10
PR1_PRU0_GPO3	PRU0 general-purpose output	OZ	C11
PR1_PRU0_GPO4	PRU0 general-purpose output	OZ	D11
PR1_PRU0_GPO5	PRU0 general-purpose output	OZ	E11
PR1_PRU0_GPO6	PRU0 general-purpose output	OZ	F12
PR1_PRU0_GPO7	PRU0 general-purpose output	OZ	E12
PR1_PRU0_GPO8	PRU0 general-purpose output	OZ	C12
PR1_PRU0_GPO9	PRU0 general-purpose output	OZ	B11
PR1_PRU0_GPO10	PRU0 general-purpose output	OZ	B12
PR1_PRU0_GPO11	PRU0 general-purpose output	OZ	A12
PR1_PRU0_GPO12	PRU0 general-purpose output	OZ	A11
PR1_PRU0_GPO13	PRU0 general-purpose output	OZ	A13
PR1_PRU0_GPO14	PRU0 general-purpose output	OZ	B13
PR1_PRU0_GPO15	PRU0 general-purpose output	OZ	F13
PR1_PRU0_GPO16	PRU0 general-purpose output	OZ	C13

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Table 4-20. PRU-ICSS Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
PR1_PRU0_GPO17	PRU0 general-purpose output	OZ	E13
PR1_PRU0_GPO18	PRU0 general-purpose output	OZ	D12
PR1_PRU0_GPO19	PRU0 general-purpose output	OZ	D13
PR1_PRU1_GPI0	PRU1 general-purpose input	I	A14
PR1_PRU1_GPI1	PRU1 general-purpose input	I	B14
PR1_PRU1_GPI2	PRU1 general-purpose input	I	C14
PR1_PRU1_GPI3	PRU1 general-purpose input	I	E14
PR1_PRU1_GPI4	PRU1 general-purpose input	I	D14
PR1_PRU1_GPI5	PRU1 general-purpose input	I	A15
PR1_PRU1_GPI6	PRU1 general-purpose input	I	F14
PR1_PRU1_GPI7	PRU1 general-purpose input	I	B15
PR1_PRU1_GPI8	PRU1 general-purpose input	I	C15
PR1_PRU1_GPI9	PRU1 general-purpose input	I	D15
PR1_PRU1_GPI10	PRU1 general-purpose input	I	A16
PR1_PRU1_GPI11	PRU1 general-purpose input	I	E15
PR1_PRU1_GPI12	PRU1 general-purpose input	I	B16
PR1_PRU1_GPI13	PRU1 general-purpose input	I	C16
PR1_PRU1_GPI14	PRU1 general-purpose input	I	D17
PR1_PRU1_GPI15	PRU1 general-purpose input	I	C18
PR1_PRU1_GPI16	PRU1 general-purpose input	I	D16
PR1_PRU1_GPI17	PRU1 general-purpose input	I	F16
PR1_PRU1_GPI18	PRU1 general-purpose input	I	E17
PR1_PRU1_GPI19	PRU1 general-purpose input	I	E16
PR1_PRU1_GPO0	PRU1 general-purpose output	OZ	A14
PR1_PRU1_GPO1	PRU1 general-purpose output	OZ	B14
PR1_PRU1_GPO2	PRU1 general-purpose output	OZ	C14
PR1_PRU1_GPO3	PRU1 general-purpose output	OZ	E14
PR1_PRU1_GPO4	PRU1 general-purpose output	OZ	D14
PR1_PRU1_GPO5	PRU1 general-purpose output	OZ	A15
PR1_PRU1_GPO6	PRU1 general-purpose output	OZ	F14
PR1_PRU1_GPO7	PRU1 general-purpose output	OZ	B15
PR1_PRU1_GPO8	PRU1 general-purpose output	OZ	C15
PR1_PRU1_GPO9	PRU1 general-purpose output	OZ	D15
PR1_PRU1_GPO10	PRU1 general-purpose output	OZ	A16
PR1_PRU1_GPO11	PRU1 general-purpose output	OZ	E15
PR1_PRU1_GPO12	PRU1 general-purpose output	OZ	B16
PR1_PRU1_GPO13	PRU1 general-purpose output	OZ	C16
PR1_PRU1_GPO14	PRU1 general-purpose output	OZ	D17
PR1_PRU1_GPO15	PRU1 general-purpose output	OZ	C18
PR1_PRU1_GPO16	PRU1 general-purpose output	OZ	D16
PR1_PRU1_GPO17	PRU1 general-purpose output	OZ	F16
PR1_PRU1_GPO18	PRU1 general-purpose output	OZ	E17
PR1_PRU1_GPO19	PRU1 general-purpose output	OZ	E16
PR1_UART0_CTSN	UART clear-to-send	I	H22
PR1_UART0_RTSN	UART ready-to-send	OZ	H21
PR1_UART0_RXD	UART receive data	I	C4
PR1_UART0_TXD	UART transmit data	OZ	B9

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NOTE

PRU-ICSS has internal-multiplexing capability of pin functions. See *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)* in chapter *Processors and Accelerators* of the Device TRM. Besides, EGPIO (enhanced GPIO) module can be configured to export additional functions to EGPIO pins in place of simple GPIO. See section *PRU-ICSS PRU Cores* in chapter *Processors and Accelerators* of the Device TRM.

4.3.20 Emulation and Debug Subsystem

Table 4-21. Debug Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
EMU00	Emulator pin 0	IOZ	M22
EMU01	Emulator pin 1	IOZ	L22
EMU02	Emulator pin 2	IOZ	N23
EMU03	Emulator pin 3	IOZ	P25
EMU04	Emulator pin 4	IOZ	P24
EMU05	Emulator pin 5	IOZ	N24
EMU06	Emulator pin 6	IOZ	T25
EMU07	Emulator pin 7	IOZ	N22
EMU08	Emulator pin 8	IOZ	R24
EMU09	Emulator pin 9	IOZ	P23
EMU10	Emulator pin 10	IOZ	R22
EMU11	Emulator pin 11	IOZ	U25
EMU12	Emulator pin 12	IOZ	P21
EMU13	Emulator pin 13	IOZ	T24
EMU14	Emulator pin 14	IOZ	V25
EMU15	Emulator pin 15	IOZ	U24
EMU16	Emulator pin 16	IOZ	R21
EMU17	Emulator pin 17	IOZ	T22
EMU18	Emulator pin 18	IOZ	U22
EMU19	Emulator pin 19	IOZ	T21
TCK	JTAG test clock input	I	L3
TDI	JTAG test data input	I	L5
TDO	JTAG test port data output	OZ	K5
TMS	JTAG test port mode select input. An external pullup resistor must be used on this ball.	I	K4
TRSTn	JTAG test reset	I	L4

For more information, see chapter *On-chip Debug* of the Device TRM.

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4.3.21 System and Miscellaneous

4.3.21.1 Boot Mode Configuration

Table 4-22. Sysboot Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
BOOTCOMPLETE	Arm and DSP boot complete indicator	OZ	Y3
BOOTMODE00(1)	Bootmode pin 00	I	N23
BOOTMODE01(1)	Bootmode pin 01	I	P25
BOOTMODE02(1)	Bootmode pin 02	I	P24
BOOTMODE03(1)	Bootmode pin 03	I	N24
BOOTMODE04(1)	Bootmode pin 04	I	T25
BOOTMODE05(1)	Bootmode pin 05	I	N22
BOOTMODE06(1)	Bootmode pin 06	I	R24
BOOTMODE07(1)	Bootmode pin 07	I	P23
BOOTMODE08(1)	Bootmode pin 08	I	R22
BOOTMODE09(1)	Bootmode pin 09	I	U25
BOOTMODE10(1)	Bootmode pin 10	I	P21
BOOTMODE11(1)	Bootmode pin 11	I	T24
BOOTMODE12(1)	Bootmode pin 12	I	V25
BOOTMODE13(1)	Bootmode pin 13	I	U24
BOOTMODE14(1)	Bootmode pin 14	I	R21
BOOTMODE15(1)	Bootmode pin 15	I	T22
MAINPLL_OD_SEL(1)	Main PLL output divide	I	W22
BOOT_RSVD(1)	Reserved – This input shall always be pulled to a valid logic low level to insure the proper boot mode is selected	I	V23
NODDR(1)	Bootmode pin for no-DDR use case	I	U23

(1) Separate external pull resistors shall be connected to the balls associated with each of these signals to insure they are pulled to the appropriate and valid logic level required to select the desired boot mode on the rising edge of PORn. These inputs are synchronously latched after the rising edge of PORn using SYSOSC_IN or SYSCLK_P / N with setup and hold timing requirements defined in Table 5-15, *Boot Configuration Timing Requirements*.

For more information, see chapter *Initialization* of the Device TRM.

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4.3.21.2 Reset

Table 4-23. Reset Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
LRESETn	Local reset to DSP (Active Low)	I	V2
LRESETNMIENn	Enable for local reset to DSP and NMIn (Active Low)	I	V1
PORn	Power-on Reset (Active Low). This pin must be asserted low until all device supplies are valid (see Section 5.9.1, *Power Supply Sequencing*).	I	AA3
RESETFULLn	Cold reset (Active Low)	I	W2
RESETn	Device reset input (Active Low)	I	W3
RESETSTATn	Reset status indicator (Active Low)	O	Y2

For more information, see section *Reset Management* in chapter *Device Configuration* of the Device TRM.

4.3.21.3 Oscillator Reference Clocks and Clock Generator

Table 4-24. Clock Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
AUDOSC_IN(2)	Optional audio oscillator (AUDIOOSC) input. This input can be connected to the appropriate external crystal circuit or the oscillator can be bypassed by connecting this input to an LVCMOS clock source.	I	C17
AUDOSC_OUT	Optional audio oscillator (AUDIOOSC) output. This output is only used when AUDIOOSC is connected to the appropriate external crystal circuit.	O	A17
CLKOUT	RMII/MII reference clock output	OZ	H23
CPTS_REFCLK_N	Differential CPTS reference clock input, negative	I	L21
CPTS_REFCLK_P	Differential CPTS reference clock input, positive	I	K21
SYSCLKOUT(3)	SYSCLK divided by 6 observation output	OZ	M21
SYSCLK_N(4)	Differential system clock input, negative	I	AC25
SYSCLK_P(4)	Differential system clock input, positive	I	AD25
SYSOSC_IN(5)(6)	System oscillator (SYSOSC) input. This input can be connected to the appropriate external crystal circuit or the oscillator can be bypassed by connecting this input to an LVCMOS clock source.	I	AC19
SYSOSC_OUT	System oscillator (SYSOSC) output. This output is only used when SYSOSC is connected to the appropriate external crystal circuit.	O	AE19
XREFCLK	Optional audio reference clock input	I	C2
OBSCLK_N(1)	Observation clock output, negative	O	L1
OBSCLK_P(1)	Observation clock output, positive	O	K1
OBSPLL_LOCK(1)	Observation PLL lock output	OZ	N5

(1) These outputs are provided for test and debug purposes only. Performance of these outputs are not defined due to many complex combinations of system variables. For example, these outputs may be sourced from several PLLs with each PLL supporting many configuration options that yield various levels of performance. There are also other unpredictable contributors to performance such as application specific noise or crosstalk which may couple into the clock circuits. Therefore, there are no plans to specify performance for these outputs.

(2) When connecting AUDOSC_IN to an LVCMOS clock source, the LVCMOS clock source output must be disabled anytime AUDOSC is disabled since AUDOSC_IN has a strong internal pull-down resistor which is turned on when AUDIOOSC is disabled. This requires the LVCMOS clock source to be disabled by default and output enable controlled by a general purpose output since AUDIOOSC is disabled by default.

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(3) This output is provided for test and debug purposes only. Performance of this output is not defined due to many complex combinations of system variables. For example, this output is being sourced from the Main PLL supporting many configuration options that yield various levels of performance. There are also other unpredictable contributors to performance such as application specific noise or crosstalk which may couple into the clock circuits. Therefore, there are no plans to specify performance for this output.

(4) This input is used to source the internal system reference clock (SYS_OSCCLK) when the SYSCLKSEL input is driven high.

(5) When connecting SYSOSC_IN to an LVCMOS clock source, the LVCMOS clock source output must be disabled anytime SYSOSC is disabled since SYSOSC_IN has a strong internal pull-down resistor which is turned on when SYSOSC is disabled.

(6) This input is used to source the internal system reference clock (SYS_OSCCLK) when the SYSCLKSEL input is driven low.

4.3.21.4 Miscellaneous

Table 4-25. Miscellaneous Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
SYSCLKSEL(1)	System reference clock source selection input	I	R1

(1) This input is typically sourced by a pull resistor connected to VSS or DVDD33. If driven by any other source, this input must be driven to the appropriate logic level at least 500ns before the rising edge of PORn and held at the same logic level as long as the device is operational.

4.3.21.5 Interrupt Controllers (INTC)

Table 4-26. INTC Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
NMIn	Nonmaskable interrupt (Active Low)	I	W1

For more information, see chapter *Interrupts* of the Device TRM.

4.3.21.6 Power Supplies

Table 4-27. Power Supply Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
AVDDA_ARMPLL	ARM_PLL analog power supply	PWR	N6
AVDDA_DDRPLL	DDR_PLL analog power supply	PWR	W20
AVDDA_DSSPLL	DSS_PLL analog power supply	PWR	N20
AVDDA_ICSSPLL	ICSS_PLL analog power supply	PWR	G8
AVDDA_MAINPLL	MAIN_PLL analog power supply	PWR	M19
AVDDA_NSSPLL	NSS_PLL analog power supply	PWR	G14
AVDDA_UARTPLL	UART_PLL analog power supply	PWR	G10
CVDD	Core power supply	PWR	J10, J14, J16, K11, K13, K15, K17, K9, L10, L12, L14, L16, L18, M11, M13, M15, M17, M9, N10, N12, N14, N16, P11, P13, P15, P17, P9, R10, R12, R14, R16, R18, R8, T11, T15, T17, T9, U16
CVDD1	Core fixed power supply	PWR	M5, J12, N18, N8, T13
DVDD18	1.8-V I/Os power supply	PWR	F17, F19, G6, H5, J6, K19, L20, L6, M7, U18, U6, V19, W6

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Table 4-27. Power Supply Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ABY BALL [4]
DVDD33	3.3-V I/Os power supply	PWR	AA23, E23, F11, F15, F21, F7, G12, G16, G20, H11, H13, H15, H9, J20, P19, P7, R20, R6, T19, T23, T7, U20, V21
DVDD33_USB	USB 3.3-V supply	PWR	G18, H17
DVDD_DDR	DDR EMIF I/Os power supply	PWR	AD11, AD18, AD5, AE14, AE8, U10, U12, U14, U8, V11, V13, V15, V17, V7, W16, W18
DDR3_VREFSSTL	DDR EMIF reference power supply	PWR	Y9
DVDD_DDRDLL	DDR EMIF PHY DLL power supply	PWR	W10, W14, W8
LDO_PCIE_CAP(1)	SERDES LDO output	CAP	J8, L8
LDO_USB_CAP(1)	USB LDO output	CAP	H19, J18
VDDAHV	PCIe SERDES power supply	PWR	K7
VPP	Reserved, leave unconnected	PWR	Y21
VPP2(2)	Customer OTP eFuse array power supply	PWR	W21
VSS_OSC_AUDIO	AUDIOOSC Kelvin Ground	GND	B17
VSS_OSC_SYS	SYSOSC Kelvin Ground	GND	AD19
VSS	Ground	GND	A1, A25, AD14, AD8, AE1, AE11, AE18, AE25, AE5, C1, E2, E22, F1, F20, F3, F6, F8, G11, G13, G15, G17, G19, G21, G7, G9, H10, H12, H14, H16, H18, H20, H6, H8, J1, J11, J13, J15, J17, J19, J7, J9, K10, K12, K14, K16, K18, K20, K6, K8, L11, L13, L15, L17, L19, L7, L9, M10, M12, M14, M16, M18, M20, M6, M8, N11, N13, N15, N17, N19, N21, N7, N9, P10, P12, P14, P16, P18, P20, P6, P8, R11, R13, R15, R17, R19, R23, R7, R9, T10, T12, T14, T16, T18, T20, T6, T8, U11, U13, U15, U17, U19, U7, U9, V10, V12, V14, V16, V18, V20, V8, W11, W13, W15, W17, W7, W9, Y10, Y23

(1) This pin must always be connected through a 1-µF, ±50% decoupling capacitor with ESR of 10-100 mΩ to VSS with less than 0.5 nH of loop inductance.

(2) The VPP2 power supply pin is only valid for high-security (66AK2G1xS) devices. The VPP2 power source shall only be enabled while programming the customer OTP eFuse array and shall be disabled during power-up sequence, normal operation, and power-down sequence. When disabled, the power source shall not source current to, or sink current from the VPP2 terminal. This power supply pin is reserved for general purpose (66AK2G1x) devices and shall not be connected to any signal, test point, or printed circuit board trace when using 66AK2G1x devices.

For more information, see section *Power Management* in chapter *Device Configuration* of the Device TRM.

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4.4 Pin Multiplexing

Table 4-28 describes the signal multiplexing associated with pins.

NOTE

Many device pins support multiple signal functions. Some signal functions are selected via a single layer of multiplexers associated with pins. Other signal functions are selected via two or more layers of multiplexers, where one layer is associated with the pins and other layers are associated with peripheral logic functions.

Table 4-28, *Pin Multiplexing* only describes signal multiplexing at the pins. For more information, related to signal multiplexing at the pins, see section Pad Configuration Registers in section Control Module (BOOT_CFG) of chapter Device Configuration of the Device TRM. Refer to the respective peripheral chapter of the Device TRM for information associated with peripheral signal multiplexing.

NOTE

When a pad is set into a pin multiplexing mode which is not defined, that pad's behavior is undefined. This should be avoided.

NOTE

Any balls without an associated pin multiplexing register have a dedicated function that is defined in the MUXMODE "0" column of this table.

For more information on the I/O cell configurations, see section *Pad Configuration Registers* in section *Control Module (BOOT_CFG)* of chapter *Device Configuration* of the Device TRM.

Table 4-28. Pin Multiplexing

ADDRESS OFFSET	REGISTER NAME	BALL NUMBER	MUXMODE AND BOOTSTRAP SETTINGS						
			0	1	2	3	4	5	Bootstrap
		R1	SYSCLKSEL						
		Y15	DDR3_A01						
		AB4	DDR3_DQM0						
		L1	OBSCLK_N						
		Y6	DDR3_D10						
		AE15	DDR3_CLKOUT_P0						
		AA3	PORn						
		AA17	DDR3_A12						
		AE7	DDR3_D22						
		A19	USB0_ID						
		AB16	DDR3_A04						

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Table 4-28. Pin Multiplexing (continued)

ADDRESS OFFSET	REGISTER NAME	BALL NUMBER	MUXMODE AND BOOTSTRAP SETTINGS						
			0	1	2	3	4	5	Bootstrap
		C19	USB0_TXRTUNE_RKELVIN						
		AE9	DDR3_DQS3_P						
		W2	RESETFULLn						
		A21	USB1_VBUS						
		AE4	DDR3_DQS1_N						
		V9	DDR3_RZQ1						
		AD16	DDR3_CLKOUT_N1						
		AE19	SYSOSC_OUT						
		L24	MLBP_SIG_P						
		AC11	DDR3_CB02						
		K1	OBSCLK_P						
		L22	EMU01						
		A20	USB1_DM						
		AD1	DDR3_DQS0_P						
		AE3	DDR3_D04						
		H7	PCIE_REFRES						
		K22	MLBP_DAT_N						
		AA8	DDR3_D20						
		AC14	DDR3_A06						
		AB8	DDR3_D17						
		AC17	DDR3_A08						
		AC6	DDR3_D21						
		W3	RESETn						
		AD6	DDR3_DQS2_N						
		AA9	DDR3_DQM3						
		AB10	DDR3_D29						
		AA12	DDR3_A13						
		Y16	DDR3_A15						
		AA4	DDR3_D05						
		AA16	DDR3_A11						
		AA5	DDR3_DQM1						
		C17	AUDOSC_IN						
		AB15	DDR3_A07						
		D20	USB1_TXRTUNE_RKELVIN						
		Y5	DDR3_D13						
		F2	PCIE_CLK_N						
		L23	MLBP_CLK_N						

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Table 4-28. Pin Multiplexing (continued)

ADDRESS OFFSET	REGISTER NAME	BALL NUMBER	MUXMODE AND BOOTSTRAP SETTINGS						
			0	1	2	3	4	5	Bootstrap
		AD13	DDR3_CEn0						
		AB9	DDR3_D30						
		D19	USB0_XO						
		AC25	SYSCLK_N						
		AE16	DDR3_CLKOUT_P1						
		L21	CPTS_REFCLK_N						
		W12	DDR3_RZQ0						
		AE24	DDR_CLK_P						
		AB5	DDR3_D15						
		AC15	DDR3_A00						
		AE10	DDR3_D25						
		AA15	DDR3_A03						
		M24	MLBP_SIG_N						
		E1	PCIE_RXP0						
		AD17	DDR3_BA2						
		AC3	DDR3_D02						
		K5	TDO						
		AC7	DDR3_D18						
		AD9	DDR3_DQS3_N						
		Y8	DDR3_D31						
		L3	TCK						
		K23	MLBP_DAT_P						
		Y11	DDR3_CBDQM						
		AB14	DDR3_A10						
		Y13	DDR3_WEn						
		A18	USB0_DP						
		AD24	DDR_CLK_N						
		Y17	DDR3_A14						
		AC8	DDR3_DQM2						
		AC12	DDR3_CB03						
		AA6	DDR3_D08						
		AD7	DDR3_D23						
		B19	USB0_VBUS						
		AA11	DDR3_CB00						
		AC10	DDR3_D27						
		AE17	DDR3_A05						
		AE12	DDR3_CBDQS_P						
		AA14	DDR3_BA0						
		G2	PCIE_CLK_P						

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Table 4-28. Pin Multiplexing (continued)

ADDRESS OFFSET	REGISTER NAME	BALL NUMBER	MUXMODE AND BOOTSTRAP SETTINGS						
			0	1	2	3	4	5	Bootstrap
		AC4	DDR3_D14						
		Y9	DDR3_VREFSSTL						
		H1	PCIE_TXN0						
		AB18	DDR3_CKE0						
		AB6	DDR3_D12						
		E20	USB1_ID						
		L4	TRSTn						
		AC19	SYSOSC_IN						
		AD3	DDR3_D06						
		B20	USB1_DP						
		AE6	DDR3_DQS2_P						
		AB7	DDR3_D16						
		M22	EMU00						
		D1	PCIE_RXN0						
		M23	MLBP_CLK_P						
		AB3	DDR3_D07						
		AD2	DDR3_D00						
		A17	AUDOSC_OUT						
		B18	USB0_DM						
		AB13	DDR3_BA1						
		K4	TMS						
		AB17	DDR3_A09						
		Y7	DDR3_D09						
		AD15	DDR3_CLKOUT_N0						
		Y18	DDR3_RESETn						
		AC13	DDR3_CASn						
		AC2	DDR3_D03						
		G1	PCIE_TXP0						
		AD12	DDR3_CBDQS_N						
		AD10	DDR3_D26						
		AE13	DDR3_RASn						
		AE2	DDR3_DQS0_N						
		AA13	DDR3_ODT0						
		C20	USB1_XO						
		L5	TDI						
		AA10	DDR3_D24						
		K21	CPTS_REFCLK_P						
		AA7	DDR3_D19						
		AC5	DDR3_D11						

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Table 4-28. Pin Multiplexing (continued)

ADDRESS OFFSET	REGISTER NAME	BALL NUMBER	MUXMODE AND BOOTSTRAP SETTINGS						
			0	1	2	3	4	5	Bootstrap
		Y4	DDR3_D01						
		AC16	DDR3_A02						
		AB11	DDR3_CB01						
		AD25	SYSCLK_P						
		AC9	DDR3_D28						
		AD4	DDR3_DQS1_P						
		U5	I2C0_SCL						
		W5	I2C0_SDA						
		V6	I2C1_SCL						
		W4	I2C1_SDA						
		V5	I2C2_SCL						
		V4	I2C2_SDA						
0x1000	PADCONFIG_0	AC21	GPMC_AD0			GPIO0_00			
0x1004	PADCONFIG_1	AE20	GPMC_AD1			GPIO0_01			
0x1008	PADCONFIG_2	AD22	GPMC_AD2			GPIO0_02			
0x100C	PADCONFIG_3	AD20	GPMC_AD3			GPIO0_03			
0x1010	PADCONFIG_4	AE21	GPMC_AD4			GPIO0_04			
0x1014	PADCONFIG_5	AE22	GPMC_AD5			GPIO0_05			
0x1018	PADCONFIG_6	AC20	GPMC_AD6			GPIO0_06			
0x101C	PADCONFIG_7	AD21	GPMC_AD7			GPIO0_07			
0x1020	PADCONFIG_8	AE23	GPMC_AD8			GPIO0_08			
0x1024	PADCONFIG_9	AB20	GPMC_AD9			GPIO0_09			
0x1028	PADCONFIG_10	AA20	GPMC_AD10			GPIO0_10			
0x102C	PADCONFIG_11	AD23	GPMC_AD11			GPIO0_11			
0x1030	PADCONFIG_12	AA21	GPMC_AD12			GPIO0_12			
0x1034	PADCONFIG_13	AB21	GPMC_AD13			GPIO0_13			
0x1038	PADCONFIG_14	AB22	GPMC_AD14			GPIO0_14			
0x103C	PADCONFIG_15	AA22	GPMC_AD15			GPIO0_15			
0x1040	PADCONFIG_16	AB23	GPMC_CLK			GPIO0_16			
0x1044	PADCONFIG_17	AC23	GPMC_ADVn_ALE			GPIO0_17			
0x1048	PADCONFIG_18	AC22	GPMC_OEn_REn			GPIO0_18			
0x104C	PADCONFIG_19	Y22	GPMC_WEn			GPIO0_19			
0x1050	PADCONFIG_20	AC24	GPMC_BEn0_CLE			GPIO0_20			
0x1054	PADCONFIG_21	AB24	GPMC_BEn1			GPIO0_21			
0x1058	PADCONFIG_22	Y24	GPMC_WAIT0			GPIO0_22			
0x105C	PADCONFIG_23	AA24	GPMC_WAIT1		MLB_CLK	GPIO0_23			
0x1060	PADCONFIG_24	W25	GPMC_WPn			GPIO0_24			
0x1064	PADCONFIG_25	AA25	GPMC_DIR		MLB_SIG	GPIO0_25			
0x1068	PADCONFIG_26	AB25	GPMC_CSn0			GPIO0_26			

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Table 4-28. Pin Multiplexing (continued)

ADDRESS OFFSET	REGISTER NAME	BALL NUMBER	MUXMODE AND BOOTSTRAP SETTINGS						
			0	1	2	3	4	5	Bootstrap
0x106C	PADCONFIG_27	W24	GPMC_CSn1		MLB_DAT	GPIO0_27			
0x1070	PADCONFIG_28	W23	GPMC_CSn2		TIMI1	GPIO0_28			
0x1074	PADCONFIG_29	Y25	GPMC_CSn3		TIMO1	GPIO0_29			
0x1078	PADCONFIG_30	N23	DSS_DATA23	GPMC_A24	eHRPWM0_A	GPIO0_30	EMU02		BOOTMODE00
0x107C	PADCONFIG_31	P25	DSS_DATA22	GPMC_A23	eHRPWM0_B	GPIO0_31	EMU03		BOOTMODE01
0x1080	PADCONFIG_32	P24	DSS_DATA21	GPMC_A22	eHRPWM_TZn0	GPIO0_32	EMU04		BOOTMODE02
0x1084	PADCONFIG_33	N24	DSS_DATA20	GPMC_A21	eHRPWM0_SYNCI	GPIO0_33	EMU05		BOOTMODE03
0x1088	PADCONFIG_34	T25	DSS_DATA19	GPMC_A20	eHRPWM0_SYNCO	GPIO0_34	EMU06	DSS_RFBI_TEVSYNC1	BOOTMODE04
0x108C	PADCONFIG_35	N22	DSS_DATA18	GPMC_A19	eHRPWM1_A	GPIO0_35	EMU07	DSS_RFBI_HSYNC1	BOOTMODE05
0x1090	PADCONFIG_36	R24	DSS_DATA17	GPMC_A18	eHRPWM1_B	GPIO0_36	EMU08	DSS_RFBI_CSn1	BOOTMODE06
0x1094	PADCONFIG_37	P23	DSS_DATA16	GPMC_A17	eHRPWM_TZn1	GPIO0_37	EMU09	DSS_RFBI_CSn0	BOOTMODE07
0x1098	PADCONFIG_38	R22	DSS_DATA15	GPMC_A16	eHRPWM2_A	GPIO0_38	EMU10	DSS_RFBI_DATA15	BOOTMODE08
0x109C	PADCONFIG_39	U25	DSS_DATA14	GPMC_A15	eHRPWM2_B	GPIO0_39	EMU11	DSS_RFBI_DATA14	BOOTMODE09
0x10A0	PADCONFIG_40	P21	DSS_DATA13	GPMC_A14	eHRPWM_TZn2	GPIO0_40	EMU12	DSS_RFBI_DATA13	BOOTMODE10
0x10A4	PADCONFIG_41	T24	DSS_DATA12	GPMC_A13	eQEP0_A	GPIO0_41	EMU13	DSS_RFBI_DATA12	BOOTMODE11
0x10A8	PADCONFIG_42	V25	DSS_DATA11	GPMC_A12	eQEP0_B	GPIO0_42	EMU14	DSS_RFBI_DATA11	BOOTMODE12
0x10AC	PADCONFIG_43	U24	DSS_DATA10	GPMC_A11	eQEP0_I	GPIO0_43	EMU15	DSS_RFBI_DATA10	BOOTMODE13
0x10B0	PADCONFIG_44	R21	DSS_DATA9	GPMC_A10	eQEP0_S	GPIO0_44	EMU16	DSS_RFBI_DATA9	BOOTMODE14
0x10B4	PADCONFIG_45	T22	DSS_DATA8	GPMC_A9	eQEP1_A	GPIO0_45	EMU17	DSS_RFBI_DATA8	BOOTMODE15
0x10B8	PADCONFIG_46	U22	DSS_DATA7	GPMC_A8	eQEP1_B	GPIO0_46	EMU18	DSS_RFBI_DATA7	
0x10BC	PADCONFIG_47	T21	DSS_DATA6	GPMC_A7	eQEP1_I	GPIO0_47	EMU19	DSS_RFBI_DATA6	
0x10C0	PADCONFIG_48	V24	DSS_DATA5	GPMC_A6	eQEP1_S	GPIO0_48		DSS_RFBI_DATA5	
0x10C4	PADCONFIG_49	U23	DSS_DATA4	GPMC_A5	eQEP2_A	GPIO0_49		DSS_RFBI_DATA4	NODDR
0x10C8	PADCONFIG_50	V23	DSS_DATA3	GPMC_A4	eQEP2_B	GPIO0_50		DSS_RFBI_DATA3	BOOT_RSVD
0x10CC	PADCONFIG_51	W22	DSS_DATA2	GPMC_A3	eQEP2_I	GPIO0_51		DSS_RFBI_DATA2	MAINPLL_OD_SEL
0x10D0	PADCONFIG_52	U21	DSS_DATA1	GPMC_A2	eQEP2_S	GPIO0_52		DSS_RFBI_DATA1	
0x10D4	PADCONFIG_53	V22	DSS_DATA0	GPMC_A1		GPIO0_53		DSS_RFBI_DATA0	
0x10D8	PADCONFIG_54	R25	DSS_VSYNC	GPMC_A25	PR1_eCAP0_eCAP_CAPIN_APWM_O	GPIO0_54		DSS_RFBI_TEVSYNC0	
0x10DC	PADCONFIG_55	P22	DSS_HSYNC	GPMC_A26	PR1_eCAP0_eCAP_SYNCIN	GPIO0_55		DSS_RFBI_HSYNC0	
0x10E0	PADCONFIG_56	N25	DSS_PCLK	GPMC_A27	PR1_eCAP0_eCAP_SYNCOUT	GPIO0_56		DSS_RFBI_REn	
0x10E4	PADCONFIG_57	M25	DSS_DE	GPMC_A0	PR1_EDIO_OUTVALID	GPIO0_57		DSS_RFBI_WEn	
0x10E8	PADCONFIG_58	L25	DSS_FID		PR0_EDIO_OUTVALID	GPIO0_58		DSS_RFBI_A0	
0x10EC	PADCONFIG_59	G5	MMC1_DAT7			GPIO0_59			
0x10F0	PADCONFIG_60	F4	MMC1_DAT6			GPIO0_60			
0x10F4	PADCONFIG_61	G4	MMC1_DAT5			GPIO0_61			
0x10F8	PADCONFIG_62	E3	MMC1_DAT4			GPIO0_62			

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Table 4-28. Pin Multiplexing (continued)

ADDRESS OFFSET	REGISTER NAME	BALL NUMBER	MUXMODE AND BOOTSTRAP SETTINGS						
			0	1	2	3	4	5	Bootstrap
0x10FC	PADCONFIG_63	H4	MMC1_DAT3			GPIO0_63			
0x1100	PADCONFIG_64	J5	MMC1_DAT2			GPIO0_64			
0x1104	PADCONFIG_65	F5	MMC1_DAT1			GPIO0_65			
0x1108	PADCONFIG_66	H3	MMC1_DAT0			GPIO0_66			
0x110C	PADCONFIG_67	J4	MMC1_CLK			GPIO0_67			
0x1110	PADCONFIG_68	J2	MMC1_CMD			GPIO0_68			
0x1114	PADCONFIG_69	J3	MMC1_SDCD			GPIO0_69			
0x1118	PADCONFIG_70	K3	MMC1_SDWP			GPIO0_70			
0x111C	PADCONFIG_71	K2	MMC1_POW			GPIO0_71			
0x1120	PADCONFIG_72	A22	MII_RXCLK	RGMII_RXC		GPIO0_72			
0x1124	PADCONFIG_73	A23		PR0_EDIO_DATA3		GPIO0_73	eHRPWM3_A		
0x1128	PADCONFIG_74	B22		PR0_EDIO_DATA2		GPIO0_74	eHRPWM3_B		
0x112C	PADCONFIG_75	C22		PR0_EDIO_DATA1		GPIO0_75	eHRPWM3_SYNCI		
0x1130	PADCONFIG_76	D23		PR0_EDIO_DATA0		GPIO0_76	eHRPWM3_SYNCO		
0x1134	PADCONFIG_77	F22	MII_RXD3	RGMII_RXD3		GPIO0_77			
0x1138	PADCONFIG_78	B23	MII_RXD2	RGMII_RXD2		GPIO0_78			
0x113C	PADCONFIG_79	C23	MII_RXD1	RGMII_RXD1	RMII_RXD1	GPIO0_79			
0x1140	PADCONFIG_80	B24	MII_RXD0	RGMII_RXD0	RMII_RXD0	GPIO0_80			
0x1144	PADCONFIG_81	A24	MII_RXDV	RGMII_RXCTL		GPIO0_81			
0x1148	PADCONFIG_82	F23	MII_RXER		RMII_RXER	GPIO0_82			
0x114C	PADCONFIG_83	B25	MII_COL			GPIO0_83			
0x1150	PADCONFIG_84	G22	MII_CRS		RMII_CRS_DV	GPIO0_84			
0x1154	PADCONFIG_85	C25	MII_TXCLK	RGMII_TXC		GPIO0_85			
0x1158	PADCONFIG_86	C24		SPI3_SCSn0	PR0_eCAP0_eCAP_CAPIN_APWM_O	GPIO0_86			
0x115C	PADCONFIG_87	E25		SPI3_SCSn1	PR0_UART0_RXD	GPIO0_87			
0x1160	PADCONFIG_88	E24		SPI3_CLK	PR0_UART0_TXD	GPIO0_88			
0x1164	PADCONFIG_89	F25		SPI3_SOMI	PR0_UART0_CTSN	GPIO0_89			
0x1168	PADCONFIG_90	F24		SPI3_SIMO	PR0_UART0_RTSN	GPIO0_90			
0x116C	PADCONFIG_91	D25	MII_TXD3	RGMII_TXD3		GPIO0_91			
0x1170	PADCONFIG_92	G25	MII_TXD2	RGMII_TXD2		GPIO0_92			
0x1174	PADCONFIG_93	G24	MII_TXD1	RGMII_TXD1	RMII_TXD1	GPIO0_93			
0x1178	PADCONFIG_94	G23	MII_TXD0	RGMII_TXD0	RMII_TXD0	GPIO0_94			
0x117C	PADCONFIG_95	H25	MII_TXEN	RGMII_TXCTL	RMII_TXEN	GPIO0_95			
0x1180	PADCONFIG_96	H24	MII_TXER		PR0_eCAP0_eCAP_SYNCIN	GPIO0_96	eHRPWM_TZn3		
0x1184	PADCONFIG_97	D24	RMII_REFCLK		PR0_eCAP0_eCAP_SYNCOUT				
0x1188	PADCONFIG_98	V3	MDIO_DATA			GPIO0_97			
0x118C	PADCONFIG_99	U3	MDIO_CLK			GPIO0_98			

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Table 4-28. Pin Multiplexing (continued)

ADDRESS OFFSET	REGISTER NAME	BALL NUMBER	MUXMODE AND BOOTSTRAP SETTINGS						
			0	1	2	3	4	5	Bootstrap
0x1190	PADCONFIG_100	M3	SPI0_SCSn0						
0x1194	PADCONFIG_101	M4	SPI0_SCSn1			GPIO0_99			
0x1198	PADCONFIG_102	M2	SPI0_CLK						
0x119C	PADCONFIG_103	M1	SPI0_SOMI						
0x11A0	PADCONFIG_104	N4	SPI0_SIMO						
0x11A4	PADCONFIG_105	P1	SPI1_SCSn0						
0x11A8	PADCONFIG_106	N3	SPI1_SCSn1			GPIO0_100			
0x11AC	PADCONFIG_107	N2	SPI1_CLK						
0x11B0	PADCONFIG_108	N1	SPI1_SOMI						
0x11B4	PADCONFIG_109	P2	SPI1_SIMO						
0x11B8	PADCONFIG_110	P3	SPI2_SCSn0			GPIO0_101			
0x11BC	PADCONFIG_111	P4	SPI2_SCSn1			GPIO0_102			
0x11C0	PADCONFIG_112	R2	SPI2_CLK			GPIO0_103			
0x11C4	PADCONFIG_113	R4	SPI2_SOMI			GPIO0_104			
0x11C8	PADCONFIG_114	R3	SPI2_SIMO			GPIO0_105			
0x11CC	PADCONFIG_115	T4	UART0_RXD						
0x11D0	PADCONFIG_116	T1	UART0_TXD						
0x11D4	PADCONFIG_117	T2	UART0_CTSn	TIMI0		GPIO0_106			
0x11D8	PADCONFIG_118	U1	UART0_RTSn	TIMO0		GPIO0_107			
0x11DC	PADCONFIG_119	T3	UART1_RXD			GPIO1_48			
0x11E0	PADCONFIG_120	T5	UART1_TXD			GPIO1_49			
0x11E4	PADCONFIG_121	U2	UART1_CTSn			GPIO1_50			
0x11E8	PADCONFIG_122	U4	UART1_RTSn			GPIO1_51			
0x11EC	PADCONFIG_123	E21	UART2_RXD	PR1_EDIO_DATA3	UART0_DCDn	GPIO1_52	CPTS_HW1_TSPUSH		
0x11F0	PADCONFIG_124	D21	UART2_TXD	PR1_EDIO_DATA2	UART0_DSRn	GPIO1_53	CPTS_HW2_TSPUSH		
0x11F4	PADCONFIG_125	D22	UART2_CTSn	PR1_EDIO_DATA1	UART0_DTRn	GPIO1_54	CPTS_TS_SYNC		
0x11F8	PADCONFIG_126	C21	UART2_RTSn	PR1_EDIO_DATA0	UART0_RIN	GPIO1_55	CPTS_TS_COMP		
0x11FC	PADCONFIG_127	P5	DCAN0_TX			GPIO1_56			
0x1200	PADCONFIG_128	R5	DCAN0_RX			GPIO1_57			
0x1204	PADCONFIG_129	K25	QSPI_CLK			GPIO1_58			
0x1208	PADCONFIG_130	K24	QSPI_RCLK			GPIO1_59			
0x120C	PADCONFIG_131	J23	QSPI_D0			GPIO1_60			
0x1210	PADCONFIG_132	J22	QSPI_D1			GPIO1_61			
0x1214	PADCONFIG_133	J21	QSPI_D2			GPIO1_62			
0x1218	PADCONFIG_134	J24	QSPI_D3			GPIO1_63			
0x121C	PADCONFIG_135	J25	QSPI_CSn0			GPIO1_64			
0x1220	PADCONFIG_136	H23	QSPI_CSn1	CLKOUT		GPIO1_65			
0x1224	PADCONFIG_137	H22	QSPI_CSn2	DCAN1_TX	PR1_UART0_CTSN	GPIO1_66	USB0_EXT_TRIGGER		
0x1228	PADCONFIG_138	H21	QSPI_CSn3	DCAN1_RX	PR1_UART0_RTSN	GPIO1_67	USB1_EXT_TRIGGER		

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Table 4-28. Pin Multiplexing (continued)

ADDRESS OFFSET	REGISTER NAME	BALL NUMBER	MUXMODE AND BOOTSTRAP SETTINGS						
			0	1	2	3	4	5	Bootstrap
0x122C	PADCONFIG_139	D3	PR0_PRU0_GPO0	PR0_PRU0_GPI0		GPIO0_108	MCASP2_AXR0		
0x1230	PADCONFIG_140	A2	PR0_PRU0_GPO1	PR0_PRU0_GPI1		GPIO0_109	MCASP2_AXR1		
0x1234	PADCONFIG_141	E4	PR0_PRU0_GPO2	PR0_PRU0_GPI2		GPIO0_110	MCASP2_AXR2		
0x1238	PADCONFIG_142	B1	PR0_PRU0_GPO3	PR0_PRU0_GPI3		GPIO0_111	MCASP2_AXR3		
0x123C	PADCONFIG_143	A3	PR0_PRU0_GPO4	PR0_PRU0_GPI4		GPIO0_112	MCASP2_AXR4		
0x1240	PADCONFIG_144	E5	PR0_PRU0_GPO5	PR0_PRU0_GPI5		GPIO0_113	MCASP2_AXR5		
0x1244	PADCONFIG_145	B2	PR0_PRU0_GPO6	PR0_PRU0_GPI6		GPIO0_114	MCASP2_ACLKR		
0x1248	PADCONFIG_146	D4	PR0_PRU0_GPO7	PR0_PRU0_GPI7		GPIO0_115	MCASP2_AFSR		
0x124C	PADCONFIG_147	E6	PR0_PRU0_GPO8	PR0_PRU0_GPI8		GPIO0_116	MCASP2_AHCLKR		
0x1250	PADCONFIG_148	C2	PR0_PRU0_GPO9	PR0_PRU0_GPI9	XREFCLK	GPIO0_117	MCASP2_AMUTE		
0x1254	PADCONFIG_149	C3	PR0_PRU0_GPO10	PR0_PRU0_GPI10		GPIO0_118	MCASP2_AFSX		
0x1258	PADCONFIG_150	D5	PR0_PRU0_GPO11	PR0_PRU0_GPI11		GPIO0_119	MCASP2_AHCLKX		
0x125C	PADCONFIG_151	B3	PR0_PRU0_GPO12	PR0_PRU0_GPI12		GPIO0_120	MCASP2_ACLKX		
0x1260	PADCONFIG_152	B4	PR0_PRU0_GPO13	PR0_PRU0_GPI13		GPIO0_121	MCASP1_ACLKR		
0x1264	PADCONFIG_153	A4	PR0_PRU0_GPO14	PR0_PRU0_GPI14		GPIO0_122	MCASP1_AFSR		
0x1268	PADCONFIG_154	E7	PR0_PRU0_GPO15	PR0_PRU0_GPI15		GPIO0_123	MCASP1_AHCLKR		
0x126C	PADCONFIG_155	D6	PR0_PRU0_GPO16	PR0_PRU0_GPI16		GPIO0_124	MCASP1_ACLKX		
0x1270	PADCONFIG_156	C4	PR0_PRU0_GPO17	PR0_PRU0_GPI17	PR1_UART0_RXD	GPIO0_125	MCASP1_AFSX		
0x1274	PADCONFIG_157	C5	PR0_PRU0_GPO18	PR0_PRU0_GPI18	PR0_EDC_LATCH0_IN	GPIO0_126	MCASP1_AHCLKX		
0x1278	PADCONFIG_158	A5	PR0_PRU0_GPO19	PR0_PRU0_GPI19	PR0_EDC_SYNC0_OUT	GPIO0_127	MCASP1_AMUTE		
0x127C	PADCONFIG_159	B5	PR0_PRU1_GPO0	PR0_PRU1_GPI0		GPIO0_128	MCASP1_AXR0		
0x1280	PADCONFIG_160	B6	PR0_PRU1_GPO1	PR0_PRU1_GPI1		GPIO0_129	MCASP1_AXR1		
0x1284	PADCONFIG_161	D7	PR0_PRU1_GPO2	PR0_PRU1_GPI2		GPIO0_130	MCASP1_AXR2		
0x1288	PADCONFIG_162	A6	PR0_PRU1_GPO3	PR0_PRU1_GPI3		GPIO0_131	MCASP1_AXR3		
0x128C	PADCONFIG_163	C6	PR0_PRU1_GPO4	PR0_PRU1_GPI4		GPIO0_132	MCASP1_AXR4		
0x1290	PADCONFIG_164	E8	PR0_PRU1_GPO5	PR0_PRU1_GPI5		GPIO0_133	MCASP1_AXR5		
0x1294	PADCONFIG_165	A7	PR0_PRU1_GPO6	PR0_PRU1_GPI6		GPIO0_134	MCASP1_AXR6		
0x1298	PADCONFIG_166	D8	PR0_PRU1_GPO7	PR0_PRU1_GPI7		GPIO0_135	MCASP1_AXR7		
0x129C	PADCONFIG_167	F9	PR0_PRU1_GPO8	PR0_PRU1_GPI8		GPIO0_136	MCASP1_AXR8		
0x12A0	PADCONFIG_168	B7	PR0_PRU1_GPO9	PR0_PRU1_GPI9		GPIO0_137	MCASP1_AXR9		
0x12A4	PADCONFIG_169	C7	PR0_PRU1_GPO10	PR0_PRU1_GPI10		GPIO0_138	MCASP0_AMUTE		
0x12A8	PADCONFIG_170	E9	PR0_PRU1_GPO11	PR0_PRU1_GPI11		GPIO0_139	MCASP0_ACLKR		
0x12AC	PADCONFIG_171	A8	PR0_PRU1_GPO12	PR0_PRU1_GPI12		GPIO0_140	MCASP0_AFSR		
0x12B0	PADCONFIG_172	B8	PR0_PRU1_GPO13	PR0_PRU1_GPI13		GPIO0_141	MCASP0_AHCLKR		
0x12B4	PADCONFIG_173	D9	PR0_PRU1_GPO14	PR0_PRU1_GPI14		GPIO0_142	MCASP0_ACLKX		
0x12B8	PADCONFIG_174	C8	PR0_PRU1_GPO15	PR0_PRU1_GPI15		GPIO0_143	MCASP0_AFSX		
0x12BC	PADCONFIG_175	C9	PR0_PRU1_GPO16	PR0_PRU1_GPI16		GPIO1_00	MCASP0_AHCLKX		
0x12C0	PADCONFIG_176	B9	PR0_PRU1_GPO17	PR0_PRU1_GPI17	PR1_UART0_TXD	GPIO1_01	MCASP0_AXR0		

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Table 4-28. Pin Multiplexing (continued)

ADDRESS OFFSET	REGISTER NAME	BALL NUMBER	MUXMODE AND BOOTSTRAP SETTINGS						
			0	1	2	3	4	5	Bootstrap
0x12C4	PADCONFIG_177	A9	PR0_PRU1_GPO18	PR0_PRU1_GPI18	PR0_EDC_LATCH1_IN	GPIO1_02	MCASP0_AXR1		
0x12C8	PADCONFIG_178	B10	PR0_PRU1_GPO19	PR0_PRU1_GPI19	PR0_EDC_SYNC1_OUT	GPIO1_03	MCASP0_AXR2		
0x12CC	PADCONFIG_179	A10	PR0_MDIO_DATA			GPIO1_04	MCASP0_AXR3		
0x12D0	PADCONFIG_180	C10	PR0_MDIO_MDCLK			GPIO1_05	MCASP0_AXR4		
0x12D4	PADCONFIG_181	E10	PR1_PRU0_GPO0	PR1_PRU0_GPI0		GPIO1_06	MCASP0_AXR5		
0x12D8	PADCONFIG_182	D10	PR1_PRU0_GPO1	PR1_PRU0_GPI1		GPIO1_07	MCASP0_AXR6		
0x12DC	PADCONFIG_183	F10	PR1_PRU0_GPO2	PR1_PRU0_GPI2		GPIO1_08	MCASP0_AXR7		
0x12E0	PADCONFIG_184	C11	PR1_PRU0_GPO3	PR1_PRU0_GPI3		GPIO1_09	MCASP0_AXR8		
0x12E4	PADCONFIG_185	D11	PR1_PRU0_GPO4	PR1_PRU0_GPI4	MMC0_POW	GPIO1_10	MCASP0_AXR9		
0x12E8	PADCONFIG_186	E11	PR1_PRU0_GPO5	PR1_PRU0_GPI5	MMC0_SDWP	GPIO1_11	MCASP0_AXR10		
0x12EC	PADCONFIG_187	F12	PR1_PRU0_GPO6	PR1_PRU0_GPI6	MMC0_SDCD	GPIO1_12	MCASP0_AXR11		
0x12F0	PADCONFIG_188	E12	PR1_PRU0_GPO7	PR1_PRU0_GPI7	MMC0_DAT7	GPIO1_13	MCASP0_AXR12		
0x12F4	PADCONFIG_189	C12	PR1_PRU0_GPO8	PR1_PRU0_GPI8	MMC0_DAT6	GPIO1_14	MCASP0_AXR13		
0x12F8	PADCONFIG_190	B11	PR1_PRU0_GPO9	PR1_PRU0_GPI9	MMC0_DAT5	GPIO1_15	MCASP0_AXR14		
0x12FC	PADCONFIG_191	B12	PR1_PRU0_GPO10	PR1_PRU0_GPI10	MMC0_DAT4	GPIO1_16	MCASP0_AXR15		
0x1300	PADCONFIG_192	A12	PR1_PRU0_GPO11	PR1_PRU0_GPI11	MMC0_DAT3	GPIO1_17			
0x1304	PADCONFIG_193	A11	PR1_PRU0_GPO12	PR1_PRU0_GPI12	MMC0_DAT2	GPIO1_18			
0x1308	PADCONFIG_194	A13	PR1_PRU0_GPO13	PR1_PRU0_GPI13	MMC0_DAT1	GPIO1_19			
0x130C	PADCONFIG_195	B13	PR1_PRU0_GPO14	PR1_PRU0_GPI14	MMC0_DAT0	GPIO1_20			
0x1310	PADCONFIG_196	F13	PR1_PRU0_GPO15	PR1_PRU0_GPI15	MMC0_CLK	GPIO1_21			
0x1314	PADCONFIG_197	C13	PR1_PRU0_GPO16	PR1_PRU0_GPI16	MMC0_CMD	GPIO1_22			
0x1318	PADCONFIG_198	E13	PR1_PRU0_GPO17	PR1_PRU0_GPI17		GPIO1_23	eHRPWM_TZn4	eHRPWM_SOCA	
0x131C	PADCONFIG_199	D12	PR1_PRU0_GPO18	PR1_PRU0_GPI18	PR1_EDC_LATCH0_IN	GPIO1_24	eHRPWM4_A		
0x1320	PADCONFIG_200	D13	PR1_PRU0_GPO19	PR1_PRU0_GPI19	PR1_EDC_SYNC0_OUT	GPIO1_25	eHRPWM4_B		
0x1324	PADCONFIG_201	A14	PR1_PRU1_GPO0	PR1_PRU1_GPI0		GPIO1_26			
0x1328	PADCONFIG_202	B14	PR1_PRU1_GPO1	PR1_PRU1_GPI1		GPIO1_27			
0x132C	PADCONFIG_203	C14	PR1_PRU1_GPO2	PR1_PRU1_GPI2		GPIO1_28			
0x1330	PADCONFIG_204	E14	PR1_PRU1_GPO3	PR1_PRU1_GPI3		GPIO1_29			
0x1334	PADCONFIG_205	D14	PR1_PRU1_GPO4	PR1_PRU1_GPI4		GPIO1_30			
0x1338	PADCONFIG_206	A15	PR1_PRU1_GPO5	PR1_PRU1_GPI5		GPIO1_31			
0x133C	PADCONFIG_207	F14	PR1_PRU1_GPO6	PR1_PRU1_GPI6		GPIO1_32			
0x1340	PADCONFIG_208	B15	PR1_PRU1_GPO7	PR1_PRU1_GPI7		GPIO1_33			
0x1344	PADCONFIG_209	C15	PR1_PRU1_GPO8	PR1_PRU1_GPI8		GPIO1_34			
0x1348	PADCONFIG_210	D15	PR1_PRU1_GPO9	PR1_PRU1_GPI9	MCBSP_DR	GPIO1_35			
0x134C	PADCONFIG_211	A16	PR1_PRU1_GPO10	PR1_PRU1_GPI10	MCBSP_DX	GPIO1_36			
0x1350	PADCONFIG_212	E15	PR1_PRU1_GPO11	PR1_PRU1_GPI11	MCBSP_FSX	GPIO1_37			
0x1354	PADCONFIG_213	B16	PR1_PRU1_GPO12	PR1_PRU1_GPI12	MCBSP_CLKX	GPIO1_38			

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Table 4-28. Pin Multiplexing (continued)

ADDRESS OFFSET	REGISTER NAME	BALL NUMBER	MUXMODE AND BOOTSTRAP SETTINGS						
			0	1	2	3	4	5	Bootstrap
0x1358	PADCONFIG_214	C16	PR1_PRU1_GPO13	PR1_PRU1_GPI13	MCBSP_FSR	GPIO1_39			
0x135C	PADCONFIG_215	D17	PR1_PRU1_GPO14	PR1_PRU1_GPI14	MCBSP_CLKR	GPIO1_40			
0x1360	PADCONFIG_216	C18	PR1_PRU1_GPO15	PR1_PRU1_GPI15		GPIO1_41			
0x1364	PADCONFIG_217	D16	PR1_PRU1_GPO16	PR1_PRU1_GPI16		GPIO1_42			
0x1368	PADCONFIG_218	F16	PR1_PRU1_GPO17	PR1_PRU1_GPI17		GPIO1_43	eHRPWM_TZn5	eHRPWM_SOCB	
0x136C	PADCONFIG_219	E17	PR1_PRU1_GPO18	PR1_PRU1_GPI18	PR1_EDC_LATCH1_IN	GPIO1_44	eHRPWM5_A		
0x1370	PADCONFIG_220	E16	PR1_PRU1_GPO19	PR1_PRU1_GPI19	PR1_EDC_SYNC1_OUT	GPIO1_45	eHRPWM5_B		
0x1374	PADCONFIG_221	E18	PR1_MDIO_DATA			GPIO1_46	eCAP0_IN_APWM0_OUT		
0x1378	PADCONFIG_222	D18	PR1_MDIO_MDCLK			GPIO1_47	eCAP1_IN_APWM1_OUT		
0x1394	PADCONFIG_229	W1	NMIn						
0x1398	PADCONFIG_230	V2	LRESETn						
0x139C	PADCONFIG_231	V1	LRESETNMIENn						
0x13AC	PADCONFIG_235	Y2	RESETSTATn						
0x13B0	PADCONFIG_236	Y3	BOOTCOMPLETE						
0x13B4	PADCONFIG_237	M21	SYSCLKOUT						
0x13B8	PADCONFIG_238	N5	OBSPLL_LOCK						
0x1408	PADCONFIG_258	E19	USB0_DRVVBUS						
0x140C	PADCONFIG_259	B21	USB1_DRVVBUS						

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4.5 Connections for Unused Pins

This section describes the unused/reserved balls connection requirements.

NOTE

All power balls must be supplied with the voltages specified in Section 5.4, *Recommended Operating Conditions*.

Table 4-29. Unused Balls Specific Connection Requirements(2)

Balls	Connection Requirements
L4 / AD1 / AD4 / AE6 / AE9 / AE12 / M2 / N4 / M1 / N2 / P2 / N1 / T1 / D24 / L23	Each of these balls must be connected to VSS through a separate external pull resistor to insure these balls are held to a valid logic low level if unused
L3 / W1 / W3 / K4 / AE2 / AE4 / AD6 / AD9 / AD12 / U5 / W5 / V6 / W4 / V5 / V4 / M23 / M3 / P1 / T4 / L5 / W2 / M22 / L22	Each of these balls must be connected to the corresponding power supply through a separate external pull resistor to insure these balls are held to a valid logic high level if unused(1)

(1) To determine which power supply is associated with any IO refer to Table 4-1, *Pin Attributes*.

(2) Unused connection requirements for oscillator and LVDS clock inputs are defined in the respective section of Clock Specifications.

NOTE

The following balls are reserved: AA19 (RSV1) / AB19 (RSV2) / Y20 (RSV3) / W19 (RSV4) / D2 (RSV5) / G3 (RSV7) / F18 (RSV8) / H2 (RSV9) / AA18 (RSV10) / Y19 (RSV11) / Y14 (RSV12) / AC18 (RSV19) / AB12 (RSV20) / Y12 (RSV21)

These balls must be left unconnected.

NOTE

The following ball is reserved: L2 (RSV6)

This ball must be connected to VSS through a separate external pull resistor to insure it is held to a valid logic low level.

NOTE

The following balls are reserved: Y1 (RSV13) / AA1 (RSV14) / AB1 (RSV15) / AA2 (RSV16) / AB2 (RSV17) / AC1 (RSV18)

Each of these balls must be connected to DVDD18 through a separate external pull resistor to insure they are held to a valid logic high level.

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NOTE

All other unused signal balls **with** a Pad Configuration Register can be left unconnected with their multiplexing mode set to GPIO input and internal pulldown resistor enabled.

Unused balls are defined as those which only connect to a PCB solder pad. This is the only use case where internal pull resistors are allowed as the only source/sink to hold a valid logic level.

Any balls connected to a via, test point, or PCB trace are considered used and must not depend on the internal pull resistor to hold a valid logic level.

Internal pull resistors are weak and may not source enough current to maintain a valid logic level for some operating conditions. This may be the case when connected to components with leakage to the opposite logic level, or when external noise sources couple to signal traces attached to balls which are only pulled to a valid logic level by the internal resistor. Therefore, external pull resistors may be required to hold a valid logic level on balls with external connections.

If balls are allowed to float between valid logic levels, the input buffer may enter a high-current state which could damage the IO cell.

NOTE

All other unused signal balls **without** Pad Configuration Register can be left unconnected.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)[1][2]

PARAMETERS			MIN	MAX	UNIT
V_{SUPPLY} (steady-state)	Supply steady state voltage ranges	CVDD	-0.3	1.3	V
		CVDD1	-0.3	1.3	V
		VPP2[5]	-0.3	1.98	V
		AVDDA_DDRPLL	-0.3	1.98	V
		AVDDA_DSSPLL	-0.3	1.98	V
		AVDDA_MAINPLL	-0.3	1.98	V
		AVDDA_NSSPLL	-0.3	1.98	V
		AVDDA_UARTPLL	-0.3	1.98	V
		AVDDA_ICSSPLL	-0.3	1.98	V
		AVDDA_ARMPLL	-0.3	1.98	V
		DVDD_DDR	-0.3	1.98	V
		DVDD_DDRDLL	-0.3	2.45	V
		VDDAHV	-0.3	2.45	V
		DVDD18	-0.3	2.45	V
		DVDD33	-0.3	3.63	V
		DVDD33_USB	-0.3	3.63	V
V_{IO} (steady-state)	Non-fail-safe IO steady-state voltage ranges[3][6]	All IOs which are not fail-safe	-0.3	IO supply voltage + 0.3	V
		DDR3_VREFSSTL	0.49 × DVDD_DDR	0.51 × DVDD_DDR	V
	Fail-safe IO steady-state voltage ranges[7]	USB0_VBUS	0	5.25	V
		USB1_VBUS	0	5.25	V
SR	Maximum slew rate	All supplies except VPP2		1×10^5	V/s
		VPP2		0.6×10^5	V/s
V_{IO} (transient overshoot and undershoot)	IO transient voltage ranges (transient overshoot and undershoot)[4]	I2C IOs[8]	10% overshoot / undershoot for 10% of signal duty cycle (see Figure 5-1)		V
		All other IOs	20% overshoot / undershoot for 20% of signal duty cycle (see Figure 5-2)		V
T_{STG}	Storage temperature after soldered onto PC board		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 5.4, *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to V_{SS}, unless otherwise noted.

(3) Refer to Table 4-1, *Pin Attributes* to determine which power supply is associated with an IO.

(4) Overshoot/Undershoot percentage relative to IO operating values - for example the maximum overshoot value for a standard LVCMOS IO operating at 1.8 V is DVDD18 + (0.20 × DVDD18) and maximum undershoot value would be VSS - (0.20 × DVDD18).

(5) The VPP2 power supply pin is only valid for high-security (66AK2G1xS) devices. The VPP2 power source shall only be enabled while programming the customer OTP eFuse array and shall be disabled during power-up sequence, normal operation, and power-down sequence. When disabled, the power source shall not source current to, or sink current from the VPP2 terminal. This power supply pin is reserved for general purpose (66AK2G1x) devices and shall not be connected to any signal, test point, or printed circuit board trace when using 66AK2G1x devices.

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(6) This parameter applies to all IO terminals which are not fail-safe and the requirement applies to all values of IO supply voltage. For example, if the voltage applied to a specific IO supply is 0 volts the valid input voltage range for any IO powered by that supply will be –0.3 V to +0.3 V. Apply special attention anytime peripheral devices are not powered from the same power sources used to power the respective IO supply. It is important the attached peripheral never sources a voltage outside the valid input voltage range, including power supply ramp-up and ramp-down sequences.

(7) This parameter is associated with a fail-safe IO and does not have a dependence on any IO supply voltage.

(8) Designing a system that is able to meet the I2C overshoot/undershoot limit defined by this parameter should not be an issue since the I2C specification defines a minimum rise/fall time which minimizes overshoots and undershoots. However, special design precautions may need to be taken if the I2C IOs are connected to other devices which are not compliant to the minimum rise/fall time parameters defined in the I2C specification.

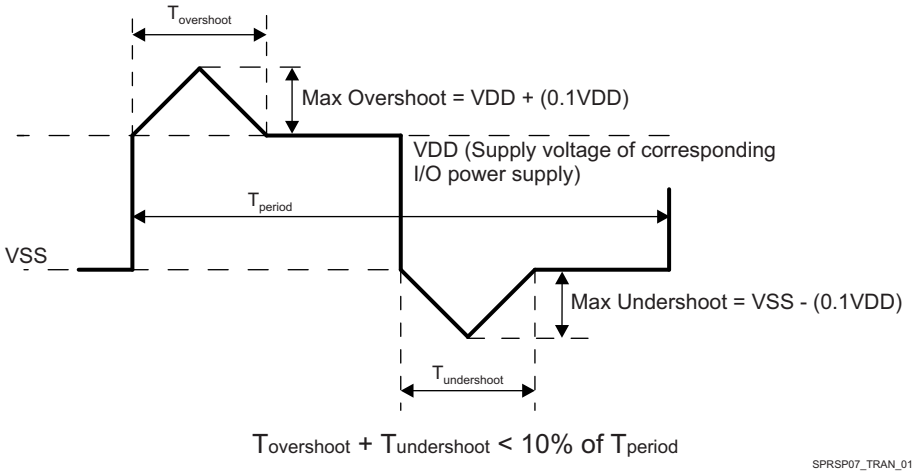

Figure 5-1. I2C I/O transient voltage ranges

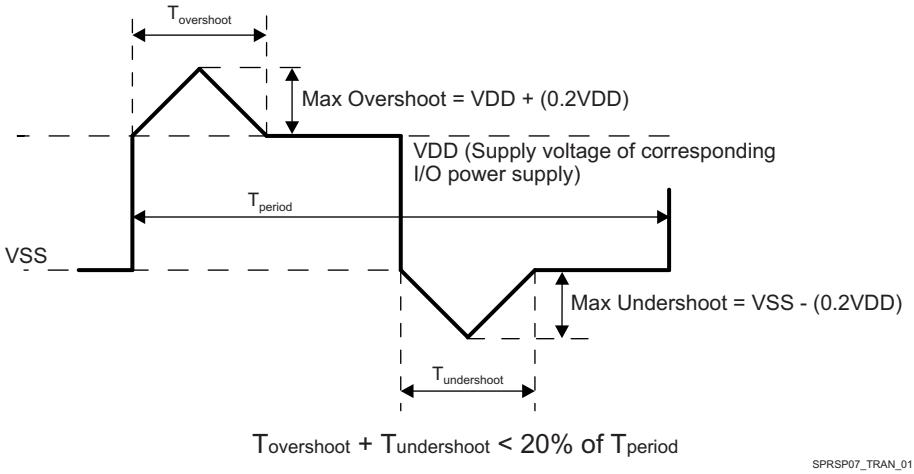

Figure 5-2. All other I/Os transient voltage ranges

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	All balls (except M5)	±2000	V
			Ball M5	±1000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	All balls (except H5, A1, A25, AE1, and AE25)	±500	V
			Ball H5	±250	
			Corner balls (A1, A25, AE1, and AE25)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Power-On-Hour (POH) Limits[1][2][3]

COMMERCIAL TEMPERATURE RANGE		EXTENDED TEMPERATURE RANGE		INDUSTRIAL EXTENDED TEMPERATURE RANGE	
JUNCTION TEMP (Tj)	LIFETIME (POH)	JUNCTION TEMP (Tj)	LIFETIME (POH)	JUNCTION TEMP (Tj)	LIFETIME (POH)
0°C to 90°C	100000	-40°C to 105°C	100000	-40°C to 125°C	20000

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

(2) Unless specified in the table above, all voltage domains and operating conditions are supported in the device at the noted temperatures.

(3) POH is a function of voltage, temperature and time. Usage at higher voltages and temperatures will result in a reduction in POH.

5.4 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)[4][7]

SUPPLY NAME	DESCRIPTION		MIN[1]	NOM	MAX[1]	UNIT
INPUT POWER SUPPLY VOLTAGE RANGE						
CVDD	Core voltage domain supply	Device Speed 60	0.855	0.9	0.945	V
		Device Speed 100	0.95	1	1.05	V
CVDD1	Core memory array power supply	Device Speed 60	0.855	0.9	0.945	V
		Device Speed 100	0.95	1	1.05	V
VPP2[3]	Supply voltage range for the eFuse ROM domain		1.71	1.80	1.89	V
AVDDA_DDRPLL	DDR PLL supply		1.71	1.80	1.89	V
AVDDA_DSSPLL	DSS PLL supply		1.71	1.80	1.89	V
AVDDA_MAINPLL	CORE PLL supply		1.71	1.80	1.89	V
AVDDA_NSSPLL	NSS PLL supply		1.71	1.80	1.89	V
AVDDA_UARTPLL	UART PLL supply		1.71	1.80	1.89	V
AVDDA_ICSSPLL	ICSS PLL supply		1.71	1.80	1.89	V
AVDDA_ARMPLL	ARM PLL supply		1.71	1.80	1.89	V
DVDD_DDRDLL	DDR EMIF PHY DLL supply		1.71	1.80	1.89	V
VDDAHV	PCIe SERDES 1.8-V supply		1.71	1.80	1.89	V
DVDD_DDR	DDR EMIF IO supply when using DDR EMIF		1.28	1.35	1.42	V
	DDR EMIF IO supply when not using DDR EMIF[6]		1.71	1.80	1.89	V
DVDD18	1.8 V IO supply		1.71	1.80	1.89	V
DVDD33	3.3 V IO supply		3.135	3.3	3.465	V
DVDD33_USB	USB 3.3-V supply		3.135	3.3	3.465	V
DDR3_VREFSSTL	DDR EMIF reference input		0.49 × DVDD_DDR	0.5 × DVDD_DDR	0.51 × DVDD_DDR	V
USB0_VBUS	USB0 VBUS comparator input		0	5.0	5.25	V
USB1_VBUS	USB1 VBUS comparator input		0	5.0	5.25	V

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Recommended Operating Conditions *(continued)*

over operating junction temperature range (unless otherwise noted)[4][7]

SUPPLY NAME	DESCRIPTION		MIN[1]	NOM	MAX[1]	UNIT
USB0_ID				[5]		
USB1_ID				[5]		
T_J[2]	Operating junction temperature range	Industrial Extended	–40		125	°C
		Extended	–40		105	
		Commercial	0		90	

(1) The voltage at the device ball must never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, and so forth.

(2) Refer to Section 5.3, *Power-On-Hour (POH) Limits*.

(3) The VPP2 power supply pin is only valid for high-security (66AK2G1xS) devices. The VPP2 power source shall only be enabled while programming the customer OTP eFuse array and shall be disabled during power-up sequence, normal operation, and power-down sequence. When disabled, the power source shall not source current to, or sink current from the VPP2 terminal. This power supply pin is reserved for general purpose (66AK2G1x) devices and shall not be connected to any signal, test point, or printed circuit board trace when using 66AK2G1x devices.

(4) All voltage values are with respect to VSS, unless otherwise noted.

(5) This terminal is connected to analog circuits in the respective USB PHY. The circuit sources a known current while measuring voltage of this terminal relative to VSS. This allows the USB PHY to measure resistance of the attached ID signal. The terminal should never be connected to any external voltage source.

(6) When DDR EMIF is not being used, the DVDD_DDR supply may be connected to a 1.8 V power source to eliminate the 1.35 V power source which is required when using DDR EMIF.

(7) For details of additional power supply and reference voltage input requirements, see Section 7.3, *Power Distribution Network (PDN) Implementation Guidance*.

5.5 Operating Performance Points

This section describes the maximum operating conditions of the device.

Table 5-1 describes the operating performance point for each device speed grade.

Table 5-1. Supported Max Frequency

Maximum Frequency (MHz)	Subsystem (PLL Output)		
	Arm A15 (ARM_PLLOUT)	C66x (CHIP_CLK1)	DDR EMIF (DDR_PLLOUT)
Device Speed 60	600	600	400 (DDR3-800)
Device Speed 100	1000	1000	533 (DDR3-1066)

5.6 Power Consumption Summary

Power consumption of this device depends on several operating parameters such as operating voltages, frequencies, and temperature. Power consumption also varies by end applications that determine the overall processor, MPU/DSP, and peripheral activity. For more specific power consumption details, see *66AK2G12 Power Estimation Tool* [literature number SPRACD9]. This document references a spreadsheet for estimating power based on parameters that closely resemble the end application to generate a realistic estimate of power consumption based on use-case and operating conditions.

5.7 Electrical Characteristics

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NOTE

The interfaces or signals described in Table 5-2 through Table 5-10 correspond to the interfaces or signals available in multiplexing mode 0 (Primary Function).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY and GPIO combination, in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

Table 5-2. DDR3L SSTL DC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BALL NAMES in MUXMODE 0: DDR3_DQM[3:0], DDR3_CB[03:00], DDR3_CBDQM, DDR3_D[31:00], DDR3_CEn0, DDR3_BA[2:0], DDR3_A[15:00], DDR3_CASn, DDR3_RASn, DDR3_WEn, DDR3_CKE0, DDR3_ODT0, DDR3_RESETn, DDR3_DQS0_P, DDR3_DQS0_N, DDR3_DQS1_P, DDR3_DQS1_N, DDR3_DQS2_P, DDR3_DQS2_N, DDR3_DQS3_P, DDR3_DQS3_N, DDR3_CLKOUT_P0, DDR3_CLKOUT_N0, DDR3_CLKOUT_P1, DDR3_CLKOUT_N1, DDR3_CBDQS_P, DDR3_CBDQS_N						
BALL NUMBERS: AB4, AA5, AC8, AA9, AA11, AB11, AC11, AC12, Y11, AD2, Y4, AC3, AC2, AE3, AA4, AD3, AB3, AA6, Y7, Y6, AC5, AB6, Y5, AC4, AB5, AB7, AB8, AC7, AA7, AA8, AC6, AE7, AD7, AA10, AE10, AD10, AC10, AC9, AB10, AB9, Y8, AD13, AA14, AB13, AD17, AC15, Y15, AC16, AA15, AB16, AE17, AC14, AB15, AC17, AB17, AB14, AA16, AA17, AA12, Y17, Y16, AC13, AE13, Y13, AB18, AA13, Y18, AD1, AE2, AD4, AE4, AE6, AD6, AE9, AD9, AE15, AD15, AE16, AD16, AE12, AD12						
V_{OH}	High-level output voltage	DVDD_DDR = 1.35 V (I_{OH} = -8 mA)	DVDD_DDR – 0.4			V
V_{OL}	Low-level output voltage	DVDD_DDR = 1.35 V (I_{OL} = 8 mA)			0.4	V
V_{IH}	High-level input voltage	DVDD_DDR = 1.35 V	DDR3_VREFSSTL + 0.09			V
V_{IL}	Low-level input voltage	DVDD_DDR = 1.35 V			DDR3_VREFSSTL – 0.09	V

Table 5-3. I2C OPEN DRAIN DC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
BALL NAMES in MUXMODE 0: I2C0_SCL, I2C0_SDA, I2C1_SCL, I2C1_SDA, I2C2_SCL, I2C2_SDA					
BALL NUMBERS: U5, W5, V6, W4, V5, V4					
(I^2C STANDARD MODE / FAST MODE – 3.3 V)					
V_{IH}	High-level input voltage	0.7 × VDDS[1]			V
V_{IL}	Low-level input voltage			0.3 × VDDS[1]	V
V_{HYS}	Hysteresis	0.05 × VDDS[1]		—	V
I_{IN}	Input leakage current. This value represents the maximum current flowing in or out of the pin while the output driver is disabled and the input is swept from VSS to VDD.			8	µA
V_{OL}	Low-level output voltage at 3-mA sink current			0.4	V

(1) VDDS in this table stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see Table 4-1, POWER column.

Table 5-4. Oscillators DC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)[2]

PARAMETER		MIN	TYP	MAX	UNIT
BALL NAMES in MUXMODE 0: AUDOSC_IN, SYSOSC_IN					
BALL NUMBERS: C17, AC19					
V_{IH}	Input high-level threshold	0.65 × VDDS[1]			V
V_{IL}	Input low-level threshold			0.35 × VDDS[1]	V

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Table 5-4. Oscillators DC Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)[2]

PARAMETER			MIN	TYP	MAX	UNIT
I_{IN}	Input leakage current	Oscillator enabled, internal pull-down disabled, VSS ≤ V_I ≤ VDDS[1]			±8	µA
		Oscillator disabled, internal pull-down enabled, V_I = VDDS[1]	0.9		4.5	mA

(1) VDDS in this table stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see Table 4-1, POWER column.

(2) This table only defines input characteristics of the oscillator when being used with an LVCMOS clock source.

Table 5-5. LVDS Input Buffer DC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
BALL NAMES in MUXMODE 0: SYSCLK_P, SYSCLK_N, DDR_CLK_N, DDR_CLK_P, CPTS_REFCLK_N, CPTS_REFCLK_P					
BALL NUMBERS: AD25, AC25, AD24, AE24, L21, K21					
V_I	Input Voltage	0		VDDS[1]	V
V_{CM}	Common mode input voltage	0.1		VDDS[1] – 0.1	V
V_{IDH}	Input Differential High Voltage	100			mV
V_{IDL}	Input Differential Low Voltage			-100	mV
V_{HYS}	Input Differential Hysteresis Voltage	25			mV
R_I	Input Resistance	71		129	Ω

(1) VDDS in this table stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see Table 4-1, POWER column.

Table 5-6. LVDS Output Buffer DC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
BALL NAMES in MUXMODE 0: OBSCLK_N, OBSCLK_P						
BALL NUMBERS: L1, K1						
V_{OH}	Output High Voltage	Differential Load = 100 Ω			1.5	V
V_{OL}	Output Low Voltage	Differential Load = 100 Ω		0.9		V
V_{CM}	Common mode output voltage			1.125	1.275	V
V_{ODH}	Output Differential High Voltage	Differential Load = 100 Ω		250	450	mV
V_{ODL}	Output Differential Low Voltage	Differential Load = 100 Ω		-450	-250	mV

Table 5-7. MLB LVDS Buffers DC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
BALL NAMES in MUXMODE 0: MLBP_SIG_P, MLBP_SIG_N, MLBP_DAT_P, MLBP_DAT_N, MLBP_CLK_P, MLBP_CLK_N						
BALL NUMBERS: L24, M24, K23, K22, M23, L23						
V_I	Input Voltage		0		VDDS[1]	V
V_{IDH}	Input Differential High Voltage		50			mV
V_{IDL}	Input Differential Low Voltage				-50	mV
V_{ODH}	Output Differential High Voltage	Differential Load = 50 Ω	300		500	mV
V_{ODL}	Output Differential Low Voltage	Differential Load = 50 Ω	-500		-300	mV
$_{\Delta}V_{OD}$	Difference in Differential Output Voltage, between high/low steady-states		-50		50	mV
V_{OCM}	Common mode output voltage		1.0		1.5	V

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Table 5-7. MLB LVDS Buffers DC Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$_{\Delta}V_{OCM}$	Difference in Common Mode Output Voltage, between high/low steady-states	-50		50	mV
V_{CMV}	Variation in Common Mode Output Voltage, during logic state transitions			150	mVpp

(1) VDDS in this table stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see Table 4-1, POWER column.

Table 5-8. PORn DC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
BALL NAMES in MUXMODE 0: PORn					
BALL NUMBERS: AA3					
V_{IH}	Input High-Level Threshold	2			V
V_{IL}	Input Low-Level Threshold			0.8	V
V_{HYS}	Input Hysteresis Voltage	200			mV

Table 5-9. 1.8-Volt I/O LVCMOS DC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
BALL NAMES in MUXMODE 0: MMC1_DAT7, MMC1_DAT6, MMC1_DAT5, MMC1_DAT4, MMC1_DAT3, MMC1_DAT2, MMC1_DAT1, MMC1_DAT0, MMC1_CLK, MMC1_CMD, MMC1_SDCD, MMC1_SDWP, MMC1_POW, OBSPLL_LOCK						
BALL NUMBERS: G5, F4, G4, E3, H4, J5, F5, H3, J4, J2, J3, K3, K2, N5						
V_{IH}	Input High-Level Threshold		0.65 × VDDS[2]			V
V_{IL}	Input Low-Level Threshold				0.35 × VDDS[2]	V
V_{HYS}	Input Hysteresis Voltage		228			mV
V_{OH}	Output High-Hevel Threshold	BUFFERCLASS = 00 (I_{OH}= -6 mA)	VDDS[2] – 0.45			V
		BUFFERCLASS = 01, 10, or 11 (I_{OH}= -7 mA)	VDDS[2] – 0.45			V
V_{OL}	Output Low-Level Threshold	BUFFERCLASS = 00 (I_{OL}= 6 mA)			0.45	V
		BUFFERCLASS = 01, 10, or 11 (I_{OL}= 7 mA)			0.45	V
I_{IN}	Input Leakage Current, Pull-up or Pull-down Inhibited				3	µA
	Input Leakage Current, Pull-down Enabled, V_I = VDDS[2]		58	100	188	µA
	Input Leakage Current, Pull-up Enabled, V_I = VSS		-58	-100	-188	µA
I_{OZ}	Total leakage current through the driver/receiver combination, which may include an internal pull-up or pull-down. This value represents the maximum current flowing in or out of the pin while the output driver is disabled, the pull-up or pull-down is inhibited, and the input is swept from VSS to VDD.				3	µA

(1) For more information on the I/O cell configurations, see section *Pad Configuration Registers* in section *Control Module (BOOT_CFG)* of chapter *Device Configuration* of the Device TRM.

(2) VDDS in this table stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see Table 4-1, POWER column.

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Table 5-10. 3.3-Volt I/O LVCMOS DC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER			MIN	TYP	MAX	UNIT
BALL NAMES in MUXMODE 0: ALL other IOs						
BALL NUMBERS: ALL other IOs						
V_{IH}	Input high-level threshold		2			V
V_{IL}	Input low-level threshold				0.8	V
V_{HYS}	Input hysteresis voltage		200			mV
V_{OH}	Output high-level threshold	BUFFERCLASS = 00, 01 (I_{OH} = -3 mA)	VDDS(2) – 0.2			V
		BUFFERCLASS = 10, 11 (I_{OH} = -3.5 mA)	VDDS(2) – 0.2			V
		BUFFERCLASS = 10, 11 (I_{OH} = -6 mA)	VDDS(2) – 0.45			V
V_{OL}	Output low-level threshold	BUFFERCLASS = 00, 01 (I_{OL} = 3 mA)			0.2	V
		BUFFERCLASS = 10, 11 (I_{OL} = 3.5 mA)			0.2	V
		BUFFERCLASS = 10, 11 (I_{OL} = 6 mA)			0.45	V
I_{IN}	Input leakage current, pull-up or pull-down inhibited				10	µA
	Input leakage current, pull-down enabled, V_I = VDDS(2)		50	120	210	µA
	Input leakage current, pull-up enabled, V_I = VSS		-60	-120	-200	µA
I_{OZ}	Total leakage current through the driver/receiver combination, which may include an internal pull-up or pull-down. This value represents the maximum current flowing in or out of the pin while the output driver is disabled, the pull-up or pull-down is inhibited, and the input is swept from VSS to VDD.				10	µA

(1) For more information on the I/O cell configurations, see section *Pad Configuration Registers* in section *Control Module (BOOT_CFG)* of chapter *Device Configuration* of the Device TRM.

(2) VDDS in this table stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see Table 4-1, POWER column.

5.7.1 USB0_PHY and USB1_PHY DC Electrical Characteristics

NOTE

USB0 and USB1 Electrical Characteristics are compliant with Universal Serial Bus Revision 2.0 Specification dated April 27, 2000 including ECNs and Errata as applicable.

5.7.2 PCIe SERDES DC Electrical Characteristics

NOTE

The PCIe interfaces are compliant with the electrical parameters specified in PCI Express® Base Specification Revision 2.0 and PCI Express Card Electromechanical Specification Revision 2.0.

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5.8 Thermal Resistance Characteristics for ABY Package

This section provides the thermal resistance characteristics for the ABY package used on this device.

The *Thermal Design Guide for DSP and Arm Application Processors Application Report* (SPRABI3) available from http://www.ti.com/lit/pdf/sprabi3 provides guidance for successful implementation of a thermal solution for system designs containing this device. This document provides background information on common terms and methods related to thermal solutions. TI only supports designs that follow system design guidelines contained in the application report.

For reliability and operability concerns, the maximum junction temperature of the Device has to be at or below the T_J value identified in Section 5.4, *Recommended Operating Conditions*.

Table 5-11. Thermal Resistance Characteristics for ABY Package

It is recommended to perform thermal simulations at the system level with the worst case device power consumption(3).

NO.	NAME	DESCRIPTION	ABY °C/W(1) (4)	AIR FLOW (m/s)(2)
T1	$R\Theta_{JC}$	Junction-to-case	0.3	N/A
T2	$R\Theta_{JB}$	Junction-to-board	4.2	N/A
T3	$R\Theta_{JA}$	Junction-to-free air	14.2	0.0
T4	$R\Theta_{JMA}$	Junction-to-moving air	9.1	1.0
T5			8.2	2.0
T6			7.7	3.0
T7	Ψ_{JT}	Junction-to-package top	0.2	0.0
T8			0.2	1.0
T9			0.2	2.0
T10			0.2	3.0
T11	Ψ_{JB}	Junction-to-board	3.9	0.0
T12			3.4	1.0
T13			3.3	2.0
T14			3.2	3.0

(1) These values were derived from thermal simulations using 1W of power dissipation and an ambient temperature of 25°C following methods defined in the standards listed below. These values may not represent actual use conditions of the device.
The following standards define test methods used to derive JA, JMA, JB and JC:
- JESD51-2:*Integrated Circuits Thermal Test Method Environmental Conditions – Natural Convection (Still Air)*
- JESD51-6:*Integrated Circuits Thermal Test Method Environmental Conditions – Force Convection (Moving Air)*
- JESD51-8: *Integrated Circuits Thermal Test Method Environmental Conditions – Junction-to-Board*
- SEMI G30-88: *Junction-to-Case Thermal Resistance Measurements of Ceramic Packages*

The following standard defines the test board used in above tests:
- JESD51-9: *Test Boards for Area Array Surface Mount Package Thermal Measurement*

(2) m/s = meters per second.

(3) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

(4) °C/W = degrees Celsius per watt.

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5.9 Timing and Switching Characteristics

The timing parameter symbols used in Section 5.9 are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated in Table 5-12:

Table 5-12. Timing Parameters Subscripts

SYMBOL	PARAMETER
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or don't care level
F	Fall time
H	High
L	Low
R	Rise time
V	Valid
IV	Invalid
AE	Active Edge
FE	First Edge
LE	Last Edge
Z	High impedance

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5.9.1 Power Supply Sequencing

This section describes the power-up and power-down sequences required to ensure proper device operation. The power supply names described in this section comprise a superset of a family of compatible devices. Some members of this family will not include a subset of these power supplies and their associated device modules. Refer to Section 4.2, *Pin Attributes* of the Section 4, *Terminal Configuration and Functions* to determine which power supplies are applicable.

5.9.1.1 Power-Up Sequence

Figure 5-3 describes the Power-Up Sequencing of the device.

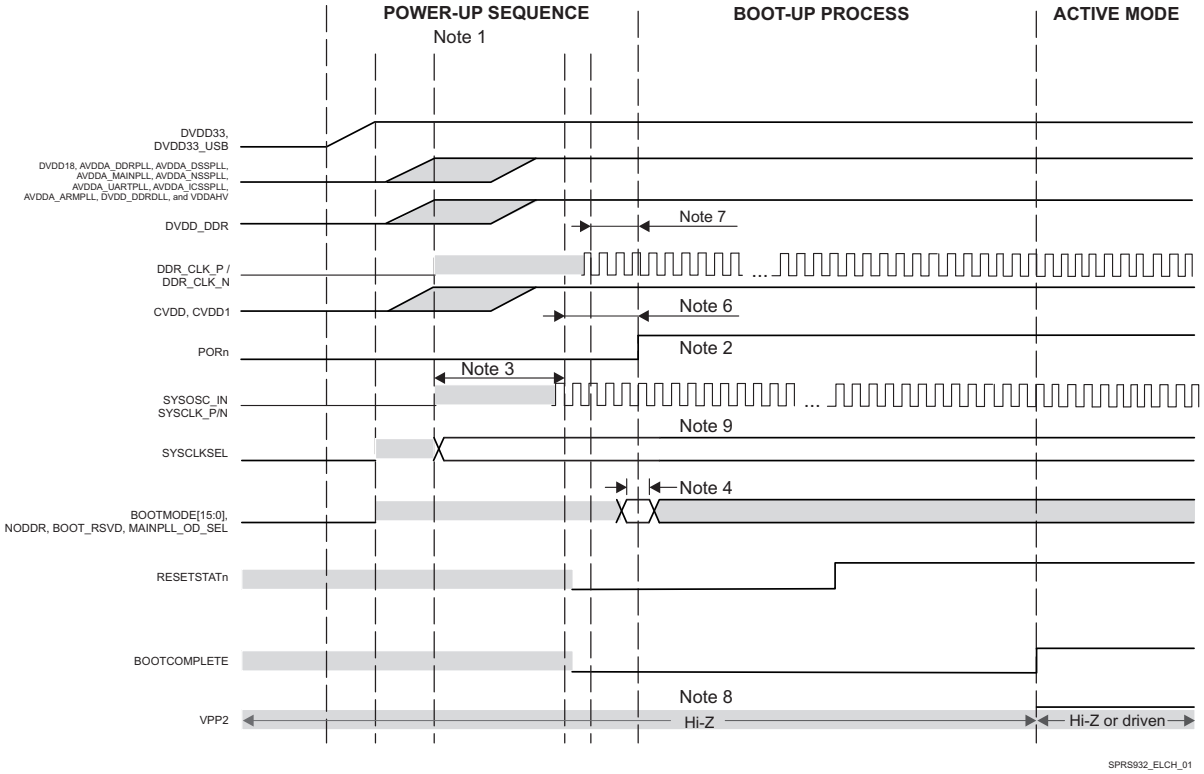

Figure 5-3. Power-Up Sequencing

(1) Power-up begins by asserting PORn and applying DVDD33 first.

(2) PORn shall be asserted before the power-up sequence begins and held until all power supplies are within their specified recommended operating range.

(3) Oscillator Power-up time defines where SYSOSC may start oscillation and the time required for oscillation to become stable, which is a function the crystal circuit components selected.

(4) BOOTMODE pins are synchronously latched after the rising edge of PORn using SYSOSC_IN or SYSCLK_P / N with setup and hold timing requirements defined in Table 5-15, *Boot Configuration Timing Requirements*.

(5) RESETSTATn and BOOTCOMPLETE are outputs and only shown for informational purposes.

(6) SYSOSC_IN or SYSCLK_P/N reference clock shall be valid at least 2 ms before PORn is released.

(7) If externally sourced, must be present prior to PORn.

(8) The VPP2 power supply pin is only valid for high-security (66AK2G1xS) devices. The VPP2 power source shall only be enabled while programming the customer OTP eFuse array and shall be disabled during power-up sequence, normal operation, and power-down sequence. When disabled, the power source shall not source current to, or sink current from the VPP2 terminal. This power supply pin is reserved for general purpose (66AK2G1x) devices and shall not be connected to any signal, test point, or printed circuit board trace when using 66AK2G1x devices.

(9) The SYSCLKSEL must be driven to the appropriate and valid logic level at least 500ns before the rising edge of PORn, then held at the same logic level as long as the device is operational.

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5.9.1.2 Power-Down Sequence

The Power-up sequence shall be reversed for the Power-down sequence.

- Assert PORn while all power supplies are still valid.
- Remove voltage sources connected to non-fail-safe inputs.
- Continue to hold PORn low and DVDD33 valid while other power supplies decay.
- Continue to hold PORn low while DVDD33 decays.

Figure 5-4 describes the Power-down Sequencing of the device.

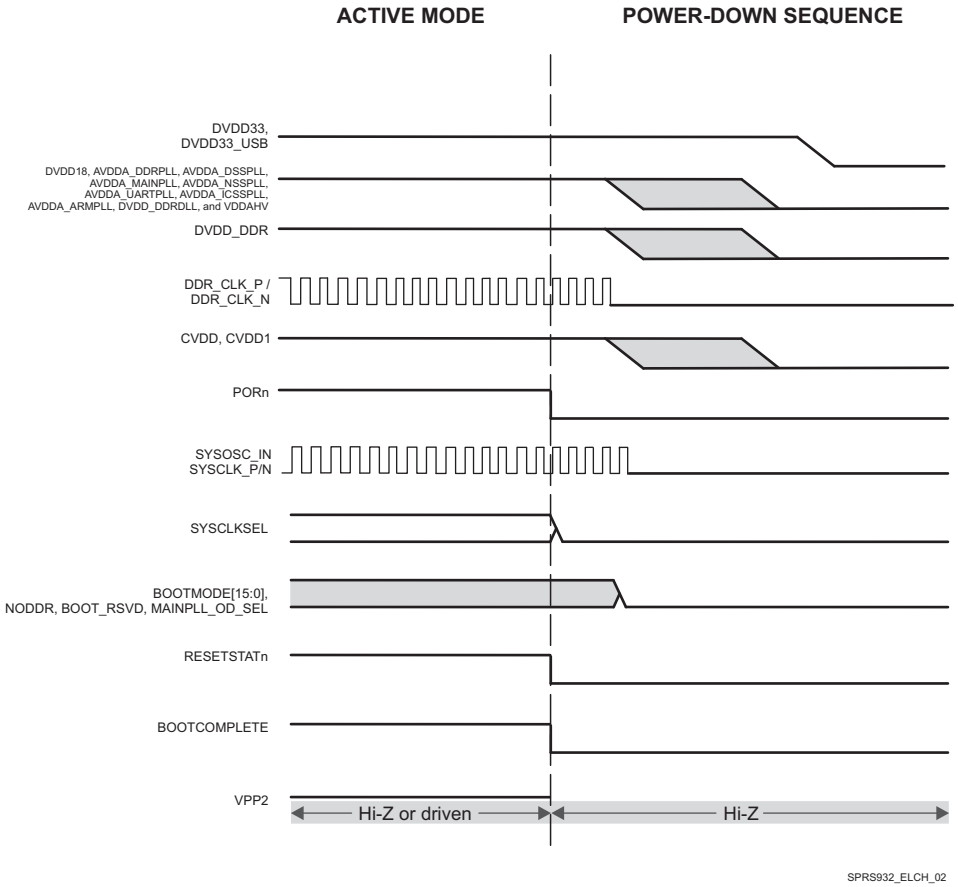

Figure 5-4. Power-Down Sequencing

5.9.2 Reset Timing

5.9.2.1 Reset Electrical Data/Timing

For more details about features and additional description information on the subsystem multiplexing signals, see the corresponding sections within Section 4.3, *Signal Descriptions* and Section 6, *Detailed Description*.

Table 5-13, Table 5-14, Figure 5-5, and Figure 5-6 present the reset timing requirements and switching characteristics.

Table 5-13. Reset Timing Requirements

NO.	PARAMETER		MIN	MAX	UNIT
	PORn Pin				
RST1	$t_{w(PORn)}$	Pulse width - pulse width PORn low	500C[1]		ns
	RESETn Pin				
RST2	$t_{w(RESETn)}$	Pulse width - pulse width RESETn low	500C[1]		ns

(1) C = 1/SYSCLK1 in ns. SYSCLK1 clock is sourced from the main PLL.

Table 5-14. Reset Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
	PORn Pin				
RST3	$t_{d(CVDD - PORn)}$	Delay time - PORn high after CVDD/CVDD1 ramped		2	ms
RST4	$t_{d(PORn - RESETSTATn)}$	Delay time - RESETSTATn high after PORn high		50000C[1]	ns
	RESETn Pin				
RST5	$t_{d(RESETn-RESETSTATn)}$	Delay time - RESETSTATn high after RESETn high		50000C[1]	ns

(1) C = 1/SYSCLK1 in ns. SYSCLK1 clock is sourced from the main PLL.

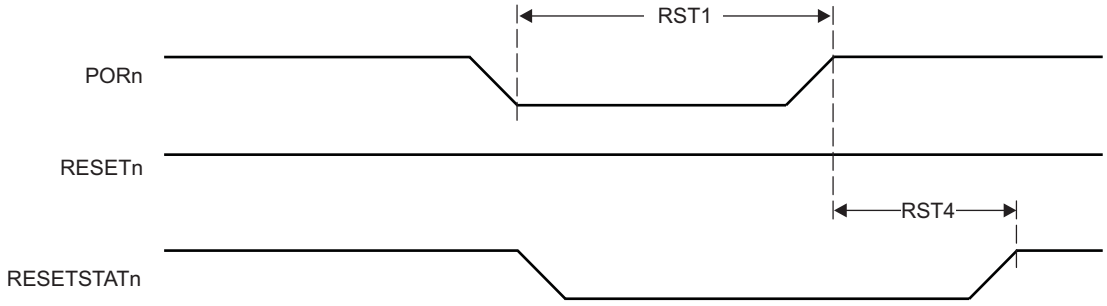

Figure 5-5. PORn Reset Timing

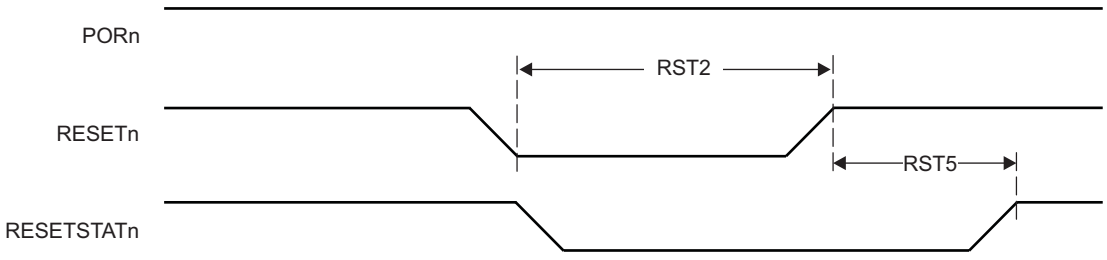

Figure 5-6. Soft/Hard Reset Timing

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Table 5-15 and Figure 5-7 present the boot configuration timing requirements.

Table 5-15. Boot Configuration Timing Requirements

NO.	PARAMETER		MIN	MAX	UNIT
BC1	$t_{su(BOOTMODE-PORn)}$	Setup time – BOOTMODE valid before PORn asserted	12C[1]		ns
BC2	$t_{h(PORn-BOOTMODE)}$	Hold time – BOOTMODE valid after PORn asserted	12C[1]		ns

(1) C = 1/SYSCLK1 in ns. SYSCLK1 clock is sourced from the main PLL.

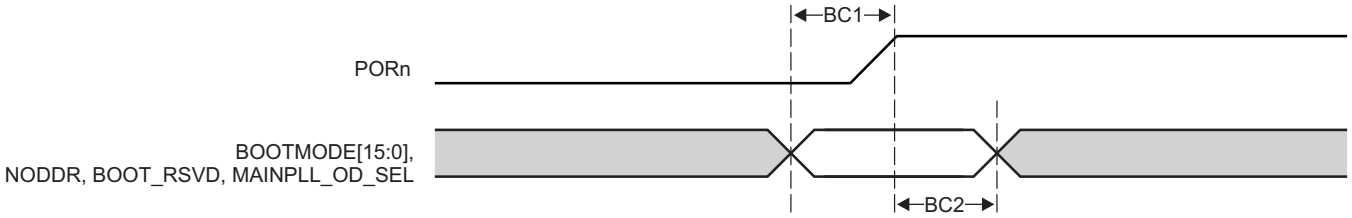

Figure 5-7. Boot Configuration Timing

5.9.3 Clock Specifications

5.9.3.1 Input Clocks / Oscillators

Various external clock sources are required as timing references for the device. Specific clock requirements are based on use cases supported by the application. Summary of these input clock signals are:

- SYSOSC_IN / SYSOSC_OUT - system oscillator (SYSOSC) pins. SYSOSC is used to source the system reference clock (SYS_OSCCLK) when the SYSCLKSEL pin is low. The SYSOSC pins can be connected to the appropriate external crystal circuit or the oscillator can be bypassed when using an LVCMOS clock source connected to the SYSOSC_IN pin.

NOTE

When connecting SYSOSC_IN to an LVCMOS clock source, the LVCMOS clock source output must be disabled anytime SYSOSC is disabled since SYSOSC_IN has a strong internal pull-down resistor which is turned on when SYSOSC is disabled.

- SYSCLK_P / SYSCLK_N - optional system clock LVDS differential input. This input is used to source the system reference clock (SYS_OSCCLK) when the SYSCLKSEL pin is high.
- DDR_CLK_P / DDR_CLK_N - optional DDR/EMIF clock LVDS differential input. This input is used to produce a DDR PLL reference clock (DDR_CLK) when the DDR_CLK_MUXSEL bit is high.
- AUDOSC_IN / AUDOSC_OUT - optional audio oscillator (AUDIOOSC) pins. AUDIOOSC can be used to produce an audio reference clock (AUDIO_OSCCLK) which is one of several clock options for the McASPs and McBSP. When used, AUDIOOSC can be connected to the appropriate external crystal circuit or the oscillator can be bypassed when using an LVCMOS clock source connected to the AUDOSC_IN pin.

NOTE

When connecting AUDOSC_IN to an LVCMOS clock source, the LVCMOS clock source output must be disabled anytime AUDOSC is disabled since AUDOSC_IN has a strong internal pull-down resistor which is turned on when AUDIOOSC is disabled. This requires the LVCMOS clock source to be disabled by default and output enable controlled by software via a general purpose output since AUDIOOSC is disabled by default.

- PCIE_CLK_P / PCIE_CLK_N - PCIe reference clock LVDS differential input.
- USB0_XO / USB1_XO - optional USB PHY reference clock.

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- CPTS_REFCLK_P / CPTS_REFCLK_N - CPTS reference clock LVDS differential input.

Figure 5-8 shows the external input clock sources to peripherals.

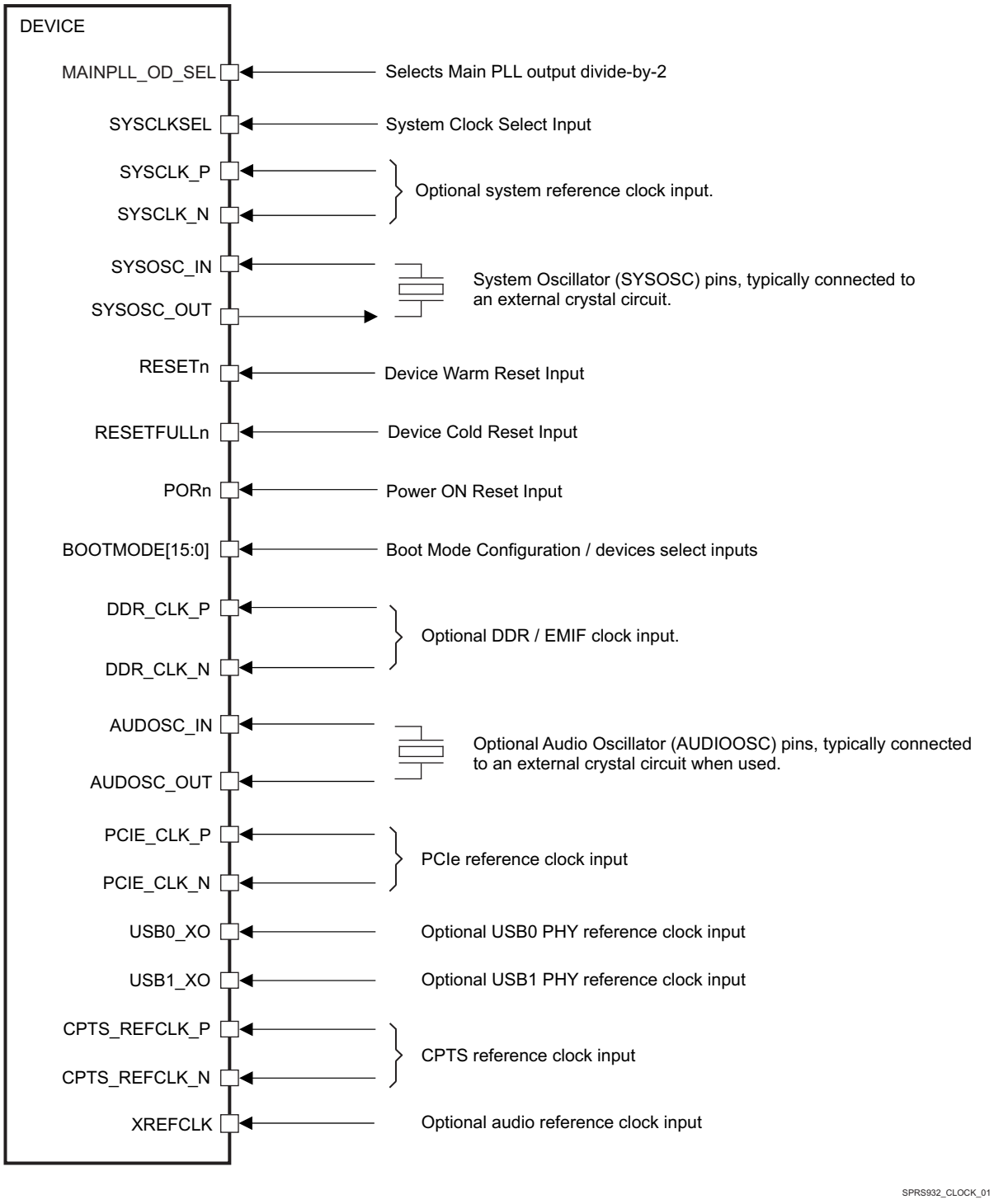

Figure 5-8. Input Clocks Interface

For more information related to clock inputs, see section *Clock Management* in chapter *Device Configuration* of the Device TRM.

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5.9.3.1.1 System Oscillator (SYSOSC) with External Crystal Circuit

Figure 5-9 shows the recommended crystal circuit. It is recommended that preproduction printed-circuit board (PCB) designs include the optional resistor Rd in case a damping resistor is required for proper oscillator operation when combined with production crystal circuit components. In most cases, Rd is a 0-Ω resistor. This resistor may be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on preproduction PCBs.

The SYSOSC_IN terminal has a 400-Ω to 2-kΩ internal pull-down resistor which is enabled when SYSOSC is disabled. This internal resistor prevents the SYSOSC_IN terminal from floating to an invalid logic level which may increase leakage current through the oscillator input buffer.

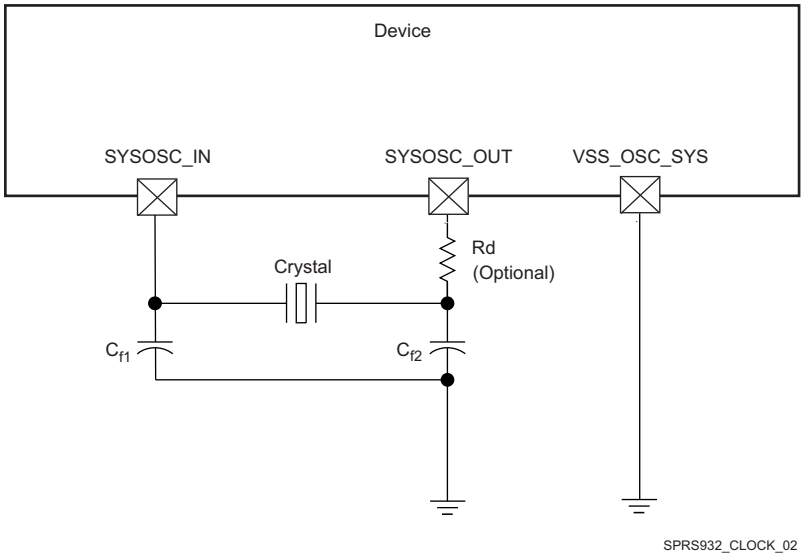

Figure 5-9. Crystal Implementation(1)

(1) Rd = 0 Ω for no damping case.

NOTE

The load capacitors, C_{f1} and C_{f2} in Figure 5-9, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the SYSOSC_IN and SYSOSC_OUT pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

SPRS932_CLOCK_03

Figure 5-10. Load capacitance equation

When selecting a crystal, the system designer must consider the temperature and aging characteristics of a crystal based on the worst case environment and life expectancy of the system.

The crystal must be in the fundamental mode of operation and parallel resonant. Table 5-16 summarizes the required electrical constraints.

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Table 5-16. SYSOSC Crystal Circuit Requirements[2]

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_c	Parallel resonance crystal frequency		19.2, 24, 25, 26		MHz
C_{f1}	C_{f1} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$	12		24	pF
C_{f2}	C_{f2} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$	12		24	pF
ESR(C_{f1}, C_{f2})	Crystal ESR			65	Ω
C_O	Crystal shunt capacitance			4	pF
$f_{a(SYSOSC_IN)}$	Frequency accuracy[1], SYSOSC_IN			50	ppm

(1) Frequency accuracy should include all components of frequency error - initial frequency tolerance, frequency stability across worst case environmental conditions, and frequency shifts due to aging.

(2) It may be difficult to find a crystal that meets all of the requirements defined in this table when searching commonly available crystal data sheets. Most commonly available crystal data sheets are non-part number specific and publish worst case parameters for all crystal within the family or series. For example, the data sheet may publish a single value for ESR and shunt capacitance which represents the worst case value for every part number within the series. However, these values may be much lower for higher frequency crystals within the series.
The recommended approach is to search non-part number specific data sheets to identify a few candidates that meet your specific system requirements along with the requirements defined in this table. Once a few candidates have been identified, contact the respective crystal manufacture and request part number specific data sheets to validate each crystal specific parameter meets all requirements

5.9.3.1.2 System Oscillator (SYSOSC) with External LVCMOS Clock Source

The internal oscillator may be bypassed by connecting to an LVCMOS clock source as shown in Figure 5-11. The SYSOSC_IN pin is connected to the LVCMOS-Compatible clock source. The SYSOSC_OUT pin is left unconnected. The VSS_OSC_SYS pin is connected to board ground (VSS).

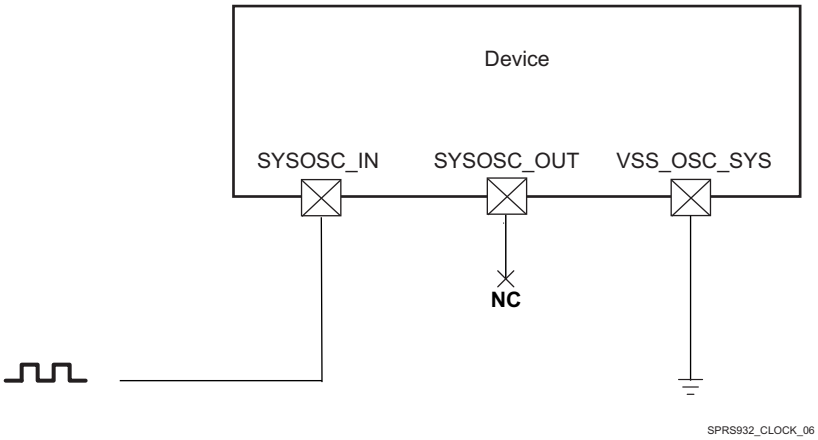

Figure 5-11. LVCMOS-Compatible Clock Input

Table 5-17 details the SYSOSC_IN input clock timing requirements.

Table 5-17. SYSOSC_IN Input Clock Timing Requirements

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
CK0	$f_{c(SYSOSC_IN)}$	Frequency, SYSOSC_IN		19.2, 24, 25, 26		MHz
CK1	$t_{w(SYSOSC_IN)}$	Pulse duration, SYSOSC_IN low or high	1/(2.22 × $f_{c(SYSOSC_IN)}$)		1/(1.82 × $f_{c(SYSOSC_IN)}$)	ns
	$t_{j(SYSOSC_IN)}$	Period jitter[1], SYSOSC_IN			50	ps
	$t_{R(SYSOSC_IN)}$	Rise time, SYSOSC_IN			5	ns
	$t_{F(SYSOSC_IN)}$	Fall time, SYSOSC_IN			5	ns
	$f_{a(SYSOSC_IN)}$	Frequency accuracy[2], SYSOSC_IN			50	ppm

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(1) Period jitter is meant here as follows:

– The maximum value is the difference between the longest measured clock period and the expected clock period

– The minimum value is the difference between the shortest measured clock period and the expected clock period

(2) LVCMOS clock source frequency accuracy should include all components of frequency error - initial frequency tolerance, frequency stability across worst case environmental conditions, and frequency shifts due to aging.

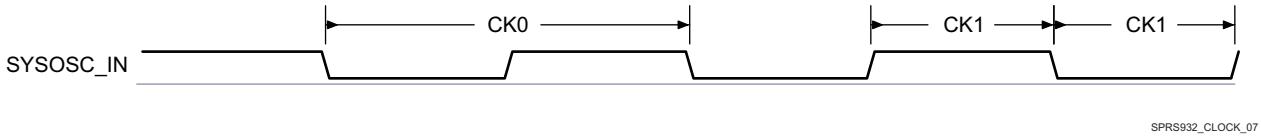

Figure 5-12. SYSOSC_IN Input Clock

5.9.3.1.3 System Oscillator (SYSOSC) Not Used

SYSOSC_IN must be connected to VSS through an external pull resistor to insure this input is held to a valid logic low level when unused since the internal pull-down resistor is disabled by default.

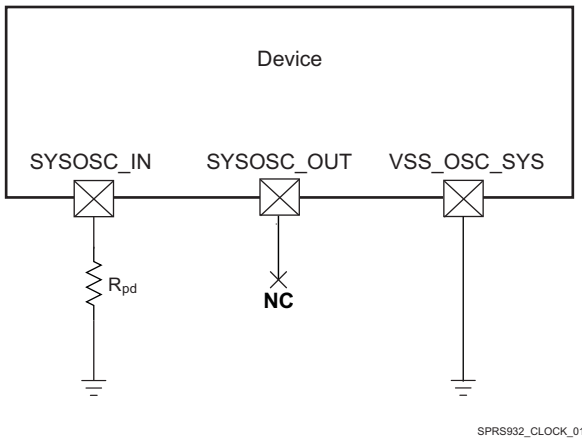

Figure 5-13. System Oscillator (SYSOSC) Not Used

5.9.3.1.4 Optional LVDS Clock Inputs

SYSCLK_P/N is an optional LVDS clock input for the system reference clock.

DDR_CLK_P/N is an optional LVDS clock input for the DDR EMIF reference clock.

CPTS_REFCLK_P/N is optional LVDS clock input for the CPTS reference clock.

External connections to support these optional clock inputs are shown in Figure 5-14, where the respective pins are connected to an LVDS-compatible clock source. Refer to Table 5-18 and Figure 5-15 for respective input clock requirements.

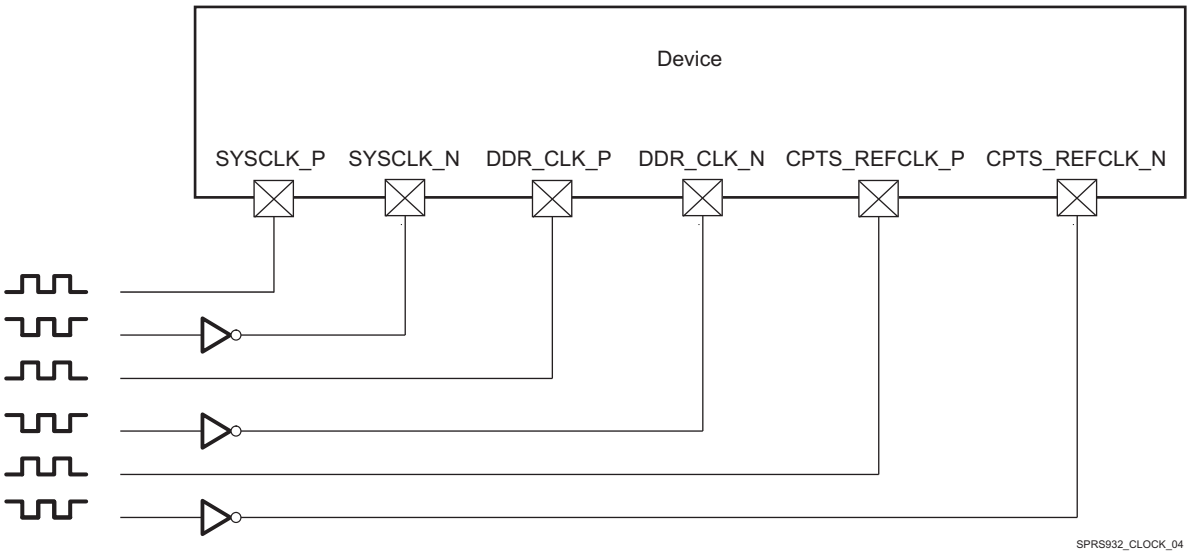

Figure 5-14. LVDS-Compatible Clock Input

Table 5-18 details the SYSCLK_P/N input clock requirements.

Table 5-18. SYSCLK_P/N Input Clock Requirements(3)

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
CK0	$f_{c(SYSCLK_P/N)}$	Frequency, SYSCLK_P/N		19.2, 24, 25, 26		MHz
	$f_{c(DDR_CLK_P/N)}$	Frequency, DDR_CLK_P/N		19.2, 24, 25, 26		
	$f_{c(CPTS_REFCLK_P/N)}$	Frequency, CPTS_REFCLK_P/N	30.72		307.2	
CK1	$t_{w(SYSCLK_P/N)}$	Pulse duration, SYSCLK_P/N low or high	1/(2.22 × $f_{c(SYSCLK_P/N)}$)		1/(1.82 × $f_{c(SYSCLK_P/N)}$)	ns
	$t_{w(DDR_CLK_P/N)}$	Pulse duration, DDR_CLK_P/N low or high				
	$t_{w(CPTS_REFCLK_P/N)}$	Pulse duration, CPTS_REFCLK_P/N low or high				
	$t_{j(SYSCLK_P/N)}$	Period jitter(1), SYSCLK_P/N			50	ps
	$t_{j(DDR_CLK_P/N)}$	Period jitter(1), DDR_CLK_P/N			100	
	$t_{j(CPTS_REFCLK_P/N)}$	Period jitter(1), CPTS_REFCLK_P/N			100	
	$t_{R(SYSCLK_P/N)}$	Rise time, SYSCLK_P/N (10%-90%)			300	ps
	$t_{R(DDR_CLK_P/N)}$	Rise time, DDR_CLK_P/N (10%-90%)				
	$t_{R(CPTS_REFCLK_P/N)}$	Rise time, CPTS_REFCLK_P/N (10%-90%)				
	$t_{F(SYSCLK_P/N)}$	Fall time, SYSCLK_P/N (90%-10%)			300	ps
	$t_{F(DDR_CLK_P/N)}$	Fall time, DDR_CLK_P/N (90%-10%)				
	$t_{F(CPTS_REFCLK_P/N)}$	Fall time, CPTS_REFCLK_P/N (90%-10%)				
	$f_{a(SYSCLK_P/N)}$	Frequency accuracy(2), SYSCLK_P/N			50	ppm
	$f_{a(DDR_CLK_P/N)}$	Frequency accuracy(2), DDR_CLK_P/N			100	
	$f_{a(CPTS_REFCLK_P/N)}$	Frequency accuracy(2), CPTS_REFCLK_P/N			100	

(1) Period jitter is meant here as follows:
- The maximum value is the difference between the longest measured clock period and the expected clock period
- The minimum value is the difference between the shortest measured clock period and the expected clock period

(2) Frequency accuracy should include all components of frequency error - initial frequency tolerance, frequency stability across worst case environmental conditions, and frequency shifts due to aging.

(3) DC electrical specifications for the SYSCLK_P/N, DDR_CLK_P/N, and CPTS_REFCLK_P/N LVDS differential inputs are defined in Table 5-5, *LVDS Input Buffer DC Electrical Characteristics*.

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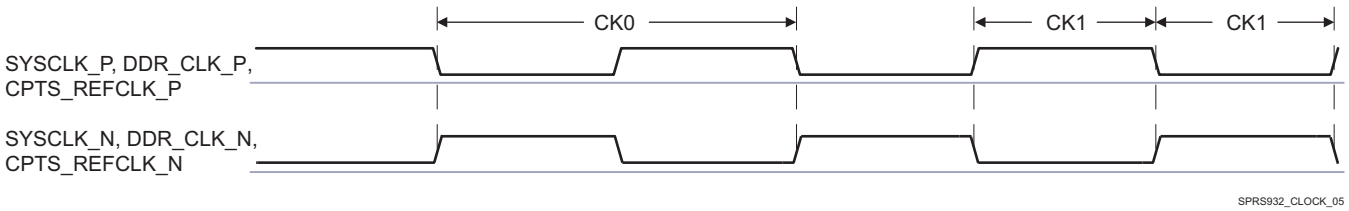

Figure 5-15. Optional LVDS Clock Inputs

5.9.3.2 Optional LVDS Clock Inputs Not Used

The differential LVDS clock inputs should be connected to the appropriate pull resistors when not used. Refer to Figure 5-16 for recommended connections.

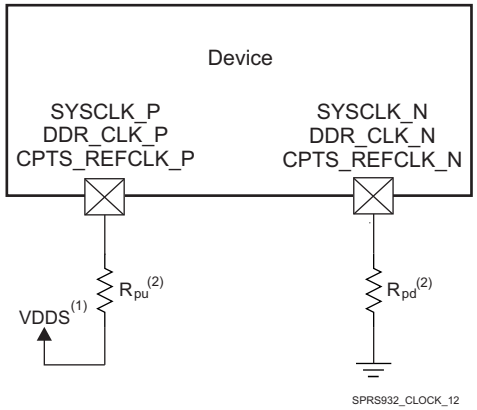

Figure 5-16. Optional LVDS Clock Input Connections Not Used

(1) VDDS in this figure stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see Table 4-1, POWER column.

(2) $R_{pu} = R_{pd} = 130\ \Omega$.

5.9.3.3 Optional Audio Oscillator (AUDOSC) with External Crystal Circuit

Figure 5-17 shows the recommended crystal circuit. It is recommended that preproduction printed-circuit board (PCB) designs include the optional resistor Rd in case a damping resistor is required for proper oscillator operation when combined with production crystal circuit components. In most cases, Rd is a 0-Ω resistor. This resistor may be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on preproduction PCBs.

The AUDOSC_IN terminal has a 400-Ω to 2-kΩ internal pull-down resistor which is enabled when AUDOSC is disabled. This internal resistor prevents the AUDOSC_IN terminal from floating to an invalid logic level which may increase leakage current through the oscillator input buffer.

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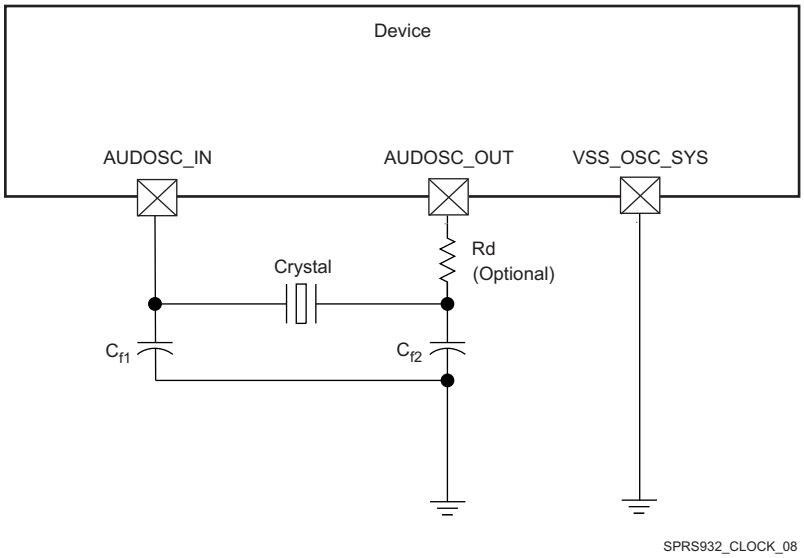

Figure 5-17. Crystal Implementation(1)

(1) Rd = 0 Ω for no damping case.

NOTE

The load capacitors, C_{f1} and C_{f2} in Figure 5-17, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the AUDOSC_IN and AUDOSC_OUT pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

SPRS932_CLOCK_03

Figure 5-18. Load capacitance equation

When selecting a crystal, the system designer must consider the temperature and aging characteristics of a crystal based on the worst case environment and life expectancy of the system.

The crystal must be in the fundamental mode of operation and parallel resonant. Table 5-19 summarizes the required electrical constraints.

Table 5-19. AUDOSC Crystal Circuit Requirements

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
f_c	Parallel resonance crystal frequency			11.2896 – 49.152		MHz
C_{f1}	C_{f1} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$		12		24	pF
C_{f2}	C_{f2} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$		12		24	pF
ESR(C_{f1},C_{f2})	Crystal ESR	11.2896 MHz –15 MHz			100	Ω
		15 MHz – 30 MHz			65	Ω
		30 MHz – 40 MHz			50	Ω
		40 MHz – 49.152 MHz			30	Ω
C_O	Crystal shunt capacitance				4	pF
$f_{a(AUDOSC_IN)}$	Frequency accuracy(1), AUDOSC_IN				100	ppm

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(1) Frequency accuracy should include all components of frequency error - initial frequency tolerance, frequency stability across worst case environmental conditions, and frequency shifts due to aging.

(2) It may be difficult to find a crystal that meets all of the requirements defined in this table when searching commonly available crystal data sheets. Most commonly available crystal data sheets are non-part number specific and publish worst case parameters for all crystal within the family or series. For example, the data sheet may publish a single value for ESR and shunt capacitance which represents the worst case value for every part number within the series. However, these values may be much lower for higher frequency crystals within the series.
The recommended approach is to search non-part number specific data sheets to identify a few candidates that meet your specific system requirements along with the requirements defined in this table. Once a few candidates have been identified, contact the respective crystal manufacture and request part number specific data sheets to validate each crystal specific parameter meets all requirements

5.9.3.4 Optional Audio Oscillator (AUDOSC) with External LVCMOS Clock Source

The internal oscillator may be bypassed by connecting to an LVCMOS clock source as shown in Figure 5-19. The AUDOSC_IN pin is connected to the LVCMOS-Compatible clock source. The AUDOSC_OUT pin is left unconnected. The VSS_OSC_SYS pin is connected to board ground (VSS).

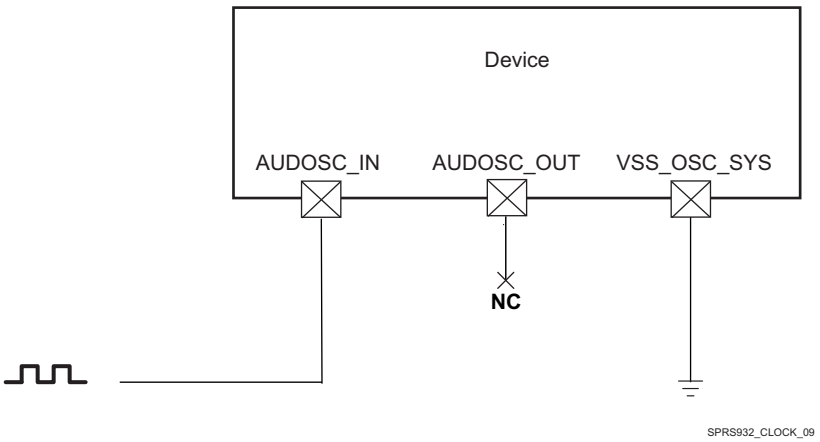

Figure 5-19. LVCMOS-Compatible Clock Input

Table 5-20 details the AUDOSC_IN input clock timing requirements.

Table 5-20. AUDOSC_IN Input Clock Timing Requirements

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
CK0	$f_{c(AUDOSC_IN)}$	Frequency, AUDOSC_IN	11.2896 – 49.152			MHz
CK1	$t_{w(AUDOSC_IN)}$	Pulse duration, AUDOSC_IN low or high	1/(2.22 x $f_{c(AUDOSC_IN)}$)		1/(1.82 x $f_{c(AUDOSC_IN)}$)	ns
	$t_{j(AUDOSC_IN)}$	Period jitter(1), AUDOSC_IN			100	ps
	$t_{R(AUDOSC_IN)}$	Rise time, AUDOSC_IN			5	ns
	$t_{F(AUDOSC_IN)}$	Fall time, AUDOSC_IN			5	ns
	$f_{a(AUDOSC_IN)}$	Frequency accuracy(1), AUDOSC_IN			100	ppm

(1) Period jitter is meant here as follows:
- The maximum value is the difference between the longest measured clock period and the expected clock period
- The minimum value is the difference between the shortest measured clock period and the expected clock period

(2) LVCMOS clock source frequency accuracy should include all components of frequency error - initial frequency tolerance, frequency stability across worst case environmental conditions, and frequency shifts due to aging.

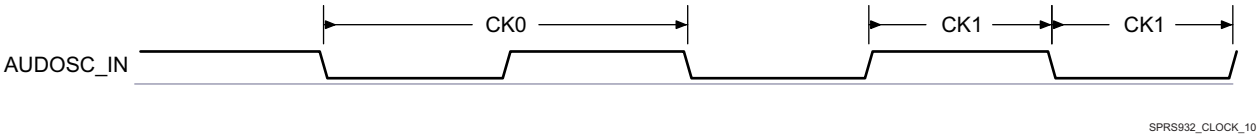

Figure 5-20. AUDOSC_IN Input Clock

5.9.3.5 Optional Audio Oscillator (AUDOSC) Not Used

AUDOSC_IN may be a no-connect while the oscillator remains disabled since the internal pull-down resistor is enabled by default.

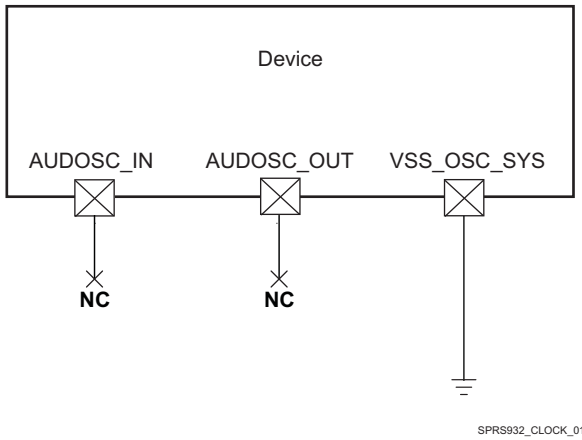

Figure 5-21. Optional Audio Oscillator (AUDOSC) Not Used

5.9.3.6 Optional USB PHY Reference Clock

Each USB PHY has an optional 1.8-Volt LVCMOS reference clock input. USB0_XO is the input to USB0 and USB1_XO is the input to USB1. A valid clock source shall be connected anytime it is selected as the reference clock. The inputs can be left floating or tied to ground if not being used.

Table 5-21. Optional USB PHY Reference Clock Requirements

NAME		DESCRIPTION	MIN	TYP	MAX	UNIT
CK0	$f_{c(USB0_XO)}$	Frequency, USB0_XO	12, 19.2, 24, 50			MHz
	$f_{c(USB1_XO)}$	Frequency, USB1_XO				
CK1	$t_{w(USB0_XO)}$	Pulse Duration, USB0_XO low or high	1/(2.5 x $f_{c(USB_XO)}$)		1/(1.67 x $f_{c(USB_XO)}$)	ns
	$t_{w(USB1_XO)}$	Pulse Duration, USB1_XO low or high				
	$t_{j(USB0_XO)}$	Period Jitter(1), USB0_XO			100	ps
	$t_{j(USB1_XO)}$	Period Jitter(1), USB1_XO				
	$t_{R(USB0_XO)}$	Rise time, USB0_XO			5	ns
	$t_{R(USB1_XO)}$	Rise time, USB1_XO				
	$t_{F(USB0_XO)}$	Fall time, USB0_XO			5	ns
	$t_{F(USB1_XO)}$	Fall time, USB1_XO				
	$t_{a(USB0_XO)}$	Frequency accuracy(2), USB0_XO			400	ppm
	$t_{a(USB1_XO)}$	Frequency accuracy(2), USB1_XO				

(1) Period jitter is meant here as follows:
- The maximum value is the difference between the longest measured clock period and the expected clock period
- The minimum value is the difference between the shortest measured clock period and the expected clock period

(2) LVCMOS clock source frequency accuracy should include all components of frequency error - initial frequency tolerance, frequency stability across worst case environmental conditions, and frequency shifts due to aging.

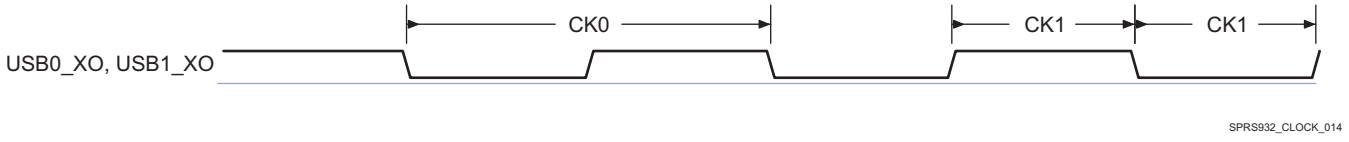

Figure 5-22. Optional USB PHY Reference Clock

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5.9.3.7 PCIe Reference Clock

PCIe requires an external reference clock. Refer to the PCI Express Card Electromechanical Specification for clock requirements.

5.9.3.8 Output Clocks

The device provides several system clock outputs. Summary of these output clock outputs are as follows:

- **CLKOUT**
  - CLKOUT port provides an option to output 50 MHz or 25 MHz clock. This clock can be used as a reference clock for RMII or MII Ethernet companion devices.
- **SYSCLKOUT**
  - SYSCLKOUT is an LVCMOS clock output of the internal clock SYSCLK1 which has been divided by 6. This output is provided for test and debug purposes only. Performance of this output is not defined due to many complex combinations of system variables. For example, this output is being sourced from the Main PLL supporting many configuration options that yield various levels of performance. There are also other unpredictable contributors to performance such as application specific noise or crosstalk which may couple into the clock circuits. Therefore, there are no plans to specify performance for this output.
- **OBSCLK**
  - OBSCLK_N / OBSCLK_P is an LVDS clock output that can be configured to observe one of 9 internal clocks. This output is provided for test and debug purposes only. Performance of this output is not defined due to many complex combinations of system variables. For example, this output may be sourced from several PLLs with each PLL supporting many configuration options that yield various levels of performance. There are also other unpredictable contributors to performance such as application specific noise or crosstalk which may couple into the clock circuits. Therefore, there are no plans to specify performance for this output.

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5.9.3.9 PLLs

Power is supplied to the PLLs by internal regulators that derive power from the off-chip power-supply.

There are seven Phase Locked Loops (PLLs) in the device:

- MAIN_PLL with PLL_CONTROLLER: (SoC, Peripherals) The Main PLL — which is used to drive the switch fabrics, accelerators, and a majority of the peripheral clocks — requires a PLL controller to manage the various clock divisions, gating, and synchronization.
- ARM_PLL: The ARM PLL, which is used to drive the ARMSS.
- DSS_PLL: (Display Subsystem) The DSS PLL, which is used to drive the DSS.
- UART_PLL: (ICSS UART) The UART PLL, which is used to drive the UART in ICSS, QSPI, MMC/SD and USB.
- ICSS_PLL: (ICSS PRUs) The ICSS PLL, which is used to drive the ICSS.
- NSS/IEP_PLL: (NSS, ICSS) The NSS/IEP PLL, which is used to drive the NSS_L and ICSS.
- DDR_PLL: (DDR EMIF / DDR PHY) The DDR PLL is used to drive the DDR EMIF PHY for the DDR EMIF.

Most of the Device is driven by the output from the main PLL except the following items:

- ARMSS has its own dedicated PLL.
- DDR subsystem has its own dedicated PLL which sources DDR EMIF and DDR EMIF PHY.
- ICSS receives clocks from several PLLs – MAIN_PLL, UART_PLL, ICSS_PLL, and NSS/IEP_PLL.
- DSS has its own dedicated PLL, which generates the DSS pixel clock.
- PCIe subsystem receives clocks from MAIN_PLL and the external 100 MHz reference clock input.
- USB has the option of being clocked from UART_PLL, NSS_PLL, or an optional external clock reference input.

NOTE

For more information, see:

- *Device Configuration* / *Clock Management* / *PLLs* section
- *Peripherals* / *Display Subsystem* Overview section of the Device TRM.

NOTE

The input reference clocks (SYSCLK_P/N or SYSOSC_IN) are specified and the lock time is guaranteed by the PLL controller, as documented in the *Device Configuration* chapter of the Device TRM.

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5.9.3.9.1 DDR_PLL Settings

Table 5-22 lists the recommended and supported values to set up the DDR3-800 configurations.

Table 5-22. DDR3-800 Configurations

Parameter	Value	Configuration Register	Register Value
Configuration 1			
Reference Clock Input	19.2 MHz	N/A	N/A
PLL Reference Divider	1	BOOTCFG_DDR3A_PLL_CTL0[5-0] PLLD	0
PLL Multiplier	167	BOOTCFG_DDR3A_PLL_CTL0[18-6] PLLM	166
PLL Output Divider	16	BOOTCFG_DDR3A_PLL_CTL0[22-19] CLKOD	15
PHY PLL Frequency Select (In DDR3 Initialization)	N/A	DDR_PHY_PLLCR[19-18] FRQSEL	0x3
PHY PLL Charge Pump Proportional Current Control (In DDR3 Initialization)	N/A	DDR_PHY_PLLCR[16-13] CPPC	0xE
Configuration 2			
Reference Clock Input	24 MHz	N/A	N/A
PLL Reference Divider	1	BOOTCFG_DDR3A_PLL_CTL0[5-0] PLLD	0
PLL Multiplier	133	BOOTCFG_DDR3A_PLL_CTL0[18-6] PLLM	132
PLL Output Divider	16	BOOTCFG_DDR3A_PLL_CTL0[22-19] CLKOD	15
PHY PLL Frequency Select (In DDR3 Initialization)	N/A	DDR_PHY_PLLCR[19-18] FRQSEL	0x3
PHY PLL Charge Pump Proportional Current Control (In DDR3 Initialization)	N/A	DDR_PHY_PLLCR[16-13] CPPC	0xE
Configuration 3			
Reference Clock Input	25 MHz	N/A	N/A
PLL Reference Divider	1	BOOTCFG_DDR3A_PLL_CTL0[5-0] PLLD	0
PLL Multiplier	128	BOOTCFG_DDR3A_PLL_CTL0[18-6] PLLM	127
PLL Output Divider	16	BOOTCFG_DDR3A_PLL_CTL0[22-19] CLKOD	15
PHY PLL Frequency Select (In DDR3 Initialization)	N/A	DDR_PHY_PLLCR[19-18] FRQSEL	0x3
PHY PLL Charge Pump Proportional Current Control (In DDR3 Initialization)	N/A	DDR_PHY_PLLCR[16-13] CPPC	0xE
Configuration 4			
Reference Clock Input	26 MHz	N/A	N/A
PLL Reference Divider	1	BOOTCFG_DDR3A_PLL_CTL0[5-0] PLLD	0
PLL Multiplier	123	BOOTCFG_DDR3A_PLL_CTL0[18-6] PLLM	122
PLL Output Divider	16	BOOTCFG_DDR3A_PLL_CTL0[22-19] CLKOD	15
PHY PLL Frequency Select (In DDR3 Initialization)	N/A	DDR_PHY_PLLCR[19-18] FRQSEL	0x3
PHY PLL Charge Pump Proportional Current Control (In DDR3 Initialization)	N/A	DDR_PHY_PLLCR[16-13] CPPC	0xE

5.9.3.10 Recommended Clock and Control Signal Transition Behavior

All clocks and strobe signals must transition from V_{IH} to V_{IL}, or from V_{IL} to V_{IH} in a monotonic manner. Monotonic transitions are more easily ensured with faster switching signals. Slower input transitions are more susceptible to glitches due to noise, and special care must be taken for clock sources with slow rise/fall times.

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5.9.4 Peripherals

5.9.4.1 DCAN

For more details about features and additional description information on the device Controller Area Network Interface, see the corresponding sections within Section 4.3, *Signal Descriptions* and Section 6, *Detailed Description*.

Table 5-23, Table 5-24, and Figure 5-23 present timing requirements and switching characteristics for DCANx Interface.

Table 5-23. Timing Requirements for DCANx Receive

NO.			MIN	MAX	UNIT
	$f_{baud(baud)}$	Maximum programmable baud rate		1	Mbps
CAN1	$t_{w(RX)}$	Pulse duration, receive data bit	H - 2(1)	H + 2(1)	ns

(1) H = period of baud rate, 1/programmed baud rate.

Table 5-24. Switching Characteristics Over Recommended Operating Conditions for DCANx Transmit

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{baud(baud)}$	Maximum programmable baud rate		1	Mbps
CAN2	$t_{w(TX)}$	Pulse duration, transmit data bit	H - 2(1)	H + 2(1)	ns

(1) H = period of baud rate, 1/programmed baud rate.

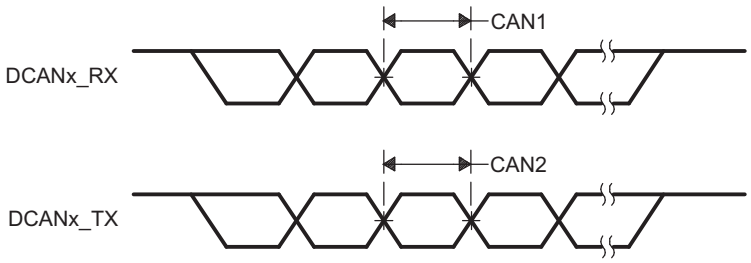

Figure 5-23. DCANx Timings

For more information, see section *Dual Controller Area Network (DCAN) Interface* in chapter *Peripherals* of the Device TRM.

5.9.4.2 DSS

For more details about features and additional description information on the device Display Subsystem – Video Output Ports, see the corresponding sections within Section 4.3, *Signal Descriptions* and Section 6, *Detailed Description*.

Table 5-25 and Figure 5-24 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-25. DPI Video Output Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
D1	$t_{c(clk)}$	Cycle time, output pixel clock DSS_PCLK	6.67		ns
D2	$t_{w(clkL)}$	Pulse duration, output pixel clock DSS_PCLK low	P(1) × 0.45		ns
D3	$t_{w(clkH)}$	Pulse duration, output pixel clock DSS_PCLK high	P(1) × 0.45		ns
D4	$t_{t(clk)}$	Transition time, output pixel clock DSS_PCLK (10%-90%)	0.7	3	ns
D5	$t_{d(clk-ctlV)}$	Delay time, output pixel clock DSS_PCLK transition to output data DSS_DATA[23:0] valid	-1.39	1.15	ns

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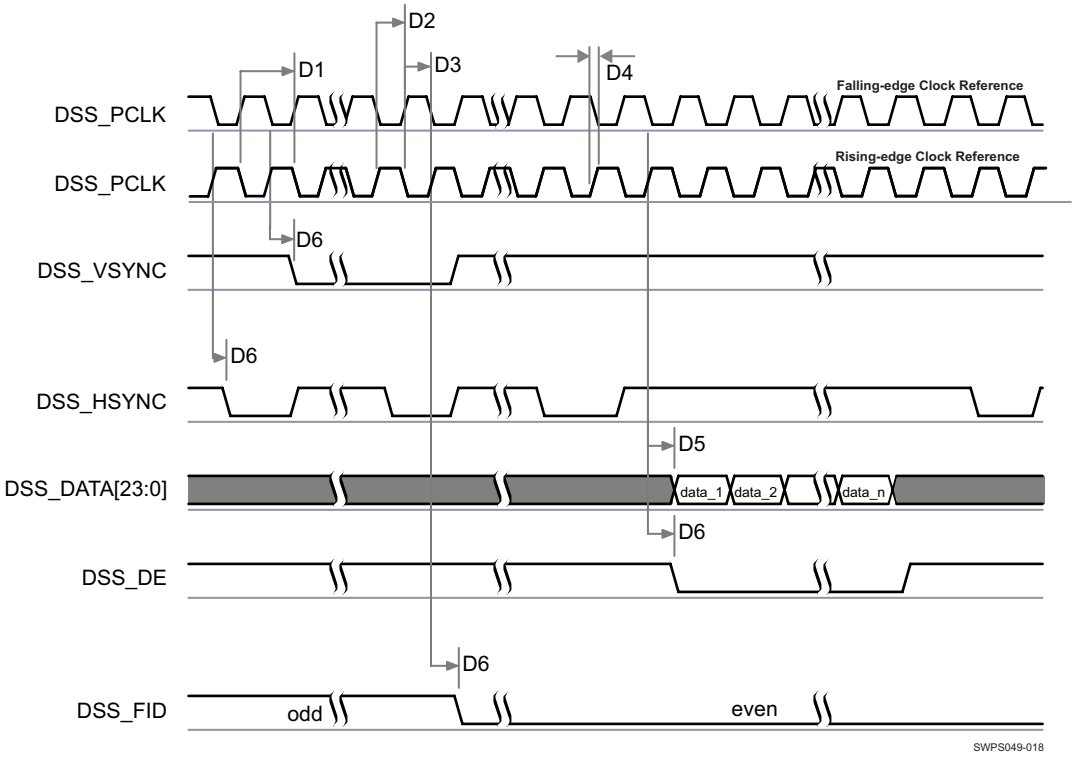
Table 5-25. DPI Video Output Switching Characteristics (continued)

NO.	PARAMETER		MIN	MAX	UNIT
D6	$t_{d(clk-dV)}$	Delay time, output pixel clock DSS_PCLK transition to output control signals DSS_VSYNC, DSS_HSYNC, DSS_DE, and DSS_FID valid	-1.39	1.15	ns

(1) P = output DSS_PCLK period in ns.



(1) The configuration of assertion of the data can be programmed on the falling or rising edge of the pixel clock.

(2) The polarity and the pulse width of DSS_HSYNC and DSS_VSYNC are programmable, refer to section *Display Subsystem (DSS)* in chapter *Peripherals* of the Device TRM.

(3) The DSS_PCLK frequency can be configured, refer to section *Display Subsystem* in chapter *Peripherals* of the Device TRM.

Figure 5-24. DPI Video Output (1)(2)(3)

5.9.4.3 DDR EMIF

For more details about features and additional description information on the device DDR3L Memory Interface, see the corresponding sections within Section 4.3, *Signal Descriptions* and Section 6, *Detailed Description*.

The device has a dedicated interface to DDR3L SDRAM. It supports JEDEC JESD79-3F and JESD79-3-1 standards compliant DDR3L SDRAM devices with the following features:

- 16-bit or 32-bit data path to external SDRAM memory
- Memory device capacity: Up to 4 GB address space available over one chip select

5.9.4.4 EMAC

For more details about features and additional description information on the device Gigabit Ethernet MAC, see the corresponding sections within Section 4.3, *Signal Descriptions* and Section 6, *Detailed Description*.

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5.9.4.4.1 EMAC MDIO Interface Timings

Table 5-26, Table 5-27, and Figure 5-25 present timing requirements for MDIO.

Table 5-26. Timing Requirements for MDIO Input

NO.	PARAMETER		MIN	MAX	UNIT
MDIO1	$t_{su(MDIO_MDC)}$	Setup time, MDIO_DATA valid before MDIO_CLK high	90		ns
MDIO2	$t_{h(MDIO_MDC)}$	Hold time, MDIO_DATA valid after MDIO_CLK high	0		ns

Table 5-27. Switching Characteristics Over Recommended Operating Conditions for MDIO Output

NO.	PARAMETER		MIN	MAX	UNIT
MDIO3	$t_{c(MDC)}$	Cycle time, MDIO_CLK	400		ns
MDIO4	$t_{w(MDCH)}$	Pulse Duration, MDIO_CLK high	160		ns
MDIO5	$t_{w(MDCL)}$	Pulse Duration, MDIO_CLK low	160		ns
MDIO6	$t_{t(MDC)}$	Transition time, MDIO_CLK		5	ns
MDIO7	$t_{d(MDC_MDIO)}$	Delay time, MDIO_CLK High to MDIO_DATA valid	10	390	ns

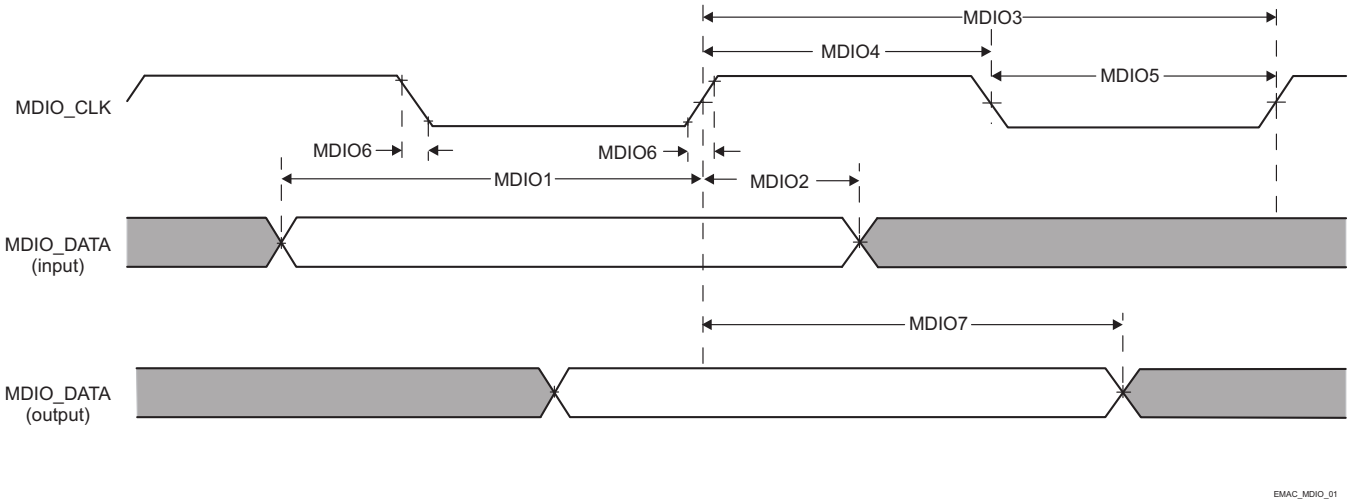

Figure 5-25. EMAC MDIO Diagrams receive and transmit

5.9.4.4.2 EMAC MII Timings

Table 5-28 and Figure 5-26 present timing requirements for MII in receive operation.

Table 5-28. Timing Requirements for MII_RXCLK—MII Operation

NO.	PARAMETER		SPEED	MIN	MAX	UNIT
MII1	$t_{c(RXCLK)}$	Cycle time, MII_RXCLK	10 Mbps	399.96	400.04	ns
			100 Mbps	39.996	40.004	ns
MII2	$t_{w(RXCLKH)}$	Pulse duration, MII_RXCLK high	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
MII3	$t_{w(RXCLKL)}$	Pulse duration, MII_RXCLK low	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
MII4	$t_{t(RXCLK)}$	Transition time, MII_RXCLK	10 Mbps		5	ns
			100 Mbps		5	ns

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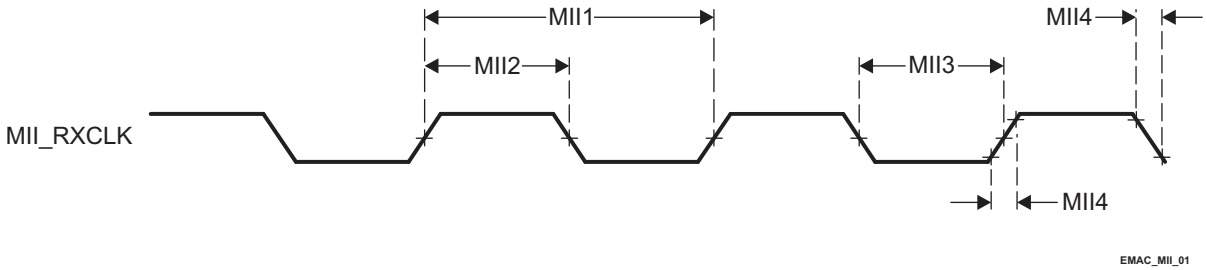

Figure 5-26. Clock Timing (EMAC Receive)—MII operation

Table 5-29 and Figure 5-27 present timing requirements for MII in transmit operation.

Table 5-29. Timing Requirements for MII_TXCLK—MII Operation

NO.	PARAMETER		SPEED	MIN	MAX	UNIT
MII1	$t_{c(TXCLK)}$	Cycle time, MII_TXCLK	10 Mbps	399.96	400.04	ns
			100 Mbps	39.996	40.004	ns
MII2	$t_{w(TXCLKH)}$	Pulse duration, MII_TXCLK high	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
MII3	$t_{w(TXCLKL)}$	Pulse duration, MII_TXCLK low	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
MII4	$t_{t(TXCLK)}$	Transition time, MII_TXCLK	10 Mbps		5	ns
			100 Mbps		5	ns

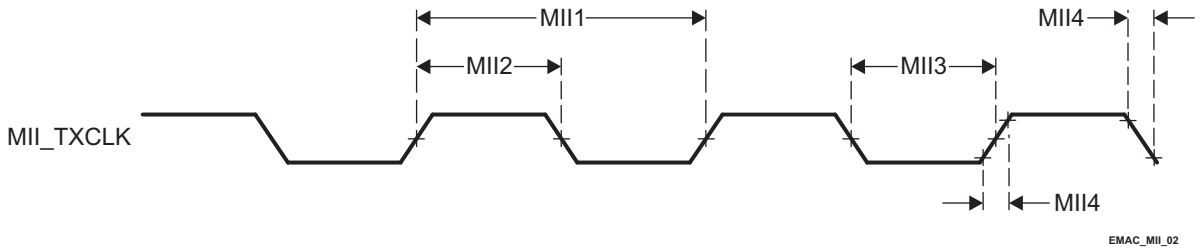

Figure 5-27. Clock Timing (EMAC Transmit)—MII operation

Table 5-30 and Figure 5-28 present timing requirements for EMAC MII Receive 10 Mbps and 100 Mbps.

Table 5-30. Timing Requirements for EMAC MII Receive 10 Mbps and 100 Mbps

NO.	PARAMETER		MIN	MAX	UNIT
MII5	$t_{su(RXD-RXCLK)}$	Setup time, receive selected signals valid before MII_RXCLK	8		ns
	$t_{su(RXDV-RXCLK)}$				
	$t_{su(RXER-RXCLK)}$				
MII6	$t_{h(RXCLK-RXD)}$	Hold time, receive selected signals valid after MII_RXCLK	8		ns
	$t_{h(RXCLK-RXDV)}$				
	$t_{h(RXCLK-RXER)}$				

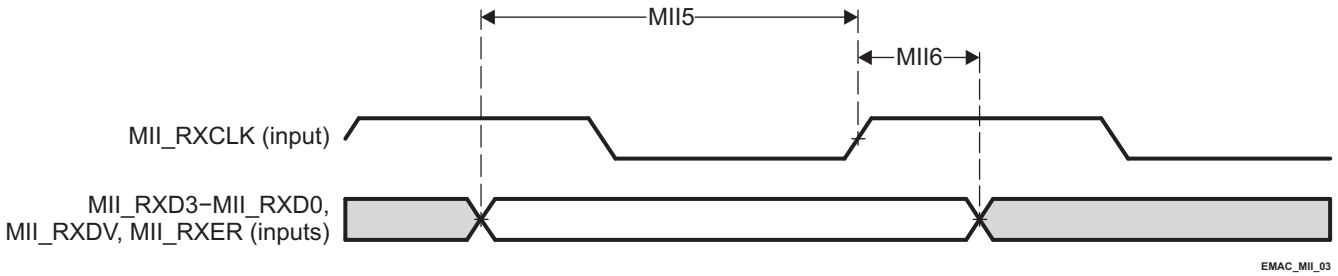

Figure 5-28. EMAC Receive Interface Timing MII operation

Table 5-31 and Figure 5-29 present timing requirements for EMAC MII Transmit 10 Mbps and 100 Mbps.

Table 5-31. Switching Characteristics Over Recommended Operating Conditions for EMAC MII Transmit 10 Mbps and 100 Mbps

NO.	PARAMETER		SPEED	MIN	MAX	UNIT
MII7	$t_{d(TXCLK-TXD)}$	Delay time, MII_TXCLK to transmit selected signals valid	10 Mbps	5	25	ns
	$t_{d(TXCLK-TXEN)}$		100 Mbps	5	25	ns

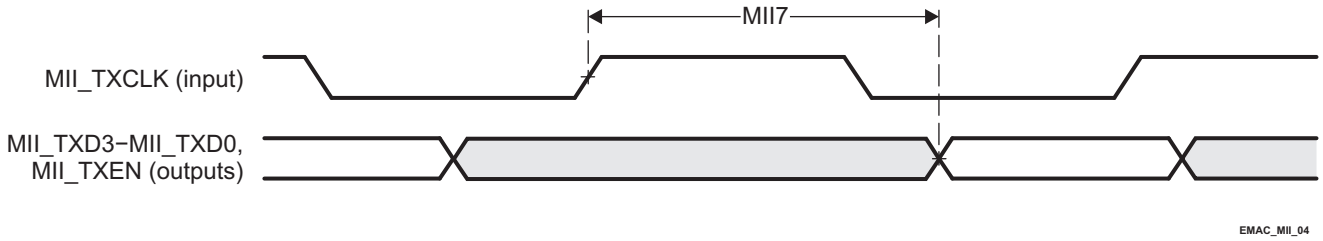

Figure 5-29. EMAC Transmit Interface Timing MII operation

5.9.4.4.3 EMAC RMII Timings

Table 5-32, Table 5-33, and Figure 5-30 present timing requirements for EMAC RMII receive.

Table 5-32. Timing Requirements for EMAC RMII_REFCLK—RMII Operation

NO.	PARAMETER		MIN	MAX	UNIT
RMII1	$t_{c(REFCLK)}$	Cycle time, RMII_REFCLK	19.999	20.001	ns
RMII2	$t_{w(REFCLKH)}$	Pulse duration, RMII_REFCLK high	7	13	ns
RMII3	$t_{w(REFCLKL)}$	Pulse duration, RMII_REFCLK low	7	13	ns
RMII4	$t_{t(REFCLK)}$	Transition time, RMII_REFCLK		5	ns

Table 5-33. Timing Requirements for EMAC RMII Receive

NO.	PARAMETER		MIN	MAX	UNIT
RMII5	$t_{su(RXD-REFCLK)}$	Setup time, receive selected signals valid before RMII_REFCLK	4		ns
	$t_{su(CRS_DV-REFCLK)}$				
	$t_{su(RXER-REFCLK)}$				
RMII6	$t_{h(REFCLK-RXD)}$	Hold time, receive selected signals valid after RMII_REFCLK	2		ns
	$t_{h(REFCLK-CRS_DV)}$				
	$t_{h(REFCLK-RXER)}$				

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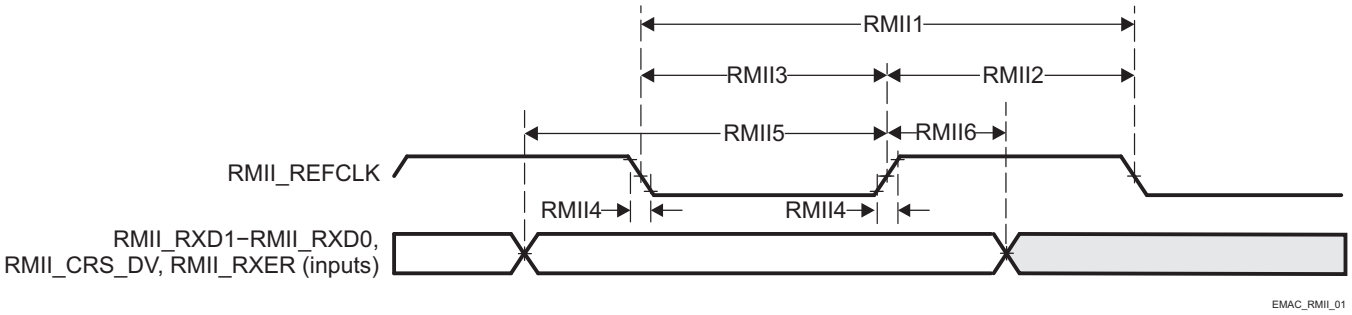


Figure 5-30. EMAC Receive Interface Timing RMII operation

Table 5-34, Table 5-34, and Figure 5-31 present switching characteristics for EMAC RMII Transmit 10 Mbps and 100 Mbps.

Table 5-34. Switching Characteristics Over Recommended Operating Conditions for EMAC RMII_REFCLK —RMII Operation

NO.	PARAMETER		MIN	MAX	UNIT
RMII7	$t_{c(REFCLK)}$	Cycle time, RMII_REFCLK	19.999	20.001	ns
RMII8	$t_{w(REFCLKH)}$	Pulse duration, RMII_REFCLK high	7	13	ns
RMII9	$t_{w(REFCLKL)}$	Pulse duration, RMII_REFCLK low	7	13	ns
RMII10	$t_{t(REFCLK)}$	Transition time, RMII_REFCLK		5	ns

Table 5-35. Switching Characteristics Over Recommended Operating Conditions for EMAC RMII Transmit 10 Mbps and 100 Mbps

NO.	PARAMETER		MIN	MAX	UNIT
RMII11	$t_{d(REFCLK-TXD)}$	Delay time, RMII_REFCLK high to selected transmit signals valid	2	13	ns
	$t_{d(REFCLK-TXEN)}$				
RMII12	$t_{r(TXD)}$	Rise time, TXD outputs	1	5	ns
	$t_{r(TXEN)}$	Rise time, TXEN output			
RMII13	$t_{f(TXD)}$	Fall time, TXD outputs	1	5	ns
	$t_{f(TXEN)}$	Fall time, TXEN output			

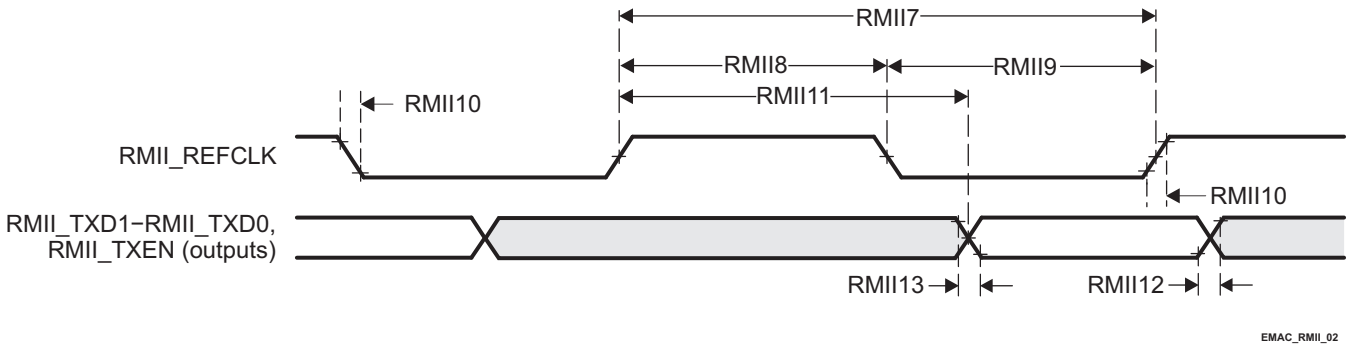


Figure 5-31. EMAC Transmit Interface Timing RMII Operation

5.9.4.4.4 EMAC RGMII Timings

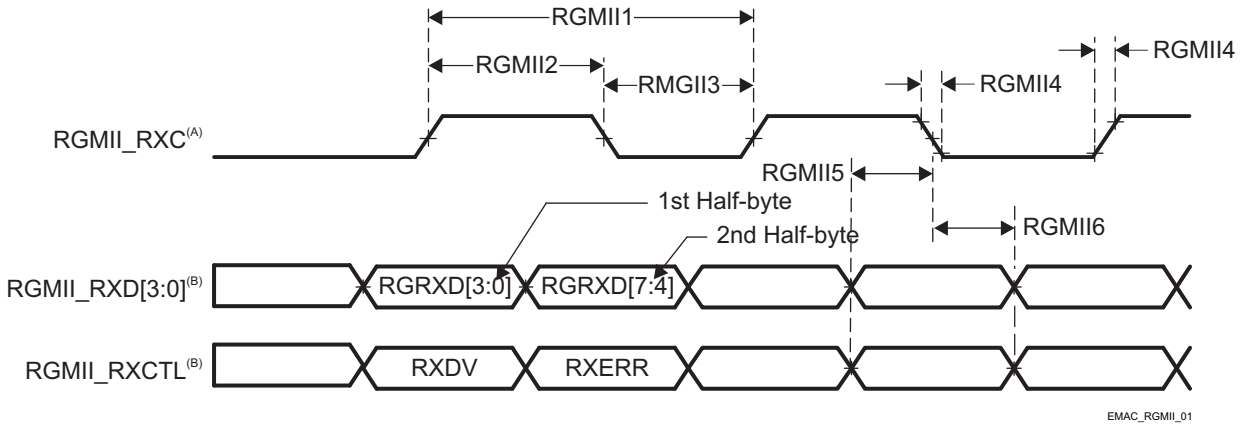
Table 5-36, Table 5-37, and Figure 5-32 present timing requirements for receive RGMII operation.

Table 5-36. Timing Requirements for RGMII_RXC—RGMII Operation

NO.	PARAMETER		SPEED	MIN	MAX	UNIT
RGMII1	$t_{c(RXC)}$	Cycle time, RGMII_RXC	10 Mbps	360	440	ns
			100 Mbps	36	44	ns
			1000 Mbps	7.2	8.8	ns
RGMII2	$t_{w(RXCH)}$	Pulse duration, RGMII_RXC high	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns
RGMII3	$t_{w(RXCL)}$	Pulse duration, RGMII_RXC low	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns
RGMII4	$t_{t(RXC)}$	Transition time, RGMII_RXC	10 Mbps		0.75	ns
			100 Mbps		0.75	ns
			1000 Mbps		0.75	ns

Table 5-37. Timing Requirements for EMAC RGMII Input Receive for 10 Mbps, 100 Mbps, and 1000 Mbps

NO.	PARAMETER		MIN	MAX	UNIT
RGMII5	$t_{su(RXD-RXC)}$	Setup time, receive selected signals valid before RGMII_RXC high and low	1		ns
RGMII6	$t_{h(RXC-RXD)}$	Hold time, receive selected signals valid after RGMII_RXC high and low	1		ns



A. RGMII_RXC must be externally delayed relative to the data and control pins.

B. Data and control information is received using both edges of the clocks. RGMII_RXD[3:0] carries data bits 3-0 on the rising edge of RGMII_RXC and data bits 7-4 on the falling edge of RGMII_RXC. Similarly, RGMII_RXCTL carries RXDV on rising edge of RGMII_RXC and RXERR on falling edge of RGMII_RXC.

Figure 5-32. EMAC Receive Interface Timing, RGMII operation

Table 5-38, Table 5-39, and Figure 5-34 present switching characteristics for transmit - RGMII for 10 Mbps, 100 Mbps, and 1000 Mbps.

Table 5-38. Switching Characteristics Over Recommended Operating Conditions for Transmit - RGMII

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Table 5-38. Switching Characteristics Over Recommended Operating Conditions for Transmit - RGMII operation for 10 Mbps, 100 Mbps, and 1000 Mbps (continued)

operation for 10 Mbps, 100 Mbps, and 1000 Mbps

NO.	PARAMETER		SPEED	MIN	MAX	UNIT
RGMII1	$t_{c(TXC)}$	Cycle time, RGMII_TXC	10 Mbps	360	440	ns
			100 Mbps	36	44	ns
			1000 Mbps	7.2	8.8	ns
RGMII2	$t_{w(TXCH)}$	Pulse duration, RGMII_TXC high	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns
RGMII3	$t_{w(TXCL)}$	Pulse duration, RGMII_TXC low	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns
RGMII4	$t_{t(TXC)}$	Transition time, RGMII_TXC	10 Mbps		0.75	ns
			100 Mbps		0.75	ns
			1000 Mbps		0.75	ns

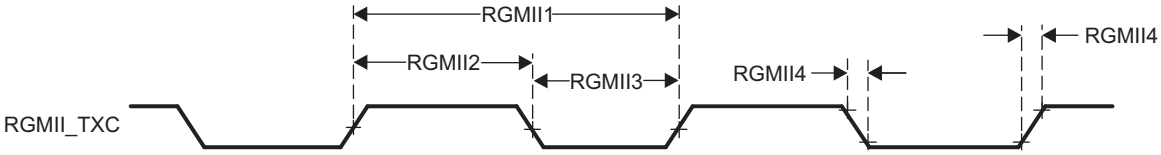
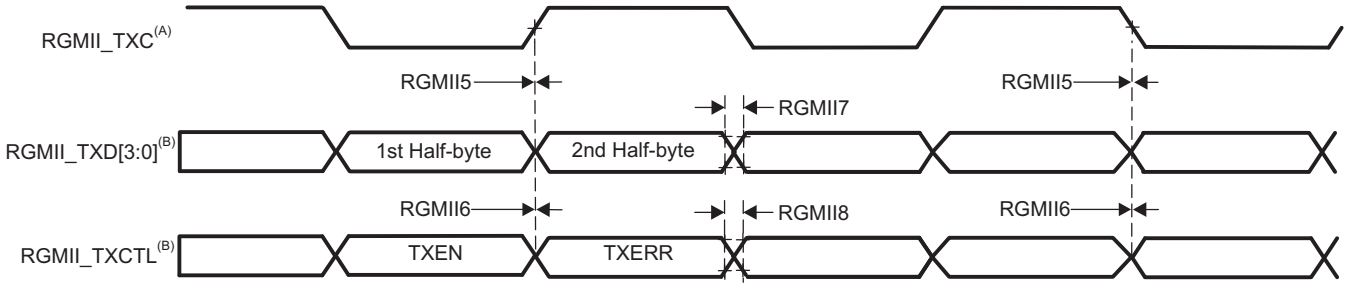


Figure 5-33. RGMII_TCX Timing - RGMII Mode

Table 5-39. Switching Characteristics Over Recommended Operating Conditions for EMAC RGMII Transmit - RGMII_TXD[3:0], and RGMII_TXCTL - RGMII Mode (1)

NO.	PARAMETER		MIN	MAX	UNIT
RGMII5	$t_{d(TXD-TXC)}$	Delay time, TXD to TXC	-0.35	0.65	ns
RGMII6	$t_{d(TXCTL-TXC)}$	Delay time, TXCTL to TXC	-0.35	0.65	ns
RGMII7	$t_{t(TXD)}$	Transition time, TXD		0.75	ns
RGMII8	$t_{t(TXCTL)}$	Transition time, TXCTL		0.75	ns

(1) PCB traces for RGMII_TXD[3:0] and RGMII_TXCTL should insert an additional 150ps of delay relative to the PCB trace delay of RGMII_TXC. This provides the expected output timing as defined by the RGMII specification for a transmitter not operating in RGMII-ID timing mode. Timing analysis should be performed on this interface using actual timing requirements/characteristics of the attached RGMII PHY. In some cases, additional PCB delays may be required to provide proper timing margins.



A. RGMII_TXC must be externally delayed relative to the data and control pins.

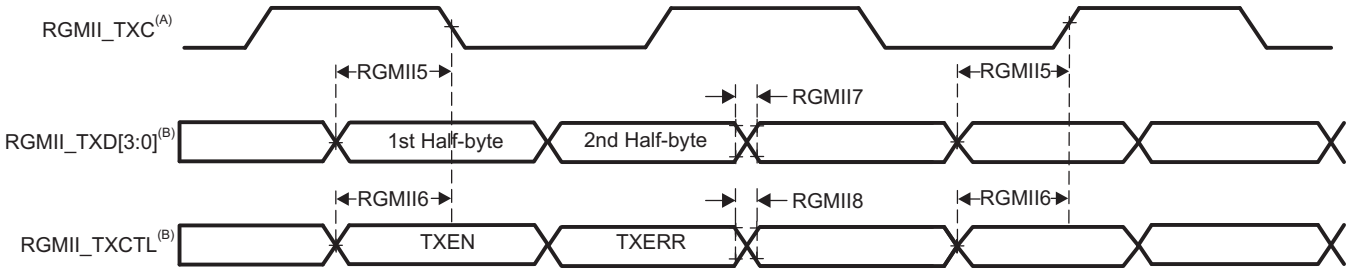
B. Data and control information is received using both edges of the clocks. RGMII_TXD[3:0] carries data bits 3-0 on the rising edge of RGMII_TXC and data bits 7-4 on the falling edge of RGMII_TXC. Similarly, RGMII_TXCTL carries TXDV on rising edge of RGMII_TXC and RTXERR on falling edge of RGMII_TXC.

Figure 5-34. EMAC Transmit Interface Timing RGMII Mode

Table 5-40. Switching Characteristics Over Recommended Operating Conditions for EMAC RGMII Transmit - RGMII_TXD[3:0], and RGMII_TXCTL - RGMII ID Mode(1)

NO.	PARAMETER		MIN	MAX	UNIT
RGMII5	$t_{d(TXD-TXC)}$	Delay time, TXD to TXC	$(0.25 \times t_{c(TXC)}) - 0.24$	$(0.25 \times t_{c(TXC)}) + 0.60$	ns
RGMII6	$t_{d(TXCTL-TXC)}$	Delay time, TXCTL to TXC	$(0.25 \times t_{c(TXC)}) - 0.24$	$(0.25 \times t_{c(TXC)}) + 0.60$	ns
RGMII7	$t_{t(TXD)}$	Transition time, TXD		0.75	
RGMII8	$t_{t(TXCTL)}$	Transition time, TXCTL		0.75	

(1) PCB traces for RGMII_TXD[3:0] and RGMII_TXCTL should insert an additional 150ps of delay relative to the PCB trace delay of RGMII_TXC. This provides the expected output timing as defined by the RGMII specification for a transmitter operating in RGMII-ID timing mode. Timing analysis should be performed on this interface using actual timing requirements/characteristics of the attached RGMII PHY. In some cases, additional PCB delays may be required to provide proper timing margins.



A. RGMII_TXC must be externally delayed relative to the data and control pins.

B. Data and control information is received using both edges of the clocks. RGMII_TXD[3:0] carries data bits 3-0 on the rising edge of RGMII_TXC and data bits 7-4 on the falling edge of RGMII_TXC. Similarly, RGMII_TXCTL carries TXDV on rising edge of RGMII_TXC and RTXERR on falling edge of RGMII_TXC.

Figure 5-35. EMAC Transmit Interface Timing - RGMII ID Mode

For more information, see section *Networking Subsystem (NSS)* in chapter *Peripherals* of the Device TRM.

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5.9.4.5 GPMC

For more details about features and additional description information on the device General-Purpose Memory Controller, see the corresponding sections within Section 4.3, *Signal Descriptions* and Section 6, *Detailed Description*.

5.9.4.5.1 GPMC and NOR Flash—Synchronous Mode

Table 5-42 and Table 5-43 assume testing over the recommended operating conditions and electrical characteristic conditions shown in Table 5-41 (see Figure 5-36 through Figure 5-40).

Table 5-41. GPMC and NOR Flash Timing Conditions—Synchronous Mode

PARAMETER		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input signal rise time	0.9		3.1(1)	ns
t_F	Input signal fall time	0.9		3.1(1)	ns
Output Condition					
C_{LOAD}	Output load capacitance	5		20	pF

(1) Max t_R & t_F = 25% of clock period when GPMC_CLK = 79.78 MHz.

Table 5-42. GPMC and NOR Flash Timing Requirements—Synchronous Mode

NO.			MIN	MAX	UNIT
F12	$t_{su(dV-clkH)}$	Setup time, input data GPMC_AD[15:0] valid before output clock GPMC_CLK high	3.5		ns
F13	$t_{h(clkH-dV)}$	Hold time, input data GPMC_AD[15:0] valid after output clock GPMC_CLK high	2.5		ns
F21	$t_{su(waitV-clkH)}$	Setup time, input wait GPMC_WAIT[x](1) valid before output clock GPMC_CLK high	3.5		ns
F22	$t_{h(clkH-waitV)}$	Hold time, input wait GPMC_WAIT[x](1) valid after output clock GPMC_CLK high	2.5		ns

(1) In GPMC_WAIT[x], x is equal to 0 or 1.

Table 5-43. GPMC and NOR Flash Switching Characteristics—Synchronous Mode(2)

NO.	PARAMETER		MIN	MAX	UNIT
F0	$1 / t_{c(clk)}$	Frequency(18), output clock GPMC_CLK		100	MHz
F1	$t_{w(clkH)}$	Typical pulse duration, output clock GPMC_CLK high	0.5P(15)	0.5P(15)	ns
F1	$t_{w(clkL)}$	Typical pulse duration, output clock GPMC_CLK low	0.5P(15)	0.5P(15)	ns
	$t_{dc(clk)}$	Duty cycle error, output clock GPMC_CLK	-500	500	ps
	$t_{J(clk)}$	Jitter standard deviation(19), output clock GPMC_CLK		33.33	ps
	$t_{R(clk)}$	Rise time, output clock GPMC_CLK		2	ns
	$t_{F(clk)}$	Fall time, output clock GPMC_CLK		2	ns
	$t_{R(do)}$	Rise time, output data GPMC_AD[15:0]		2	ns
	$t_{F(do)}$	Fall time, output data GPMC_AD[15:0]		2	ns
F2	$t_{d(clkH-csnV)}$	Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CSn[x](14) transition	F(6) - 2.2	F(6) + 4.5	ns
F3	$t_{d(clkH-csnIV)}$	Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CSn[x](14) invalid	E(5) - 2.2	E(5) + 4.5	ns
F4	$t_{d(aV-clk)}$	Delay time, output address GPMC_A[27:1] valid to output clock GPMC_CLK first edge	B(2) - 4.5	B(2) + 3.1	ns
F5	$t_{d(clkH-aIV)}$	Delay time, output clock GPMC_CLK rising edge to output address GPMC_A[27:1] invalid	-2.3	4.5	ns
F6	$t_{d(be[x]nV-clk)}$	Delay time, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n valid to output clock GPMC_CLK first edge	B(2) - 1.9	B(2) + 2.3	ns

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Table 5-43. GPMC and NOR Flash Switching Characteristics—Synchronous Mode[2] (continued)

NO.	PARAMETER			MIN	MAX	UNIT
F7	$t_{d(clkH-be[x]nIV)}$	Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n invalid[11]		D[4] - 2.3	D[4] + 1.9	ns
F7	$t_{d(clkL-be[x]nIV)}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid[12]		D[4] - 2.3	D[4] + 1.9	ns
F7	$t_{d(clkL-be[x]nIV)}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid[13]		D[4] - 2.3	D[4] + 1.9	ns
F8	$t_{d(clkH-advn)}$	Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE transition		G[7] - 2.3	G[7] + 4.5	ns
F9	$t_{d(clkH-advnIV)}$	Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE invalid		D[4] - 2.3	D[4] + 4.5	ns
F10	$t_{d(clkH-oen)}$	Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn transition		H[8] - 2.3	H[8] + 3.5	ns
F11	$t_{d(clkH-oenIV)}$	Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn invalid		H[8] - 2.3	H[8] + 3.5	ns
F14	$t_{d(clkH-wen)}$	Delay time, output clock GPMC_CLK rising edge to output write enable GPMC_WEn transition		I[9] - 2.3	I[9] + 4.5	ns
F15	$t_{d(clkH-do)}$	Delay time, output clock GPMC_CLK rising edge to output data GPMC_AD[15:0] transition[11]		J[10] - 2.3	J[10] + 2.7	ns
F15	$t_{d(clkL-do)}$	Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition[12]		J[10] - 2.3	J[10] + 2.7	ns
F15	$t_{d(clkL-do)}$	Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition[13]		J[10] - 2.3	J[10] + 2.7	ns
F17	$t_{d(clkH-be[x]n)}$	Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE transition[11]		J[10] - 2.3	J[10] + 1.9	ns
F17	$t_{d(clkL-be[x]n)}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition[12]		J[10] - 2.3	J[10] + 1.9	ns
F17	$t_{d(clkL-be[x]n)}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition[13]		J[10] - 2.3	J[10] + 1.9	ns
F18	$t_{w(csnV)}$	Pulse duration, output chip select GPMC_CSn[x][14] low	Read	A[1]		ns
			Write	A[1]		ns
F19	$t_{w(be[x]nV)}$	Pulse duration, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n low	Read	C[3]		ns
			Write	C[3]		ns
F20	$t_{w(advnV)}$	Pulse duration, output address valid and address latch enable GPMC_ADVn_ALE low	Read	K[16]		ns
			Write	K[16]		ns

(1) For single read: A = (CSRdOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
With n being the page burst access number.

(2) B = ClkActivationTime × GPMC_FCLK[17]

(3) For single read: C = RdCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK[17]
For burst read: C = (RdCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
For burst write: C = (WrCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
With n being the page burst access number.

(4) For single read: D = (RdCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
For burst read: D = (RdCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
For burst write: D = (WrCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]

(5) For single read: E = (CSRdOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
For burst read: E = (CSRdOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
For burst write: E = (CSWrOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]

(6) For csn falling edge (CS activated):
- Case GpmcFCLKDivider = 0:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK[17]
- Case GpmcFCLKDivider = 1:

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  - F = 0.5 × CSExtraDelay × GPMC_FCLK(17) if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
  - F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK(17) otherwise
- Case GpmcFCLKDivider = 2:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK(17) if ((CSOnTime - ClkActivationTime) is a multiple of 3)
  - F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK(17) if ((CSOnTime - ClkActivationTime - 1) is a multiple of 3)
  - F = (2 + 0.5 × CSExtraDelay) × GPMC_FCLK(17) if ((CSOnTime - ClkActivationTime - 2) is a multiple of 3)

(7) For ADV falling edge (ADV activated):

- Case GpmcFCLKDivider = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(17)
- Case GpmcFCLKDivider = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(17) if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(17) otherwise
- Case GpmcFCLKDivider = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(17) if ((ADVOnTime - ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(17) if ((ADVOnTime - ClkActivationTime - 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(17) if ((ADVOnTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:

- Case GpmcFCLKDivider = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(17)
- Case GpmcFCLKDivider = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(17) if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(17) otherwise
- Case GpmcFCLKDivider = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(17) if ((ADVRdOffTime - ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(17) if ((ADVRdOffTime - ClkActivationTime - 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(17) if ((ADVRdOffTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:

- Case GpmcFCLKDivider = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(17)
- Case GpmcFCLKDivider = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(17) if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(17) otherwise
- Case GpmcFCLKDivider = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(17) if ((ADVWrOffTime - ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(17) if ((ADVWrOffTime - ClkActivationTime - 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(17) if ((ADVWrOffTime - ClkActivationTime - 2) is a multiple of 3)

(8) For OE falling edge (OE activated) and IO DIR rising edge (Data Bus input direction):

- Case GpmcFCLKDivider = 0:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(17)
- Case GpmcFCLKDivider = 1:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(17) if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(17) otherwise
- Case GpmcFCLKDivider = 2:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(17) if ((OEOnTime - ClkActivationTime) is a multiple of 3)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(17) if ((OEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK(17) if ((OEOnTime - ClkActivationTime - 2) is a multiple of 3)

For OE rising edge (OE deactivated):

- Case GpmcFCLKDivider = 0:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(17)
- Case GpmcFCLKDivider = 1:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(17) if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(17) otherwise
- Case GpmcFCLKDivider = 2:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(17) if ((OEOffTime - ClkActivationTime) is a multiple of 3)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(17) if ((OEOffTime - ClkActivationTime - 1) is a multiple of 3)
  - H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK(17) if ((OEOffTime - ClkActivationTime - 2) is a multiple of 3)

(9) For WE falling edge (WE activated):

- Case GpmcFCLKDivider = 0:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(17)
- Case GpmcFCLKDivider = 1:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(17) if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)

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  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK[17] otherwise
- Case GpmcFCLKDivider = 2:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK[17] if ((WEOnTime - ClkActivationTime) is a multiple of 3)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK[17] if ((WEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK[17] if ((WEOnTime - ClkActivationTime - 2) is a multiple of 3)

For WE rising edge (WE deactivated):
- Case GpmcFCLKDivider = 0:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK [17]
- Case GpmcFCLKDivider = 1:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK[17] if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK[17] otherwise
- Case GpmcFCLKDivider = 2:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK[17] if ((WEOffTime - ClkActivationTime) is a multiple of 3)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK[17] if ((WEOffTime - ClkActivationTime - 1) is a multiple of 3)
  - I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK[17] if ((WEOffTime - ClkActivationTime - 2) is a multiple of 3)

(10) J = GPMC_FCLK[17]

(11) First transfer only for CLK DIV 1 mode.

(12) Half cycle; for all data after initial transfer for CLK DIV 1 mode.

(13) Half cycle of GPMC_CLK_OUT; for all data for modes other than CLK DIV 1 mode. GPMC_CLK_OUT divide down from GPMC_FCLK.

(14) In GPMC_CSn[x], x is equal to 0, 1, 2 or 3. In GPMC_WAIT[x], x is equal to 0 or 1.

(15) P = GPMC_CLK period in ns

(16) For read: K = (ADVRdOffTime - ADVOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
For write: K = (ADVWrOffTime - ADVOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]

(17) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.

(18) Related to the GPMC_CLK output clock maximum and minimum frequencies programmable in the GPMC module by setting the GPMC_CONFIG1_CSx configuration register bit field GpmcFCLKDivider.

(19) The jitter probability density can be approximated by a Gaussian function.

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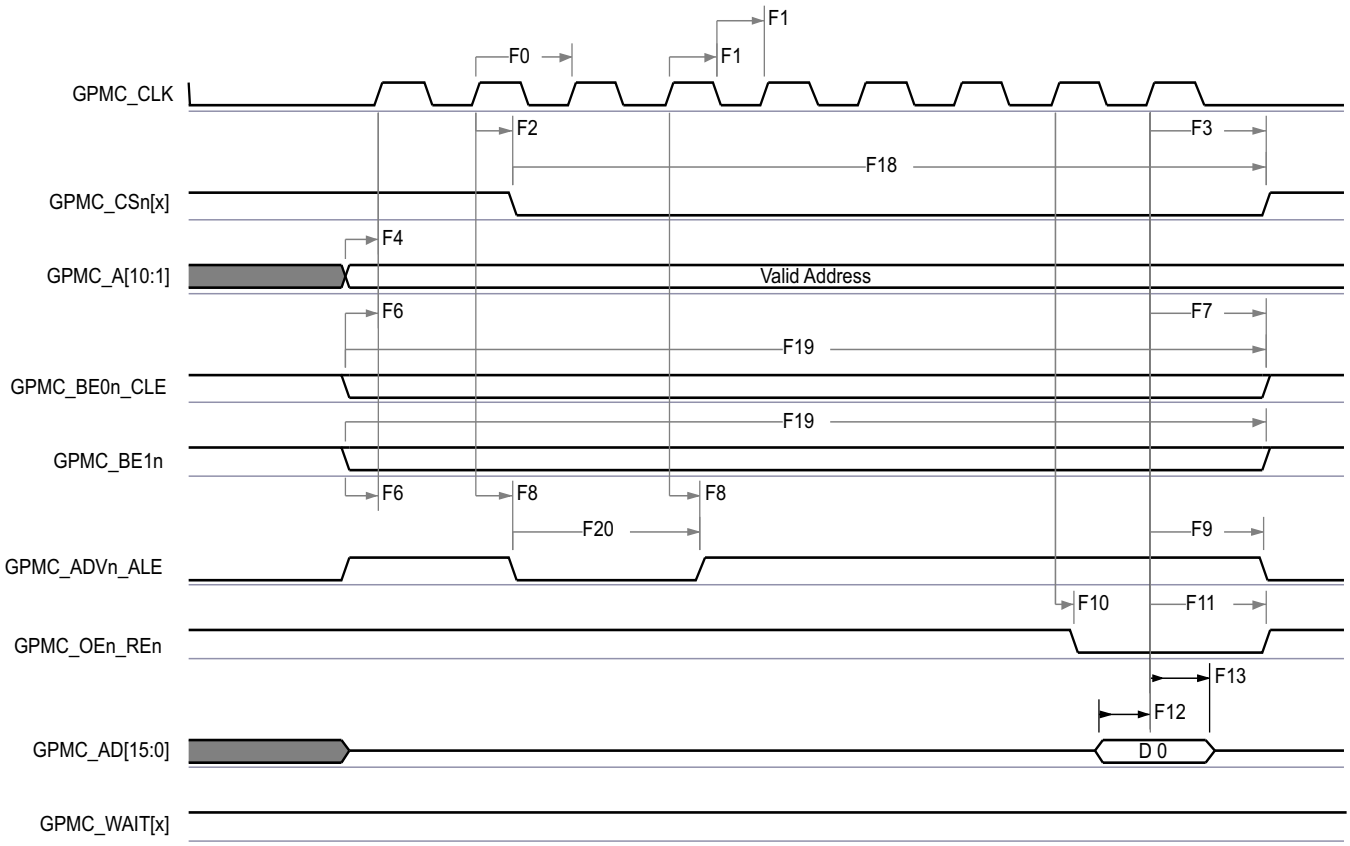
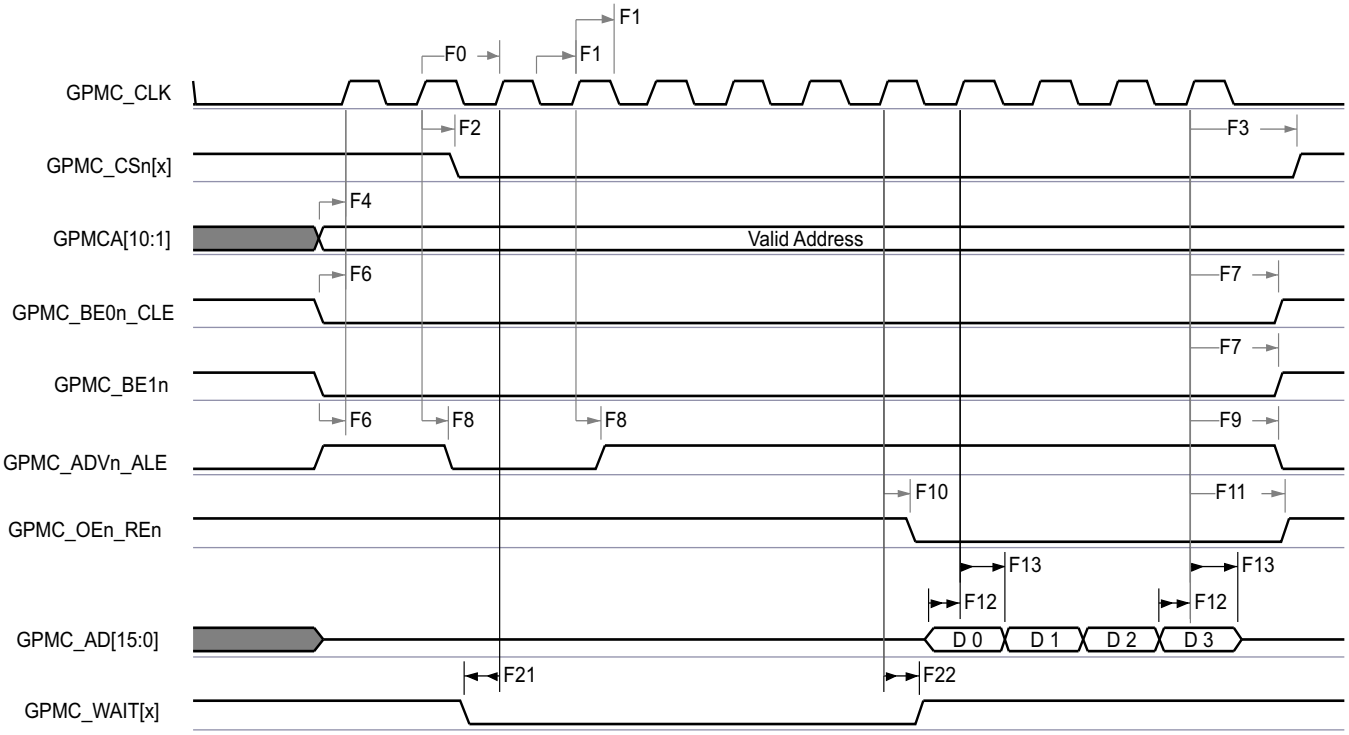


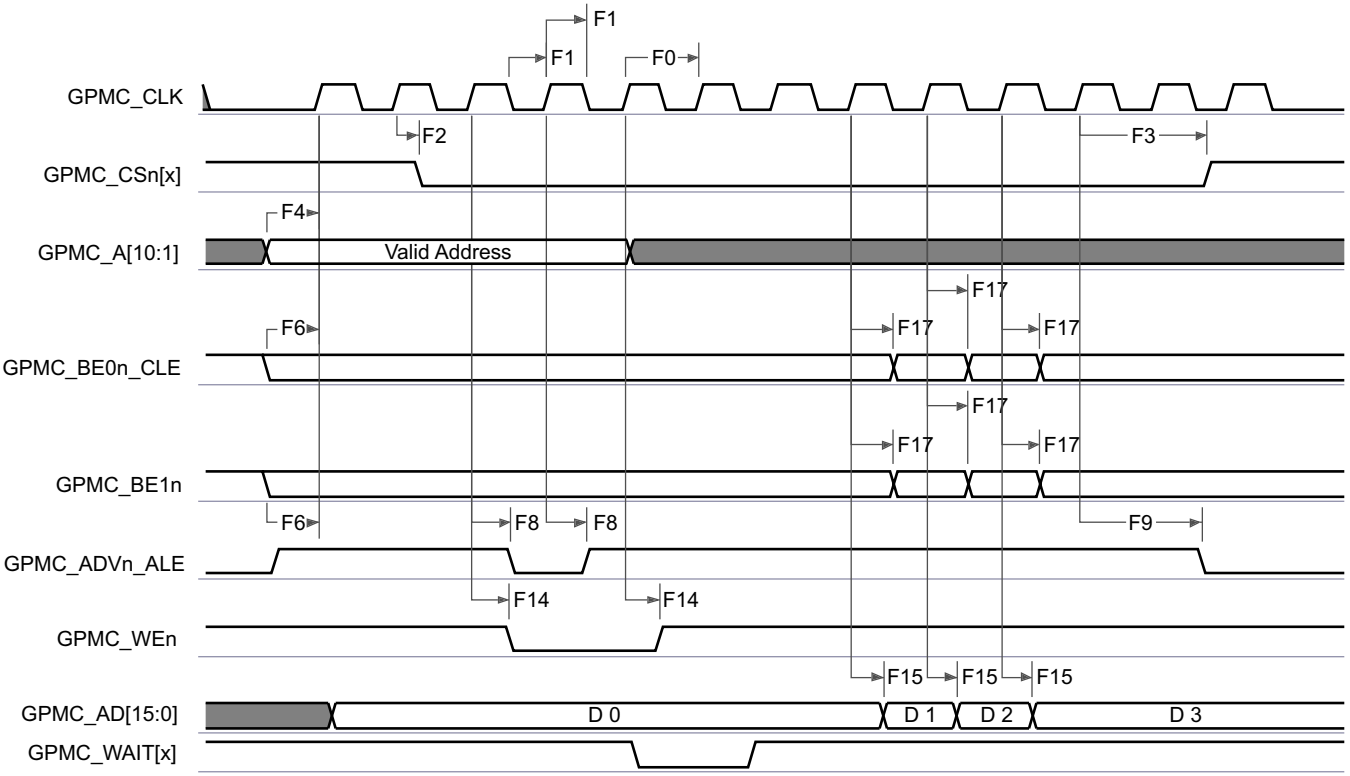
A. In GPMC_CSn[x], x is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[x], x is equal to 0 or 1.

Figure 5-36. GPMC and NOR Flash—Synchronous Single Read—(GpmcFCLKDivider = 0)



A. In GPMC_CSn[x], x is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[x], x is equal to 0 or 1.

Figure 5-37. GPMC and NOR Flash—Synchronous Burst Read—4x16-bit (GpmcFCLKDivider = 0)



A. In GPMC_CSn[x], x is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[x], x is equal to 0 or 1.

Figure 5-38. GPMC and NOR Flash—Synchronous Burst Write—(GpmcFCLKDivider > 0)

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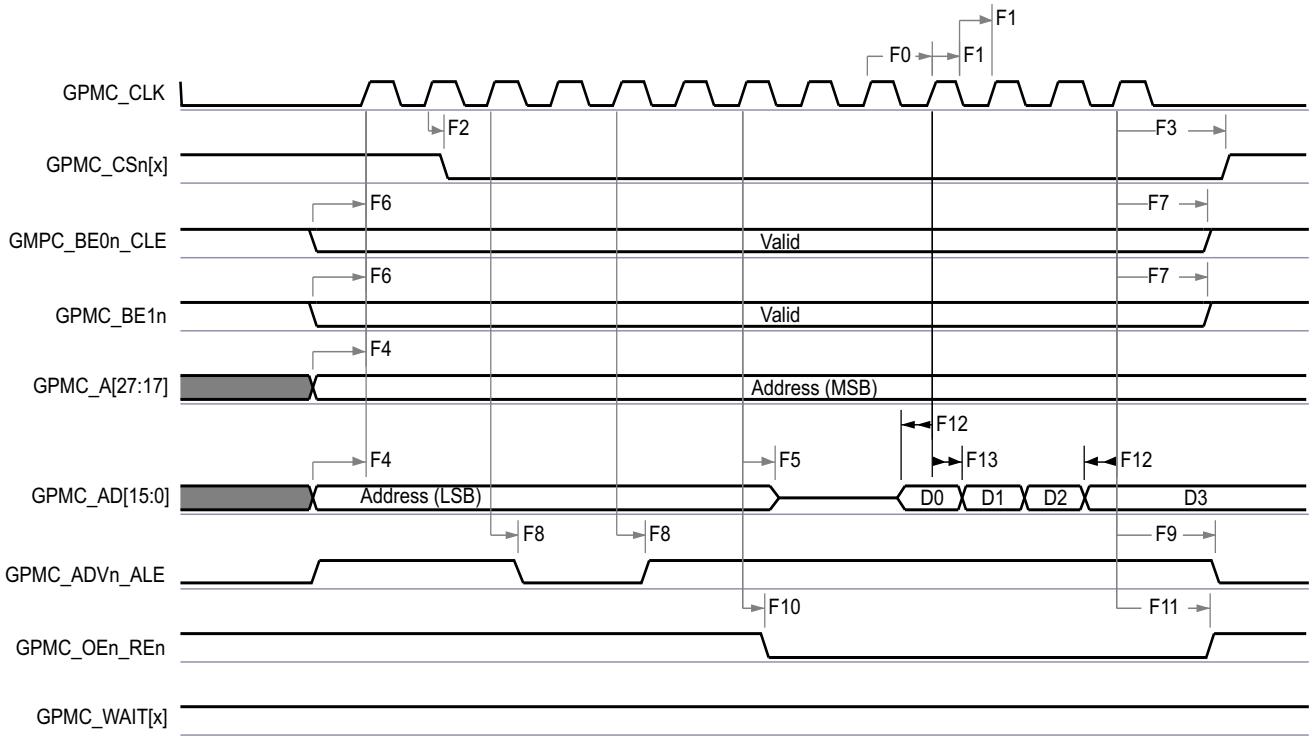
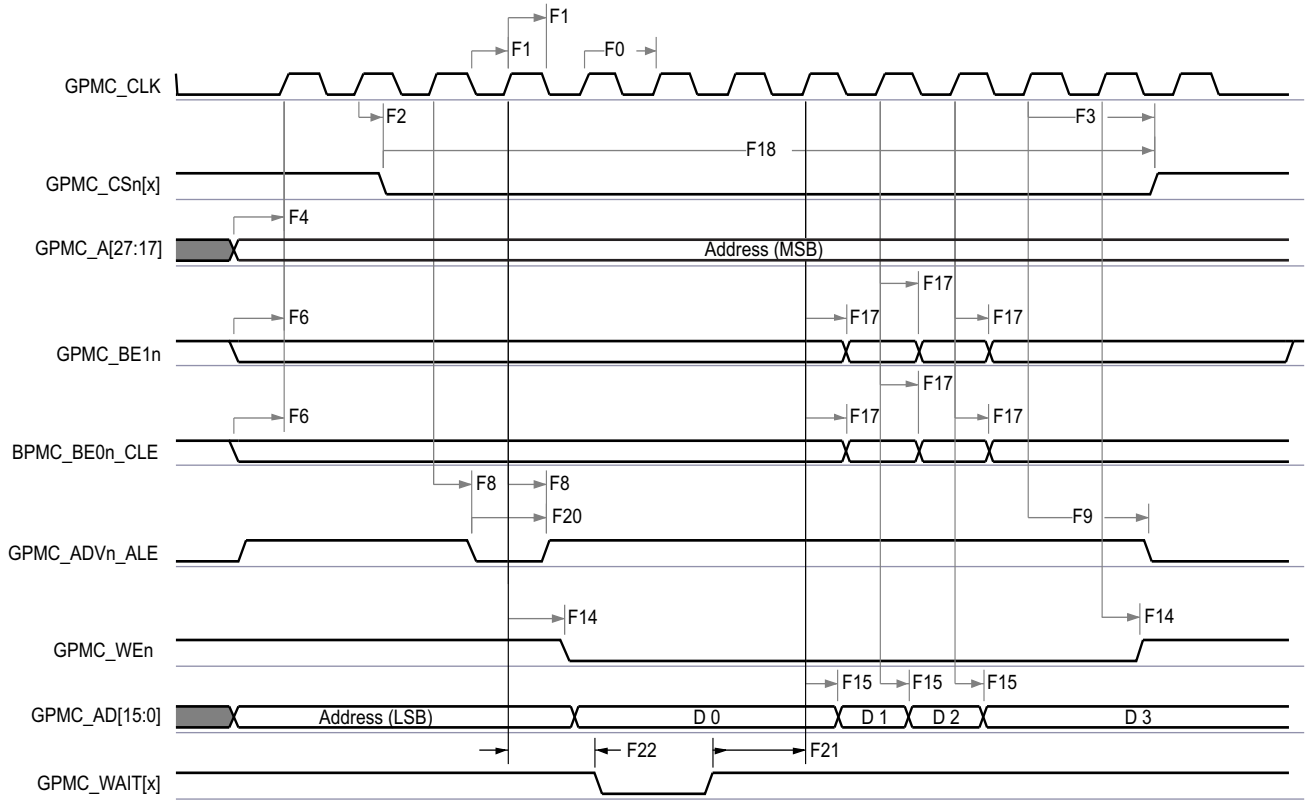


A. In GPMC_CSn[x], x is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[x], x is equal to 0 or 1.

Figure 5-39. GPMC and Multiplexed NOR Flash—Synchronous Burst Read



A. In GPMC_CSn[x], x is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[x], x is equal to 0 or 1.

Figure 5-40. GPMC and Multiplexed NOR Flash—Synchronous Burst Write

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5.9.4.5.2 GPMC and NOR Flash—Asynchronous Mode

Table 5-44 and Table 5-45 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 5-41 through Figure 5-46).

Table 5-44. GPMC and NOR Flash Internal Timing Parameters—Asynchronous Mode[1][2]

NO.		MIN	MAX	UNIT
FI1	Delay time, output data GPMC_AD[15:0] generation from internal functional clock GPMC_FCLK[3]		6.5	ns
FI2	Delay time, input data GPMC_AD[15:0] capture from internal functional clock GPMC_FCLK[3]		4	ns
FI3	Delay time, output chip select GPMC_CSn[x] generation from internal functional clock GPMC_FCLK[3]		6.5	ns
FI4	Delay time, output address GPMC_A[27:1] generation from internal functional clock GPMC_FCLK[3]		6.5	ns
FI5	Delay time, output address GPMC_A[27:1] valid from internal functional clock GPMC_FCLK[3]		6.5	ns
FI6	Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n generation from internal functional clock GPMC_FCLK[3]		6.5	ns
FI7	Delay time, output enable GPMC_OEn_REn generation from internal functional clock GPMC_FCLK[3]		6.5	ns
FI8	Delay time, output write enable GPMC_WEn generation from internal functional clock GPMC_FCLK[3]		6.5	ns
FI9	Skew, internal functional clock GPMC_FCLK[3]		100	ps

(1) The internal parameters table must be used to calculate data access time stored in the corresponding CS register bit field.

(2) Internal parameters are referred to the GPMC functional internal clock which is not provided externally.

(3) GPMC_FCLK is general-purpose memory controller internal functional clock.

Table 5-45. GPMC and NOR Flash Timing Requirements—Asynchronous Mode

NO.			MIN	MAX	UNIT
FA5[1]	$t_{acc(d)}$	Data access time		H[5]	ns
FA20[2]	$t_{acc1\text{-}pgmode(d)}$	Page mode successive data access time		P[4]	ns
FA21[3]	$t_{acc2\text{-}pgmode(d)}$	Page mode first data access time		H[5]	ns

(1) The FA5 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.

(2) The FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.

(3) The FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data is internally sampled by active functional clock edge. FA21 value must be stored inside the AccessTime register bit field.

(4) P = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC_FCLK[6]

(5) H = AccessTime × (TimeParaGranularity + 1) × GPMC_FCLK[6]

(6) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.

Table 5-46. GPMC and NOR Flash Switching Characteristics—Asynchronous Mode

NO.	PARAMETER			MIN	MAX	UNIT
	$t_{R(d)}$	Rise time, output data GPMC_AD[15:0]			2	ns
	$t_{F(d)}$	Fall time, output data GPMC_AD[15:0]			2	ns
FA0	$t_{w(be[x]nV)}$	Pulse duration, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid time	Read		N[12]	ns
			Write		N[12]	
FA1	$t_{w(csnV)}$	Pulse duration, output chip select GPMC_CSn[x][13] low	Read		A[1]	ns
			Write		A[1]	

Table 5-46. GPMC and NOR Flash Switching Characteristics—Asynchronous Mode (continued)

NO.	PARAMETER			MIN	MAX	UNIT
FA3	$t_{d(csnV-advnIV)}$	Delay time, output chip select GPMC_CSn[x](13) valid to output address valid and address latch enable GPMC_ADVn_ALE invalid	Read	B(2) - 0.2	B(2) + 2.0	ns
			Write	B(2) - 0.2	B(2) + 2.0	
FA4	$t_{d(csnV-oenIV)}$	Delay time, output chip select GPMC_CSn[x](13) valid to output enable GPMC_OEn_REn invalid (Single read)		C(3) - 0.2	C(3) + 2.0	ns
FA9	$t_{d(aV-csnV)}$	Delay time, output address GPMC_A[27:1] valid to output chip select GPMC_CSn[x](13) valid		J(9) - 0.2	J(9) + 2.0	ns
FA10	$t_{d(be[x]nV-csnV)}$	Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid to output chip select GPMC_CSn[x](13) valid		J(9) - 0.2	J(9) + 2.0	ns
FA12	$t_{d(csnV-advnV)}$	Delay time, output chip select GPMC_CSn[x](13) valid to output address valid and address latch enable GPMC_ADVn_ALE valid		K(10) - 0.2	K(10) + 2.0	ns
FA13	$t_{d(csnV-oenV)}$	Delay time, output chip select GPMC_CSn[x](13) valid to output enable GPMC_OEn_REn valid		L(11) - 0.2	L(11) + 2.0	ns
FA16	$t_{w(aIV)}$	Pulse durationm output address GPMC_A[26:1] invalid between 2 successive read and write accesses		G(7)		ns
FA18	$t_{d(csnV-oenIV)}$	Delay time, output chip select GPMC_CSn[x](13) valid to output enable GPMC_OEn_REn invalid (Burst read)		I(8) - 0.2	I(8) + 2.0	ns
FA20	$t_{w(aV)}$	Pulse duration, output address GPMC_A[27:1] valid - 2nd, 3rd, and 4th accesses		D(4)		ns
FA25	$t_{d(csnV-wenV)}$	Delay time, output chip select GPMC_CSn[x](13) valid to output write enable GPMC_WEn valid		E(5) - 0.2	E(5) + 2.0	ns
FA27	$t_{d(csnV-wenIV)}$	Delay time, output chip select GPMC_CSn[x](13) valid to output write enable GPMC_WEn invalid		F(6) - 0.2	F(6) + 2.0	ns
FA28	$t_{d(wenV-dV)}$	Delay time, output write enable GPMC_WEn valid to output data GPMC_AD[15:0] valid			2.8	ns
FA29	$t_{d(dV-csnV)}$	Delay time, output data GPMC_AD[15:0] valid to output chip select GPMC_CSn[x](13) valid		J(9) - 0.2	J(9) + 2.8	ns
FA37	$t_{d(oenV-aIV)}$	Delay time, output enable GPMC_OEn_REn valid to output address GPMC_AD[15:0] phase end			2.8	ns

(1) For single read: A = (CSRdOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For single write: A = (CSWrOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
with n being the page burst access number

(2) For reading: B = ((ADVRdOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)
For writing: B = ((ADVWrOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)

(3) C = ((OEOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)

(4) D = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC_FCLK(14)

(5) E = ((WEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)

(6) F = ((WEOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)

(7) G = Cycle2CycleDelay × GPMC_FCLK(14)

(8) I = ((OEOffTime + (n - 1) × PageBurstAccessTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)

(9) J = (CSOnTime × (TimeParaGranularity + 1) + 0.5 × CSExtraDelay) × GPMC_FCLK(14)

(10) K = ((ADVOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)

(11) L = ((OEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)

(12) For single read: N = RdCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For single write: N = WrCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst read: N = (RdCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst write: N = (WrCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)

(13) In GPMC_CSn[x], x is equal to 0, 1, 2 or 3.

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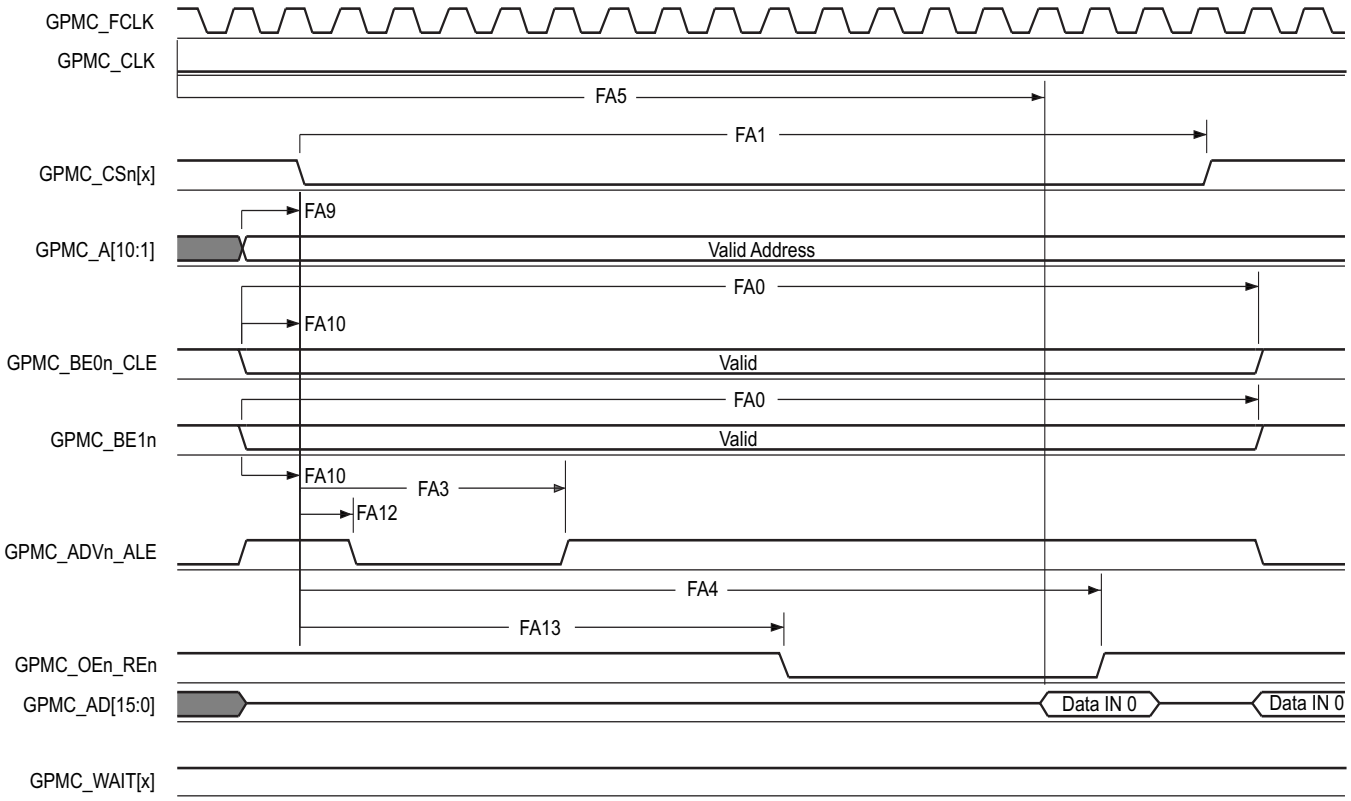
(14) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.



A. In GPMC_CSn[x], x is equal to 0, 1, 2 or 3. In GPMC_WAIT[x], x is equal to 0 or 1.

B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.

C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 5-41. GPMC and NOR Flash—Asynchronous Read—Single Word

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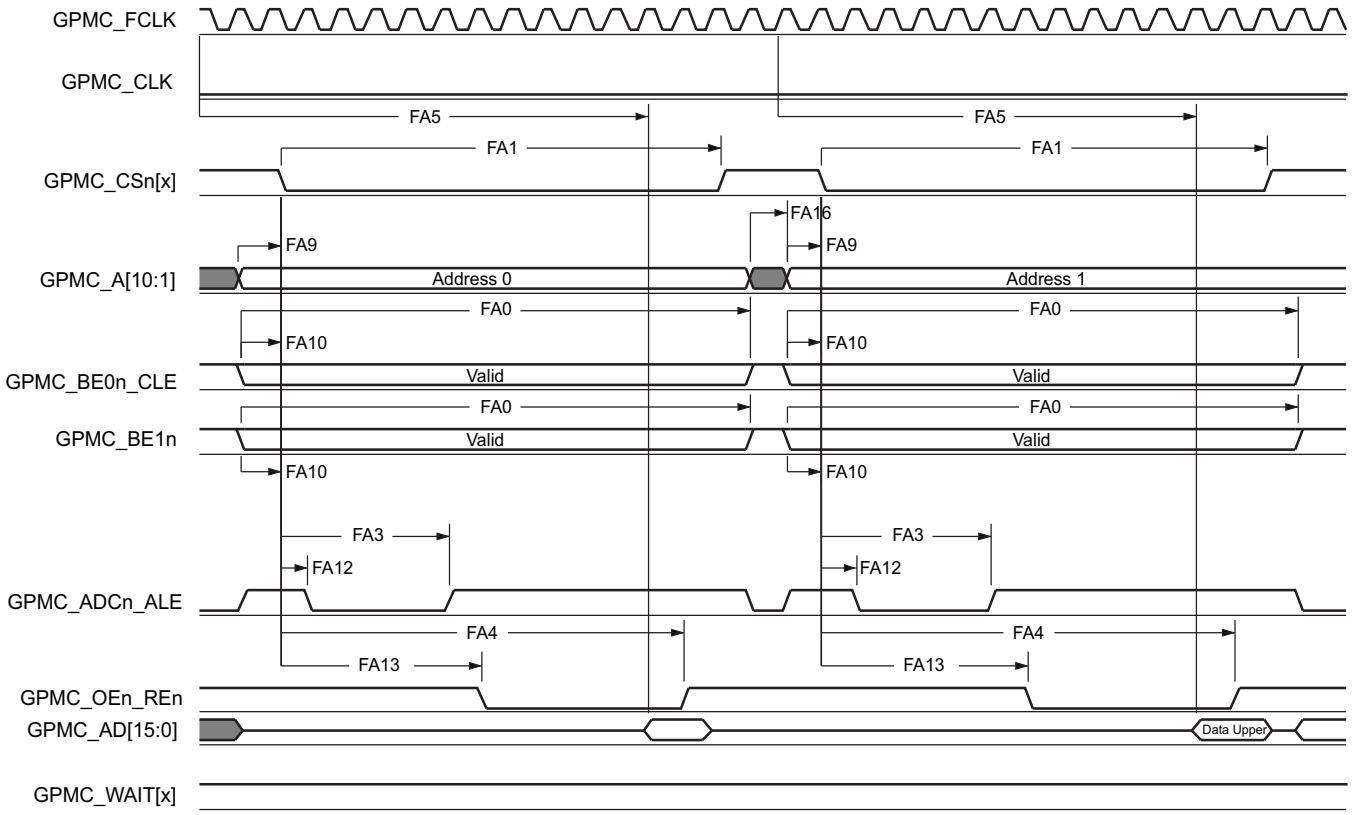

A. In GPMC_CSn[x], x is equal to 0, 1, 2 or 3. In GPMC_WAIT[x], x is equal to 0 or 1.

B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.

C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 5-42. GPMC and NOR Flash—Asynchronous Read—32-Bit

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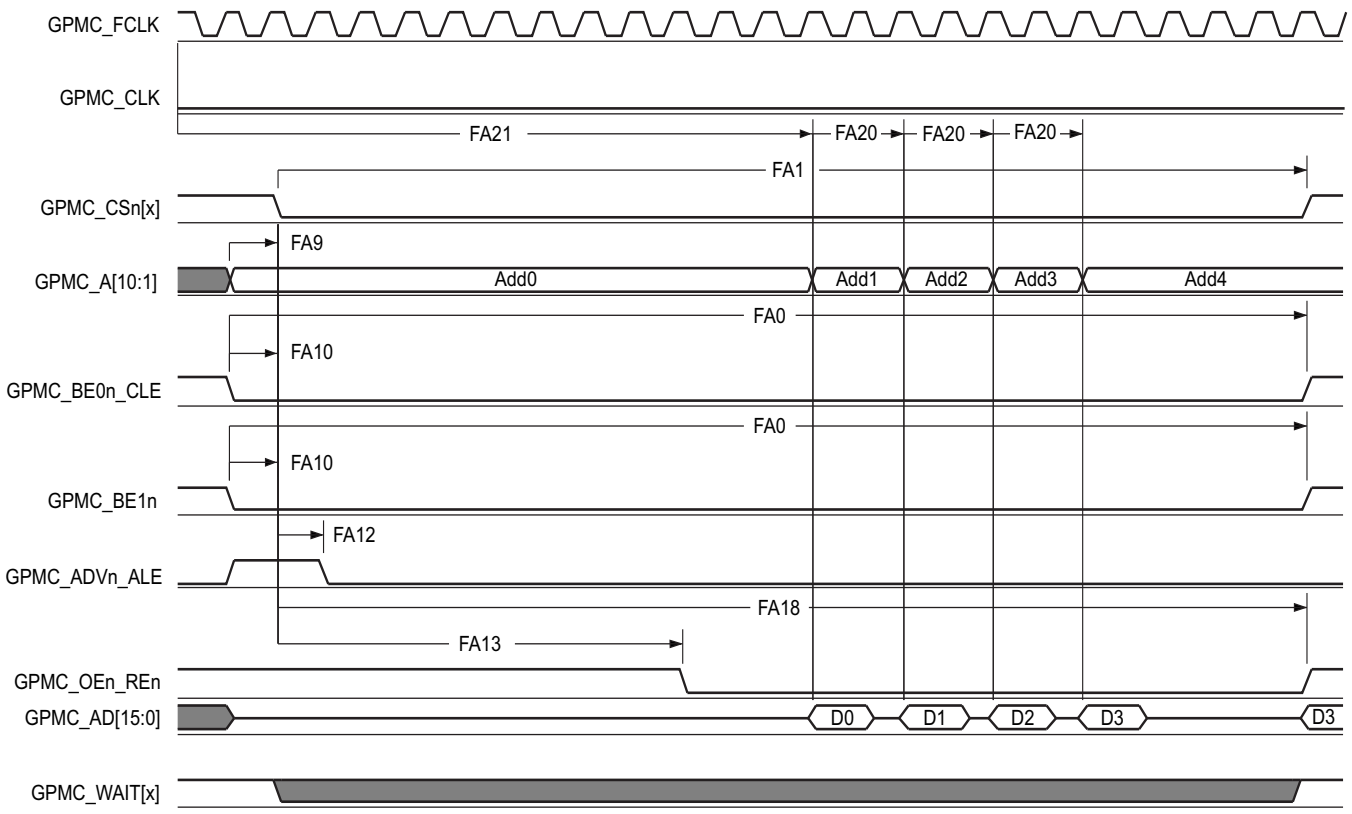

A. In GPMC_CSn[x], x is equal to 0, 1, 2 or 3. In GPMC_WAIT[x], x is equal to 0 or 1.

B. FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data will be internally sampled by active functional clock edge. FA21 calculation must be stored inside AccessTime register bits field.

C. FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bits field.

D. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 5-43. GPMC and NOR Flash—Asynchronous Read—Page Mode 4x16-Bit

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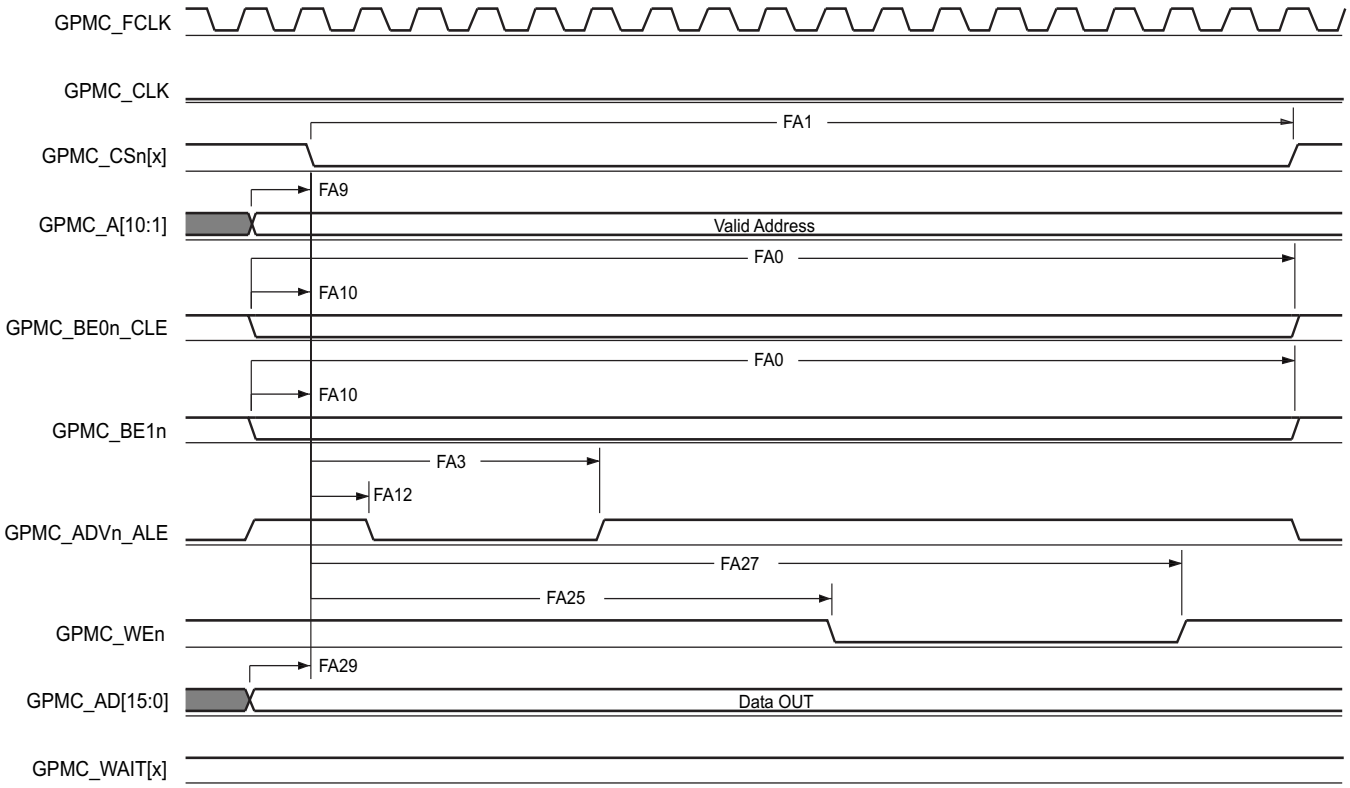

A. In GPMC_CSn[x], x is equal to 0, 1, 2 or 3. In GPMC_WAIT[x], x is equal to 0 or 1.

Figure 5-44. GPMC and NOR Flash—Asynchronous Write—Single Word

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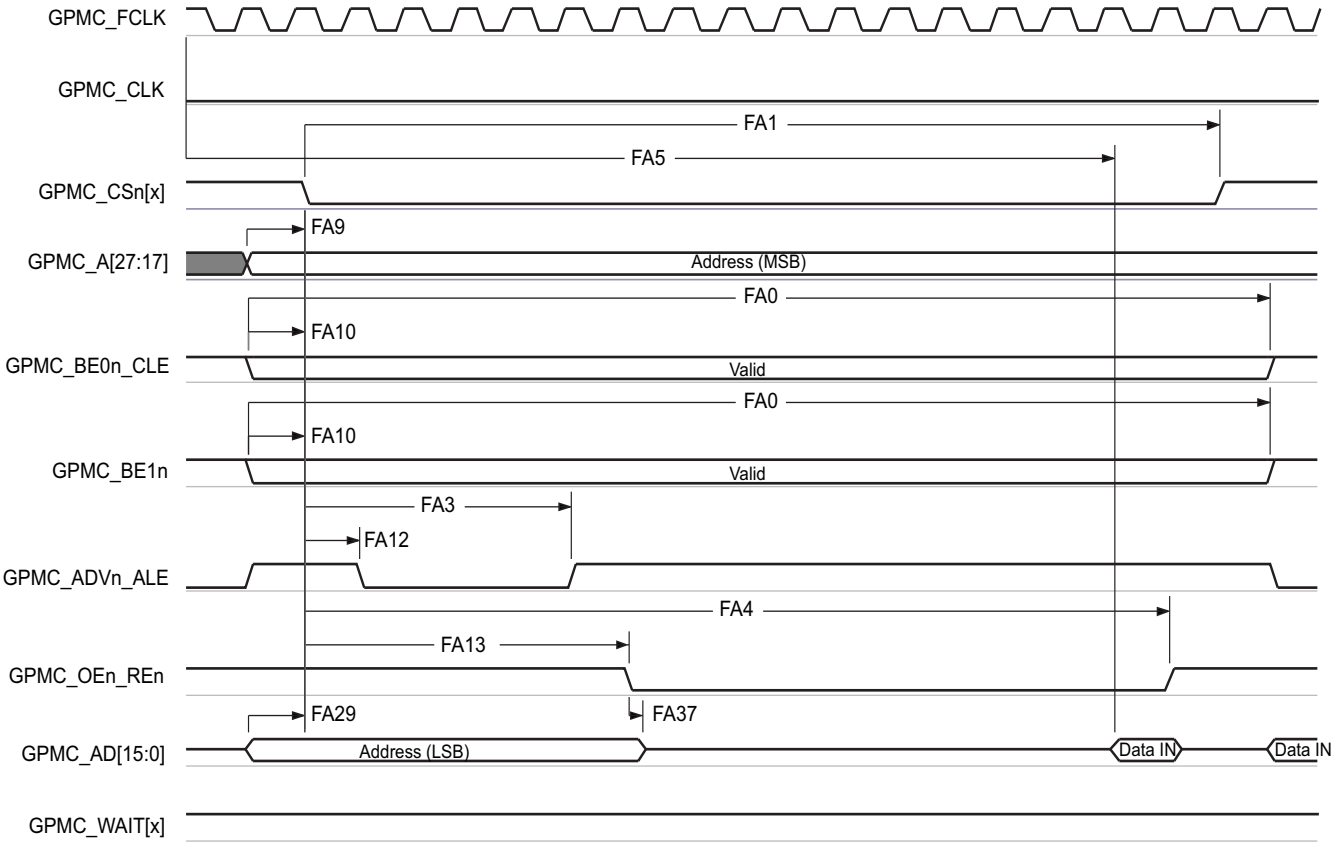
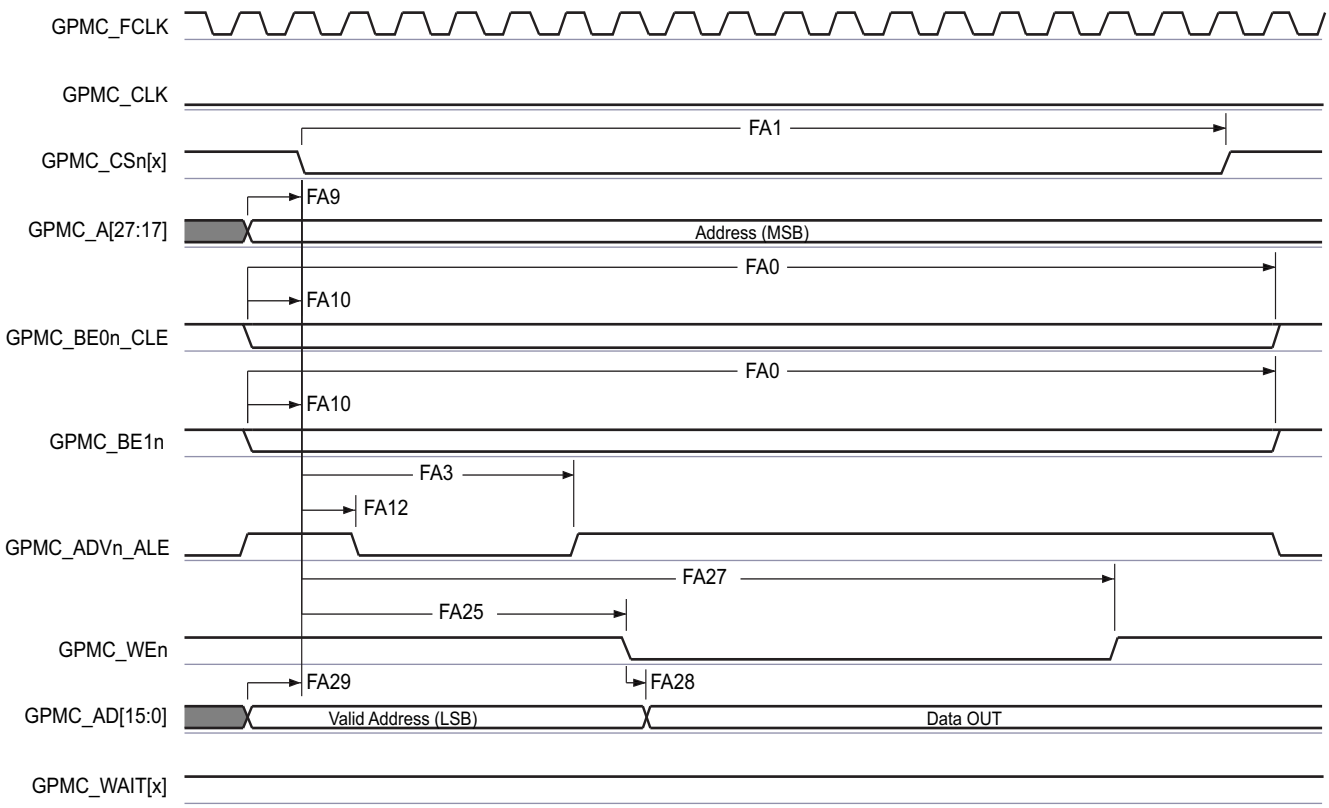


A. In GPMC_CSn[x], x is equal to 0, 1, 2 or 3. In GPMC_WAIT[x], x is equal to 0 or 1.

B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.

C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 5-45. GPMC and Multiplexed NOR Flash—Asynchronous Read—Single Word



A. In GPMC_CSn[x], x is equal to 0, 1, 2 or 3. In GPMC_WAIT[x], x is equal to 0 or 1.

Figure 5-46. GPMC and Multiplexed NOR Flash—Asynchronous Write—Single Word

For more information, see section *General-Purpose Memory Controller (GPMC)* in chapter *Memory Subsystem* of the Device TRM.

5.9.4.6 I2C

For more details about features and additional description information on the device Inter-Integrated Circuit, see the corresponding sections within Section 4.3, *Signal Descriptions* and Section 6, *Detailed Description*.

Table 5-47 and Figure 5-47 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-47. Timing Requirements for I2C Input Timings

NO.			STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
I1	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
I2	$t_{su(SCLH-SDAL)}$	Setup Time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
I3	$t_{h(SDAL-SCLL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
I4	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
I5	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
I6	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid before SCL high	250		100(1)		ns
I7	$t_{h(SCLL-SDAV)}$	Hold time, SDA valid after SCL low	0(2)	3.45(3)	0(2)	0.9(3)	µs
I8	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs

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Table 5-47. Timing Requirements for I2C Input Timings (continued)

NO.			STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
I9	$t_{r(SDA)}$	Rise time, SDA		1000	20 + 0.1Cb(4)	300	ns
I10	$t_{r(SCL)}$	Rise time, SCL		1000	20 + 0.1Cb(4)	300	ns
I11	$t_{f(SDA)}$	Fall time, SDA		300	20 + 0.1Cb(4)	300	ns
I12	$t_{f(SCL)}$	Fall time, SCL		300	20 + 0.1Cb(4)	300	ns
I13	$t_{su(SCLH-SDAH)}$	Setup time, high before SDA high (for STOP condition)	4		0.6		µs
I14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)	0	50	0	50	ns

(1) A fast-mode I2C-bus™ device can be used in a standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device stretches the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\ max} + t_{su(SDA-SCLH)} = 1000 + 250 = 1250$ ns (according to the standard-mode I2C-Bus Specification) before the SCL line is released.

(2) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

(3) The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.

(4) Cb is line load in pF.

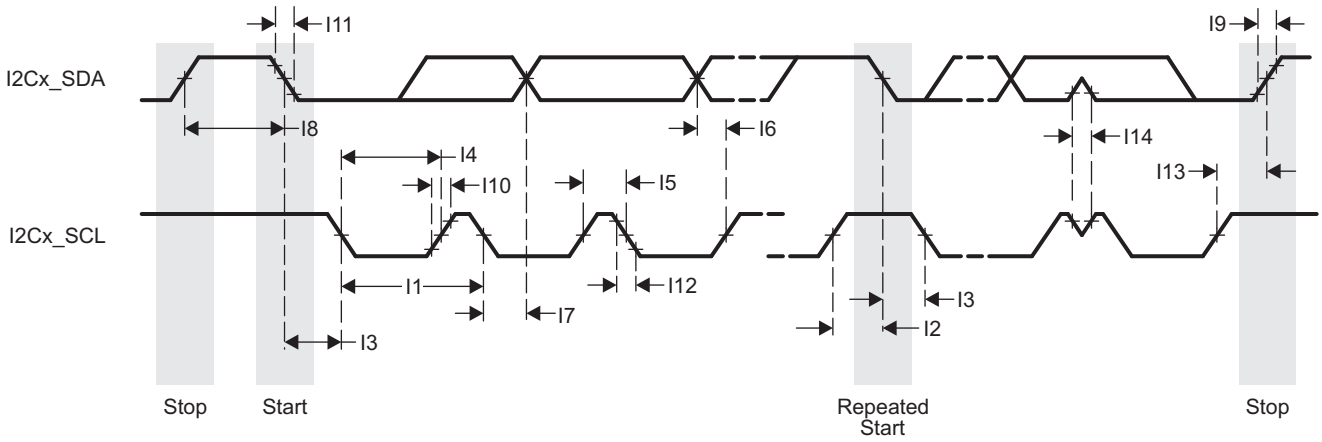

Figure 5-47. I2C Receive Timing(1)

(1) x in I2Cx_SDA and I2Cx_SCL is 0, 1 or 2.

Table 5-48 and Figure 5-48 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-48. Switching Characteristics Over Recommended Operating Conditions for I2C Output Timings

NO.	PARAMETER		STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
I15	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
I16	$t_{su(SCLH-SDAL)}$	Setup Time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
I17	$t_{h(SDAL-SCLL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
I18	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
I19	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
I20	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid before SCL high	250		100		ns
I21	$t_{h(SCLL-SDAV)}$	Hold time, SDA valid after SCL low	0	3.45	0	0.9	µs
I22	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
I23	$t_{r(SDA)}$	Rise time, SDA		1000	20 + 0.1Cb(1)	300	ns
I24	$t_{r(SCL)}$	Rise time, SCL		1000	20 + 0.1Cb(1)	300	ns

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Table 5-48. Switching Characteristics Over Recommended Operating Conditions for I2C Output Timings (continued)

NO.	PARAMETER		STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
I25	$t_{f(SDA)}$	Fall time, SDA		300	20 + 0.1Cb(1)	300	ns
I26	$t_{f(SCL)}$	Fall time, SCL		300	20 + 0.1Cb(1)	300	ns
I27	$t_{su(SCLH-SDAH)}$	Setup time, high before SDA high (for STOP condition)	4		0.6		µs

(1) Cb is line load in pF.

NOTE

I2C emulation is achieved by configuring the LVCMOS buffers to output HiZ instead of driving high when transmitting logic-1.

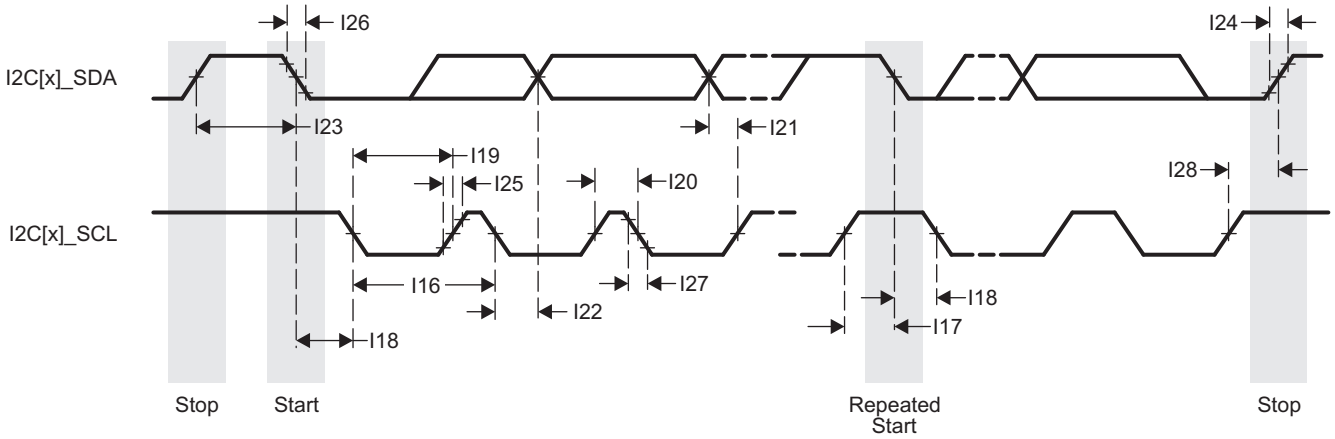

Figure 5-48. I2C Transmit Timing(1)

(1) x in I2Cx_SDA and I2Cx_SCL is 0, 1 or 2.

For more information, see section *Inter-IC module (I2C)* in chapter *Peripherals* of the Device TRM.

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5.9.4.7 McASP

For more details about features and additional description information on the device Multichannel Audio Serial Port, see the corresponding sections within Section 4.3, *Signal Descriptions* and Section 6, *Detailed Description*.

Table 5-49, Table 5-50, and Figure 5-49 present timing requirements for McASP0 to McASP2.

Table 5-49. Timing Requirements for McASP(4)

NO.				MIN	MAX	UNIT
ASP1	$t_{c(AHCLKRX)}$	Cycle time, McASP[x]_AHCLKR/X		20		ns
ASP2	$t_{w(AHCLKRX)}$	Pulse duration, McASP[x]_AHCLKR/X high or low		0.5P - 2.5(2)		ns
ASP3	$t_{c(ACLKRX)}$	Cycle time, McASP[x]_ACLKR/X		20		ns
ASP4	$t_{w(ACLKRX)}$	Pulse duration, McASP[x]_ACLKR/X high or low		0.5R - 2.5(3)		ns
ASP5	$t_{su(AFSRX-ACLKRX)}$	Setup time, McASP[x]_AFSR/X input valid before McASP[x]_ACLKR/X	ACLKR/X int	12.3		ns
			ACLKR/X ext in	4		
			ACLKR/X ext out	4		
ASP6	$t_{h(ACLKRX-AFSRX)}$	Hold time, McASP[x]_AFSR/X input valid after McASP[x]_ACLKR/X	ACLKR/X int	-1		ns
			ACLKR/X ext in	1.6		
			ACLKR/X ext out	1.6		
ASP7	$t_{su(AXR-ACLKRX)}$	Setup time, McASP[x]_AXR input valid before McASP[x]_ACLKR/X	ACLKR/X int	12.3		ns
			ACLKR/X ext in	4		
			ACLKR/X ext out	4		
ASP8	$t_{h(ACLKRX-AXR)}$	Hold time, McASP[x]_AXR input valid after McASP[x]_ACLKR/X	ACLKR/X int	-1		ns
			ACLKR/X ext in	1.6		
			ACLKR/X ext out	1.6		

(1) ACLKR internal: ACLKRCTL.CLKRM = 1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR external output: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
ACLKX internal: ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX external output: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1

(2) P = McASP[x]_AHCLKR and McASP[x]_AHCLKX period in ns.

(3) R = McASP[x]_ACLKR and McASP[x]_ACLKX period in ns.

(4) x in McASP[x]_* is 0, 1 or 2

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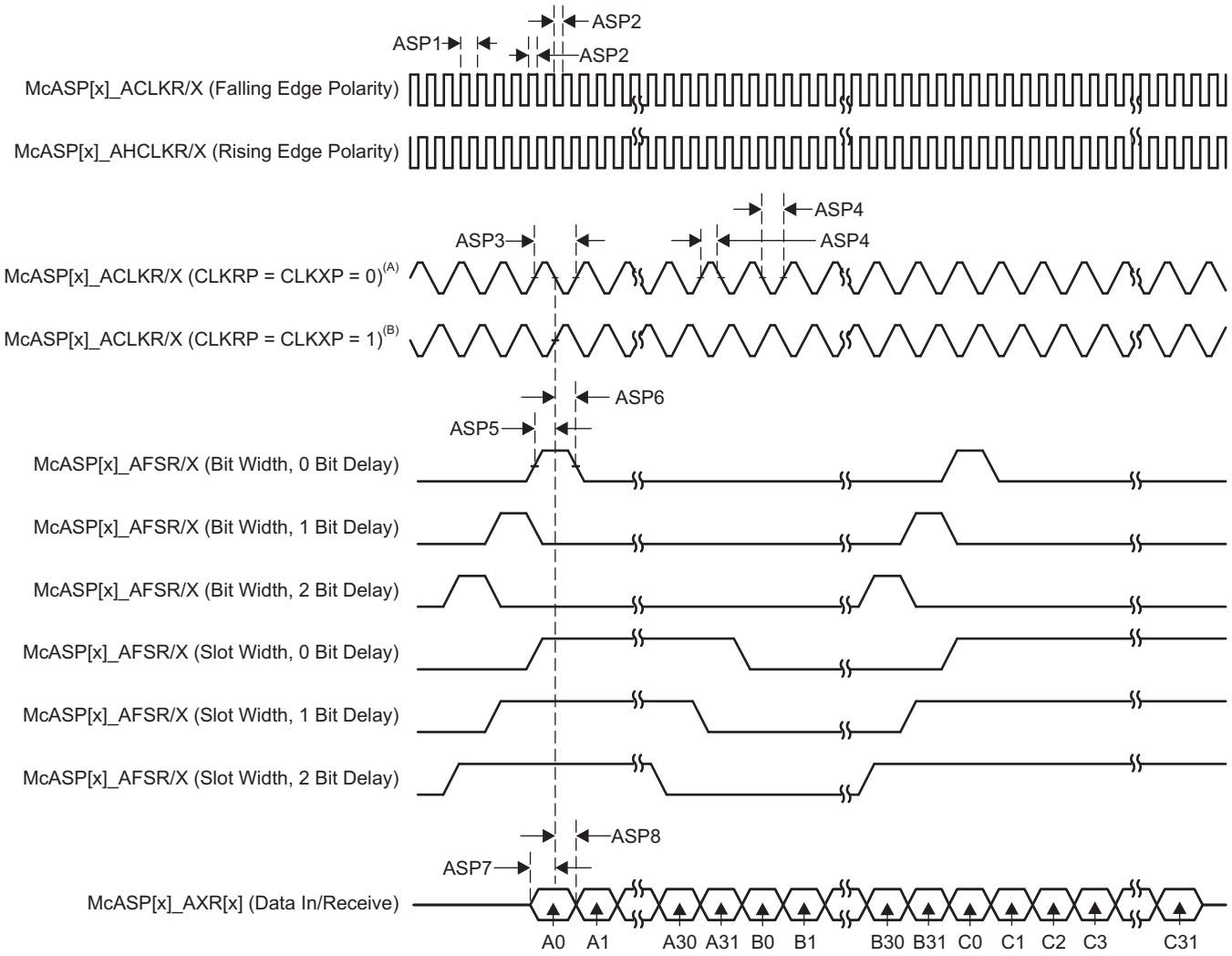

A. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

B. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

Figure 5-49. McASP Input Timing

(1) x in McASP[x]_* is 0, 1 or 2

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Table 5-50 and Figure 5-50 present switching characteristics over recommended operating conditions for McASP0 to McASP2.

Table 5-50. Switching Characteristics Over Recommended Operating Conditions for McASP(4)

NO.				MIN	MAX	UNIT
ASP9	$t_{c(AHCLKRX)}$	Cycle time, McASP[x]_AHCLKR/X		20(2)		ns
ASP10	$t_{w(AHCLKRX)}$	Pulse duration, McASP[x]_AHCLKR/X high or low		0.5P - 2.5(3)		ns
ASP11	$t_{c(ACLKRX)}$	Cycle time, McASP[x]_ACLKR/X		20		ns
ASP12	$t_{w(ACLKRX)}$	Pulse duration, McASP[x]_ACLKR/X high or low		0.5P - 2.5(3)		ns
ASP13	$t_{d(ACLKRX-AFSRX)}$	Delay time, McASP[x]_ACLKR/X transmit edge to McASP[x]_AFSR/X output valid	ACLKR/X int	0	7.25	ns
			ACLKR/X ext in	2	14	
		Delay time, McASP[x]_ACLKR/X transmit edge to McASP[x]_AFSR/X output valid with Pad Loopback	ACLKR/X ext out	2	14	
ASP14	$t_{d(ACLKX-AXR)}$	Delay time, McASP[x]_ACLKX transmit edge to McASP[x]_AXR output valid	ACLKX int	0	7.25	ns
			ACLKX ext in	2	14	
		Delay time, McASP[x]_ACLKX transmit edge to McASP[x]_AXR output valid with Pad Loopback	ACLKX ext out	2	14	
ASP15	$t_{dis(ACLKX-AXR)}$	Disable time, McASP[x]_ACLKX transmit edge to McASP[x]_AXR output high impedance	ACLKX int	0	7.25	ns
			ACLKX ext in	2	14	
		Disable time, McASP[x]_ACLKX transmit edge to McASP[x]_AXR output high impedance with Pad Loopback	ACLKX ext out	2	14	

(1) ACLKR internal: ACLKRCTL.CLKRM = 1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR external output: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
ACLKX internal: ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX external output: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1

(2) 50 MHz

(3) P = AHCLKR and AHCLKX period.

(4) x in McASP[x]_* is 0, 1 or 2

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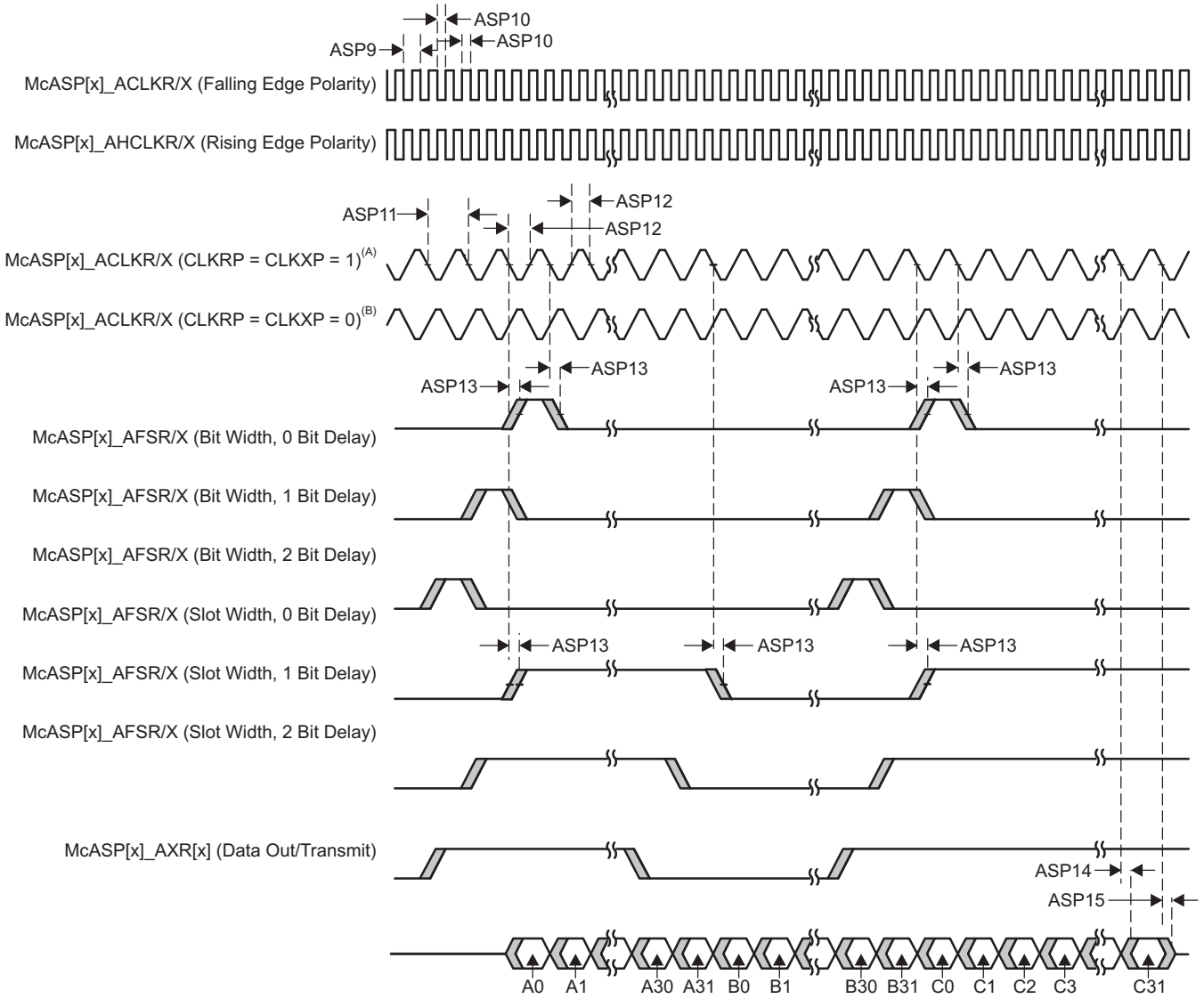

A. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

B. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

Figure 5-50. McASP Output Timing

(1) x in McASP[x]_* is 0, 1 or 2

For more information, see section *Multi-channel Audio Serial Port (McASP)* in chapter *Peripherals* of the Device TRM.

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5.9.4.8 McBSP

For more details about features and additional description information on the device Multichannel Buffered Serial Port, see the corresponding sections within Section 4.3, *Signal Descriptions* and Section 6, *Detailed Description*.

Table 5-51, Table 5-52, and Figure 5-51 present timing requirements and switching characteristics for McBSP Interface.

Table 5-51. McBSP Timing Requirements[1]

NO.				MIN	MAX	UNIT
BSP2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X ext	2P[2] or 20[3]		ns
BSP3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X ext	P-1[4]		ns
BSP5	$t_{su(FRH-CKRL)}$	Setup time, external FSR high before CLKR low	CLKR int	14		ns
			CLKR ext	4		
BSP6	$t_{h(CKRL-FRH)}$	Hold time, external FSR high after CLKR low	CLKR int	6		ns
			CLKR ext	3		
BSP7	$t_{su(DRV-CKRL)}$	Setup time, DR valid before CLKR low	CLKR int	14		ns
			CLKR ext	4		
BSP8	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR low	CLKR int	3		ns
			CLKR ext	3		
BSP10	$t_{su(FXH-CKXL)}$	Setup time, external FSX high before CLKX low	CLKR int	14		ns
			CLKR ext	4		
BSP11	$t_{h(CKXL-FXH)}$	Hold time, external FSX high after CLKX low	CLKR int	6		ns
			CLKR ext	3		

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

(2) P = 1/SYSCLK1 period in ns.

(3) Use whichever value is greater. Minimum CLKR/X cycle times must be met, even when CLKR/X is generated by an internal clock source. The minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.

(4) This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.

Table 5-52. McBSP Switching Characteristics[1]

NO.	PARAMETER			MIN	MAX	UNIT
BSP1	$t_{d(CKSH-CKRXH)}$	Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input.		1	14.5	ns
BSP2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X int	2P[2] or 20[3]		ns
BSP3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X int	C – 2[4]	C + 2[4]	ns
BSP4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid	CLKR int	–4	5.5	ns
			CLKR int	1	14.5	ns
BSP9	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid	CLKX int	–4	5.5	ns
			CLKX ext	1	14.5	
BSP12	$t_{dis(CKXH-DXHZ)}$	Disable time, DX HiZ following last data bit from CLKX high	CLKX int	–4	7.5	ns
			CLKX ext	1	14.5	
BSP13	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	CLKX int	–4 + D1[5]	5.5 + D2[5]	ns
			CLKX ext	1 + D1[5]	14.5 + D2[5]	
BSP14	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid applies ONLY when in data delay 0 (XDATDLY = 00b) mode	FSX int	–4 + D1[6]	5 + D2[6]	ns
			FSX ext	–2 + D1[6]	14.5 + D2[6]	

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(1) Minimum delay times also represent minimum output hold times.

(2) P = 1/SYSCLK1 period in ns.

(3) Use whichever value is greater.

(4) C = H or L

S = sample rate generator input clock = P if CLKSM = 1 (P = 1/SYSCLK1 period in ns)
S = sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
If CLKGDV is even:
(1) H = CLKX high pulse width = (CLKGDV/2 + 1) × S
(2) L = CLKX low pulse width = (CLKGDV/2) × S
If CLKGDV is odd:
(1) H = (CLKGDV + 1)/2 × S
(2) L = (CLKGDV + 1)/2 × S
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit.

(5) Extra delay from CLKX high to DX valid applies only to the first data bit of a device, if and only if DXENA = 1 in SPCR.

if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 4P, D2 = 8P

(6) Extra delay from FSX high to DX valid applies only to the first data bit of a device, if and only if DXENA = 1 in SPCR.

if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 4P, D2 = 8P

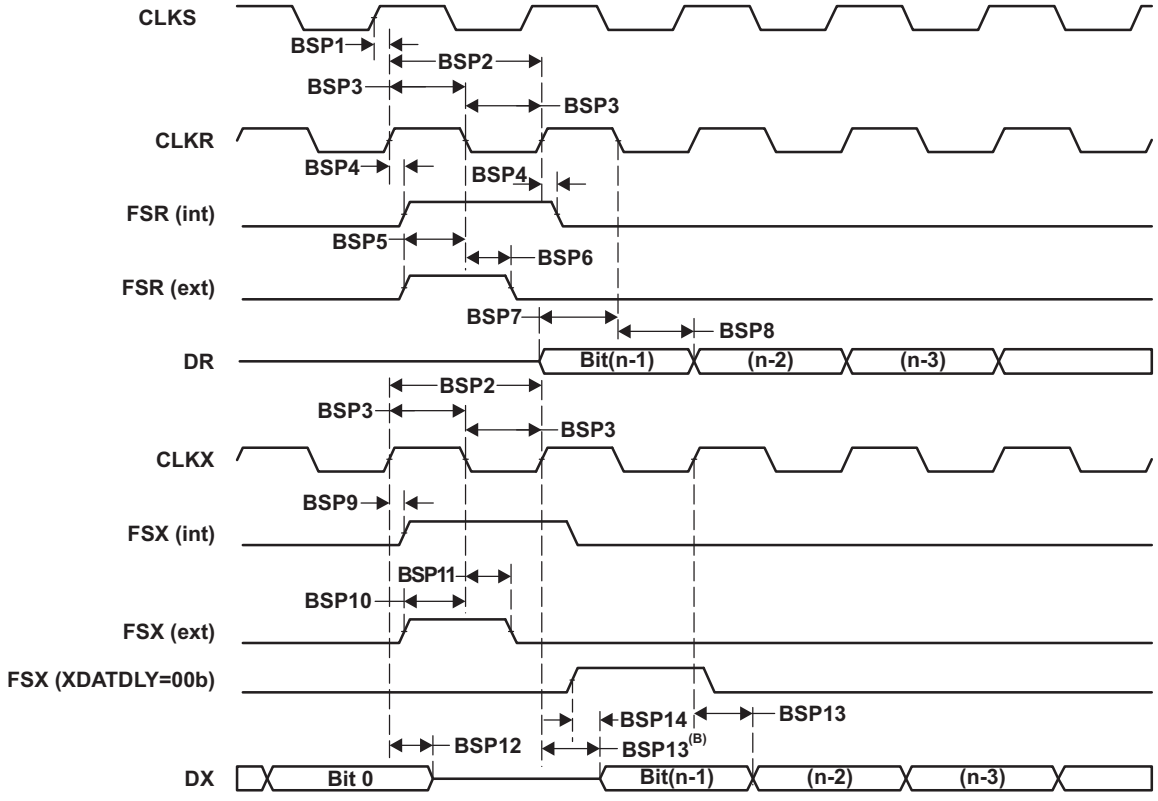

Figure 5-51. McBSP Timing

Table 5-53. McBSP Timing Requirements for FSR When GSYNC = 1

NO.			MIN	MAX	UNIT
BSPF1	$t_{su(FRH-CKSH)}$	Setup time, FSR high before CLKS high	4		ns
BSPF2	$t_{h(CKSH-FRH)}$	Hold time, FSR high after CLKS high	4		ns

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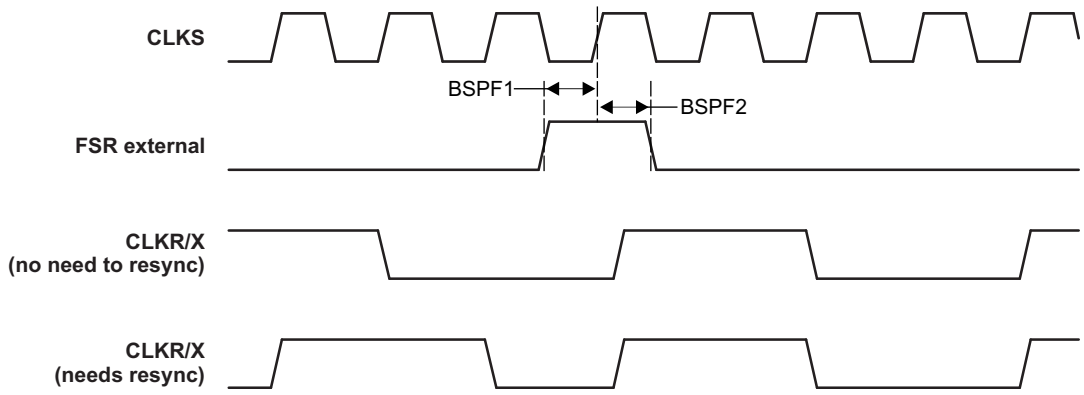

Figure 5-52. FSR Timing When GSYNC = 1

5.9.4.9 MLB

For more details about features and additional description information on the device Media Local Bus, see the corresponding sections within Section 4.3, *Signal Descriptions* and Section 6, *Detailed Description*.

NOTE

MLB in 6-pin mode may require pullups/ pulldowns on SIG and DAT bus signals. For additional details, please consult the MediaLB Interface Specification.

Table 5-54 and Figure 5-53 present Timing Requirements for MLBCLK 3-Pin Option.

Table 5-54. Timing Requirements for MLBCLK 3-Pin Option

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
M31	$t_{c(MLBCLK)}$	Cycle time, MLB_CLK	512FS	39		ns
			1024FS	19.5		ns
M32	$t_{w(MLBCLKH)}$	Pulse duration, MLB_CLK high	512FS	14		ns
			1024FS	9.3		ns
M33	$t_{w(MLBCLKL)}$	Pulse duration, MLB_CLK low	512FS	14		ns
			1024FS	6.1		ns
M34	$t_{t(MLBCLKH)}$	Transition time, MLB_CLK high	512FS		3	ns
			1024FS		1	ns
	$t_{t(MLBCLKL)}$	Transition time, MLB_CLK low	512FS		3	ns
			1024FS		1	ns

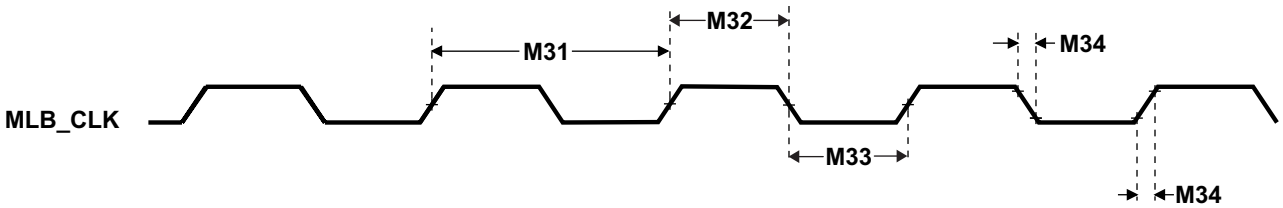

Figure 5-53. MLB_CLK Timing

Table 5-55, Table 5-56, and Figure 5-54 present Timing Requirements and Switching Characteristics for MLB 3-Pin Option.

Table 5-55. Timing Requirements for Receive Data for the MLB 3-Pin Option

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
M35	$t_{su(MLBDAT-MLBCLKL)}$	Setup time, MLB_DAT/MLB_SIG input valid before MLB_CLK low	512FS	1		ns
			1024FS	1		ns
M36	$t_{h(MLBCLKL-MLBDAT)}$	Hold time, MLB_DAT/MLB_SIG input valid after MLB_CLK low	512FS	4		ns
			1024FS	2		ns

Table 5-56. Switching Characteristics Over Recommended Operating Conditions for MLB 3-Pin Option

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
M37	$t_{d(MLBCLKH-MLBDATV)}$	Delay time, MLB_CLK rising to MLB_DAT/MLB_SIG valid	512FS	0	10	ns
			1024FS	0	7	ns
M38	$t_{dis(MLBCLKL-MLBDATZ)}$	Disable time, MLB_CLK falling to MLB_DAT/MLB_SIG HiZ	512FS	0	14	ns
			1024FS	0	6.1	ns

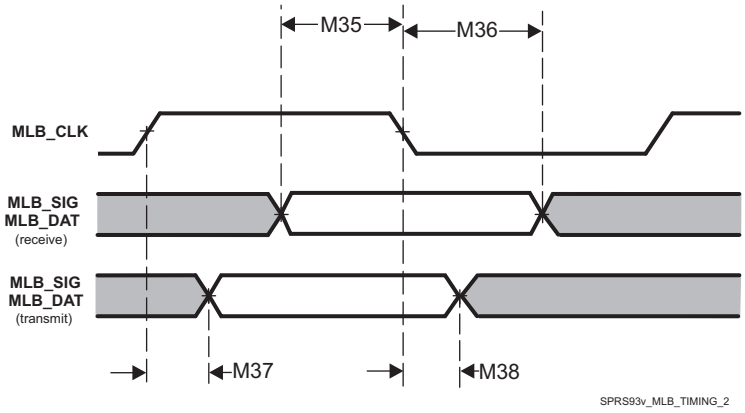

Figure 5-54. MLB 3-Pin Timing

Table 5-57 and Figure 5-55 present Timing Requirements for MLKCLK 6-Pin Option.

Table 5-57. Timing Requirements for MLBCLK 6-Pin Option (1)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
M61	$t_{c(CLKx)}$	Cycle time, MLBP_CLK_x	2048FS	10		ns
M62	$t_{w(CLKxH)}$	Pulse duration, MLBP_CLK_x high	2048FS	4.5		ns
M63	$t_{w(CLKxL)}$	Pulse duration, MLBP_CLK_x low	2048FS	4.5		ns
M64	$t_{t(CLKxH)}$	Transition time, MLBP_CLK_x high	2048FS		1	ns
	$t_{t(CLKxL)}$	Transition time, MLBP_CLK_x low	2048FS		1	ns

(1) x in MLBP_CLK_x is P or N.

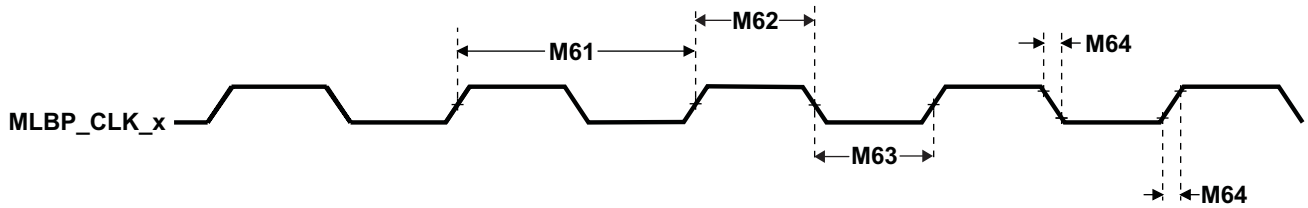

Figure 5-55. MLB_CLKP/N Timing(1)

(1) x in MLBP_CLK_x is P or N.

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Table 5-58, Table 5-59, and Figure 5-56 present Timing Requirements and Switching Characteristics for MLB 6-Pin Option.

Table 5-58. Timing Requirements for Receive Data for the MLB 6-Pin Option (1)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
M65	$t_{su(DATx-CLKxH)}$	Setup time, MLBP_DAT_x/MLBP_SIG_x input valid before MLBP_CLK_x rising	2048FS	1		ns
M66	$t_{h(CLKxH-DATx)}$	Hold time, MLBP_DAT_x_/MLBP_SIG_x input valid after MLBP_CLK_x rising	2048FS	0.5		ns

(1) x in MLBP_CLK_x, MLBP_DAT_x, and MLBP_SIG_x is P or N.

Table 5-59. Switching Characteristics Over Recommended Operating Conditions for MLB 6-Pin Option (1)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
M67	$t_{d(CLKxH-DATxV)}$	Delay time, MLBP_CLK_x rising to MLB_DAT_x/MLB_SIG_x valid	2048FS	0.5	7	ns
M68	$t_{dis(CLKxH-DATxZ)}$	Disable time, MLBP_CLK_x rising to MLBP_DAT_x/MLBP_SIG_x HiZ	2048FS	0.5	7	ns

(1) x in MLBP_CLK_x, MLBP_DAT_x, and MLBP_SIG_x is P or N.

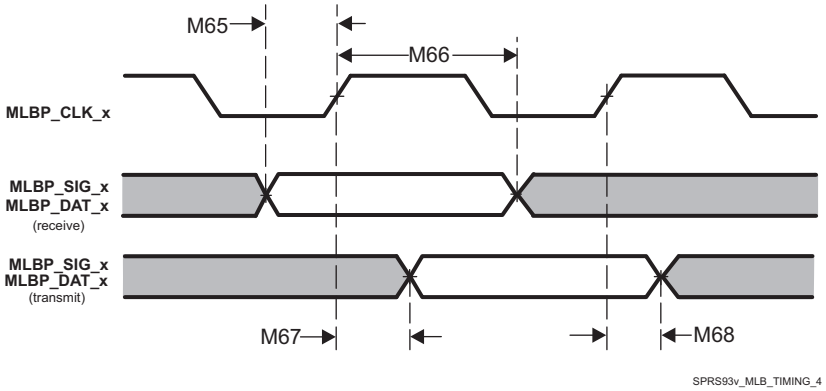

Figure 5-56. MLB 6-Pin Timing(1)

(1) x in MLBP_CLK_x, MLBP_DAT_x, and MLBP_SIG_x is P or N.

For more information, see section *Media Local Bus (MLB)* in chapter *Peripherals* of the Device TRM.

5.9.4.10 MMC/SD

For more details about features and additional description information on the device Multi Media Card, see the corresponding sections within Section 4.3, *Signal Descriptions* and Section 6, *Detailed Description*.

NOTE

The MMC/SD/SDIOi (i = 0 to 1) controller is also referred to as MMCi.

Table 5-60. MMC Timing Conditions

TIMING CONDITION PARAMETER		MIN	TYP	MAX	UNIT
Input Conditions					
t_r	Input signal rise time (10% to 90%)	1		2.2	ns
t_f	Input signal fall time (90% to 10%)	1		2.2	ns
Output Condition					
C_{load}	Output load capacitance	2		40	pF

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Table 5-61. Timing Requirements for MMC0_CMD and MMC0_DATn[1]

(see Figure 5-57)

NO.	PARAMETER		3.3 V			UNIT
			MIN	TYP	MAX	
MMC1	$t_{su(CMDV-CLKH)}$	Setup time, MMC_CMD valid before MMC_CLK rising clock edge	3.9			ns
MMC2	$t_{h(CLKH-CMDV)}$	Hold time, MMC_CMD valid after MMC_CLK rising clock edge	2.5			ns
MMC3	$t_{su(DATV-CLKH)}$	Setup time, MMC_DATn valid before MMC_CLK rising clock edge	3.9			ns
MMC4	$t_{h(CLKH-DATV)}$	Hold time, MMC_DATn valid after MMC_CLK rising clock edge	2.5			ns

(1) n in MMC_DATn is 0 to 7.

Table 5-62. Timing Requirements for MMC1_CMD and MMC1_DATn when operating in SDR mode[1]

(see Figure 5-57)

NO.	PARAMETER		1.8 V			UNIT
			MIN	TYP	MAX	
MMC1	$t_{su(CMDV-CLKH)}$	Setup time, MMC_CMD valid before MMC_CLK rising clock edge	4.2			ns
MMC2	$t_{h(CLKH-CMDV)}$	Hold time, MMC_CMD valid after MMC_CLK rising clock edge	2.5			ns
MMC3	$t_{su(DATV-CLKH)}$	Setup time, MMC_DATn valid before MMC_CLK rising clock edge	4.2			ns
MMC4	$t_{h(CLKH-DATV)}$	Hold time, MMC_DATn valid after MMC_CLK rising clock edge	2.5			ns

(1) n in MMC_DATn is 0 to 7.

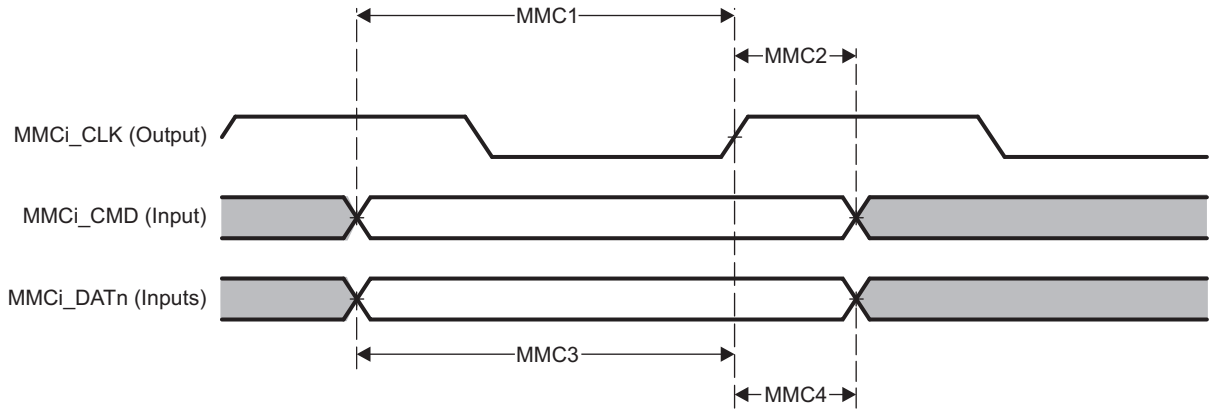

Figure 5-57. MMCi_CMD and MMCi_DATn Input Timing[1]

(1) i in MMCi_CLK, MMCi_CMD, and MMCi_DATn is 0 or 1, where n = 0 to 7.

Table 5-63. Timing Requirements for MMC1_CMD and MMC1_DATn when operating in DDR mode[3]

(see Figure 5-58)

NO.	PARAMETER		1.8 V			UNIT
			MIN	TYP	MAX	
MMC1	$t_{su(CMDV-CLKH)}$	Setup time, MMC_CMD valid before MMC_CLK rising clock edge	4.2			ns
MMC2	$t_{h(CLKH-CMDV)}$	Hold time, MMC_CMD valid after MMC_CLK rising clock edge	2.5			ns
MMC3	$t_{su(DATV-CLKH)}$	Setup time, MMC_DATn valid before MMC_CLK rising or falling clock edge	0.5[1]			ns

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Table 5-63. Timing Requirements for MMC1_CMD and MMC1_DATn when operating in DDR mode(3) (continued)

(see Figure 5-58)

NO.	PARAMETER		1.8 V			UNIT
			MIN	TYP	MAX	
MMC4	$t_{h(CLKH-DATV)}$	Hold time, MMC_CLK rising or falling clock edge after MMC_DATn valid	1.62(2)			ns

(1) The minimum setup time of 0.5 ns is a function of the maximum output delay of 7 ns defined in the JESD84 standard plus the combined PCB delay of the MMC_CLK and MMC_DATn signal traces. Therefore, the PCB shall be designed with less than 2.9 ns of combined delay in the MMC_CLK and MMC_DATn signal traces when operating at the maximum frequency of 48 MHz.

(2) The minimum hold time of 1.62 ns exceeds the minimum output delay of 1.5 ns defined in the JESD84 standard. Therefore, the PCB shall be designed with greater than 120 ps of combined delay in the MMC_CLK and MMC_DATn signal traces.

(3) n in MMC_DATn is 0 to 7.

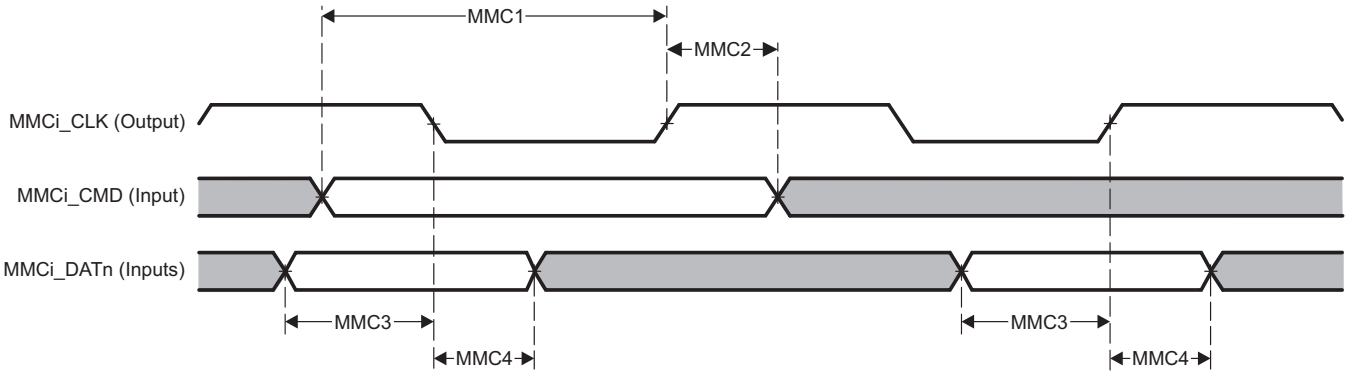

Figure 5-58. MMC1_CMD and MMC1_DATn Input Timing - DDR Mode(1)

(1) i in MMCi_CLK, MMCi_CMD, and MMCi_DATn is 1, where n = 0 to 7.

Table 5-64. Switching Characteristics for MMCi_CLK(2)

(see Figure 5-59)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
MMC5	$f_{op(CLK)}$	Operating frequency, MMC_CLK			48	MHz
	$t_{cop(CLK)}$	Operating period: MMC_CLK	20.8			ns
	$f_{id(CLK)}$	Identification mode frequency, MMC_CLK			400	kHz
	$t_{cid(CLK)}$	Identification mode period: MMC_CLK	2500			ns
MMC6	$t_{w(CLKL)}$	Pulse duration, MMC_CLK low	(0.5 × P) - $t_{f(CLK)}$(1)			ns
MMC7	$t_{w(CLKH)}$	Pulse duration, MMC_CLK high	(0.5 × P) - $t_{r(CLK)}$(1)			ns
MMC8	$t_{r(CLK)}$	Rise time, All Signals (10% to 90%)			2.2	ns
MMC9	$t_{f(CLK)}$	Fall time, All Signals (90% to 10%)			2.2	ns

(1) P = MMC_CLK period.

(2) i in MMCi_CLK is 0 or 1.

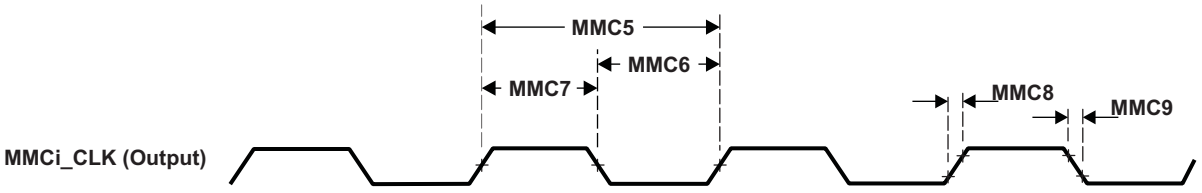

Figure 5-59. MMCi_CLK Timing(1)

(1) i in MMCi_CLK is 0 or 1.

Table 5-65. Switching Characteristics for MMC0_CMD and MMC0_DATn—HSPE=0[(1)]

(see Figure 5-60)

NO.	PARAMETER		3.3 V			UNIT
			MIN	TYP	MAX	
MMC10	$t_{d(CLKL-CMD)}$	Delay time, MMC_CLK falling clock edge to MMC_CMD transition	-7.4		4.4	ns
MMC11	$t_{d(CLKL-DAT)}$	Delay time, MMC_CLK falling clock edge to MMC_DATn transition	-7.4		4.4	ns

(1) n in MMC_DATn is 0 to 7.

Table 5-66. Switching Characteristics for MMC1_CMD and MMC1_DATn—HSPE=0 when operating in SDR mode[(1)]

(see Figure 5-60)

NO.	PARAMETER		1.8 V			UNIT
			MIN	TYP	MAX	
MMC10	$t_{d(CLKL-CMD)}$	Delay time, MMC_CLK falling clock edge to MMC_CMD transition	-7.4		7.4	ns
MMC11	$t_{d(CLKL-DAT)}$	Delay time, MMC_CLK falling clock edge to MMC_DATn transition	-7.4		7.4	ns

(1) n in MMC_DATn is 0 to 7.

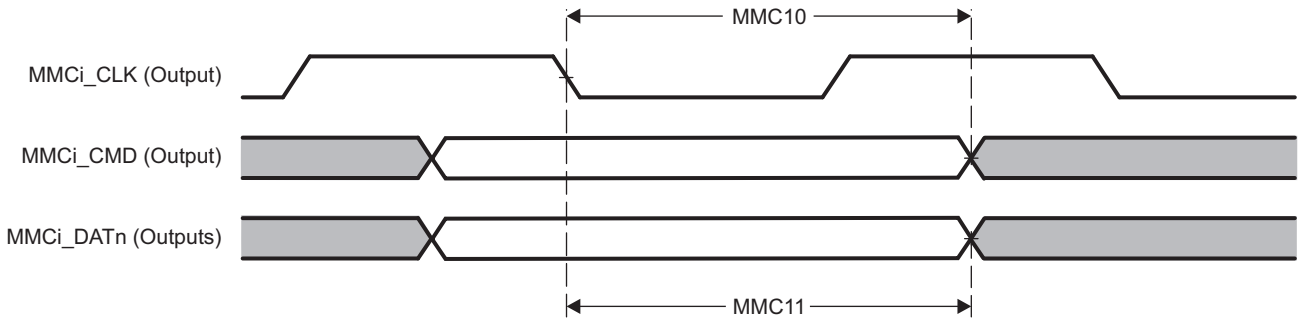

Figure 5-60. MMCi_CMD and MMCi_DATn Output Timing—HSPE=0[(1)]

(1) i in MMCi_CLK, MMCi_CMD, and MMCi_DATn is 0 or 1, where n = 0 to 7.

Table 5-67. Switching Characteristics for MMC1_CMD and MMC1_DATn—HSPE=0 when operating in DDR mode

(see Figure 5-61)

NO.	PARAMETER		1.8 V			UNIT
			MIN	TYP	MAX	
MMC10	$t_{d(CLKL-CMD)}$	Delay time, MMC_CLK falling clock edge to MMC_CMD transition	-4.4		2.2	ns
MMC11	$t_{d(CLKL-DAT)}$	Delay time, MMC_CLK rising or falling clock edge to MMC_DATn transition	-4.4		2.2	ns

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1. n in MMC_DATn is 0 to 7.

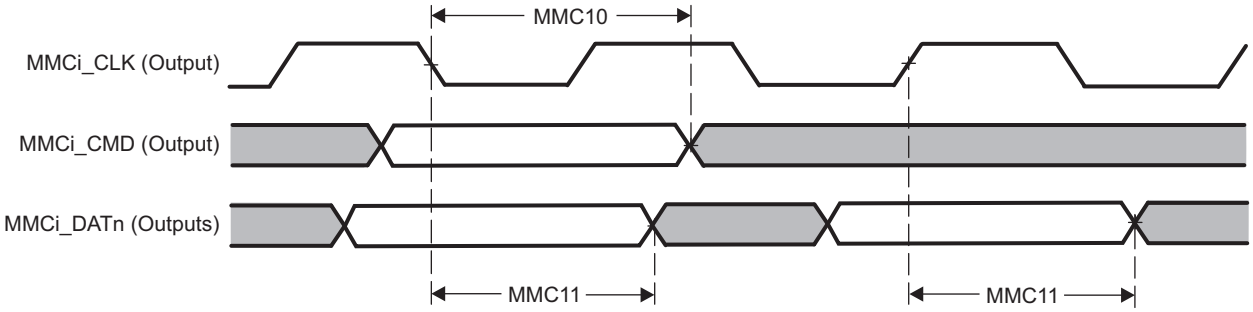

Figure 5-61. MMC1_CMD and MMC1_DATn Output Timing—HSPE=0 – DDR Mode(1)

(1) i in MMCi_CLK, MMCi_CMD, and MMCi_DATn is 1, where n = 0 to 7.

5.9.4.11 PCIESS

For more details about features and additional description information on the device Peripheral Component Interconnect Express, see the corresponding sections within Section 4.3, *Signal Descriptions* and Section 6, *Detailed Description*.

5.9.4.12 PRU-ICSS

The device has integrated two identical PRU subsystems (PRU-ICSS_0 and PRU-ICSS_1). The programmable nature of the PRU cores, along with their access to pins, events and all device resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores of the device.

For more details about features and additional description information on the device Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem, see the corresponding sections within Section 4.3, *Signal Descriptions* and Section 6, *Detailed Description*.

NOTE

The PRU-ICSS_0 and PRU-ICSS_1 support an internal wrapper multiplexing that expands the device top-level multiplexing. Signal naming in this section must match the internal wrapper multiplexing.

For more information, please refer to the Device TRM, Chapter *Processors and Accelerators*, Section *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)*.

5.9.4.12.1 Programmable Real-Time Unit (PRU-ICSS PRU)

NOTE

The PRU-ICSS PRU signals have different functionality depending on the mode of operation. The signal naming in this section matches the naming used in the PRU Module Interface section in the Device TRM.

5.9.4.12.1.1 PRU-ICSS PRU Direct Input/Output Mode Electrical Data and Timing

Table 5-68. PRU-ICSS PRU Timing Requirements - Direct Input Mode

NO.	PARAMETER		MIN	MAX	UNIT
PRDI1	$t_{w(GPI)}$	Pulse width, GPI	2 × P(1)		ns

(1) P = ICSS_n_COREn_CLK clock period, where n = 0 or 1.

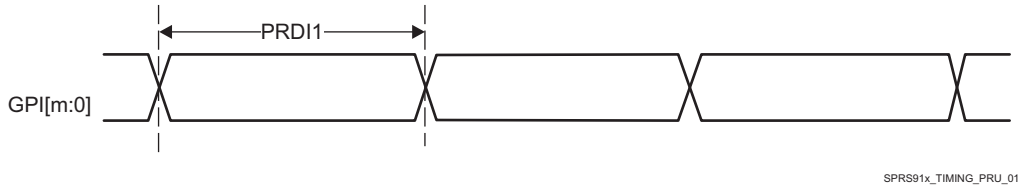

Figure 5-62. PRU-ICSS PRU Direct Input Timing

(1) m in GPI[m:0] = 19.

Table 5-69. PRU-ICSS PRU Switching Requirements – Direct Output Mode

NO.	PARAMETER		MIN	MAX	UNIT
PRDO1	$t_{w(GPO)}$	Pulse width, GPO	2 × P(1)		ns
PRDO2	$t_{sk(GPO)}$	Skew between GPO[19:0] signals		3	ns

(1) P = ICSS_n_COREn_CLK clock period, where n = 0 or 1.

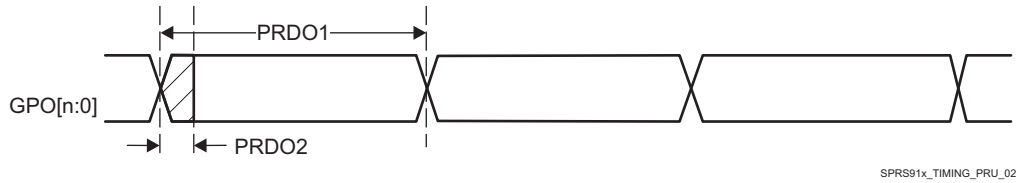

Figure 5-63. PRU-ICSS PRU Direct Output Timing

(1) n in GPO[n:0] = 19.

5.9.4.12.1.2 PRU-ICSS PRU Parallel Capture Mode Electrical Data and Timing

Table 5-70. PRU-ICSS PRU Timing Requirements – Parallel Capture Mode

NO.	PARAMETER		MIN	MAX	UNIT
PRPC1	$t_{w(CLOCKIN)}$	Cyle time, CLOCKIN	20		ns
PRPC2	$t_{w(CLOCKINL)}$	Pulse duration, CLOCKIN low	10		ns
PRPC3	$t_{w(CLOCKINH)}$	Pulse duration, CLOCKIN high	10		ns
PRPC4	$t_{su(DATAIN-CLOCKIN)}$	Setup time, DATAIN valid before CLOCKIN	4.4		ns
PRPC5	$t_{h(CLOCKIN-DATAIN)}$	Hold time, DATAIN valid after CLOCKIN	0		ns

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(1) P = ICSS_n_COREn_CLK clock period, where n = 0 or 1.

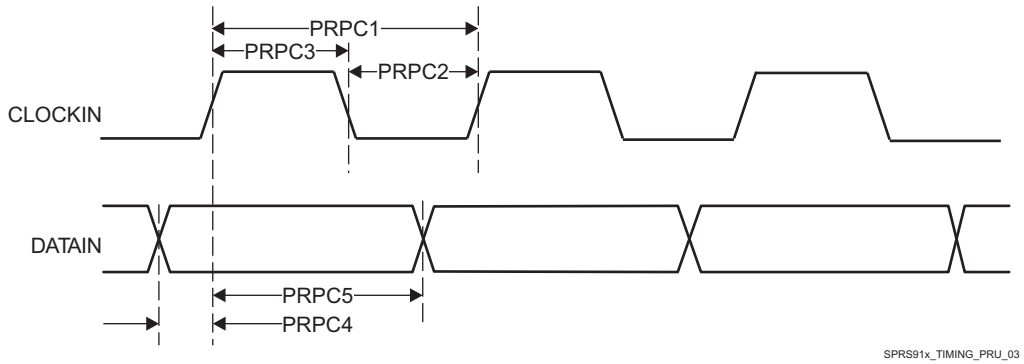

Figure 5-64. PRU-ICSS PRU Parallel Capture Timing – Rising Edge Mode

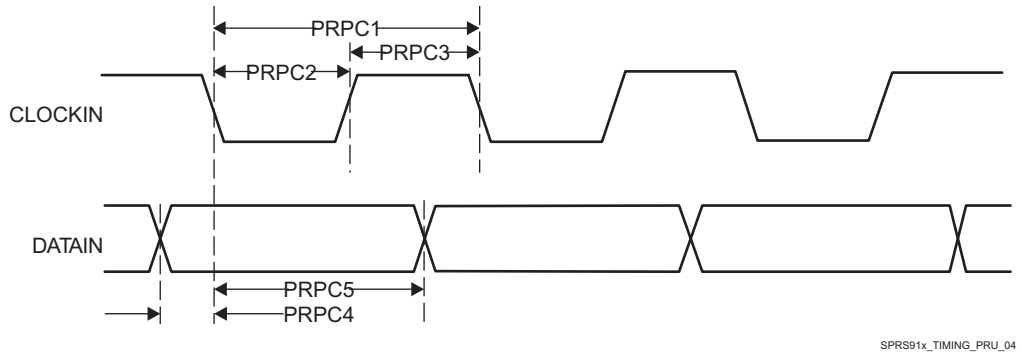

Figure 5-65. PRU-ICSS PRU Parallel Capture Timing – Falling Edge Mode

5.9.4.12.1.3 PRU-ICSS PRU Shift Mode Electrical Data and Timing

Table 5-71. PRU-ICSS PRU Timing Requirements – Shift In Mode

NO.	PARAMETER		MIN	MAX	UNIT
PRSI1	$t_{w(DATAIN)}$	Pulse width, DATAIN	2 × P[(1)] + 3		ns

(1) P = Internal shift in clock period, defined by PRUn_GPI_DIV0 and PRUn_GPI_DIV1 bit fields in the PRUSS_GPCFGn register. For more information, see section *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)* in chapter *Processors and Accelerators* of the Device TRM.

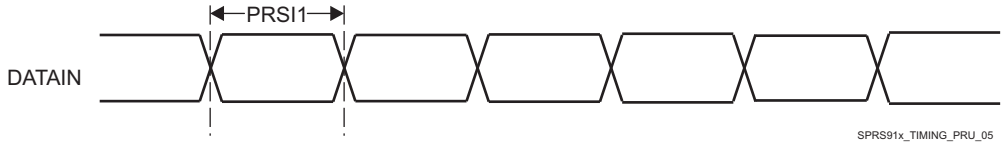

Figure 5-66. PRU-ICSS PRU Shift In Timing

Table 5-72. PRU-ICSS PRU Switching Requirements – Shift Out Mode

NO.	PARAMETER		MIN	MAX	UNIT
PRSO1	$t_{c(CLOCKOUT)}$	Cycle time, CLOCKOUT	13.3		ns
PRSO2	$t_{w(CLOCKOUT)}$	Pulse width, CLOCKOUT	0.4 × P[(1)]	0.5 × P[(1)]	ns
PRSO3	$t_{d(CLOCKOUT-DATAOUT)}$	Delay time, CLOCKOUT to DATAOUT valid	-1.5	3	ns

(1) P = Software programmable shift out clock period, defined by PRUn_GPO_DIV0 and PRUn_GPO_DIV1 bit fields in the PRUSS_GPCFGn register. For more information, see section *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)* in chapter *Processors and Accelerators* of the Device TRM.

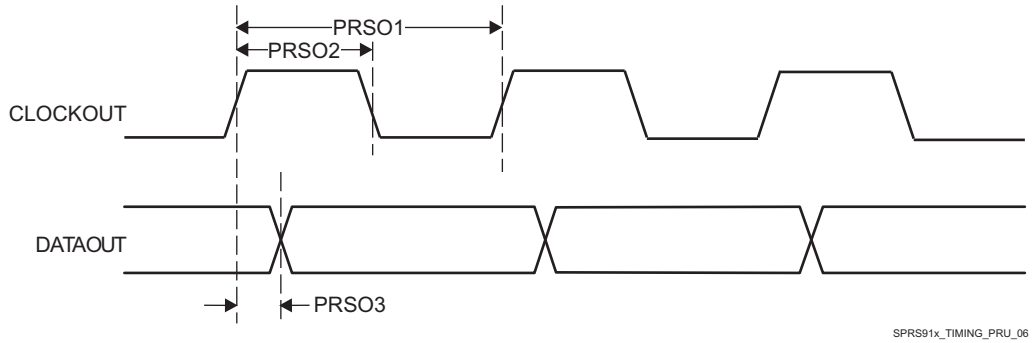

Figure 5-67. PRU-ICSS PRU Shift Out Timing

5.9.4.12.2 PRU-ICSS EtherCAT™ (PRU-ICSS ECAT)

5.9.4.12.2.1 PRU-ICSS ECAT Electrical Data and Timing

Table 5-73. PRU-ICSS ECAT Timing Requirements – Input Validated With SYNCx

NO.	PARAMETER		MIN	MAX	UNIT
EDCS1	$t_{w(EDC_SYNCx_OUT)}$	Pulse width, EDC_SYNCx_OUT	100.00		ns
EDCS2	$t_{su(EDIO_DATA_IN-EDC_SYNCx_OUT)}$	Setup time, EDIO_DATA_IN valid before EDC_SYNCx_OUT rising edge	20.00		ns
EDCS3	$t_{h(EDC_SYNCx_OUT-EDIO_DATA_IN)}$	Hold time, EDIO_DATA_IN valid after EDC_SYNCx_OUT rising edge	20.00		ns

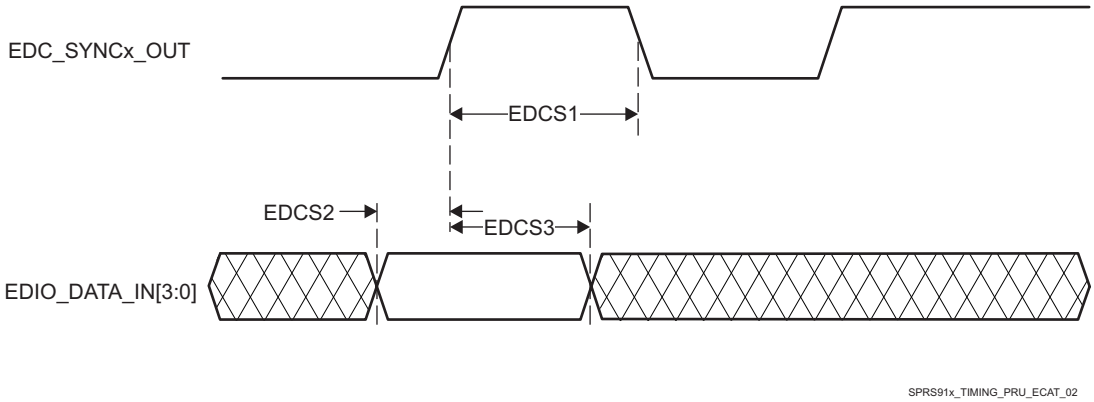

Figure 5-68. PRU-ICSS ECAT Input Validated With SYNCx Timing

Table 5-74. PRU-ICSS ECAT Timing Requirements – LATCHx_IN

NO.	PARAMETER		MIN	MAX	UNIT
EDCL1	$t_{w(EDC_LATCHx_IN)}$	Pulse duration, EDC_LATCHx_IN	3 × P[(1)]		ns

(1) P = ICSS_n_IEP_CLK, where n = 0 or 1.

Figure 5-69. PRU-ICSS ECAT LATCHx_IN Timing

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Table 5-75. PRU-ICSS ECAT Switching Requirements – Digital IOs

NO.	PARAMETER		MIN	MAX	UNIT
EDIOD1	$t_{sk(EDIO_DATA_OUT)}$	EDIO_DATA_OUT skew		8	ns

Figure 5-70. PRU-ICSS EDIO DATA_OUT Timing

(1) n in EDIO_DATA_OUT[n:0] = 3.

5.9.4.12.3 PRU-ICSS MII_RT and Switch

5.9.4.12.3.1 PRU-ICSS MDIO Electrical Data and Timing

Table 5-76. PRU-ICSS MDIO Timing Requirements – MDIO_DATA

NO.	PARAMETER		MIN	MAX	UNIT
PRMDI1	$t_{su(MDIO-MDC)}$	Setup time, MDIO valid before MDC high	90		ns
PRMDI2	$t_{h(MDIO-MDC)}$	Hold time, MDIO valid from MDC high	0		ns

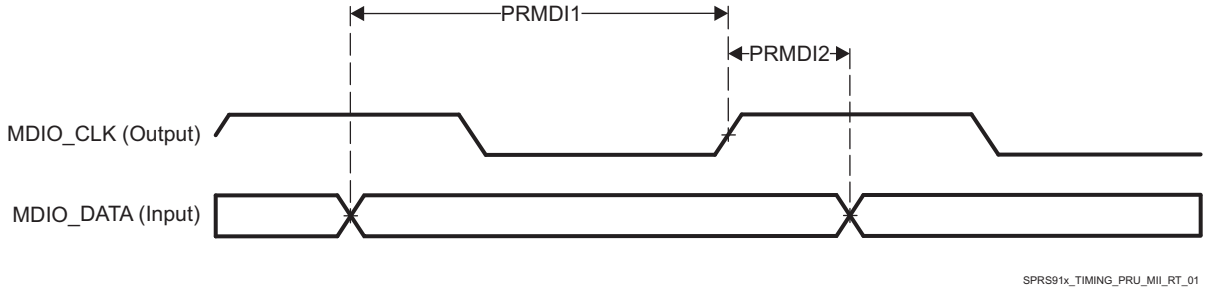

Figure 5-71. PRU-ICSS MDIO_DATA Timing – Input Mode

Table 5-77. PRU-ICSS MDIO Switching Characteristics – MDIO_CLK

NO.	PARAMETER		MIN	MAX	UNIT
PRMC1	$t_{c(MDC)}$	Cycle time, MDC	400		ns
PRMC2	$t_{w(MDCH)}$	Pulse duration, MDC high	160		ns
PRMC3	$t_{w(MDCL)}$	Pulse duration, MDC low	160		ns
PRMC4	$t_{t(MDC)}$	Transition time, MDC		5	ns

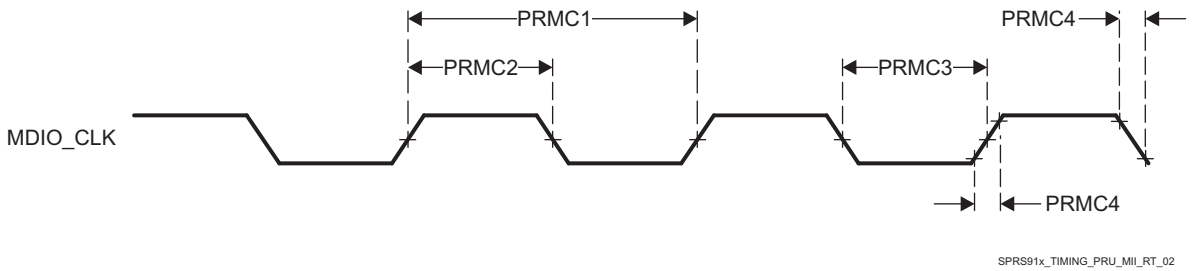

Figure 5-72. PRU-ICSS MDIO_CLK Timing

Table 5-78. PRU-ICSS MDIO Switching Characteristics – MDIO_DATA

NO.	PARAMETER		MIN	MAX	UNIT
PRMDO1	$t_{d(MDC-MDIO)}$	Delay time, MDC high to MDIO valid	10	390	ns

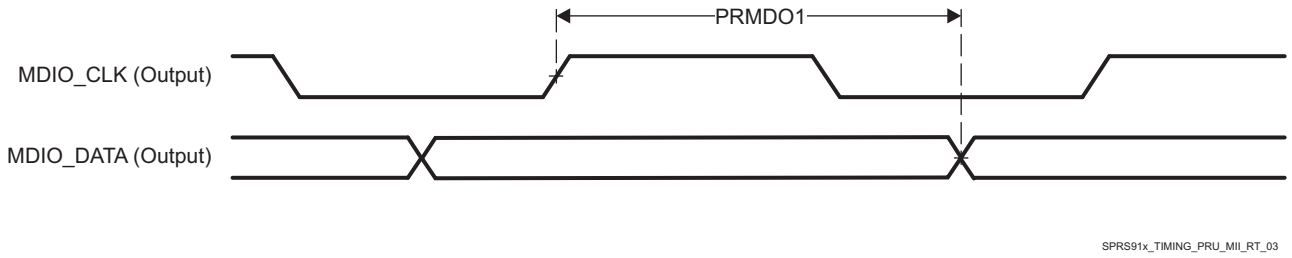

Figure 5-73. PRU-ICSS MDIO_DATA Timing – Output Mode

5.9.4.12.3.2 PRU-ICSS MII_RT Electrical Data and Timing

Table 5-79. PRU-ICSS MII_RT Timing Requirements – MII_RXCLK

NO.	PARAMETER		SPEED	MIN	MAX	UNIT
PMIR1	$t_{c(RXCLK)}$	Cycle time, RXCLK	10 Mbps	399.96	400.04	ns
			100 Mbps	39.996	40.004	ns
PMIR2	$t_{w(RXCLKH)}$	Pulse duration, RXCLK high	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
PMIR3	$t_{w(RXCLKL)}$	Pulse duration, RXCLK low	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
PMIR4	$t_{t(RXCLK)}$	Transition time, RXCLK	10 Mbps		3	ns
			100 Mbps		3	ns

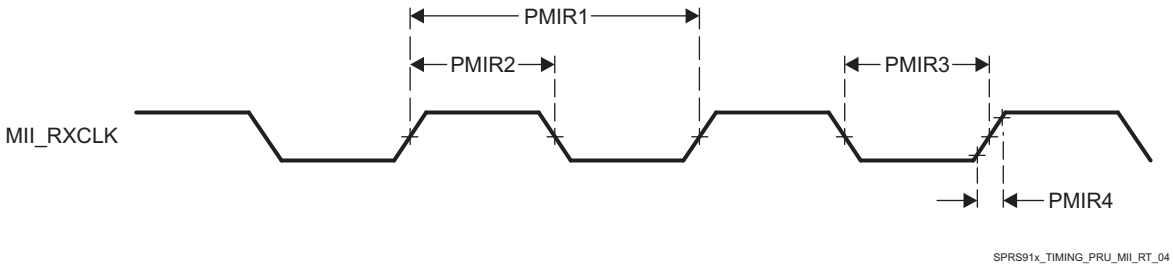

Figure 5-74. PRU-ICSS MII_RXCLK Timing

Table 5-80. PRU-ICSS MII_RT Timing Requirements – MII_TXCLK

NO.	PARAMETER		SPEED	MIN	MAX	UNIT
PMIT1	$t_{c(TXCLK)}$	Cycle time, TXCLK	10 Mbps	399.96	400.04	ns
			100 Mbps	39.996	40.004	ns
PMIT2	$t_{w(TXCLKH)}$	Pulse duration, TXCLK high	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
PMIT3	$t_{w(TXCLKL)}$	Pulse duration, TXCLK low	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
PMIT4	$t_{t(TXCLK)}$	Transition time, TXCLK	10 Mbps		3	ns
			100 Mbps		3	ns

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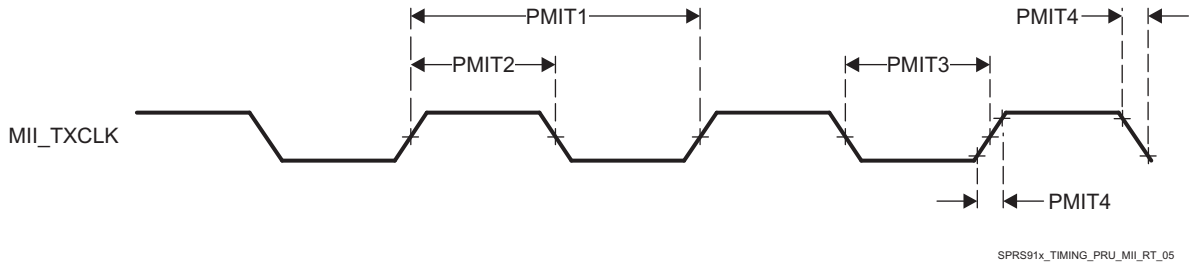

Figure 5-75. PRU-ICSS MII_TXCLK Timing

Table 5-81. PRU-ICSS MII_RT Timing Requirements – MII_RXD[3:0], MII_RXDV, and MII_RXER

NO.	PARAMETER		SPEED	MIN	MAX	UNIT
PMIR5	$t_{su(RXD-RXCLK)}$	Setup time, RXD[3:0] valid before RXCLK	10 Mbps	8		ns
	$t_{su(RXDV-RXCLK)}$	Setup time, RXDV valid before RXCLK				
	$t_{su(RXER-RXCLK)}$	Setup time, RXER valid before RXCLK				
	$t_{su(RXD-RXCLK)}$	Setup time, RXD[3:0] valid before RXCLK	100 Mbps	8		ns
	$t_{su(RXDV-RXCLK)}$	Setup time, RXDV valid before RXCLK				
	$t_{su(RXER-RXCLK)}$	Setup time, RXER valid before RXCLK				
PMIR6	$t_{h(RXCLK-RXD)}$	Hold time, RXD[3:0] valid after RXCLK	10 Mbps	8		ns
	$t_{h(RXCLK-RXDV)}$	Hold time, RXDV valid after RXCLK				
	$t_{h(RXCLK-RXER)}$	Hold time, RXER valid after RXCLK				
	$t_{h(RXCLK-RXD)}$	Hold time, RXD[3:0] valid after RXCLK	100 Mbps	8		ns
	$t_{h(RXCLK-RXDV)}$	Hold time, RXDV valid after RXCLK				
	$t_{h(RXCLK-RXER)}$	Hold time, RXER valid after RXCLK				

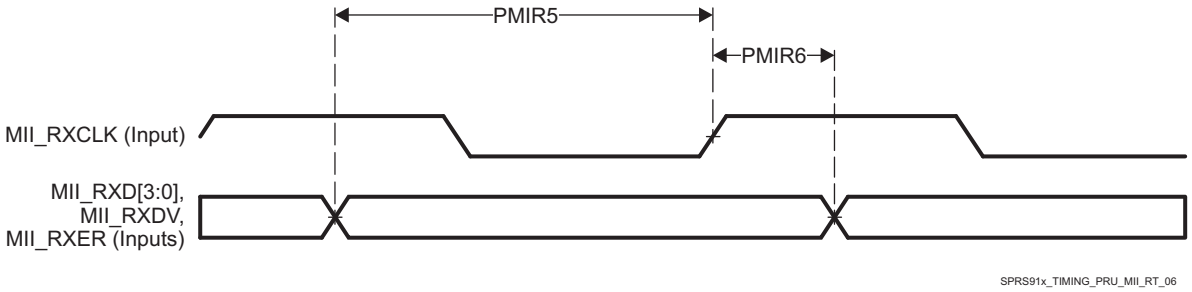

Figure 5-76. PRU-ICSS MII_RXD[3:0], MII_RXDV, and MII_RXER Timing

Table 5-82. PRU-ICSS MII_RT Switching Characteristics – MII_TXD[3:0] and MII_TXEN

NO.	PARAMETER		SPEED	MIN	MAX	UNIT
PMIT5	$t_{d(TXCLK-TXD)}$	Delay time, TXCLK high to TXD[3:0] valid	10 Mbps	4	25	ns
	$t_{d(TXCLK-TXEN)}$	Delay time, TXCLK to TXEN valid				
	$t_{d(TXCLK-TXD)}$	Delay time, TXCLK high to TXD[3:0] valid	100 Mbps	4	25	ns
	$t_{d(TXCLK-TXEN)}$	Delay time, TXCLK to TXEN valid				

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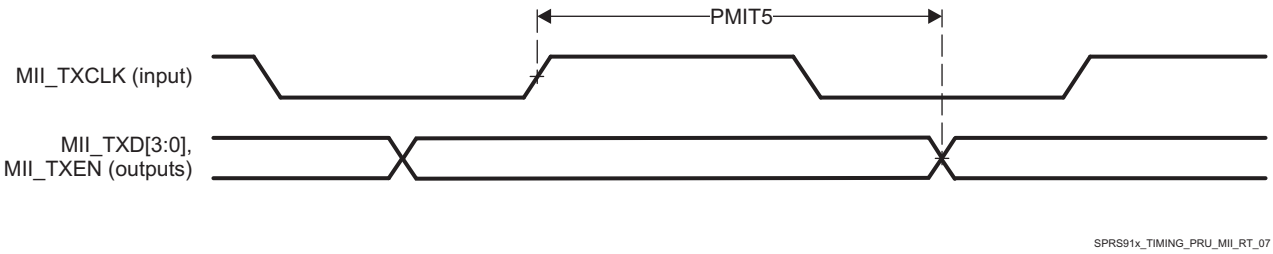

Figure 5-77. PRU-ICSS MII_TXD[3:0], MII_TXEN Timing

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5.9.4.12.4 PRU-ICSS Universal Asynchronous Receiver Transmitter (PRU-ICSS UART)

Table 5-83. PRU-ICSS UART Timing Conditions

PARAMETER		MIN	TYP	MAX	UNIT
Output Condition					
C_{LOAD}	Output load capacitance	5		25	pF

Table 5-84. Timing Requirements for PRU-ICSS UART Receive

NO.	PARAMETER		MIN	MAX	UNIT
PRUR1	$t_{w(RX)}$	Pulse duration, receive start, stop, data bit	0.96U(1)	1.05U (1)	ns

(1) U = UART baud time = 1 / programmed baud rate. For more information, see section *PRU-ICSS UART Clock Generation and Control* in the Device TRM.

Table 5-85. Switching Characteristics Over Recommended Operating Conditions for PRU-ICSS UART Transmit

NO.	PARAMETER		MIN	MAX	UNIT
PRUT1	$f_{(baud)}$	Maximum programmable baud rate	0	12	MHz
PRUT2	$t_{w(TX)}$	Pulse duration, transmit start, stop, data bit	U(1) - 2	U(1) - 2	ns

(1) U = UART baud time = 1 / programmed baud rate. For more information, see section *PRU-ICSS UART Clock Generation and Control* in the Device TRM.

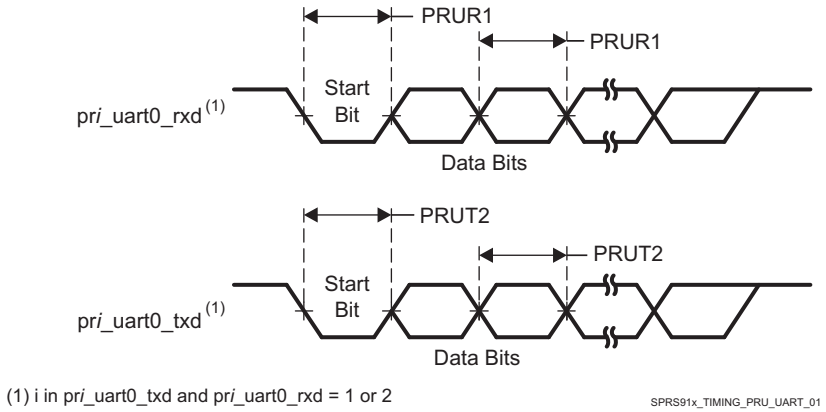

Figure 5-78. PRU-ICSS UART Timing

5.9.4.12.5 PRU-ICSS PRU Sigma Delta and EnDAT Modes

Table 5-86. PRU-ICSS PRU Timing Requirements - Sigma Delta Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRSD1	$t_{w(SDx_CLK)}$	Pulse width, SDx_CLK	20		ns
PRSD2	$t_{su(SDx_D-SDx_CLK)}$	Setup time, SDx_D valid before SDx_CLK active edge	10		ns
PRSD3	$t_{h(SDx_CLK-SDx_D)}$	Hold time, SDx_D valid before SDx_CLK active edge	5		ns

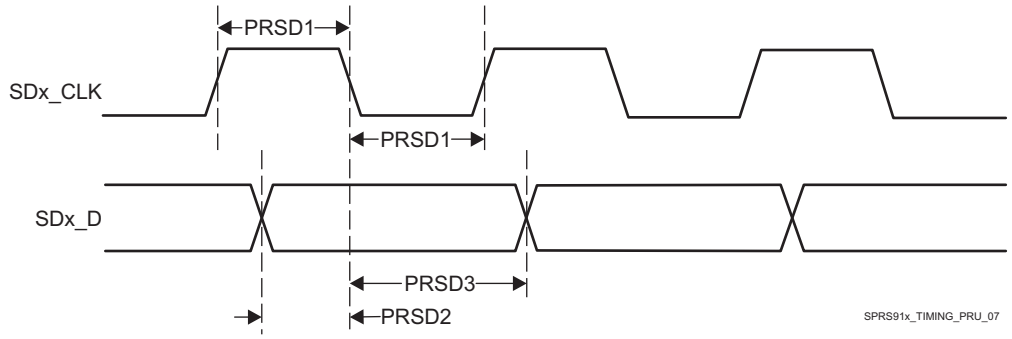

Figure 5-79. PRU-ICSS PRU SD_CLK Falling Active Edge

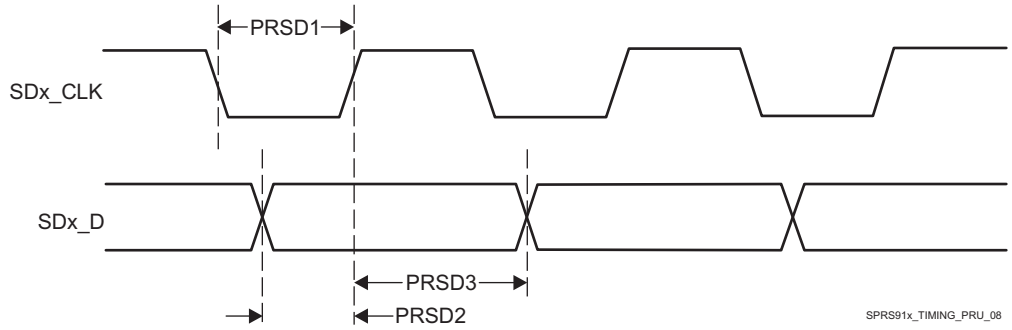

Figure 5-80. PRU-ICSS PRU SD_CLK Rising Active Edge

Table 5-87. PRU-ICSS PRU Timing Requirements - EnDAT Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRTE1	$t_{w(ENDATx_IN)}$	Pulse width, ENDATx_IN	40		ns

Table 5-88. PRU-ICSS PRU Switching Requirements - EnDAT Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRSE2	$t_{w(ENDATx_CLK)}$	Pulse width, ENDATx_CLK	20		ns
PRSE3	$t_{d(ENDATx_OUT-ENDATx_CLK)}$	Delay time, ENDATx_CLK fall to ENDATx_OUT	-10	10	ns
PRSE4	$t_{d(ENDATx_OUT_EN-ENDATx_CLK)}$	Delay time, ENDATx_CLK Fall to ENDATx_OUT_EN	-10	10	ns

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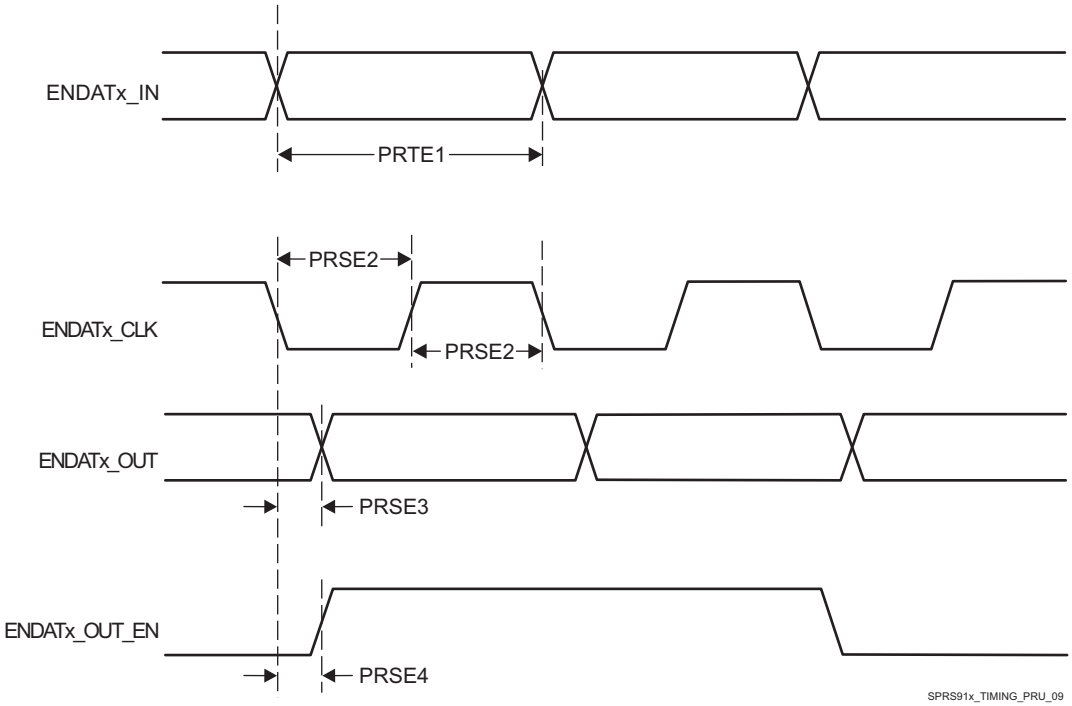

Figure 5-81. PRU-ICSS PRU EnDAT Timing

For more information, see section *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)* in chapter *Processors and Accelerators* of the Device TRM.

5.9.4.13 QSPI

For more details about features and additional description information on the device Quad Serial Port Interface, see the corresponding sections within Section 4.3, *Signal Descriptions* and Section 6, *Detailed Description*.

Table 5-89 and Table 5-90 present timing requirements and switching characteristics for QSPI interface.

Table 5-89. Timing Requirements for QSPI

NO.	PARAMETER		MIN	MAX	UNIT
Q7	$t_{su(D-RTCLK)}$	Setup time, QSPI_D[3:0] valid before active QSPI_RTCLK edge	1.5		ns
Q8	$t_{h(RTCLK-D)}$	Hold time, QSPI_D[3:0] valid after inactive QSPI_RTCLK edge	0		ns

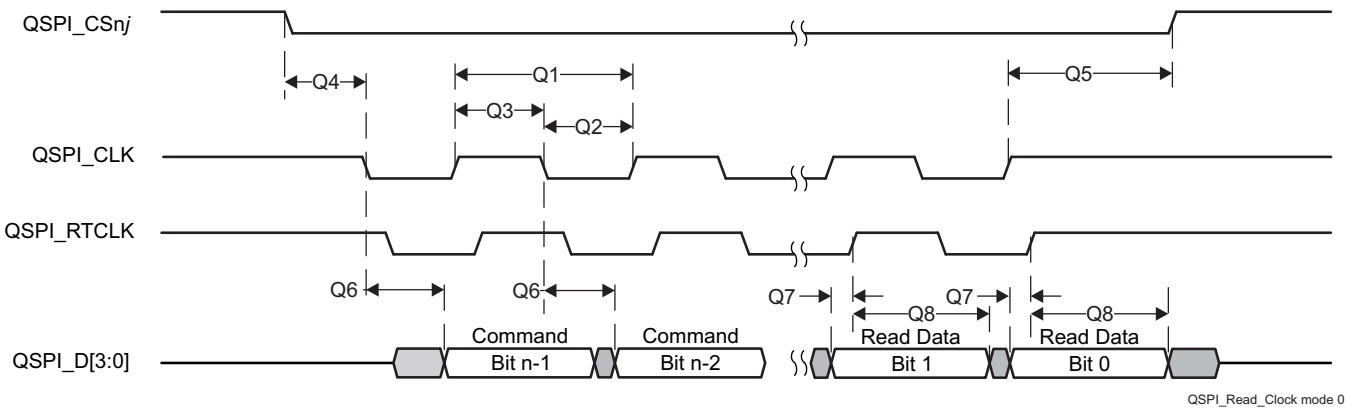

Figure 5-82. QSPI Read (Mode [3:0])

Table 5-90. Switching Characteristics for QSPI

NO.	PARAMETER		MIN	MAX	UNIT
Q1	$t_{c(CLK)}$	Cycle time, QSPI_CLK	10.42[1]		ns
Q2	$t_{w(CLK\ L)}$	Pulse duration, QSPI_CLK low	0.48 × P[2]		ns
Q3	$t_{w(CLK\ H)}$	Pulse duration, QSPI_CLK high	0.48 × P[2]		ns
Q4	$t_{d(CSn-CLK)}$	Delay time, QSPI_CSn active edge to QSPI_CLK transition	5.00		ns
Q5	$t_{d(CLK-CSn)}$	Delay time, QSPI_CLK transition to QSPI_CSn inactive edge	5.00		ns
Q6	$t_{d(CLK-D0)}$	Delay time, QSPI_CLK active edge to QSPI_D[0] transition	0	2	ns

(1) Maximum supported frequency is 96 MHz (Mode 0 only).

(2) P = QSPI_CLK period.

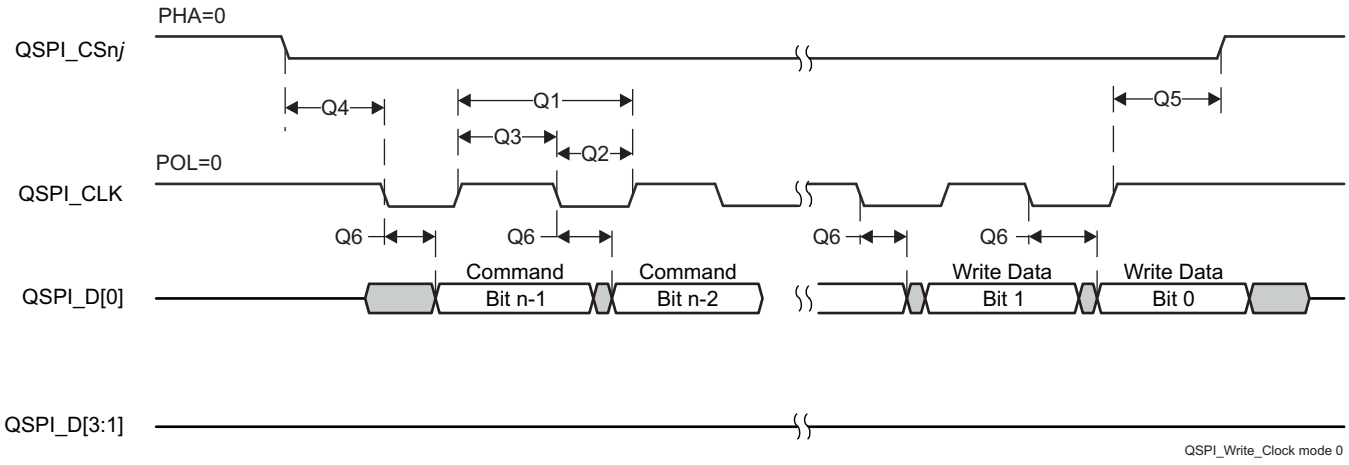

Figure 5-83. QSPI Write (Mode [3:0])

For more information, see section *Quad Serial Peripheral Interface (QSPI)* in chapter *Peripherals* of the Device TRM.

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5.9.4.14 SPI

For more details about features and additional description information on the device Serial Port Interface, see the corresponding sections within Section 4.3, *Signal Descriptions* and Section 6, *Detailed Description*.

For more information, see section *Serial Peripheral Interface (SPI)* in chapter *Peripherals* of the Device TRM.

5.9.4.14.1 SPI—Slave Mode

Table 5-91, Table 5-92, Figure 5-84, and Figure 5-85 present Timing Requirements for SPI - Slave Mode.

Table 5-91. Timing Requirements for SPI Input Timings—Slave Mode

NO.	PARAMETER		MIN	MAX	UNIT
S1	$t_{c(SPICLK)}$	Cycle time, SPI_CLK	40		ns
S2	$t_{w(SPICLKL)}$	Typical Pulse duration, SPI_CLK low	0.45P(1)	0.45P(1)	ns
S3	$t_{w(SPICLKH)}$	Typical Pulse duration, SPI_CLK high	0.45P(1)	0.45P(1)	ns
S4	$t_{su(SIMO-SPICLK)}$	Setup time, SPI_D[x] (SIMO) valid before SPI_CLK active edge(2)(3)	2		ns
S5	$t_{h(SPICLK-SIMO)}$	Hold time, SPI_D[x] (SIMO) valid after SPI_CLK active edge(2)(3)	2		ns
S8	$t_{su(CS-SPICLK)}$	Setup time, SPI_CS valid before SPI_CLK first edge(2)	2		ns
S9	$t_{h(SPICLK-CS)}$	Hold time, SPI_CS valid after SPI_CLK last edge(2)	2		ns
	$t_{d(CS-SPICLK)}$	Required delay from SPIx_CS asserted at slave to first SPI_CLK edge at slave. Phase = 0	C + 5(4)		ns
	$t_{d(CS-SPICLK)}$	Required delay from SPIx_CS asserted at slave to first SPI_CLK edge at slave. Phase = 1	A + 5(4)		ns
	$t_{d(SPICLK-CS)}$	Required delay from final SPI_CLK edge before SPI_CS is deasserted at slave. Phase = 0	G + 5(4)		ns
	$t_{d(SPICLK-CS)}$	Required delay from final SPI_CLK edge before SPI_CS is deasserted at slave. Phase = 1	E + 5(4)		ns
	$t_{d(CSH-SPCN)}$	Minimum delay from slave deselected (SPI_CS deasserted) to SPI_CLK edge (for another slave on the bus)	C + 5(4)		ns

(1) P = SPI_CLK period.

(2) This timing applies to all configurations regardless of SPIx_CLK polarity and which clock edges are used to drive output data and capture input data.

(3) Pins SPIx_D0 and SPIx_D1 can function as SIMO or SOMI.

(4) A = (2 × P2) + (0.5 × SPI_CLK)
C = (2 × P2)
E = (1 × P2)
G = (1 × P2) + (0.5 × SPI_CLK)
P2 = 1 / (SYSCLK1 / 6)

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Table 5-92. Switching Characteristics for SPI Output Timings—Slave Mode

NO.	PARAMETER		MIN	MAX	UNIT
S6	$t_{d(SPICLK-SOMI)}$	Delay time, SPI_CLK active edge to SPI_D[x] (SOMI) transition(1)(2)	0	12	ns
S7	$t_{ena(CS-SOMI)}$	Delay from master asserting SPIx_CS to slave driving SPIx_SOMI valid(2)	0	5	ns
S10	$t_{dis(CS-SOMI)}$	Delay from master deasserting SPIx_CS to slave 3-stating SPIx_SOMI(2)	1 x P2(3)	1 x P2(3) + 5	ns

(1) This timing applies to all configurations regardless of SPIx_CLK polarity and which clock edges are used to drive output data and capture input data.

(2) Pins SPIx_D0 and SPIx_D1 can function as SIMO or SOMI.

(3) P2 = 1 / (SYSCLK1 / 6).

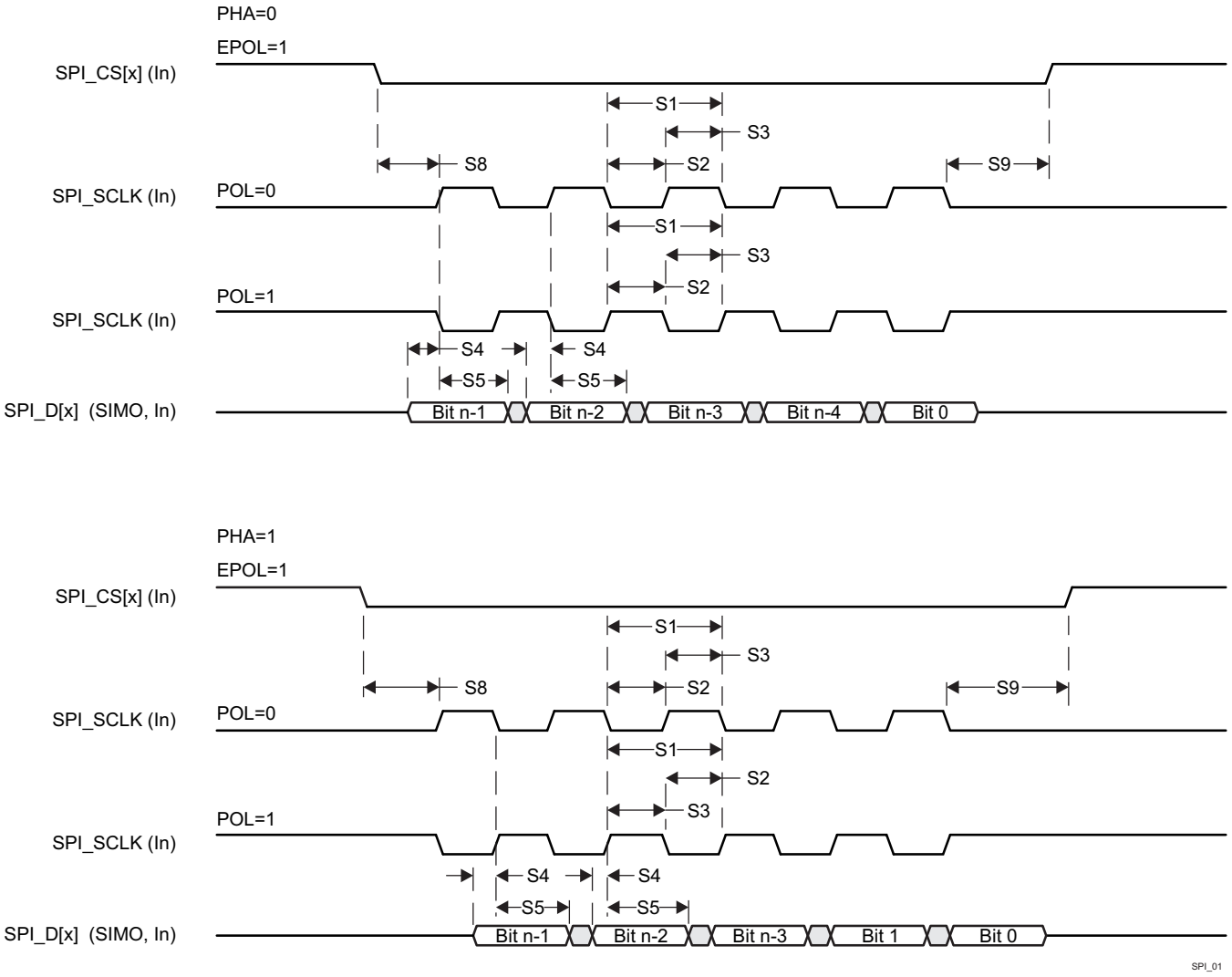

Figure 5-84. SPI Slave Mode Receive Timing

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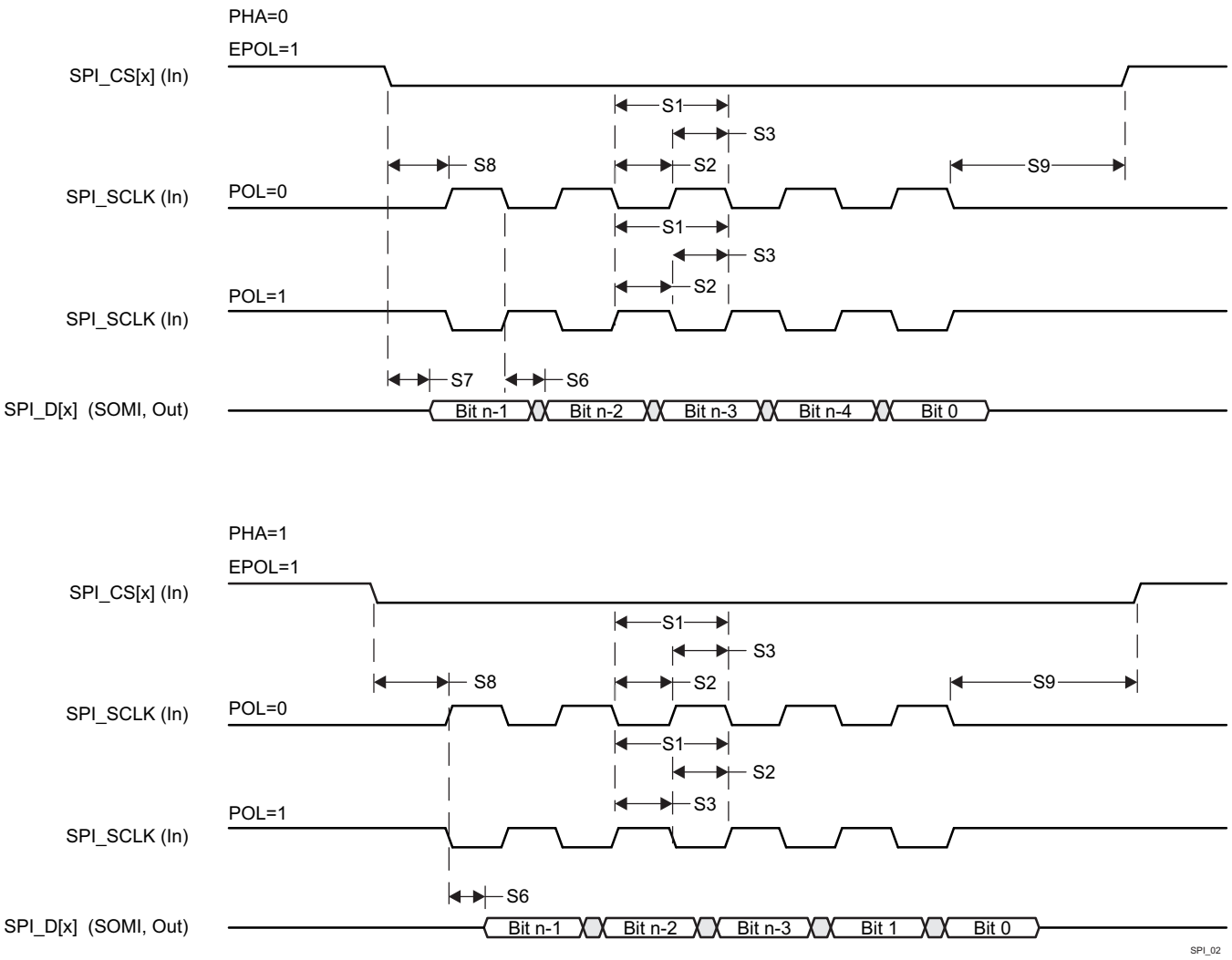

Figure 5-85. SPI Slave Mode Transmit Timing

5.9.4.14.2 SPI—Master Mode

Table 5-94, Table 5-95, Figure 5-86 and Figure 5-87 present Timing Requirements for SPI - Master Mode.

Table 5-93. SPI Timing Conditions—Master Mode

PARAMETER		MIN	MAX	UNIT
Input Conditions				
t_r	Input signal rise time		4	ns
t_f	Input signal fall time		4	ns
Output Condition				
C_{load}	Output load capacitance		20	pF

Table 5-94. Timing Requirements for SPI Input Timings—Master Mode

NO.	PARAMETER		MIN	MAX	UNIT
S4	$t_{su(SOMI-SPICLK)}$[1]	Setup time, SPI_D[x] (SOMI) valid before SPI_CLK active edge[2]	3		ns
S5	$t_{h(SPICLK-SOMI)}$[1]	Hold time, SPI_D[x] (SOMI) valid after SPI_CLK active edge[2]	2		ns

(1) This timing applies to all configurations regardless of SPIx_CLK polarity and which clock edges are used to capture input data.

(2) Pins SPIx_D0 and SPIx_D1 can function as SIMO or SOMI.

Table 5-95. Switching Characteristics for SPI Output Timings—Master Mode

NO.	PARAMETER			MIN	MAX	UNIT
S1	$t_{c(SPICLK)}$	Cycle time, SPI_CLK		20[5]		ns
S2	$t_{w(SPICLKL)}$	Typical Pulse duration, SPI_CLK low		0.45P[1]	0.45P[1]	ns
S3	$t_{w(SPICLKH)}$	Typical Pulse duration, SPI_CLK high		0.45P[1]	0.45P[1]	ns
S3R	$t_{r(SPICLK)}$	Rising time, SPI_CLK			5	ns
S3F	$t_{f(SPICLK)}$	Falling time, SPI_CLK			5	ns
S6	$t_{d(SPICLK-SIMO)}$	Delay time, SPI_CLK active edge to SPI_D[x] (SIMO) transition[2]		-2	2	ns
S8	$t_{d(CS-SPICLK)}$	Delay time, SPI_CS active to SPI_CLK first edge	Mode 1 and 3[3]	A - 5[4]	B + 5[4]	ns
			Mode 0 and 2[3]	C - 5[4]	D + 5[4]	ns
S9	$t_{d(SPICLK-CS)}$	Delay time, SPI_CLK last edge to SPI_CS inactive	Mode 1 and 3[3]	E - 5[4]	F + 5[4]	ns
			Mode 0 and 2[3]	G - 5[4]	H + 5[4]	ns

(1) P = SPI_CLK period.

(2) Pins SPIx_D0 and SPIx_D1 can function as SIMO or SOMI.

(3) The polarity of SPIx_CLK and the active edge (rising or falling) on which spix_simo is driven and spix_somi is latched is all software configurable:
- PHASE = 1 Mode 3 and Mode 1.
- PHASE = 0 Mode 2 and Mode 0.

(4) A = (2 × P2) + (0.5 × SPI_CLK)
B = (2 × P2) + (C2TDELAY +1) × P2) + (0.5 × SPI_CLK)
C = (2 × P2)
D = (2 × P2) + (C2TDELAY +1) × P2)
E = (1 × P2)
F = (1 × P2) + ((T2CDELAY+1) × P2)
G = (1 × P2) + (0.5 × SPI_CLK)
H = (1 × P2) + ((T2CDELAY+1) × P2) + (0.5 × SPI_CLK)
P2 = 1/(SYSCLK1 / 6)

(5) Minimum clock period is dependent on SYSCLK1 and SPI module prescaler settings and may be higher than shown in the table.

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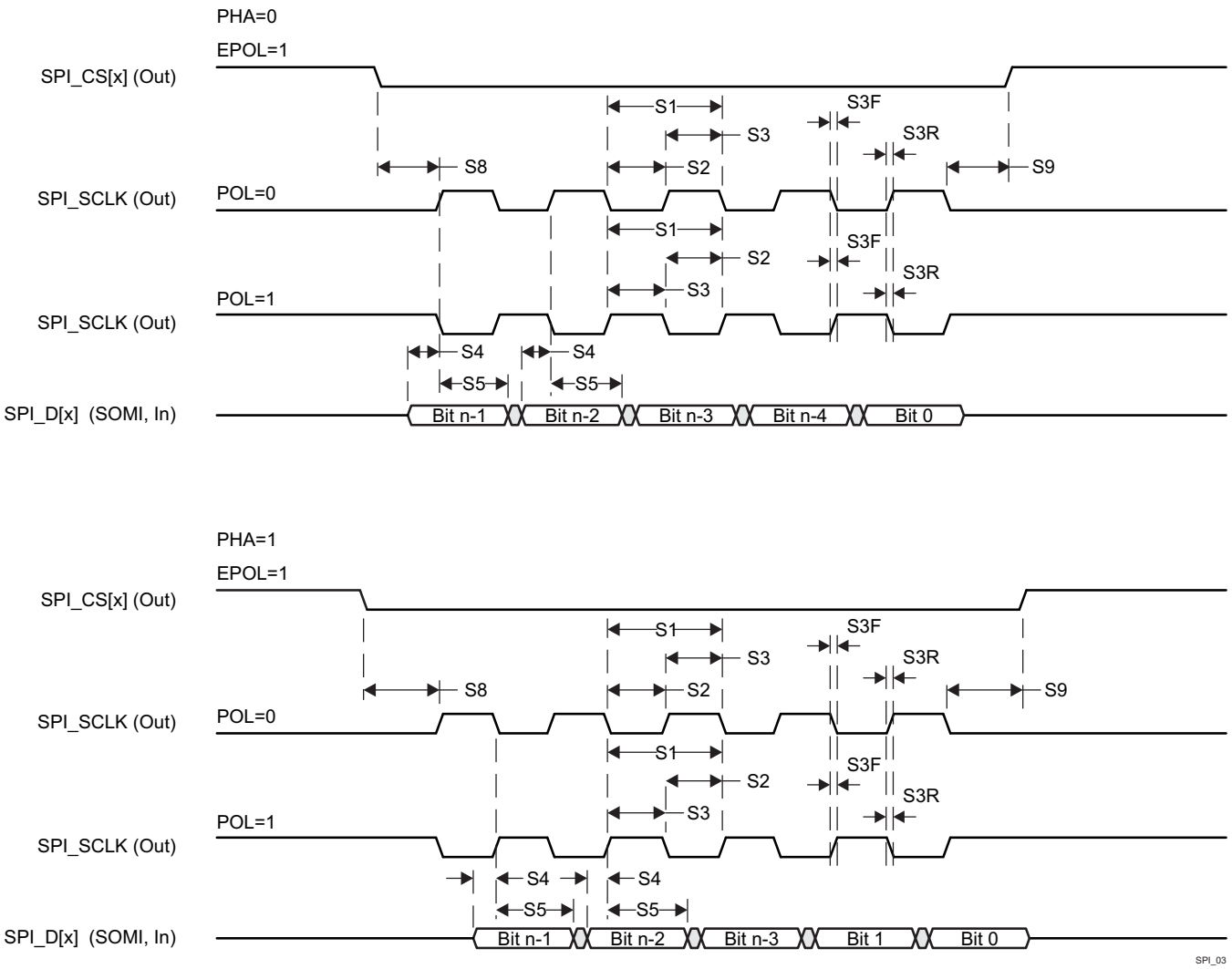

Figure 5-86. SPI Master Mode Receive Timing

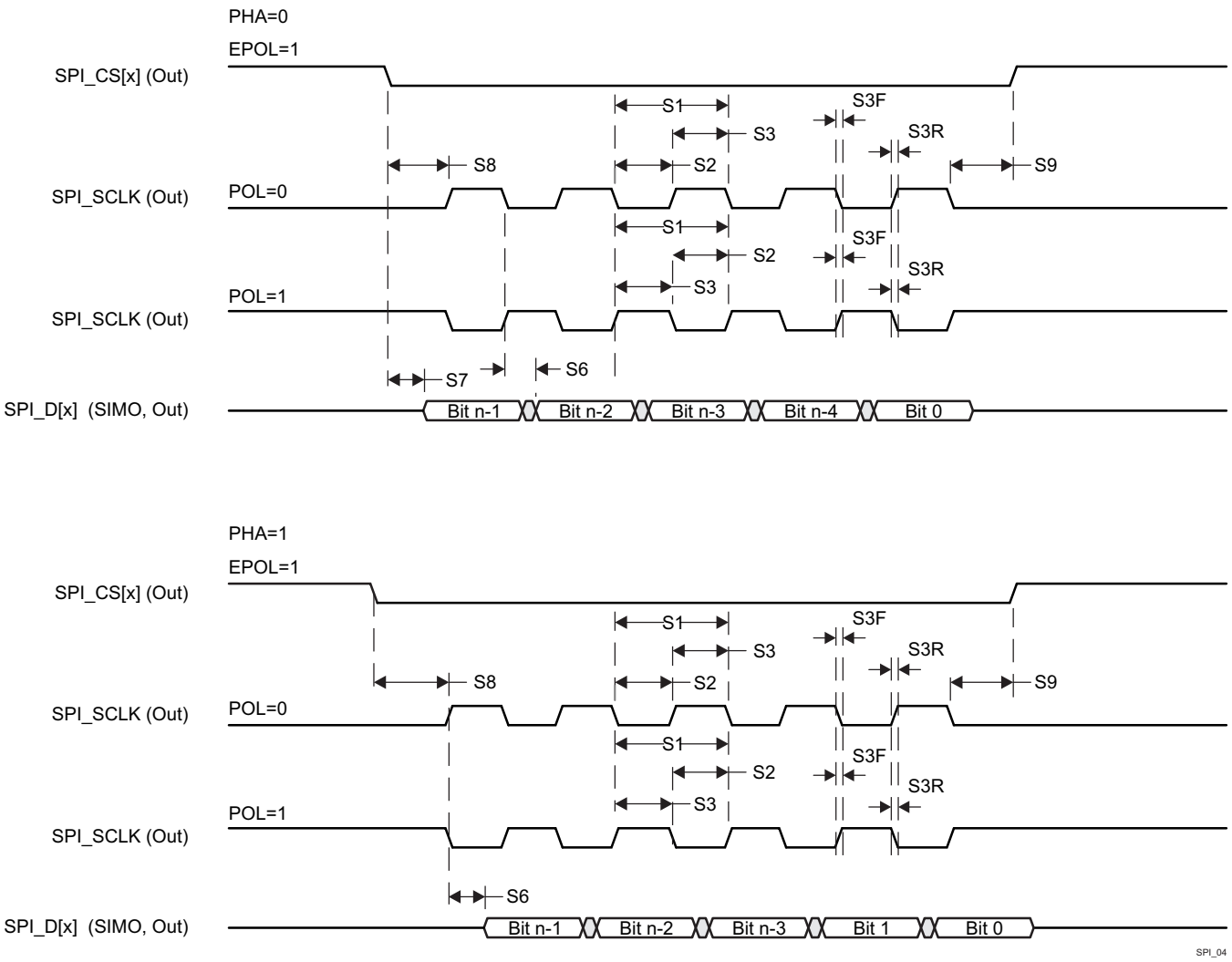

Figure 5-87. SPI Master Mode Transmit Timing

5.9.4.15 Timers

For more details about features and additional description information on the device Timers, see the corresponding sections within Section 4.3, *Signal Descriptions* and Section 6, *Detailed Description*.

Table 5-96. Timer Input Timing Requirements

NO.	PARAMETER		MIN	MAX	UNIT
T1	$t_{w(TINPH)}$	Pulse duration, high	12C(1)		ns
T2	$t_{w(TINPL)}$	Pulse duration, low	12C(1)		ns

(1) C=1/SYSCLK1 in ns. SYSCLK1 clock is sourced from the main PLL.

Table 5-97. Timer Output Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
T3	$t_{w(TOUTH)}$	Pulse duration, high	12C(1) - 3		ns
T4	$t_{w(TOUTL)}$	Pulse duration, low	12C(1) - 3		ns

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(1) C=1/SYSCLK1 in ns. SYSCLK1 clock is sourced from the main PLL.

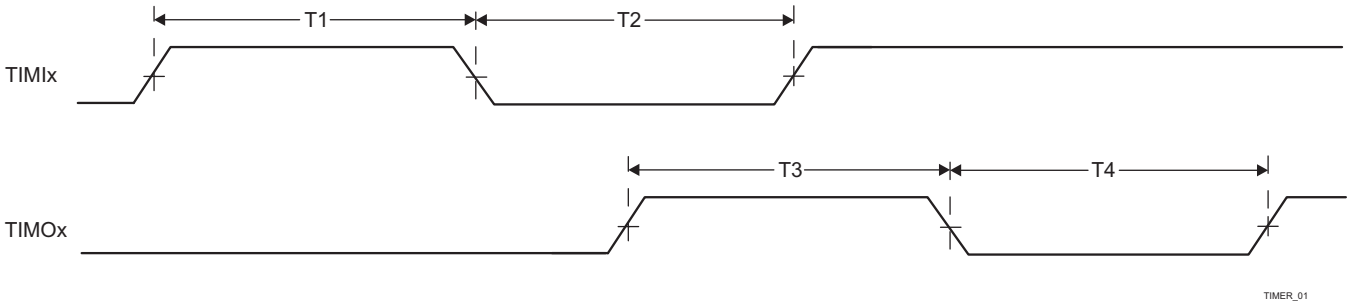

Figure 5-88. Timer Timing

For more information, see section *Timers* in chapter *Peripherals* of the Device TRM.

5.9.4.16 UART

For more details about features and additional description information on the device Universal Asynchronous Receiver Transmitter, see the corresponding sections within Section 4.3, *Signal Descriptions* and Section 6, *Detailed Description*.

Table 5-98, Figure 5-89, and Figure 5-92 present Timing Requirements for UART interface.

Table 5-98. Timing Requirements for UART

NO.			MIN	MAX	UNIT
Receive Timing					
U4	$t_{w(RXSTART)}$	Pulse width, receive start bit	0.96U(1)	1.05U(1)	ns
U5	$t_{w(RXH)}$	Pulse width, receive data/parity bit high	0.96U(1)	1.05U(1)	ns
	$t_{w(RXL)}$	Pulse width, receive data/parity bit low	0.96U(1)	1.05U(1)	ns
U6	$t_{w(RXSTOP)}$	Pulse width, receive stop bit	0.96U(1)	1.05U(1)	ns

(1) U = UART baud time = 1 / programmed baud rate.

(2) P = 1/(SYSCLK1/6). SYSCLK1 clock is sourced from the main PLL.

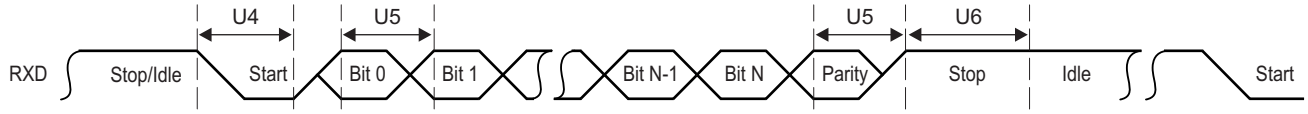

Figure 5-89. UART Receive Timing Waveform

Table 5-99, Figure 5-90, and Figure 5-91 present Switching Characteristics for UART interface.

Table 5-99. Switching Characteristics Over Recommended Operating Conditions for UART

NO.	PARAMETER		MIN	MAX	UNIT
Transmit Timing					
U1	$t_{w(TXSTART)}$	Pulse width, transmit start bit	U(1) - 2	U(1) + 2	ns
U2	$t_{w(TXH)}$	Pulse width, transmit data/parity bit high	U(1) - 2	U(1) + 2	ns
	$t_{w(TXL)}$	Pulse width, transmit data/parity bit low	U(1) - 2	U(1) + 2	ns
U3	$t_{w(TXSTOP1)}$	Pulse width, transmit stop bit 1	U(1) - 2	U(1) + 2	ns
	$t_{w(TXSTOP15)}$	Pulse width, transmit stop bit 1.5	1.5U(1) - 2	1.5U(1) + 2	ns
	$t_{w(TXSTOP2)}$	Pulse width, transmit stop bit 2	2U(1) - 2	2U(1) + 2	ns
Autoflow Timing Requirements					
U7	$t_{d(RX-RTSH)}$	Delay time, STOP bit received to RTS deasserted	P(2)	5P(2)	ns
U8	$t_{d(CTSL-TX)}$	Delay time, CTS asserted to START bit transmit	P(2)	5P(2)	ns

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(1) U = UART baud time = 1 / programmed baud rate.
(2) P = 1/(SYSCLK1/6). SYSCLK1 clock is sourced from the main PLL.

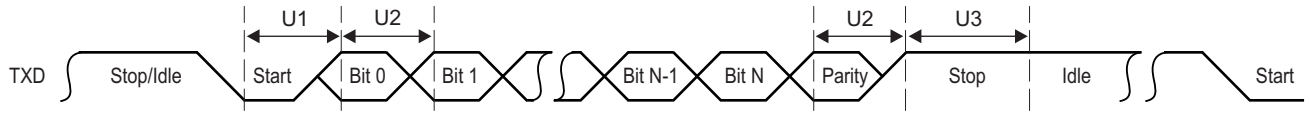

Figure 5-90. UART Transmit Timing Waveform

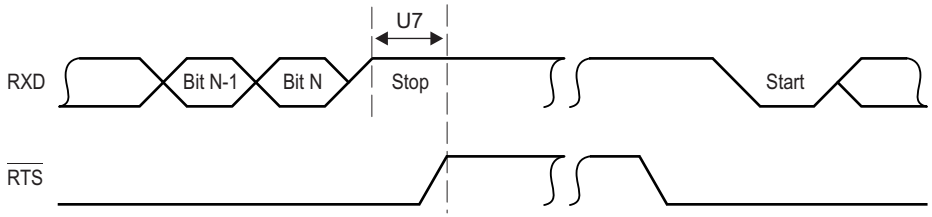

Figure 5-91. UART RTS (RXD Stop to RTS Output) – Autoflow Timing Waveform

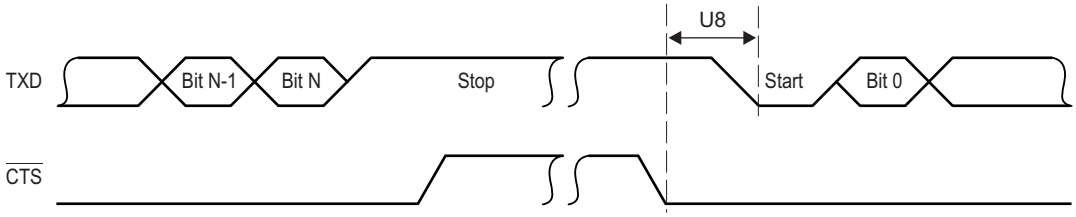

Figure 5-92. UART CTS (CTS to TXD Start Output) — Autoflow Timing Waveform

For more information, see section *Universal Asynchronous Receiver/Transmitter (UART)* in chapter *Peripherals* of the Device TRM.

5.9.4.17 USB

The USB 2.0 subsystem is fully-compliant with the Universal Serial Bus (USB) Specification, revision 2.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Universal Serial Bus Subsystem (USB), see the corresponding sections within Section 4.3, *Signal Descriptions* and Section 6, *Detailed Description*.

For more information, see section *Universal Serial Bus Subsystem (USB)* in chapter *Peripherals* of the Device TRM.

5.9.5 Emulation and Debug Subsystem

5.9.5.1 IEEE 1149.1 Standard-Test-Access Port (JTAG)

For more details about features and additional description information on the device IEEE 1149.1 Standard-Test-Access Port, see the corresponding sections within Section 4.3, *Signal Descriptions* and Section 6, *Detailed Description*.

5.9.5.1.1 JTAG Electrical Data and Timing

Table 5-100, Table 5-101, and Figure 5-93 assume testing over the recommended operating conditions and electrical characteristic conditions.

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Table 5-100. Timing Requirements for IEEE 1149.1 JTAG

NO.			MIN	MAX	UNIT
J1	$t_{c(TCK)}$	Cycle time, TCK	23		ns
J1H	$t_{w(TCKH)}$	Pulse duration, TCK high (40% of t_c)	9.2		ns
J1L	$t_{w(TCKL)}$	Pulse duration, TCK low(40% of t_c)	9.2		ns
J3	$t_{su(TDI-TCK)}$	Input setup time, TDI valid to TCK high	2		ns
	$t_{su(TMS-TCK)}$	Input setup time, TMS valid to TCK high	2		ns
J4	$t_{h(TCK-TDI)}$	Input hold time, TDI valid from TCK high	10		ns
	$t_{h(TCK-TMS)}$	Input hold time, TMS valid from TCK high	10		ns

Table 5-101. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG

NO.	PARAMETER		MIN	MAX	UNIT
J2	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid		8.24	ns

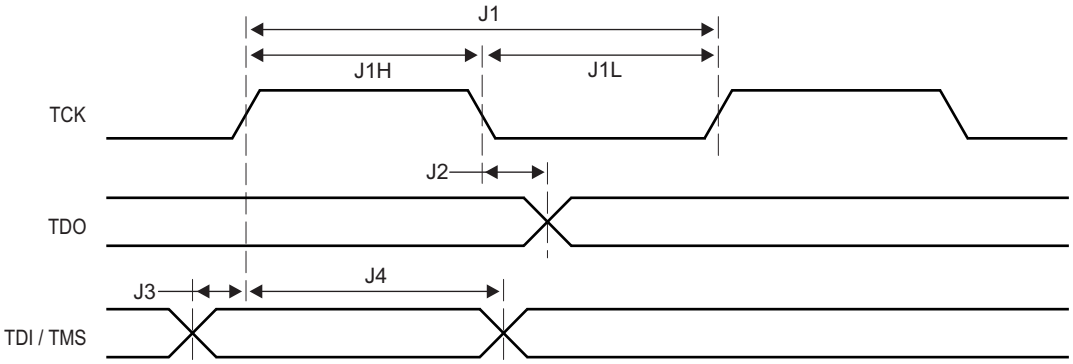

Figure 5-93. JTAG Test-Port Timing

6 Detailed Description

6.1 Overview

The SoC is a low-cost, low-power device based on TI KeyStone II (KS2) Multicore SoC architecture. It is optimized to achieve better power efficiency at similar performance compared to the preceding devices in the KS2 family. In addition to cost and power optimization, the device also integrates peripherals that facilitate industrial communications, control and performance audio applications. It incorporates the performance-optimized Cortex-A15 and a C66x DSP core, built to meet the processing and system-level integration needs enterprise media gateway, focused end equipment (FEE), and broad-market applications (software-defined radio (SDR), ProAudio, emerging equipment that requires a low-power A15 or C66-class SoC).

NOTE

For more information on features, subsystems, and architecture of superset System on Chip (SoC), see the Device TRM.

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6.2 Functional Block Diagram

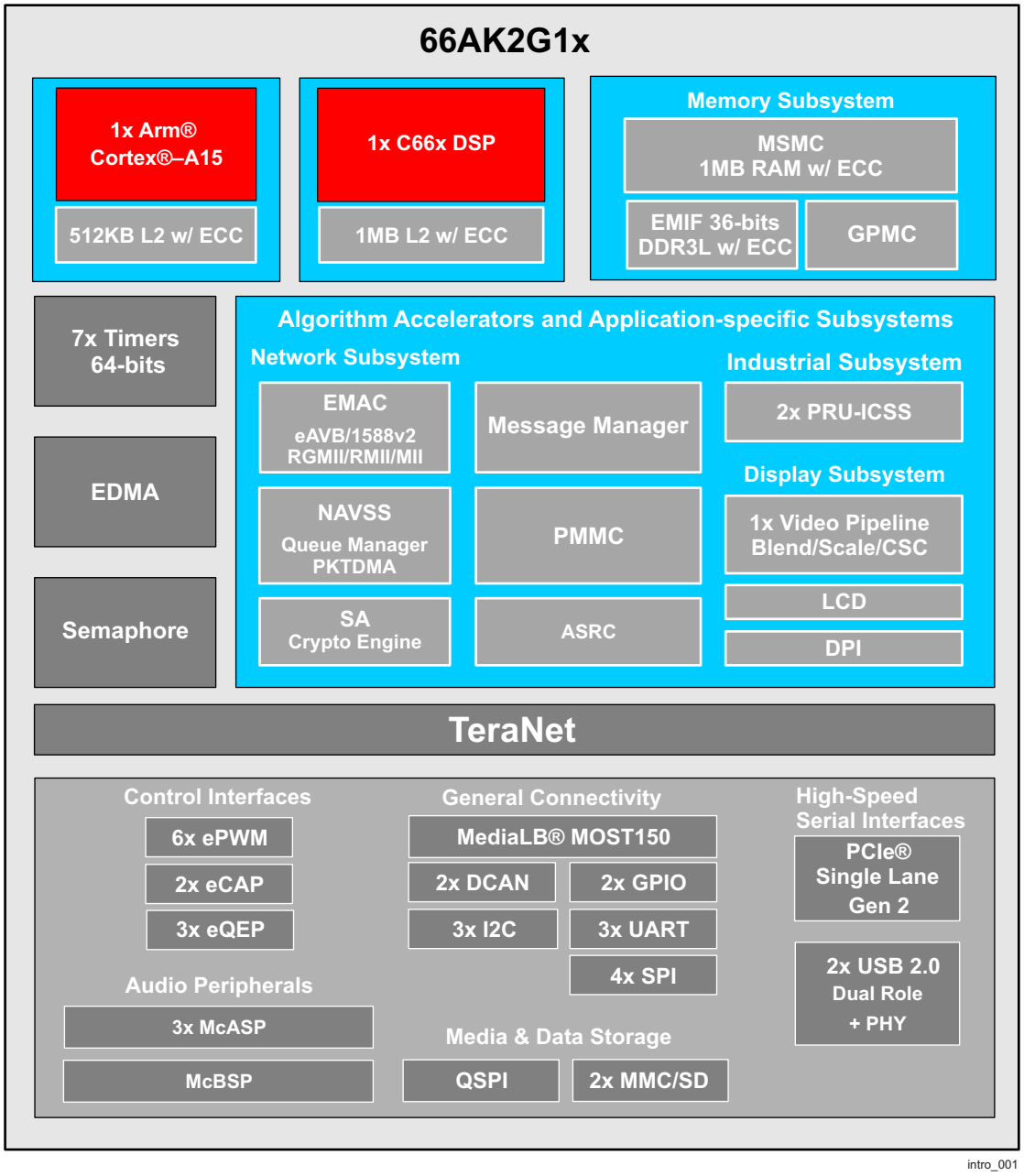

Figure 6-1. Functional Block Diagram

6.3 Arm A15

The Arm Subsystem (ARMSS) of the SoC integrates a single Cortex-A15 processor with additional logic for bus protocol conversion, local power management, and various debug and trace enhancements.

The Cortex-A15 processor is an Armv7A-compatible, multi-issue out-of-order superscalar execution engine with integrated L1 caches.

The implementation also supports advanced SIMDv2 (NEON™ technology) and VFPv4 (vector floating point) architecture extensions, security, virtualization, LPAE (large physical address extension), and multiprocessing extensions.

The Arm Subsystem includes a 512KB L2 cache and support for AMBA4 AXI and AXI coherence extension (ACE) protocols.

NOTE

The **Arm Subsystem** is also referred to as **Arm CorePac**.

The Arm subsystem supports the following key features:

- Arm Cortex-A15 processor, full implementation of Armv7-A architecture instruction set
- 32KB L1 instruction (L1I) and data (L1D) caches
- 512KB L2 cache
- Super scalar, variable-length, out-of-order pipeline (12 stage in-order, 3-12 stage out-of-order)
- 128-bit instruction fetch
- 3-wide instruction decode
- 3-wide instruction dispatch
- 8-wide instruction issue
- Dynamic branch prediction with Branch Target Buffer (BTB) and Global History Buffer (GHB), a return stack, and an indirect predictor
- Integrated Neon and VFP (Vector Floating Point unit)
- Support for security and virtualization extensions
- Error Correction Code (ECC) protection for L1 data cache and L2 cache, parity protection for L1 instruction cache
- 32-entry fully-associative L1 Translation Look-aside Buffers (TLBs), for instruction fetch, data loads, and data stores
- 512-entry 4-way set-associative L2 TLB
- AMBA 4.0 AXI Coherency Extension (ACE) master port which is directly connected to MSMC (Multicore Shared Memory Controller) for low-latency access to shared MSMC SRAM
- Dedicated Arm clocking (ARM_PLL) for full flexibility in performance trade-offs
- Support for four integrated generic timers, in addition to 1 dedicated SoC-level watchdog timer (TIMER_5)
- Support for invasive (stop-mode) and non-invasive (tracing, performance monitoring) debug modes and cross triggering for multiprocessor debugging
- Support for processor instruction trace using Program Trace Macrocell (PTM) and data trace (printf style debug) using System Trace Macrocell (STM)
- Support for up to 480 interrupt requests via the Arm Interrupt Controller (AINTC) module

The Arm subsystem does not support the following features:

- ACP (Accelarator Coherancy Port) Slave
- Native AXI Master interface (only MSMC option is used)

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The Arm subsystem integrates the following major blocks:

- Single-core Arm Cluster
- AXI2VBUS_MASTER
- Debug and Trace components
- ARM_VBUSP registers
- AINTC
- Global Timebase Counter (GTC)
- Various interfaces for interaction with other SoC subsystems and modules

  For more information, see section *Arm Cortex-A15 Subsystem* in chapter *Processors and Accelerators* of the Device TRM.

6.4 C66x DSP Subsystem

The C66x DSP is the next-generation fixed-point and floating-point DSP. The new DSP enhances the C674x, which merged the C67x+ floating point and the C64x+ fixed-point instruction set architectures. The C66x DSP is object-code compatible with the C64x+ and C674x DSP.

The DSP sybsystem (C66x CorePac) supports the following key features:

- Fixed/Floating-point C66x CPU based on a superset of the C64x+ and C67x+ ISA
- Program Memory Controller (PMC):
  - 32KB Level 1 Program (L1P) Cache/SRAM
- Data Memory Controller (DMC):
  - 32KB L1 Data (L1D) Cache/SRAM
- Unified Memory Controller (UMC):
  - 1024KB L2 Cache/SRAM
- External Memory Controller (EMC):
  - Internal DMA (IDMA) engine
  - One 128-bit VBUSM slave port from TeraNet_DMA
  - One 32-bit VBUSP master port to TeraNet_CFG
- XMC (Extended Memory Controller):
  - One 256-bit port to MSMC controller
- Multistream prefetch buffer
- Address extension/translation (32-bit to 36-bit)
- Memory protection for multiple segments
- Memory protection for all internal L1/L2 RAM
- Error Detection for L1P
- Error Detection and Correction for L1D
- Error Detection and Correction for all L2
- Integrated C66x CorePac interrupt controller (INTC) that works in conjunction with Chip-level Interrupt Controller (CIC) for distribution of system interrupts to the C66x core. Interrupts can be routed directly to the C66x core or through the CIC module in a flexible manner
- Integrated leakage and dynamic power management
- Debug/emulation capabilities:
  - Support for halt mode, real time and monitor mode debug capabilities
  - Support for processor instruction trace and system trace (**printf**-style debug)
- Dedicated timer module (TIMER_0) for the C66x CorePac, integrated at SoC level. TIMER_0 can be used as either general-purpose timer or watchdog timer

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Fore more information about:

- C66x CorePac, see the *TMS320C66x DSP CorePac User's Guide* (SPRUGW0).
- C66x CPU core, see the *TMS320C66x DSP CPU and Instruction Set Reference Guide* (SPRUGH7).
- C66x cache memory system, see the *TMS320C66x DSP Cache User's Guide* (SPRUGY8).
- C66x debug/trace support, see chapter *On-chip Debug* of the Device TRM.

6.5 C66x Cache Subsystem

The purpose of this section is to provide an overview of the C66x cache memory architecture and to specify its configuration in this device. Details on the C66x cache functionality can be found in the *TMS320C66x DSP Cache User Guide* (SPRUGY8).

The device contains a 1024KB level-2 memory (L2), a 32KB level-1 program memory (L1P), and a 32KB level-1 data memory (L1D). Each memory has a unique location in the memory map (see chapter *Memory Map* of the Device TRM).

After device reset, L1P and L1D cache are configured as all cache, by default. The L1P and L1D cache can be reconfigured via software through the L1PMODE field of the L1P Configuration Register (L1PMODE) and the L1DMODE field of the L1D Configuration Register (L1DCFG) of the C66x CorePac. L1D is a two-way set-associative cache, while L1P is a direct-mapped cache.

For more information, see section *C66x Cache Subsystem* in chapter *Processors and Accelerators* of the Device TRM.

6.6 PRU-ICSS

The Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS) consists of:

- Two 32-bit load/store RISC CPU cores — Programmable Real-Time Units (PRU0 and PRU1)
- Data RAMs per PRU core
- Instruction RAMs per PRU core
- Shared RAM
- Peripheral modules
- Interrupt controller (ICSS_INTC).

The programmable nature of the PRU cores, along with their access to pins, events and all device resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores of the device.

The device has integrated two identical PRU subsystems (PRU-ICSS_0 and PRU-ICSS_1).

The PRU cores within each PRU-ICSS have access to all resources on the SoC through the Interface Master port, and the external host processors can access the PRU-ICSS resources through the Interface Slave port. The 32-bit interconnect bus connects the various internal and external masters to the resources inside the PRU-ICSS. The PRU cores within the subsystems also have access to all resources on the SoC through the TeraNet DMA Interconnect. A subsystem local Interrupt Controller — ICSS_INTC handles system input events and posts events back to the device-level host CPUs.

The PRU cores are programmed with a small, deterministic instruction set. Each PRU can operate independently or in coordination with each other and can also work in coordination with the device-level host CPU. This interaction between processors is determined by the nature of the firmware loaded into the PRU's instruction memory.

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The PRU subsystem includes the following main features:

- Two PRU CPUs:
  - 20 Enhanced General-Purpose Inputs (EGPI) and 20 Enhanced General-Purpose Outputs (EGPO)
  - Asynchronous capture [Serial Capture Unit (SCU)] with EnDat 2.2 protocol and Sigma-Delta demodulation support
    NOTE: There is no Sigma-Delta modulator inside the PRU. However, Sigma-Delta support is enabled through digital filtering hardware in the PRU to perform Sinc filtering.
  - Multiplier with accumulation (MAC)
  - CRC16 and CRC32 HW accelerator
  - 16-KB program RAM per PRU CPU (signified IRAM0 for PRU0 and IRAM1 for PRU1) with ECC
  - 8-KB data RAM per PRU CPU (signified RAM0 for PRU0 and RAM1 for PRU1) with ECC
  - Two high-performance master (initiator) ports on the TeraNet_DMA interconnect — one per PRU
- 64-KB general purpose memory RAM (signified RAM2) with ECC, shared between PRU0 and PRU1
- One Scratch-Pad (SPAD) memory:
  - 3 Banks of 30 × 32-bit registers
- Broadside direct connect between PRU cores within subsystem. Optional address translation for PRU transaction to External Host
- 16 software events generated by two PRUs
- One Ethernet MII_RT module (ICSS_MII_RT_CFG) with two MII ports and configurable connections to PRUs
- One MDIO Port (ICSS_MII_MDIO) to control external Ethernet PHY
- One Industrial Ethernet Peripheral (IEP) to manage/generate Industrial Ethernet functions:
  - One Industrial Ethernet 64-bit timer with 9 capture and 16 compare events with slow and fast compensation
- 16550-compatible UART with a dedicated 192-MHz clock to support 12-Mbps PROFIBUS
- Enhanced Capture Module (eCAP_0)
- Interrupt Controller (ICSS_INTC):
  - Up to 64 input events supported
  - Supports up to to 10 interrupt channels
  - Generation of 10 Host interrupts: 2 Host interrupts to PRU0 and PRU1, 1 Host interrupt to PRU-ICSS_0 and PRU-ICSS_1, 7 Host interrupts exported from the ICSS for signaling the Arm interrupt controllers (pulse and level provided)
  - Each system event can be enabled and disabled
  - Each host event can be enabled and disabled
  - Hardware prioritization of events
- One 32-bit VBUSP slave (target) port for memory mapped register and internal memories access
- Two (master and slave) 32-bit VBUSP ports for low-latency interface between PRU-ICSS subsystems
- Flexible power management support
- Integrated 32-bit interconnect
- All memories support ECC

  For more information, see section *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)* in chapter *Processors and Accelerators* of the Device TRM.

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6.7 Memory Subsystem

6.7.1 MSMC

The Multicore Shared Memory Controller (MSMC) manages traffic among the device ARMSS, DSP, DMA, other master peripherals, and the DDR EMIF controller. It also provides a shared on-chip SRAM that is accessible by the ARMSS, DSP and the master peripherals in the device.

The MSMC module has the following features:

- CPU/1 frequency of operation (that is, frequency same as that of the ARMSS/DSP)
- One 256-bit master interface for connection to external SDRAM (through DDR EMIF controller)
- One 256-bit master interface for connection to TeraNet_DMA
- One 256-bit slave interface for the DSP
- One 256-bit slave interface for the ARMSS
- One 256-bit slave interface for accesses to the shared SRAM
- One 256-bit slave interface for accesses to the external SDRAM
- Memory protection for accesses to both the shared SRAM and external SDRAM spaces
- Address extension from 32-bit to 36-bit for larger addressing space
- Error Detection and Correction (EDC) and scrubbing support for the MSMC SRAM
- Level 2 or Level 3 shared SRAM that is accessible by the device ARMSS, DSP and the master peripherals
- Coherency between ARMSS L1/L2 cache and EDMA/system master peripherals (through SES/SMS ports) in the SRAM space and SDRAM space

For more information, see section *Multicore Shared Memory Controller (MSMC)* in chapter *Memory Subsystem* of the Device TRM.

6.7.2 DDR EMIF

This section describes the DDR External Memory Interface (EMIF) for the device.

The DDR EMIF controller supports:

- DDR3L Memory device compliant to JEDEC JESD79-3F and JESD79-3-1 (DDR3L addendum) standards
- 16-bit and 32-bit SDRAM data bus without ECC
- 32-bit SDRAM data bus with 4-bit ECC
- CAS latencies of 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, and 16
- CAS write latencies of 5, 6, 7, 8, 9, 10, 11, and 12
- 1, 2, 4, and 8 internal banks
- Burst length of 8
- Sequential burst type
- 4GB address space available over one chip select
- 33-bit system address for address space of 4GB
- Page sizes with 256, 512, 1024, and 2048 words
- Self-refresh mode
- Power-down mode
- Output impedance calibration
- On-Die Termination (ODT)
- Prioritized refresh scheduling
- Programmable SDRAM refresh rate and backlog counter
- Programmable SDRAM timing parameters
- Only little endian mode

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- ECC on SDRAM data bus:
  - 8-bit ECC per 64-bit data quanta without additional cycle latency
  - 1-bit correction and 2-bit detection
  - Statistics for 1-bit ECC and 2-bit ECC errors
  - Programmable address ranges to define ECC protected region
  - ECC calculated and stored on all writes to ECC protected address region
  - ECC verified on all reads to ECC protected address region
  - Two ECC modes supported:
    - Read-Modify-Write (RMW) ECC enabled to support sub quanta accesses to the ECC space.
    - RMW ECC disabled
- Class of service
- UDIMM address mirroring.

The DDR EMIF controller does not support:

- Any memory types except DDR3L
- RDIMMs
- ECC for 16-bit mode
- Single ended DQS
- Mixed 8-bit and 16-bit SDRAM configurations
- 4-bit SDRAMs.

For more information, see section *DDR External Memory Interface (EMIF)* in chapter *Memory Subsystem* of the Device TRM.

6.7.3 GPMC

The general-purpose memory controller (GPMC) is a unified memory controller dedicated for interfacing with external memory devices like:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous, and page mode (available only in nonmultiplexed mode) burst NOR flash devices
- Pseudo-SRAM devices

The main features of the GPMC are:

- 8- or 16-bit-wide data path to external memory device
- Supports up to 4 chip select regions of programmable size and programmable base addresses in a total address space of 1 GB
- Fully pipelined operation for optimal memory bandwidth usage
- The clock to the external memory is provided from GPMC_FCLK divided by 1, 2, 3, or 4
- Supports programmable autoclock gating when no access is detected
- Independent and programmable control signal timing parameters for setup and hold time on a per-chip basis. Parameters are set according to the memory device timing parameters with a timing granularity of one GPMC_FCLK clock cycle.
- Flexible internal access time control (wait state) and flexible handshake mode using external WAIT pin monitoring
- Support bus keeping
- Support bus turnaround
- 32-bit TeraNet slave interface which supports non-wrapping and wrapping burst of up to 16 x 32 bits.

The GPMC supports the following various access types:

- Asynchronous read/write access
- Asynchronous read page access (4-, 8-, and 16- Word16)

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- Synchronous read/write access
- Synchronous read/write burst access without wrap capability (4-, 8-, and 16- Word16)
- Synchronous read/write burst access with wrap capability (4-, 8-, and 16- Word16)
- Address-data-multiplexed (AD) access
- Address-address-data (AAD) multiplexed access
- Little-endian access only

The GPMC can communicate with a wide range of external devices:

- External asynchronous or synchronous 8-bit wide memory or device (non burst device)
- External asynchronous or synchronous 16-bit wide memory or device
- External 16-bit nonmultiplexed NOR flash device
- External 16-bit address and data multiplexed NOR Flash device
- External 16-bit pseudo-SRAM (pSRAM) device

For more information, see section *General-Purpose Memory Controller (GPMC)* in chapter *Memory Subsystem* of the Device TRM.

6.8 Interprocessor Communication

6.8.1 MSGMGR

The SoC implements a single instance of the Message Manager to provide inter-processor communication between the various processing units:

- Arm (Cortex-A15)
- DSP (C66x)
- PMMC (CPU)
- PRU-ICSS (PRUs)

The Message Manager is a hardware engine used for queuing messages in a secure and self-contained manner. There is no limitation on the message format or content. It is software responsibility to define the message format.

The Message Manager provides a multi-core and multi-process safe message interface which allows multiple users (message senders and receivers) to access the queues without the need for any mutual exclusion. It also allows for secure and authorized access to the queues.

The general features of the Message Manager module include:

- Provides hardware acceleration for pushing/popping messages to/from logical queues
- Supports the following SoC configuration:
  - 64 queues
  - Up to 128 pending messages
  - 64-byte messages
  - 32 proxies (single proxy per page)
- Support for highly-pipelined push/pop operations
- Support for self-contained mode with zero SW initialization
- Provides a secure front-end for the queues
- Provides flexible message allocation with ability to store the same message multiple times in different queues or multiple times in the same queue
- Queue depth limited only by the maximum number of messages
- Support for little-endian (LE) operation only

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Monitoring and trace functions include:

- Provides hardware signals to monitor the empty status for all transmit source queues
- Provides ability to read Linking RAM contents for debug purposes
- Provides ability to generate an interrupt when there are no free entries in the Linking RAM
- Provides ability to generate an interrupt due to a proxy fault

For more information, see section *Message Manager* in chapter *Interprocessor Communication* of the Device TRM.

6.8.2 SEM

This chapter describes the operation of the Semaphore hardware module. The Semaphore module is accessible across all the cores on a multicore environment. The module supports up to 64 independent semaphores that help the application to implement shared-resource protection mechanism across multiple cores. Each of the semaphores can be accessed by the cores in direct, indirect, or combined modes.

In a multicore environment where system resources must be shared it is important to control simultaneous accesses to the available resources. To ensure correct system operation, it is necessary to limit access to a resource by one and only one core at a time; that is, it is necessary to provide mutual exclusion for resources shared across multiple cores.

The Semaphore module provides a mechanism that applications can use to implement mutual exclusion of shared resources across multiple cores. The following CPU cores can be semaphore masters on this device:

- DSP C66x
- Arm Cortex-A15
- PMMC CPU
- ICSS0_PRU0
- ICSS0_PRU1
- ICSS1_PRU0
- ICSS1_PRU1

The Semaphore module supports the following features:

- Provides mutual exclusion for a shared resource
- A maximum of 16 semaphore masters (device cores)
- A maximum of 64 independent semaphores
- Semaphore request methods:
  - Direct request
  - Indirect request
  - Combined request
- Endian independent
- Atomic semaphore access
- Lock-out mechanism for used semaphores
- Queued requests for used semaphores
- Semaphores access grant interrupt for queued requests
- Allows the application to check the status of any of the semaphores
- Error detection and interrupts

For more information, see section *Semaphore Module* in chapter *Interprocessor Communication* of the Device TRM.

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6.9 EDMA

The primary purpose of the Enhanced Direct Memory Access (EDMA) controller is to service user-programmed data transfers between two memory-mapped slave endpoints on the device.

Typical usage of the EDMA controller includes:

- Servicing software-driven paging transfers (for example, data movement between external memory [such as SDRAM] and internal memory [such as DSP L2 SRAM])
- Servicing event-driven peripherals, such as a serial port
- Performing sorting or sub-frame extraction of various data structures
- Offloading data transfers from the main device CPUs, such as the C66x DSP CorePac or the Arm CorePac

The EDMA controller consists of two major principle blocks:

- EDMA Channel Controller
- EDMA Transfer Controller(s)

The EDMA Channel Controller (EDMACC) serves as the user interface for the EDMA controller. The EDMACC includes parameter RAM (PaRAM), channel control registers, and interrupt control registers. The EDMACC serves to prioritize incoming software requests or events from peripherals and submits transfer requests (TR) to the EDMA transfer controller.

The EDMA Transfer Controller (EDMATC) is responsible for data movement. The transfer request packets (TRP) submitted by the EDMACC contain the transfer context, based on which the transfer controller issues read/write commands to the source and destination addresses programmed for a given transfer.

There are two EDMA controllers present on this device:

- EDMA_0, integrating:
  - 1 Channel Controller, referenced as: EDMACC_0
  - 2 Transfer Controllers, referenced as: EDMACC_0_TC_0 (or EDMATC_0) and EDMACC_0_TC_1 (or EDMATC_1)
- EDMA_1, integrating:
  - 1 Channel Controller, referenced as: EDMACC_1
  - 2 Transfer Controllers, referenced as: EDMACC_1_TC_0 (or EDMATC_2) and EDMACC_1_TC_1 (or EDMATC_3)

The two EDMA channel controllers (EDMACC_0 and EDMACC_1) are functionally identical. For simplification, the unified name EDMACC shall be regularly used throughout this chapter when referring to EDMA Channel Controllers functionality and features.

The four EDMA transfer controllers (EDMACC_0_TC_0, EDMACC_0_TC_1, EDMACC_1_TC_0 and EDMACC_1_TC_1) are functionally identical. For simplification, the unified name EDMATC shall be regularly used throughout this chapter when referring to EDMA Transfer Controllers functionality and features.

Each EDMACC has the following features:

- Fully orthogonal transfer description:
  - 3 transfer dimensions:
    - Array (multiple bytes)
    - Frame (multiple arrays)
    - Block (multiple frames)
  - Single event can trigger transfer of array, frame, or entire block
  - Independent indexes on source and destination
- Flexible transfer definition:
  - Increment or constant addressing modes
  - Linking mechanism allows automatic PaRAM set update
  - Chaining allows multiple transfers to execute with one event

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- 64 DMA channels:
  - Channels triggered by either:
    - Event synchronization
    - Manual synchronization (CPU write to event set register)
    - Chain synchronization (completion of one transfer triggers another transfer)
  - Support for programmable DMA Channel to PaRAM mapping
- 8 Quick DMA (QDMA) channels:
  - QDMA channels are triggered automatically upon writing to PaRAM set entry
  - Support for programmable QDMA channel to PaRAM mapping
- 512 PaRAM sets:
  - Each PaRAM set can be used for a DMA channel, QDMA channel, or link set
- 2 transfer controllers/event queues:
  - 16 event entries per event queue
- Interrupt generation based on:
  - Transfer completion
  - Error conditions
- Debug visibility:
  - Queue water marking/threshold
  - Error and status recording to facilitate debug
- Memory protection support:
  - Proxied memory protection for TR submission
  - Active memory protection for accesses to PaRAM and registers

Each EDMATC has the following features:

- Supports 2-dimensional (2D) transfers with independent indexes on source and destination (EDMACC manages the 3rd dimension)
- Up to 4 in-flight transfer requests (TR)
- Programmable priority levels
- Support for increment or constant addressing mode transfers
- Interrupt and error support
- Supports only little-endian operation in this device
- Memory mapped register (MMR) bit fields are fixed position in 32-bit MMR

For more information chapter *EDMA Controller* of the Device TRM.

6.10 Peripherals

6.10.1 DCAN

Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time applications. CAN has high immunity to electrical interference and the ability to self-diagnose and repair data errors. In a CAN network, many short messages are broadcast to the entire network, which provides for data consistency in every node of the system.

The device supports two DCAN modules, referred to as DCAN_0 and DCAN_1, connecting to the CAN network through external (for the device) transceivers. The DCAN modules support bit rates up to 1 Mbit/s and are compliant to the CAN 2.0B Protocol Specification.

The DCAN module implements the following features:

- Support for CAN protocol version 2.0 part A, B
- Bit rates up to 1 Mbit/s
- Dual clock source
- 64 message objects in a dedicated message RAM
- Individual identifier mask for each message object

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- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation
- Software module reset
- Suspend mode for debug support
- Automatic bus on after Bus-Off state by a programmable 32-bit timer
- Message RAM single error correction and double error detection mechanism (SECDED)
- Direct access to message RAM during test mode.
- Support for three interrupt lines: Level 0 and Level 1, and a separate ECC interrupt line
- Local power down and wakeup support
- Automatic message RAM initialization
- Support for DMA access

For more information, see section *Dual Controller Area Network (DCAN) Interface* in chapter *Peripherals* of the Device TRM.

6.10.2 DSS

The Display Subsystem (DSS) provides the logic to interface display peripherals. DSS includes a DMA engine as part of the integrated Display Controller (DISPC) module, which allows direct access to the frame buffer (system memory). Various pixel processing capabilities are supported, such as: color space conversion, filtering, scaling, etc.

The supported display interfaces (connections to external panel) are:

- One parallel interface, which can be used for MIPI® DPI 2.0, or BT-656 or BT-1120.
- One RFBI interface, supporting MIPI DBI 2.0.

The modules integrated in DSS are:

- Display Controller (DISPC), with the following main features
  - One Direct Memory Access (DMA) engine
  - One Video Pipeline (VID1) with color space conversion and in-loop up/down-scaling
  - One Overlay Manager (OVR1)
  - Active Matrix color support for 12/16/18/24-bit (truncated or dithered encoded pixel values)
  - One Video Port (VP1) with programmable timing generator to support up to 148.5 MHz pixel clock video formats defined in CEA-861-E and VESA DMT standards
  - Supported maximum FrameBuffer width of 4096 for all pixel formats
  - Configurable output mode: progressive or interlaced
  - Selection between RGB and YUV422 output pixel formats (YUV4:2:2 only available when BT-656 or BT-1120 output mode is enabled on the DPI interface)
  - Stall Mode support for RFBI
- Remote Frame Buffer Interface (RFBI) module, with the following main features:
  - Access to RFB direct "ARMSS interface":
    - Sending commands and data to the RFB panel, received from DISPC or from ARMSS (through the 32-bit interconnect slave port)
    - Reading data/status from the RFB through the 32-bit interconnect slave port
  - RFB interface:
    - 8/9/12/16-bit data bus (for up to QVGA @30fps)
    - Two programmable configurations for two peripheral devices connected to the RFBI module
    - Tearing Effect control logic: Horizontal Synchronization (HSync) and Vertical Synchronization (VSync) embedded in a single signal (TE) or using two signals (HS+VS)
    - Programmable pixel memory and output formats

DSS provides two interfaces to SoC interconnect:

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- One 128-bit master port (with MFLAG support). The DMA engine in DISPC uses this single master port to read data from SoC system memory.
- One 32-bit slave port. Used for configuration of the memory mapped registers inside DSS. It is further connected internally to DISPC and RFBI modules.

For more information, see section *Display Subsystem (DSS)* in chapter *Peripherals* of the Device TRM.

6.10.3 eCAP

The enhanced Capture (eCAP) module can be used for:

- Sample rate measurements of audio inputs
- Speed measurements of rotating machinery (for example, toothed sprockets sensed via Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors.

The eCAP module includes the following features:

- 32-bit time base counter
- 4-event time-stamp registers (each 32 bits)
- Edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single shot capture of up to four event time-stamps
- Continuous mode capture of time-stamps in a four-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- All above resources dedicated to a single input pin
- When not used in capture mode, the eCAP module can be configured as a single channel PWM output.

For more information, see section *Enhanced Capture (eCAP) Module* in chapter *Peripherals* of the Device TRM.

6.10.4 ePWM

An effective PWM peripheral must be able to generate complex pulse width waveforms with minimal CPU overhead or intervention. It needs to be highly programmable and very flexible while being easy to understand and use. The ePWM unit described here addresses these requirements by allocating all needed timing and control resources on a per PWM channel basis. Cross coupling or sharing of resources has been avoided; instead, the ePWM is built up from smaller single channel modules with separate resources and that can operate together as required to form a system. This modular approach results in an orthogonal architecture and provides a more transparent view of the peripheral structure, helping users to understand its operation quickly.

In the further description the letter x within a signal or module name is used to indicate a generic ePWM instance on a device. For example, output signals EPWMxA and EPWMxB refer to the output signals from the ePWM_x instance. Thus, EPWM1A and EPWM1B belong to ePWM_1, EPWM2A and EPWM2B belong to ePWM_2, and so forth.

The ePWM module represents one complete PWM channel composed of two PWM outputs: EPWMxA and EPWMxB. A given ePWM module functionality can be extended with the so called High-Resolution Pulse Width modulator.

Each ePWM module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control

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- Two PWM outputs (EPWMxA and EPWMxB) that can be used in the following configurations:
  - Two independent PWM outputs with single-edge operation
  - Two independent PWM outputs with dual-edge symmetric operation
  - One independent PWM output with dual-edge asymmetric operation
- Asynchronous override control of PWM signals through software
- Programmable phase-control support for lag or lead operation relative to other ePWM modules
- Hardware-locked (synchronized) phase relationship on a cycle-by-cycle basis
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions
- A trip condition can force either high, low, or high-impedance state logic levels at PWM outputs
- Allows events to trigger both CPU interrupts and ADC start of conversions
- Programmable event prescaling minimizes CPU overhead on interrupts
- PWM chopping by high-frequency carrier signal, useful for pulse transformer gate drives.

For more information, see section *Enhanced PWM (ePWM) Module* in chapter *Peripherals* of the Device TRM.

6.10.5 eQEP

A single track of slots patterns the periphery of an incremental encoder disk. These slots create an alternating pattern of dark and light lines. The disk count is defined as the number of dark/light line pairs that occur per revolution (lines per revolution). As a rule, a second track is added to generate a signal that occurs once per revolution (index signal: QEPI), which can be used to indicate an absolute position. Encoder manufacturers identify the index pulse using different terms such as index, marker, home position and zero reference.

To derive direction information, the lines on the disk are read out by two different photo-elements that "look" at the disk pattern with a mechanical shift of 1/4 the pitch of a line pair between them. This shift is realized with a reticle or mask that restricts the view of the photo-element to the desired part of the disk lines. As the disk rotates, the two photo-elements generate signals that are shifted 90 degrees out of phase from each other. These are commonly called the quadrature QEPA and QEPB signals. The clockwise direction for most encoders is defined as the QEPA channel going positive before the QEPB channel and vise versa.

The encoder wheel typically makes one revolution for every revolution of the motor or the wheel may be at a geared rotation ratio with respect to the motor. Therefore, the frequency of the digital signal coming from the QEPA and QEPB outputs varies proportionally with the velocity of the motor. For example, a 2000-line encoder directly coupled to a motor running at 5000 revolutions per minute (rpm) results in a frequency of 166.6 KHz, so by measuring the frequency of either the QEPA or QEPB output, the processor can determine the velocity of the motor.

For more information, see section *Enhanced Quadrature Encoder Pulse (eQEP) Module* in chapter *Peripherals* of the Device TRM.

6.10.6 GPIO

The general-purpose input/output (GPIO) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, user can write to an internal register to control the state driven on the output pin. When configured as an input, user can obtain the state of the input by reading the state of an internal register.

In addition, the GPIO peripheral can produce CPU interrupts and EDMA synchronization events in different interrupt/event generation modes.

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The device has two instances of GPIO144 modules (GPIO_0 and GPIO_1). The GPIO pins are grouped into banks (16 pins per bank), which means that each GPIO module provides up to 144 dedicated general-purpose pins with input and output capabilities; thus, the general-purpose interface supports up to 288 (2 instances × (9 banks × 16 pins)) pins. Since GPIO1_[143:68] are reserved in this Device, general-purpose interface supports up to 212 pins.

Each channel in the GPIO modules has the following features:

- Supports 9 banks of 16 GPIO signals
- Supports up to 9 banks of interrupt capable GPIOs
- Interrupts:
  - Can enable interrupts for each bank of 16 GPIO signals
  - Interrupts can be triggered by rising and/or falling edge (or neither edge = disabled), specified for each interrupt capable GPIO signal
- Set/clear functionality:
  - Software writes 1 to corresponding bit position(s) to set or to clear GPIO signal(s). This allows multiple software processes to toggle GPIO output signals without critical section protection (disable interrupts, program GPIO, re-enable interrupts, to prevent context switching to anther process during GPIO programming).
- Separate Input/Output registers:
  - Output register in addition to set/clear so that if preferred by software, some GPIO output signals can be toggled by direct write to the output register(s).
  - Output register, when read in, reflects output drive status. This, in addition to the input register reflecting pin status and open-drain I/O cell, allows wired logic be implemented.

For more information, see section *General-Purpose Interface (GPIO)* in chapter *Peripherals* of the Device TRM.

6.10.7 I2C

The multi-master inter-integrated circuit (I2C) peripheral provides an interface between the device and any I^2C-bus-compatible device that is connected via the I^2C serial bus. External components attached to the I^2C bus can serially transmit/receive up to 8-bit data to/from the device through the two-wire I^2C interface.

Each I2C module has the following features:

- Compliance with the Philips Semiconductors I^2C-bus Specification (version 2.1):
  - Supports standard mode (up to 100 kbps) and fast mode (up to 400 kbps)
  - Support for byte format transfer
  - 7-bit addressing mode
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers mode
  - Support for multiple slave-transmitters and master-receivers mode
  - Combined master transmit/receive and receive/transmit mode
- 2 to 7 bit format transfer
- Free data format mode
- One read DMA event and one write DMA event that can be used by the DMA
- Seven interrupts that can be used by the CPU
- Module enable/disable capability

I2C module unsupported features:

- GPIO mode
- High-speed (HS) mode

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- 10-bit device addressing mode

The I2C module is compliant with the Philips Semiconductors Inter-IC bus (I^2C-bus) Specification version 2.1.

For more information, see section *Inter-IC module (I2C)* in chapter *Peripherals* of the Device TRM.

6.10.8 ASRC

The reception of many different audio sources and the transmission of these to different audio zones, may require different audio clocks. The asynchronous Audio Sample Rate Converter (ASRC) module takes samples from one clock zone and moves them to another, while maintaining a high signal to noise ratio to ensure that the output quality is sufficient to meet the requirements for various high-end algorithms.

The ASRC module supports the following main features:

- High performance Asynchronous Sample Rate Converter with 140 dB Signal-to-Noise (SNR)
- Up to 8 stereo streams (16 audio channels)
- Automatically sensing / detection of input sample frequencies
- Attenuation of sampling clock jitter
- 16-, 18-, 20-, 24-bit data input/output
- Audio sample rates from 8 kHz to 216 kHz
- Input/output sampling ratios from 16:1 to 1:16
- Group mode, where multiple ASRC blocks use the same timing loop for input or output
- Linear phase FIR filter
- Controllable soft mute
- Independent Clock Generator, and Rate and Stamp generator, for each input and output clock zone
- Separate DMA events for input and output, for each channel and group

For more information, see section *Audio Sample Rate Converter (ASRC)* in chapter *Peripherals* of the Device TRM.

6.10.9 McASP

The Multi-channel Audio Serial Port (McASP) module functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP supports transmission and reception of time-division multiplexed (TDM) and Inter-IC Sound (I^2S) protocols. In addition, it supports intercomponent digital audio interface transmission (DIT).

The McASP consists of transmit and receive sections that may operate synchronized, or completely independently with separate master clocks, bit clocks, and frame syncs, and using different transmit modes with different bit-stream formats. The McASP module also includes up to 16 serializers that can be individually enabled to either transmit or receive.

The device integrates three McASP modules (McASP0, McASP1, and McASP2) with:

- McASP0 supporting 16 serializers with independent TX/RX clock zones
- McASP1 supporting 10 serializers with independent TX/RX clock zones
- McASP2 supporting 6 serializers with independent TX/RX clock zones

Each McASP module includes the following main features:

- Up to 16 individually assignable serializers, each with its own data pins (AXR)
- A single 32-bit buffer per serializer for transmit and receive operations
- 2x interconnect slave interface ports:
  - A configuration (CFG) port
  - A slave DMA data port synchronized with functional clock

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- Two independent clock generator modules for transmit and receive:
  - Clocking flexibility allows the McASP to receive and transmit at different rates. For example, the McASP can receive data at 48 kHz but output up-sampled data at 96 kHz or 192 kHz.
- Configurable functional clocks:
  - May be generated internally (master mode)
  - May be supplied by an external device (slave mode)
  - May be divided down internally
- Independent transmit and receive modules, each providing:
  - Programmable clock and frame sync generator
  - TDM streams from 2 to 32, and 384 time slots
  - Support for time slot sizes of 8, 12, 16, 20, 24, 28, and 32 bits
  - Data formatter for bit manipulation
- Glueless connection to audio analog-to-digital converters (ADC), digital-to-analog converters (DAC), codec, digital audio interface receiver (DIR), and S/PDIF transmit physical layer components.
- Support for wide variety of I^2S and similar bit-stream formats
- Integrated digital audio interface transmitter (DIT):
  - S/PDIF, IEC60958-1, AES-3 formats.
  - Enhanced channel status/user data RAM
- 384-slot TDM with external digital audio interface receiver (DIR) device:
  - For DIR reception, an external DIR receiver integrated circuit should be used with I^2S output format and connected to the McASP receive section
- Support for 2x DMA requests (1 per direction) per each McASP module:
  - 1 level-sensitive transmit direct memory access (DMA) request common for all of the McASP serializers
  - 1 level-sensitive receive direct memory access (DMA) request common for all of the McASP serializers
- One transmit interrupt request common for all serializers per McASP module
- One receive interrupt request common for all serializers per McASP module
- Extensive error checking and recovery:
  - Transmit underruns and receiver overruns due to the system not meeting real-time requirements
  - Early or late frame sync in TDM mode
  - DMA error due to incorrect programming
- McASP Audio FIFO (AFIFO):
  - Provides additional data buffering
  - Provides added tolerance to variations in host/DMA controller response times
  - May be used as a DMA event pacer
  - Independent Read FIFO and Write FIFO
  - 256 bytes of RAM for each FIFO (read and write), where:
    - 256 bytes = four 32-bit words per serializer in the case of 16 data pins
    - 256 bytes = 64 32-bit words in the case of one data pin
  - Option to bypass Write FIFO and/or Read FIFO independently

For more information, see section *Multi-channel Audio Serial Port (McASP)* in chapter *Peripherals* of the Device TRM.

6.10.10 McBSP

The Multi-channel Buffered Serial Port (McBSP) provides a full-duplex serial communication interface between the device and other devices in a system. The primary use for the McBSP is for audio interface purposes. The main audio modes that are supported are the AC97 and I^2S modes. In addition to the primary audio modes, the McBSP can be programmed to support other serial formats but is not intended to be used as a high-speed interface. The device communicates to the McBSP using 32-bit-wide control registers accessible via the internal peripheral bus.

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The McBSP provides the following functions:

- Full-duplex communication
- Double-buffered data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit
- Direct interface to industry-standard codecs, analog interface chips (AICs), and other serially connected analog-to-digital (A/D) and digital-to-analog (D/A) devices
- External shift clock or an internal, programmable frequency shift clock for data transfer

In addition, the McBSP has the following capabilities:

- Direct interface to:
  - T1/E1 framers
  - MVIP switching compatible and ST-BUS compliant devices including:
    - MVIP framers
    - H.100 framers
    - SCSA framers
  - IOM-2 compliant devices
  - AC97 compliant devices (the necessary multiphase frame synchronization capability is provided)
  - I^2S compliant devices
- Multi-channel transmit and receive of up to 128 channels
- A wide selection of data sizes, including 8, 12, 16, 20, 24, and 32 bits
- μ-Law and A-Law companding
- 8-bit data transfers with the option of LSB or MSB first
- Programmable polarity for both frame synchronization and data clocks
- Highly programmable internal clock and frame generation
- Additional McBSP Buffer FIFO (BFIFO):
  - Provides additional data buffering
  - Provides added tolerance to variations in host/DMA controller response times
  - May be used as a DMA event pacer
  - Independent Read FIFO and Write FIFO
  - 256 bytes of RAM for each FIFO (read and write)
  - Option to bypass Write FIFO and/or Read FIFO, independently

McBSP module unsupported features:

- The McBSP on this device does not support the SPI protocol.
- 512 Channel Mode
- Individual enable/disable channel control
- Timeslot buffering
- Super frame synchronization
- ABIS Mode

For more information, see section *Multi-channel Buffered Serial Port (McBSP)* in chapter *Peripherals* of the Device TRM.

6.10.11 MLB

The Media Local Bus subsystem (MLB) is based on a module designed by SMSC. This module provides a MediaLB/MediaLB+ controller and an interface to other MediaLB/MediaLB+ devices. The MediaLB/MediaLB+ interface allows also connection to a MOST (Media Oriented Systems Transport) network controller.

The MLB supports the following features:

- 3-pin MediaLB 3.3V LVCMOS I/Os compliant to MediaLB Physical Layer Specification v4.2
- 6-pin MediaLB+ low-voltage differential signaling (LVDS) I/Os (3 differential pairs) compliant to MediaLB Physical Layer Specification v4.2

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- MediaLB core functionality compliant to MediaLB Physical Layer and Link Layer Specification v4.2
- Supports 256/512/1024Fs in 3-pin mode and 2048Fs in 6-pin mode
- Supports all types of transfer (synchronous stream data, asynchronous packet data, control message data, and isochronous data) over 64 logical channels
- Supports single 32-bit TeraNet_CFG slave interface for configuration
- Supports single 32-bit TeraNet_DMA master interface with burst capability for DMA transfers into system memory. The maximum burst size is 32 Bytes
- Has 16 KB buffer for all types of transfers in the subsystem
- Dedicated BOOT_CFG bits for controlling the MLB priority on the system interconnect

The MLB does not support:

- 5-pin mode
- Digital Transmission Content Protection (DTCP) cipher accelerators

For more information, see section *Media Local Bus (MLB)* in chapter *Peripherals* of the Device TRM.

6.10.12 MMC/SD

The multimedia card (MMC), secure digital (SD), and secure digital I/O (SDIO) high-speed controller (MMC/SD) provides an interface between a local host (LH) such as microprocessor unit (MPU) or digital signal processor (DSP) and either MMC, SD memory card, or SDIO card and handles MMC, SD, and SDIO transactions with minimal LH intervention. There are two MMC/SD host controllers inside the device. Each controller has an 8-bit wide data bus.

The MMC/SD host controllers support the following main features:

- Full compliance with MMC/eMMC command/response sets as defined in the JC64 MMC/eMMC Standard Specification, v4.5.
- Full compliance with SD command/response sets as defined in the SD Physical Layer Specification v3.01.
- Full compliance with SDIO command/response sets and interrupt/read-wait suspend-resume operations as defined in the SD part E1 Specification v3.00.
- Full compliance with SD Host Controller Standard Specification sets as defined in the SD card Specification Part A2 v3.00.

Main features of the MMC/SD host controllers:

- Flexible architecture allowing support for new command structure
- Designed for low power (Local Power Management)
- Programmable clock generation
- Card insertion/removal detection and write protect detection
- The slave interface supports:
  - 32-bit wide data bus
  - Streaming burst supported only with burst length up to 7
  - WNP supported
- The master interface supports:
  - 32-bit wide data bus
  - Burst supported
- Built-in 1024-byte buffer for read or write
- Two DMA channels, one interrupt line
- Support JC 64 v4.4.1 boot mode operations
- Support SDA 3.00 Part A2 programming model
- Support SDA 3.00 Part A2 DMA feature (ADMA2)

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- Supported data transfer rates:
  - MMC0 supports the following data transfer rates (eMMC/SD):
    - SDR12 (3.3 V IOs): up to 12 MBps (24 MHz clock)
    - SDR25 (3.3 V IOs): up to 24 MBps (48 MHz clock)
    - HS mode (3.3 V IOs): up to 24 MBps (48 MHz clock)
    - DS mode (3.3 V IOs): up to 12 MBps (24 MHz clock)
    - Default SD mode 1-bit data transfer up to 24 Mbps (3 MBps)
  - MMC1 supports the following data transfer rates (eMMC):
    - SDR12 (1.8 V IOs): up to 12 MBps (24 MHz clock)
    - SDR25 (1.8 V IOs): up to 24 MBps (48 MHz clock)
    - DDR50 (1.8 V IOs): up to 48 MBps (48 MHz clock)
    - 1.8 V legacy modes with 1/4/8-bit single data rate at up to 26 MHz bus clock
- MMC0 Supports 3.3-V IO modes only
- MMC1 Supports 1.8-V IO modes only

The differences between the MMC/SD host controller and a standard SD host controller defined by the SD Card Specification, Part A2, SD Host Controller Standard Specification, v3.00 are:

- The clock divider in the MMC/SD host controller supports a wider range of frequency than specified in the SD Memory Card Specifications, v3.0. The MMC/SD host controller supports odd and even clock ratio.
- The MMC/SD host controller supports configurable busy time-out.
- ADMA2 64-bit mode is not supported.
- There is no external LED control.

The following features are not supported:

- Byte or half-word accesses. Only word accesses to the slave port are supported.
- MMC Out-of-band interrupt.
- Dual voltage I/O (MMC0 Supports 3.3-V only. MMC1 Supports 1.8-V only).
- No built-in hardware support for error correction codes (ECC).
- SPI transfers are not supported.
- Module doesn't support card insertion/removal sensing with pull up resistor on MMCi_DAT[3] data bus line as specified in the SD Physical Layer Specification.

For more information, see section *Multimedia Card High Speed Interface (MMC/SD)* in chapter *Peripherals* of the Device TRM.

6.10.13 NSS

Networking Subsystem (NSS) consists of DMA/Queue Management components – Navigator Subsystem (NAVSS), an Ethernet MAC (EMAC) Subsystem, and a packet Security Accelerator (SA).

The NSS, presented by its general sub-components, supports the following features:

- NAVSS:
  - High Performance CPPI DMA Controller, 32 Receive Flows, 4 Loopback threads for infrastructure mode
  - CPPI Queue Manager (QM) features:
    - Single QM
    - Supports up to 128 queues – 21 QPEND signals for TX use, remaining 107 QPEND signals are for host use
    - 2048 buffers supported in Internal Linking RAM
    - Two Queue Proxies provided for host interaction (one per DSP and ARMSS):
      - Queue Proxy 0 assigned to DSP
      - Queue Proxy 1 assigned to ARMSS
  - Support for SER protection (SECDED)

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- EMAC Subsystem:
  - One Gigabit Ethernet port: MII/RMII/RGMII interfaces:
    - Supports 10-, 100-, 1000-Mbps full duplex
    - Supports 10-, 100-Mbps half duplex
  - One Host Port 0 CPPI Streaming Packet Interface (PSI)
  - Support Ethernet Audio/Video Bridging (eAVB) (P802.1Qav/D6.0)
  - Maximum frame size 2016 bytes (2020 bytes with VLAN)
  - Eight priority level QOS support (802.1p)
  - IEEE 1588v2 (2008 annex D, annex E, and annex F) to facilitate Audio/Video bridge 802.1AS Precision Time Protocol:
    - Timestamp module capable of time stamping external timesync events like Pulse Per Second and also generating Pulse Per Second outputs
    - CPTS module that supports time stamping for IEEE 1588v2 with support for 8 hardware push events and generation of compare output pulses
  - DSCP Priority Mapping (IPv4 and IPv6)
  - Maximum frame size 2016 bytes (2020 with VLAN)
  - Address Lookup Engine (ALE)
  - Castagnoli or Ethernet CRC selectable for Ethernet ingress and egress (Host Port0 CRC is Ethernet only)
  - MDIO module for PHY management
  - EtherStats and 802.3Stats RMON statistics gathering
  - Support for SER protection (SECDED)
- Security Accelerator (SA):
  - Support IPSec and SRTP protocol stack
  - Support various encryption modes and algorithms such as:
    - ECB, CBC, CFB, OFB, F8, CTR, CBC-MAC, CCM, GCM, GMAC and AES-CMAC
    - AES, DES, 3DES, SHA-1, SHA-2 (224, 256-bit operation) and MD5
  - Support for True random number generator (TRNG) and Public Key Accelerator (PKA)
  - Support for SER protection (SECDED)

The NSS does not support the following features:

- No external queue RAM supported
- Priority Based Flow Control is not supported.
- No Castignoli CRC to Host CPPI port.

For more information, see section *Networking Subsystem (NSS)* in chapter *Peripherals* of the Device TRM.

6.10.14 PCIESS

Peripheral Component Interconnect Express (PCIE) controllers provide a high-speed glueless serial interconnect to peripherals utilizing high bandwidth applications.

PCIe module is a multi-lane I/O interconnect that provides low pin-count, high reliability, and high-speed data transfer at rates of up to 5.0 Gbps per lane, per direction, for serial links on backplanes and printed curcuit boards. It is a 2nd generation I/O interconnect technology succeeding PCI and ISA bus designed to be used as a general-purpose serial I/O interconnect. It is also used as a bridge to other interconnects such as SATA, USB2/3.0, GbE MAC, and so forth.

The PCI Express standard's predecessor - PCI, is a parallel bus architecture that is increasingly difficult to scale-up in bandwidth, which is usually performed by increasing the number of data signal lines. The PCIe architecture was developed to help minimize I/O bus bottlenecks within systems and to provide the necessary bandwidth for high-speed, chip-to-chip, and board-to-board communications within a system. It is designed to replace the PCI-based shared, parallel bus signaling technology that is approaching its practical performance limits while simplifying the interface design.

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PCIe module supports the following features:

- Dual operation mode: Root Complex (RC) or End Point (EP)
- Supports a single bidirectional link interface (a single input port and a single output port) with one lane
- Operated at a raw speed of 2.5 Gbps or 5.0 Gbps per lane per direction
- Maximum outbound payload size of 128 bytes
- Maximum inbound payload size of 256 bytes
- Maximum remote read request size of 256 bytes
- Ultra-low transmit and receive latency
- Support for dynamic-width conversion
- Automatic lane reversal
- Polarity inversion on receive
- Single virtual channel (VC)
- Single traffic class (TC)
- Single function in End Point (EP) mode
- Automatic credit management
- ECRC generation and checking
- PCI device power management with the exception of D3cold with Vaux
- PCI Express active state power management (ASPM) state L0s and L1
- PCI Express link power management states, except L2 state
- PCI Express advanced error reporting
- PCI Express messages for both transmit and receive
- Filtering for posted, non-posted, and completion traffic
- Configurable BAR filtering, I/O filtering, configuration filtering, and completion lookup/timeout
- Access to configuration space registers and external application memory-mapped registers through BAR0 and through configuration access
- Legacy interrupts reception (in RC) and generation (in EP)
- MSI generation and reception
- PHY loopback in RC mode

PCIe module does not support the following features:

- No support for multiple lanes
- No support for multiple VCs
- No support for multiple TCs
- No support for function-level reset
- No support for PCI Express beacon for in-band wake
- No built-in hardware support for hot-plug
- No support for vendor messaging
- No support for I/O access in inbound direction in RC or EP mode
- No support for addressing modes other than incremental for burst transactions. Thus, the PCIe addresses cannot be in cacheable memory space
- No auxiliary power to maintain controller context when rezuming from D3cold state
- No support for L2 link state

For more information, see section *Peripheral Component Interconnect Express Subsystem (PCIe SS)* in chapter *Peripherals* of the Device TRM.

6.10.15 QSPI

The Quad Serial Peripheral Interface (QSPI™) module is a kind of Serial Peripheral Interface (SPI) module which allows single, dual or quad read and write access to external flash devices. This module has a memory mapped register interface, which provides a direct memory interface for accessing data from external flash devices, simplifying software requirements.

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The QSPI module has the following features:

- Memory-Mapped *Direct* mode of operation for performing flash data transfers and executing code from flash memory.
- Software triggered 'indirect' mode of operation for performing low latency and non-processor intensive flash data transfers.
- Local SRAM to reduce bus overhead and buffer flash data during indirect transfers.
- Set of software accessible flash control registers to perform any flash command, including data transfers up to 8-bytes at a time.
- Supports any device clock frequency, including frequencies of 96 MHz (QSPI mode 0 only).
- Supports XIP (Execute in Place), also referred to as continuous mode.
- Supports single, dual or quad I/O instructions.
- Supports 16/32/64 byte cacheline wrap accesses.
- Supports ECC for its internal SRAM buffer.
- Programmable device sizes.
- Programmable write protected regions to block system writes from taking effect.
- Programmable delays between transactions.
- Legacy mode allowing software direct access to low level transmit and receive FIFOs bypassing the higher layer processes.
- Independent reference clock to decouple bus clock from SPI clock – allows slow system clocks.
- Serial clock with programmable polarity.
- Programmable baud rate generator to generate QSPI clocks.
- Features included to improve high speed read data capture mechanism.
- Option to use adapted clocks to further improve read data capturing.
- Programmable interrupt generation.
- Up to four external chip selects.
- Supports Little-endian operation only.

For more information, see section *Quad Serial Peripheral Interface (QSPI)* in chapter *Peripherals* of the Device TRM.

6.10.16 SPI

The SPI module is a master/slave high-speed synchronous serial input/output interface that allows a serial bit stream of programmed length (2 to 16 bits) to be shifted in and out of the device at a programmed bit-transfer rate. There are four separate SPI modules (SPI0, SPI1, SPI2, and SPI3) in the device. All these four modules support up to two external devices (two chip selects) and are able to work as both master and slave. The SPI module allows multiple programmable chip-selects. It is normally used for communication between the device and external peripherals. Typical applications include interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EEPROMS, and analog-to-digital converters. The SPI module may be used to connect to serial flash memory devices for booting. The SPI module supports EDMA events and can be used in conjunction with EDMA for data transfer with minimal CPU overhead.

The SPI module has the following features:

- 16-bit Shift register
- 16-bit Receive buffer register and 16-bit Receive buffer emulation *alias* register
- 16-bit Transmit data register and 16-bit Transmit data and format selection register
- 8-bit Baud clock generator
- Serial clock (SPIm_CLK) I/O pin
- Slave in, master out (SPIm_SIMO) I/O pin
- Slave out, master in (SPIm_SOMI) I/O pin
- 2 Chip select signals (SPIm_SCSn0 and SPIm_SCSn1)
- Programmable SPI clock frequency range

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- Programmable character length (2 to 16 bits)
- Programmable clock phase (delay or no delay)
- Programmable clock polarity (high or low)
- Interrupt capability
- DMA support (read/write synchronization events)
- Operates at up to 50 MHz in master mode and 25 MHz in slave mode (actual speed depends on SPI functional clock and SPI clock divider)

The SPI module allows software to program the following options:

- SPIm_CLK frequency (SPI functional clock / 2 through SPI functional clock / 256)
- 3-pin and 4-pin options
- Character length (2 to 16 bits) and shift out direction (MSB/LSB first)
- Clock phase (delay or no delay) and polarity (high or low)
- Delay between transmissions in master mode
- Chip select setup and hold times in master mode
- Chip select hold in master mode

The SPI module does not support the following features:

- Multibuffer mode
- Parallel mode and parity
- GPIO mode

For more information, see section *Serial Peripheral Interface (SPI)* in chapter *Peripherals* of the Device TRM.

6.10.17 Timers

There are total of 7 chip-level timers.

The device includes several types of timers used by the system software, including general-purpose (GP) timers, watchdog timers, and a wake-up timer, as it follows:

- TIMER_0 is dedicated/tightly coupled for C66x CorePac. TIMER_0 can be used as general-purpose timer or watchdog timer
- TIMER_1 through TIMER_4 are general-purpose timers
- TIMER_5 is dedicated/tightly coupled for the Arm core 0. TIMER_5 can be used as general-purpose timer or watchdog timer
- TIMER_6 is dedicated as device wake-up timer by interrupting PMMC CPU. TIMER_6 cannot be used by high-level software as a general-purpose timer or watchdog. TIMER_6 is neither connected to Timer pin manager block nor to Timer IOs.
  - On-the-fly read/write register (while counting)

Each timer has two input pins (TINPL and TINPH) and two output pins (TOUTL and TOUTH).

At the chip level there are 4 timer pins — two input pins (TIMI[1:0]) and two output pins (TIMO[1:0]). Each of TIMER_0 through TIMER_5 input can be configured to be driven by the timer input pins. Each of TIMO[1:0] output pin can be driven by any of the timer outputs. The selection of timer inputs and outputs is controlled by Timer pin manager. The Timer pin manager block is controlled by registers in BOOT_CFG module.

For more information, see section *Timers* in chapter *Peripherals* of the Device TRM.

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6.10.18 UART

The Universal Asynchronous Receiver/Transmitter peripheral is 16550 standard compatible asynchronous communications element. The UART can be placed in an alternate FIFO mode. This relieves the CPU of excessive software overhead by buffering received and transmitted characters. The receiver and transmitter FIFOs store up to 16 bytes including three additional bits of error status per byte for the receiver FIFO.

There are 3 UART (UART_0, UART_1 and UART_2) modules in the device. Only UART_0 supports full modem control functions. Each UART can be used for configuration and data exchange with a number of external peripheral devices or interprocessor communication between devices.

The UART_i (where i = 0 to 2) include the following features:

- 16550 standard compatible
- 16-byte FIFO buffer for receiver and 16-byte FIFO for transmitter
- Baud generation based on programmable divisors operating from a fixed functional clock of 192 MHz
- Oversampling is programmed by software as 16 or 13. Thus, the baud rate computation is one of two options:
  - Baud rate = (functional clock / 16) / N
  - Baud rate = (functional clock / 13) / N
- Break character detection and generation
- Configurable data format:
  - Data bit: 5, 6, 7, or 8 bits
  - Parity bit: Even, odd, none
  - Stop-bit: 1, 1.5, 2 bit(s)
- Flow control: Hardware (RTS/CTS)
- The 192 MHz functional clock option allows baud rates up to 12Mbps

The UART performs serial-to-parallel conversions on data received from a peripheral device or modem and parallel-to-serial conversion on data received from the CPU. The CPU can read the UART status at any time. The UART includes control capability and a processor interrupt system that can be tailored to minimize software management of the communications link.

For more information, see section *Universal Asynchronous Receiver/Transmitter (UART)* in chapter *Peripherals* of the Device TRM.

6.10.19 USB

Similar to earlier versions of USB bus, USB 2.0 is a general-purpose cable bus, supporting data exchange between a host device and a wide range of simultaneously accessible peripherals.

The device supports two USB 2.0 subsystems with High Speed Dual-Role-Device (DRD) ports with integrated PHY.

The USB 2.0 subsystem, supports the following USB features:

- Dual-role-device (DRD) capability:
  - Supports USB 2.0 Peripheral (or Device) mode at Highspeed (480 Mbps) and Fullspeed (12 Mbps)
  - Supports USB 2.0 Host mode at Highspeed (480 Mbps), Fullspeed (12 Mbps), and Lowspeed (1.5 Mbps)
  - USB 2.0 static peripheral operation
  - USB 2.0 static host operation
  - xHCI Debug Capability
  - External Buffer Control (EBC) mode for IN (Tx) Endpoint

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- Each controller instance contains single xHCI with the following features:
  - Compatible to the xHCI Specification (Revision 1.1) in Host mode
  - Supports 15 Transmit (TX), 15 Receive (RX) endpoints (EPs), and one EP0 endpoint which is bidirectional
  - Internal DMA controller
  - Interrupt moderation and blocking
  - Supports for all USB transfer modes - Control, Bulk, Interrupt, and Isochronous
  - Supports high bandwidth ISO mode
  - Descriptor caching and data pre-fetching used to improve system performance
  - Dynamic FIFO memory allocation for all endpoints
- Operation flexibility:
  - Uniform programming model for HS, FS, and LS operation
  - Multiple interrupt lines:
    - 16 interrupts associated with 16 programmable Event Rings for multi-core support
    - A MISC interrupt line for all miscellaneous events
- ECC RAM
- External requirements:
  - An external charge pump for VBUS 5 V generation
  - An external reference clock input for USB PHY operation
  - An external high-precision resistor for internal PHY termination calibration

The following are USB features which are not supported:

- USB 3.0 SuperSpeed (5 Gbps) or USB3.1 SuperSpeed+ (10 Gbps) operation in either host or device modes
- OTG Functionality
- HSIC (High Speed inter-chip)
- ULPI Interface for external PHY
- Battery Charger Support
- Accessory Charger Adaptor Support
- xHCI Virtualization
- Hibernation (separate power domain for wake up from USB and save/ restore on wakeup) mode
- External Buffer Control (EBC) for OUT (Rx) Endpoint

For more information, see section *Universal Serial Bus Subsystem (USB)* in chapter *Peripherals* of the Device TRM.

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7 Applications, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test design implementation to confirm system functionality.

7.1 DDR3L Board Design and Layout Guidelines

7.1.1 DDR3L General Board Layout Guidelines

To help ensure good signaling performance, consider the following board design guidelines:

- Avoid crossing splits in the power plane.
- Minimize Vref noise.
- Use the widest trace that is practical between decoupling capacitors and memory module.
- Maintain a single reference.
- Minimize ISI by keeping impedances matched.
- Minimize crosstalk by isolating sensitive bits, such as strobes, and avoiding return path discontinuities.
- Use proper low-pass filtering on the Vref pins.
- Keep the stub length as short as possible.
- Add additional spacing for on-clock and strobe nets to eliminate crosstalk.
- Maintain a common ground reference for all bypass and decoupling capacitors.
- Take into account the differences in propagation delays between microstrip and stripline nets when evaluating timing constraints.

7.1.2 DDR3L Board Design and Layout Guidelines

7.1.2.1 Board Designs

TI only supports board designs using DDR3L memory that follow the guidelines in this document. The switching characteristics and timing diagram for the DDR3L memory controller are shown in Table 7-1 and Figure 7-1.

Table 7-1. Switching Characteristics Over Recommended Operating Conditions for DDR3L Memory Controller

NO.	PARAMETER			MIN	MAX	UNIT
1	$t_{c(DDR3_CLKOUT_P/N)}$	Cycle time, DDR3_CLKOUT_P/N	Device Speed 60	2.5	3.3(1)	ns
			Device Speed 100	1.876	3.3(1)	ns

(1) This is the absolute maximum value of the clock period. Actual maximum clock period may be limited by DDR3L speed grade and operating frequency (see the DDR3L memory device data sheet).

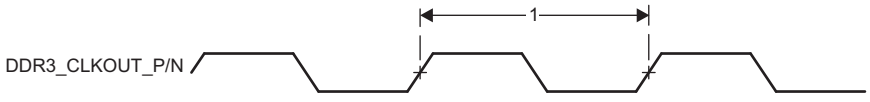

Figure 7-1. DDR3L Memory Controller Clock Timing

7.1.2.2 DDR3L Device Combinations

Because there are several possible combinations of device counts and single- or dual-side mounting, Table 7-2 summarizes the supported device configurations.

Table 7-2. Supported DDR3L Device Combinations

NUMBER OF DDR3L DEVICES	DDR3L DEVICE WIDTH (BITS)	MIRRORED?	DDR EMIF WIDTH (BITS)
1	16	N	16
2	8	Y(1)	16
2	16	N	32
2	16	Y(1)	32
3	16	N	32
4	8	N	32
4	8	Y(2)	32
5	8	N	3

(1) Two DDR3L devices are mirrored when one device is placed on the top of the board and the second device is placed on the bottom of the board.

(2) This is two mirrored pairs of DDR3L devices.

7.1.2.3 DDR3L Interface Schematic

7.1.2.3.1 32-Bit DDR3L Interface

The DDR EMIF schematic varies, depending upon the width of the DDR3L devices used and the width of the bus used (16 or 32 bits). General connectivity is straightforward and very similar. 16-bit DDR devices look like two 8-bit devices. Figure 7-2 and Figure 7-3 show the schematic connections for 32-bit interfaces using ×16 devices.

7.1.2.3.2 16-Bit DDR3L Interface

Note that the 16-bit wide interface schematic is practically identical to the 32-bit interface (see Figure 7-2 and Figure 7-3); only the high-word DDR memories are removed and the unused DQS inputs are tied off.

When not using all or part of the DDR EMIF, the proper method of handling the unused pins is to tie off the DDR3_DQS*_P*i* pins to ground via a 1k-Ω resistor and to tie off the DDR3_DQS*_N*i* pins to the corresponding DVDD_DDR supply via a 1k-Ω resistor. This needs to be done for each byte not used. Although these signals have internal pullups and pulldowns, external pullups and pulldowns provide additional protection against external electrical noise causing activity on the signals.

The DVDD_DDR, DVDD_DDRDLL, and DDR3_VREFSSTL power supply pins need to be connected to their respective power supplies even if the DDR EMIF is not being used. All other DDR EMIF pins can be left unconnected.

Note: The only DDR EMIF configurations supported are 32-bits wide, 16-bits wide, or not used.

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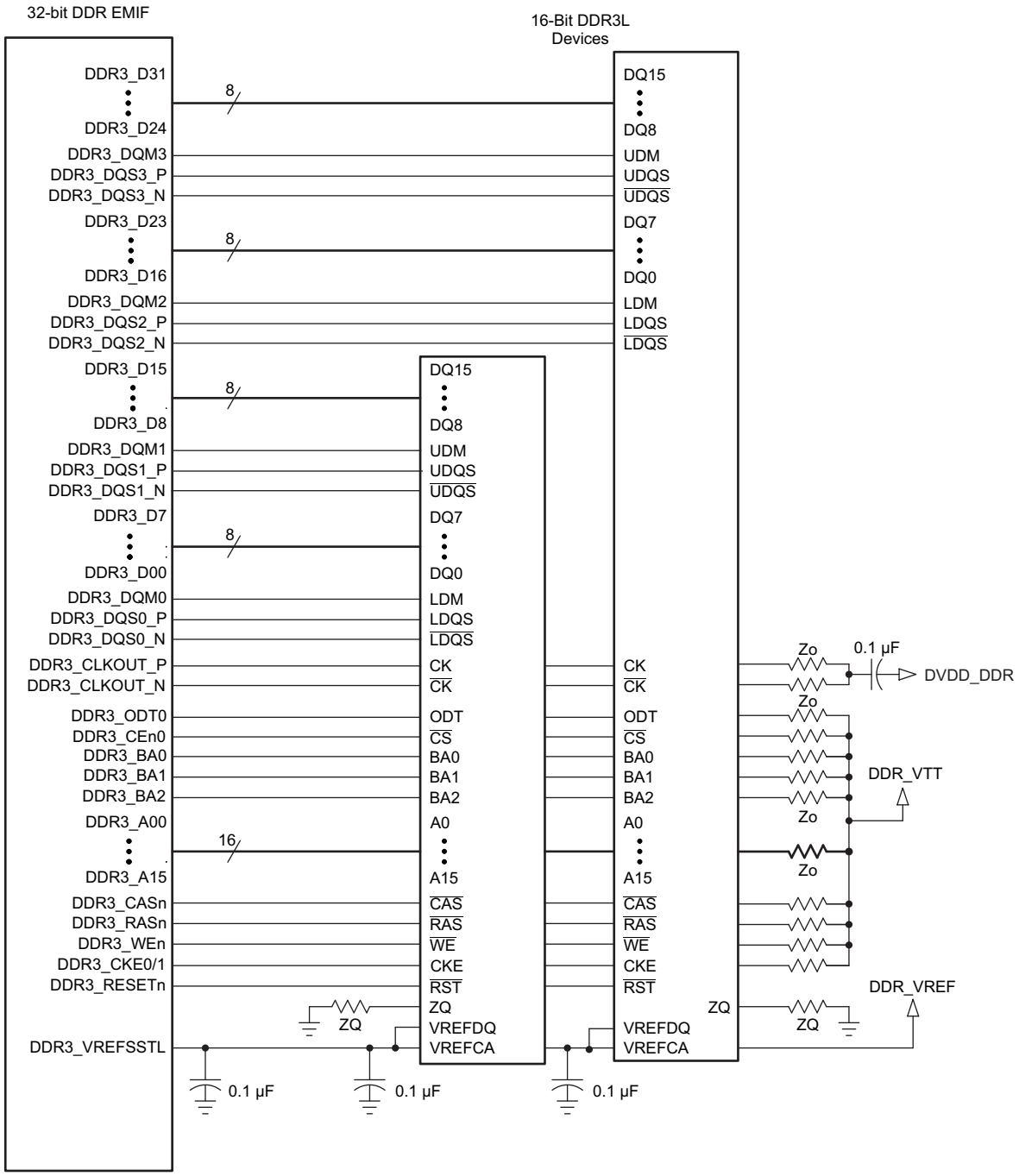
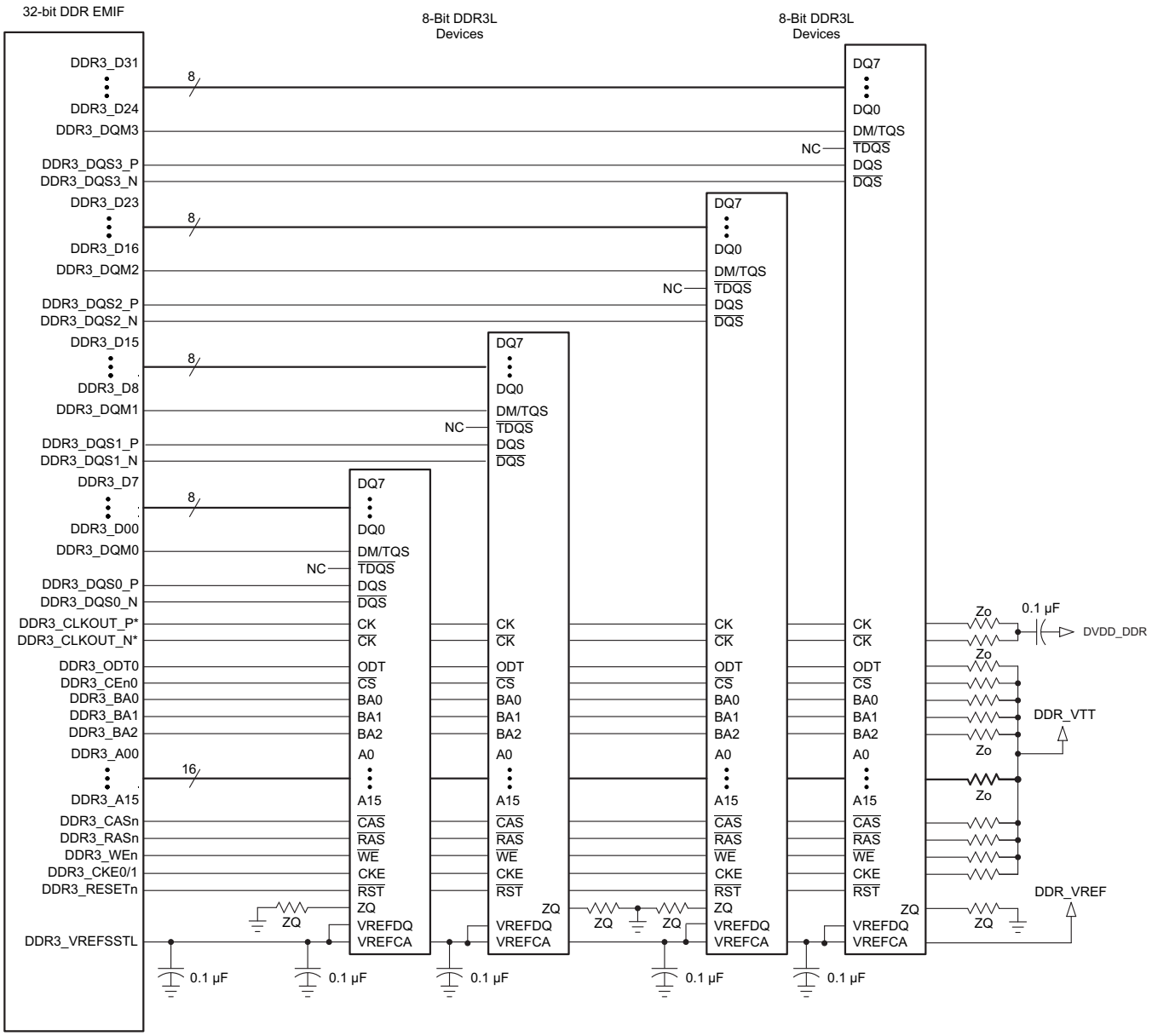


Zo Termination is required. See terminator comments.

ZQ Value determined according to the DDR memory device data sheet.

Figure 7-2. 32-Bit, One-Bank DDR EMIF Interface Schematic Using Two 16-Bit DDR3L Devices



Zo Termination is required. See terminator comments.

ZQ Value determined according to the DDR memory device data sheet.

Figure 7-3. 32-Bit, One-Bank DDR EMIF Interface Schematic Using Four 8-Bit DDR3L Devices

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7.1.2.4 Compatible JEDEC DDR3L Devices

Table 7-3 shows the parameters of the JEDEC DDR3L devices that are compatible with this interface.

Table 7-3. Compatible JEDEC DDR3L Devices

NO.	PARAMETER	CONDITION	MIN	MAX	UNIT
1	JEDEC DDR3L device speed grade(1)	DDR clock rate ≤ 400 MHz	800	1600	MT/s
		400 MHz < DDR clock rate ≤ 533 MHz	1066	1600	MT/s
2	JEDEC DDR3L device bit width		x8	x16	Bits
3	JEDEC DDR3L device count(2)		2	5	Devices

(1) Refer to Table 7-1 Switching Characteristics Over Recommended Operating Conditions for DDR3L Memory Controller for the range of supported DDR clock rates.

(2) For valid DDR3L device configurations and device counts, see Section 7.1.2.2, Figure 7-2, and Figure 7-3.

7.1.2.5 PCB Stackup

The minimum stackup for routing the DDR EMIF interface is a six-layer stack up as shown in Table 7-4. Additional layers may be added to the PCB stackup to accommodate other circuitry, enhance SI/EMI performance, or to reduce the size of the PCB footprint. Complete stackup specifications are provided in Table 7-5.

Table 7-4. Six-Layer PCB Stackup Suggestion

LAYER	TYPE	DESCRIPTION
1	Signal	Top routing mostly vertical
2	Plane	Ground
3	Plane	Split power plane
4	Plane	Split power plane or Internal routing
5	Plane	Ground
6	Signal	Bottom routing mostly horizontal

Table 7-5. PCB Stackup Specifications

NO.	PARAMETER	MIN	TYP	MAX	UNIT
PS1	PCB routing/plane layers	6			
PS2	Signal routing layers	3			
PS3	Full ground reference layers under DDR3L routing region(1)	1			
PS4	Full 1.5-V power reference layers under the DDR3L routing region(1)	1			
PS5	Number of reference plane cuts allowed within DDR3L routing region(2)			0	
PS6	Number of layers between DDR3L routing layer and reference plane(3)			0	
PS7	PCB routing feature size		4		Mils
PS8	PCB trace width, w		4		Mils
PS9	Single-ended impedance, Zo		40	75	Ω
PS10	Impedance control(5)	Z - 5	Z	Z + 5	Ω

(1) Ground reference layers are preferred over power reference layers. Be sure to include bypass caps to accommodate reference layer return current as the trace routes switch routing layers.

(2) No traces should cross reference plane cuts within the DDR3L routing region. High-speed signal traces crossing reference plane cuts create large return current paths which can lead to excessive crosstalk and EMI radiation.

(3) Reference planes are to be directly adjacent to the signal plane to minimize the size of the return current loop.

(4) An 18-mil pad assumes Via Channel is the most economical BGA escape. A 20-mil pad may be used if additional layers are available for power routing. An 18-mil pad is required for minimum layer count escape.

(5) Z is the nominal singled-ended impedance selected for the PCB specified by PS9.

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7.1.2.6 Placement

Figure 7-4 shows the required placement for the processor as well as the DDR3L devices. The dimensions for this figure are defined in Table 7-6. The placement does not restrict the side of the PCB on which the devices are mounted. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For a 16-bit DDR memory system, the high-word DDR3L devices are omitted from the placement.

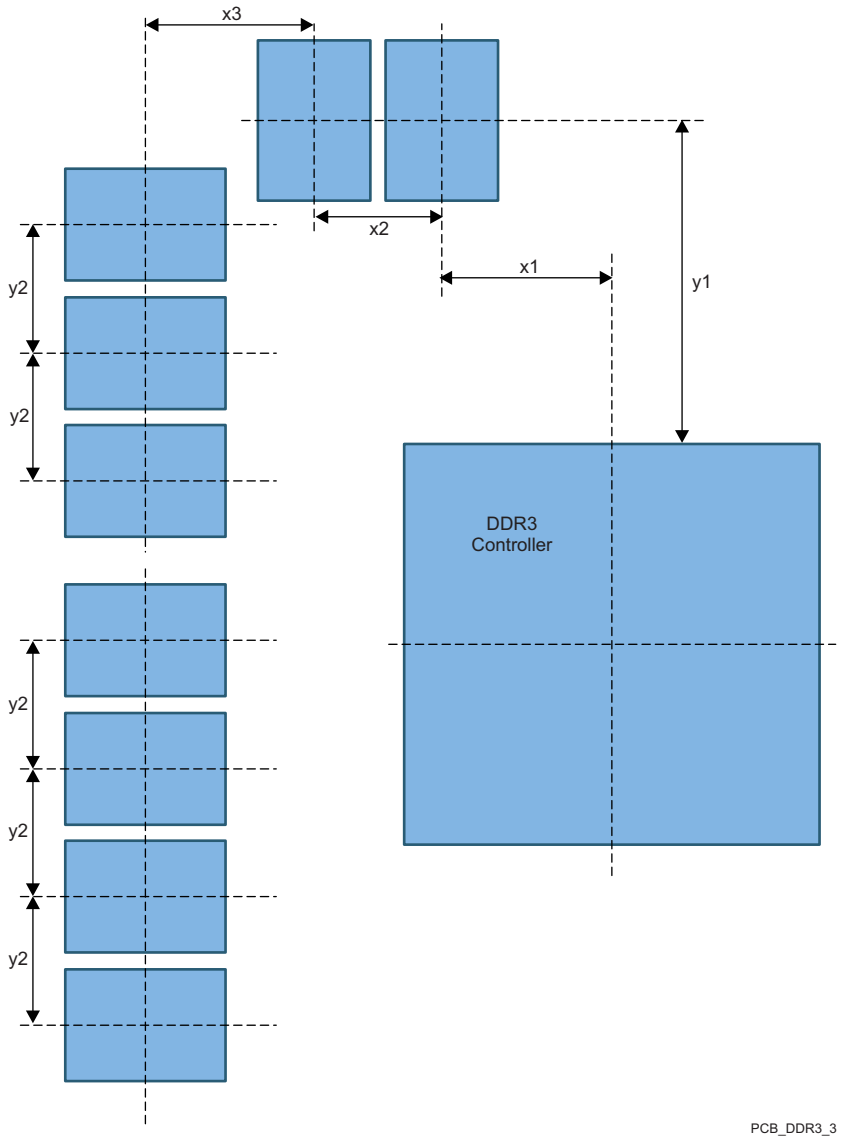

Figure 7-4. Placement Specifications

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Table 7-6. Placement Specifications DDR3L

NO.	PARAMETER	MIN	MAX	UNIT
KOD31	X1		500	Mils
KOD32	X2		600	Mils
KOD33	X3		600	Mils
KOD34	Y1		1800	Mils
KOD35	Y2		600	Mils
KOD36	DDR3L keepout region(1)			
KOD37	Clearance from non-DDR3L signal traces to DDR3L signal traces (2)	4		W

(1) DDR3L keepout region to encompass entire DDR3L routing area.

(2) Non-DDR3L signals allowed within DDR3L keepout region provided they are separated from DDR3L routing layers by a ground plane.

7.1.2.7 DDR3L Keepout Region

The region of the PCB used for DDR3L circuitry must be isolated from other signals. The DDR3L keepout region is defined for this purpose and is shown in Figure 7-5. The size of this region varies with the placement and DDR3L routing. Additional clearances required for the keepout region are shown in Table 7-6. Non-DDR3L signals should not be routed on the DDR3L signal layers within the DDR3L keepout region. Non-DDR3L signals may be routed in the region, provided they are routed on layers separated from the DDR3L signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the DVDD_DDR power plane should cover the entire keepout region. Also note that the two signals from the DDR3L controller should be separated from each other by the specification in Table 7-6 (see KOD37).

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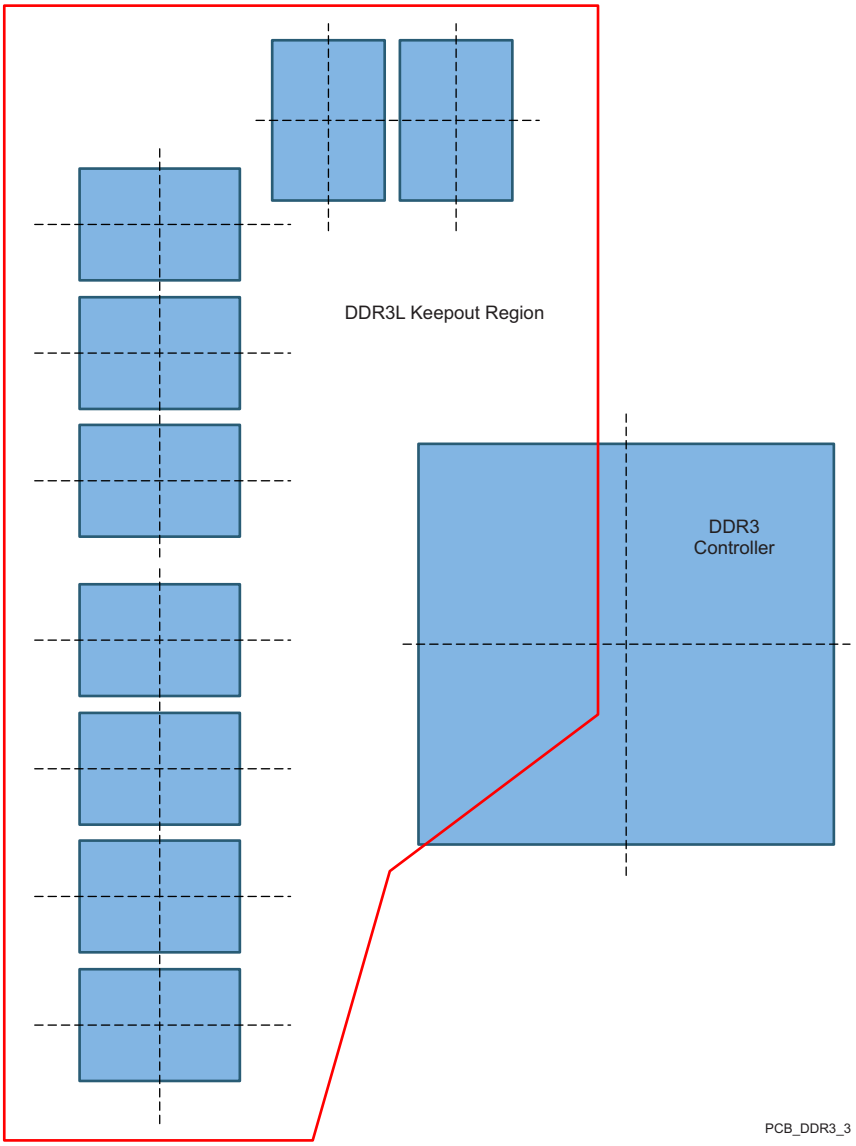

Figure 7-5. DDR3L Keepout Region

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7.1.2.8 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR3L and other circuitry. Table 7-7 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the DDR EMIF controller and DDR3L devices. Additional bulk bypass capacitance may be needed for other circuitry.

Table 7-7. Bulk Bypass Capacitors

NO.	PARAMETER	MIN	MAX	UNIT
1	DVDD_DDR bulk bypass capacitor count(1)	1		Devices
2	DVDD_DDR bulk bypass total capacitance	22		µF

(1) These devices should be placed near the devices they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass capacitors and DDR3L signal routing.

7.1.2.9 High-Speed Bypass Capacitors

High-speed (HS) bypass capacitors are critcal for proper DDR3L interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass capacitors, processor/DDR power, and processor/DDR ground connections. Table 7-8 contains the specification for the HS bypass capacitors as well as for the power connections on the PCB. Generally speaking, it is good to:

1. Fit as many HS bypass capacitors as possible.
2. Minimize the distance from the bypass cap to the pins/balls being bypassed.
3. Use the smallest physical sized capacitors possible with the highest capacitance readily available.
4. Connect the bypass capacitor pads to their vias using the widest traces possible and using the largest hole size via possible.
5. Minimize via sharing. Note the limites on via sharing shown in Table 7-8.

Table 7-8. High-Speed Bypass Capacitors

NO.	PARAMETER	MIN	TYP	MAX	UNIT
1	HS bypass capacitor package size(1)		0201	0402	10 Mils
2	Distance, HS bypass capacitor to processor being bypassed(2)(3)(4)			400	Mils
3	Processor HS bypass capacitor count per DVDD_DDR rail(12)	See Section 7.3 and(11)			Devices
4	Processor HS bypass capacitor total capacitance per DVDD_DDR rail(12)	See Section 7.3 and(11)			µF
5	Number of connection vias for each device power/ground ball(5)				Vias
6	Trace length from device power/ground ball to connection via(2)		35	70	Mils
7	Distance, HS bypass capacitor to DDR3L device being bypassed(6)			150	Mils
8	DDR3L device HS bypass capacitor count(7)	12			Devices
9	DDR3L device HS bypass capacitor total capacitance(7)	0.85			µF
10	Number of connection vias for each HS capacitor(8)(9)	2			Vias
11	Trace length from bypass capacitor connect to connection via(2)(9)		35	100	Mils
12	Number of connection vias for each DDR3L device power/ground ball(10)	1			Vias
13	Trace length from DDR3L device power/ground ball to connection via(2)(8)		35	60	Mils

(1) LxW, 10-mil units, that is, a 0402 is a 40×20-mil surface-mount capacitor.

(2) Closer/shorter is better.

(3) Measured from the nearest processor power/ground ball to the center of the capacitor package.

(4) Three of these capacitors should be located underneath the processor, between the cluster of DVDD_DDR balls and ground balls, between the DDR3L interfaces on the package.

(5) See the Via Channel™ escape for the processor package.

(6) Measured from the DDR3L device power/ground ball to the center of the capacitor package.

(7) Per DDR3L device.

(8) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board. No sharing of vias is permitted on the same side of the board.

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(9) An HS bypass capacitor may share a via with a DDR3L device mounted on the same side of the PCB. A wide trace should be used for the connection and the length from the capacitor pad to the DDR3L device pad should be less than 150 mils.

(10) Up to a total of two pairs of DDR power/ground balls may share a via.

(11) The capacitor recommendations in this data manual reflect only the needs of this processor. Please see the memory vendor's guidelines for determining the appropriate decoupling capacitor arrangement for the memory device itself.

(12) For more information, see Section 7.3, *Power Distribution Network Implementation Guidance*.

7.1.2.9.1 Return Current Bypass Capacitors

Use additional bypass capacitors if the return current reference plane changes due to DDR3L signals hopping from one signal layer to another. The bypass capacitor here provides a path for the return current to hop planes along with the signal. As many of these return current bypass capacitors should be used as possible. Because these are returns for signal current, the signal via size may be used for these capacitors.

7.1.2.10 Net Classes

Table 7-9 lists the clock net classes for the DDR EMIF. Table 7-10 lists the signal net classes, and associated clock net classes, for signals in the DDR EMIF. These net classes are used for the termination and routing rules that follow.

Table 7-9. Clock Net Class Definitions

CLOCK NET CLASS	PROCESSOR PIN NAMES
CK	DDR3_CLKOUT_N* / DDR3_CLKOUT_P*
DQS0	DDR3_DQS0_P / ddrx_dqsn0
DQS1	DDR3_DQS0_P / DDR3_DQS0_N
DQS2(1)	DDR3_DQS1_P / DDR3_DQS1_N
DQS3(1)	DDR3_DQS2_P / DDR3_DQS2_N

(1) Only used on 32-bit wide DDR3L memory systems.

Table 7-10. Signal Net Class Definitions

SIGNAL NET CLASS	ASSOCIATED CLOCK NET CLASS	PROCESSOR PIN NAMES
ADDR_CTRL	CK	DDR3_BA[2:0], DDR3_A[14:0], DDR3_CEn0, DDR3_CASn, DDR3_RASn, DDR3_WEn, DDR3_CKE0, DDR3_ODT0
DQ0	DQS0	DDR3_D[7:0], DDR3_DQM0
DQ1	DQS1	DDR3_D[15:8], DDR3_DQM1
DQ2(1)	DQS2	DDR3_D[23:16], DDR3_DQM2
DQ3(1)	DQS3	DDR3_D[31:24], DDR3_DQM3

(1) Only used on 32-bit wide DDR3L memory systems.

7.1.2.11 DDR3L Signal Termination

Signal terminators are required for the CK and ADDR_CTRL net classes. The data lines are terminated by ODT and, thus, the PCB traces should be unterminated. Detailed termination specifications are covered in the routing rules in the following sections.

7.1.2.12 VREF_DDR Routing

DDR3_VREFSSTL (VREF) is used as a reference by the input buffers of the DDR3L memories as well as the processor. VREF is intended to be half the DDR3L power supply voltage and is typically generated with the DVDD_DDR and VTT power supply. It should be routed as a nominal 20-mil wide trace with 0.1 µF bypass capacitors near each device connection. Narrowing of VREF is allowed to accommodate routing congestion.

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7.1.2.13 VTT

Like VREF, the nominal value of the VTT supply is half the DDR3L supply voltage. Unlike VREF, VTT is expected to source and sink current, specifically the termination current for the ADDR_CTRL net class Thevinen terminators. VTT is needed at the end of the address bus and it should be routed as a power sub-plane. VTT should be bypassed near the terminator resistors.

7.1.2.14 CK and ADDR_CTRL Topologies and Routing Definition

The CK and ADDR_CTRL net classes are routed similarly and are length matched to minimize skew between them. CK is a bit more complicated because it runs at a higher transition rate and is differential. The following subsections show the topology and routing for various DDR3L configurations for CK and ADDR_CTRL. The figures in the following subsections define the terms for the routing specification detailed in Table 7-11.

7.1.2.14.1 Four DDR3L Devices

Four DDR3L devices are supported on the DDR EMIF consisting of four x8 DDR3L devices arranged as one bank (CS). These four devices may be mounted on a single side of the PCB, or may be mirrored in two pairs to save board space at a cost of increased routing complexity and parts on the backside of the PCB.

7.1.2.14.1.1 CK and ADDR_CTRL Topologies, Four DDR3L Devices

Figure 7-6 shows the topology of the CK net classes and Figure 7-7 shows the topology for the corresponding ADDR_CTRL net classes.

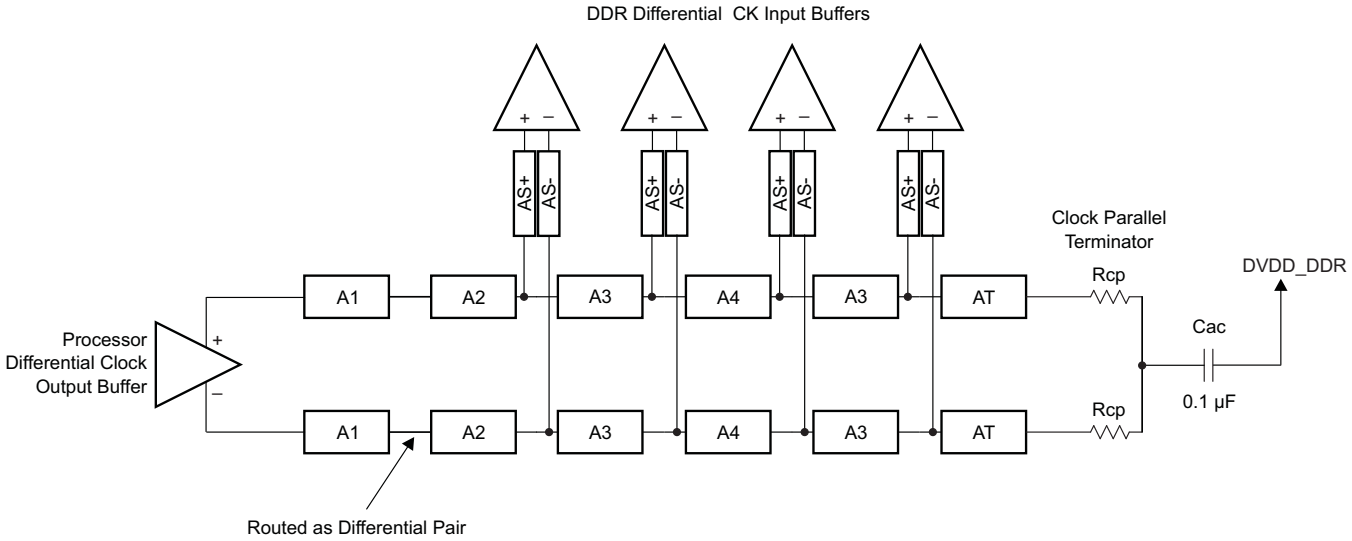

Figure 7-6. CK Topology for Four x8 DDR3L Devices

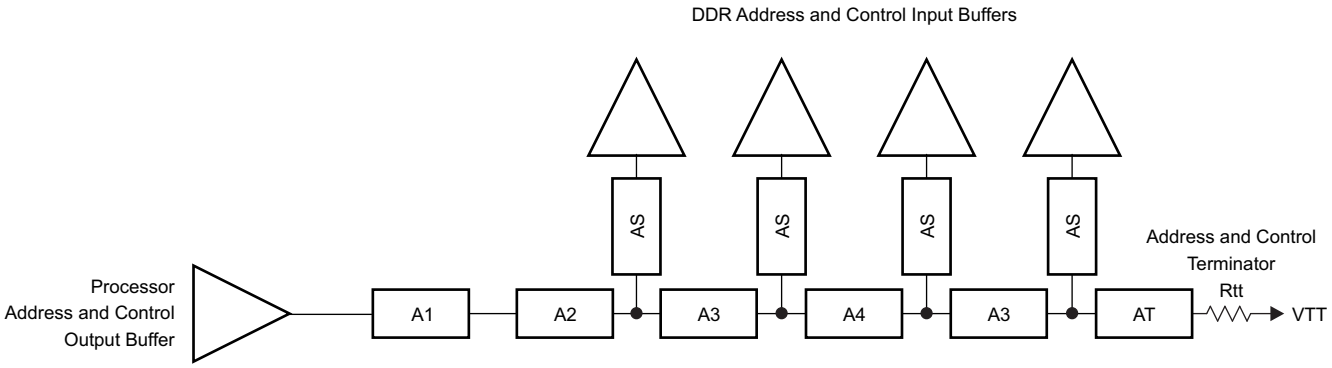

Figure 7-7. ADDR_CTRL Topology for Four x8 DDR3L Devices

7.1.2.14.1.2 CK and ADDR_CTRL Routing, Four DDR3L Devices

Figure 7-8 shows the CK routing for four DDR3L devices placed on the same side of the PCB. Figure 7-9 shows the corresponding ADDR_CTRL routing.

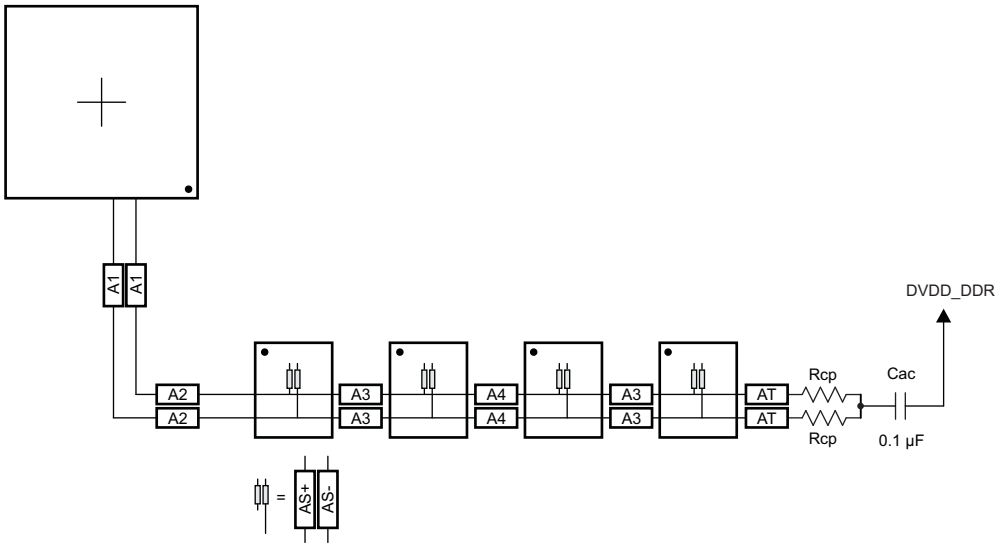

Figure 7-8. CK Routing for Four Single-Side DDR3L Devices

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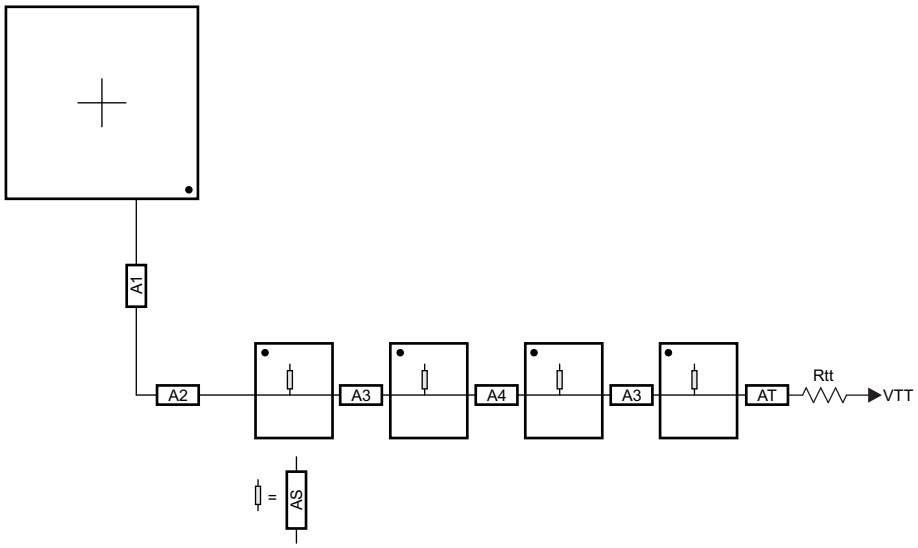

Figure 7-9. ADDR_CTRL Routing for Four Single-Side DDR3L Devices

To save PCB space, the four DDR3L memories may be mounted as two mirrored pairs at a cost of increased routing and assembly complexity. Figure 7-10 and Figure 7-11 show the routing for CK and ADDR_CTRL, respectively, for four DDR3L devices mirrored in a two-pair configuration.

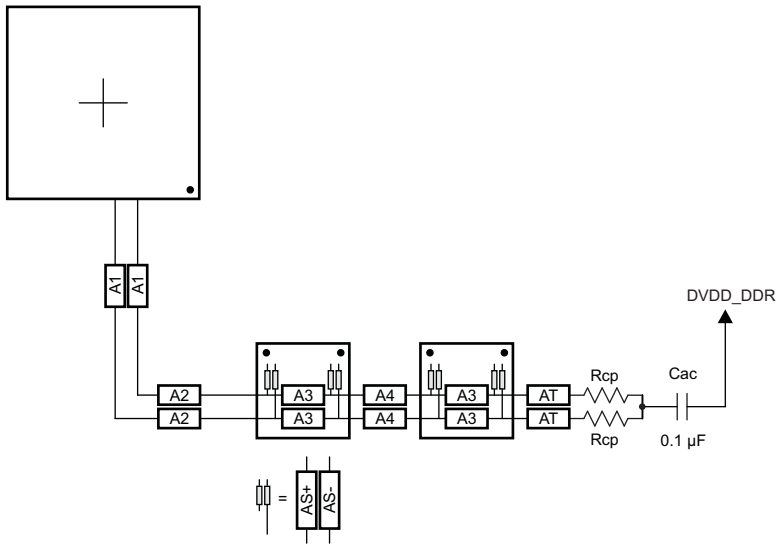

Figure 7-10. CK Routing for Four Mirrored DDR3L Devices

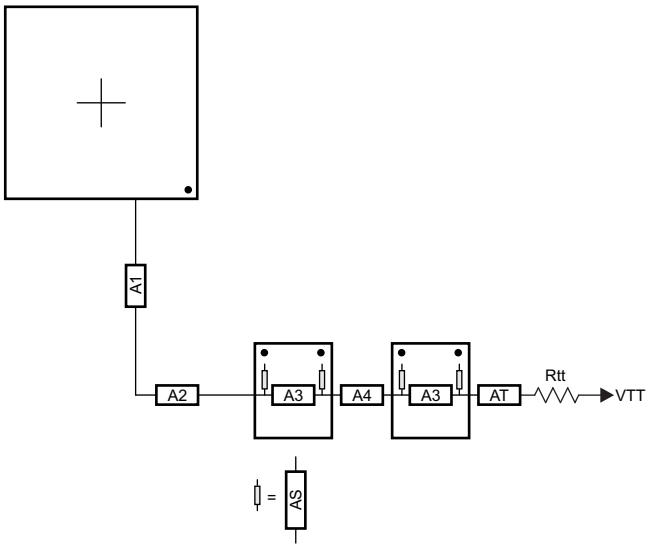

Figure 7-11. ADDR_CTRL Routing for Four Mirrored DDR3L Devices

7.1.2.14.2 One DDR3L Device

A single DDR3L device is supported on the DDR EMIF consisting of one x16 DDR3L device arranged as one bank (CS), 16 bits wide.

7.1.2.14.2.1 CK and ADDR_CTRL Topologies, One DDR3L Device

Figure 7-12 shows the topology of the CK net classes and Figure 7-13 shows the topology for the corresponding ADDR_CTRL net classes.

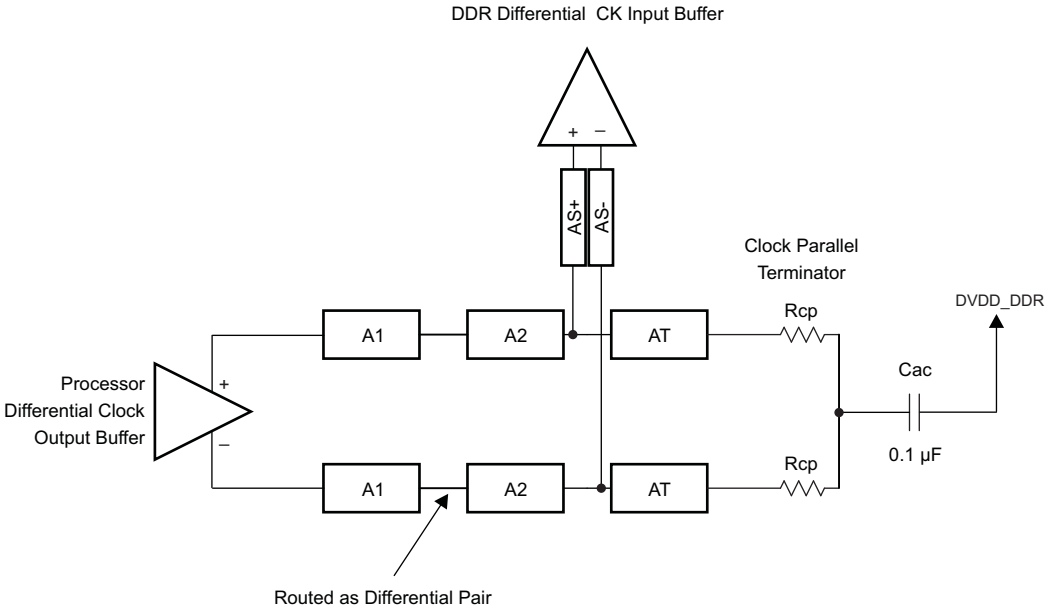

Figure 7-12. CK Topology for One DDR3L Device

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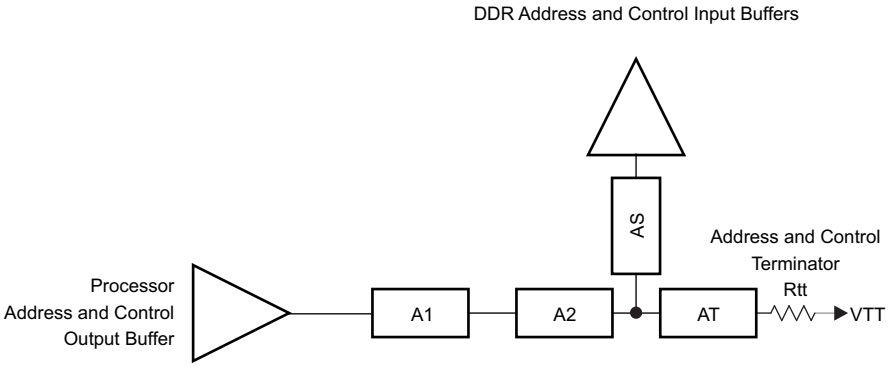

Figure 7-13. ADDR_CTRL Topology for One DDR3L Device

7.1.2.14.2.2 CK and ADDR/CTRL Routing, One DDR3L Device

Figure 7-14 shows the CK routing for one DDR3L device placed on the same side of the PCB. Figure 7-15 shows the corresponding ADDR_CTRL routing.

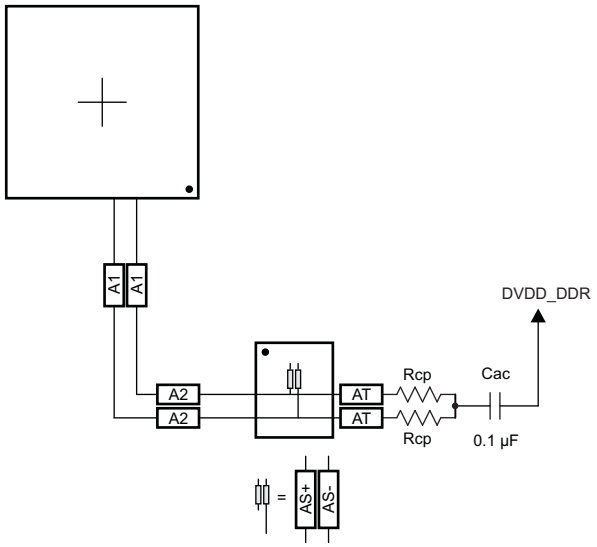

Figure 7-14. CK Routing for One DDR3L Device

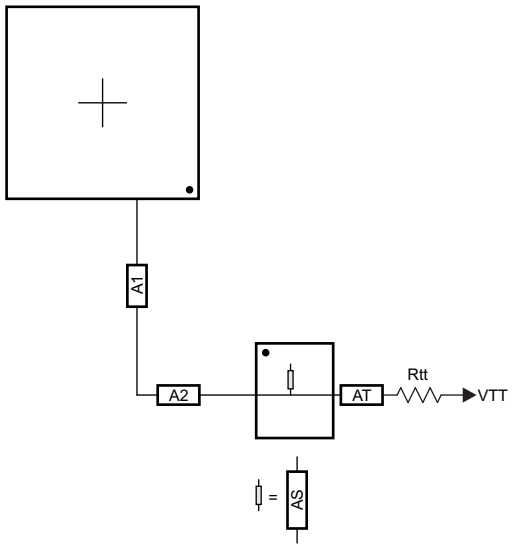

Figure 7-15. ADDR_CTRL Routing for One DDR3L Device

7.1.2.15 Data Topologies and Routing Definition

No matter the number of DDR3L devices used, the data line topology is always point to point, so its definition is simple.

Care should be taken to minimize layer transitions during routing. If a layer transition is necessary, it is better to transition to a layer using the same reference plane. If this cannot be accommodated, ensure there are nearby ground vias to allow the return currents to transition between reference planes if both reference planes are ground or DVDD_DDR. Ensure there are nearby bypass capacitors to allow the return currents to transition between reference planes if one of the reference planes is ground. The goal is to minimize the size of the return current loops.

7.1.2.15.1 DQS and DQ/DM Topologies, Any Number of Allowed DDR3L Devices

DQS lines are point-to-point differential, and DQ/DM lines are point-to-point singled ended. Figure 7-16 and Figure 7-17 show these topologies.

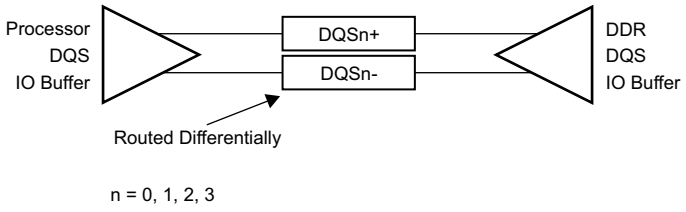

Figure 7-16. DQS Topology

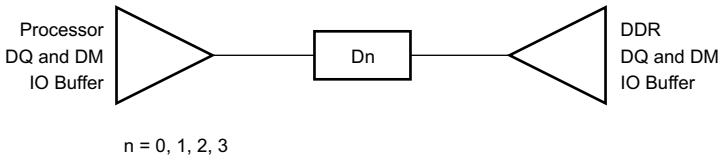

Figure 7-17. DQ/DM Topology

7.1.2.15.2 DQS and DQ/DM Routing, Any Number of Allowed DDR3L Devices

Figure 7-18 and Figure 7-19 show the DQS and DQ/DM routing.

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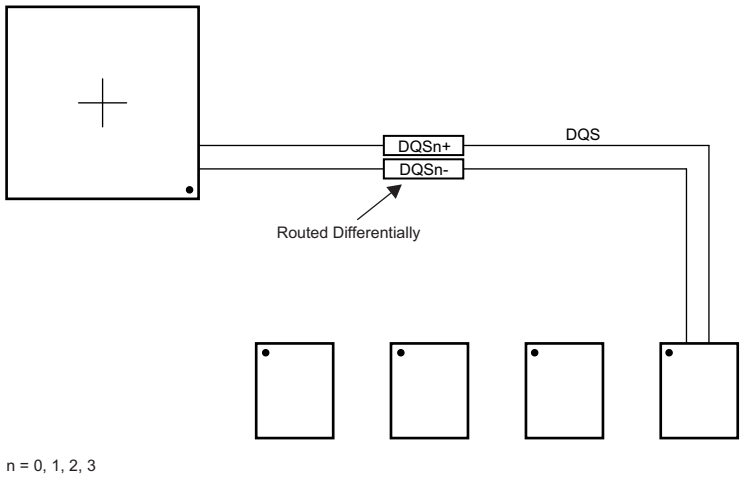

Figure 7-18. DQS Routing With Any Number of Allowed DDR3L Devices

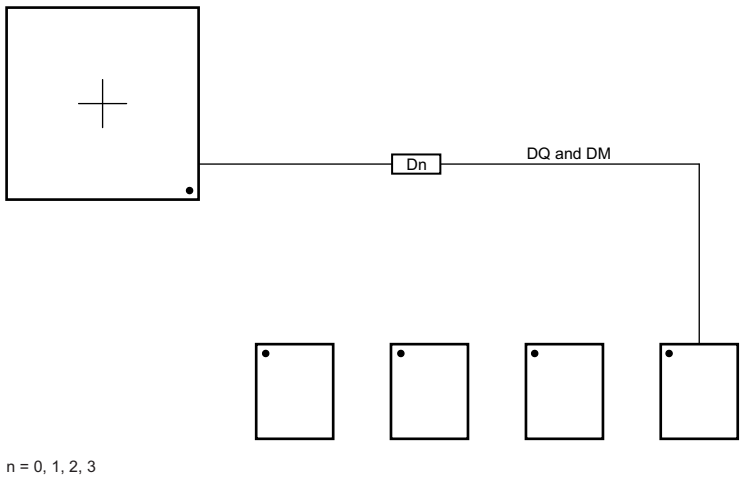

Figure 7-19. DQ/DM Routing With Any Number of Allowed DDR3L Devices

7.1.2.16 Routing Specification

7.1.2.16.1 CK and ADDR_CTRL Routing Specification

Skew within the CK and ADDR_CTRL net classes directly reduces setup and hold margin and, thus, this skew must be controlled. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. A metric to establish this maximum length is Manhattan distance. The Manhattan distance between two points on a PCB is the length between the points when connecting them only with horizontal or vertical segments. A reasonable trace route length is to within a percentage of its Manhattan distance. CACLM is defined as Clock Address Control Longest Manhattan distance.

Given the clock and address pin locations on the processor and the DDR3L memories, the maximum possible Manhattan distance can be determined given the placement. Figure 7-20 and Figure 7-21 show this distance for four loads and two loads, respectively. It is from this distance that the specifications on the lengths of the transmission lines for the address bus are determined. CACLM is determined similarly for other address bus configurations; that is, it is based on the longest net of the CK/ADDR_CTRL net class. For CK and ADDR_CTRL routing, these specifications are contained in Table 7-11.

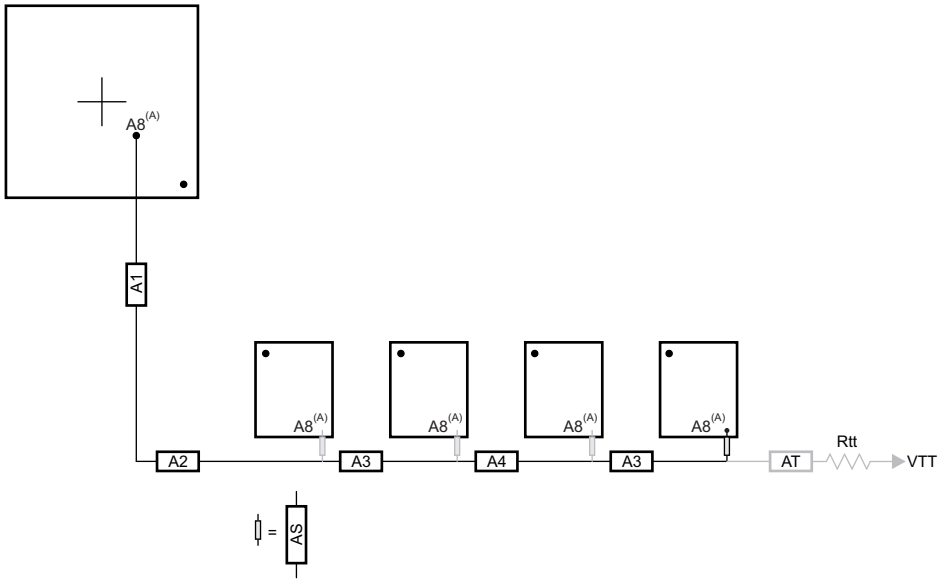

Figure 7-20. Four Address Loads on One Side of PCB

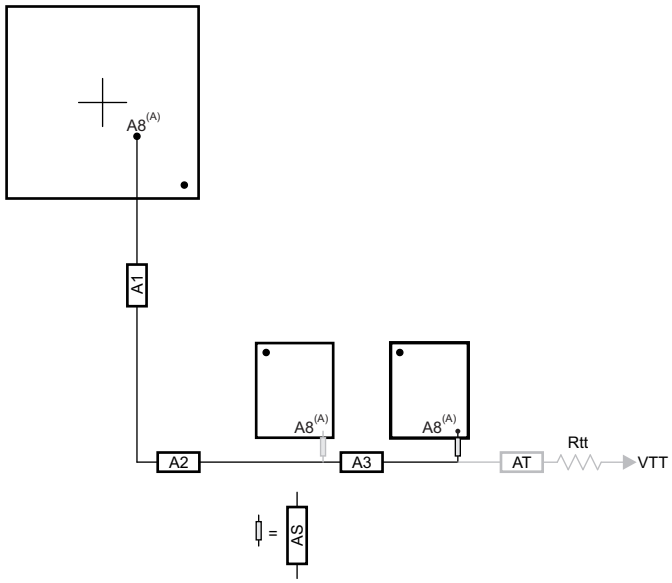

Figure 7-21. Two Address Loads on One Side of PCB

Table 7-11. CK and ADDR_CTRL Routing Specification[(2)(3)]

NO.	PARAMETER	MIN	TYP	MAX	UNIT
CARS31	A1+A2 length			500[(1)]	ps
CARS32	A1+A2 skew			29	ps
CARS33	A3 length			125	ps
CARS34	A3 skew[(4)]			6	ps
CARS35	A3 skew[(5)]			6	ps
CARS36	A4 length			125	ps
CARS37	A4 skew			6	ps
CARS38	AS length		5[(1)]	17	ps
CARS39	AS skew		1.3[(1)]	14	ps

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Table 7-11. CK and ADDR_CTRL Routing Specification[2][3] (continued)

NO.	PARAMETER	MIN	TYP	MAX	UNIT
CARS310	AS+/AS- length		5	12	ps
CARS311	AS+/AS- skew			1	ps
CARS312	AT length[6]		75		ps
CARS313	AT skew[7]		14		ps
CARS314	AT skew[8]			1	ps
CARS315	CK/ADDR_CTRL trace length			1020	ps
CARS316	Vias per trace			3[1]	vias
CARS317	Via count difference			1[15]	vias
CARS318	Center-to-center CK to other DDR3L trace spacing[9]	4w			
CARS319	Center-to-center ADDR_CTRL to other DDR3L trace spacing[9][10]	4w			
CARS320	Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing[9]	3w			
CARS321	CK center-to-center spacing[11][12]				
CARS322	CK spacing to other net[9]	4w			
CARS323	Rcp[13]	Zo-1	Zo	Zo+1	Ω
CARS324	Rtt[13][14]	Zo-5	Zo	Zo+5	Ω

(1) Max value is based upon conservative signal integrity approach. This value could be extended only if detailed signal integrity analysis of rise time and fall time confirms desired operation.

(2) The use of vias should be minimized.

(3) Additional bypass capacitors are required when using the DVDD_DDR plane as the reference plane to allow the return current to jump between the DVDD_DDR plane and the ground plane when the net class switches layers at a via.

(4) Non-mirrored configuration (all DDR3L memories on same side of PCB).

(5) Mirrored configuration (one DDR3L device on top of the board and one DDR3L device on the bottom).

(6) While this length can be increased for convenience, its length should be minimized.

(7) ADDR_CTRL net class only (not CK net class). Minimizing this skew is recommended, but not required.

(8) CK net class only.

(9) Center-to-center spacing is allowed to fall to minimum 2w for up to 1250 mils of routed length.

(10) The ADDR_CTRL net class of the other DDR EMIF is considered *other DDR3L trace spacing*.

(11) CK spacing set to ensure proper differential impedance.

(12) The most important thing to do is control the impedance so inadvertent impedance mismatches are not created. Generally speaking, center-to-center spacing should be either 2w or slightly larger than 2w to achieve a differential impedance equal to twice the singleended impedance, Zo.

(13) Source termination (series resistor at driver) is specifically not allowed.

(14) Termination values should be uniform across the net class.

(15) Via count difference may increase by 1 only if accurate 3D modeling of the signal flight times – including accurately modeled signal propagation through vias – has been applied to ensure all segment skew maximums are not exceeded.

7.1.2.16.2 DQS and DQ Routing Specification

Skew within the DQS and DQ/DM net classes directly reduces setup and hold margin and thus this skew must be controlled. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. As with CK and ADDR_CTRL, a reasonable trace route length is to within a percentage of its Manhattan distance. DQLMn is defined as DQ Longest Manhattan distance n, where n is the byte number. For a 32-bit interface, there are four DQLMs, DQLM0-DQLM3. Likewise, for a 16-bit interface, there are two DQLMs, DQLM0-DQLM1.

Given the DQS and DQ/DM pin locations on the processor and the DDR3L memories, the maximum possible Manhattan distance can be determined given the placement. Figure 7-22 shows this distance for four loads. It is from this distance that the specifications on the lengths of the transmission lines for the data bus are determined. For DQS and DQ/DM routing, these specifications are contained in Table 7-12.

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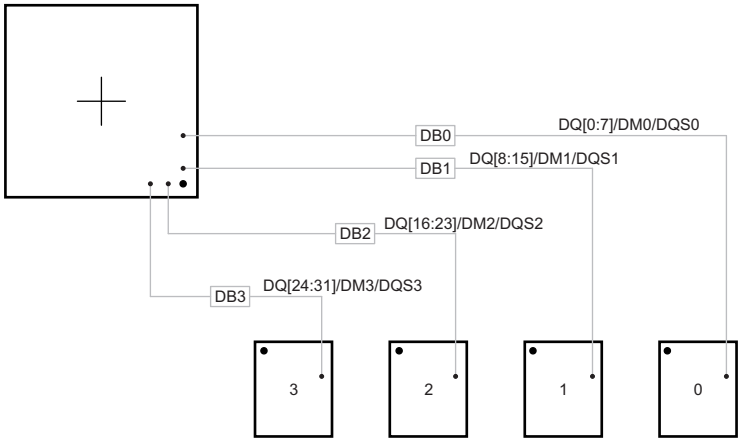

DB0 - DB3 represent data bytes 0 - 3.

Figure 7-22. Any Number of Allowed DDR3L Devices

Table 7-12. Data Routing Specification(2)(11)

NO.	PARAMETER	MIN	TYP	MAX	UNIT
DRS31	DB0 length			340	ps
DRS32	DB1 length			340	ps
DRS33	DB2 length			340	ps
DRS34	DB3 length			340	ps
DRS35	DBn skew(3)			5	ps
DRS36	DQSn+ to DQSn- skew			1	ps
DRS37	DQSn to DBn skew(3)(4)			5(10)	ps
DRS38	Vias per trace			2(1)	vias
DRS39	Via count difference			0(10)	vias
DRS310	Center-to-center DBn to other DDR3L trace spacing(6)	4			w(5)
DRS311	Center-to-center DBn to other DBn trace spacing(7)	3			w(5)
DRS312	DQSn center-to-center spacing(8)(9)				
DRS313	DQSn center-to-center spacing to other net	4			w(5)

(1) Max value is based upon conservative signal integrity approach. This value could be extended only if detailed signal integrity analysis of rise time and fall time confirms desired operation.

(2) External termination disallowed. Data termination should use built-in ODT functionality.

(3) Length matching is only done within a byte. Length matching across bytes is neither required nor recommended.

(4) Each DQS pair is length matched to its associated byte.

(5) Center-to-center spacing is allowed to fall to minimum 2w for up to 1250 mils of routed length.

(6) Other DDR3L trace spacing means other DDR3L net classes not within the byte.

(7) This applies to spacing within the net classes of a byte.

(8) DQS pair spacing is set to ensure proper differential impedance.

(9) The most important thing to do is control the impedance so inadvertent impedance mismatches are not created. Generally speaking, center-to-center spacing should be either 2w or slightly larger than 2w to achieve a differential impedance equal to twice the singleended impedance, Zo.

(10) Via count difference may increase by 1 only if accurate 3D modeling of the signal flight times – including accurately modeled signal propagation through vias – has been applied to ensure DBn skew and DQSn to DBn skew maximums are not exceeded.

(11) It is not required to match lengths across all bytes. Length matching is only required within the data bits of a given byte.

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7.2 High Speed Differential Signal Routing Guidance

The *High-Speed Interface Layout Guidelines Application Report (SPRAAR7)* available from http://www.ti.com/lit/pdf/spraar7 provides guidance for successful routing of the high speed differential signals. This includes PCB stackup and materials guidance as well as routing skew, length and spacing limits. TI supports *only* designs that follow the board design guidelines contained in the application report.

7.3 Power Distribution Network (PDN) Implementation Guidance

66AK2G1x: EVMK2GX General Purpose EVM Power Distribution Network Analysis [literature number SPRACE6] provides guidance for successful implementation of the PDN. This includes PCB stack-up guidance as well as guidance for optimizing the selection and placement of the decoupling capacitors. TI supports only designs that follow the board design guidelines contained in the application report.

7.3.1 Decoupling/Filtering of Analog Power Supplies and Reference Inputs

7.3.1.1 PLL Power Supplies

The analog VDD pins with a prefix of AVDDA_ provide power to internal PLLs. Each of these analog VDD pins shall be connected to DVDD18 through a dedicated low-pass filter. Each filter shall reduce power supply noise of the respective analog VDD pin such that it has less than 250-mV peak-to-peak noise while remaining within the voltage ranged defined in Section 5.4, *Recommended Operating Conditions*.

7.3.1.2 DDR EMIF PHY DLL Power Supplies

The DVDD_DDRDLL pins provide power to DDR EMIF PHY DLLs. These supply pins must be filtered such that they have less than 36-mV peak-to-peak noise while remaining within the voltage ranged defined in Section 5.4, *Recommended Operating Conditions*.

The recommended circuit topology for this filter is shown in Figure 7-23.

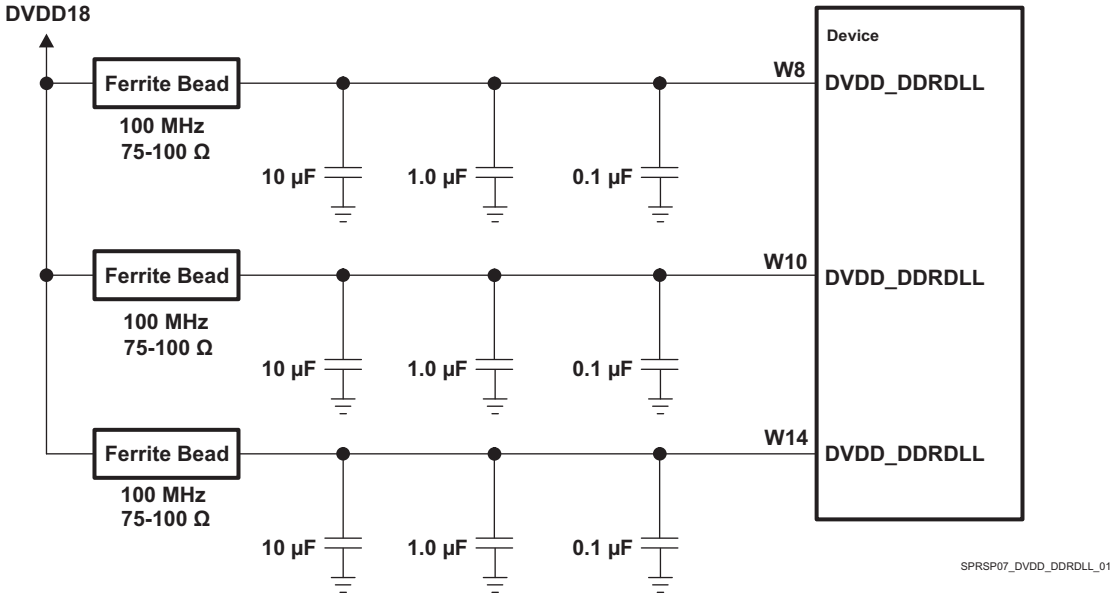

Figure 7-23. Recommended DVDD_DDRDLL Filter Circuit

7.3.1.3 DDR EMIF PHY Voltage Reference Input

DDR3_VREFSSTL is a mid-supply voltage reference input which the DDR EMIF PHY uses as the switching threshold for its input buffers. This pin must be filtered such that it has less than 13.5-mV peak-to-peak noise while remaining within the voltage ranged defined in Section 5.4, *Recommended Operating Conditions*.

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7.3.1.4 Internal LDO Outputs

There are two internal LDOs that require external decoupling capacitors.

The LDO_PCIE_CAP pins are connected to the output of an internal LDO that sources the PCIe PHY core power rail. A single 1.0 µF, ±50% decoupling capacitor with ESR of 10–100 mΩ must be connected between the LDO_PCIE_CAP pins and VSS with less than 0.5 nH of loop inductance.

The LDO_USB_CAP pins are connected to the output of an internal LDO that sources both USB PHY core power rails. A single 1.0 µF, ±50% decoupling capacitor with ESR of 10–100 mΩ must be connected between the LDO_USB_CAP pins and VSS with less than 0.5 nH of loop inductance.

7.3.1.5 PCIe PHY Power Supply

The VDDAHV pin provides power to the PCIe PHY. This supply pin must be filtered such that it has less than 50-mV peak-to-peak noise while remaining within the voltage ranged defined in Section 5.4, *Recommended Operating Conditions*.

7.3.1.6 USB PHY Power Supplies

The DVDD33_USB pins provide power to the USB PHYs. These supply pins must be filtered such that they have less than 198-mV peak-to-peak noise while remaining within the voltage ranged defined in Section 5.4, *Recommended Operating Conditions*.

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7.4 Single-Ended Interfaces

7.4.1 General Routing Guidelines

The following paragraphs detail the routing guidelines that must be observed when routing the various functional LVCMOS interfaces.

- Line spacing:
  - For a line width equal to W, the spacing between two lines must be 2 W, at least. This minimizes the crosstalk between switching signals between the different lines. On the PCB, this is not achievable everywhere (for example, when breaking signals out from the device package), but it is recommended to follow this rule as much as possible. When violating this guideline, minimize the length of the traces running parallel to each other (see Figure 7-24).

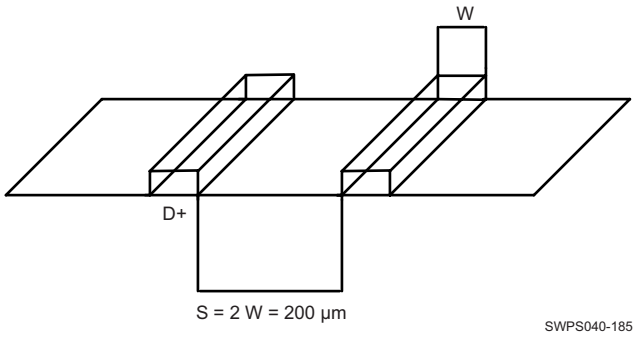

Figure 7-24. Ground Guard Illustration

- Length matching (unless otherwise specified):
  - For bus or traces at frequencies less than 10 MHz, the trace length matching (maximum length difference between the longest and the shortest lines) must be less than 25 mm.
  - For bus or traces at frequencies greater than 10 MHz, the trace length matching (maximum length difference between the longest and the shortest lines) must be less than 2.5 mm.
- Characteristic impedance
  - Unless otherwise specified, the characteristic impedance for single-ended interfaces is recommended to be between 35-Ω and 65-Ω.
- Multiple peripheral support
  - For interfaces where multiple peripherals have to be supported in the star topology, the length of each branch has to be balanced. Before closing the PCB design, it is highly recommended to verify signal integrity based on simulations including actual PCB extraction.

7.5 Clock Routing Guidelines

7.5.1 Oscillator Routing

When designing the printed-circuit board:

- Place the crystal circuit on the same side of the PCB as the 66AK2G1x device and as close as possible to the respective device pins SYSOSC_IN / SYSOSC_OUT, or AUDOSC_IN / AUDOSC_OUT.
- The crystal circuit traces should be placed on the outer layer of the PCB when possible, with the lengths being as short as possible to reduce parasitic capacitance and minimize crosstalk from other signals.
- Do not route any other signals under the crystal circuit traces if there is an adjacent signal layer on the PCB.
- Route all crystal circuit component ground connections to one common ground via. This via must directly connect to the ground plane.
- Treat VSS_OSC_AUDIO and VSS_OSC_SYS pins the same way as other device VSS pins: connect them to board ground as near to the ball as possible.

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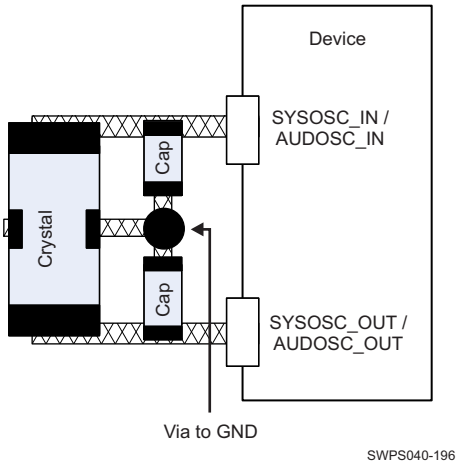

Figure 7-25. SYSOSC and AUDIOOSC PCB requirements

7.5.2 Oscillator Ground Connection

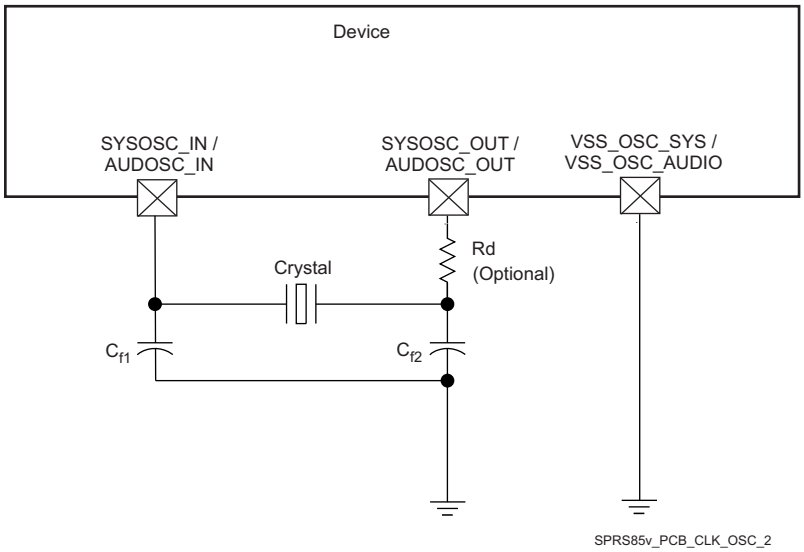

Figure 7-26. Grounding Scheme for internal oscillators

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8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, 66AK2G12). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ABY), the temperature range (for example, blank is the default commercial temperature range), and the device speed range, in megahertz (for example, *60 is 600 MHz*). Figure 8-1 provides a legend for reading the complete device name for any 66AK2G1x device.

For orderable part numbers of 66AK2G1x devices in the ABY package type, see the Package Option Addendum of this document, the TI website (www.ti.com), or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the Device Silicon Errata.

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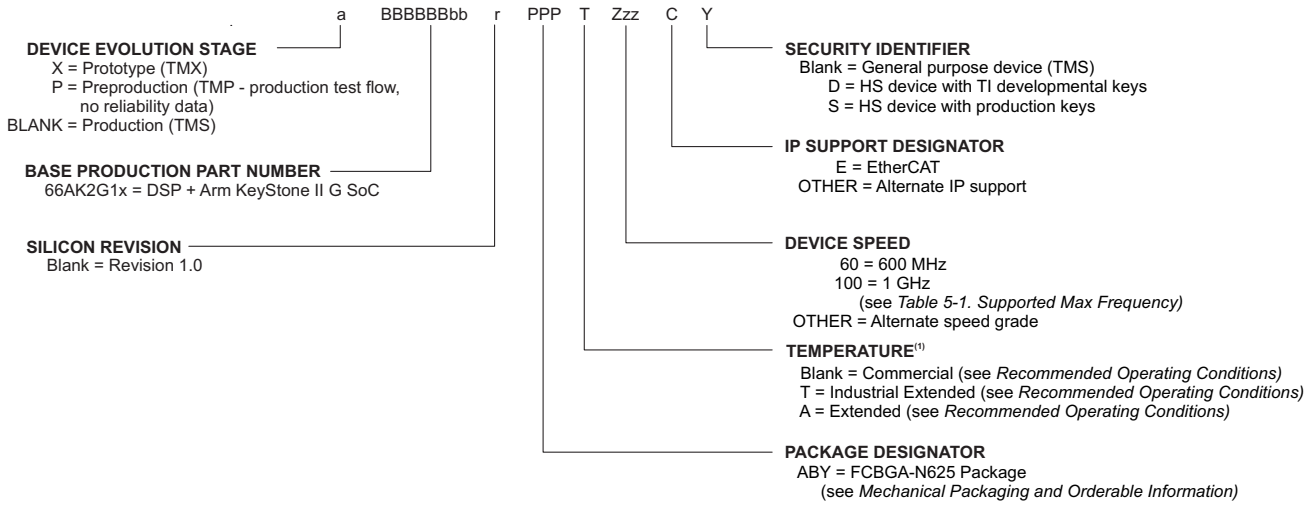

Figure 8-1. Device Nomenclature

(1) Applies to device max junction temperature.

8.2 Tools and Software

The following products support development for 66AK2G platforms:

Design kits and evaluation modules

EVMK2GX Evaluation Module (EVM) enables developers to immediately start evaluating the 66AK2Gx processor family, and to accelerate the development of audio, industrial motor control, smart grid protection and other high reliability, real-time compute intensive applications. Similar to existing KeyStone-based SoC devices, the 66AK2Gx enables both the DSP and ARM cores to master all memory and peripherals in the system. This architecture facilitates maximum software flexibility where either DSP- or ARM-centric system designs can be achieved..

Development tools

Clock Tree Tool for Sitara, Automotive, Vision Analytics, & Digital Signal Processors The Clock Tree Tool (CTT) for Sitara™ ARM®, Automotive, and Digital Signal Processors is an interactive clock tree configuration software that provides information about the clocks and modules in these TI devices. It allows the user to:

- Visualize the device clock tree
- Interact with clock tree elements and view the effect on PRCM registers
- Interact with the PRCM registers and view the effect on the device clock tree
- View a trace of all the device registers affected by the user interaction with clock tree

Code Composer Studio™ (CCS) Integrated Development Environment (IDE) for Sitara ARM Processors Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

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Pin mux tool The Pin MUX Utility is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI MPUs. Results are output as C header/code files that can be imported into software development kits (SDKs) or used to configure customer's custom software. Version 4 of the Pin Mux utility adds the capability of automatically selecting a mux configuration that satisfies the entered requirements.

Models

66AK2G12 BSDL Model BSDL Model

66AK2G12 IBIS File IBIS Model

66AK2G12 Thermal Models Thermal Model

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

8.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the processor, related peripherals, and other technical collateral is listed below:

Technical Reference Manual

66AK2G1x Multicore DSP+Arm KeyStone II System-on-Chip (SoC) Technical Reference Manual
Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the 66AK2G family of devices.

Errata

66AK2G1x Silicon Errata
Describes known exceptions to the functional specifications (advisories) with workarounds and situations where the device's behavior may not match presumed or documented behavior (usage notes).

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

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9 Mechanical, Packaging, and Orderable Information

9.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
66AK2G12ABY100	ACTIVE	FCCSP	ABY	625	60	RoHS & Green	Call TI	Level-3-260C-168 HR	0 to 90	66AK2G12ABY100 742 ABY	Samples
66AK2G12ABY60	ACTIVE	FCCSP	ABY	625	60	RoHS & Green	Call TI	Level-3-260C-168 HR	0 to 90	66AK2G12ABY60 742 ABY	Samples
66AK2G12ABYA100	ACTIVE	FCCSP	ABY	625	60	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 105	66AK2G12ABYA100 742 ABY	Samples
66AK2G12ABYA100E	ACTIVE	FCCSP	ABY	625	60	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 105	66AK2G12ABYA100E 742 ABY	Samples
66AK2G12ABYA60	ACTIVE	FCCSP	ABY	625	60	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 105	66AK2G12ABYA60 742 ABY	Samples
66AK2G12ABYA60E	ACTIVE	FCCSP	ABY	625	60	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 105	66AK2G12ABYA60E 742 ABY	Samples
66AK2G12ABYT100	ACTIVE	FCCSP	ABY	625	60	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 125	66AK2G12ABYT100 742 ABY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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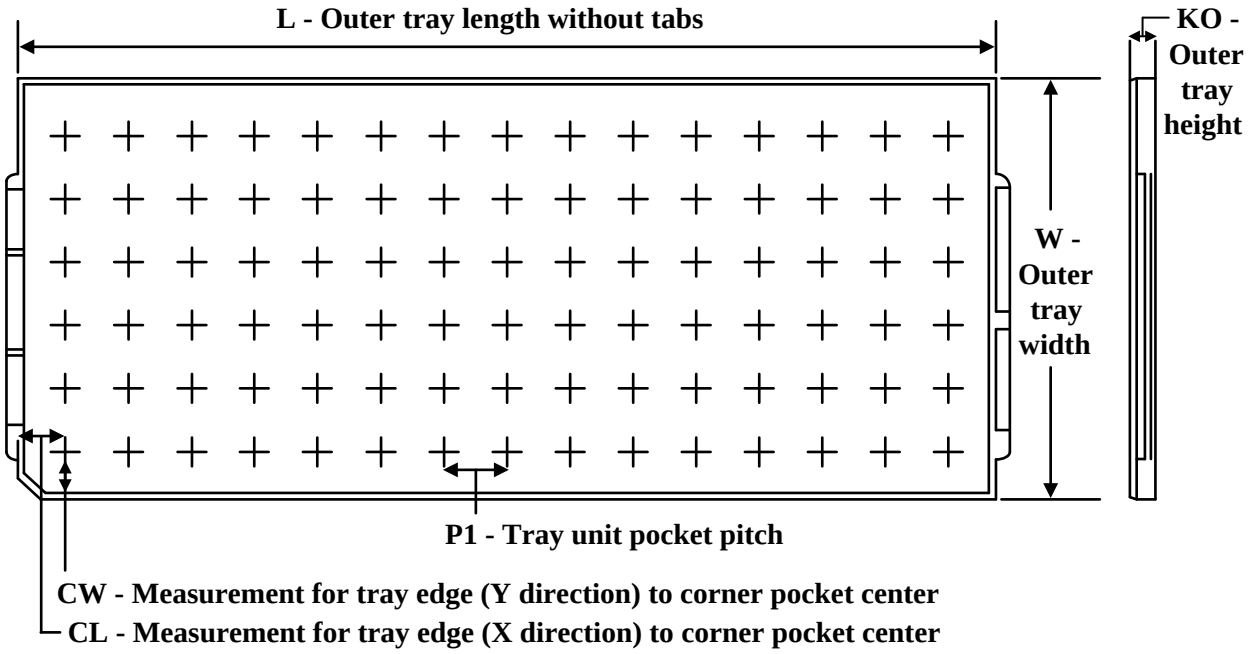
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

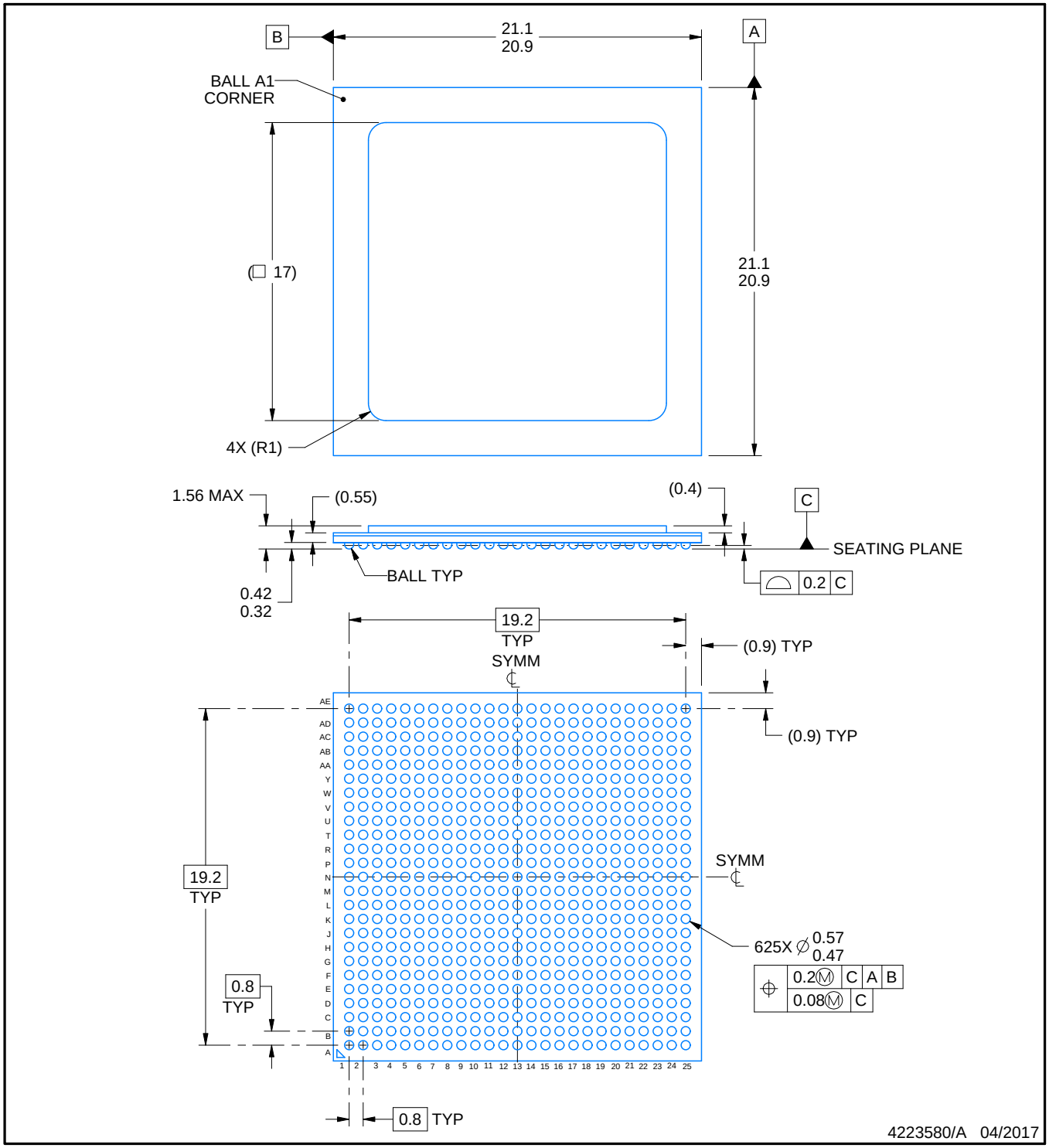
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
66AK2G12ABY100	ABY	FCCSP	625	60	5 x 12	150	315	135.9	7620	23.9	26.05	20.15
66AK2G12ABY60	ABY	FCCSP	625	60	5 x 12	150	315	135.9	7620	23.9	26.05	20.15
66AK2G12ABYA100	ABY	FCCSP	625	60	5 x 12	150	315	135.9	7620	23.9	26.05	20.15
66AK2G12ABYA100E	ABY	FCCSP	625	60	5 x 12	150	315	135.9	7620	23.9	26.05	20.15
66AK2G12ABYA60	ABY	FCCSP	625	60	5 x 12	150	315	135.9	7620	23.9	26.05	20.15
66AK2G12ABYA60E	ABY	FCCSP	625	60	5 x 12	150	315	135.9	7620	23.9	26.05	20.15
66AK2G12ABYT100	ABY	FCCSP	625	60	5 x 12	150	315	135.9	7620	23.9	26.05	20.15

PACKAGE OUTLINE

ABY0625A

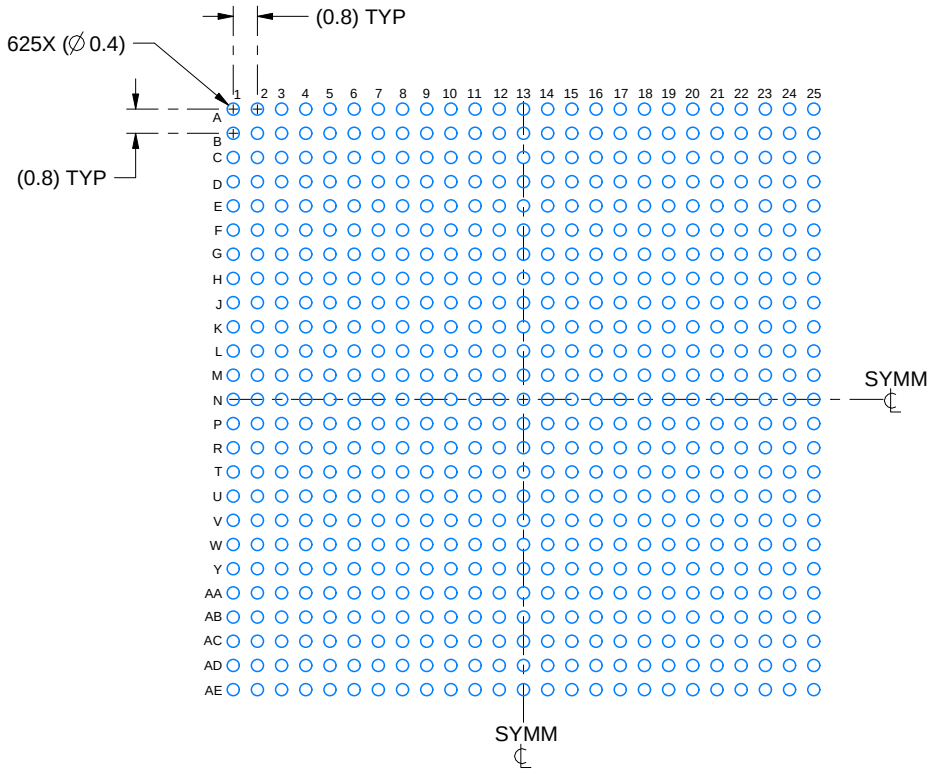
FCBGA - 1.56 mm max height

BALL GRID ARRAY

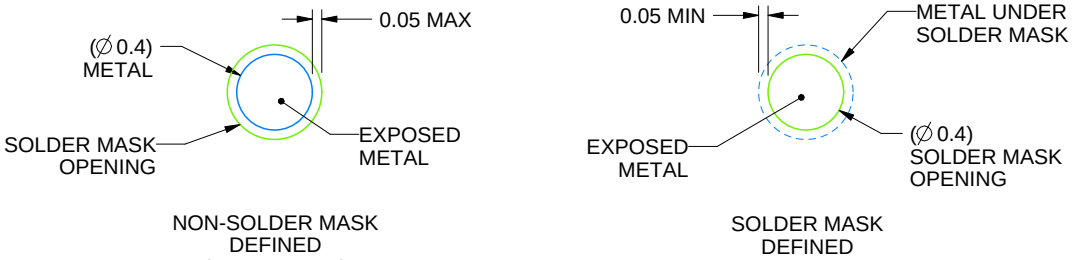


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 4X

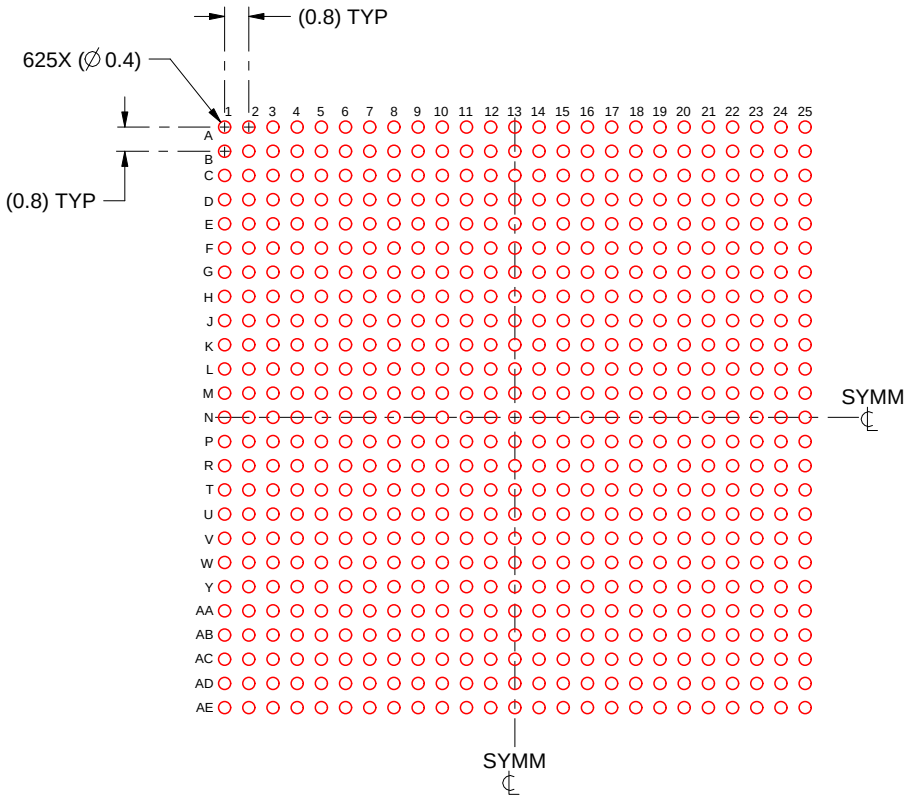


SOLDER MASK DETAILS
NOT TO SCALE

4223580/A 04/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE: 4X

4223580/A 04/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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