THE DATASHEET OF

LTC4218IDHC-12#PBF

FEATURES

- **Wide Operating Voltage Range: 2.9V to 26.5V**
- **Adjustable, 5% Accurate 15mV Current Limit**
- Current Monitor Output
- Adjustable Current Limit Timer Before Fault
- Power Good and Fault Outputs
- Adjustable Inrush Current Control
- 2% Accurate Undervoltage and Overvoltage Protection
- Available in 16-Lead SSOP and 16-Pin 5mm × 3mm DFN Packages

APPLICATIONS

- RAID Systems
- ATCA, AMC, µTCA Systems
- Server I/O Cards
- Industrial

DESCRIPTION

The LTC®4218 is a Hot Swap controller that allows a board to be safely inserted and removed from a live backplane. An internal high side switch driver controls the gate of an external N-channel MOSFET for supply voltages from 2.9V to 26.5V. A dedicated 12V version (LTC4218-12) contains preset 12V specific thresholds, while the standard LTC4218 allows adjustable thresholds.

The LTC4218 provides an accurate (5%) current limit with current foldback limiting. The current limit threshold can be adjusted dynamically using an external pin. Additional features include a current monitor output that amplifies the sense voltage for ground referenced current sensing. Overvoltage, undervoltage and power good monitoring are also provided.

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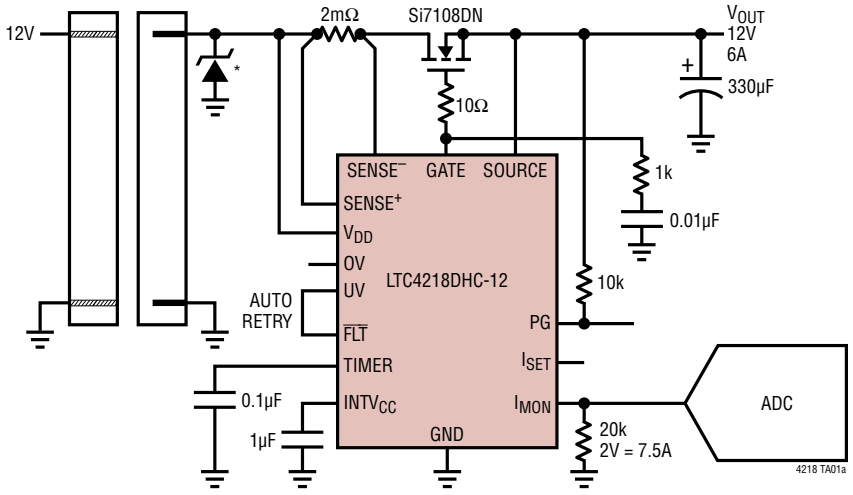
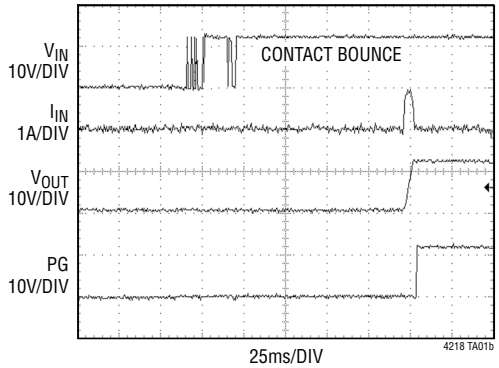
TYPICAL APPLICATION

12V, 6A Card Resident Application



*TVS: DIODES INC SMAJ17A

Power-Up Waveform



ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

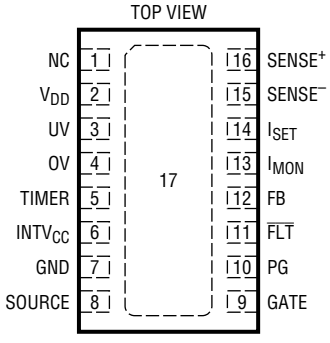
Supply Voltage (V_{DD}) ..... –0.3V to 35V
Input Voltages
- FB, OV, UV ..... –0.3V to 12V
- TIMER ..... –0.3V to 3.5V
- $SENSE^-$ ..... V_{DD} – 10V or –0.3V to V_{DD}
- $SENSE^+$ ..... V_{DD} – 10V or –0.3V to V_{DD}
- SOURCE ..... – 5V to V_{DD} + 0.3V

Output Voltages
- I_{SET}, I_{MON} ..... –0.3V to 3V
- PG, $\overline{FLT}$ ..... –0.3V to 35V
- $INTV_{CC}$ ..... –0.3V to 3.5V
- GATE (Note 3) ..... –0.3V to 35V

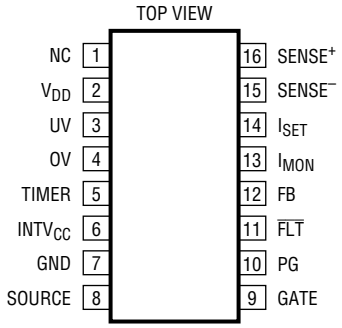
Operating Ambient Temperature Range
- LTC4218C ..... 0°C to 70°C
- LTC4218I ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
- GN Package Only ..... 300°C

PIN CONFIGURATION



DHC PACKAGE
16-LEAD (5mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 17) IS SUBSTRATE GND



GN PACKAGE
16-LEAD PLASTIC SSOP
T_{JMAX} = 150°C, θ_{JA} = 135°C/W

ORDER INFORMATION

(http://www.linear.com/product/LTC4218#orderinfo)

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4218CDHC-12#PBF	LTC4218CDHC-12#TRPBF	421812	16-Lead (5mm × 3mm) Plastic DFN	0°C to 70°C
LTC4218IDHC-12#PBF	LTC4218IDHC-12#TRPBF	421812	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4218CGN#PBF	LTC4218CGN#TRPBF	4218	16-Lead Plastic SSOP	0°C to 70°C
LTC4218IGN#PBF	LTC4218IGN#TRPBF	4218I	16-Lead Plastic SSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Characteristics							
V_{DD}	Input Supply Range		●	2.9		26.5	V
I_{DD}	Input Supply Current	FET On	●		1.6	5	mA
$V_{DD(UVL)}$	Input Supply Undervoltage Lockout	V_{DD} Rising	●	2.65	2.73	2.85	V
$V_{DD(UVTH)}$	Input Supply Undervoltage Threshold	LTC4218-12 Only V_{DD} Rising	●	9.6	9.88	10.2	V
$\Delta V_{DD(UVHYST)}$	Input Supply Undervoltage Hysteresis	LTC4218-12 Only	●	520	640	760	mV
$V_{DD(OVTH)}$	Input Supply Overvoltage Threshold	LTC4218-12 Only V_{DD} Rising	●	14.7	15.05	15.4	V
$\Delta V_{DD(OVHYST)}$	Input Supply Overvoltage Hysteresis	LTC4218-12 Only	●	183	244	305	mV
$V_{SOURCE(PGTH)}$	SOURCE Power Good Threshold	LTC4218-12 Only V_{SOURCE} Rising	●	10.2	10.5	10.8	V
$\Delta V_{SOURCE(PGHYST)}$	SOURCE Power Good Hysteresis	LTC4218-12 Only	●	127	170	213	mV
$\Delta V_{SNS(TH)}$	Current Limit Sense Voltage Threshold ($V_{SENSE}^+ - V_{SENSE}^-$)	V_{FB} = 1.23V V_{FB} = 0V V_{FB} = 1.23V, R_{SET} = 20kΩ	● ● ●	14.25 2.8 6.7	15 3.75 7.5	15.75 4.7 8.325	mV mV mV
$I_{SENSE^-(IN)}$	$SENSE^-$ Input Current	V_{SENSE^-} = 12V	●		4	±10	µA
$I_{SENSE^+(IN)}$	$SENSE^+$ Input Current	V_{SENSE^+} = 12V	●		5.5	±20	µA
ΔV_{GATE}	External N-Channel Gate Drive ($V_{GATE} - V_{SOURCE}$)	V_{DD} = 2.9V to 26.5V (Note 3) I_{GATE} = 0, –1µA	●	5	6.15	6.5	V
$\Delta V_{GATE-HIGH(TH)}$	Gate High Threshold ($V_{GATE} - V_{SOURCE}$)		●	3.5	4.2	4.8	V
$I_{GATE(UP)}$	External N-Channel Gate Pull-Up Current	Gate Drive On, V_{GATE} = V_{SOURCE} = 12V	●	–19	–24	–29	µA
$I_{GATE(FST)}$	External N-Channel Gate Fast Pull-Down Current	Fast Turn Off, V_{GATE} = 18V, V_{SOURCE} =12V	●	100	170	220	mA
$I_{GATE(DN)}$	External N-Channel Gate Pull-Down Current	Gate Drive Off, V_{GATE} = 18V, V_{SOURCE} =12V	●	200	250	400	µA
Inputs							
I_{IN}	OV, UV, FB Input Current	V_{PIN} = 1.2V, LTC4218 Only	●		0	±1	µA
R_{IN}	OV, UV, FB Input Resistance	LTC4218-12 Only	●	13	18	23	kΩ
$V_{(TH)}$	OV, UV, FB Threshold Voltage	V_{PIN} Rising	●	1.21	1.235	1.26	V
$\Delta V_{OV(HYST)}$	OV Hysteresis		●	10	20	30	mV
$\Delta V_{UV(HYST)}$	UV Hysteresis		●	50	80	110	mV
$V_{UV(RTH)}$	UV Reset Threshold Voltage	V_{UV} Falling	●	0.55	0.62	0.7	V
$\Delta V_{FB(HYST)}$	FB Power Good Hysteresis		●	10	20	30	mV
R_{ISET}	I_{SET} Internal Resistor		●	19.5	20	20.5	kΩ
I_{SOURCE}	SOURCE Input Current	V_{SOURCE} = V_{GATE} = 12V, LTC4218-12 Only V_{SOURCE} = V_{GATE} = 12V, LTC4218 Only V_{SOURCE} = V_{GATE} = 0V	● ● ●	50 1	70 2 0	90 4 ±1	µA µA µA
Outputs							
V_{INTVCC}	$INTV_{CC}$ Output Voltage	I_{SINK} = 0mA, –10mA			3.1		V
V_{OL}	PG, $\overline{FLT}$ Output Low Voltage	I_{SINK} = 2mA	●		0.4	0.8	V
I_{OH}	PG, $\overline{FLT}$ Input Leakage Current	V = 30V	●		0	±10	µA
$V_{TIMER(H)}$	TIMER High Threshold	V_{TIMER} Rising	●	1.2	1.235	1.28	V
$V_{TIMER(L)}$	TIMER Low Threshold	V_{TIMER} Falling	●	0.1	0.21	0.3	V
$I_{TIMER(UP)}$	TIMER Pull Up Current	V_{TIMER} = 0V	●	–80	–100	–120	µA
$I_{TIMER(DN)}$	TIMER Pull-Down Current	V_{TIMER} = 1.2V	●	1.4	2	2.6	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{TIMER(RATIO)}$	TIMER Current Ratio $I_{TIMER(DN)}/I_{TIMER(UP)}$		●	1.6	2	2.7	%
$I_{MON(FS)}$	I_{MON} Full-Scale Output Current	$V_{SENSE}^+ - V_{SENSE}^-$ = 15mV	●	94	100	106	µA
$I_{MON(OFF)}$	I_{MON} Offset Current	$V_{SENSE}^+ - V_{SENSE}^-$ = 1mV	●		±0	±6	µA
G_{IMON}	I_{MON} Gain	$V_{SENSE}^+ - V_{SENSE}^-$ = 15mV and 1mV	●	6.47	6.67	6.87	µA/mV
BW_{IMON}	I_{MON} Bandwidth				250		kHz
AC Characteristics							
$t_{PHL(GATE)}$	Input High (OV), Input Low (UV) to GATE Low Propagation Delay	V_{GATE} < 16.5V Falling	●		3	5	µs
$t_{PHL(SENSE)}$	$V_{SENSE}^+ - V_{SENSE}^-$ High to GATE Low Propagation Delay	V_{FB} = 0, Step ($V_{SENSE}^+ - V_{SENSE}^-$) to 60mV, C_{GATE} = 1.5nF, V_{GATE} < 16.5V Falling	●		0.2	1	µs
$t_{D(ON)}$	Turn-On Delay	Step V_{UV} to 2V, V_{GATE} > 13V	●	50	100	150	ms
$t_{D(FAULT)}$	UV Low to Clear Fault Latch Delay				1		µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

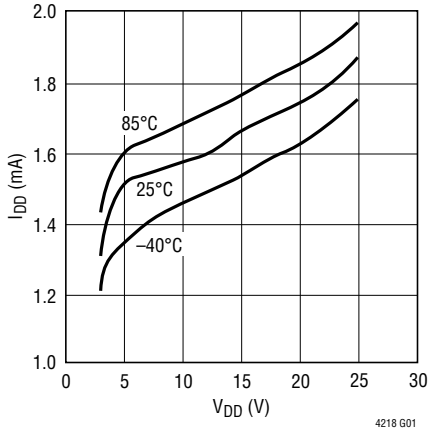
Note 2: All currents into pins are positive, all voltages are referenced to GND unless otherwise specified.

Note 3: An internal clamp limits the GATE pin to a maximum of 6.5V above the SOURCE pin. Driving either GATE or SOURCE pin to voltages beyond the clamp may damage the device.

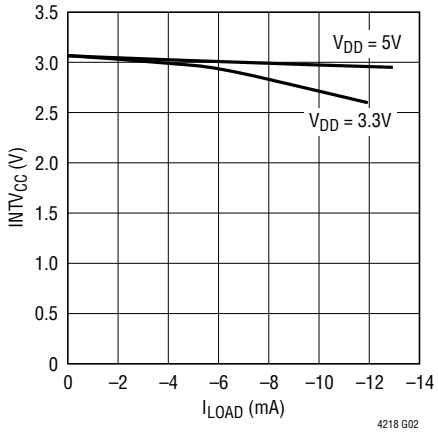
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 12V unless otherwise noted.

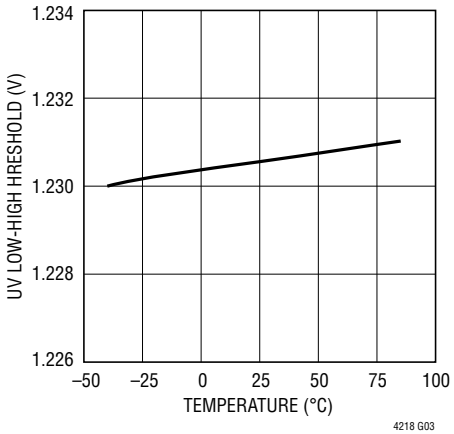
I_{DD} vs V_{DD}



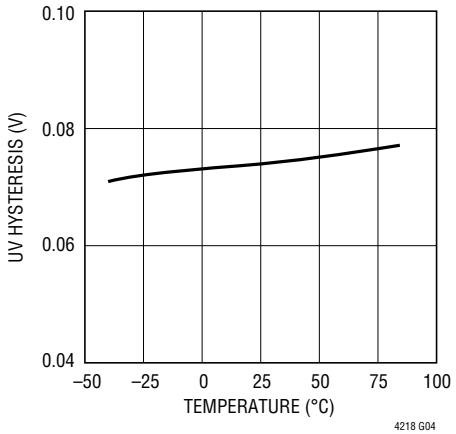
$INTV_{CC}$ Load Regulation



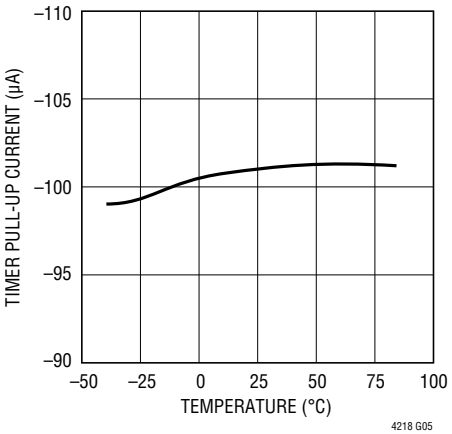
UV Low-High Threshold vs Temperature



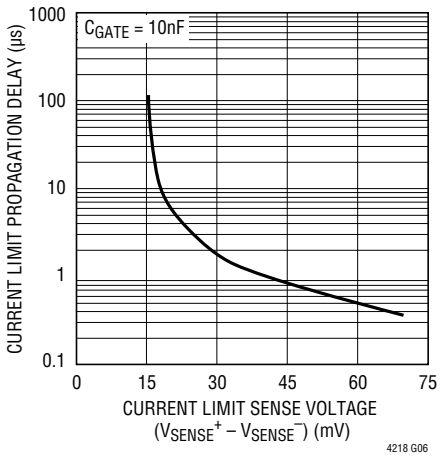
UV Hysteresis vs Temperature



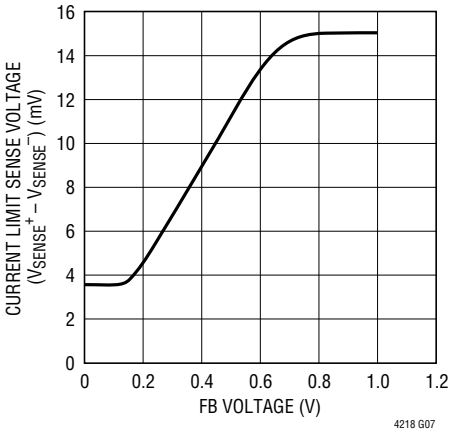
Timer Pull-Up Current vs Temperature



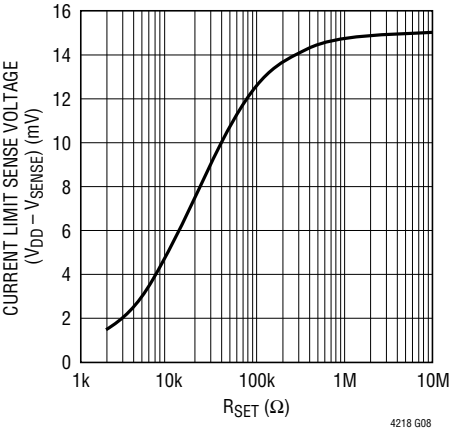
Current Limit Delay



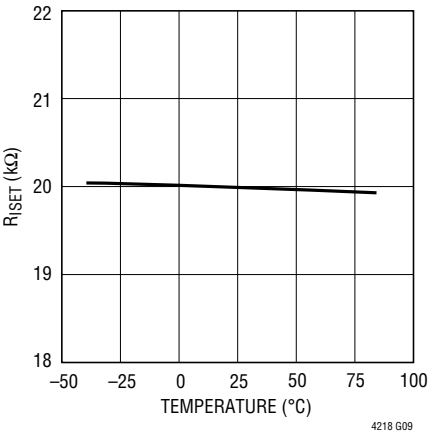
Current Limit Threshold Foldback



Current Limit Adjustment



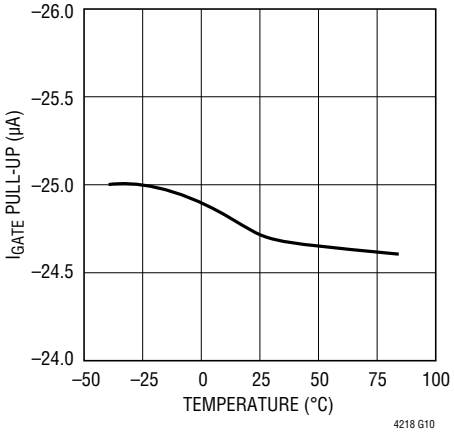
Internal I_{SET} Resistor (R_{ISET}) vs Temperature



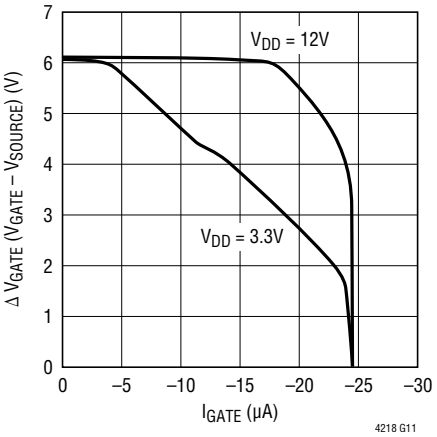
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 12V unless otherwise noted.

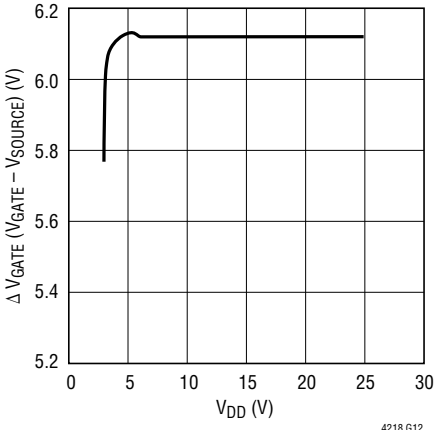
GATE Pull-Up Current vs Temperature



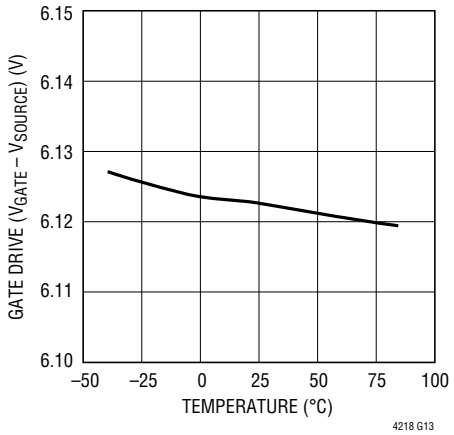
Gate Drive vs Gate Pull-Up Current



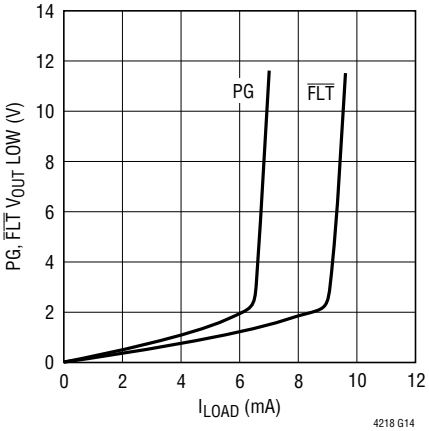
Gate Drive vs V_{DD}



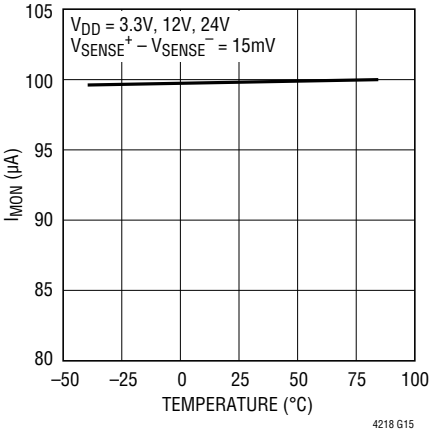
Gate Drive vs Temperature



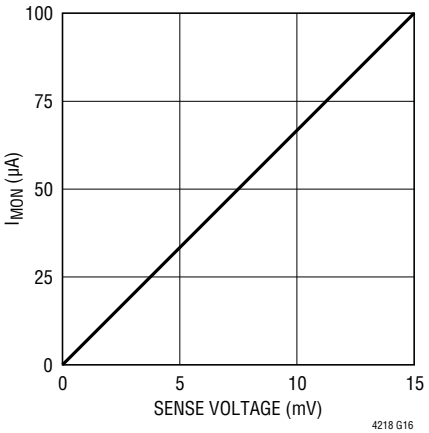
PG, $\overline{FLT}$ V_{OUT} Low vs I_{LOAD}



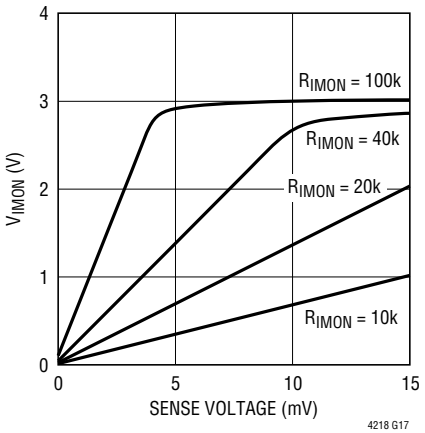
I_{MON} vs Temperature and V_{DD}



I_{MON} vs Sense



V_{IMON} vs Sense



PIN FUNCTIONS

Exposed Pad: Exposed pad may be left open or connected to device ground.

FB: Foldback and Power Good Comparator Input. Connect this pin to an external resistive divider from SOURCE for the LTC4218 (adjustable version). The LTC4218-12 version uses a fixed internal divider with optional external adjustment. Open the pin if the LTC4218-12 thresholds for 12V operation are desired. If the voltage falls below 0.6V, the output power is considered bad and the current limit is reduced. If the voltage falls below 1.21V the PG pin will pull low to indicate the power is bad.

$\overline{\text{FLT}}$: Overcurrent Fault Indicator. Open drain output pulls low when an overcurrent fault has occurred and the circuit breaker trips. For overcurrent auto-retry tie to UV pin (see Applications Information for details).

GATE: Gate Drive for External N-Channel FET. An internal 24µA current source charges the gate of the external N-channel MOSFET. A resistor and capacitor network from this pin to ground sets the turn-on rate. During an undervoltage or overvoltage generated turn-off a 250µA pull-down current turns the MOSFET off. During a short circuit or undervoltage lockout, a 170mA pull-down current source between GATE and SOURCE is activated.

GND: Device Ground.

I_{MON}: Current Monitor Output. The current sourced from this pin is defined as the current sense voltage (between the $SENSE^+$ and $SENSE^-$ pins) multiplied by 6.67µA/mV. Placing a 20k resistor from this pin to GND creates a 0V to 2V voltage swing when the current sense voltage ranges from 0mV to 15mV.

$INTV_{CC}$: Internal 3.1V Supply Decoupling Output. This pin must have a 1µF or larger capacitor. Overloading this pin can disrupt internal operation.

I_{SET}: Current Limit Adjustment Pin. For 15mV current limit threshold, open this pin. This pin is driven by a 20k resistor in series with a voltage source. The pin voltage is used to generate the current limit threshold. The internal 20k resistor (R_{ISET}) and an external resistor (R_{SET}) between I_{SET} and ground create an attenuator that lowers the current limit value. Due to circuit tolerance, the I_{SET} resistor should not be less than 2k.

NC: No Connection

OV: Overvoltage Comparator Input. Connect this pin to an external resistive divider from V_{DD} for the LTC4218 (adjustable version). The LTC4218-12 version uses a fixed internal divider with optional external adjustment for 12V operation. Open the pin if the LTC4218-12 thresholds are desired. If the voltage at this pin rises above 1.235V, an overvoltage is detected and the switch turns off. Tie to GND if unused.

PG: Power Good Indicator. Open drain output pulls low when the FB pin drops below 1.21V indicating the power is bad. If the FB pin rises above 1.23V and the GATE to SOURCE voltage exceeds 4.2V, the open-drain pull-down releases the PG pin to go high.

$SENSE^-$: Current Sense Minus Input. Connect this pin to the opposite of V_{DD} current sense resistor side. The current limit circuit controls the GATE pin to limit the sense voltage between the $SENSE^+$ and $SENSE^-$ pins to 15mV or less depending on the voltage at the FB pin.

$SENSE^+$: Current Sense Plus Input. Connect this pin to the V_{DD} side of the current sense resistor.

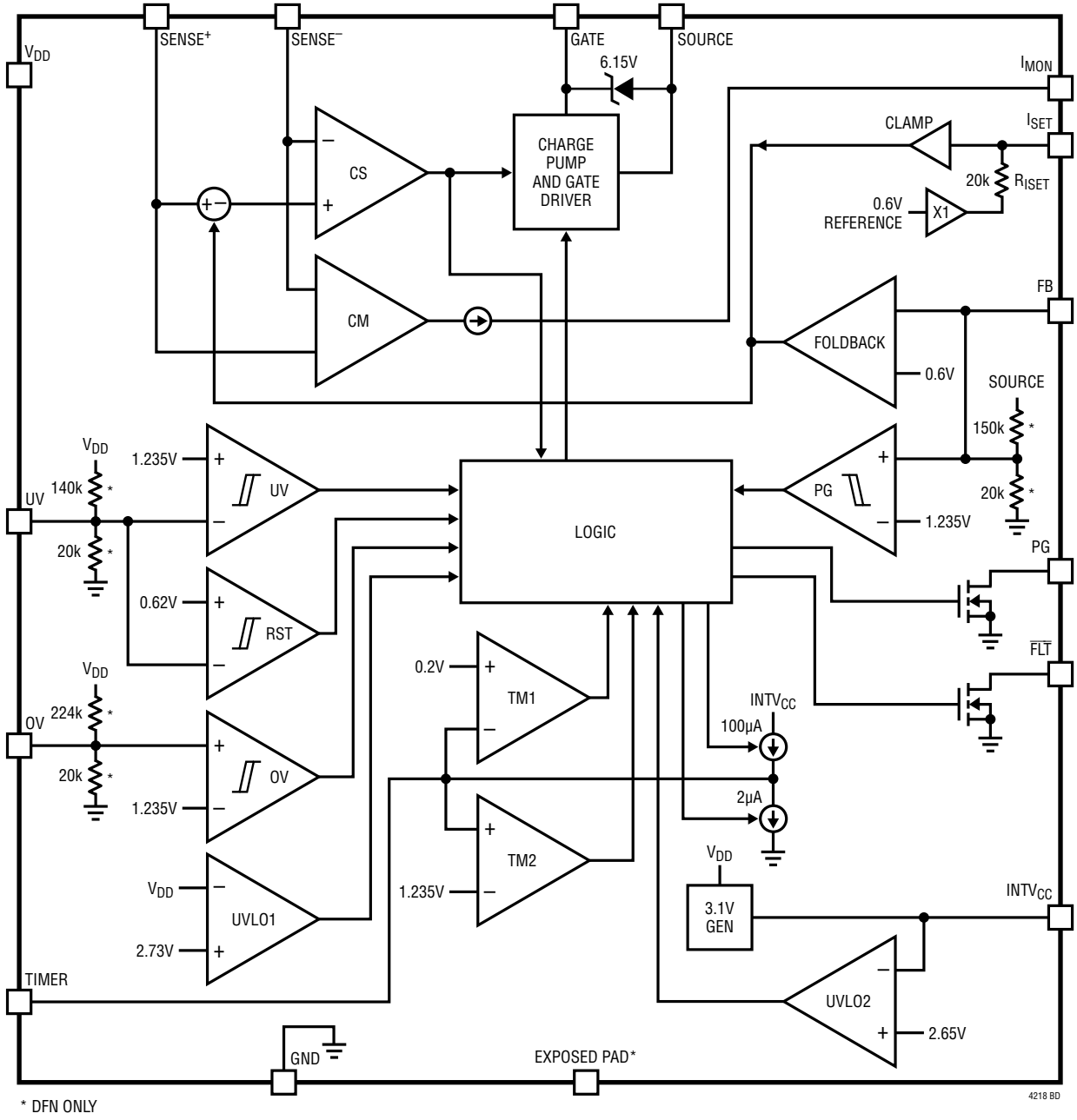
SOURCE: N-Channel MOSFET Source Connection. Connect this pin to the source of the external N-channel MOSFET switch. This pin provides a return for the gate pull-down circuit. In the LTC4218-12 version, the power good comparator monitors an internal resistive divider between the SOURCE pin and GND.

TIMER: Timer Input. Connect a capacitor between this pin and ground to set a 12ms/µF duration for current limit before the switch is turned off. If the UV pin is toggled low while the MOSFET switch is off, the switch will turn on again following a cool down time of 518ms/µF duration.

UV: Undervoltage Comparator Input. Tie high if unused. Connect this pin to an external resistive divider from V_{DD} for the LTC4218 (adjustable version). The LTC4218-12 version drives the UV pin with an internal resistive divider from V_{DD}. Open the pin if the preset LTC4218-12 thresholds for 12V operation are desired. If the UV pin voltage falls below 1.15V, an undervoltage is detected and the switch turns off. Pulling this pin below 0.62V resets the overcurrent fault and allows the switch to turn back on (see Applications Information for details). If overcurrent auto-retry is desired then tie this pin to the $\overline{\text{FLT}}$ pin.

V_{DD}: Supply Voltage. This pin has an undervoltage lockout threshold of 2.73V.

FUNCTIONAL DIAGRAM



OPERATION

The Functional Diagram displays the main circuits of the device. The LTC4218 is designed to turn a board's supply voltage on and off in a controlled manner, allowing the board to be safely inserted and removed from a live backplane. During normal operation, the charge pump and gate driver turn on the external N-channel pass FET's gate to provide power to the load.

The current sense (CS) amplifier monitors the load current using the voltage sensed across the current sense resistor. The CS amplifier limits the current in the load by reducing the GATE-to-SOURCE voltage in an active control loop. It is simple to adjust the current limit threshold using the current limit adjustment (I_{SET}) pin. This allows a different threshold during other times such as startup.

A short circuit on the output to ground causes significant power dissipation during active current limiting. To limit this power, the foldback amplifier reduces the current limit value from 15mV to 3.75mV (referred to the $SENSE^+$ minus $SENSE^-$ voltage) in a linear manner as the FB pin drops below 0.6V (see Typical Performance Characteristics).

If an overcurrent condition persists, the TIMER pin ramps up with a 100µA current source until the pin voltage exceeds 1.2V (comparator TM2). This indicates to the logic that it is time to turn off the MOSFET to prevent overheating. At this point the TIMER pin ramps down using the 2µA current source until the voltage drops below 0.2V (Comparator TM1) which tells the logic to start an internal 100ms timer. At this point, the pass transistor has cooled and it is safe to turn it on again. Latchoff is the normal operating condition following overcurrent turn-off. Retry is initiated by pulling the UV pin low for a minimum of 1µs then high. Autoretry is implemented by tying the $\overline{FLT}$ to the UV pin.

The fixed 12V version, LTC4218-12, uses two separate internal dividers from V_{DD} to drive the UV and OV pins. This version also features a divider from the SOURCE pin to drive the FB pin. The LTC4218-12 is available in a DFN package while the LTC4218 (adjustable version) is in a SSOP package.

The output voltage is monitored using the FB pin and the PG comparator to determine if the power is available for the load. The power good condition is signaled by the PG pin using an open-drain pull-down transistor.

The Functional Diagram shows the monitoring blocks of the LTC4218. The comparators on the left side include the UV and OV comparators. These comparators are used to determine if the external conditions are valid prior to turning on the MOSFET. But first, the undervoltage lockout circuits (UVLO1 and UVLO2) must validate the input supply and internally generated 3.1V supply ($INTV_{CC}$) and generate the power up initialization to the logic circuits. If the external conditions remain valid for 100ms the MOSFET is allowed to turn on.

Other monitoring features include the I_{MON} current monitor. The current monitor (CM) outputs a current proportional to the sense resistor current. This current can drive an external resistor or other circuits for monitoring purposes.

APPLICATIONS INFORMATION

The typical LTC4218 application is in a high availability system that uses a positive voltage supply to distribute power to individual cards. The basic application circuit is shown in Figure 1. External component selection is discussed in detail in the following sections.

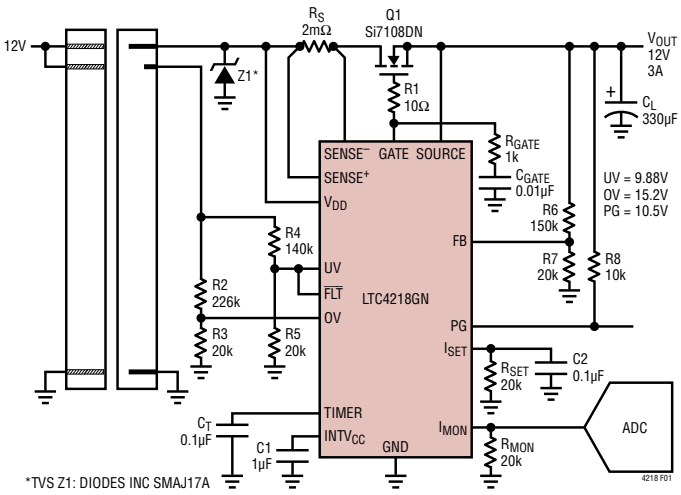


Figure 1. 3A, 12V Card Resident Application

Turn-On Sequence

The power supply on a board is controlled by placing an external N-channel pass transistor (Q1) in the power path. Note the sense resistor (R_S) detects current and the capacitor (C_{GATE}) controls gate slew rate. Resistor R1 prevents high frequency oscillations in Q1 and resistor R_{GATE} isolates C_{GATE} during fast turn-off.

Several conditions must be present before the external pass transistor can be turned on. First, the supply V_{DD} must exceed its undervoltage lockout level. Next, the internally generated supply $INTV_{CC}$ must cross its 2.65V undervoltage threshold. This generates a 25µs power-on-reset pulse which clears the logic's fault register and initializes internal latches.

After the power-on-reset pulse, the UV and OV pins must indicate that the input voltage is within the acceptable range. All of these conditions must be satisfied for a duration of 100ms to ensure that any contact bounce during the insertion has ended.

The pass transistor is turned on by charging up the GATE with a 24µA charge pump generated current source (Figure 2).

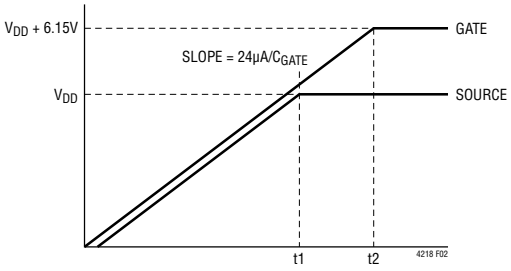


Figure 2. Supply Turn-On

The voltage at the GATE pin rises with a slope equal to $24\mu A/C_{GATE}$ and the supply inrush current is set at:

$$I_{INRUSH} = \frac{C_L}{C_{GATE}} \bullet 24\mu A$$

When the GATE voltage reaches the MOSFET threshold voltage, the switch begins to turn on and the SOURCE voltage follows the GATE voltage as it increases. Once SOURCE reaches V_{DD}, the GATE will ramp up until clamped by the 6.15V zener between GATE and SOURCE.

As the SOURCE pin voltage rises, so will the FB pin which is monitoring it. If the voltage across the current sense resistor (R_S) gets too high, the inrush current will be limited by the internal current limiting circuitry. Once the FB pin crosses its 1.235V threshold and the GATE to SOURCE voltage exceeds 4.2V, the PG pin will cease to pull low and indicate that the power is good.

Turn-Off Sequence

The switch can be turned off by a variety of conditions. A normal turn-off is initiated by the UV pin going below its 1.235V threshold. Additionally, several fault conditions will turn off the switch. These include an input overvoltage (OV pin) and overcurrent circuit breaker (SENSE pin). Normally, the switch is turned off with a 250µA current pulling down the GATE pin to ground. With the switch turned off, the SOURCE pin voltage drops which pulls the FB pin below its threshold. The PG then pulls low to indicate output power is no longer good.

APPLICATIONS INFORMATION

If V_{DD} drops below 2.65V for greater than 5µs or $INTV_{CC}$ drops below 2.5V for greater than 1µs, a fast shutdown of the switch is initiated. The GATE is pulled down with a 170mA current to the SOURCE pin.

Overcurrent Fault

The LTC4218 features an adjustable current limit with foldback that protects the MOSFET when excessive load current happens. To protect the switch during active current limit, the available current is reduced as a function of the output voltage sensed by the FB pin. A graph in the Typical Performance Characteristics shows the Current Limit Threshold Foldback.

An overcurrent fault occurs when the current limit circuitry has been engaged for longer than the time-out delay set by the TIMER. Current limiting begins when the current sense voltage between the $SENSE^+$ and $SENSE^-$ pins reaches 3.75mV to 15mV (depending on the foldback). The GATE pin is then brought down with a 170mA GATE-to-SOURCE current. The voltage on the GATE is regulated in order to limit the current sense voltage to less than 15mV. At this point, a circuit breaker time delay starts by charging the external timing capacitor with a 100µA pull-up current from the TIMER pin. If the TIMER pin reaches its 1.2V threshold, the external switch turns off (with a 250µA current from GATE to ground). Next, the $\overline{FLT}$ pin is pulled low to indicate an overcurrent fault has turned off the MOSFET. For a given circuit breaker time delay, the equation for setting the timing capacitor's value is as follows:

$$C_T = T_{CB} \bullet 0.083[\mu F/ms]$$

After the switch is turned off, the TIMER pin begins discharging the timing capacitor with a 2µA pull-down current. When the TIMER pin reaches its 0.2V threshold, the switch is allowed to turn on again if the overcurrent fault latch has been cleared. Bringing the UV pin below 0.6V for a minimum of 1µs and then high will clear the fault latch.

Tying the $\overline{FLT}$ pin to the UV pin allows the part to self-clear the fault and turn the MOSFET on as soon as TIMER pin has ramped below 0.2V. In this auto retry mode, the LTC4218 repeatedly tries to turn on after an overcurrent at a period determined by the capacitor on the TIMER pin.

The waveform in Figure 3 shows how the output latches off following a short circuit. The drop across the sense resistor is 3.75mV as the timer ramps up.

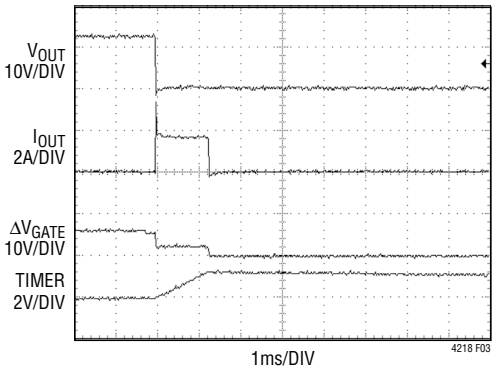


Figure 3. Short-Circuit Waveform

Current Limit Stability

The C_{GATE} value is chosen to set the inrush current. The R_{GATE} value should be chosen to stabilize the current limit large signal response. For most large MOSFETs 1k is a suitable value. Smaller sized MOSFETs may require R_{GATE} values up to 100k. To determine stability create a load step using a resistive load equal to half supply divided by the current limit value. Increase R_{GATE} until the GATE pin voltage is devoid of ringing during the load step.

Current Limit Adjustment

The default value of the active current limiting signal threshold is 15mV. The current limit threshold can be adjusted lower by placing a resistor on the I_{SET} pin. As shown in the Functional Block Diagram the voltage at the I_{SET} pin (via the clamp circuit) sets the CS amplifier's built-in offset voltage. This offset voltage directly determines the active current limit value. With the I_{SET} pin open, the voltage at the I_{SET} pin is determined by the buffered reference voltage. This voltage is set to 0.618V which corresponds to a 15mV current limit threshold.

An external R_{SET} resistor placed between the I_{SET} pin and ground forms a resistive divider with the internal 20k R_{ISET} sourcing resistor. The divider acts to lower the voltage at the I_{SET} pin and therefore lower the current limit threshold. The overall current limit threshold precision is reduced

APPLICATIONS INFORMATION

to ±11% when using a 20k resistor to half the threshold. This pin's 20k sourcing impedance allows noise to couple to this pin and disturb the current limit threshold. Place a 0.1µF capacitor between the I_{SET} pin and ground when a board trace is connected to this pin.

Using a switch (connected to ground) in series with R_{SET} allows the active current limit to change only when the switch is closed. This feature can be used to program a reduced running current while the maximum current limit is used at start-up.

Monitor MOSFET Current

The current in the MOSFET passes through the sense resistor. The voltage on the sense resistor is converted to a current that is sourced out of the I_{MON} pin. The gain of the I_{SENSE} amplifier is 100µA from I_{MON} for 15mV on the sense resistor. This output current can be converted to a voltage using an external resistor to drive a comparator or ADC. The voltage compliance for the I_{MON} pin is from 0V to $INTV_{CC}$ – 0.7V.

A microcontroller with a built-in comparator can build a simple integrating single-slope ADC by resetting a capacitor that is charged with this current. When the capacitor voltage trips the comparator and the capacitor is reset, a timer is started. The time between resets will indicate the MOSFET current.

Monitor OV and UV Faults

Protecting the load from an overvoltage condition is the main function of the OV pin. In the LTC4218-12 an internal resistive divider (driving the OV pin) connects to a comparator to turn off the MOSFET when the V_{DD} voltage exceeds 15.05V. If the V_{DD} pin subsequently falls back below 14.8V, the switch will be allowed to turn on immediately. In the LTC4218, the OV pin threshold is 1.235V when rising and 1.215V when falling out of overvoltage.

The UV pin functions as an undervoltage protection pin or as an "on" pin. In the LTC4218-12 the MOSFET turns off when V_{DD} falls below 9.23V. If the V_{DD} pin subsequently rises above 9.88V for 100ms, the switch will be allowed to turn on again. The LTC4218 UV turn on/off threshold is 1.235V (rising) and 1.155V (falling).

In the case of an undervoltage or overvoltage, the MOSFET turns off and there is indication on the PG status pin. When the overvoltage is removed, the MOSFET's gate ramps up immediately.

Power Good Indication

In addition to setting the foldback current limit threshold, the FB pin is used to determine a power good condition. The LTC4218-12 uses an internal resistive divider on the SOURCE pin to drive the FB pin. The PG comparator indicates logic high when SOURCE pin rises above 10.5V. If the SOURCE pin subsequently falls below 10.3V, the comparator toggles low. On the LTC4218, the PG comparator drives high when the FB pin rises above 1.23V and low when falls below 1.215V.

Once the PG comparator is high, the GATE pin voltage is monitored with respect to the SOURCE pin. Once the GATE minus SOURCE voltage exceeds 4.2V, the PG pin goes high. This indicates to the system that it is safe to load the Output while the MOSFET is completely turned "on". The PG pin goes low when the GATE is commanded off (using the UV, OV or $SENSE^+/SENSE^-$ pins) or when the PG comparator drives low.

12V Fixed Version

In the LTC4218-12, the UV, OV and FB pins are driven by internal dividers which may need to be filtered to prevent false faults. By placing a bypass capacitor on these pins the faults are delayed by the RC time constant. Use the R_{IN} value from the electrical table for this calculation.

In cases where the fixed thresholds need a slight adjustment, placing a resistor from the UV or OV pins to V_{DD} or GND will adjust the threshold up or down. Likewise, placing a resistor between FB pin to OUT or GND adjusts the threshold. Again, use the R_{IN} value from the electrical table for this calculation.

An example in Figure 4 raises the UV turn-on voltage from 9.88V to 10.5V. Increasing the UV level requires adding a resistor between UV and ground. The resistor, (R_{SHUNT1}),

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can be calculated using electrical table parameters as follows:

$$R_{SHUNT1} = \frac{R_{(IN)} \bullet V_{OLD}}{(V_{NEW} - V_{OLD})} = \frac{18k \bullet 9.88V}{(10.5V - 9.88V)} = 287k$$

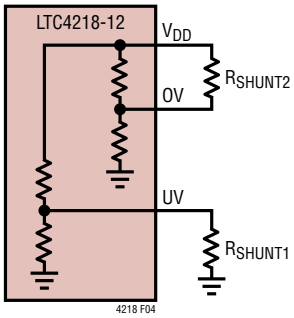

Figure 4. Adjusting LTC4218-12 Thresholds

In this same figure the OV threshold is lowered from 15.05V to 13.5V. Decreasing the OV threshold requires adding a resistor between V_{DD} and OV. This resistor can be calculated as follows:

$$R_{SHUNT2} = \frac{R_{(IN)} \bullet V_{OLD}}{V_{(TH)}} \left(\frac{(V_{NEW} - V_{OV(TH)})}{(V_{OLD} - V_{NEW})} \right) =$$

$$\frac{18k \bullet 15.05V}{1.235V} \left(\frac{(13.5V - 1.235V)}{(15.05V - 13.5V)} \right) = 1.736M$$

Use the equation for R_{SHUNT1} for increasing the OV and FB thresholds. Likewise, use the equation for R_{SHUNT2} for decreasing the UV and FB thresholds.

Design Example

Consider the following design example (Figure 5): V_{IN} = 12V, I_{MAX} = 7.5A. I_{INRUSH} = 1A, C_L = 330µF, V_{UVON} = 9.88V, V_{OVOFF} = 15.05V, $V_{PGTHRESHOLD}$ = 10.5V. A current limit fault triggers an automatic restart of the power up sequence.

The selection of the sense resistor, (R_S), is set by the overcurrent threshold of 15mV:

$$R_S = 15mV/I_{MAX} = 15mV/7.5A = 0.002\Omega$$

The MOSFET should be sized to handle the power dissipation during the inrush charging of the output capacitor C_{OUT}. The method used to determine the power in Q1 is the principal:

E_C = Energy in C_L = Energy in Q1

Thus:

$$E_C = ½\ CV^2 = ½\ (330\mu F)(12)^2 = 0.024J$$

Calculate the time it takes to charge up C_{OUT}:

$$t_{CHARGUP} = \frac{C_L \bullet V_{IN}}{I_{INRUSH}} = \frac{330\mu F \bullet 12V}{1A} = 4ms$$

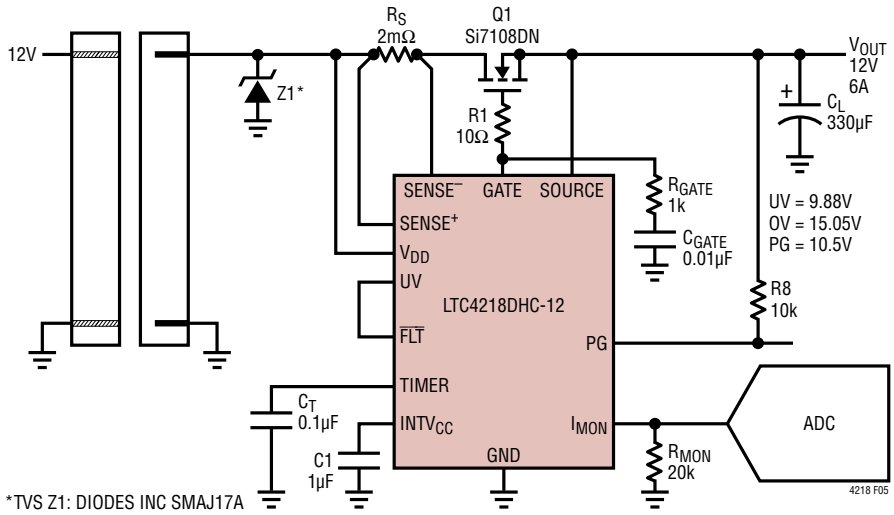

Figure 5. 6A, 12V Card Resident Application

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The inrush current is set to 1A using C_{GATE}:

$$C_{GATE} = C_L \frac{I_{GATE(UP)}}{I_{INRUSH}} = 330\mu F \frac{24\mu A}{1A} \cong 0.01\mu F$$

The average power dissipated in the MOSFET:

$$P_{DISS} = E_C/t_{CHARGUP} = 0.024J/4ms = 6W$$

The SOA (safe operating area) curves of candidate MOSFETs must be evaluated to ensure that the heat capacity of the package can stand 6W for 4ms. The SOA curves of the Vishay Siliconix Si7108DN provide 1.5A at 10V (15W) for 100ms, satisfying the requirement.

Next, the power dissipated in the MOSFET during overcurrent must be limited. The active current limit uses a timer to prevent excessive energy dissipation in the MOSFET. The worst-case power occurs when the voltage versus current profile of the foldback current limit is at the maximum. This occurs when the current is 6A and the voltage is one half of 12V or (6V). See the Current Limit Sense Voltage vs FB Voltage in the Typical Performance curves to view this profile. In order to survive 36W, the MOSFET SOA dictates a maximum time at this power level. The Si7108DN allows 60W for 10ms or less. Therefore, it is acceptable to set the current limit timeout using C_T to be 1.2ms:

$$C_T = 1.2ms/12[ms/\mu F] = 0.1\mu F$$

After the 1.2ms timeout the $\overline{FLT}$ pin needs to pull down on the UV pin to restart the power-up sequence.

Since the default values for overvoltage, undervoltage and power good thresholds for the 12V fixed version match the requirements, no external components are required for the UV, OV and FB pins.

The final schematic results in very few external components. Resistor R1 (10Ω) prevents high frequency oscillations in Q1 while R_{GATE} of 1k isolates C_{GATE} during fast turn-off. The pull-up resistor, (R2), connects to the PG pin while the 20k (R3) converts the I_{MON} current to a voltage at a ratio:

$$V_{IMON} = 6.67\left[\frac{\mu A}{mV}\right] \bullet 2\left[\frac{mV}{A}\right] \bullet 20k \bullet I_{OUT} = 0.267\left[\frac{V}{A}\right] \bullet I_{OUT}$$

In addition, there is a 0.1µF bypass (C1) on the $INTV_{CC}$ pin.

Layout Considerations

To achieve accurate current sensing, a Kelvin connection for the sense resistor is recommended. The PCB layout should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistors and the power MOSFETs should include good thermal management techniques for optimal device power dissipation. A recommended PCB layout for the sense resistor and power MOSFET is illustrated in Figure 6.

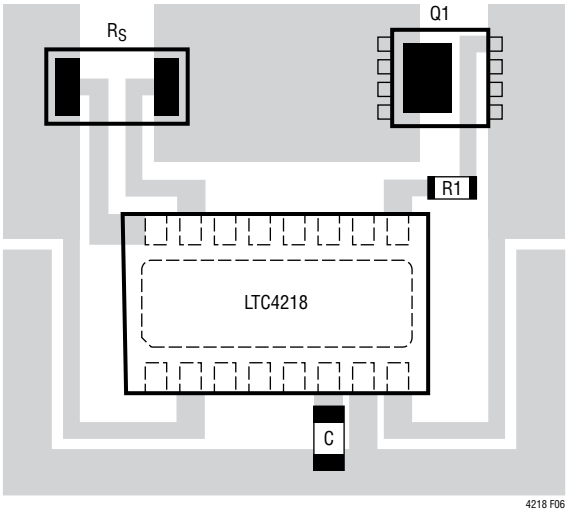


Figure 6. Recommended Layout

In Hot Swap applications where load currents can be 6A, narrow PCB tracks exhibit more resistances than wider tracks and operate at elevated temperatures. The minimum trace width for 1oz copper foil is 0.02" per amp to make sure the trace stays at a reasonable temperature. Using 0.03" per amp or wider is recommended. Note that 1oz copper exhibits a sheet resistance of about 0.5mΩ/square. Small resistances add up quickly in high current applications.

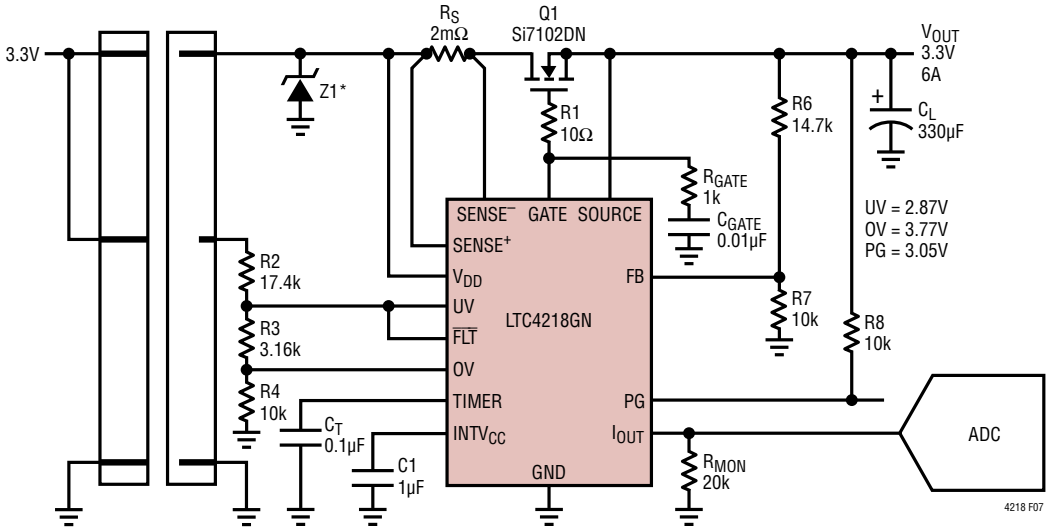
It is also important to put C1, the bypass capacitor for the $INTV_{CC}$ pin, as close as possible between the $INTV_{CC}$ and GND. Place the 10Ω resistor as close as possible to Q1. This will limit the parasitic trace capacitance that leads to Q1 self-oscillation. The traces connecting the LTC4218 to components should overlay a plane connected to the ground pin of the part (pin 7).

APPLICATIONS INFORMATION

Additional Applications

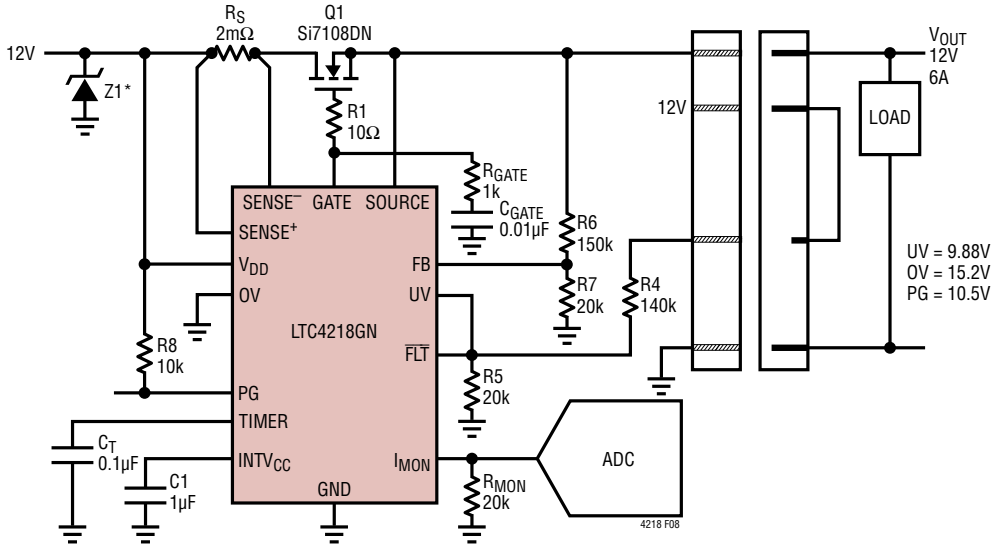
The LTC4218 has a wide operating range from 2.9V to 26.5V. The UV, OV and PG thresholds are set with a few resistors. All other functions are independent of supply voltage.

The last page includes a 24V application with a UV threshold of 19.8V, an OV threshold of 28.3V and a PG threshold of 20.75V. Figure 7 shows a 3.3V application with a UV threshold of 2.87V, an OV threshold of 3.77V and a PG threshold of 3.05V. Figure 8 shows a backplane resident application, where load insertion activates turn-on.



*TVS Z1: DIODES INC SMAJ17A

Figure 7. 3.3V, 6A Card Resident Application



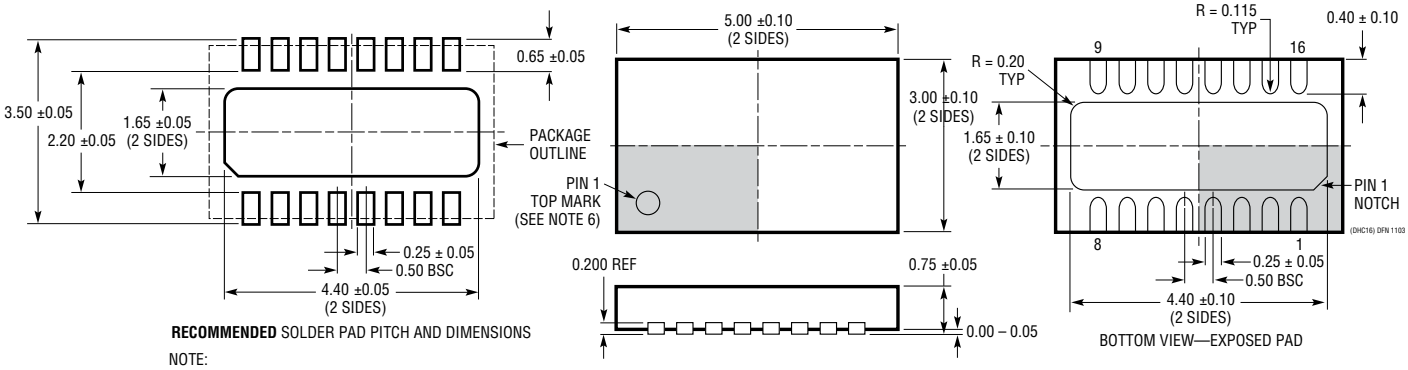
*TVS Z1: DIODES INC SMAJ17A

Figure 8. 12V, 6A Backplane Resident Application with Insertion Activated Turn -On

PACKAGE DESCRIPTION

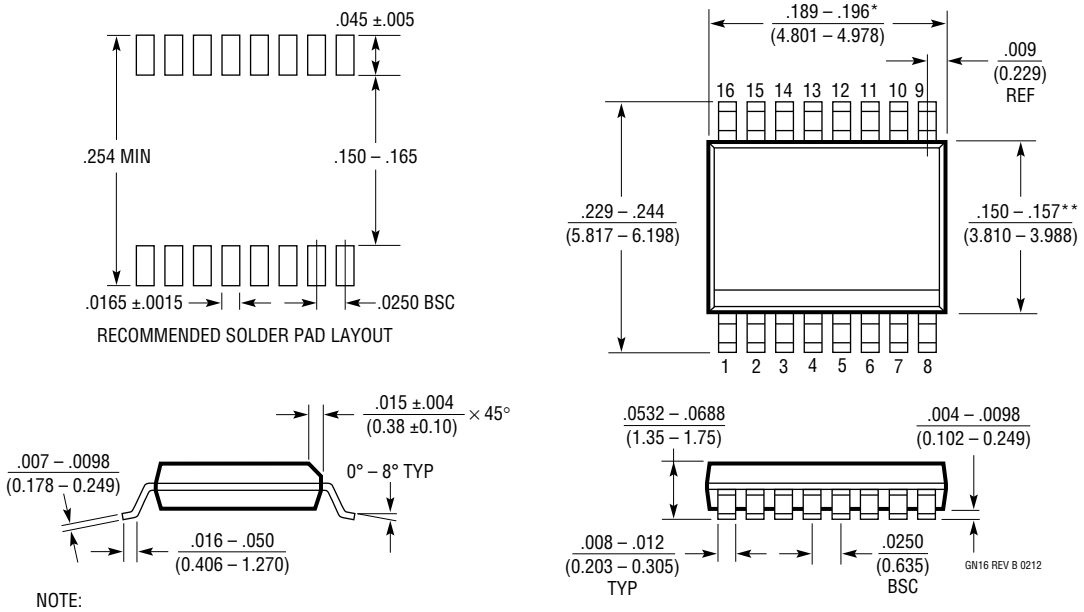
Please refer to http://www.linear.com/product/LTC4218#packaging for the most recent package drawings.

DHC Package
16-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1706)



NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641 Rev B)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

REVISION HISTORY (Revision history begins at Rev D)

REV	DATE	DESCRIPTION	PAGE NUMBER
D	12/09	Revised Order Information.	2
		Revised Equation in Applications Information.	14
E	4/10	Revised Storage Temperature Range in Absolute Maximum Ratings section.	2
		Revised Additional Applications section and inserted Figure 8 in Applications Information.	15
F	1/12	Updated Typical Applications.	1
		Revised Inputs and Outputs sections of Electrical Characteristics.	3
		Updated $INTV_{CC}$ and PG pin descriptions.	7
		Changed value of R2 in Figure 1.	10
		Deleted text from Overcurrent & Fault section and updated values in Monitor OV and UV Faults section.	11, 12
		Revised Typical Application and Related Parts list.	18
G	7/14	$I_{GATE(DN)}$ Specification: Changed maximum from 340µA to 400µA	3
		I_{SET} Pin Function: Added note that resistor should not be less than 2k	7
H	2/16	Added SMAJ17A TVS to application circuit	1, 10, 13, 15
		Changed $INTV_{CC}$ capacitor to 1µF in application circuit	1, 10, 13, 15, 18
		Clarified that operating temperature range refers to ambient	2
		Added BW_{IMON} and $t_{D(FAULT)}$ specifications	4
		Updated $INTV_{CC}$ and I_{SET} pin functions	7
		Figure 1: Added C2	10
		Added section titled Current Limit Stability	11
		Added recommendation for a 0.1µF I_{SET} capacitor	12

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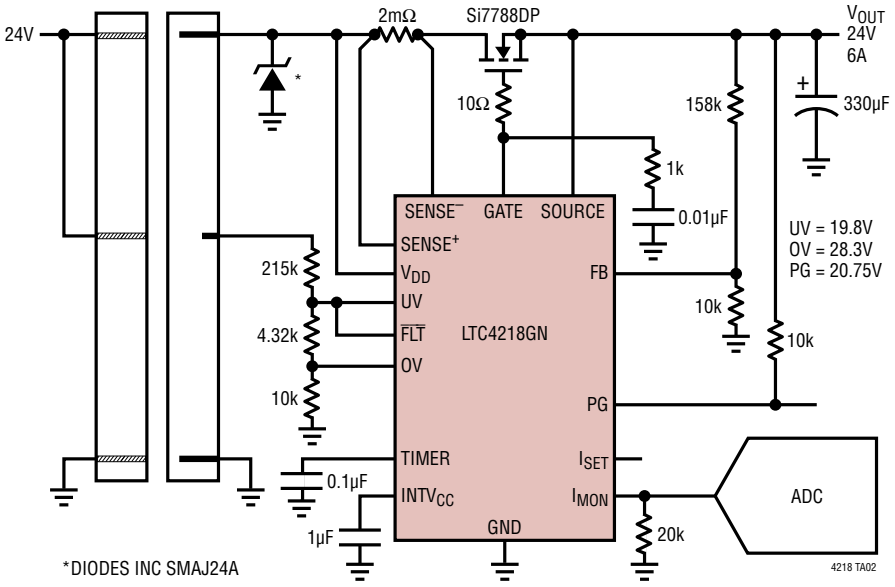
TYPICAL APPLICATION

24V, 6A Card Resident Application with Auto-Retry



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4210	Hot Swap Controller	Operates from 2.7V to 16.5V, Active Current Limiting, SOT23-6
LTC4211	Hot Swap Controller	Operates from 2.5V to 16.5V, Multifunction Current Control, MSOP-8 or MSOP-10
LTC4212	Hot Swap Controller	Operates from 2.5V to 16.5V, Power-Up Timeout, MSOP-10
LTC4214	Negative Voltage Hot Swap Controller	Operates from 0V to –16V, MSOP-10
LTC4215	Hot Swap Controller with ADC and I^2C Interface	Operates from 2.9V to 15V, Digitally Monitors Voltage and Current with 8-Bit ADC
LT4220	Positive and Negative Voltage, Dual Channel, Hot Swap Controller	Operates from ±2.7V to ±16.5V, SSOP-16
LTC4221	Dual Hot Swap Controller/Sequencer	Operates from 1V to 13.5V, Multifunction Current Control, SSOP-16
LTC4230	Triple Channel Hot Swap Controller	Operates from 1.7V to 16.5V, Multifunction Current Control, SSOP-20
LTC4245	Quad Hot Swap Controller with ADC and I^2C Interface	3.3V, 5V and ±12V for CompactPCI, or 3.3V, 3.3V Auxiliary and 12V for PCI-Express, Monitors Voltage and Current with 8-Bit ADC
LTC4232	5A Integrated Hot Swap Controller	2.9V to 15V Operation, 10% Accurate Current Limit
LTC4217	2A Integrated Hot Swap Controller	Operates from 2.9V to 26.5V, Adjustable 5% Accurate Current Limit
LTC4233	10A Guaranteed SOA Hot Swap Controller	Operates from 2.9V to 15V, Adjustable 11% Current Limit
LTC4234	20A Guaranteed SOA Hot Swap Controller	Operates from 2.9V to 15V, Adjustable 11% Current Limit

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- Obsolete Management
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- Alternative Solution
- Excess Inventory Management