



THE DATASHEET OF
963709-1



TLIN1029A-Q1 Fault Protected LIN Transceiver with Dominant State Timeout

1 Features

- AEC-Q100 (Grade 1) Qualified for automotive applications
- Compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2 A and ISO/DIS 17987–4 electrical physical layer (EPL) specification
- Conforms to SAE J2602-1 LIN network for vehicle applications
- **Functional Safety-Capable**
 - [Documentation available to aid in functional safety system design](#)
- Supports 12 V applications
- LIN transmit data rate up to 20-kbps
- LIN receive data rate up to 100 kbps
- Wide operational supply voltage range from 4-V to 36-V
- Sleep mode: ultra-low current consumption allows wake-up event from:
 - LIN bus
 - Local wake up through EN
- Power up and down glitch free operation on LIN bus and RXD output
- Protection features:
 - ± 45 -V LIN bus fault tolerant
 - Under voltage protection on V_{SUP}
 - TXD Dominant time out protection (DTO)
 - Thermal shutdown protection
 - Unpowered node or ground disconnection failsafe at system level.
- Available in SOIC (8) and leadless VSON (8) with wettable flanks

2 Applications

- [Body electronics and lighting](#)
- [Infotainment and cluster](#)
- [Hybrid electric vehicles and power train systems](#)
- [Passive safety](#)
- [Appliances](#)

3 Description

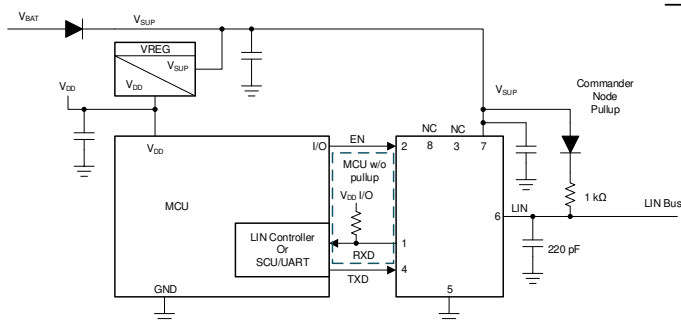
The TLIN1029A-Q1 is a local interconnect network (LIN) physical layer transceiver with integrated wake-up and protection features, compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2 A and ISO/DIS 17987–4 standards. LIN is a single-wire bidirectional bus typically used for in-vehicle networks using data rates up to 20 kbps. The TLIN1029A-Q1 is designed to support 12-V applications with wider operating voltage range and additional bus-fault protection.

The LIN receiver supports data rates up to 100 kbps for faster in-line programming. The TLIN1029A-Q1 converts the data stream on the TXD input into a LIN bus signal using a current-limited wave-shaping driver which reduces electromagnetic emissions (EME). The receiver converts the data stream to logic level signals that are sent to the microprocessor through the open-drain RXD pin. Ultra-low current consumption is possible using the sleep mode which allows wake-up via LIN bus or EN pin.

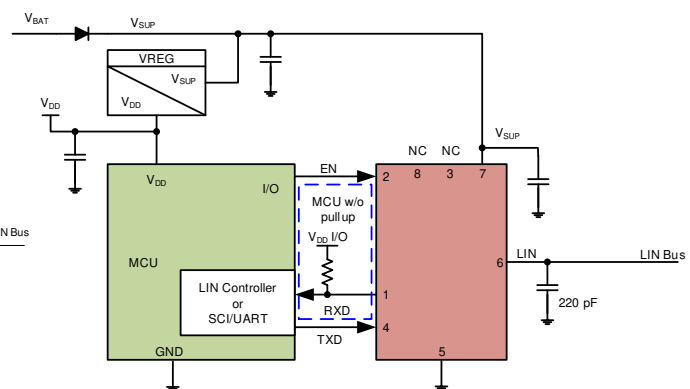
Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
TLIN1029A-Q1	SOIC (D) (8)	4.90 mm x 3.91 mm
	VSON (DRB) (8)	3.00 mm x 3.00 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematics, Commander Mode



Simplified Schematics, Responder Mode



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2020) to Revision A (April 2022)	Page
• Added the <i>Functional Safety-Capable</i> feature.....	1
• Removed the <i>Product Preview</i> note from the D package in the Device Information table	1
• Changed all instances of legacy terminology to commander and responder where mentioned.....	1
• Deleted Notes 1 and 2 from the <i>Simplified Schematics</i> images.....	1

5 Description (continued)

The TLIN1029A-Q1 integrates a resistor for LIN responder node applications, ESD protection, and fault protection which allow for a reduced amount of external components in the applications. The device prevents back-feed current through LIN to the supply input in case of a ground shift or supply voltage disconnection. The TLIN1029A-Q1 also includes undervoltage detection, temperature shutdown protection, and loss-of-ground protection.

6 Pin Configuration and Functions

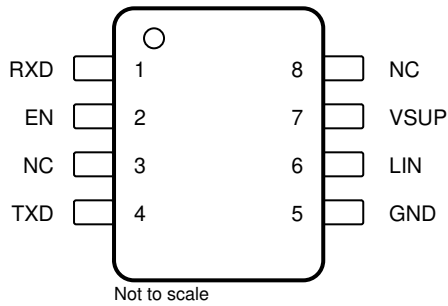


Figure 6-1. D Package, 8-Pin (SOIC), Top View

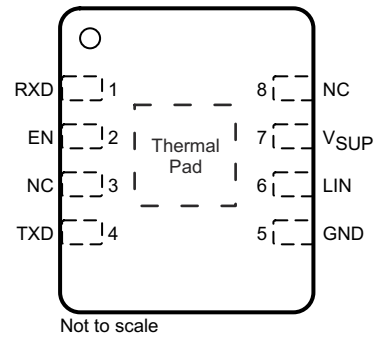


Figure 6-2. DRB Package, 8-Pin (VSON), Top View

Table 6-1. Pin Functions

PIN		Type	DESCRIPTION
Name	No.		
RXD	1	DO	RXD output (open-drain) interface reporting state of LIN bus voltage
EN	2	DI	Enable input - High puts the device in normal operation mode and low puts the device in sleep mode
NC	3	–	Not connected
TXD	4	DI	TXD input interface to control state of LIN output - Internally pulled to ground
GND	5	GND	Ground
LIN	6	HV I/O	LIN bus single-wire transmitter and receiver
V _{SUP}	7	HV Supply	Device supply voltage (connected to battery in series with external reverse blocking diode)
NC	8	–	Not connected
Thermal Pad		-	Can be connected to the PCB ground plane to improve thermal coupling (DRB package only)

7 Specifications

7.1 Absolute Maximum Ratings

(1) (2)

Symbol	Parameter	MIN	MAX	UNIT
V _{SUP}	Supply voltage range (ISO 17987)	-0.3	45	V
V _{LIN}	LIN bus input voltage (ISO 17987)	-45	45	V
V _{LOGIC}	Logic pin voltage (RXD, TXD, EN)	-0.3	6	V
I _O	Digital pin output current		8	mA
T _J	Junction temperature range	-55	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to ground terminal.

7.2 ESD Ratings

ESD Ratings			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM) classification level 3A: TXD, RXD, EN Pins, per AEC Q100-002 ⁽¹⁾	±4000	V
		Human body model (HBM) classification level 3B: LIN and V _{SUP} Pin with respect to ground	±8000	
		Charged device model (CDM) classification level C5, per AEC Q100-011	All terminals ±1500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 ESD Ratings - IEC

ESD and Surge Protection Ratings			VALUE	UNIT
V _(ESD)	Electrostatic discharge, LIN, V _{SUP} to GND ⁽¹⁾	IEC 62228-2 per ISO 10605 Contact discharge R = 330 Ω, C = 150 pF	±8000	V
V _{TRAN}	ISO 7637-2 and IEC 62228-2 per IEC 62215-3 transients according to IBEE LIN EMC test specifications ⁽²⁾ (LIN, V _{SUP} to GND)	Pulse 1	-100	V
		Pulse 2	75	V
		Pulse 3a	-150	V
		Pulse 3b	100	V

- (1) Results given here are specific to the IEC 62228-2 Integrated circuits – EMC evaluation of transceivers – Part 2: LIN transceivers. Testing performed by OEM approved independent 3rd party, EMC report available upon request.
- (2) ISO 7637 is a system level transient test. Different system level configurations may lead to different results

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TLIN1029AD-Q1	TLIN1029ADRB-Q1	UNIT
		D (SOIC)	DRB (VSON)	
		8-PINS	8-PINS	
R _{ΘJA}	Junction-to-ambient thermal resistance	115.5	48.5	°C/W
R _{ΘJC(top)}	Junction-to-case (top) thermal resistance	58.7	55.5	°C/W
R _{ΘJB}	Junction-to-board thermal resistance	58.9	22.2	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	14.1	1.2	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	58.2	22.2	°C/W

7.4 Thermal Information (continued)

THERMAL METRIC ⁽¹⁾		TLIN1029AD-Q1	TLIN1029ADRB-Q1	UNIT
		D (SOIC)	DRB (VSON)	
		8-PINS	8-PINS	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance		4.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

7.5 Recommended Operating Conditions

parameters valid across $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER - DEFINITION		MIN	NOM	MAX	UNIT
V _{SUP}	Supply voltage	4		36	V
V _{LIN}	LIN Bus input voltage	0		36	V
V _{LOGIC}	Logic Pin Voltage (RXD, TXD, EN)	0		5.25	V
T _A	Ambient temperature range	-40		125	°C
TSD	Thermal shutdown temperature	165			°C
TSD _(HYS)	Thermal shutdown hysteresis		15		°C

7.6 Electrical Characteristics

parameters valid across $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
V _{SUP}	Operational supply voltage (ISO/DIS 17987 Param 10)	Device is operational beyond the LIN defined nominal supply voltage range See Figure 8-1 and Figure 8-2	4		36	V
V _{SUP}	Nominal supply voltage (ISO/DIS 17987 Param 10)	Normal and Standby Modes: ramp V _{SUP} while LIN signal is a 10 kHz square wave with 50 % duty cycle and 36V swing. See Figure 8-1 and Figure 8-2	4		36	V
		Sleep Mode	4		36	V
UV _{SUP}	Under voltage V _{SUP} threshold	Min is falling edge and Max is rising edge	2.9		3.85	V
UV _{HYS}	Delta hysteresis voltage for V _{SUP} under voltage threshold			0.2		V
I _{SUP}	Supply current	Normal Mode: EN = high, bus dominant: total bus load where R _{LIN} > 500 Ω and C _{LIN} < 10 nF		1	5	mA
		Standby Mode: EN = low, bus dominant: total bus load where R _{LIN} > 500 Ω and C _{LIN} < 10 nF		1	2.1	mA
I _{SUP}	Supply current	Normal Mode: EN = high, bus recessive (LIN = V _{SUP})		300	650	μA
		Standby Mode: EN = low, bus recessive (LIN = V _{SUP})		10	30	μA
		Sleep Mode: 4.0 V < V _{SUP} ≤ 14 V, LIN = V _{SUP} , EN = 0 V, TXD and RXD floating		8	12	μA
		Sleep Mode: 14 V < V _{SUP} ≤ 36 V, LIN = V _{SUP} , EN = 0 V, TXD and RXD floating			20	μA
TSD	Thermal shutdown		165			°C
TSD _(HYS)	Thermal shutdown hysteresis			15		°C
RXD Output Pin (Open Drain)						

7.6 Electrical Characteristics (continued)

parameters valid across $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Output low voltage	Based upon external pull-up to V_{CC} ⁽⁴⁾			0.6	V
I_{OL}	Low level output current, open drain	LIN = 0 V, RXD = 0.4 V	1.5			mA
I_{ILG}	Leakage current, high-level	LIN = V_{SUP} , RXD = 5 V	-5	0	5	μA
TXD Input Pin						
V_{IL}	Low level input voltage		-0.3		0.8	V
V_{IH}	High level input voltage		2		5.25	V
I_{ILG}	Low level input leakage current	TXD = low	-5	0	5	μA
R_{TXD}	Internal pull-down resistor value		125	350	800	k Ω
LIN PIN						
V_{OH}	LIN recessive high-level output voltage ⁽³⁾	TXD = high, $I_O = 0$ mA, $7\text{ V} \leq V_{SUP} \leq 36$ V	0.85			V_{SUP}
V_{OH}	LIN recessive high-level output voltage ^{(1) (2)}	TXD = high, $I_O = 0$ mA, $7\text{ V} \leq V_{SUP} \leq 18$ V	0.8			V_{SUP}
V_{OH}	LIN recessive high-level output voltage ⁽³⁾	TXD = high, $I_O = 0$ mA, $4\text{ V} \leq V_{SUP} < 7$ V	3			V
V_{OL}	LIN dominant low-level output voltage ⁽³⁾	TXD = low, $7\text{ V} \leq V_{SUP} \leq 36$ V			0.2	V_{SUP}
V_{OL}	LIN dominant low-level output voltage ^{(1) (2)}	TXD = low, $7\text{ V} \leq V_{SUP} \leq 18$ V			0.2	V_{SUP}
V_{OL}	LIN dominant low-level output voltage ⁽³⁾	TXD = low, $4\text{ V} \leq V_{SUP} < 7$ V			1.2	V
$V_{SUP_NON_OP}$	V_{SUP} where impact of recessive LIN bus < 5% (ISO/DIS 17987 Param 11)	TXD & RXD open LIN = 4 V to 45 V	-0.3		45	V
I_{BUS_LIM}	Limiting current (ISO/DIS 17987 Param 12)	TXD = 0 V, $V_{LIN} = 18$ V, $V_{SUP} = 18$ V	40	90	200	mA
$I_{BUS_PAS_dom}$	Receiver leakage current, dominant (ISO/DIS 17987 Param 13)	LIN = 0 V, $V_{SUP} = 12$ V Driver off/ recessive Figure 8-6	-1			mA
$I_{BUS_PAS_rec1}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	LIN > V_{SUP} , $4\text{ V} \leq V_{SUP} \leq 36$ V Driver off; Figure 8-7			20	μA
$I_{BUS_PAS_rec2}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	LIN = V_{SUP} , Driver off; Figure 8-7	-5		5	μA
$I_{BUS_NO_GND}$	Leakage current, loss of ground (ISO/DIS 17987 Param 15)	GND = V_{SUP} , $V_{SUP} = 18$ V, $R_{Meas} = 1$ k Ω , $0\text{ V} < V_{LIN} < 18$ V; Figure 8-8	-1		1	mA
$I_{leak_gnd(dom)}$	Leakage current, loss of ground ⁽⁵⁾	$V_{SUP} = 8$ V, GND = open, $V_{SUP} = 18$ V, GND = open $R_{Commander} = 1$ k Ω , $C_L = 1$ nF $R_{Responder} = 20$ k Ω , $C_L = 1$ nF LIN = dominant	-1		1	mA
$I_{leak_gnd(rec)}$	Leakage current, loss of ground ⁽⁵⁾	$V_{SUP} = 8$ V, GND = open, $V_{SUP} = 18$ V, GND = open $R_{Commander} = 1$ k Ω , $C_L = 1$ nF $R_{Responder} = 20$ k Ω , $C_L = 1$ nF LIN = recessive	-100		100	μA
$I_{BUS_NO_BAT}$	Leakage current, loss of supply (ISO/DIS 17987 Param 16)	LIN = 18 V, $V_{SUP} = \text{GND}$; Figure 8-9			5	μA
V_{BUSdom}	Low level input voltage (ISO/DIS 17987 Param 17) ⁽³⁾	LIN dominant (including LIN dominant for wake up) See Figure 8-4 , Figure 8-3			0.4	V_{SUP}
V_{BUSrec}	High level input voltage (ISO/DIS 17987 Param 18) ⁽³⁾	LIN recessive See Figure 8-4 , Figure 8-3	0.6			V_{SUP}
V_{IH}	LIN recessive high-level input voltage ^{(1) (2)}	$7\text{ V} \leq V_{SUP} \leq 18$ V	0.47		0.6	V_{SUP}
V_{IL}	LIN dominant low-level input voltage ^{(1) (2)}	$7\text{ V} \leq V_{SUP} \leq 18$ V	0.4		0.53	V_{SUP}

7.6 Electrical Characteristics (continued)

 parameters valid across $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{BUS_CNT}	Receiver center threshold (ISO/DIS 17987 Param 19)	$V_{\text{BUS_CNT}} = (V_{\text{BUSrec}} + V_{\text{BUSdom}})/2$ See Figure 8-4 , Figure 8-3	0.475	0.5	0.525	V _{SUP}
V _{HYS}	Hysteresis voltage (ISO/DIS 17987 Param 20)	$V_{\text{HYS}} = (V_{\text{BUSrec}} - V_{\text{BUSdom}})$ See Figure 8-4 , Figure 8-3			0.175	V _{SUP}
V _{HYS}	Hysteresis voltage (SAE J2602)	$V_{\text{HYS}} = V_{\text{IH}} - V_{\text{IL}}$ See Figure 8-4 , Figure 8-3	0.07		0.175	V _{SUP}
V _{SERIAL_DIODE}	Serial diode LIN termination pull-up path	I _{SERIAL_DIODE} = 10 μA	0.4	0.7	1	V
R _{PU}	Internal pull-up resistor to V _{SUP}	Normal and standby modes	20	45	60	kΩ
I _{RSLEEP}	Pull-up current source to V _{SUP}	Sleep mode, V _{SUP} = 14 V, LIN = GND	-20		-2	μA
C _{LINPIN}	Capacitance of the LIN pin	V _{SUP} = 14 V			25	pF
EN Input Pin						
V _{IL}	Low level input voltage		-0.3		0.8	V
V _{IH}	High level input voltage		2		5.25	V
V _{IT}	Hysteresis voltage	By design and characterization		50	500	mV
I _{ILG}	Low level input current	EN = low	-5	0	5	μA
R _{EN}	Internal pull-down resistor		125	350	800	kΩ

- (1) SAE 2602 commander node load conditions: 5.5 nF/4 kΩ and 899 pF/20 kΩ
- (2) SAE 2602 responder node load conditions: 5.5 nF/875 Ω and 899 pF/900 Ω
- (3) ISO 17987 bus load conditions (C_{LINBUS}, R_{LINBUS}) include 1 nF/1 kΩ; 6.8 nF/660 Ω; 10 nF/500 Ω.
- (4) RXD uses open drain output structure therefore V_{OL} level is based upon microcontroller supply voltage V_{CC}.
- (5) $I_{\text{leak gnd}} = (V_{\text{BAT}} - V_{\text{LIN}})/R_{\text{Load}}$

7.7 Duty Cycle Characteristics

 parameters valid across $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D1 _{12V}	Duty Cycle 1 (ISO/DIS 17987 Param 27) ⁽³⁾	$TH_{\text{REC(MAX)}} = 0.744 \times V_{\text{SUP}}$, $TH_{\text{DOM(MAX)}} = 0.581 \times V_{\text{SUP}}$, V _{SUP} = 7 V to 18 V, t _{BIT} = 50 μs (20 kbps), D1 = t _{BUS_rec(min)}/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)}	0.396			
D1 _{12V}	Duty Cycle 1 (ISO/DIS 17987 Param 27) ⁽³⁾	$TH_{\text{REC(MAX)}} = 0.625 \times V_{\text{SUP}}$, $TH_{\text{DOM(MAX)}} = 0.581 \times V_{\text{SUP}}$, V _{SUP} = 4 V to 7 V, t _{BIT} = 50 μs (20 kbps), D1 = t _{BUS_rec(min)}/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)}	0.396			
D1	Duty cycle 1 ⁽¹⁾ ⁽²⁾	$TH_{\text{REC(MAX)}} = 0.744 \times V_{\text{SUP}}$, $TH_{\text{DOM(MAX)}} = 0.581 \times V_{\text{SUP}}$, V _{SUP} = 7 V to 18 V, t _{BIT} = 52 μs, D1 = t _{BUS_rec(min)}/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)}	0.396			
D2 _{12V}	Duty Cycle 2 (ISO/DIS 17987 Param 28) ⁽³⁾	$TH_{\text{REC(MIN)}} = 0.422 \times V_{\text{SUP}}$, $TH_{\text{DOM(MIN)}} = 0.284 \times V_{\text{SUP}}$, V _{SUP} = 7 V to 18 V, t _{BIT} = 50 μs (20 kbps), D2 = t _{BUS_rec(MAX)}/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)}			0.581	
D2 _{12V}	Duty Cycle 2 ⁽³⁾	$TH_{\text{REC(MIN)}} = 0.546 \times V_{\text{SUP}}$, $TH_{\text{DOM(MIN)}} = 0.4 \times V_{\text{SUP}}$, V _{SUP} = 4 V to 7 V, t _{BIT} = 50 μs (20 kbps), D2 = t _{BUS_rec(MAX)}/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)}			0.581	
D2	Duty Cycle 2 ⁽¹⁾ ⁽²⁾	$TH_{\text{REC(MIN)}} = 0.422 \times V_{\text{SUP}}$, $TH_{\text{DOM(MIN)}} = 0.284 \times V_{\text{SUP}}$, V _{SUP} = 7 V to 18 V, t _{BIT} = 52 μs, D2 = t _{BUS_rec(MAX)}/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)}			0.581	

7.7 Duty Cycle Characteristics (continued)

parameters valid across $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D3 _{12V}	Duty Cycle 3 (ISO/DIS 17987 Param 29) ⁽³⁾	$TH_{REC(MAX)} = 0.778 \times V_{SUP}$, $TH_{DOM(MAX)} = 0.616 \times V_{SUP}$, $V_{SUP} = 7\text{ V to }18\text{ V}$, $t_{BIT} = 96\ \mu\text{s}$ (10.4 kbps), $D3 = t_{BUS_rec(min)}/(2 \times t_{BIT})$ (See Figure 8-10 , Figure 8-11)	0.417			
D3 _{12V}	Duty Cycle 3 ⁽³⁾	$TH_{REC(MAX)} = 0.645 \times V_{SUP}$, $TH_{DOM(MAX)} = 0.616 \times V_{SUP}$, $V_{SUP} = 4\text{ V to }7\text{ V}$, $t_{BIT} = 96\ \mu\text{s}$ (10.4 kbps), $D3 = t_{BUS_rec(min)}/(2 \times t_{BIT})$ (See Figure 8-10 , Figure 8-11)	0.417			
D3	Duty Cycle 3 ^{(1) (2)}	$TH_{REC(MAX)} = 0.778 \times V_{SUP}$ $TH_{DOM(MAX)} = 0.616 \times V_{SUP}$ $V_{SUP} = 7\text{ V to }18\text{ V}$, $t_{BIT} = 96\ \mu\text{s}$ $D3 = t_{BUS_rec(min)}/(2 \times t_{BIT})$ (See Figure 8-10 , Figure 8-11)	0.417			
D4 _{12V}	Duty Cycle 4 (ISO/DIS 17987 Param 30) ⁽³⁾	$TH_{REC(MIN)} = 0.389 \times V_{SUP}$, $TH_{DOM(MIN)} = 0.251 \times V_{SUP}$, $V_{SUP} = 7\text{ V to }18\text{ V}$, $t_{BIT} = 96\ \mu\text{s}$ (10.4 kbps), $D4 = t_{BUS_rec(MAX)}/(2 \times t_{BIT})$ (See Figure 8-10 , Figure 8-11)			0.59	
D4 _{12V}	Duty Cycle 4 ⁽³⁾	$TH_{REC(MIN)} = 0.422 \times V_{SUP}$, $TH_{DOM(MIN)} = 0.284 \times V_{SUP}$, $V_{SUP} = 4\text{ V to }7\text{ V}$, $t_{BIT} = 96\ \mu\text{s}$ (10.4 kbps), $D4 = t_{BUS_rec(MAX)}/(2 \times t_{BIT})$ (See Figure 8-10 , Figure 8-11)			0.59	
D4	Duty Cycle 4 ^{(1) (2)}	$TH_{REC(MIN)} = 0.389 \times V_{SUP}$ $TH_{DOM(MIN)} = 0.251 \times V_{SUP}$ $V_{SUP} = 7\text{ V to }18\text{ V}$, $t_{BIT} = 96\ \mu\text{s}$ $D4 = t_{BUS_rec(MAX)}/(2 \times t_{BIT})$ (See Figure 8-10 , Figure 8-11)			0.59	
D1 _{LB}	Duty cycle 1 at low battery ^{(1) (2)}	$TH_{REC(MAX)} = 0.665 \times V_{SUP}$, $TH_{DOM(MAX)} = 0.499 \times V_{SUP}$, $V_{SUP} = 5.5\text{ V to }7\text{ V}$, $t_{BIT} = 52\ \mu\text{s}$	0.396			
D2 _{LB}	Duty cycle 2 at low battery ^{(1) (2)}	$TH_{REC(MAX)} = 0.496 \times V_{SUP}$ $TH_{DOM(MAX)} = 0.361 \times V_{SUP}$ $V_{SUP} = 6.1\text{ V to }7\text{ V}$, $t_{BIT} = 52\ \mu\text{s}$			0.581	
D3 _{LB}	Duty cycle 3 at low battery ^{(1) (2)}	$TH_{REC(MAX)} = 0.665 \times V_{SUP}$, $TH_{DOM(MAX)} = 0.499 \times V_{SUP}$, $V_{SUP} = 5.5\text{ V to }7\text{ V}$, $t_{BIT} = 96\ \mu\text{s}$	0.396			
D4 _{LB}	Duty cycle 4 at low battery ^{(1) (2)}	$TH_{REC(MAX)} = 0.496 \times V_{SUP}$ $TH_{DOM(MAX)} = 0.361 \times V_{SUP}$ $V_{SUP} = 6.1\text{ V to }7\text{ V}$, $t_{BIT} = 96\ \mu\text{s}$			0.581	
Tr-d max	Transmitter propagation delay timings for the duty cycle ^{(1) (2)} Recessive to dominant	$TH_{REC(MAX)} = 0.744 \times V_{SUP}$, $TH_{DOM(MAX)} = 0.581 \times V_{SUP}$ $7\text{ V} \leq V_{SUP} \leq 18\text{ V}$, $t_{BIT} = 52\ \mu\text{s}$ $t_{REC(MAX)_D1} - t_{DOM(MIN)_D1}$			10.8	μs
Td-r max	Transmitter propagation delay timings for the duty cycle ^{(1) (2)} Dominant to recessive	$TH_{REC(MAX)} = 0.422 \times V_{SUP}$, $TH_{DOM(MAX)} = 0.284 \times V_{SUP}$ $7\text{ V} \leq V_{SUP} \leq 18\text{ V}$, $t_{BIT} = 52\ \mu\text{s}$ $t_{DOM(MAX)_D2} - t_{REC(MIN)_D2}$			8.4	μs
Tr-d max	Transmitter propagation delay timings for the duty cycle ^{(1) (2)} Recessive to dominant	$TH_{REC(MAX)} = 0.778 \times V_{SUP}$ $TH_{DOM(MAX)} = 0.616 \times V_{SUP}$ $7\text{ V} \leq V_{SUP} \leq 18\text{ V}$, $t_{BIT} = 96\ \mu\text{s}$ $t_{REC(MAX)_D3} - t_{DOM(MIN)_D3}$			15.9	μs
Td-r max	Transmitter propagation delay timings for the duty cycle ^{(1) (2)} Dominant to recessive	$TH_{REC(MIN)} = 0.389 \times V_{SUP}$ $TH_{DOM(MIN)} = 0.251 \times V_{SUP}$ $7\text{ V} \leq V_{SUP} \leq 18\text{ V}$, $t_{BIT} = 96\ \mu\text{s}$ $t_{DOM(MAX)_D4} - t_{REC(MIN)_D4}$			17.28	μs

7.7 Duty Cycle Characteristics (continued)

 parameters valid across $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Tr-d max_low	Low battery transmitter propagation delay timings for the duty cycle ^{(1) (2)} Recessive to dominant	$T_{H_{REC(MAX)}} = 0.665 \times V_{SUP}$, $T_{H_{DOM(MAX)}} = 0.499 \times V_{SUP}$ $5.5 \text{ V} \leq V_{SUP} \leq 7 \text{ V}$, $t_{BIT} = 52 \mu\text{s}$ $t_{REC(MAX)_low} - t_{DOM(MIN)_low}$			10.8	μs
Td-r max_low	Low battery transmitter propagation delay timings for the duty cycle ^{(1) (2)} Dominant to recessive	$T_{H_{REC(MAX)}} = 0.496 \times V_{SUP}$ $T_{H_{DOM(MAX)}} = 0.361 \times V_{SUP}$ $6.1 \text{ V} \leq V_{SUP} \leq 7 \text{ V}$, $t_{BIT} = 52 \mu\text{s}$ $t_{DOM(MAX)_low} - t_{REC(MIN)_low}$			8.4	μs

 (1) SAE 2602 commander node load conditions: 5.5 nF/4 k Ω and 899 pF/20 k Ω

 (2) SAE 2602 responder node load conditions: 5.5 nF/875 Ω and 899 pF/900 Ω

 (3) ISO 17987 bus load conditions (C_{LINBUS} , R_{LINBUS}) include 1 nF/1 k Ω ; 6.8 nF/660 Ω ; 10 nF/500 Ω .

7.8 Switching Characteristics

 parameters valid across $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ (unless otherwise noted)

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{rx_pdr} , t_{rx_pdf}	Receiver rising/falling propagation delay time (ISO/DIS 17987 Param 31)	$R_{RXD} = 2.4 \text{ k}\Omega$, $C_{RXD} = 20 \text{ pF}$ (See Figure 8-12 and Figure 8-13)			6	μs
t_{rs_sym}	Symmetry of receiver propagation delay time Receiver rising propagation delay time	Rising edge with respect to falling edge, ($trx_sym = trx_pdf - trx_pdr$), $R_{RXD} = 2.4 \text{ k}\Omega$, $C_{RXD} = 20 \text{ pF}$ (See Figure 8-12 and Figure 8-13)	-2		2	μs
t_{LINBUS}	LIN wakeup time (Minimum dominant time on LIN bus for wakeup)	See Figure 8-16 , Figure 9-2 , and Figure 9-3	25	65	150	μs
t_{CLEAR}	Time to clear false wakeup prevention logic if LIN bus had a bus stuck dominant fault (recessive time on LIN bus to clear bus stuck dominant fault)	See Figure 9-3	8	25	50	μs
t_{DST}	Dominant state time out		20	45	80	ms
t_{MODE_CHANGE}	Mode change delay time	Time to change from standby mode to normal mode or normal mode to sleep mode through EN pin: (See Figure 8-14 and Figure 9-4)	2		15	μs
t_{NOMINT}	Normal mode initialization time	Time for normal mode to initialize and data on RXD pin to be valid. See Figure 8-14			35	μs
t_{PWR}	Power up time	Upon power up time it takes for valid data on RXD			1.5	ms

7.9 Typical Characteristics

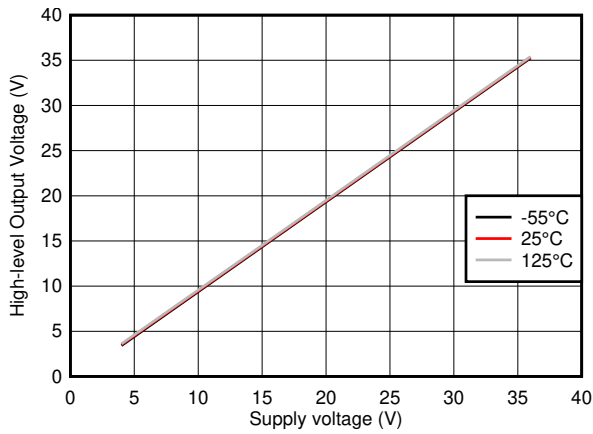


Figure 7-1. V_{OH} vs V_{SUP} and Temperature

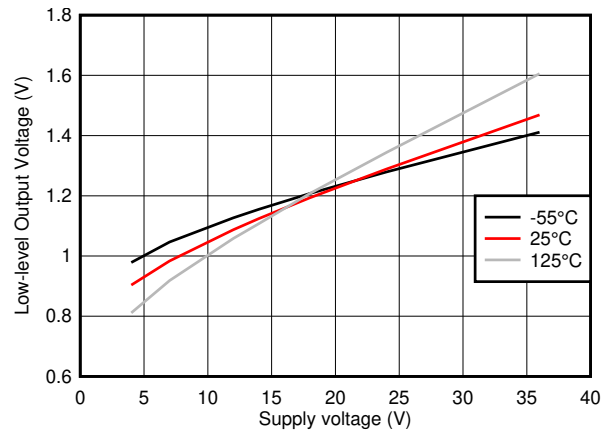


Figure 7-2. V_{OL} vs V_{SUP} and Temperature

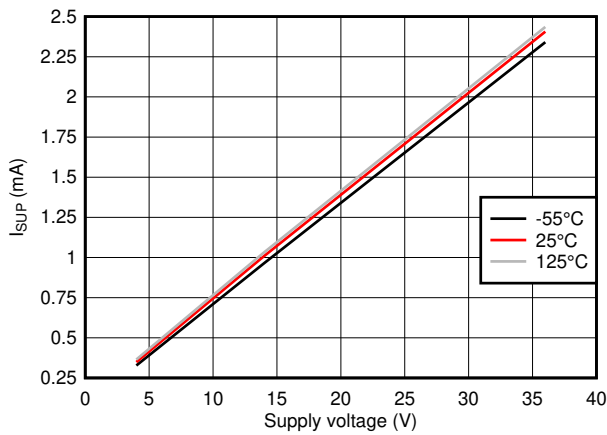


Figure 7-3. Dominant I_{SUP} vs V_{SUP} and Temperature

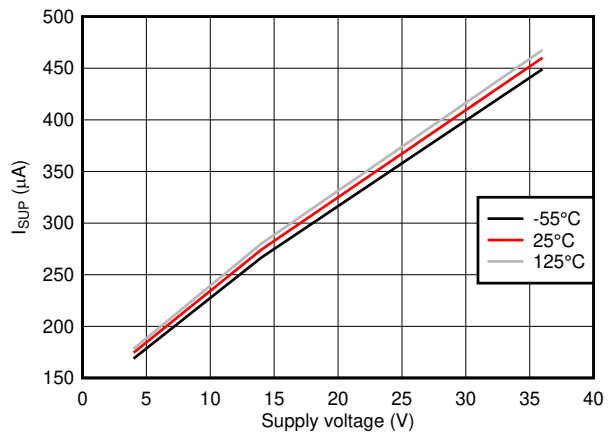


Figure 7-4. Recessive I_{SUP} vs V_{SUP} and Temperature

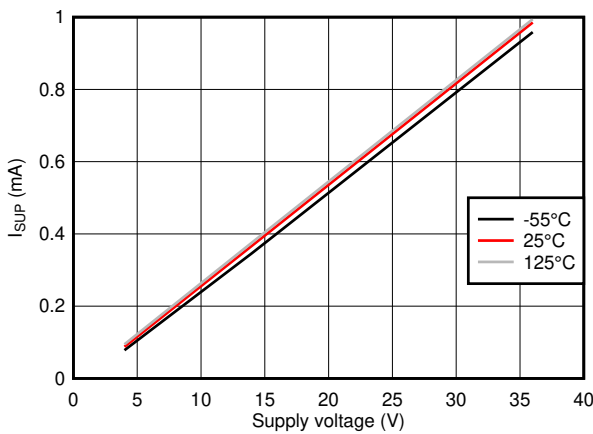


Figure 7-5. Standby Dominant I_{SUP} vs V_{SUP} and Temperature

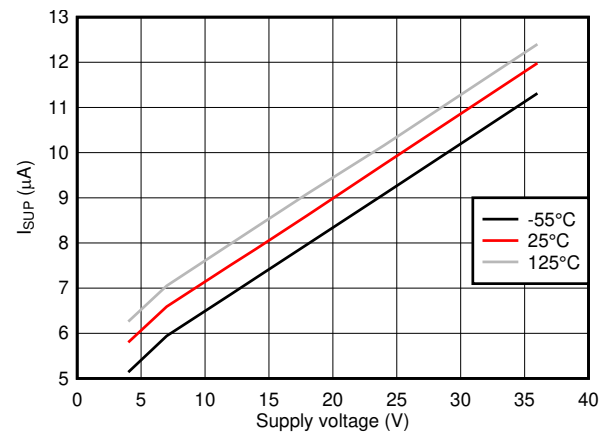


Figure 7-6. Standby Recessive I_{SUP} vs V_{SUP} and Temperature

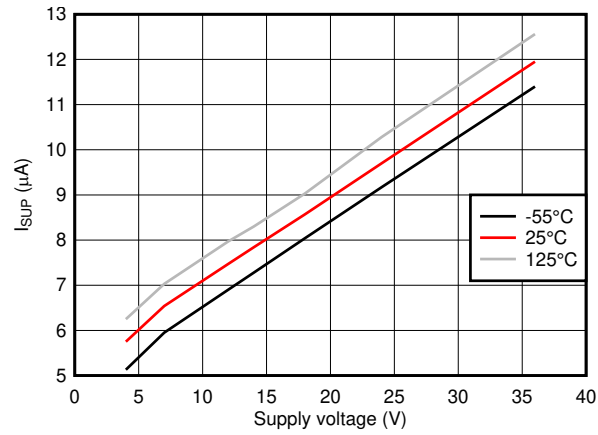
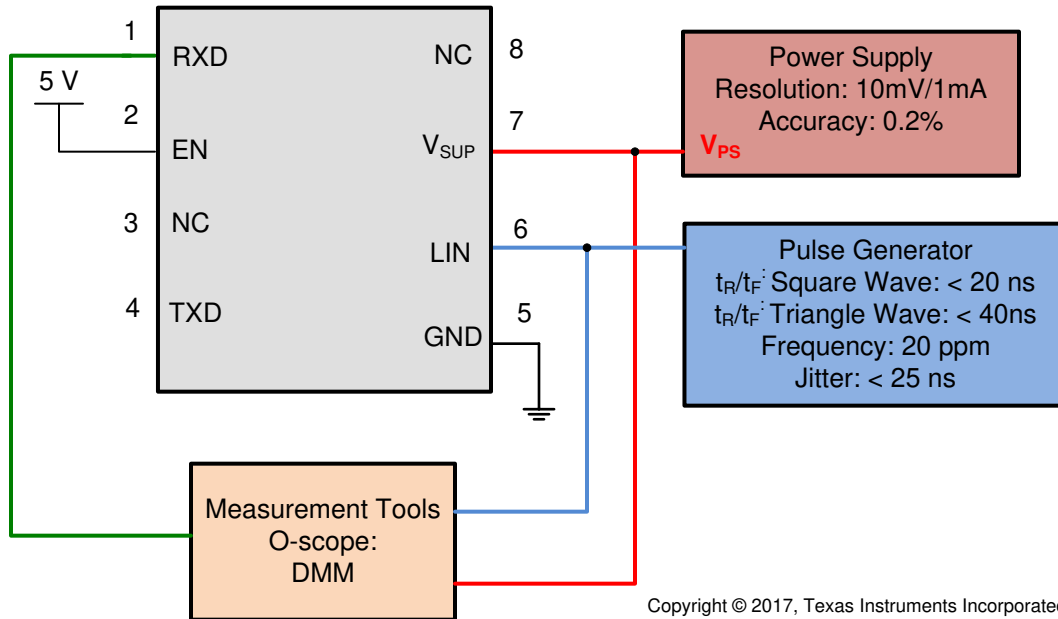


Figure 7-7. Sleep Current vs V_{SUP} and Temperature

8 Parameter Measurement Information



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Figure 8-1. Test System: Operating Voltage Range with RX and TX Access: Parameters 9, 10

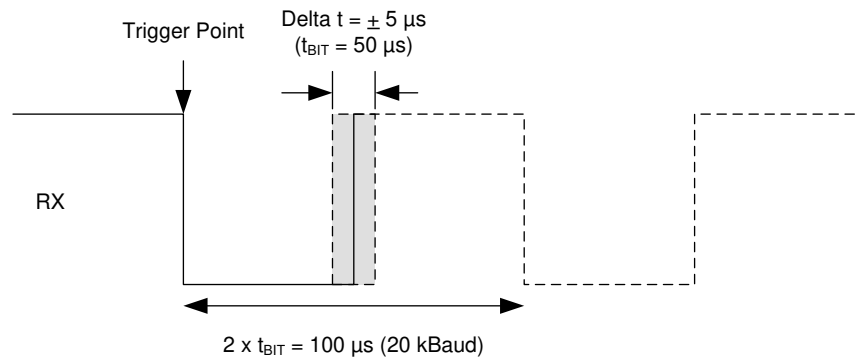


Figure 8-2. RX Response: Operating Voltage Range

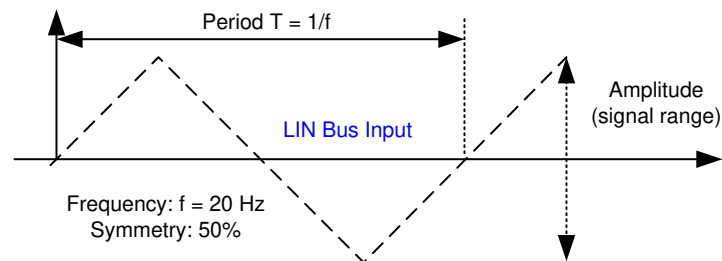


Figure 8-3. LIN Bus Input Signal

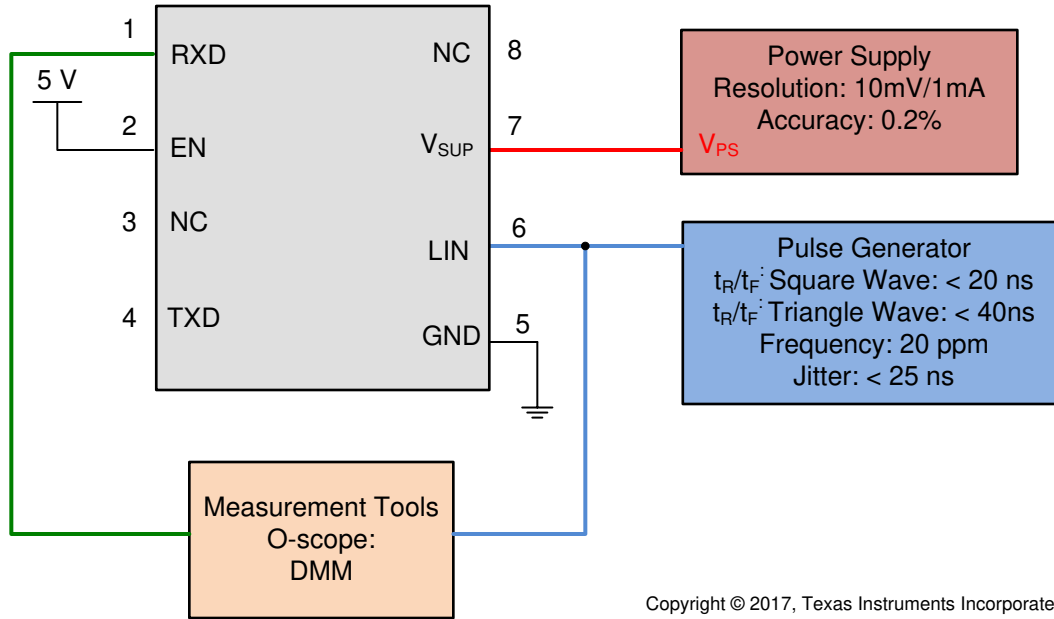


Figure 8-4. LIN Receiver Test with RX access Param 17, 18, 19, 20

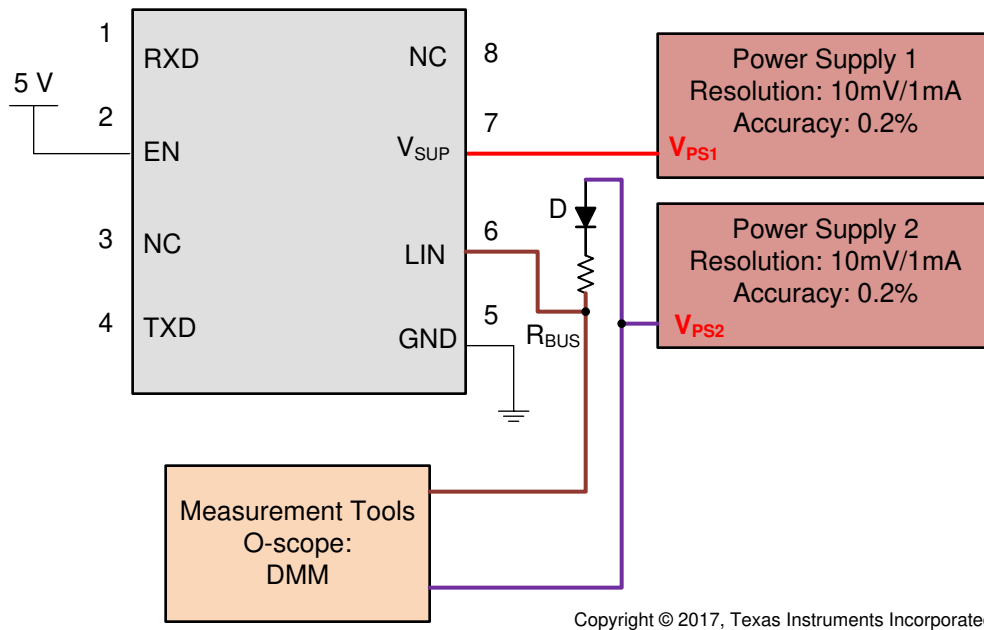
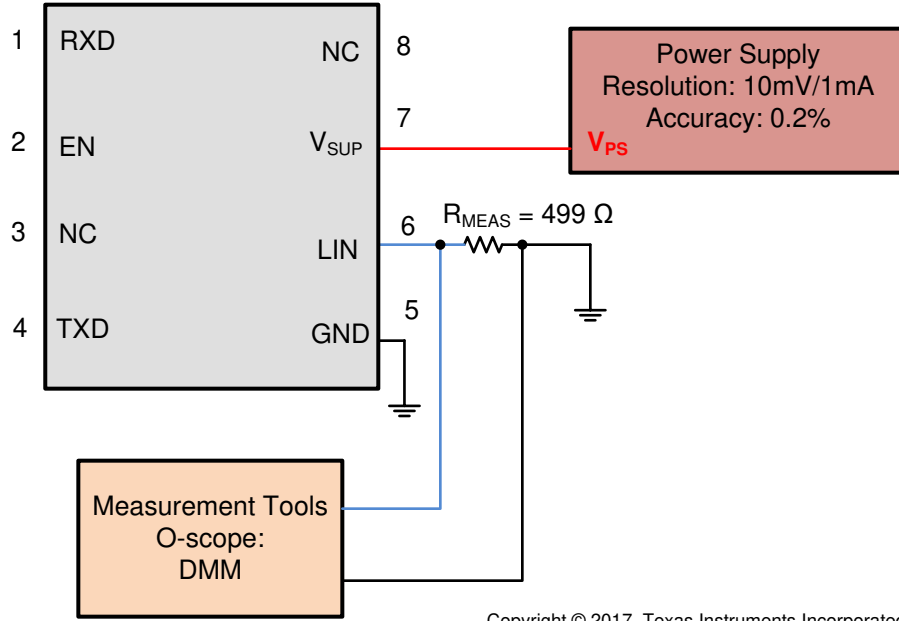
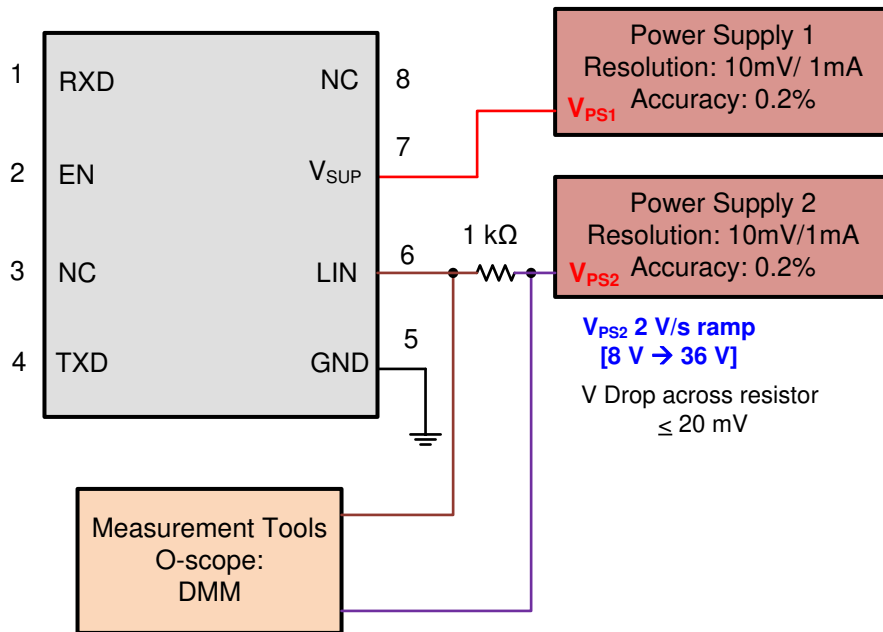


Figure 8-5. V_{SUP_NON_OP} Param 11



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Figure 8-6. Test Circuit for $I_{BUS_PAS_dom}$; TXD = Recessive State $V_{BUS} = 0$ V, Param 13



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Figure 8-7. Test Circuit for $I_{BUS_PAS_rec}$ Param 14

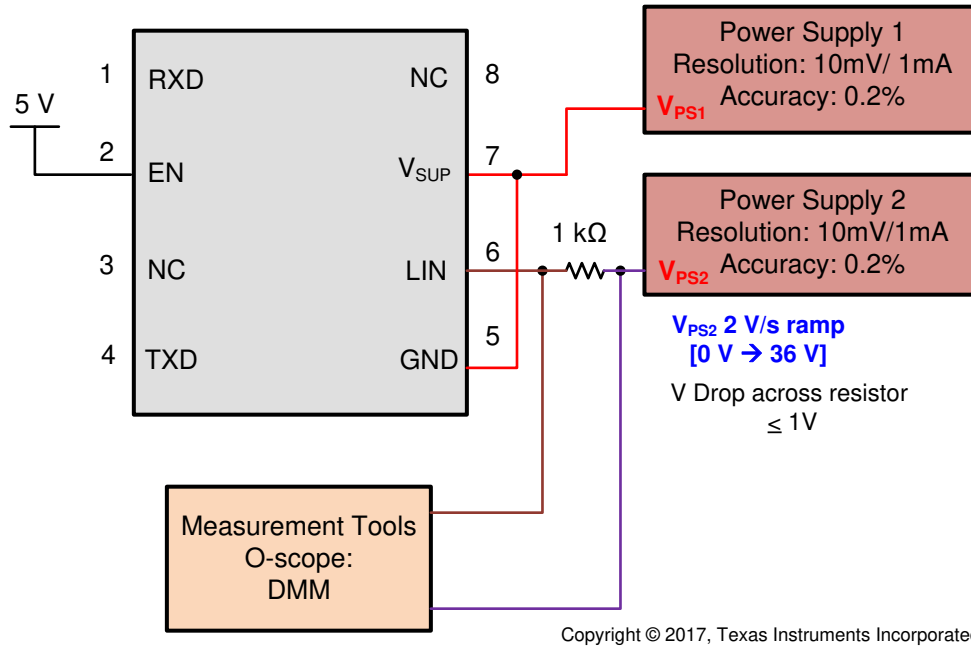


Figure 8-8. Test Circuit for $I_{BUS_NO_GND}$ Loss of GND

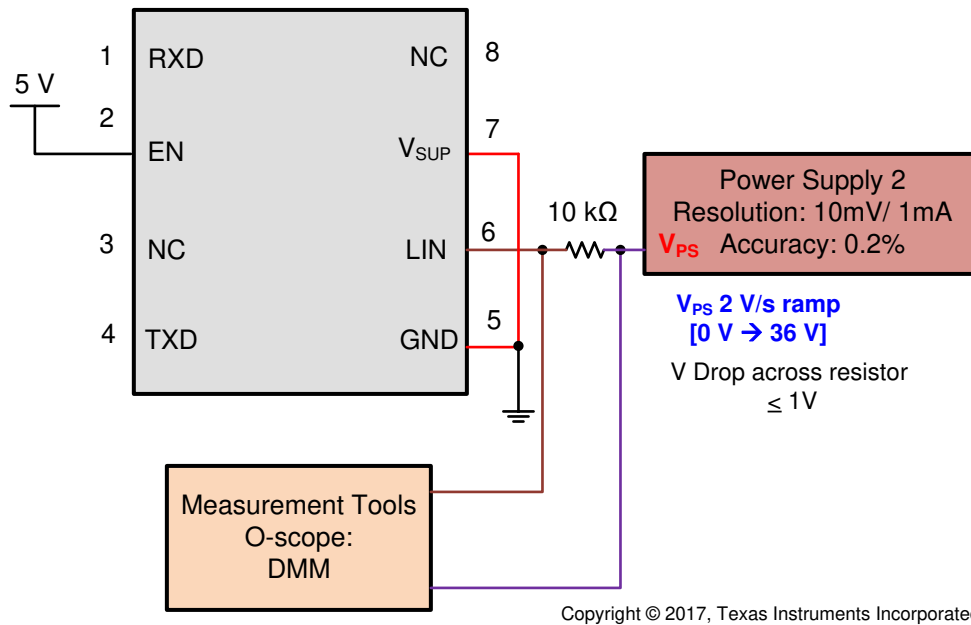


Figure 8-9. Test Circuit for $I_{BUS_NO_BAT}$ Loss of Battery

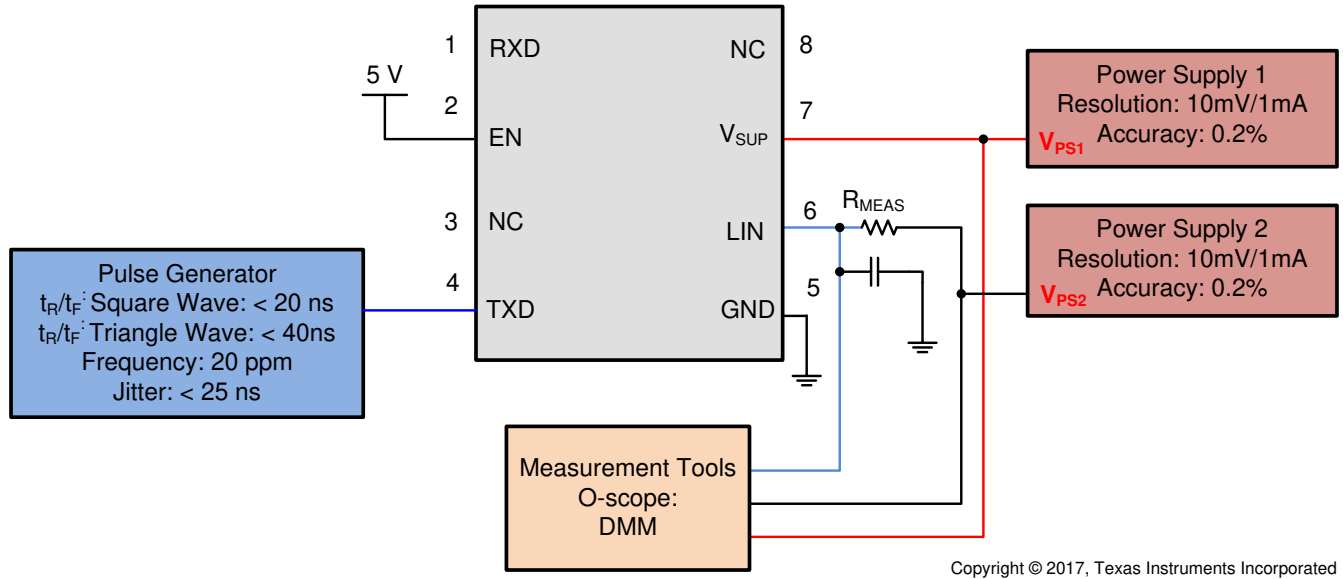


Figure 8-10. Test Circuit Slope Control and Duty Cycle Param 27, 28, 29, 30

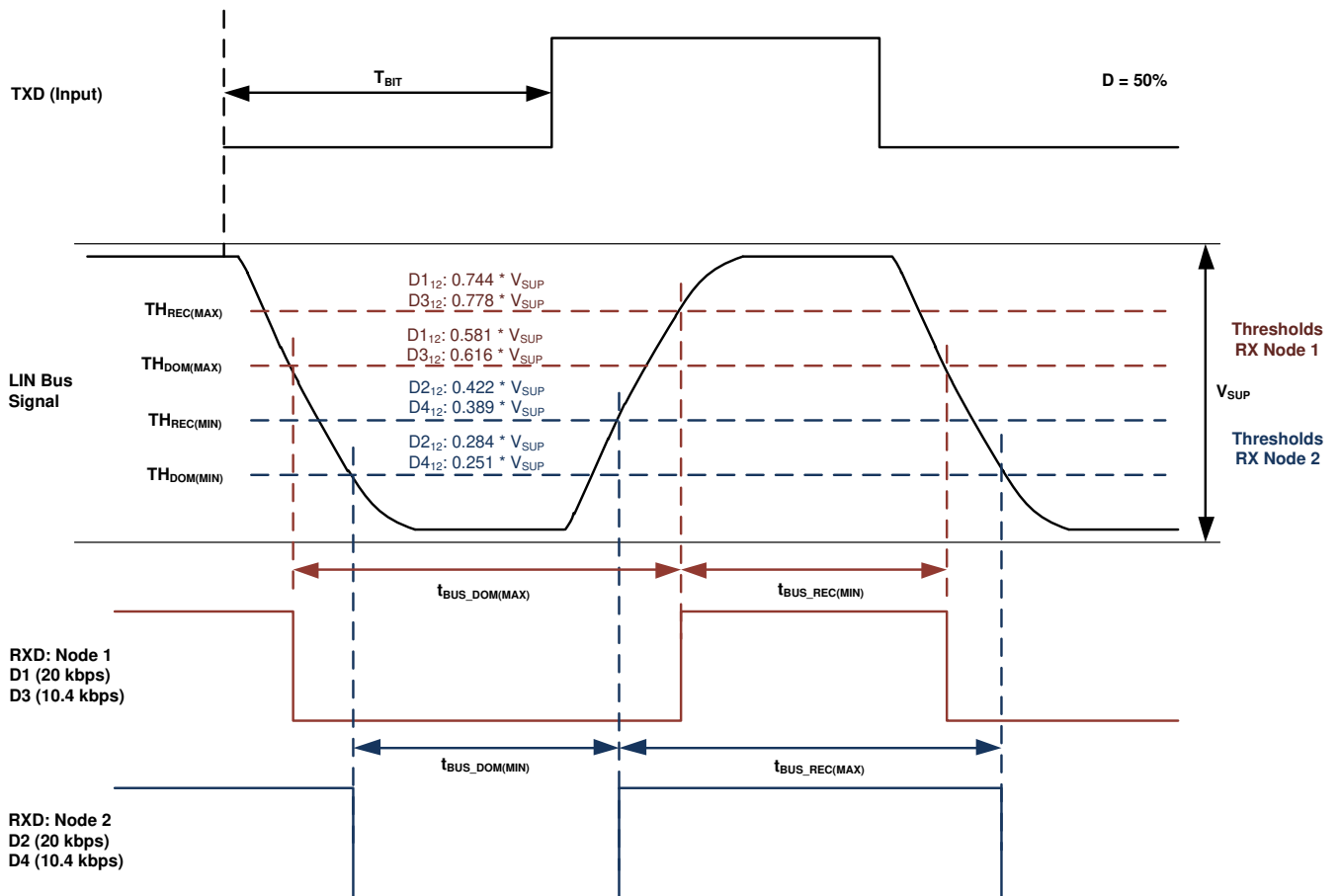
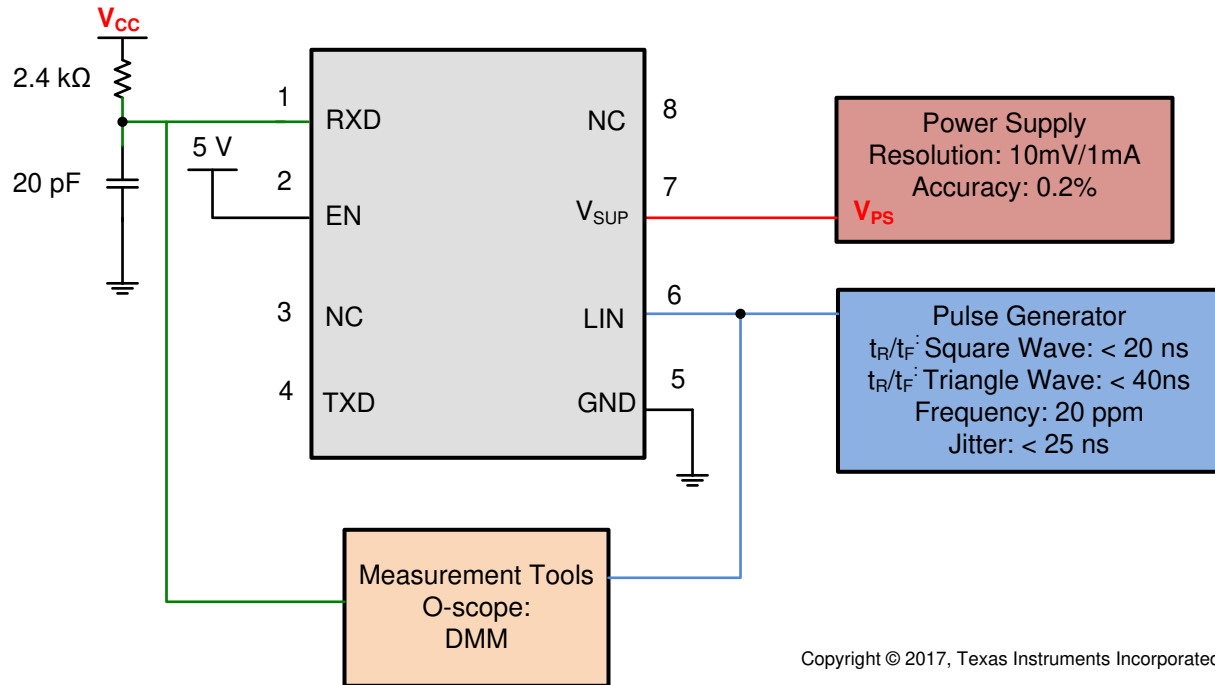


Figure 8-11. Definition of Bus Timing Parameters



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Figure 8-12. Propagation Delay Test Circuit; Param 31, 32

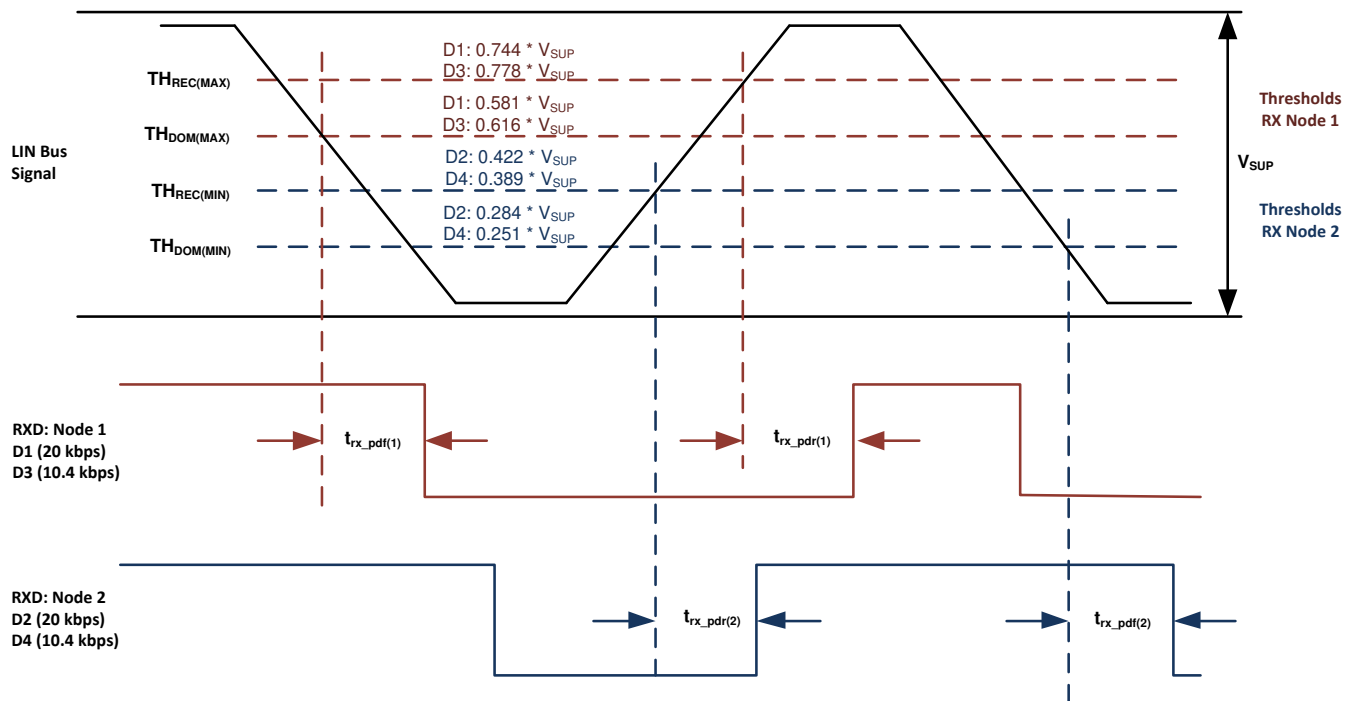


Figure 8-13. Propagation Delay

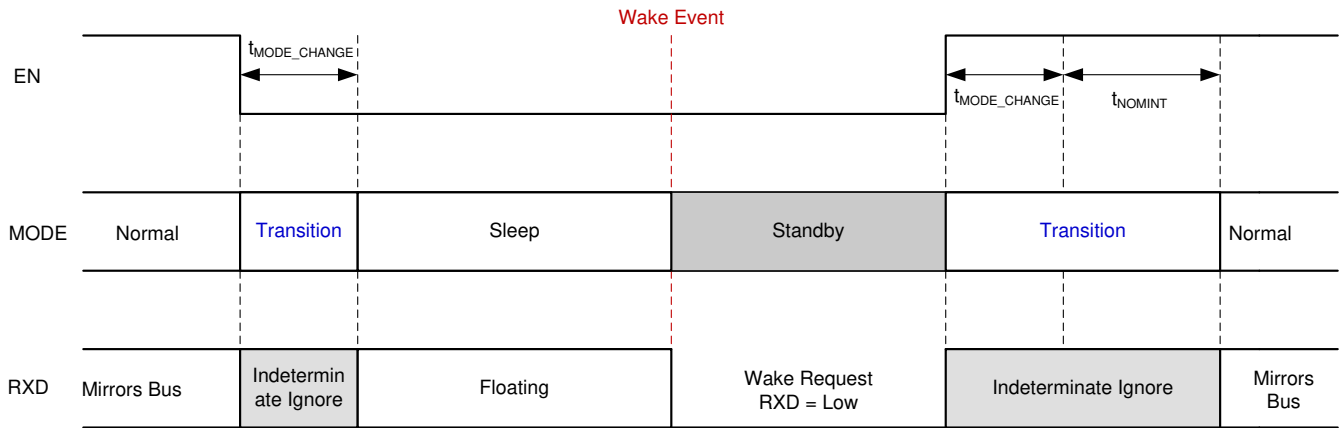


Figure 8-14. Mode Transitions

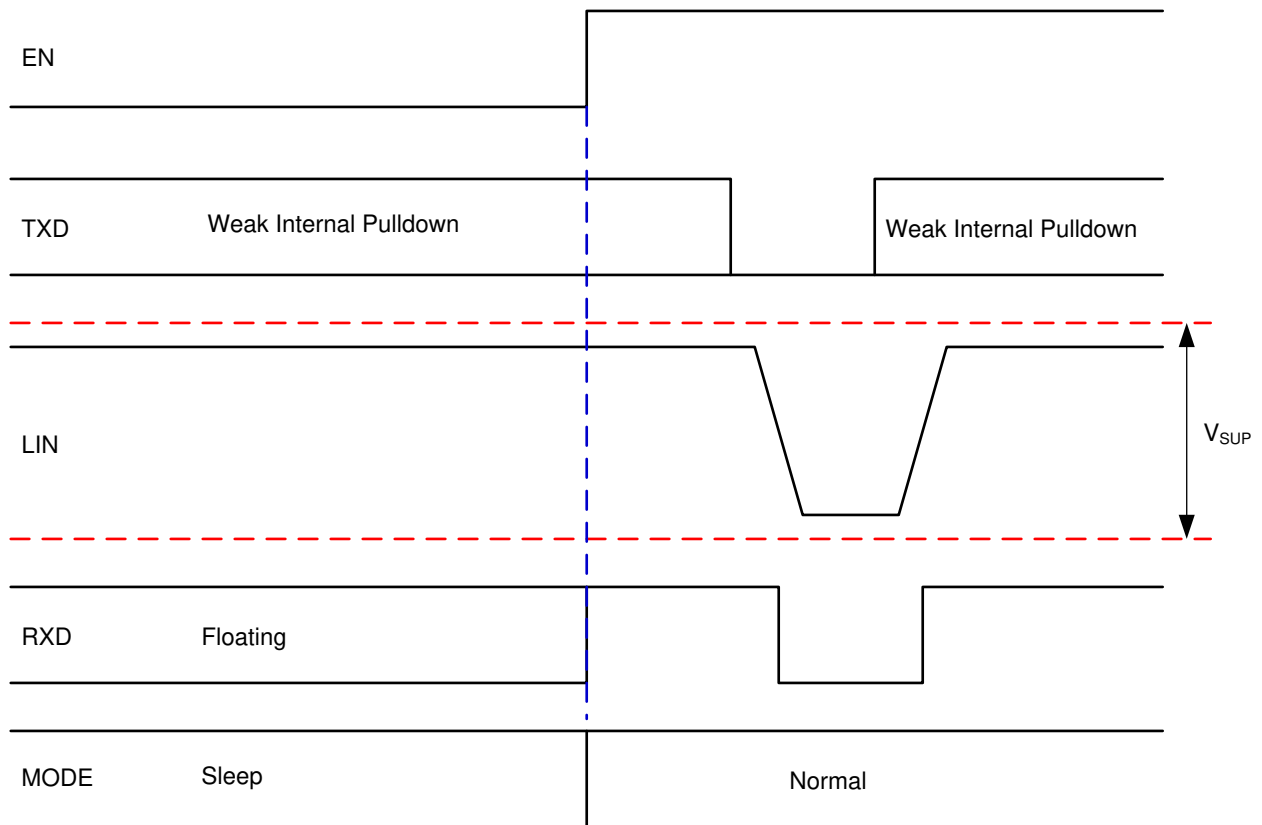


Figure 8-15. Wakeup Through EN

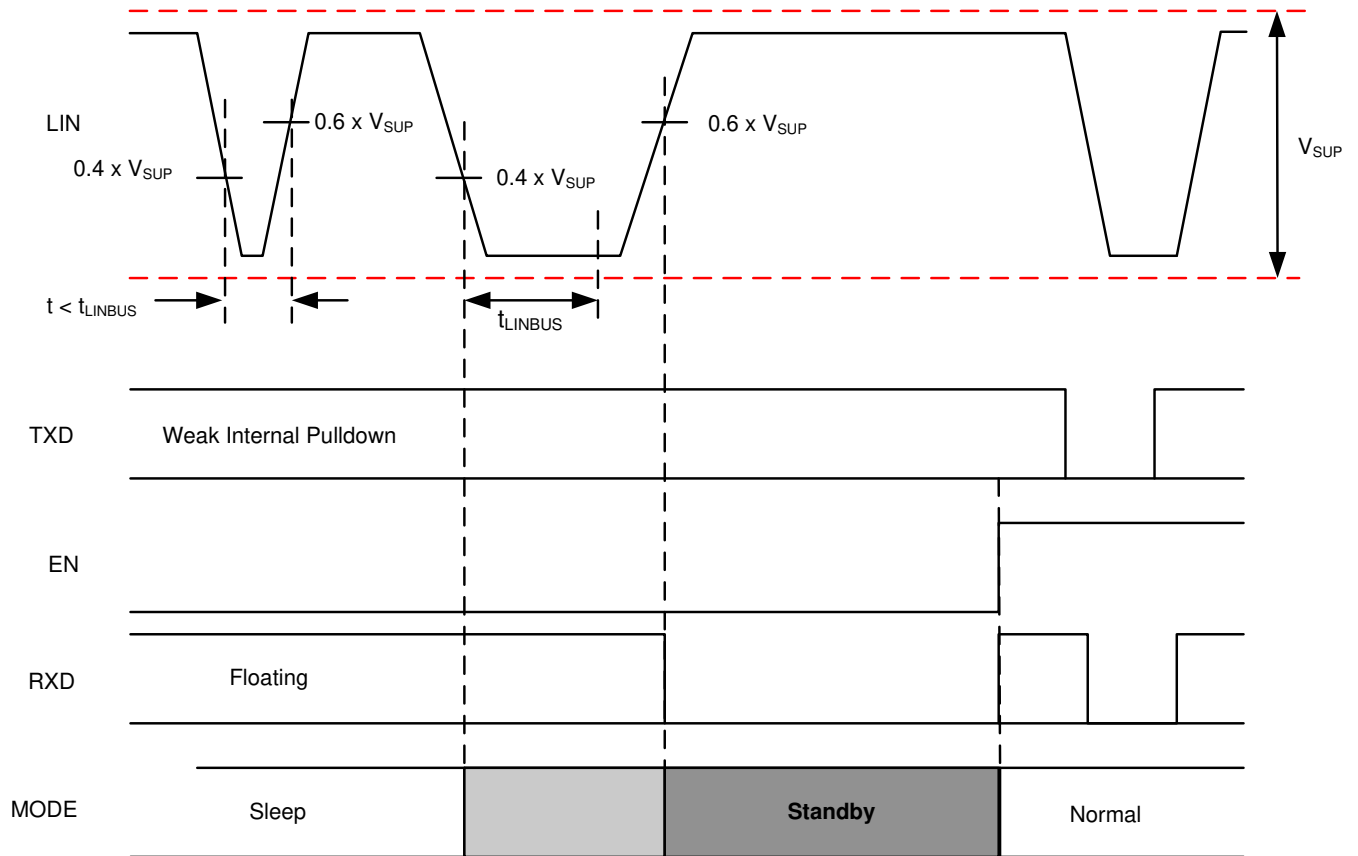


Figure 8-16. Wakeup through LIN

9 Detailed Description

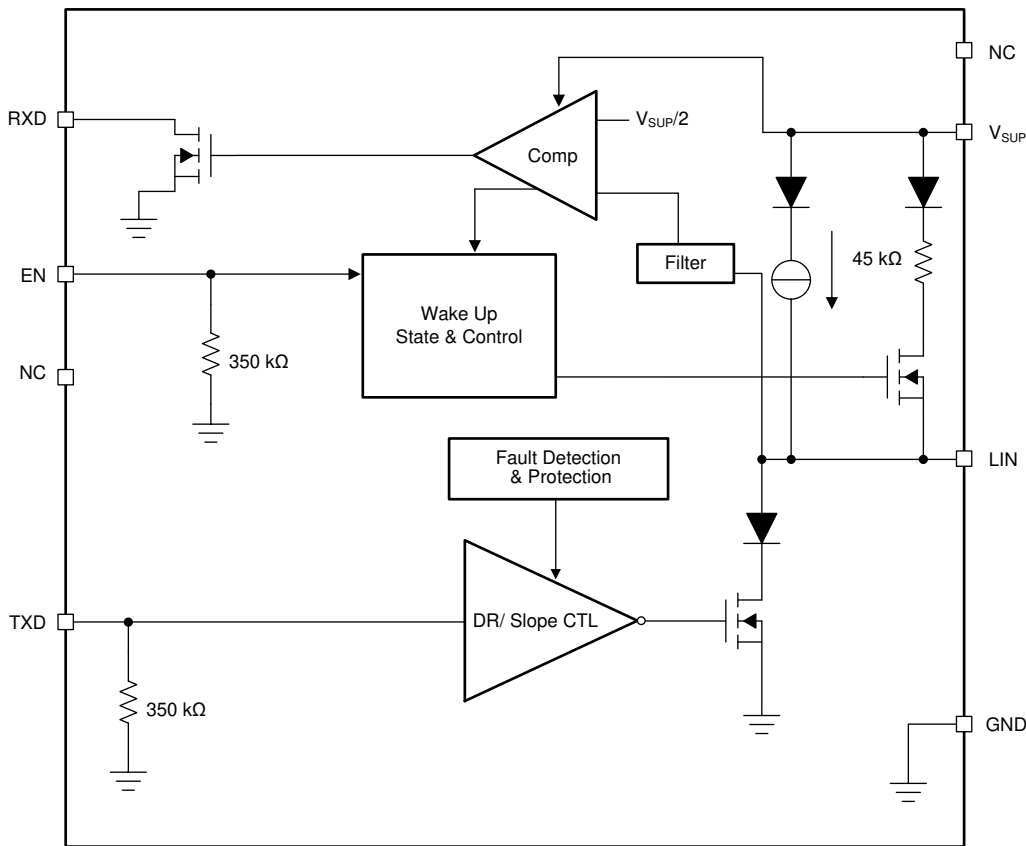
9.1 Overview

The TLIN1029A-Q1 is a Local Interconnect Network (LIN) physical layer transceiver, compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO/DIS 17987–4 standards, with integrated wake-up and protection features. The LIN bus is a single-wire bidirectional bus typically used for low speed in-vehicle networks. The device transmitter supports data rates from 2.4-kbps to 20-kbps and the receiver works up to 100 kbps supporting in-line programming. The LIN protocol data stream on the TXD input is converted by the TLIN1029A-Q1 into a LIN bus signal using a current-limited wave-shaping driver as outlined by the LIN physical layer specification. The receiver converts the data stream to logic-level signals that are sent to the microprocessor through the open-drain RXD pin. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the internal pull-up resistor (45 kΩ) and a series diode. No external pull-up components are required for responder node applications. Commander node applications require an external pull-up resistor (1 kΩ) plus a series diode per the LIN specification.

The device is designed to support 12-V applications with a wide input voltage operating range and also supports low-power sleep mode. The device also provides two methods to wake up: EN pin and from the LIN bus.

The TLIN1029A-Q1 integrates ESD protection and fault protection which allow for a reduction in the required external components in the applications. In the event of a ground shift or supply voltage disconnection, the device prevents back-feed current through LIN to the supply input. The device also includes undervoltage detection, temperature shutdown protection, and loss-of-ground protection.

9.2 Functional Block Diagram



9.3.3 RXD (Receive Output)

RXD is the interface to the MCU's LIN protocol controller or SCI and UART, which reports the state of the LIN bus voltage. LIN recessive (near V_{Battery}) is represented by a high level on the RXD and LIN dominant (near ground) is represented by a low level on the RXD pin. The RXD output structure is an open-drain output stage. This allows the device to be used with 3.3 V and 5 V I/O microcontrollers. If the microcontroller's RXD pin does not have an integrated pull-up, an external pull-up resistor to the microcontroller I/O supply voltage is required. In standby mode the RXD pin is driven low to indicate a wake up request from the LIN bus.

9.3.4 V_{SUP} (Supply Voltage)

V_{SUP} is the power supply pin. V_{SUP} is connected to the battery through an external reverse-blocking diode (Figure 9-1). If there is a loss of power at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

9.3.5 GND (Ground)

GND is the device ground connection. The device can operate with a ground shift as long as the ground shift does not reduce the V_{SUP} below the minimum operating voltage, as well as ensuring the input and output voltages are within their appropriate thresholds. If there is a loss of ground at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

9.3.6 EN (Enable Input)

EN controls the operational modes of the device. When EN is high the device is in normal operating mode allowing a transmission path from TXD to LIN and from LIN to RXD. When EN is low the device is put into sleep mode and there are no transmission paths available. The device can enter normal mode only after wake up. EN has an internal pull-down resistor to ensure the device remains in low-power mode even if EN floats.

9.3.7 Protection Features

The TLIN1029A-Q1 has several protection features that will now be described.

9.3.8 TXD Dominant Time Out (DTO)

During normal mode, if TXD is inadvertently driven permanently low by a hardware or software application failure, the LIN bus is protected by the dominant state timeout timer. This timer is triggered by a falling edge on the TXD pin. If the low signal remains on TXD for longer than t_{DST} , the transmitter is disabled, thus allowing the LIN bus to return to recessive state and communication to resume on the bus. The protection is cleared and the t_{DST} timer is reset by a rising edge on TXD. The TXD pin has an internal pull-down to ensure the device fails to a known state if TXD is disconnected. During this fault, the transceiver remains in normal mode (assuming no change of stated request on EN), the transmitter is disabled, the RXD pin reflects the LIN bus and the LIN bus pull-up termination remains on.

9.3.9 Bus Stuck Dominant System Fault: False Wake Up Lockout

The TLIN1029A-Q1 contains logic to detect bus stuck dominant system faults and prevents the device from waking up falsely during the system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake-up logic is locked out until a valid recessive on the bus "clears" the bus stuck dominant, preventing excessive current consumption. Figure 9-2 and Figure 9-3 show the behavior of this protection.

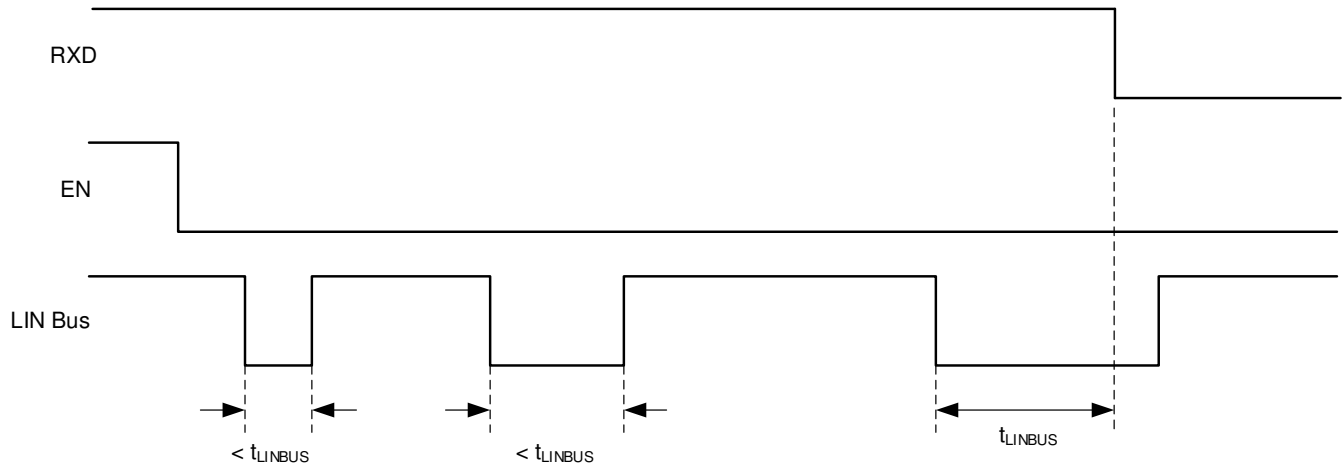


Figure 9-2. No Bus Fault: Entering Sleep Mode with Bus Recessive Condition and Wakeup

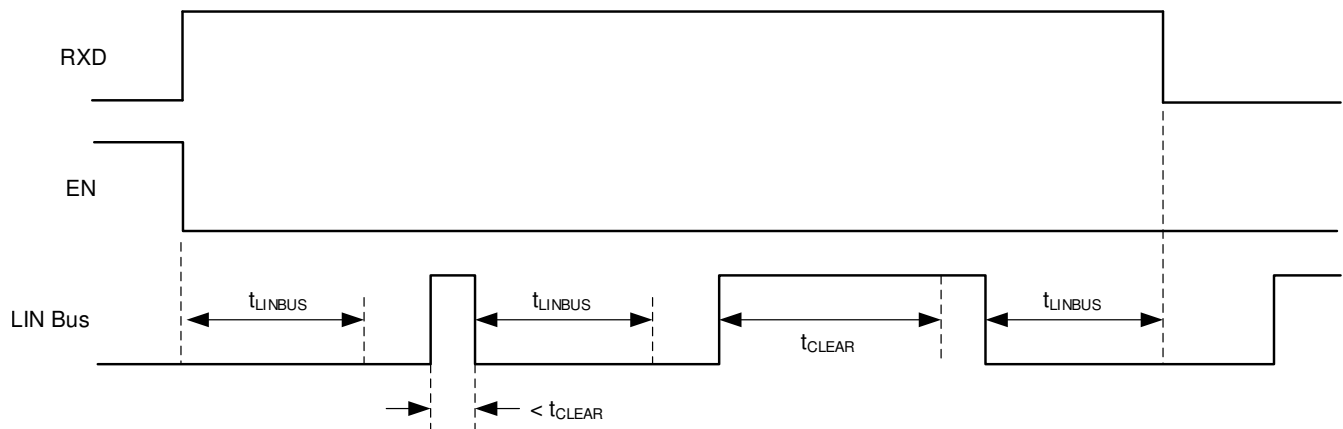


Figure 9-3. Bus Fault: Entering Sleep Mode with Bus Stuck Dominant Fault, Clearing, and Wakeup

9.3.10 Thermal Shutdown

The LIN transmitter is protected by current limiting circuitry; however, if the junction temperature of the device exceeds the thermal shutdown threshold, the device puts the LIN transmitter into the recessive state. Once the over-temperature fault condition has been removed and the junction temperature has cooled beyond the hysteresis temperature, the transmitter is re-enabled, assuming the device remained in the normal operation mode. During this fault, the transceiver remains in normal mode (assuming no change of state request on EN), the transmitter is in recessive state, the RXD pin reflects the LIN bus and LIN bus pull-up termination remains on.

9.3.11 Under Voltage on V_{SUP}

The TLIN1029A-Q1 contains a power-on reset circuit to avoid false bus messages during under voltage conditions when V_{SUP} is less than UV_{SUP} .

9.3.12 Unpowered Device and LIN Bus

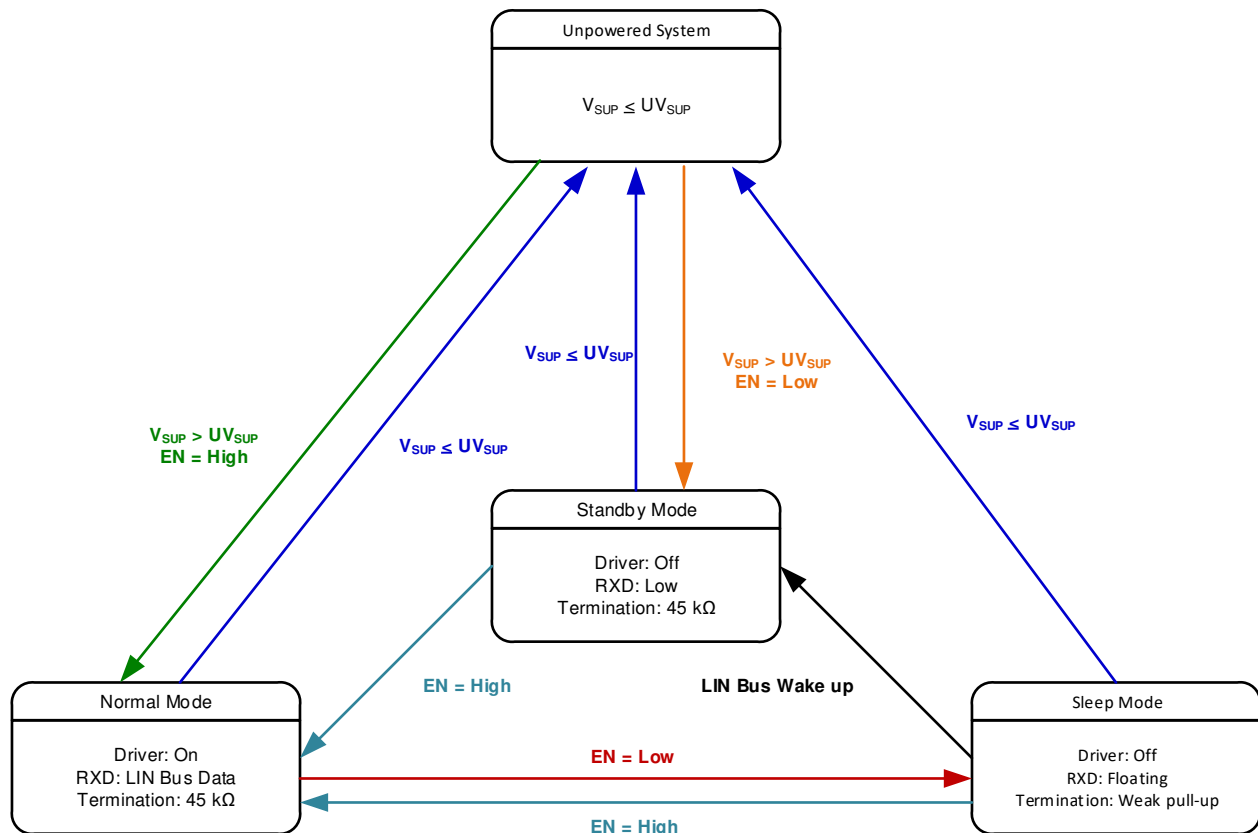
In automotive applications some LIN nodes in a system can be unpowered (ignition supplied) while others in the network remain powered by the battery. The TLIN1029A-Q1 has extremely low unpowered leakage current from the bus so an unpowered node does not affect the network or load it down.

9.4 Device Functional Modes

The TLIN1029A-Q1 has three functional modes of operation: normal, sleep, and standby. The next sections will describe these modes as well as how the device moves between the different modes. Figure 9-4 graphically shows the relationship while Table 9-1 shows the state of pins.

Table 9-1. Operating Modes

MODE	EN	RXD	LIN BUS TERMINATION	TRANSMITTER	COMMENT
Sleep	Low	Floating	Weak current pull-up	Off	
Standby	Low	Low	45 kΩ (typical)	Off	Wake-up event detected, waiting on MCU to set EN
Normal	High	LIN bus data	45 kΩ (typical)	On	LIN transmission up to 20 kbps



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Figure 9-4. Operating State Diagram

9.4.1 Normal Mode

If the EN pin is high at power up, the device will power up in normal mode. If the EN pin is low, it will power up in standby mode. The EN pin controls the mode of the device. In normal operational mode the receiver and transmitter are active and the LIN transmission up to the LIN specified maximum of 20 kbps is supported. The receiver detects the data stream on the LIN bus and outputs it on RXD for the LIN controller. A recessive signal on the LIN bus is a logic high and a dominant signal on the LIN bus is a logic low. The driver transmits input data from TXD to the LIN bus. Normal mode is entered as EN transitions high while the TLIN1029A-Q1 is in sleep or standby mode for $> t_{MODE_CHANGE}$ plus t_{NOMINT} .

9.4.2 Sleep Mode

Sleep mode is the power saving mode for the TLIN1029A-Q1. Sleep mode is only entered when the EN pin is low and from normal mode. Even with extremely low current consumption in this mode, the TLIN1029A-Q1 can still wake up from LIN bus through a wake-up signal or if EN is set high for $\geq t_{\text{MODE_CHANGE}}$. The LIN bus is filtered to prevent false wake up events. The wake-up events must be active for the respective time periods (t_{LINBUS}).

The sleep mode is entered by setting EN low for longer than $t_{\text{MODE_CHANGE}}$.

While the device is in sleep mode, the following conditions exist:

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short circuited to ground). However, the weak current pull-up is active to prevent false wake up events in case an external connection to the LIN bus is lost.
- The normal receiver is disabled.
- EN input and LIN wake up receiver are active.

9.4.3 Standby Mode

This mode is entered whenever a wake up event occurs through LIN bus while the device is in sleep mode. The LIN bus responder mode termination circuit is turned on when standby mode is entered. Standby mode is signaled through a low level on RXD. See the [Standby Mode Application Note](#) section for more application information.

When EN is set high for longer than $t_{\text{MODE_CHANGE}}$ while the device is in standby mode, the device returns to normal mode. The normal transmission paths from TXD to LIN bus and LIN bus to RXD are enabled.

9.4.4 Wake Up Events

There are two ways to wake up from sleep mode:

- Remote wake up initiated by the falling edge of a recessive (high) to dominant (low) state transition on LIN bus where the dominant state is held for t_{LINBUS} filter time. After this t_{LINBUS} filter time has been met and a rising edge on the LIN bus going from dominant state to recessive state initiates a remote wake up event, eliminating false wake ups from disturbances on the LIN bus or if the bus is shorted to ground.
- Local wake up through EN being set high for longer than $t_{\text{MODE_CHANGE}}$.

9.4.4.1 Wake Up Request (RXD)

When the TLIN1029A-Q1 encounters a wake up event from the LIN bus, RXD goes low and the device transitions to standby mode until EN is reasserted high and the device enters normal mode. Once the device enters normal mode, the RXD pin releases the wake up request signal and the RXD pin then reflects the receiver output from the LIN bus.

9.4.4.2 Mode Transitions

When the TLIN1029A-Q1 is transitioning from normal to sleep or standby modes the device needs the time $t_{\text{MODE_CHANGE}}$ to allow the change to fully propagate from the EN pin through the device into the new state. When transitioning from sleep or standby to normal mode the device needs $t_{\text{MODE_CHANGE}}$ plus t_{NOMINT} .

10 Application Information Disclaimer

Note

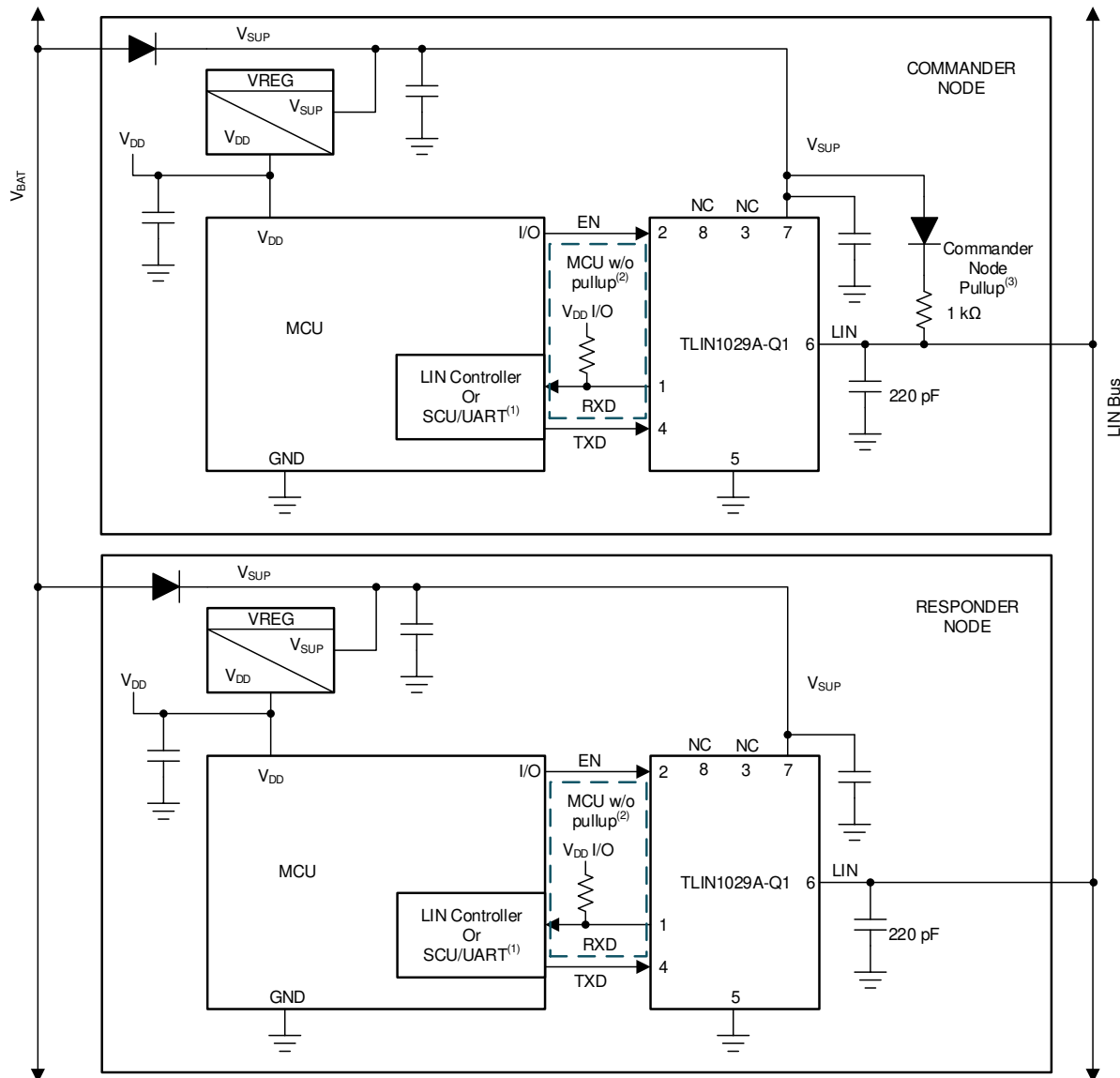
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The TLIN1029A-Q1 can be used as both a responder node device and a commander node device in a LIN network. The device comes with the ability to support both remote wake up request and local wake up request.

10.2 Typical Application

The device integrates a 45 k Ω pull-up resistor and series diode for responder node applications. For commander applications an external 1 k Ω pull-up resistor with series blocking diode can be used. [Figure 10-1](#) shows the device being used in both commander mode and responder mode applications.



- A. If RXD on MCU on LIN responder node has internal pullup; no external pullup resistor is needed.
- B. If RXD on MCU or LIN responder node does not have an internal pullup requires external pullup resistor.
- C. Commander node applications require an external 1 kΩ pullup resistor and serial diode.
- D. Decoupling capacitor values on V_{SUP} are system dependent but usually have 100 nF, 1 μ F and $\geq 10 \mu$ F.

Figure 10-1. Typical LIN Bus

10.2.1 Design Requirements

The RXD output structure is an open-drain output stage. This allows the TLIN1029A-Q1 to be used with 3.3-V and 5-V I/O processor. If the RXD pin of the processor does not have an integrated pull-up, an external pull-up resistor to the processor I/O supply voltage is required. The select external pull-up resistor value should be between 1 kΩ to 10 kΩ, depending on supply used (See I_{OL} in electrical characteristics). The V_{SUP} pin of the device should be decoupled with a 100-nF capacitor by placing it close to the V_{SUP} supply pin. The system should include additional decoupling on the V_{SUP} line as needed per the application requirements.

10.2.2 Detailed Design Procedures

10.2.2.1 Normal Mode Application Note

When using the TLIN1029A-Q1 in systems which are monitoring the RXD pin for a wake up request, special care should be taken during the mode transitions. The output of the RXD pin is indeterminate for the transition period between states as the receivers are switched. The application software should not look for an edge on the RXD pin indicating a wake up request until $t_{\text{MODE_CHANGE}}$. This is shown in [Figure 8-14](#)

10.2.2.2 Standby Mode Application Note

If the TLIN1029A-Q1 detects an under voltage on V_{SUP} the RXD pin transitions low and would signal to the software that the TLIN1029A-Q1 is in standby mode and should be returned to sleep mode for the lowest power state.

10.2.3 Application Curves

The below figures show the propagation delay from the TXD pin to the LIN pin for both dominant to recessive and recessive to dominant edges. Device was configured in commander mode with external pull-up resistor (1 k Ω) and 680 pF bus capacitance.

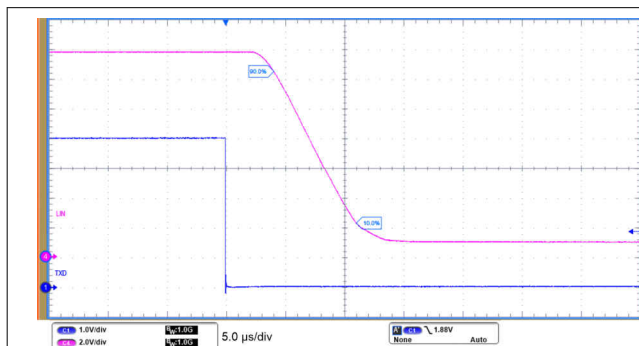


Figure 10-2. Recessive to Dominant Propagation

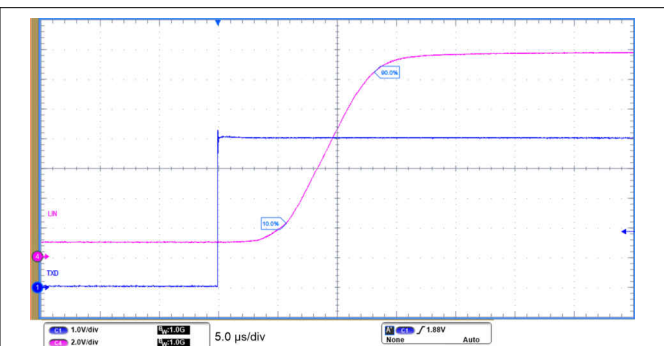


Figure 10-3. Dominant to Recessive Propagation

11 Power Supply Recommendations

The TLIN1029A-Q1 was designed to operate directly off a car battery, or any other DC supply ranging from 4 V to 36 V. A 100 nF decoupling capacitor should be placed as close to the V_{SUP} pin of the device as possible. It is good practice for some applications with noisier supplies to include 1 μF and 10 μF decoupling capacitor, as well.

12 Layout

In order for your PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design. Placement at the connector also prevents these noisy events from propagating further into the PCB and system.

12.1 Layout Guidelines

- **Pin 1 (RXD):** The pin is an open-drain output and requires an external pull-up resistor in the range of 1 k Ω to 10 k Ω to function properly. Note that the minimum value will depend on the VIO supply used. See I_{OL} in electrical specifications. If the microprocessor paired with the transceiver does not have an integrated pull-up, an external resistor should be placed between RXD and the regulated voltage supply for the microprocessor.
- **Pin 2 (EN):** EN is an input pin that is used to place the device in a low-power sleep mode. If this feature is not used the pin should be pulled high to the regulated voltage supply of the microprocessor through a series resistor between 1 k Ω and 10 k Ω . Additionally, a series resistor may be placed on the pin to limit current on the digital lines in the case of an over voltage fault.
- **Pin 3 (NC):** Not Connected.
- **Pin 4 (TXD):** The TXD pin is used to transmit the input signal from the microcontroller. A series resistor can be placed to limit the input current to the device in the case of an over-voltage on this pin. A capacitor to ground can be placed close to the input pin of the device to filter noise.
- **Pin 5 (GND):** This is the ground connection for the device. This pin should be tied to the ground plane through a short trace with the use of two vias to limit total return inductance.
- **Pin 6 (LIN):** This pin connects to the LIN bus. For responder mode applications a 220 pF capacitor to ground is implemented. For commander mode applications an additional series resistor and blocking diode should be placed between the LIN pin and the V_{SUP} pin. See [Figure 10-1](#).
- **Pin 7 (VSUP):** This is the supply pin for the device. A 100 nF decoupling capacitor should be placed as close to the device as possible.
- **Pin 8 (NC):** Not Connected.

Note

All ground and power connections should be made as short as possible and use at least two vias to minimize the total loop inductance.

12.2 Layout Example

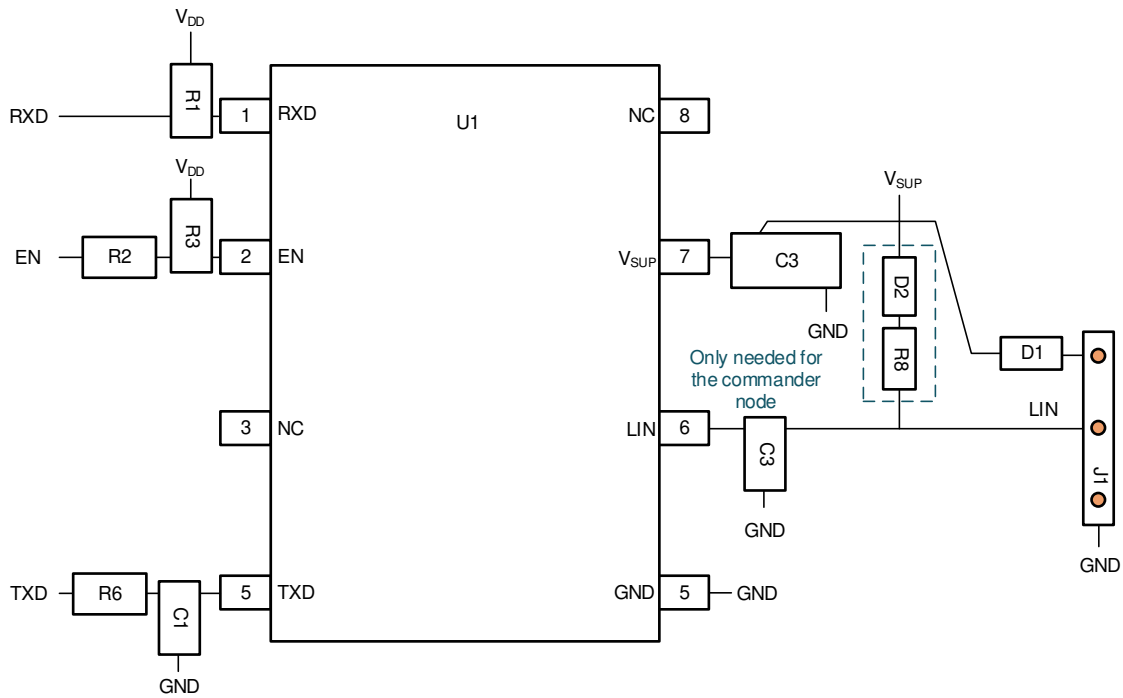


Figure 12-1. Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- LIN Standards:
 - ISO/DIS 17987-1.2: Road vehicles -- Local Interconnect Network (LIN) -- Part 1: General information and use case definition
 - ISO/DIS 17987-4.2: Road vehicles -- Local Interconnect Network (LIN) -- Part 4: Electrical Physical Layer (EPL) specification 12V/24V
 - SAEJ2602-1: LIN Network for Vehicle Applications
 - LIN Specifications LIN 2.0, LIN 2.1, LIN 2.2 and LIN 2.2A
- EMC requirements:
 - SAEJ2962-1: Communication Transceivers Qualification Requirements - LIN
 - ISO 10605: Road vehicles - Test methods for electrical disturbances from electrostatic discharge
 - ISO 11452-4:2011: Road vehicles - Component test methods for electrical disturbances from narrowband radiated electromagnetic energy - Part 4: Harness excitation methods
 - ISO 7637-1:2015: Road vehicles - Electrical disturbances from conduction and coupling - Part 1: Definitions and general considerations
 - ISO 7637-3: Road vehicles - Electrical disturbances from conduction and coupling - Part 3: Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines
 - IEC 62132-4:2006: Integrated circuits - Measurement of electromagnetic immunity 150 kHz to 1 GHz - Part 4: Direct RF power injection method
 - IEC 61000-4-2
 - IEC 61967-4
 - CISPR25
- Conformance Test requirements:
 - ISO/DIS 17987-7.2: Road vehicles -- Local Interconnect Network (LIN) -- Part 7: Electrical Physical Layer (EPL) conformance test specification
 - SAEJ2602-2: LIN Network for Vehicle Applications Conformance Test
-

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLIN1029ADRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(TL029, TL029A)	Samples
TLIN1029ADRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TL029A	Samples
TLIN1029AMDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(TL029, TL029A)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

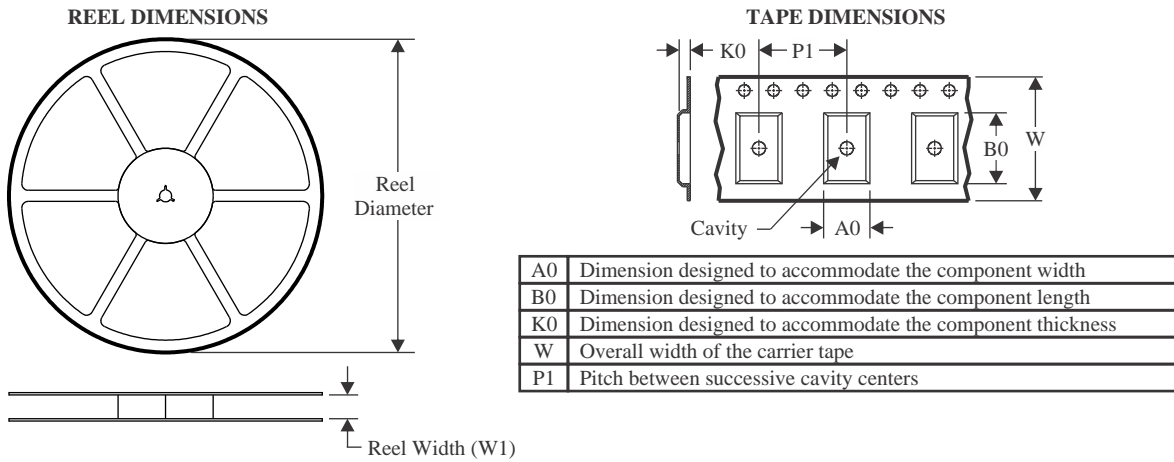
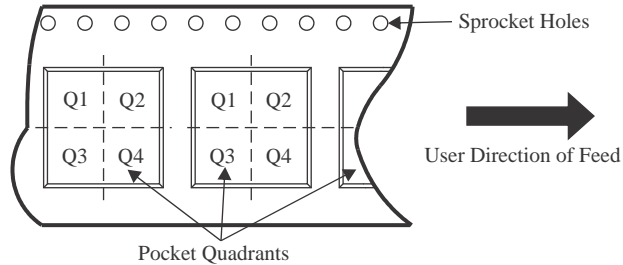
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLIN1029ADRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLIN1029ADRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLIN1029AMDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLIN1029ADRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TLIN1029ADRQ1	SOIC	D	8	2500	340.5	336.1	25.0
TLIN1029AMDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

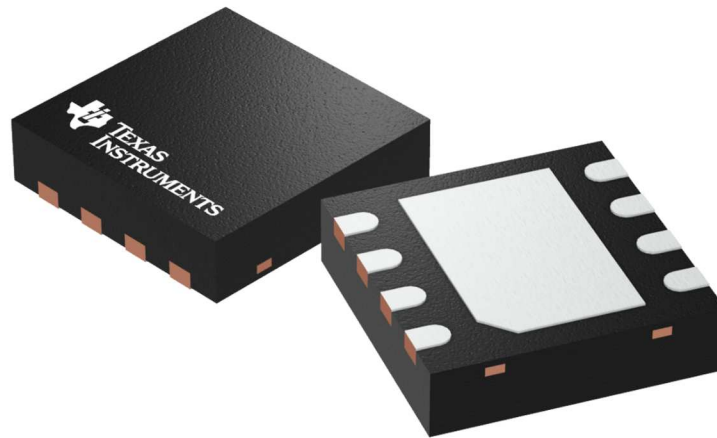
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRB 8

GENERIC PACKAGE VIEW

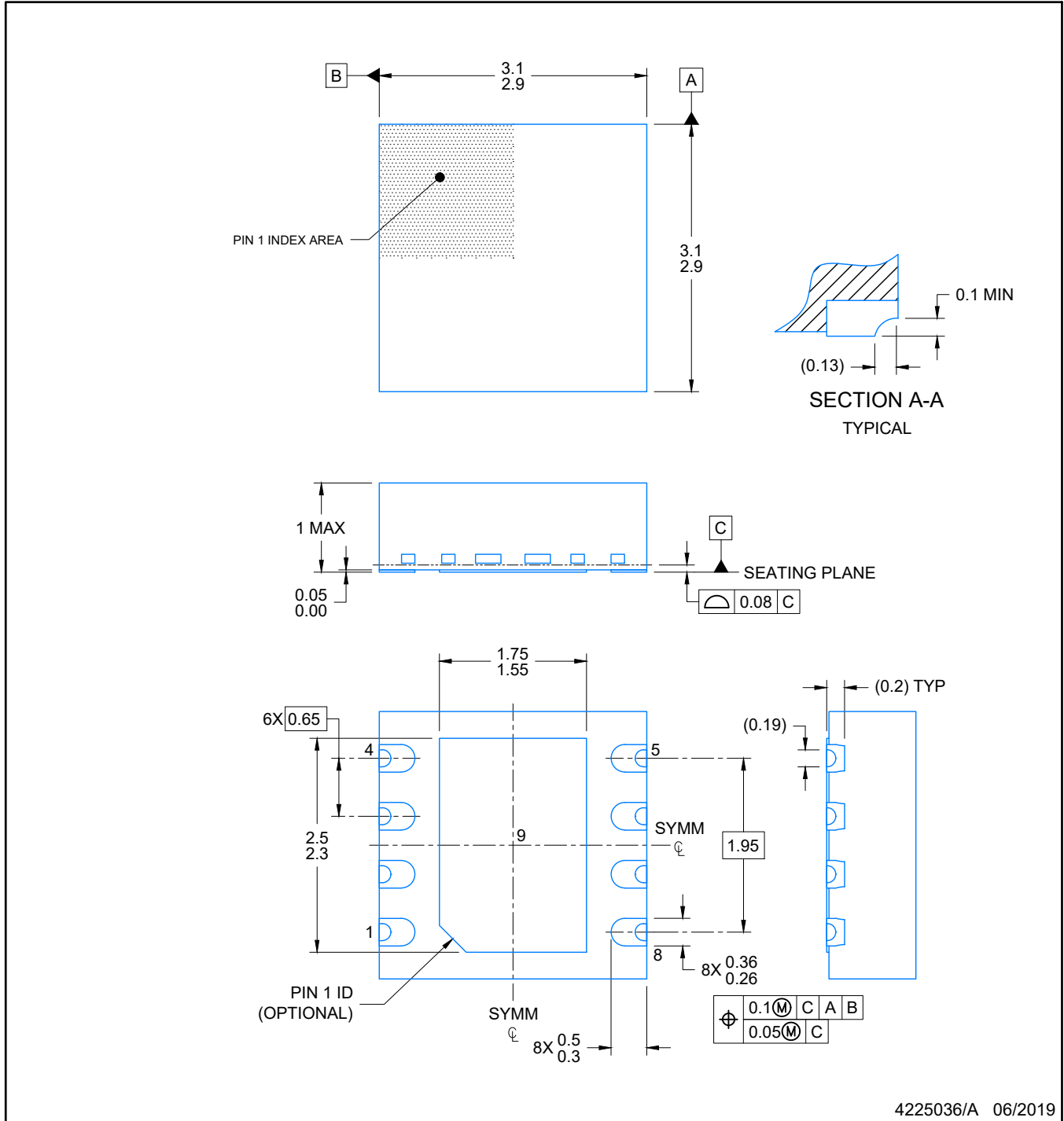
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

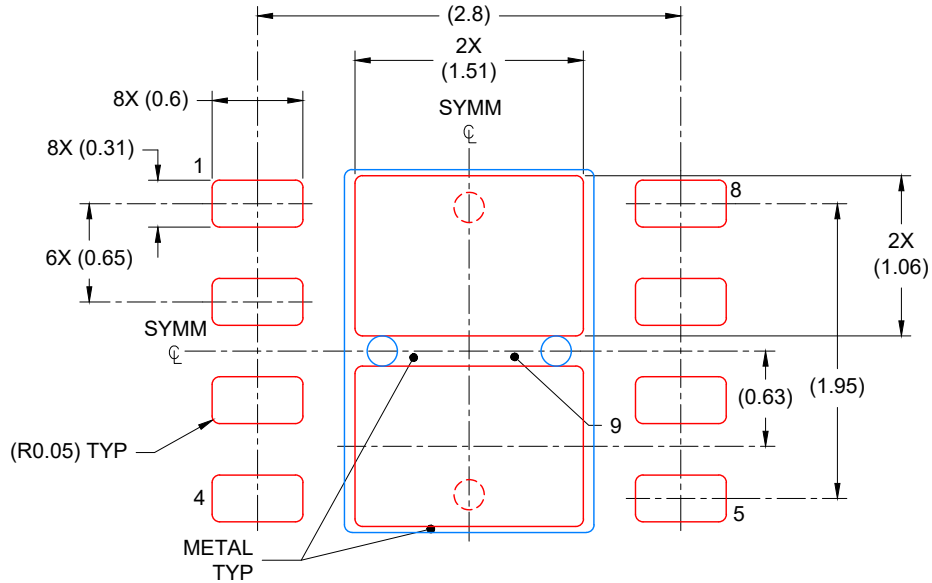
4203482/L



4225036/A 06/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 81% PRINTED COVERAGE BY AREA
 SCALE: 20X

4225036/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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