



**THE DATASHEET OF  
MAX40023ANT+**



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## MAX40023/MAX40024

## Low-Noise, Low-Power, Low-Bias-Current Amplifiers

### General Description

The MAX40023/MAX40024 are single and dual amplifiers optimized for power-sensitive applications that require low noise and very low-leakage input current (bias current).

The MAX40023/MAX40024 amplifiers consume less than 17 $\mu$ A (typ) of supply current per channel, but also feature incredibly low noise as low as 32nV/ $\sqrt{\text{Hz}}$ . The input bias current is <1pA at room temperature.

These amplifiers are available in a space-saving, 6-bump wafer-level package (WLP) with a 0.4mm bump pitch (single), 9-bump WLP (dual), 6-pin SOT23 (single), and 10-pin TDFN (dual). They are designed for use as a sensor interface in wearable medical and industrial sensor applications.

The MAX40023/MAX40024 amplifiers operate from a 1.6V to 3.6V power supply voltage and are specified over the -40°C to +125°C operating temperature range.

### Applications

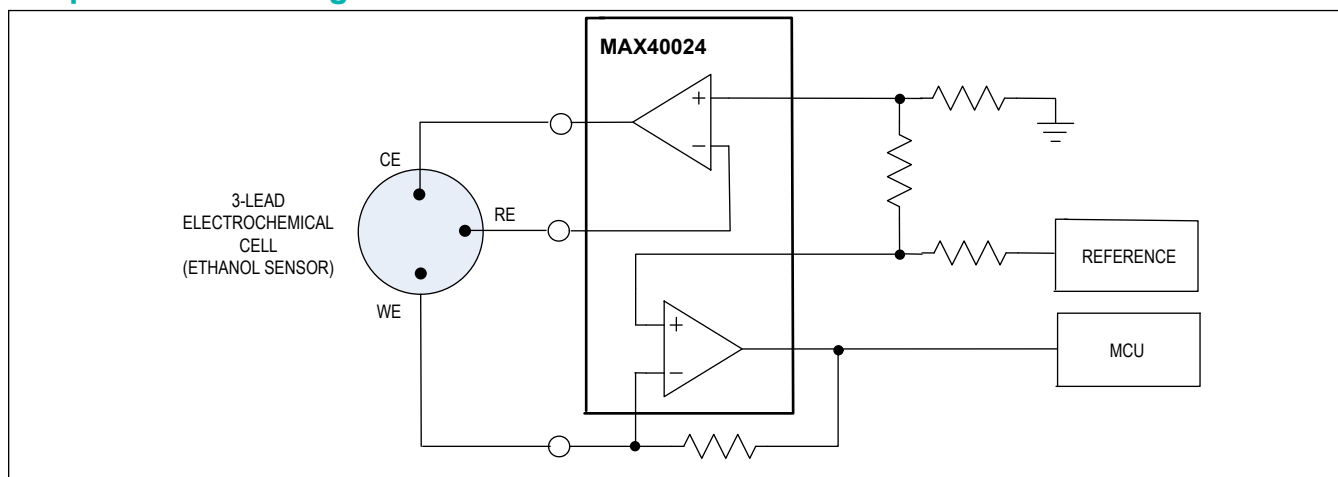
- Wearable Medical
- Industrial Sensors
- Battery-Powered Devices

### Benefits and Features

- Ultra-Low <1pA Input Bias Current
- Low 17 $\mu$ A Quiescent Current (per Op Amp)
- Low 32nV/ $\sqrt{\text{Hz}}$  Input-Voltage Noise
- Internal EMI Rejection
- Supply Voltage Range: 1.6V to 3.6V
- Power-Saving Shutdown Mode
- Available in 6-Bump WLP and 6-Pin SOT23 (Single) and 9-Bump WLP and 10-Pin TDFN (Dual)

*Ordering Information appears at end of data sheet.*

### Simplified Block Diagram



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**Absolute Maximum Ratings**

V <sub>DD</sub> to GND.....	-0.3V to +4V	Output Short-Circuit Duration to Either V <sub>DD</sub> or GND..	Continuous
IN+ to IN- .....	-0.3V to V <sub>DD</sub> + 0.3V	Operating Temperature Range .....	-40°C to 125°C
OUT to GND .....	-0.3V to V <sub>DD</sub> + 0.3V	Junction Temperature .....	+150°C
IN+, IN- to GND .....	-0.3V to V <sub>DD</sub> + 0.3V	Storage Temperature Range .....	-40°C to +150°C
Continuous Current into Any Input/Output Pin .....	10mA	Soldering Temperature (reflow) .....	+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

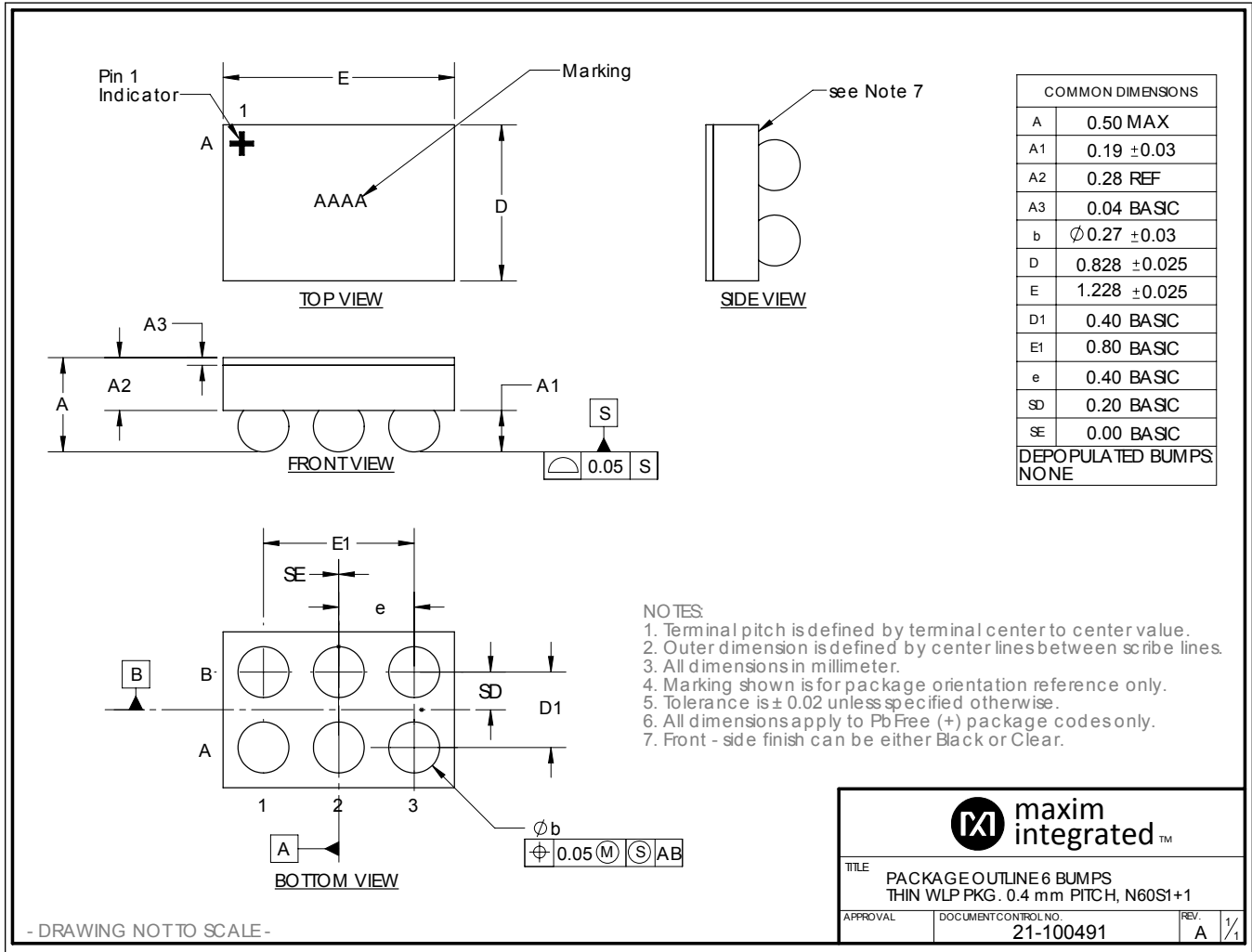
**Package Information**

**6 WLP**

Package Code	N60S1+1
Outline Number	<a href="#">21-100491</a>
Land Pattern Number	Refer to <a href="#">Application Note 1891</a>
<b>Thermal Resistance, Single-Layer Board:</b>	
Junction to Ambient (θ <sub>JA</sub> )	N/A
Junction to Case (θ <sub>JC</sub> )	N/A
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient (θ <sub>JA</sub> )	95.15°C/W
Junction to Case (θ <sub>JC</sub> )	N/A

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).



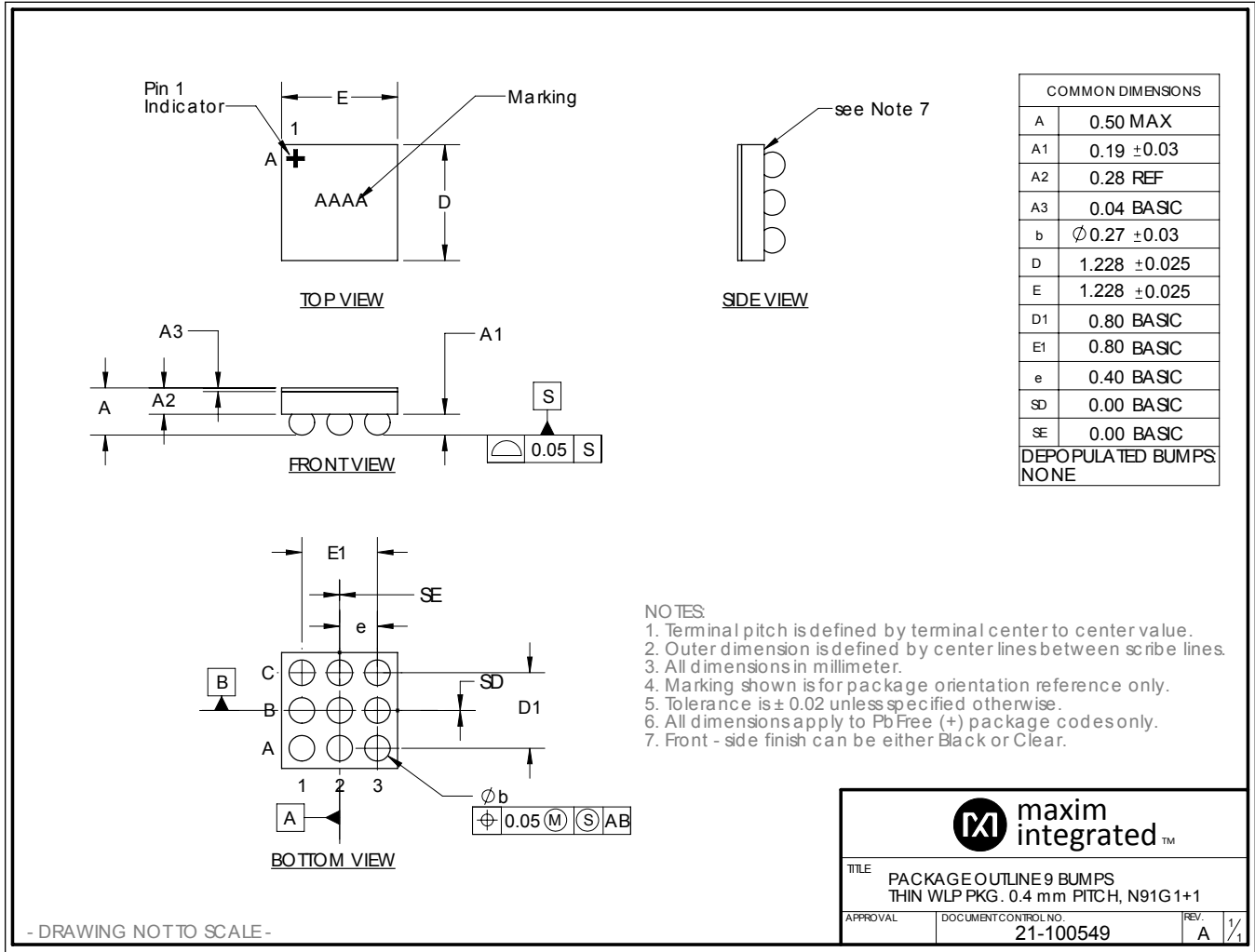
**9 WLP**

Package Code	N91G1+1
Outline Number	<a href="#">21-100549</a>
Land Pattern Number	Refer to <a href="#">Application Note 1891</a>
<b>Thermal Resistance, Single-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	N/A
Junction to Case ( $\theta_{JC}$ )	N/A
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	83.98°C/W
Junction to Case ( $\theta_{JC}$ )	N/A

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a

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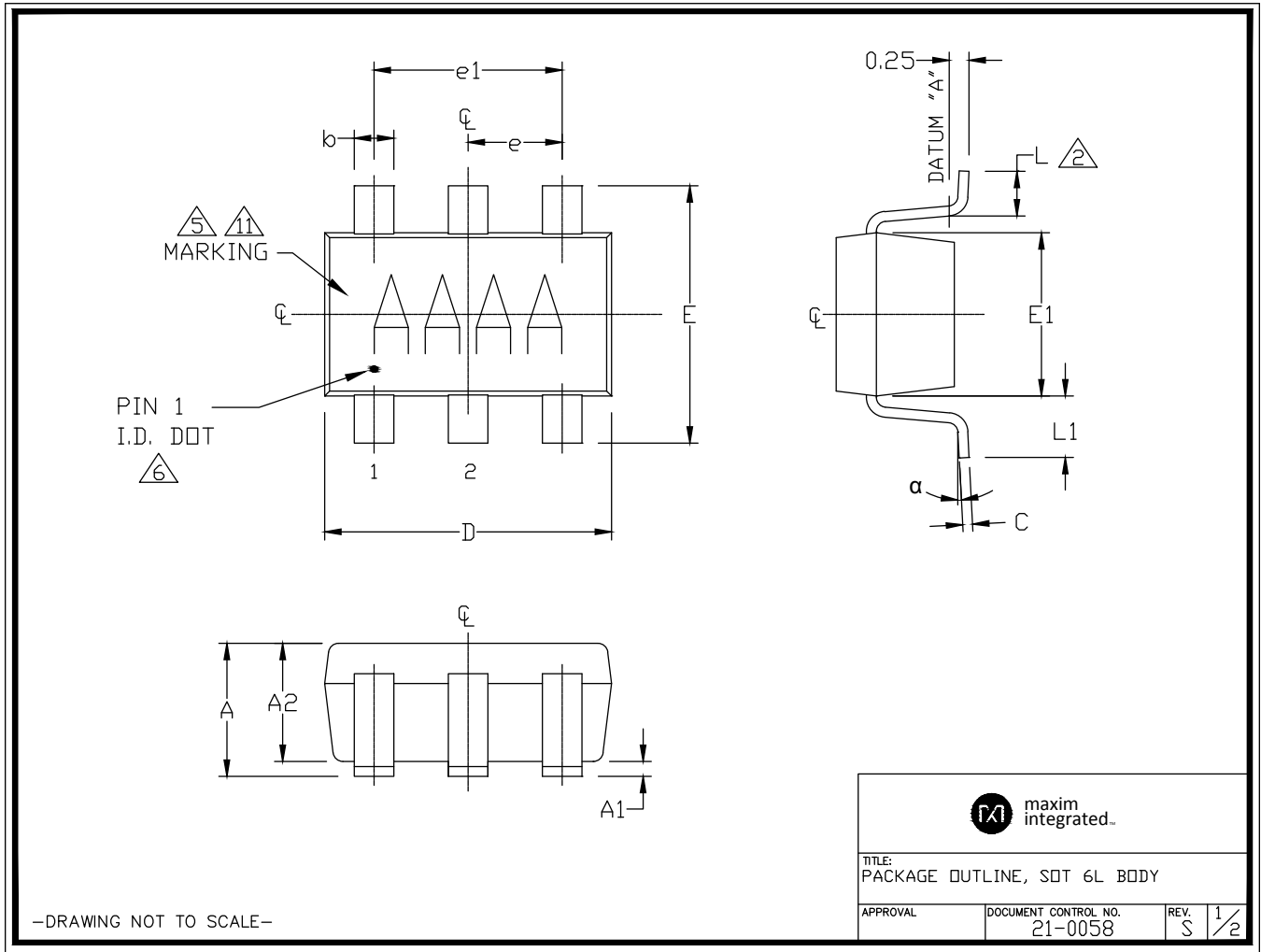
**6 SOT23**

Package Code	U6+1C
Outline Number	<a href="#">21-0058</a>
Land Pattern Number	<a href="#">90-0175</a>
<b>Thermal Resistance, Single-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	N/A
Junction to Case ( $\theta_{JC}$ )	N/A
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	230°C/W
Junction to Case ( $\theta_{JC}$ )	76°C/W





For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different

suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).



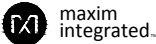
NOTES:

- ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHER SPECIFIED.
-  FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
- PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25mm.
- PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
-  PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT.
-  PIN 1 I.D. DOT IS  $\phi 0.3\text{mm}$  MIN. LOCATED ABOVE PIN 1.
- MEETS JEDEC MO178, VARIATION AB.
- SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
- LEAD TO BE COPLANAR WITHIN 0.1mm.
- NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
-  MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
- MATERIAL MUST BE COMPLIANT WITH MAXIM SPECIFICATION 10-0131 FOR SUBSTANCE CONTENT, MUST BE EU ROHS COMPLIANT WITHOUT EXEMPTION AND PB-FREE.
- ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

SYMBOL	MIN	NOMINAL	MAX
A	0.90	1.25	1.45
A1	0.00	0.05	0.15
A2	0.90	1.10	1.30
b	0.35	0.40	0.50
C	0.08	0.15	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.35	0.45	0.60
L1	0.60 REF.		
e1	1.90 BSC.		
e	0.95 BSC.		
a	0°	2.5°	10°

PKG CODES:  
 U6-1, U6-1A, U6-2, U6-4,  
 U6-4A, U6-5, U6-5A, U6CN-2,  
 U6F-6, U6SN-1, U6-8, U6-9,  
 U6-1C

\*\* U6-9 TO BE USED FOR RF50 PARTS ONLY WHICH USES A SI SPACER  
 \*\* U6-5 USES LOW STRESS MOLD COMPOUND



TITLE:  
 PACKAGE OUTLINE, SOT 6L BODY

APPROVAL	DOCUMENT CONTROL NO. 21-0058	REV. S	2/2
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-DRAWING NOT TO SCALE-

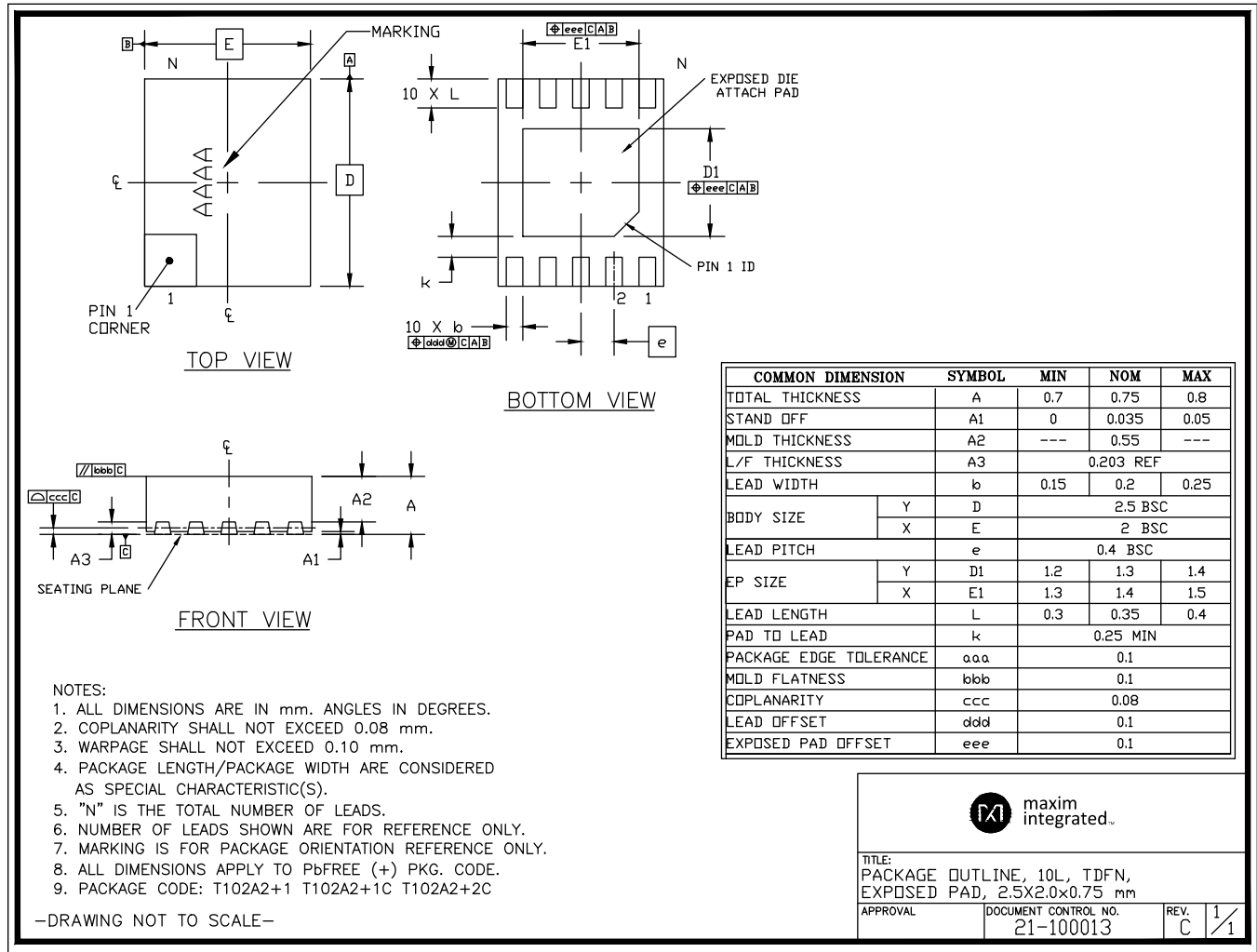
10 TDFN

Package Code	T102A2+2C
Outline Number	<a href="#">21-100013</a>
Land Pattern Number	<a href="#">90-100007</a>
<b>Thermal Resistance, Single-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	N/A
Junction to Case ( $\theta_{JC}$ )	N/A
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	102°C/W
Junction to Case ( $\theta_{JC}$ )	2.9°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a

four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).



### Electrical Characteristics

( $V_{DD} = 1.8V$ ,  $V_{CM} = V_{DD}/2$ ,  $R_{LOAD} = 10k\Omega$  to  $V_{DD}/2$ ,  $V_{SHDN} = V_{DD}$ ,  $T_A = -40^\circ$  to  $+125^\circ C$ . Typical values are at  $+25^\circ C$ , unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC SPECIFICATIONS</b>						
Input Offset Voltage	$V_{OS}$	$T_A = +25^\circ C$		100	400	$\mu V$
Input Offset Drift	$TCV_{OS}$			1	4	$\mu V/^\circ C$
Input Bias Current	$I_B$	(Note 2)	$0^\circ C \leq T_A \leq +50^\circ C$	0.1	5	pA
			$-40^\circ C \leq T_A \leq +85^\circ C$		30	
			$-40^\circ C \leq T_A \leq +125^\circ C$		550	
Input Offset Current	$I_{OS}$			0.5		pA

**Electrical Characteristics (continued)**

( $V_{DD} = 1.8V$ ,  $V_{CM} = V_{DD}/2$ ,  $R_{LOAD} = 10k\Omega$  to  $V_{DD}/2$ ,  $V_{SHDN} = V_{DD}$ ,  $T_A = -40^\circ$  to  $+125^\circ C$ . Typical values are at  $+25^\circ C$ , unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Resistance	$R_{IN}$	$0^\circ C \leq T_A \leq +50^\circ C$			15,000		G $\Omega$
Input Common-Mode Range	$V_{CM}$	Guaranteed by CMRR		-0.1		$V_{DD} + 0.1V$	V
Common-Mode Rejection Ratio	CMRR	$-40^\circ C \leq T_A \leq +125^\circ C$	$-0.1V \leq V_{CM} \leq V_{DD} + 0.1V$	75	100		dB
			$0V \leq V_{CM} \leq V_{DD} + 0.1V$	75	100		
		$0^\circ C \leq T_A \leq +50^\circ C$	$0V \leq V_{CM} \leq V_{DD} + 0.1V$	75	100		
Power Supply Rejection Ratio	PSRR	$V_{IN+} = V_{IN-} = 0V$		84	100		dB
Open-Loop Gain	$A_{OL}$	$150mV - GND \leq V_{OUT} \leq V_{DD} - 150mV$ , $R_{LOAD} = 10k\Omega$ to $V_{DD}/2$		90	110		dB
Output Voltage Swing High	$V_{OH}$	$V_{DD} - V_{OUT}$	$R_{LOAD} = 10k\Omega$ to $V_{DD}/2$			10	mV
Output Voltage Swing Low	$V_{OL}$	$V_{OUT} - GND$	$R_{LOAD} = 10k\Omega$ to $V_{DD}/2$			10	mV
Short-Circuit Current	$I_{SC}$				10		mA
<b>AC SPECIFICATIONS</b>							
Gain Bandwidth Product	GBW				80		kHz
Slew Rate	SR				0.02		V/ $\mu s$
Input Voltage-Noise Density	$V_N$	$f = 1kHz$			32		nV/ $\sqrt{Hz}$
Input Voltage Noise		0.1Hz to 10Hz			1.5		$\mu V_{P-P}$
Input Current-Noise Density	$I_N$	$f = 1kHz$			10		fA/ $\sqrt{Hz}$
EMI Rejection Ratio	EMIRR	$V_{RFpeak} = 100mV_P$ , $f = 400MHz$ , 900MHz, both IN+ and IN-			>70		dB
		$V_{RFpeak} = 100mV_P$ , $f = 1800MHz$ , 2400MHz, both IN+ and IN-			>110		
Phase Margin	PM	$C_{LOAD} = 20pF$			60		degrees
Capacitive Loading Stability					50		pF
Crosstalk		Buffer with $G = 1V/V$ , $IN1+ = 100mV_{P-P}$ , $f = 100Hz$ , test $V_{OUT2}$ (MAX40024 only)			90		dB
<b>POWER SUPPLY</b>							
Supply Voltage	$V_{DD}$	Guaranteed by PSRR, $-40^\circ C < T_A < +125^\circ C$		1.6		3.6	V
Supply Current	$I_{DD}$	$0^\circ C \leq T_A \leq +50^\circ C$			17	20	$\mu A$
		$-40^\circ C \leq T_A \leq +125^\circ C$				25	
Power-Up Time	$t_{ON}$	$V_{DD} = 0$ to $1.8V$ step, $A_V = 1V/V$	Measured at 90% of nominal final value		80		$\mu s$

**Electrical Characteristics (continued)**

( $V_{DD} = 1.8V$ ,  $V_{CM} = V_{DD}/2$ ,  $R_{LOAD} = 10k\Omega$  to  $V_{DD}/2$ ,  $V_{SHDN} = V_{DD}$ ,  $T_A = -40^\circ$  to  $+125^\circ C$ . Typical values are at  $+25^\circ C$ , unless otherwise noted. (*Note 1*))

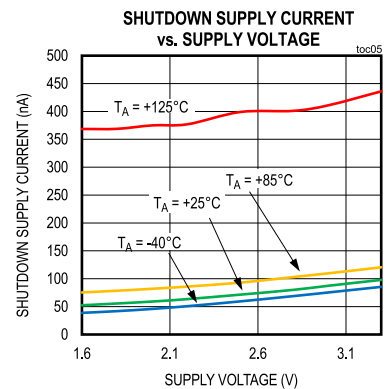
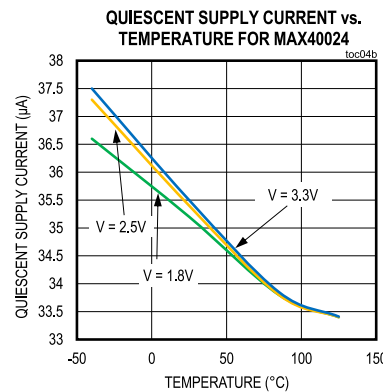
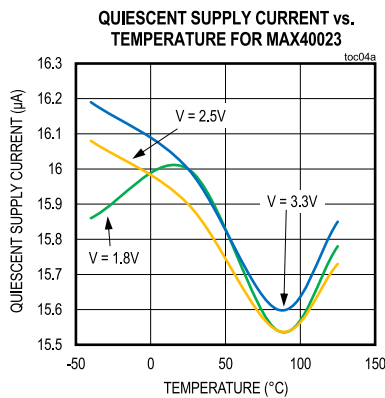
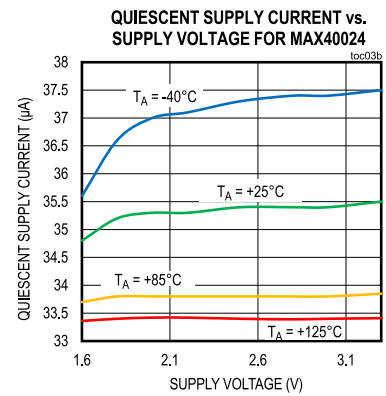
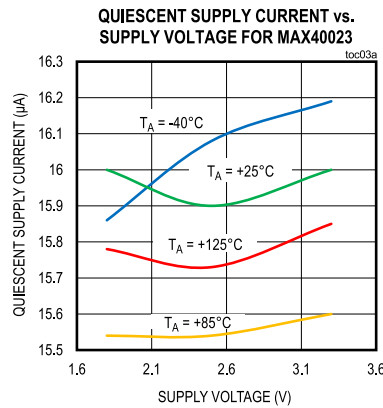
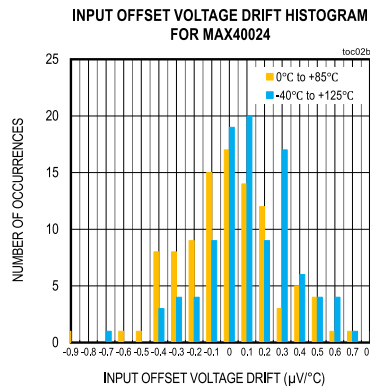
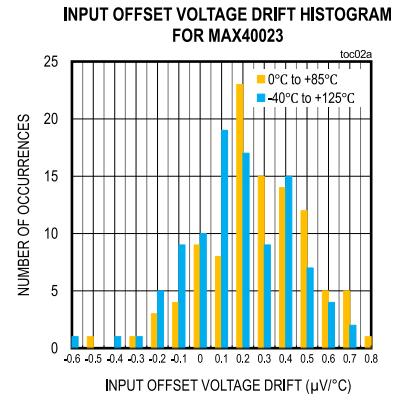
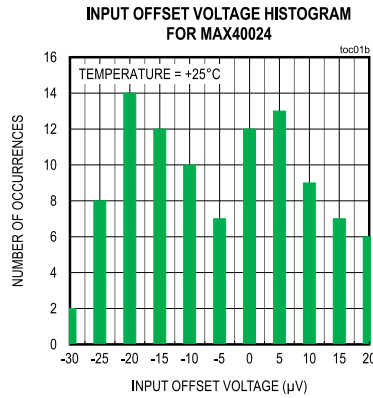
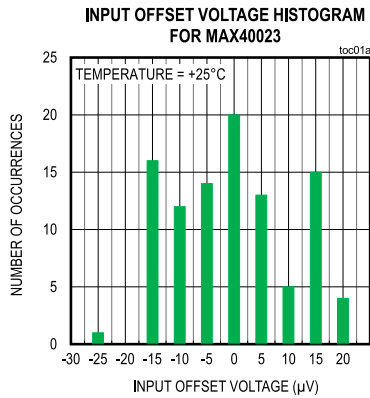
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Shutdown Supply Current	$I_{SHDN}$	$T_A = +25^\circ C$			55	100	nA
		$-40^\circ C \leq T_A \leq +125^\circ C$			55	400	
Turn-On Time from Shutdown	$t_{ONSD}$	$V_{DD} = 1.8V$ , $V_{SHDN} = 0$ to $1.8V$ step, $A_V = 1V/V$	Measured at 90% of final value		60		$\mu s$
<b>LOGIC INPUT DC CHARACTERISTICS</b>							
Input Low Level	$V_{IL}$	Active level				$0.3 \times V_{DD}$	V
Input High Level	$V_{IH}$			$0.7 \times V_{DD}$			V
Input Leakage Current	$I_L$					100	nA

**Note 1:** All devices are 100% production tested at  $T_A = +25^\circ C$ . Specifications over temperature are guaranteed by design.

**Note 2:** Not production tested, guaranteed by design and bench characterization.

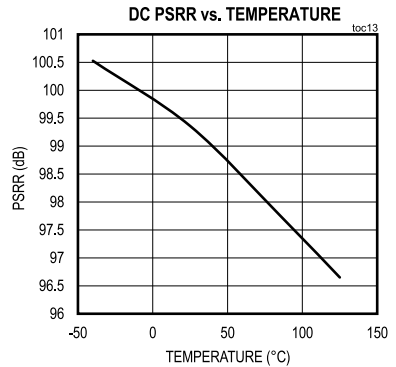
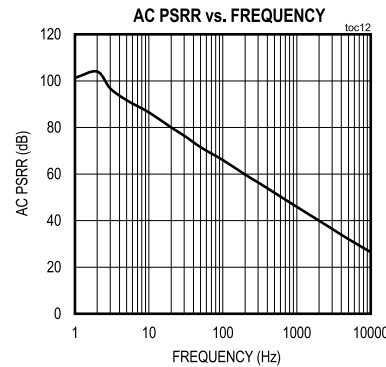
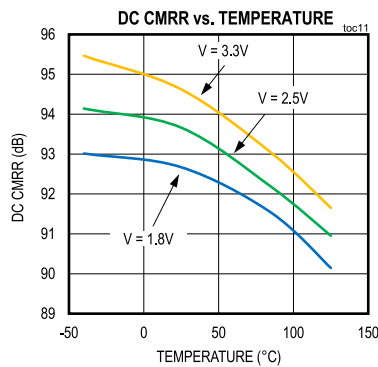
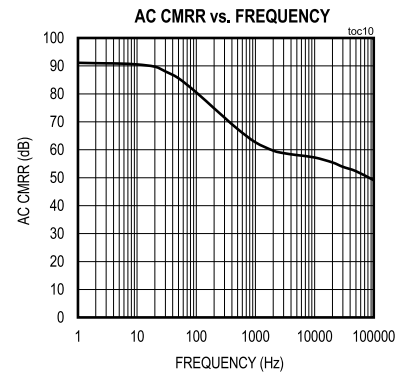
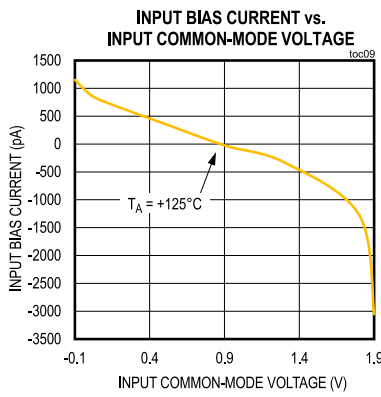
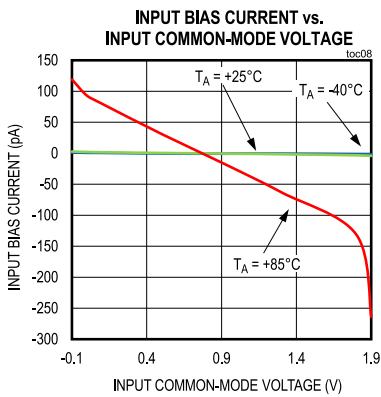
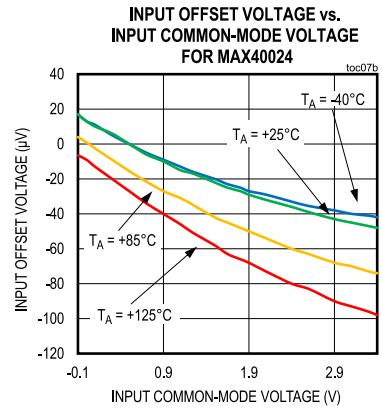
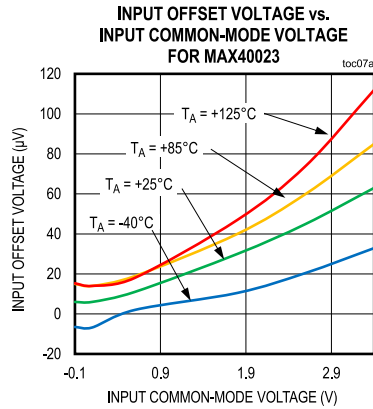
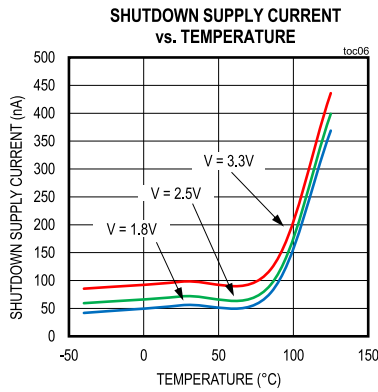
Typical Operating Characteristics

( $V_{DD} = +1.8V$ ,  $GND = 0V$ ,  $V_{IN-} = V_{IN+} = V_{DD}/2 = 0.9V$ ;  $V_{SHDN} = V_{DD}$ ,  $R_{LOAD} = 10k\Omega$  to  $V_{DD}/2$ ,  $T_A = +25^\circ C$ )



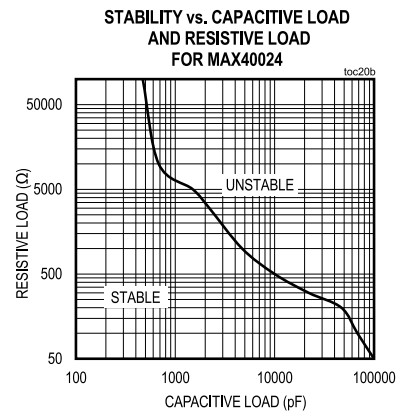
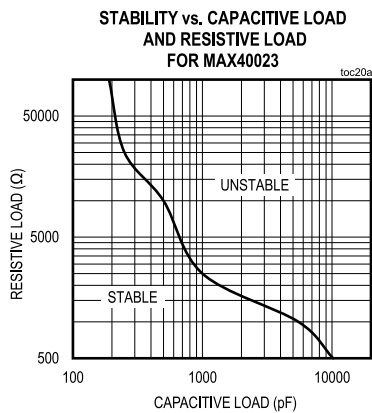
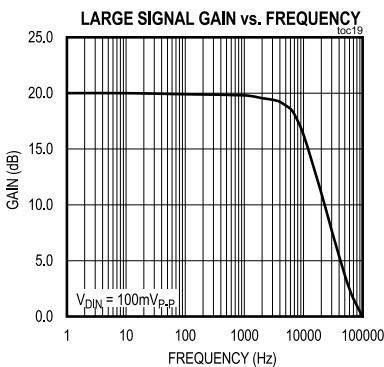
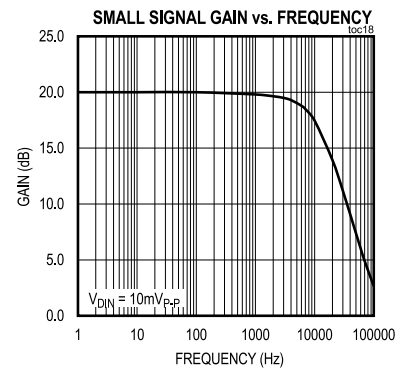
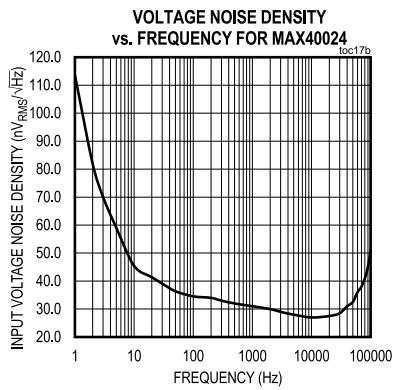
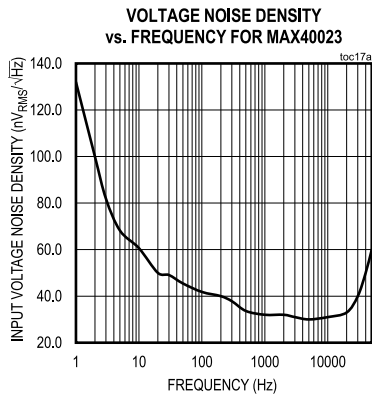
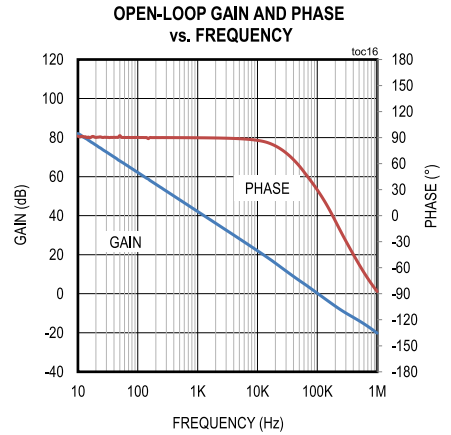
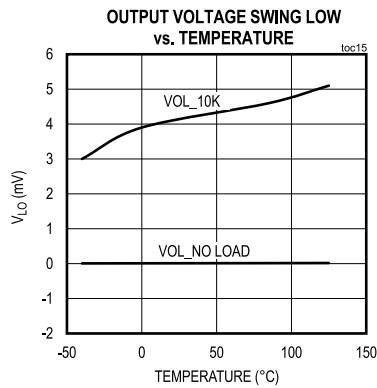
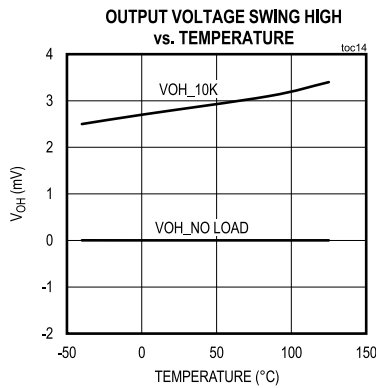
Typical Operating Characteristics (continued)

( $V_{DD} = +1.8V$ ,  $GND = 0V$ ,  $V_{IN-} = V_{IN+} = V_{DD}/2 = 0.9V$ ;  $V_{SHDN} = V_{DD}$ ,  $R_{LOAD} = 10k\Omega$  to  $V_{DD}/2$ ,  $T_A = +25^\circ C$ )



Typical Operating Characteristics (continued)

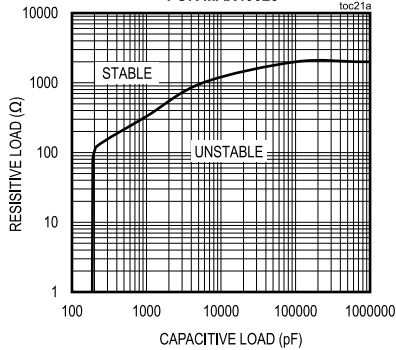
( $V_{DD} = +1.8V$ ,  $GND = 0V$ ,  $V_{IN-} = V_{IN+} = V_{DD}/2 = 0.9V$ ;  $V_{SHDN} = V_{DD}$ ,  $R_{LOAD} = 10k\Omega$  to  $V_{DD}/2$ ,  $T_A = +25^\circ C$ )



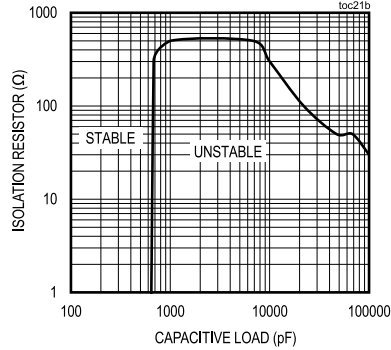
Typical Operating Characteristics (continued)

( $V_{DD} = +1.8V$ ,  $GND = 0V$ ,  $V_{IN-} = V_{IN+} = V_{DD}/2 = 0.9V$ ;  $V_{SHDN} = V_{DD}$ ,  $R_{LOAD} = 10k\Omega$  to  $V_{DD}/2$ ,  $T_A = +25^{\circ}C$ )

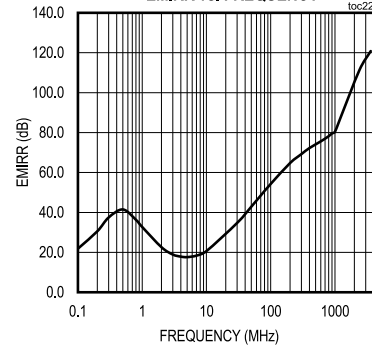
STABILITY vs. CAPACITIVE LOAD AND ISOLATION RESISTOR FOR MAX40023



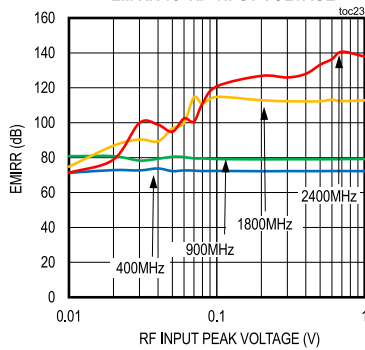
STABILITY vs. CAPACITIVE LOAD AND ISOLATION RESISTOR FOR MAX40024



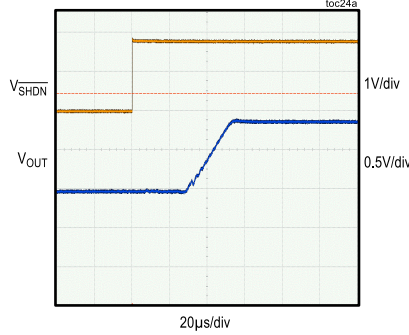
EMIRR vs. FREQUENCY



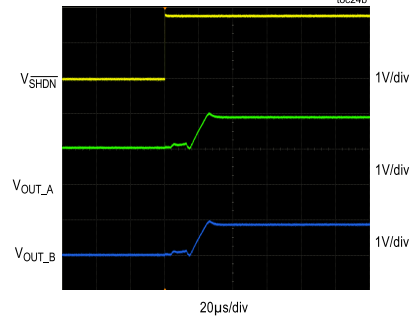
EMIRR vs. RF INPUT VOLTAGE



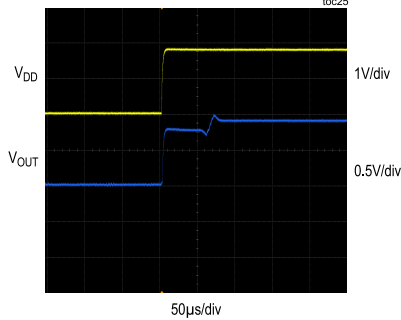
SHUTDOWN ENABLE RESPONSE FOR MAX40023



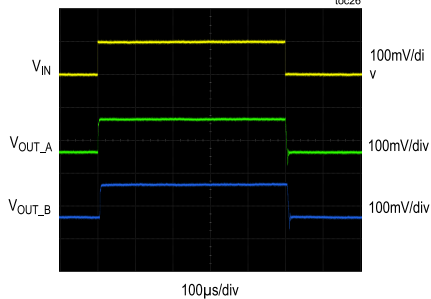
SHUTDOWN ENABLE RESPONSE FOR MAX40024



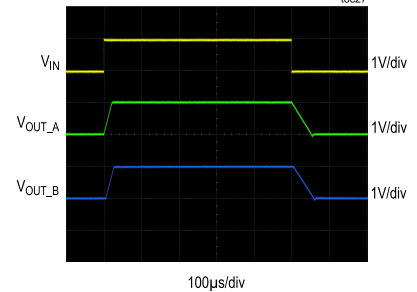
POWER-UP TIME



SMALL SIGNAL STEP RESPONSE vs. TIME

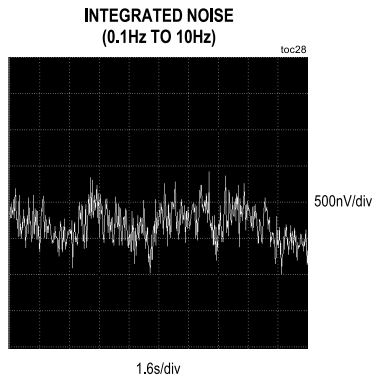


LARGE SIGNAL STEP RESPONSE vs. TIME



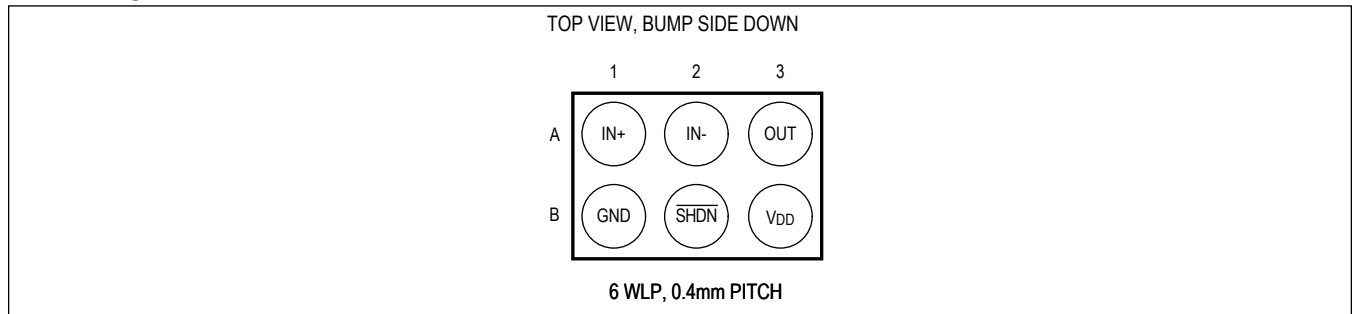
Typical Operating Characteristics (continued)

( $V_{DD} = +1.8V$ ,  $GND = 0V$ ,  $V_{IN-} = V_{IN+} = V_{DD}/2 = 0.9V$ ;  $\sqrt{SHDN} = V_{DD}$ ,  $R_{LOAD} = 10k\Omega$  to  $V_{DD}/2$ ,  $T_A = +25^{\circ}C$ )

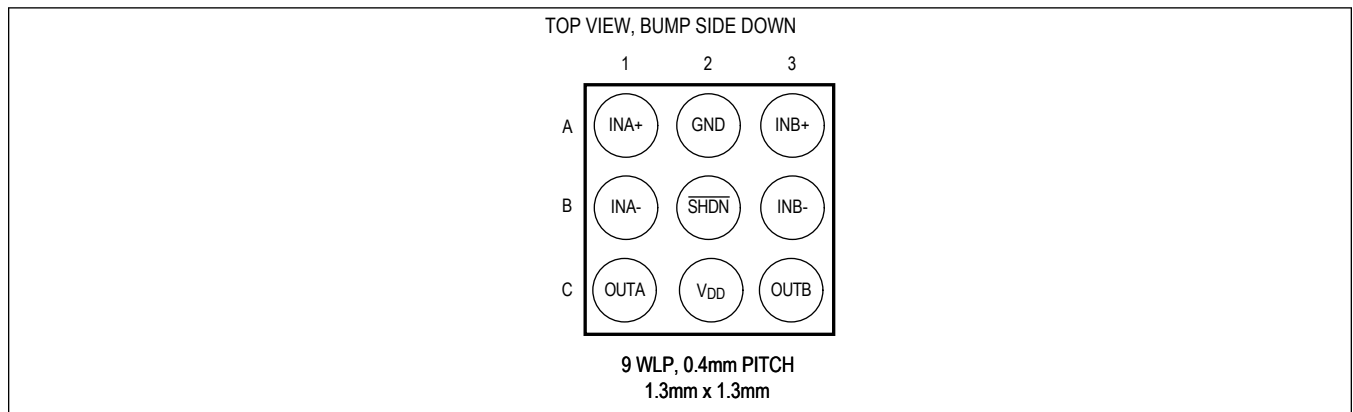


Pin Configurations

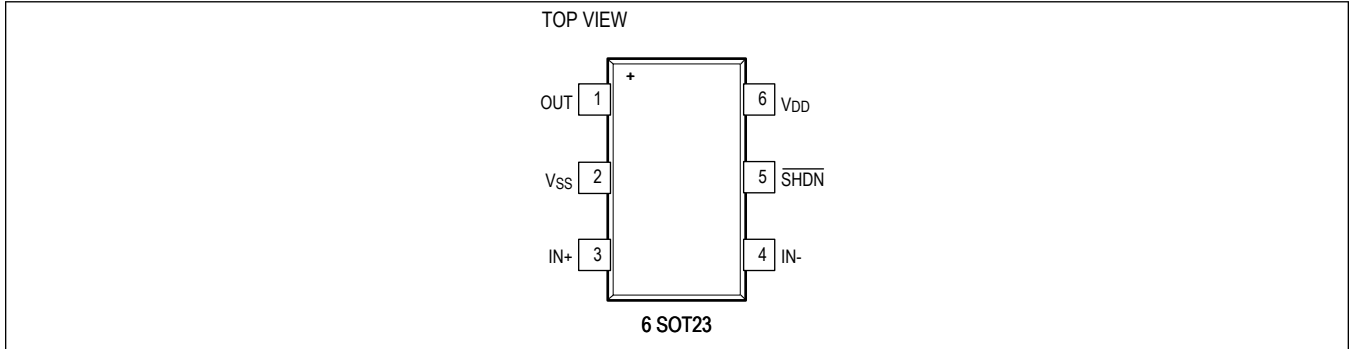
WLP Single



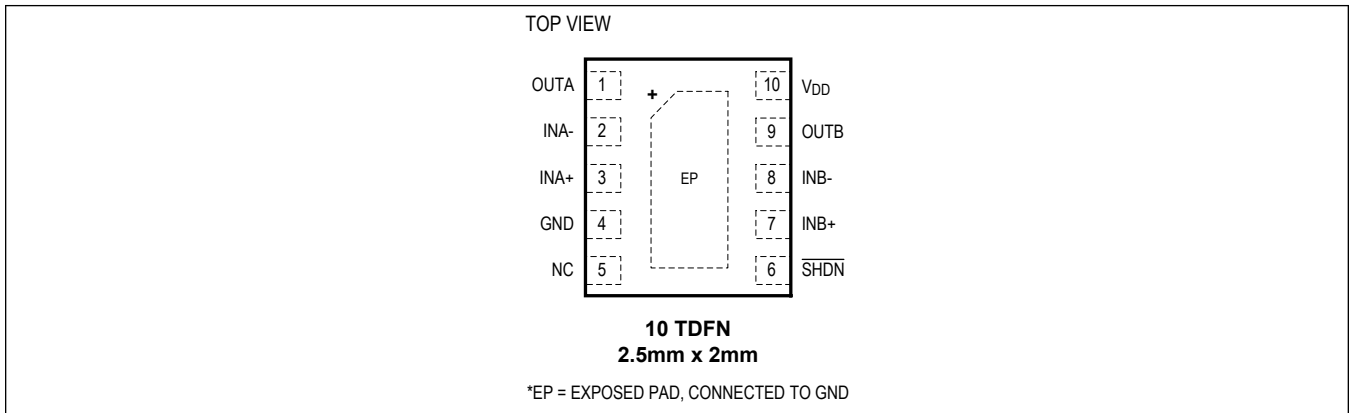
WLP Dual



**SOT23 Single**



**TDFN Dual**



**Pin Description**

PIN				NAME	FUNCTION
WLP Single	WLP Dual	SOT23 Single	TDFN Dual		
A1	A1, A3	3	3, 7	IN+	Noninverting Input
B1	A2	2	4	GND	Ground
A2	B1, B3	4	2, 8	IN-	Inverting Input
B3	C2	6	10	V <sub>DD</sub>	Positive Supply
A3	C1, C3	1	1, 9	OUT	Output
B2	B2	5	6	SHDN	Shutdown (active low)
—	—	—	5	NC	Do Not Connect
—	—	—	EP	EP	Exposed Pad. Connect to GND.

## Detailed Description

The MAX40023/MAX40024 feature a combination of low input current and voltage noise, rail-to-rail input and output voltage swing, low supply voltage, and low-power operation. High-impedance inputs on the MAX40023/MAX40024 make them ideal for use as transimpedance amplifiers and high-impedance sensor interface front-ends in medical and industrial applications. The MAX40023/MAX40024 can interface with small signals from either current sources or high-output impedance voltage sources. Applications include photodiode interfaces, pH sensors, capacitive pressure sensors, chemical analysis equipment, smoke detectors, and humidity sensors.

Low quiescent supply current and low power supply make the MAX40023/MAX40024 compatible with portable systems and applications that operate under tight power budgets. The MAX40023/MAX40024 achieve rail-to-rail performance at the input through the use of a low-noise charge pump. The rail-to-rail input maximizes the amplifier input dynamic range when it is operating at its minimum supply voltage of 1.6V. This also ensures a glitch-free, common-mode input-voltage range extending from the negative supply rail up to the positive supply rail, eliminating crossover distortion common to traditional n-channel/p-channel CMOS pair inputs. The charge pump requires no external components, and in most applications it is entirely transparent to the user. The operating frequency is well beyond the unity-gain frequency of the amplifier, avoiding aliasing or other signal integrity issues in sensitive applications.

## Shutdown Operation

The device features an active-low shutdown mode that reduces the quiescent current to a typical value of 55nA. In shutdown mode, the inputs and output are high impedance. This allows multiple devices to be multiplexed onto a single line without the use of external buffers. Pull SHDN high for normal operation. The shutdown high ( $V_{IH}$ ) and low ( $V_{IL}$ ) threshold voltages are designed for ease of integration with digital controls like microcontroller outputs. See the [Typical Operating Characteristics](#) for output voltage response to a shutdown disable signal.

## Low-Current, Low-Noise Input Stage

The MAX40023/MAX40024 feature a MOS-input stage with only 0.1pA (typ) of input bias current and a low  $32\text{nV}/\sqrt{\text{Hz}}$  (typ) input voltage-noise density. The low-frequency input voltage noise is a low  $1.5\mu\text{V}_{\text{P-P}}$  (typ). The MAX40023/MAX40024 feature rail-to-rail CMOS inputs; the input stage accepts a wide common-mode range, extending from (GND - 0.1V) to ( $V_{\text{CC}} + 0.1\text{V}$ ). The low input offset voltage, CMOS inputs, and absence of  $1/f$  noise allow for optimization of sensor interfaces, particularly for sensors that operate with low voltage and at a low frequency.

## Applications Information

### Overview

The MAX40023/MAX40024 low-power, low-noise, precision op amps are designed for applications that interface with sensors like the ones found in portable medical devices, such as ECGs and blood glucose meters, as well as industrial equipment.

### Power-Up Settling Time and Shutdown Enable Response

The MAX40023/MAX40024 typically require 80µs to power up. During this startup time, the output is indeterminate. The application circuit should allow for this initial delay. See the [Typical Operating Characteristics](#) for the Power-Up Time curve. The MAX40023/MAX40024 typically requires 60µs to respond from shutdown mode; the application circuit should allow for this delay.

### Power Supplies

The MAX40023/MAX40024 operate either with a single supply from +1.6V to +3.6V with respect to ground or with dual supplies from ±0.8V to ±1.8V. Bypass both supplies with a bypass capacitor to ground when used with dual supplies; bypass V<sub>DD</sub> with a bypass capacitor to ground when used with a single supply.

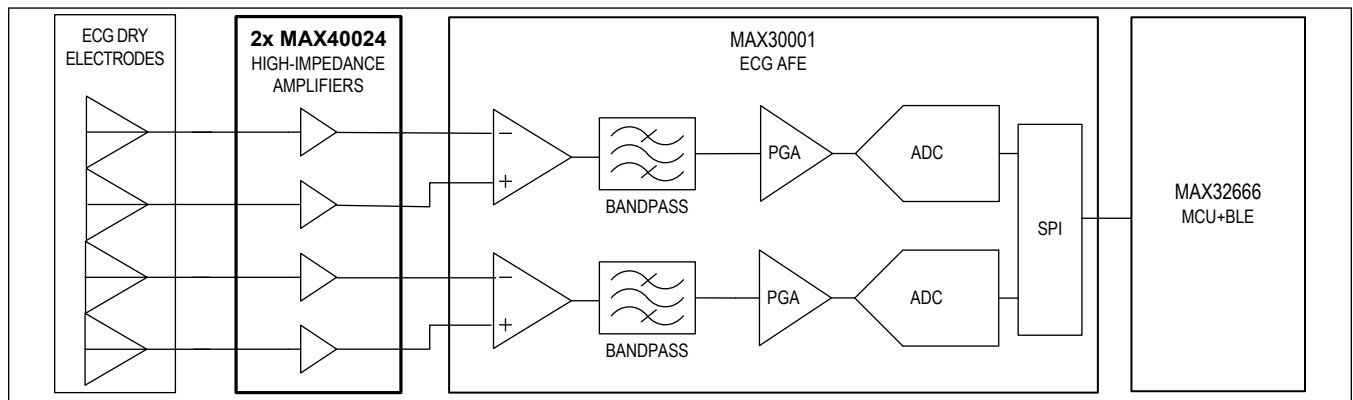
### Layout Techniques

A good layout is critical to obtaining high performance, especially when interfacing with high-impedance sensors. Use shielding techniques to guard against parasitic leakage paths. For transimpedance applications, for example, surround the inverting input and the traces connecting to it with a buffered version of its own voltage. A convenient source of this voltage is the noninverting input pin.

Take care to also decrease the amount of stray capacitance at the op amp's inputs to improve stability. To achieve this, minimize trace lengths and resistor leads by placing external components as close as possible to the package. If the sensor is inherently capacitive, or is connected to the amplifier through a long cable, use a low-value feedback capacitor to control high-frequency gain and peaking to stabilize the feedback loop.

## Typical Application Circuits

### Wearable ECG



## Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	TOP MARKING
MAX40023ANT+	-40°C to +125°C	6 WLP	+BH
MAX40023AUT+T*	-40°C to +125°C	6 SOT23	ACWH+
MAX40024ANL+	-40°C to +125°C	9 WLP	+AA
MAX40024ATB+T*	-40°C to +125°C	10 TDFN	+AZP

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

\*Future product—contact factory for availability.

**Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/21	Initial release	—

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at <https://www.maximintegrated.com/en/storefront/storefront.html>.

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