



**THE DATASHEET OF
AZC399-04S**





Features

- ESD Protect for 4 high-speed I/O channels
- Provide ESD protection for each channel to IEC 61000-4-2 (ESD) $\pm 27\text{kV}$ (air), $\pm 17\text{kV}$ (contact)
IEC 61000-4-4 (EFT) 60A (5/50ns)
IEC 61000-4-5 (Lightning) 10A (8/20 μs)
- For low operating voltage applications: 5V, 4.2V, 3.3V, 2.5V
- Low capacitance : 1.4pF typical
- Fast turn-on and Low clamping voltage
- Array of surge rated diodes with internal equivalent TVS diode
- Small package saves board space
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green Part**

Applications

- Video Graphics Cards
- USB2.0 Power and Data lines protection
- Notebook and PC Computers
- Monitors and Flat Panel Displays
- IEEE 1394 Firewire Ports
- SIM ports

Description

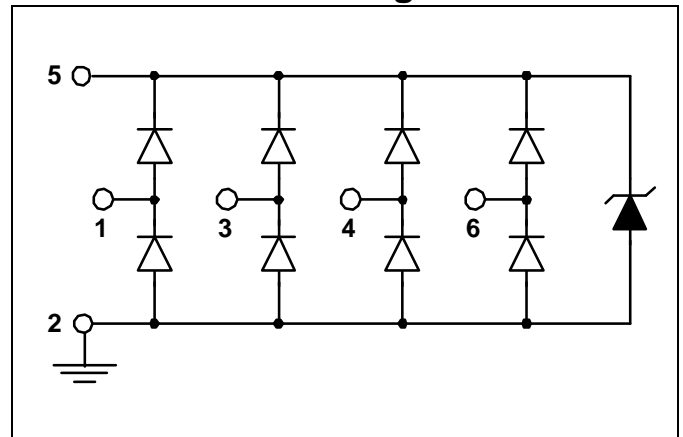
AZC399-04S is a high performance and low cost design which includes surge rated diode arrays to protect high speed data interfaces. The AZC399-04S family has been specifically designed to protect sensitive components, which are connected to data and transmission lines, from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Lightning.

AZC399-04S is a unique design which includes surge rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the power supply line or to the ground line. The internal unique design of clamping cell prevents over-voltage on the power line, protecting any downstream components.

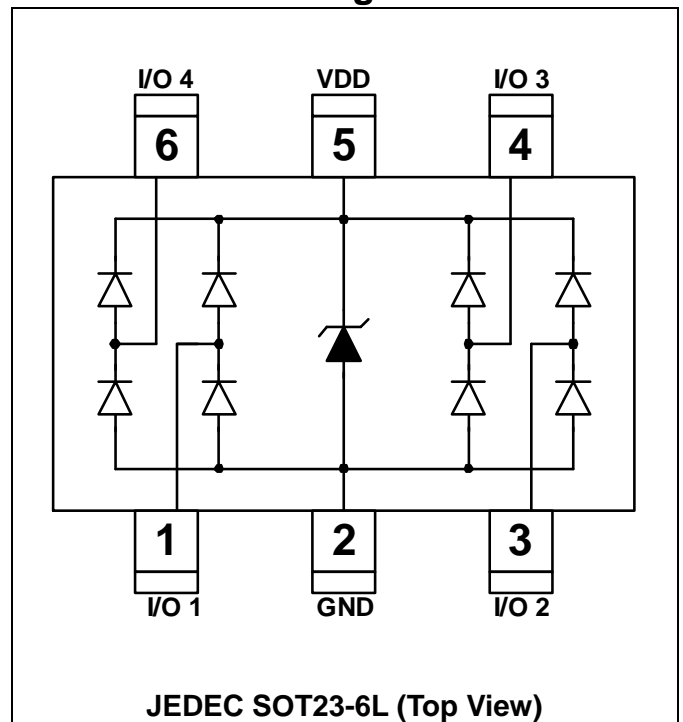
AZC399-04S may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

One AZC399-04S can be used to replace 4 BAV99 devices in a 5V application or a lower than 5V application.

Circuit Diagram



Pin Configuration



JEDEC SOT23-6L (Top View)

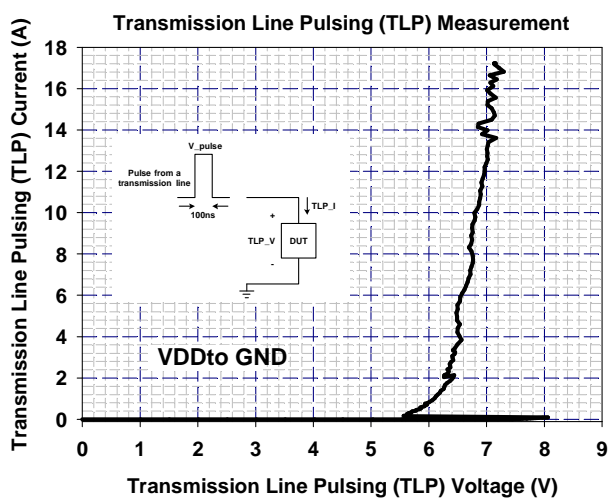
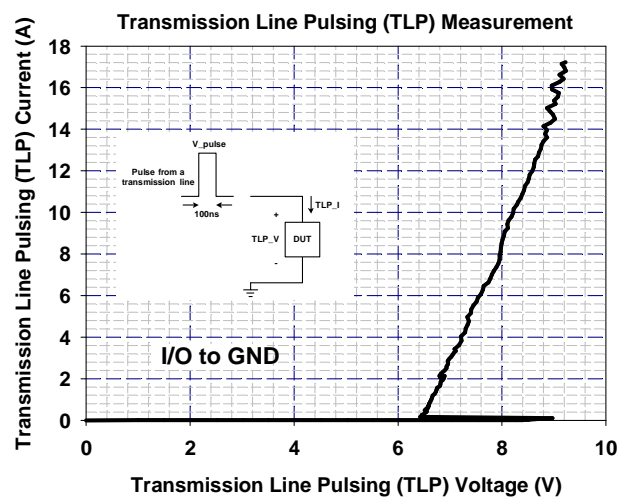
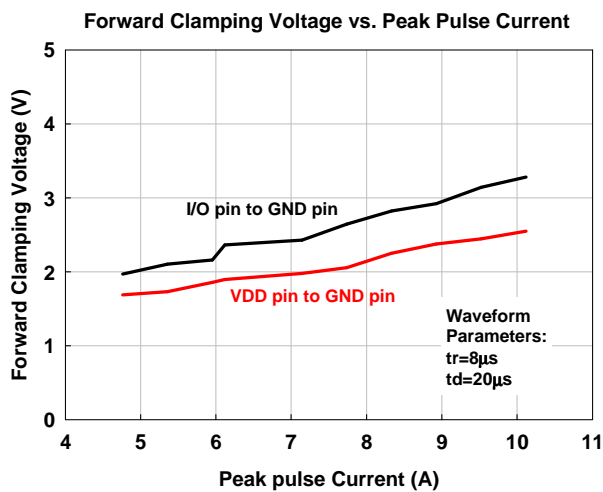
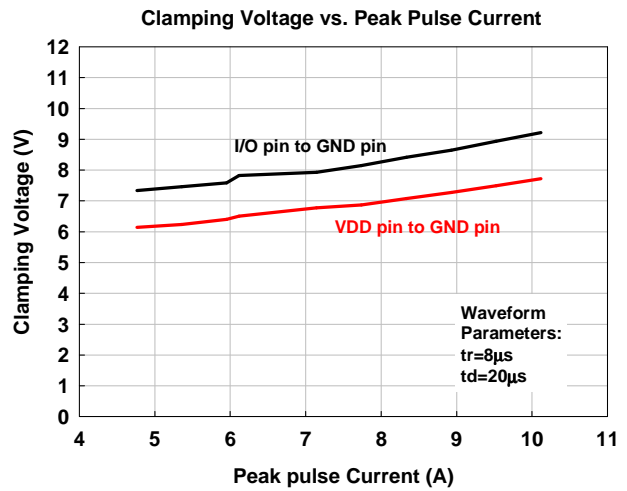
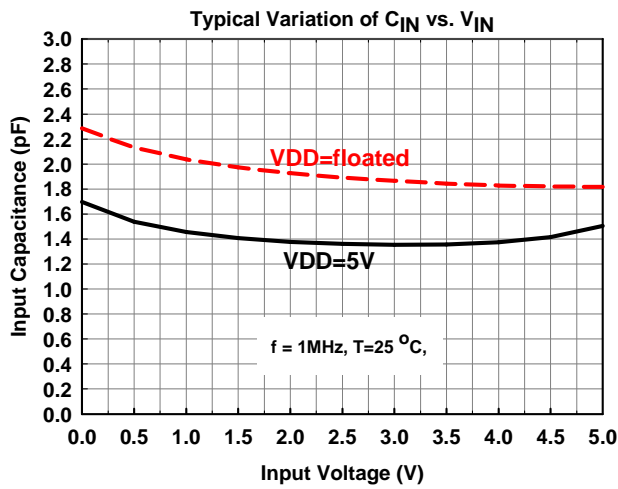


SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	PARAMETER	RATING	UNITS
Peak Pulse Current (tp =8/20μs)	I _{PP}	10	A
Operating Supply Voltage (VDD-GND)	V _{DC}	6	V
ESD per IEC 61000-4-2 (Air)	V _{ESD}	27	kV
ESD per IEC 61000-4-2 (Contact)		17	
Lead Soldering Temperature	T _{SOL}	260 (10 sec.)	°C
Operating Temperature	T _{OP}	-55 to +85	°C
Storage Temperature	T _{STO}	-55 to +150	°C
DC Voltage at any I/O pin	V _{IO}	(GND – 0.5) to (VDD + 0.5)	V

ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Stand-Off Voltage	V _{RWM}	Pin 5 to pin 2, T=25 °C			5	V
Reverse Leakage Current	I _{Leak}	V _{RWM} = 5V, T=25 °C, Pin 5 to pin 2			5	μA
Channel Leakage Current	I _{CH-Leak}	V _{Pin5} = 5V, V _{Pin2} = 0V, T=25 °C			1	μA
Reverse Breakdown Voltage	V _{BV}	I _{BV} = 1mA, T=25 °C, Pin 5 to Pin 2	6		9	V
Forward Voltage	V _F	I _F = 15mA, T=25 °C, Pin 2 to Pin 5		0.8	1.2	V
ESD Clamping Voltage –I/O	V _{clamp_io}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, Any Channel pin to Ground		11		V
ESD Clamping Voltage –VDD	V _{clamp_VDD}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, VDD pin to Ground		9		V
ESD Dynamic Turn on Resistance –I/O	R _{dynamic_io}	IEC 61000-4-2 0~+6kV, T=25 °C, Contact mode, any Channel pin to Ground		0.15		Ω
ESD Dynamic Turn on Resistance –VDD	R _{dynamic_VDD}	IEC 61000-4-2 0~+6kV, T=25 °C, Contact mode, VDD pin to Ground		0.05		Ω
Lightning Clamping Voltage	V _{lightning_io}	I _{PP} =5A, tp=8/20μs, T=25 °C Any Channel pin to Ground		7.5		V
Lightning Clamping Voltage	V _{lightning_VDD}	I _{PP} =5A, tp=8/20μs, T=25 °C VDD pin to Ground		6		V
Channel Input Capacitance -1	C _{IN-1}	V _{pin5} =5V, V _{pin2} =0V, V _{IN} =2.5V, f =1MHz, T=25 °C, Any Channel pin to Ground		1.4	1.8	pF
Channel Input Capacitance - 2	C _{IN-2}	V _{pin5} =floated, V _{pin2} =0V, V _{IN} =2.5V, f=1MHz, T=25°C, Any Channel pin to Ground		1.8	2.3	pF
Channel to Channel Input Capacitance -1	C _{CROSS-1}	V _{pin5} =5V, V _{pin2} =0V, V _{IN} =2.5V, f =1MHz, T=25 °C , Between Channel pins		0.15	0.2	pF
Channel to Channel Input Capacitance -2	C _{CROSS-2}	V _{pin5} =floated, V _{pin2} =0V, V _{IN} =2.5V, f =1MHz, T=25 °C, Between Channel pins		0.25	0.35	pF
Variation of Channel Input Capacitance -1	ΔC _{IN-1}	V _{pin5} =5V, V _{pin2} =0V, V _{IN} =2.5V, f =1MHz, T=25 °C , Channel_x pin to Ground - Channel_y pin to Ground		0.08	0.1	pF
Variation of Channel Input Capacitance -2	ΔC _{IN-2}	V _{pin5} =floated, V _{pin2} =0V, V _{IN} =2.5V, f =1MHz, T=25 °C , Channel_x pin to Ground - Channel_y pin to Ground		0.06	0.08	pF

Typical Characteristics



Applications Information

A. Design Considerations

The ESD protection scheme for system I/O connector is shown in the Fig. 1. In Fig. 1, the diodes D1 and D2 are general used to protect data line from ESD stress pulse. If the power-rail ESD clamping circuit is not placed between VDD and GND rails, the positive pulse ESD current (I_{ESD1}) will pass through the ESD current path1. Thus, the ESD clamping voltage V_{CL} of data line can be described as follow:

$$V_{CL} = \text{Fwd voltage drop of D1} + \text{supply voltage of VDD rail} + L_1 \times d(I_{ESD1})/dt + L_2 \times d(I_{ESD1})/dt$$

Where L_1 is the parasitic inductance of data line, and L_2 is the parasitic inductance of VDD rail.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30A in 1ns. Here $d(I_{ESD1})/dt$ can be approximated by $\Delta I_{ESD1}/\Delta t$, or $30/(1 \times 10^{-9})$. So

just 10nH of total parasitic inductance (L_1 and L_2 combined) will lead to over 300V increment in V_{CL} ! Besides, the ESD pulse current which is directed into the VDD rail may potentially damage any components that are attached to that rail. Moreover, it is common for the forward voltage drop of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. Of course, the discrete diode is also possible to be destroyed due to its power dissipation capability is exceeded.

The AZC399-04S has an integrated power-rail ESD clamped circuit between VDD and GND rails. It can successfully overcome previous disadvantages. During an ESD event, the positive ESD pulse current (I_{ESD2}) will be directed through the integrated power-rail ESD clamped circuit to GND rail (ESD current path2). The clamping voltage V_{CL} on the data line is small and protected IC will not be damaged because power-rail ESD clamped circuit offer a low impedance path to discharge ESD pulse current.

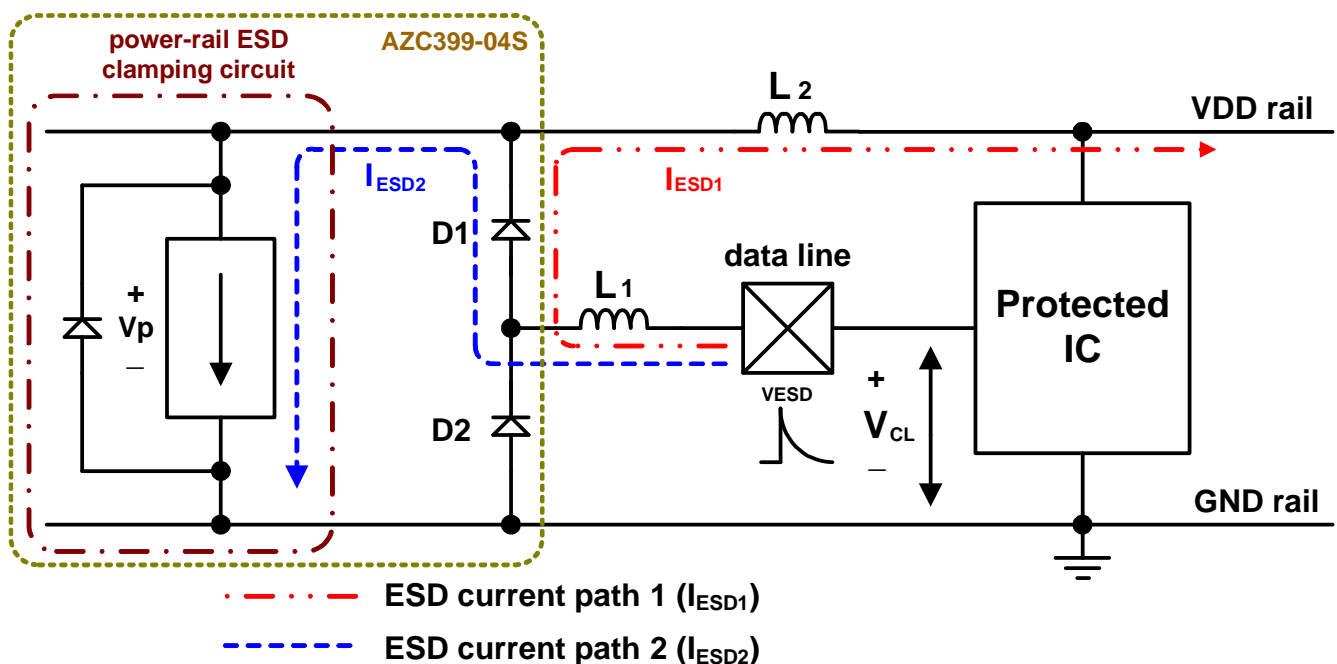


Fig. 1 Application of positive ESD pulse between data line and GND rail.

B. Device Connection

The AZC399-04S is designed to protect four data lines and power rails from transient over-voltage (such as ESD stress pulse). The device connection of AZC399-04S is shown in the Fig. 2. In Fig. 2, the four protected data lines are connected to the ESD protection pins (pin1, pin3, pin4, and pin6) of AZC399-04S. The ground pin (pin2) of AZC399-04S is a negative reference pin. This pin should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible. In addition, the power pin (pin 5) of AZC399-04S is a positive reference pin. This pin should directly connect to the VDD rail of PCB., then the VDD rail also can be protected by the power-rail ESD clamped circuit (not shown) of AZC399-04S.

AZC399-04S can provide protection for 4 I/O signal lines simultaneously. If the number of I/O signal lines is less than 4, the unused I/O pins can be simply left as NC pins.

In some cases, systems are not allowed to be reset or restart after the ESD stress directly applying at the I/O-port connector. Under this situation, in order to enhance the sustainable ESD Level, a 0.1 μ F chip capacitor can be added between the VDD and GND rails. The place of this chip capacitor should be as close as possible to the AZC399-04S.

In some cases, there isn't power rail presented on the PCB. Under this situation, the power pin (pin 5) of AZC399-04S can be left as floated. The protection will not be affected, only the load capacitance of I/O pins will be slightly increased. Fig. 3 shows the detail connection.

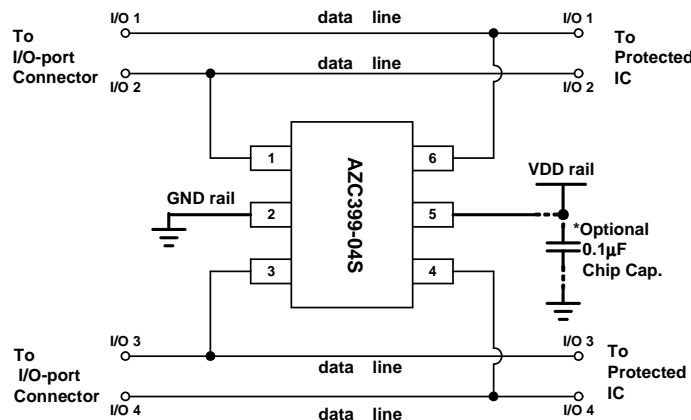


Fig. 2 Data lines and power rails connection of AZC399-04S.

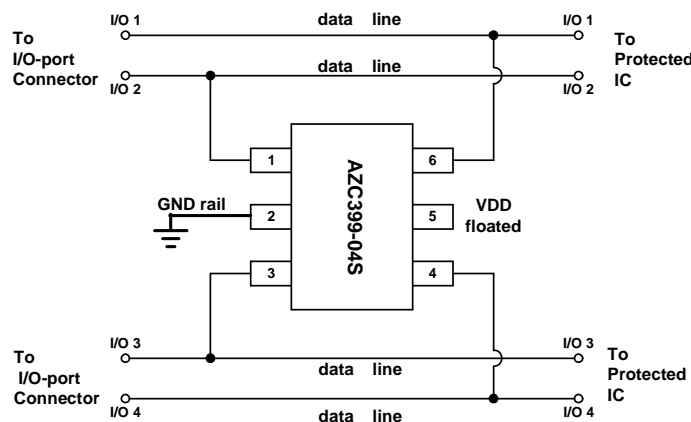


Fig. 3 Data lines and power rails connection of AZC399-04S. VDD pin is left as floating when no power rail presented on the PCB.



2. Audio Interface ESD Protection

For the audio interface, the Right/Left channel and TMC terminals should be protected from the ESD stress. The AZC399-04S can be used for the audio interface ESD protection. The ESD protection scheme for audio interface is shown in the Fig. 4. In the Fig. 4, the Right and Left channels of audio connector are connected to ESD protection pins (such as pin 1 and pin 6) of AZC399-04S. In addition, the TMC terminals of audio connector are also connected to ESD

protection pins (such as pin 3 and pin 4) of AZC399-04S. For the power pin (pin 5) of AZC399-04S, it should directly connect to the VDD power supply.

When ESD voltage pulse appears on the Right/Left channel or TMC terminals of audio connector, the ESD pulse current will be discharged by AZC399-04S. Therefore, the Right/Left channel and TMC terminals of audio chip are complementally protected with an AZC399-04S.

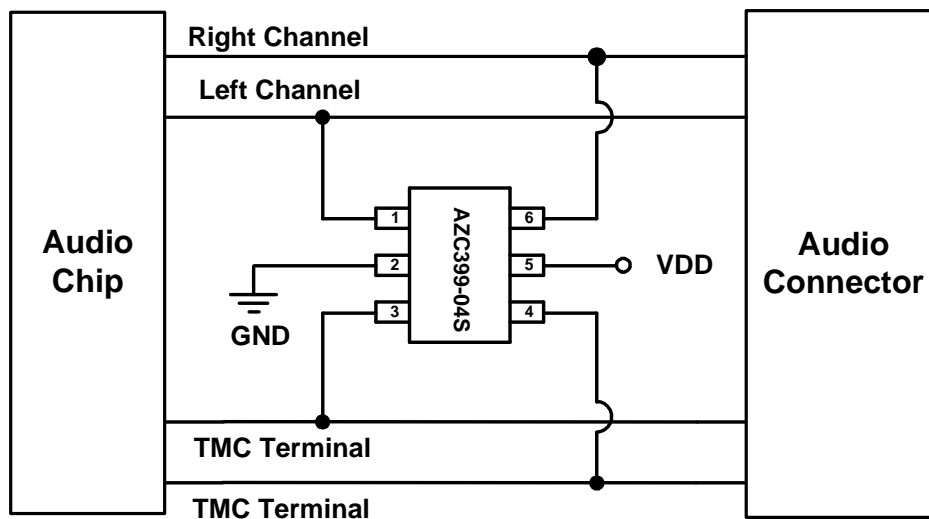


Fig. 4 ESD Protection scheme for audio interface by using AZC399-04S.



3. Video (VGA) Interface ESD Protection

AZC399-04S is designed for protecting high speed I/O ports from very high over-voltage caused by Electrostatic Discharging (ESD). Thus, a lot of kinds of high speed I/O ports can be the applications of AZC399-04S, especially, the VGA and DVI ports with the ESD spec. of contact-17kV, Air-27kV, Class-C above.

The VGA Input Port

The schematic of ESD protection design for a VGA input port on a display system is shown in Fig. 5. In most of VGA input circuit designs, there are always two power supplies, one is from the connector's DSUB-5V pin which potential comes

from another VGA output port, the other is from the own power supply circuit of the VGA input port, system 5V. The VDD pin of AZC399-04S is directly connected to the connector's DSUB-5V pin to block the ESD event which comes from the DSUB-5V pin.

The PCB layout example for the VGA Port

Fig. 6 shows the PCB layout example for a VGA port with two AZC399-04S being used. In order to get good signal quality, in this PCB example, the signal traces for R, G, and B signals are with 0.4mm width and are accompanied with GND traces, respectively.

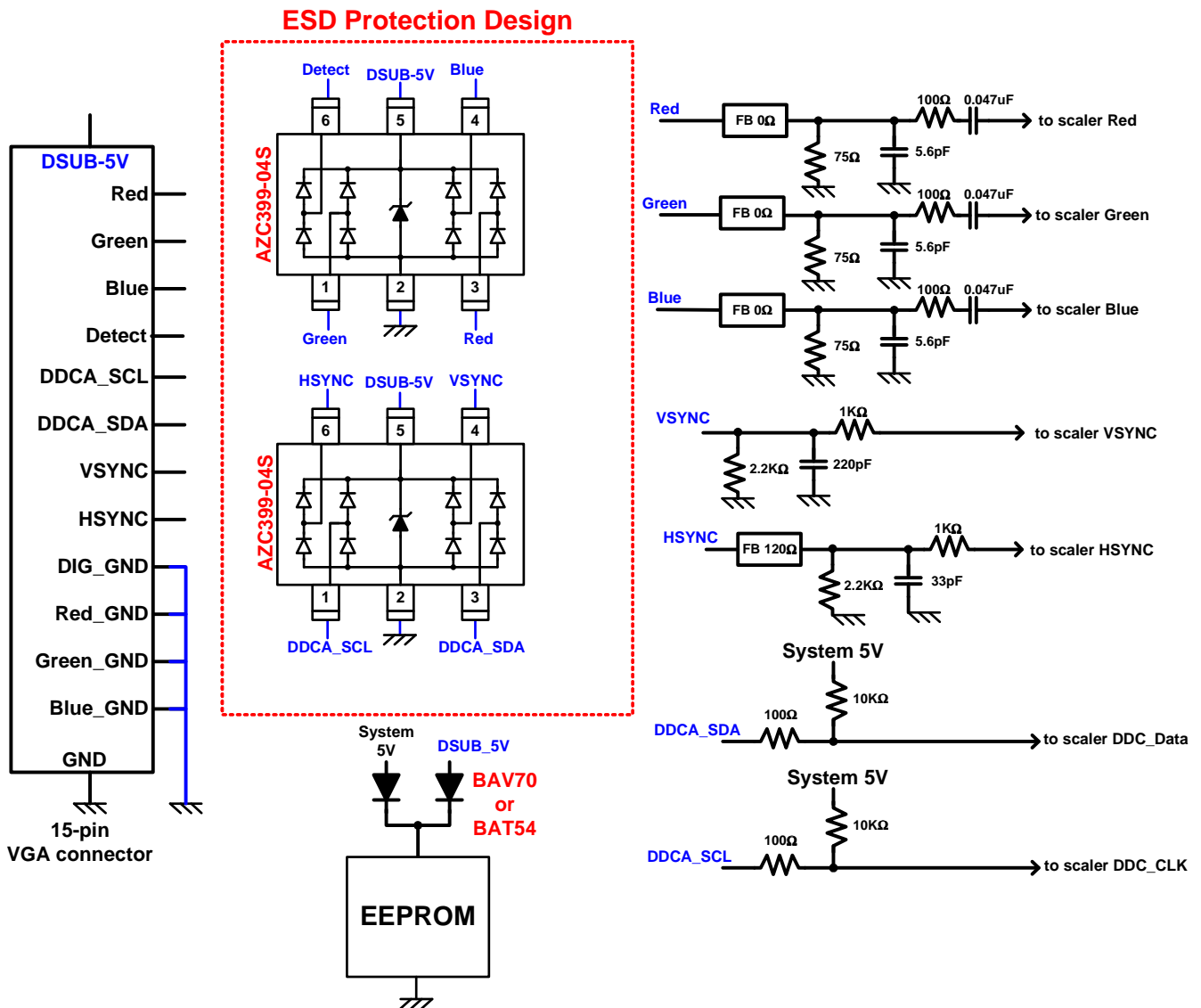


Fig. 5 The ESD design for a VGA INPUT port which two AZC399-04S are used.

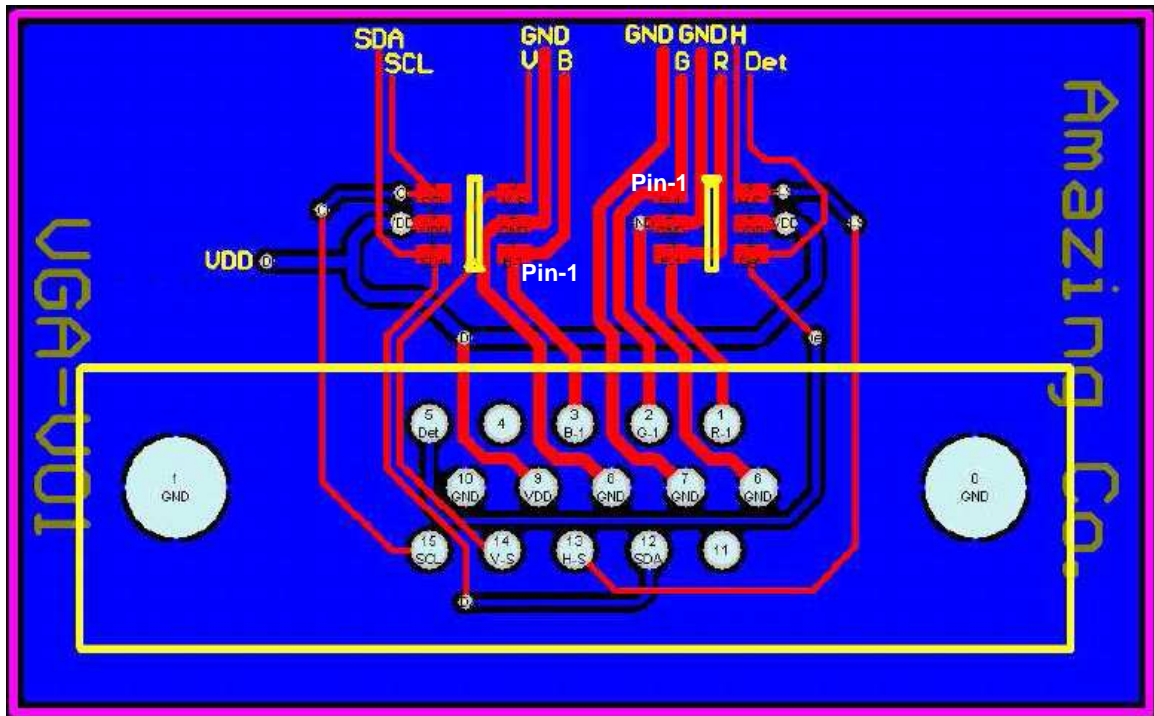


Fig. 6 The PCB layout example for a VGA port with two AZC399-04S being used.



4. SIM Port ESD Protection

The AZC399-04S can be also used to protect the SIM port. The ESD protection scheme for a SIM port is shown in Fig. 7. In the Fig.7, the voltage bus (VCC) of SIM port is connected to the power pin (pin 5) of AZC399-04S. The ground bus (GND) of SIM port is connected to the ground pin (pin 2) of AZC399-04S. The other three signal lines, I/O, Clock, and Reset, are connected three ESD protection pins of AZC399-04S, respectively. The rest ESD

protection pin of AZC399-04S is left to be floated.

When ESD voltage pulse appears on the one of the signal lines, the ESD pulse current will be conducted by AZC399-04S away from the controller chip. In addition, the ESD pulse current also can be conducted by AZC399-04S away from the controller chip when the ESD voltage pulse appears on the voltage bus (VCC) of SIM port. Therefore, the signal lines (I/O, Clock, and Reset) and voltage bus (VCC) of the SIM ports are all protected with an AZC399-04S.

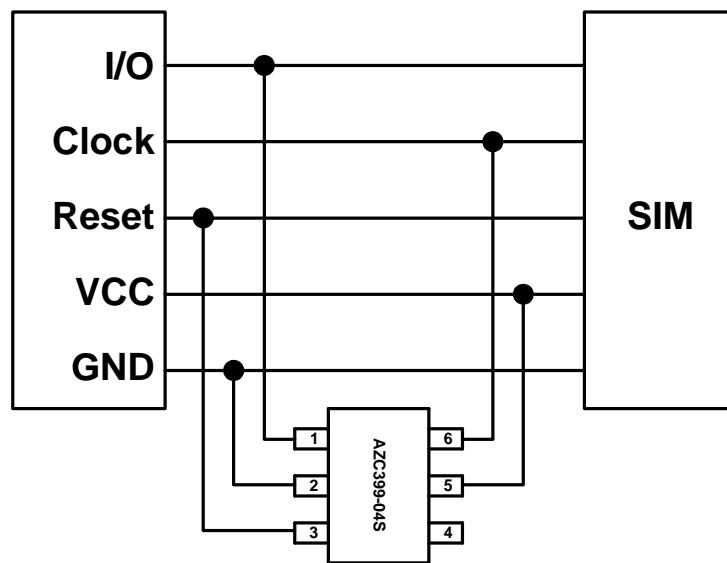
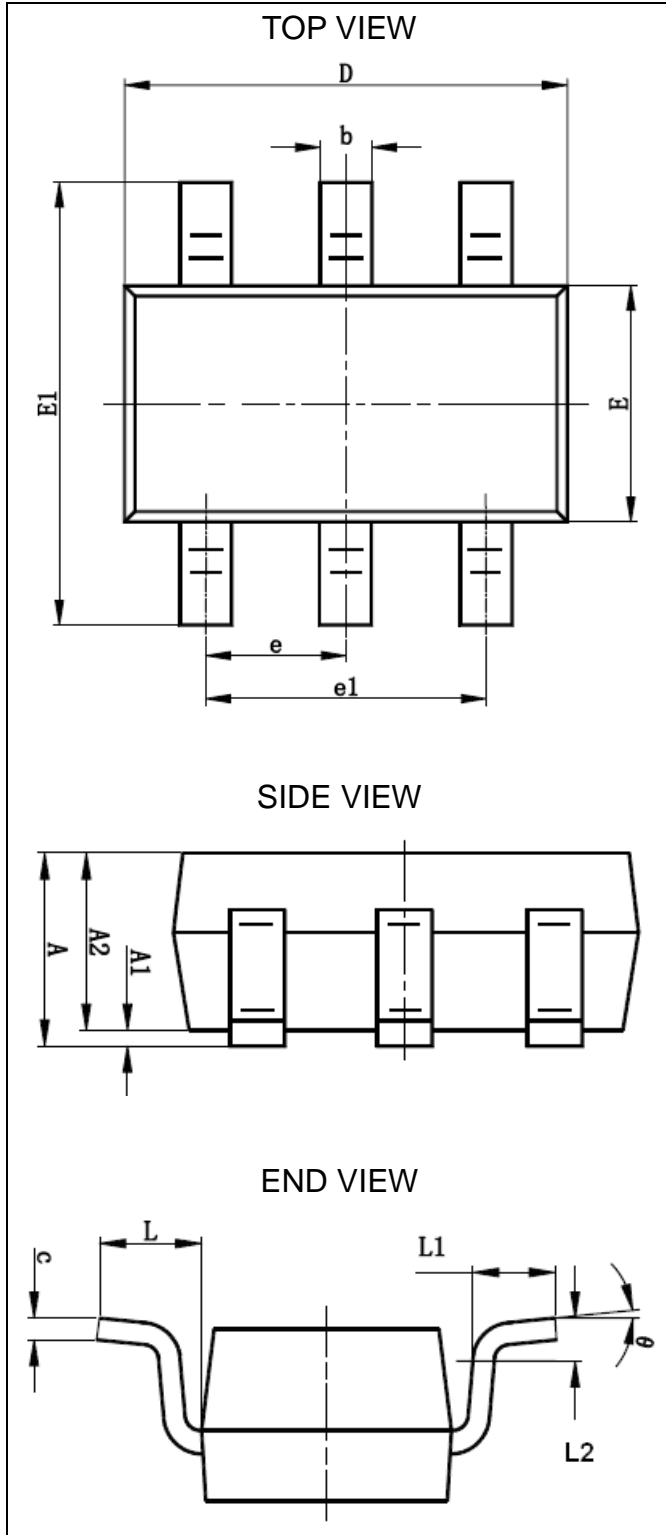


Fig. 7 ESD Protection scheme for SIM port by using AZC399-04S

Mechanical Details

SOT23-6L

PACKAGE DIAGRAMS



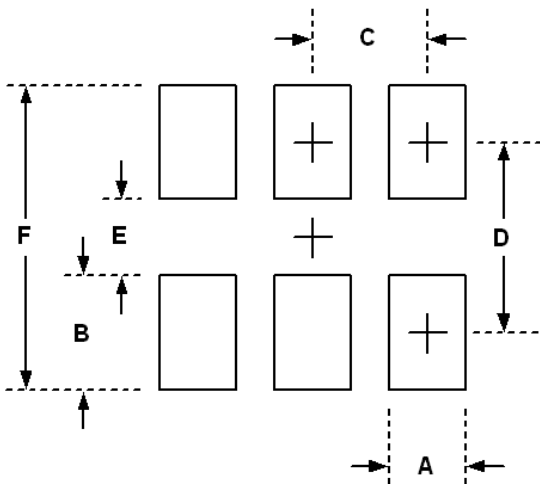
PACKAGE DIMENSIONS

Symbol	Millimeters		Inches	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0	0.15	0.000	0.006
A2	0.9	1.3	0.035	0.051
b	0.3	0.5	0.012	0.020
c	0.08	0.21	0.003	0.008
D	2.72	3.12	0.107	0.123
E	1.4	1.8	0.055	0.071
E1	2.6	3	0.102	0.118
e	0.95BSC		0.037BSC	
e1	1.9BSC		0.075BSC	
L1	0.3	0.6	0.012	0.024
L	0.7REF		0.028REF	
L2	0.25BSC		0.010BSC	
⌀	0	8	0	8

Notes:

- This dimension complies with JEDEC outline standard MO-178 Variation AB.
- Dimensioning and tolerancing per ASME Y14.5M-1994.
- All dimensions are in millimeters, and the dimensions in inches are for reference only.
- 1mm = 40 mils = 0.04 inches.

LAND LAYOUT

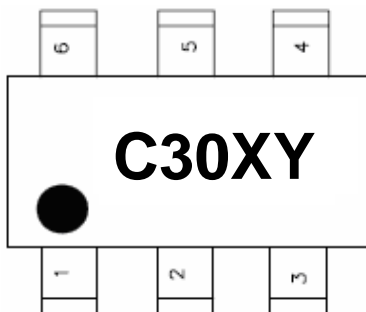


Dimensions		
Index	Millimeter	Inches
A	0.60	0.024
B	1.10	0.043
C	0.95	0.037
D	2.50	0.098
E	1.40	0.055
F	3.60	0.141

Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



Part Number	Marking Code
AZC399-04S	C30XY

C30 = Device Code
X = Date Code
Y = Control Code

Ordering Information

PN#	Material	Type	Reel size	MOQ/internal box	MOQ/carton
AZC399-04S.R7G	Green	T/R	7 inch	4 reel=12,000/box	6 box=72,000/carton



Revision History

Revision	Modification Description
Revision 2010/10/21	Formal Release.
Revision 2011/01/12	1. Update the ELECTRICAL CHARACTERISTICS. 2. Update the PACKAGE DIMENSIONS.
Revision 2011/07/30	1. Update the Company Logo. 2. Add the Ordering Information.

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