



**THE DATASHEET OF
NCS20032DMR2G**



Operational Amplifiers, High Slew Rate, Low Voltage, Rail-to-Rail Output

NCS2003/A, NCV2003, NCS20032, NCV20032, NCS20034, NCV20034

The NCS2003 family of op amps features high slew rate, low voltage operation with rail-to-rail output drive capability. The 1.8 V operation allows high performance operation in low voltage, low power applications. The fast slew rate and wide unity-gain bandwidth (5 MHz at 1.8 V) make these op amps suited for high speed applications. The low input offset voltage (4 mV max) allows the op amp to be used for current shunt monitoring. Additional features include no output phase reversal with overdriven inputs and ultra low input bias current of 1 pA.

The NCS2003 family is the ideal solution for a wide range of applications and products. The single channel NCS2003, dual channel NCS20032, and quad channel NCS20034 are available in a variety of compact and space-saving packages. The NCV prefix denotes that the device is AEC-Q100 Qualified and PPAP Capable.

Features

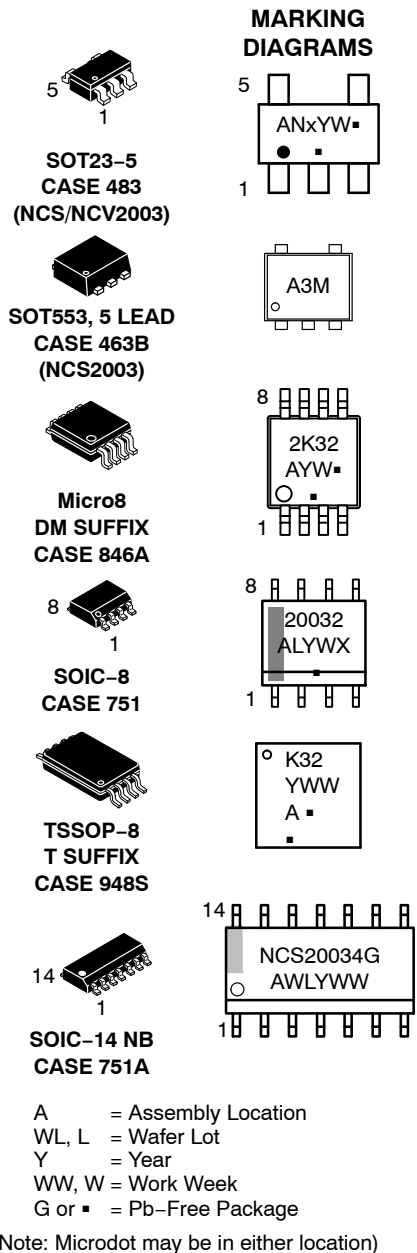
- Unity Gain Bandwidth: 7 MHz at $V_S = 5\text{ V}$
- Fast Slew Rate: 8 V/ μs rising, 12.5 V/ μs falling at $V_S = 5\text{ V}$
- Rail-to-Rail Output
- No Output Phase Reversal for Over-Driven Input Signals
- Low Offset Voltage: 0.5 mV typical
- Low Input Bias Current: 1 pA typical
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Current Shunt Monitor
- Signal Conditioning
- Active Filter
- Sensor Buffer

End Products

- Motor Control Drives
- Hard Drives
- Medical Devices
- White Goods and Air Conditioners



ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 2 of this data sheet.

NCS2003/A, NCV2003, NCS20032, NCV20032, NCS20034, NCV20034

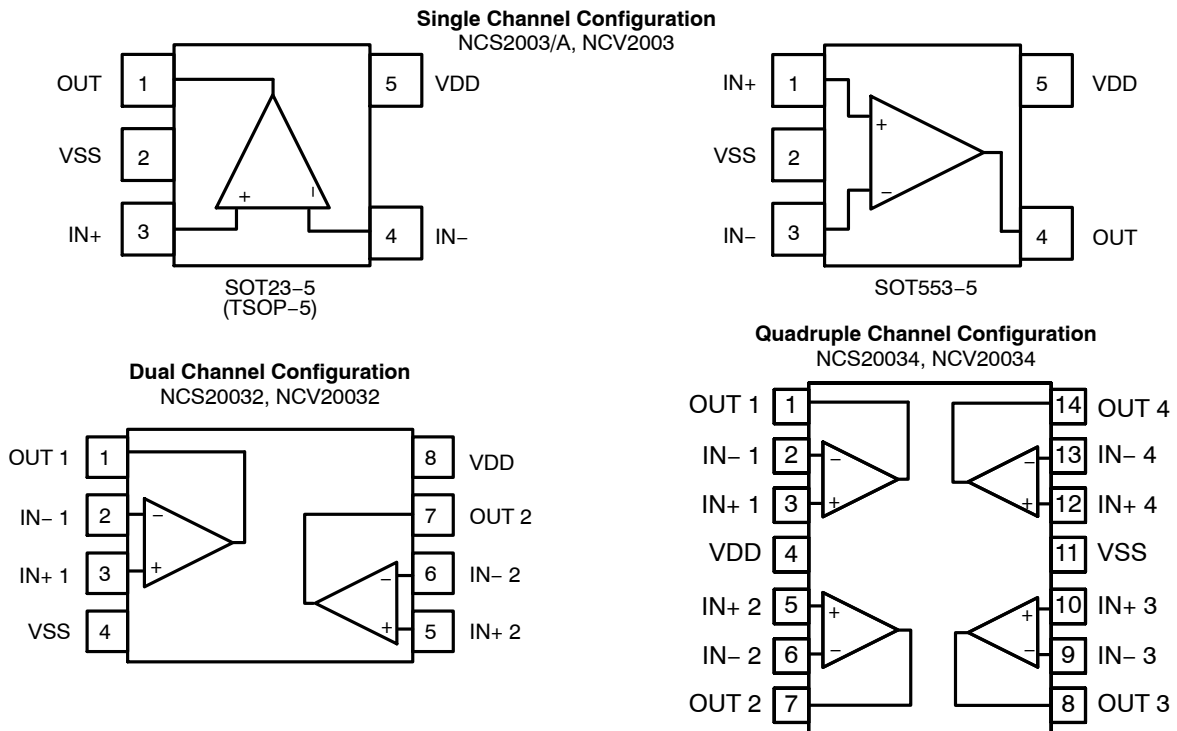


Figure 1. Pin Connections

ORDERING INFORMATION

| Device | Configuration | Automotive | Marking | Package | Shipping† |
|-----------------|---------------|------------|-----------|-----------------------|----------------------|
| NCS2003SN2T1G | Single | No | AN3 | SOT23-5 (Pb-Free) | 3000 / Tape and Reel |
| NCS2003ASN2T1G | | No | AN4 | SOT23-5 (Pb-Free) | 3000 / Tape and Reel |
| NCS2003XV53T2G | | No | A3 | SOT553-5 (Pb-Free) | 4000 /Tape and Reel |
| NCV2003SN2T1G* | | Yes | AN3 | SOT23-5 (Pb-Free) | 3000 / Tape and Reel |
| NCS20032DMR2G | Dual | No | 2K32 | Micro8 (Pb-Free) | 4000 / Tape and Reel |
| NCS20032DR2G | | | 20032 | SOIC-8 (Pb-Free) | 2500 / Tape and Reel |
| NCS20032DTBR2G | | | K32 | TSSOP-8 (Pb-Free) | 3000 / Tape and Reel |
| NCV20032DMR2G* | | Yes | 2K32 | Micro8 (Pb-Free) | 4000 / Tape and Reel |
| NCV20032DR2G* | | | 20032 | SOIC-8 (Pb-Free) | 2500 / Tape and Reel |
| NCV20032DTBR2G* | | | K32 | TSSOP-8 (Pb-Free) | 3000 / Tape and Reel |
| NCS20034DR2G | Quad | No | NCS20034G | SOIC-14 (Pb-Free) | 2500 / Tape and Reel |
| NCV20034DR2G* | | Yes | NCS20034G | SOIC-14 (Pb-Free) | 2500 / Tape and Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

NCS2003/A, NCV2003, NCS20032, NCV20032, NCS20034, NCV20034

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature, unless otherwise stated

| Parameter | Symbol | Limit | Unit |
|--------------------------------------|--------|-------|------|
| Supply Voltage ($V_{DD} - V_{SS}$) | V_S | 7.0 | V |

INPUT AND OUTPUT PINS

| | | | |
|-------------------------------|----------|-----------------------|----|
| Input Voltage (Note 1) | V_{IN} | $V_{SS} - 0.3$ to 7.0 | V |
| Input Current | I_{IN} | 10 | mA |
| Output Short Current (Note 2) | I_O | 100 | mA |

TEMPERATURE

| | | | |
|----------------------|-----------|------------|----|
| Storage Temperature | T_{STG} | -65 to 150 | °C |
| Junction Temperature | T_J | 150 | °C |

ESD RATINGS (Note 3)

| | | | | |
|----------------------|------------------------------------|-----|----------------------|---|
| Human Body Model | NCx2003, A NCx20032 NCx20034 | HBM | 3000 2000 3000 | V |
| Machine Model | NCx2003, A NCx20032 NCx20034 | MM | 200 100 150 | V |
| Charged Device Model | NCx2003, A NCx2003x | CDM | 1000 2000 | V |

OTHER PARAMETERS

| | | | |
|-------------------------------------|----------|---------|----|
| Moisture Sensitivity Level (Note 5) | MSL | Level 1 | |
| Latch-up Current (Note 4) | I_{LU} | 100 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Neither input should exceed the range of $V_{SS} - 300$ mV to 7.0 V. This device contains internal protection diodes between the input pins and V_{DD} . When V_{IN} exceeds V_{DD} , the input current should be limited to the specified value.
- Indefinite duration; however, maximum package power dissipation limits must be observed to ensure that the maximum junction temperature is not exceeded.
- This device series incorporates ESD protection and is tested by the following methods:
ESD Human Body Model tested per AEC-Q100-002 and JESD22-A114
ESD Machine Model tested per AEC-Q100-003 and JESD22-A115
ESD Charged Device Model tested per AEC-Q100-011 and ANSI/ESD S5.3.1-2009
- Latch-up current tested per JEDEC Standard JESD78.
- Moisture Sensitivity Level tested per IPC/JEDEC standard J-STD-020A.

THERMAL INFORMATION

| Thermal Metric | Symbol | Package | Single Layer Board (Note 6) | Multi Layer Board (Note 7) | Unit |
|--|---------------|----------------|-----------------------------|----------------------------|------|
| Junction to Ambient Thermal Resistance | θ_{JA} | SOT23-5/TSOP-5 | 408 | 355 | °C/W |
| | | SOT553-5 | 428 | 406 | |
| | | Micro8/MSOP8 | 235 | 163 | |
| | | SOIC-8 | 240 | 179 | |
| | | TSSOP-8 | 300 | 238 | |
| | | SOIC-14 | 167 | 123 | |

6. Values based on a 1S standard PCB according to JEDEC51-3 with 1.0 oz copper and a 300 mm² copper area

7. Values based on a 1S2P standard PCB according to JEDEC51-7 with 1.0 oz copper and a 100 mm² copper area

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Unit |
|--|--|------------|--------------|------|
| Operating Supply Voltage ($V_{DD} - V_{SS}$) | V_S | 1.7 | 5.5 | V |
| Specified Operating Range | NCS2003, A NCV2003, NCx20032, NCx20034 T_A | -40 -40 | +85 +125 | °C |
| Input Common Mode Range | V_{CM} | V_{SS} | $V_{DD}-0.6$ | V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

NCS2003/A, NCV2003, NCS20032, NCV20032, NCS20034, NCV20034

ELECTRICAL CHARACTERISTICS: $V_S = +1.8\text{ V}$

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted. **Boldface** limits apply over the specified temperature range. Guaranteed by design and/or characterization.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|------------------------------|--------------------------|---|-----------|------------|------------|------------------------------|
| INPUT CHARACTERISTICS | | | | | | |
| Input Offset Voltage | V_{OS} | NCS2003A | | 0.5 | 3.0 | mV |
| | | NCx2003, NCx20032, NCx20034 | | 0.5 | 4.0 | mV |
| | | | | | 5.0 | |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | | | 2.0 | | $\mu\text{V}/^\circ\text{C}$ |
| | | NCS2003A (Note 8) | | | 6.0 | $\mu\text{V}/^\circ\text{C}$ |
| Input Bias Current | I_{IB} | | | 1 | | pA |
| Input Offset Current | I_{OS} | | | 1 | | pA |
| Channel Separation | XTLK | DC, NCx20032, NCx20034 | | 100 | | dB |
| Input Resistance | R_{IN} | | | 1 | | $\text{T}\Omega$ |
| Input Capacitance | C_{IN} | | | 1.2 | | pF |
| Common Mode Rejection Ratio | CMRR | $V_{IN} = V_{SS}$ to $V_{DD} - 0.6\text{ V}$ | 70 | 80 | | dB |
| | | $V_{IN} = V_{SS} + 0.2\text{ V}$ to $V_{DD} - 0.6\text{ V}$ | 65 | | | |

OUTPUT CHARACTERISTICS

| | | | | | | | |
|------------------------------------|-----------|---------------------------|------------|-------------|-------|------------|----|
| Open Loop Voltage Gain | A_{VOL} | $R_L = 10\text{ k}\Omega$ | | 80 | 92 | dB | |
| | | | | 75 | | | |
| | | $R_L = 2\text{ k}\Omega$ | | | 92 | | |
| | | | | 70 | | | |
| Output Current Capability (Note 8) | I_{SC} | Sourcing | | 5 | 8 | mA | |
| | | Sinking | | 10 | 14 | | |
| Output Voltage High | V_{OH} | $R_L = 10\text{ k}\Omega$ | | 1.75 | 1.798 | V | |
| | | $R_L = 2\text{ k}\Omega$ | | 1.7 | 1.78 | | |
| Output Voltage Low | V_{OL} | $R_L = 10\text{ k}\Omega$ | NCx2003, A | | 7 | 50 | mV |
| | | | NCx2003x | | 7 | 100 | |
| | | $R_L = 2\text{ k}\Omega$ | | | | 20 | |

NOISE PERFORMANCE

| | | | | | | |
|-----------------------|-------|--------------------|--|-----|--|------------------------------|
| Voltage Noise Density | e_N | $f = 1\text{ kHz}$ | | 20 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| Current Noise Density | i_N | $f = 1\text{ kHz}$ | | 0.1 | | $\text{pA}/\sqrt{\text{Hz}}$ |

DYNAMIC PERFORMANCE

| | | | | | | |
|-------------------------|----------|---|--------------------------|-----|--|------------------------|
| Gain Bandwidth Product | GBWP | | | 5 | | MHz |
| Slew Rate at Unity Gain | SR | Rising Edge, $R_L = 2\text{ k}\Omega$, $A_V = +1$ | | 6 | | $\text{V}/\mu\text{s}$ |
| | | Falling Edge, $R_L = 2\text{ k}\Omega$, $A_V = +1$ | | 9 | | |
| Phase Margin | ψ_m | $R_L = 10\text{ k}\Omega$, $C_L = 5\text{ pF}$ | | 53 | | $^\circ$ |
| Gain Margin | A_m | $R_L = 10\text{ k}\Omega$, $C_L = 5\text{ pF}$ | NCx2003, A | 12 | | dB |
| | | | NCx2003x | 8 | | |
| Settling Time | t_s | $V_O = 1\text{ V}_{pp}$, Gain = 1, $C_L = 20\text{ pF}$ | Settling time to 0.1% | 1.8 | | μs |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Guaranteed by design and/or characterization.

NCS2003/A, NCV2003, NCS20032, NCV20032, NCS20034, NCV20034

ELECTRICAL CHARACTERISTICS: $V_S = +1.8\text{ V}$ (continued)

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted. **Boldface** limits apply over the specified temperature range. Guaranteed by design and/or characterization.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-----------|--------|------------|-----|-----|-----|------|
|-----------|--------|------------|-----|-----|-----|------|

DYNAMIC PERFORMANCE

| | | | | | | |
|------------------------------------|-------|---|--|-------|--|---|
| Total Harmonics Distortion + Noise | THD+N | $V_O = 1\text{ V}_{pp}$, $R_L = 2\text{ k}\Omega$, $A_V = +1$, $f = 1\text{ kHz}$ | | 0.005 | | % |
| | | $V_O = 1\text{ V}_{pp}$, $R_L = 2\text{ k}\Omega$, $A_V = +1$, $f = 10\text{ kHz}$ | | 0.025 | | |

POWER SUPPLY

| | | | | | | | |
|------------------------------|----------|----------------------|--------------------|-----------|-----|-------------|---------------|
| Power Supply Rejection Ratio | PSRR | NCx2003 | | 72 | 80 | | dB |
| | | | | 65 | | | |
| | | NCx20032, NCx20034 | | 80 | 100 | | |
| Quiescent Current | I_{DD} | No load, per channel | NCx2003, A | | 230 | 560 | μA |
| | | | | | | 1000 | |
| | | | NCx20032, NCx20034 | | 275 | 375 | |
| | | | | | | 575 | |

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8. Guaranteed by design and/or characterization.

ELECTRICAL CHARACTERISTICS: $V_S = +5.0\text{ V}$

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted. **Boldface** limits apply over the specified temperature range. Guaranteed by design and/or characterization.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-----------|--------|------------|-----|-----|-----|------|
|-----------|--------|------------|-----|-----|-----|------|

INPUT CHARACTERISTICS

| | | | | | | |
|----------------------|--------------------------|------------------------|--|------------|------------|------------------------------|
| Input Offset Voltage | V_{OS} | NCS2003A | | 0.5 | 3.0 | mV |
| | | NCx2003 | | 0.5 | 4.0 | mV |
| | | NCx20032, NCx20034 | | | 5.0 | mV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | | | 2.0 | | $\mu\text{V}/^\circ\text{C}$ |
| | | NCS2003A (Note 9) | | | 6.0 | $\mu\text{V}/^\circ\text{C}$ |
| Input Bias Current | I_{IB} | | | 1 | | pA |
| Input Offset Current | I_{OS} | | | 1 | | pA |
| Channel Separation | XTLK | DC, NCx20032, NCx20034 | | 100 | | dB |
| Input Resistance | R_{IN} | | | 1 | | $\text{T}\Omega$ |
| Input Capacitance | C_{IN} | | | 1.2 | | pF |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9. Guaranteed by design and/or characterization.

NCS2003/A, NCV2003, NCS20032, NCV20032, NCS20034, NCV20034

ELECTRICAL CHARACTERISTICS: $V_S = +5.0\text{ V}$ (continued)

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted. **Boldface** limits apply over the specified temperature range. Guaranteed by design and/or characterization.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit | |
|------------------------------|--------|--------------------|---|-----------|-----|------|----|
| INPUT CHARACTERISTICS | | | | | | | |
| Common Mode Rejection Ratio | CMRR | NCx2003, A | $V_{IN} = V_{SS}$ to $V_{DD} - 0.6\text{ V}$ | 65 | 90 | | dB |
| | | | $V_{IN} = V_{SS} + 0.2\text{ V}$ to $V_{DD} - 0.6\text{ V}$ | 63 | | | |
| | | NCx20032, NCx20034 | $V_{IN} = V_{SS}$ to $V_{DD} - 0.6\text{ V}$ | 70 | 90 | | |
| | | | $V_{IN} = V_{SS} + 0.2\text{ V}$ to $V_{DD} - 0.6\text{ V}$ | 65 | | | |

| | | | | | | | |
|------------------------------------|-----------|---------------------------|------------|-------------|------|------------|----|
| OUTPUT CHARACTERISTICS | | | | | | | |
| Open Loop Voltage Gain | A_{VOL} | $R_L = 10\text{ k}\Omega$ | | 86 | 92 | | dB |
| | | | | 78 | | | |
| | | $R_L = 2\text{ k}\Omega$ | | 83 | 92 | | |
| | | | | 78 | | | |
| Output Current Capability (Note 9) | I_{SC} | Sourcing | | 40 | 76 | | mA |
| | | Sinking | | 50 | 96 | | |
| Output Voltage High | V_{OH} | $R_L = 10\text{ k}\Omega$ | | 4.95 | 4.99 | | V |
| | | $R_L = 2\text{ k}\Omega$ | | 4.9 | 4.97 | | |
| Output Voltage Low | V_{OL} | $R_L = 10\text{ k}\Omega$ | NCx2003, A | | 8 | 50 | mV |
| | | | NCx2003x | | 8 | 100 | |
| | | $R_L = 2\text{ k}\Omega$ | | | 24 | 100 | |

| | | | | | | | |
|--------------------------|-------|--------------------|--|--|-----|--|------------------------------|
| NOISE PERFORMANCE | | | | | | | |
| Voltage Noise Density | e_N | $f = 1\text{ kHz}$ | | | 20 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| Current Noise Density | i_N | $f = 1\text{ kHz}$ | | | 0.1 | | $\text{pA}/\sqrt{\text{Hz}}$ |

| | | | | | | | |
|------------------------------------|----------|---|--------------------------|--|-------|--|------------------------|
| DYNAMIC PERFORMANCE | | | | | | | |
| Gain Bandwidth Product | GBWP | | | | 7 | | MHz |
| Slew Rate at Unity Gain | SR | Rising Edge, $R_L = 2\text{ k}\Omega$, $A_V = +1$ | | | 8 | | $\text{V}/\mu\text{s}$ |
| | | Falling Edge, $R_L = 2\text{ k}\Omega$, $A_V = +1$ | | | 12.5 | | |
| Phase Margin | ψ_m | $R_L = 10\text{ k}\Omega$, $C_L = 5\text{ pF}$ | NCx2003, A | | 64 | | $^\circ$ |
| | | | NCx2003x | | 56 | | |
| Gain Margin | A_m | $R_L = 10\text{ k}\Omega$, $C_L = 5\text{ pF}$ | | | 9 | | dB |
| Settling Time | t_S | $V_O = 1\text{ V}_{pp}$, Gain = 1, $C_L = 20\text{ pF}$ | Settling time to 0.1% | | 0.6 | | μs |
| Total Harmonics Distortion + Noise | THD+N | $V_O = 4\text{ V}_{pp}$, $R_L = 2\text{ k}\Omega$, $A_V = +1$, $f = 1\text{ kHz}$ | | | 0.002 | | % |
| | | $V_O = 4\text{ V}_{pp}$, $R_L = 2\text{ k}\Omega$, $A_V = +1$, $f = 10\text{ kHz}$ | | | 0.01 | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9. Guaranteed by design and/or characterization.

NCS2003/A, NCV2003, NCS20032, NCV20032, NCS20034, NCV20034

ELECTRICAL CHARACTERISTICS: $V_S = +5.0\text{ V}$ (continued)

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted. **Boldface** limits apply over the specified temperature range. Guaranteed by design and/or characterization.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit | |
|------------------------------|----------|----------------------|-----------------------|-------------|-----|------|---------------|
| POWER SUPPLY | | | | | | | |
| Power Supply Rejection Ratio | PSRR | NCx2003, A | | 72 | 80 | | dB |
| | | | | 65 | | | |
| | | NCx20032, NCx20034 | | 80 | 100 | | |
| Quiescent Current | I_{DD} | No load, per channel | NCx2003, A | | 300 | 660 | μA |
| | | | | 1000 | | | |
| | | | NCx20032, NCx20034 | | 325 | 450 | |
| | | | | 675 | | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9. Guaranteed by design and/or characterization.

TYPICAL CHARACTERISTICS

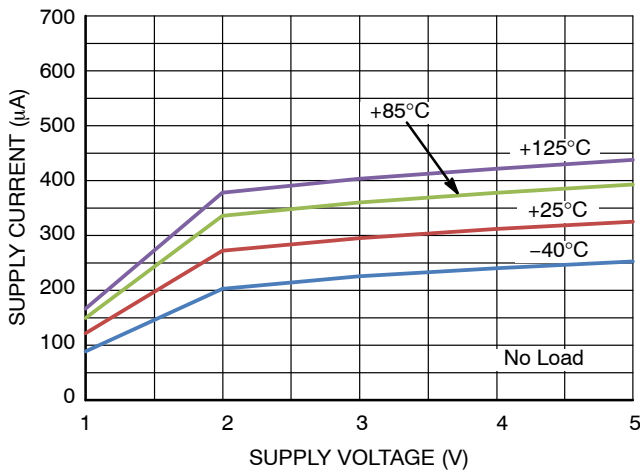


Figure 2. Quiescent Supply Current vs. Supply Voltage

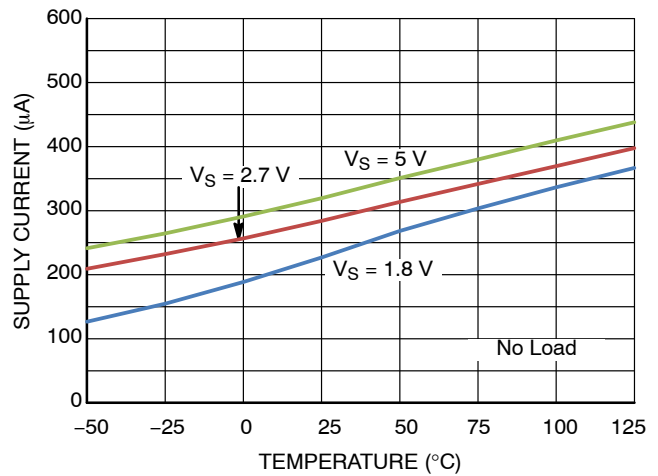


Figure 3. Quiescent Supply Current vs. Temperature

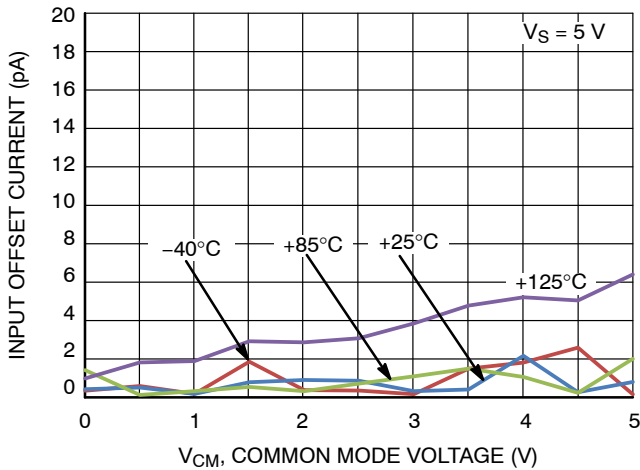


Figure 4. Input Offset Current vs. V_{CM}

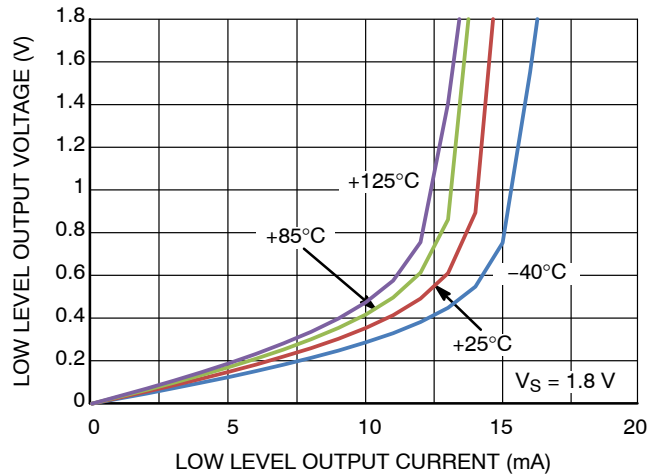


Figure 5. Low Level Output Voltage vs. Output Current @ $V_S = 1.8 V$

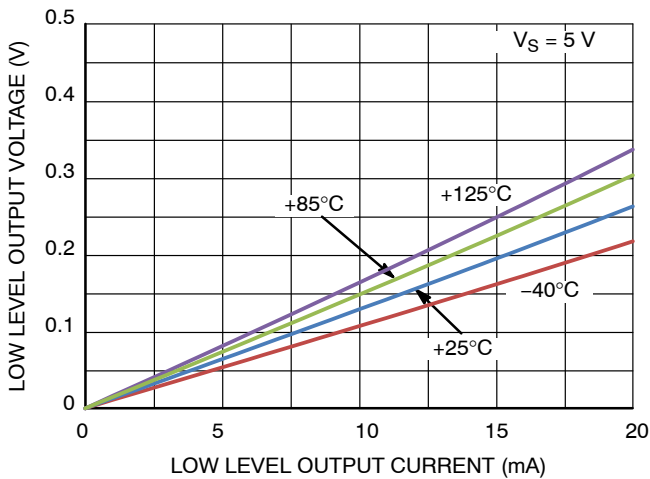


Figure 6. Low Level Output Voltage vs. Output Current @ $V_S = 5 V$

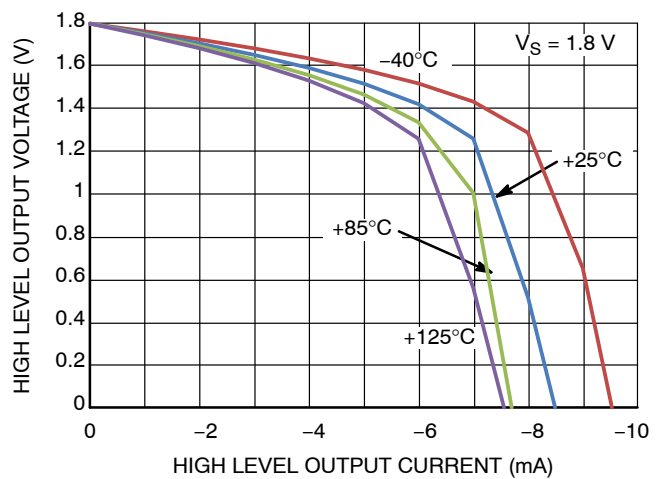


Figure 7. High Level Output Voltage vs. Output Current @ $V_S = 1.8 V$

TYPICAL CHARACTERISTICS (Continued)

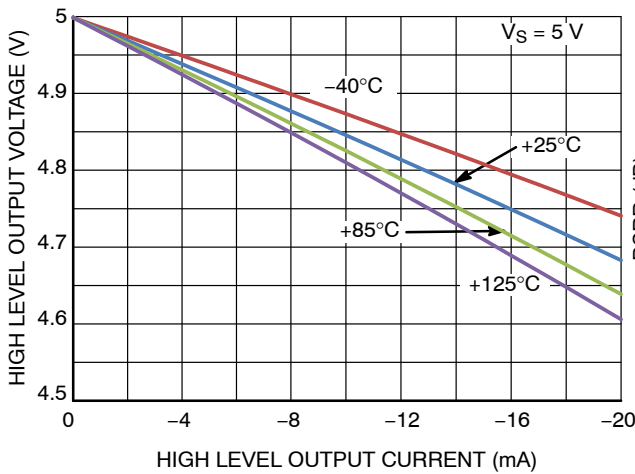


Figure 8. High Level Output Voltage vs. Output Current @ $V_S = 5\text{ V}$

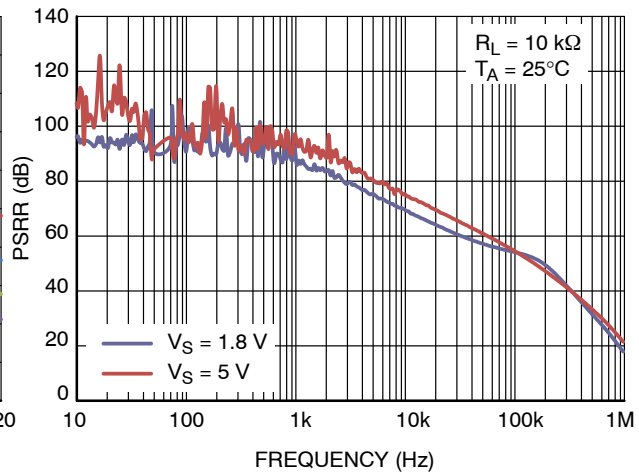


Figure 9. PSRR vs. Frequency

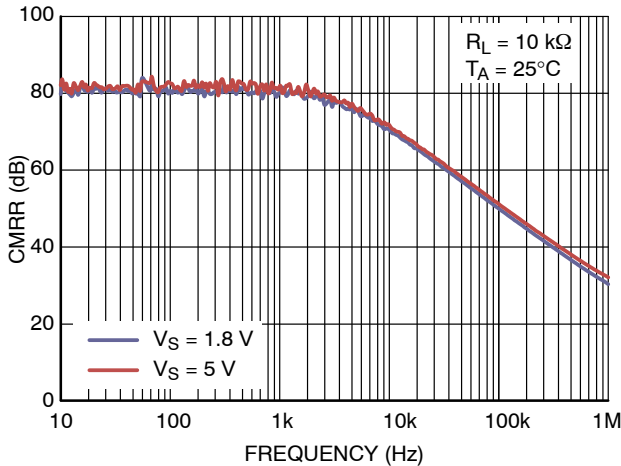


Figure 10. CMRR vs. Frequency

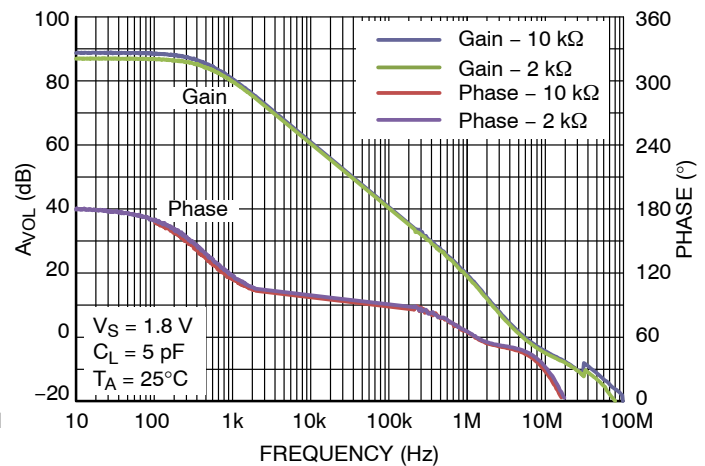


Figure 11. Open Loop Gain and Phase vs. Frequency @ $V_S = 1.8\text{ V}$

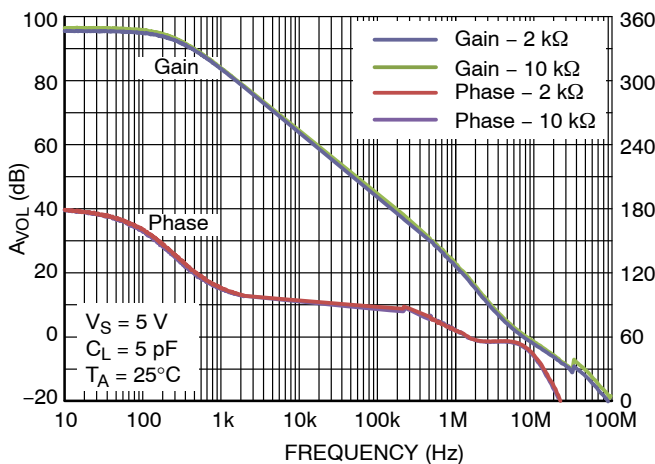


Figure 12. Open Loop Gain and Phase vs. Frequency @ $V_S = 5\text{ V}$

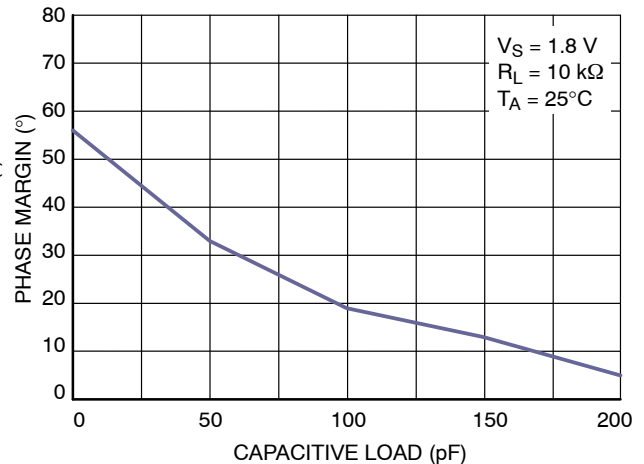


Figure 13. Phase Margin vs. Capacitive Load

TYPICAL CHARACTERISTICS (Continued)

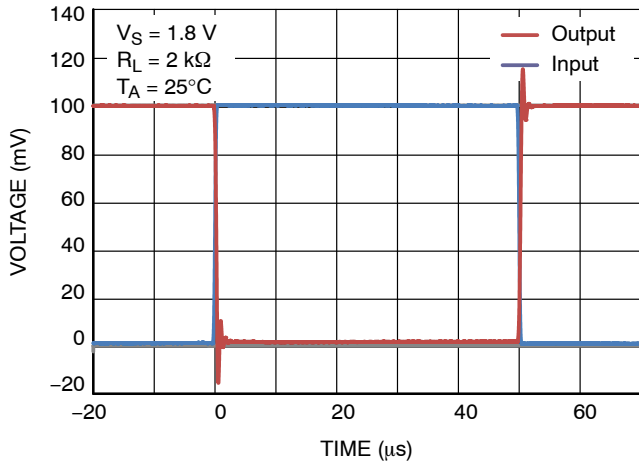


Figure 14. Inverting Small Signal Transient Response

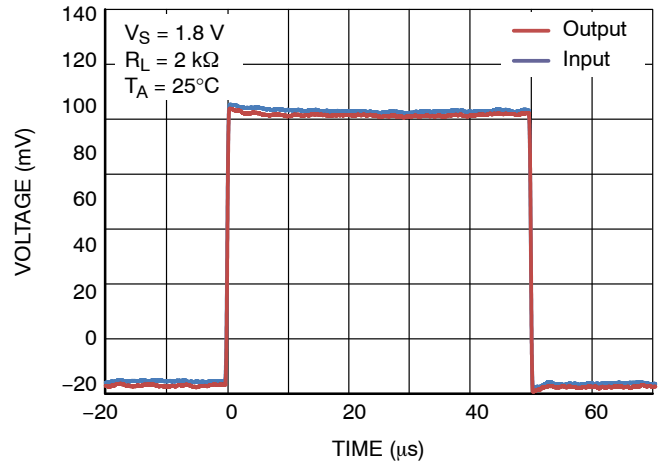


Figure 15. Non-Inverting Small Signal Transient Response

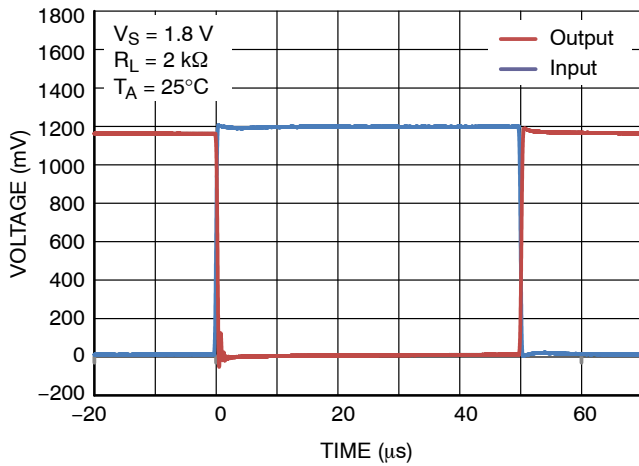


Figure 16. Inverting Large Signal Transient Response

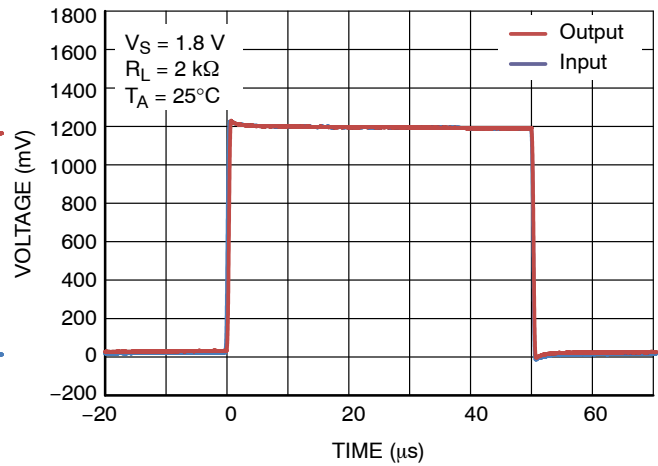


Figure 17. Non-Inverting Large Signal Transient Response

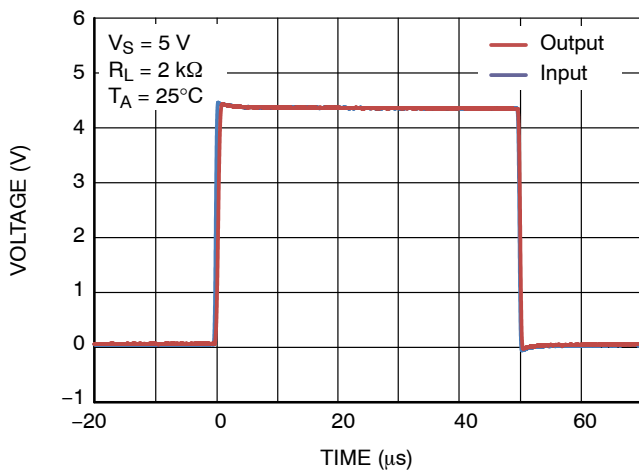


Figure 18. Non-Inverting Large Signal Transient Response

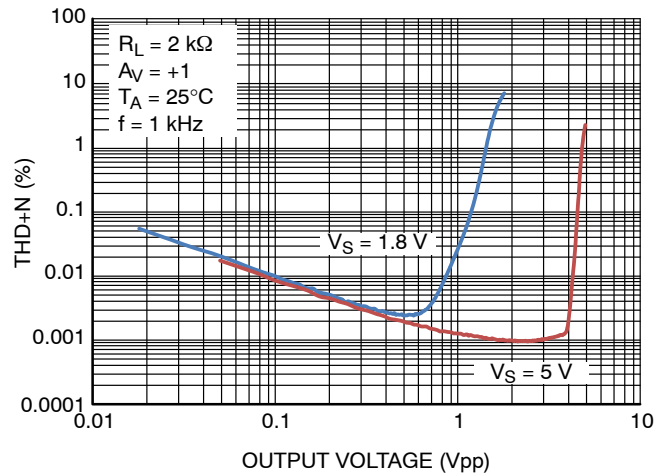


Figure 19. THD+N vs. Output Voltage

TYPICAL CHARACTERISTICS (Continued)

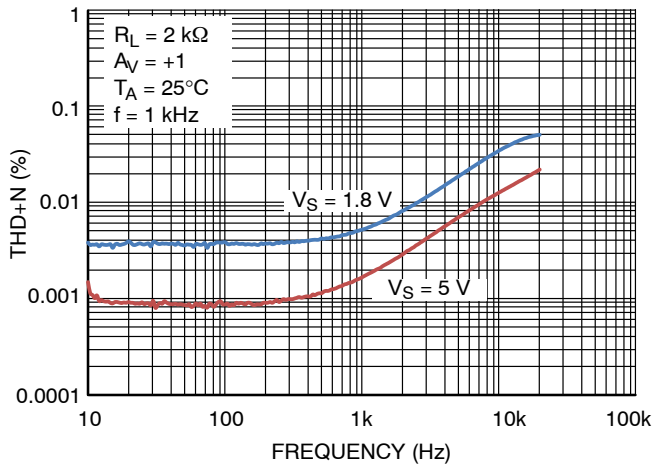


Figure 20. THD+N vs. Frequency

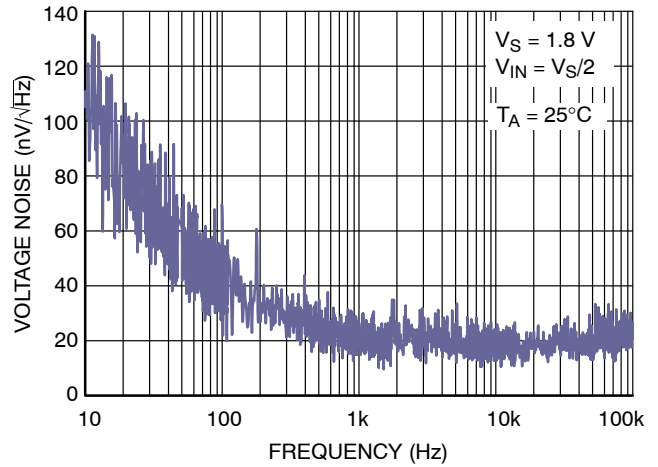


Figure 21. Input Voltage Noise vs. Frequency

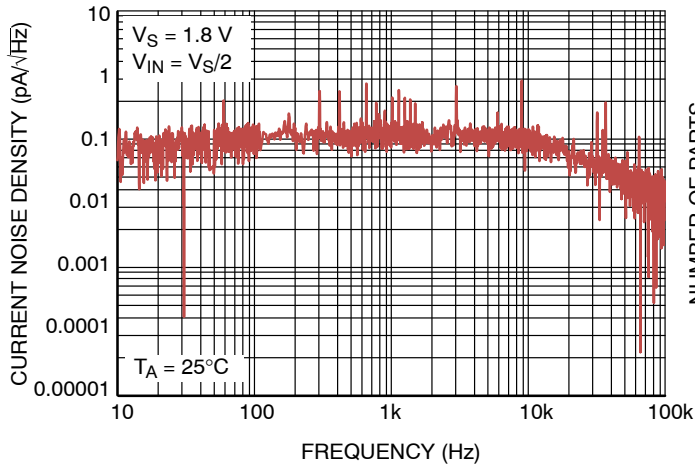


Figure 22. Noise Density vs. Frequency

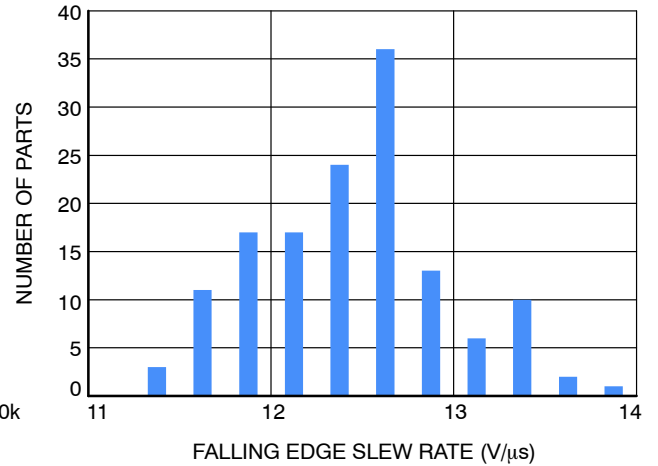


Figure 23. Falling Edge Slew Rate @ Vs = 5 V

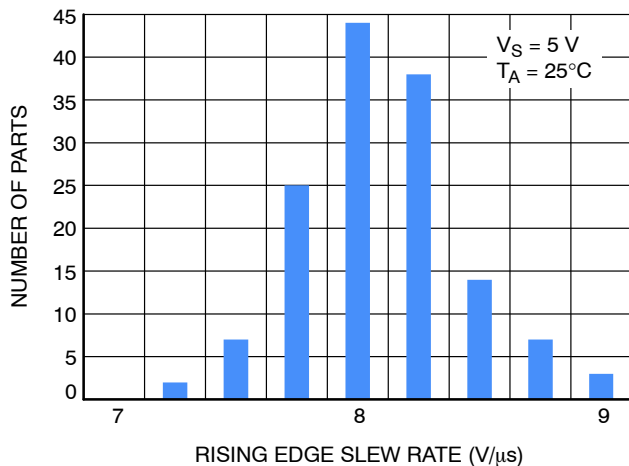


Figure 24. Rising Edge Slew Rate @ Vs = 5 V

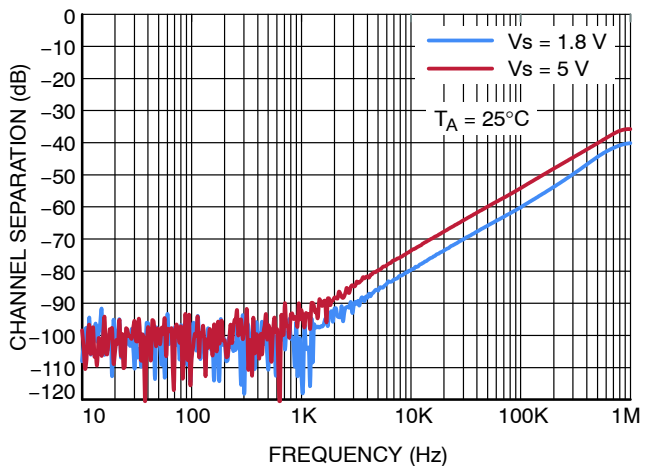
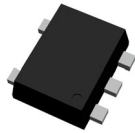


Figure 25. Channel Separation

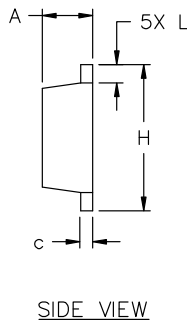
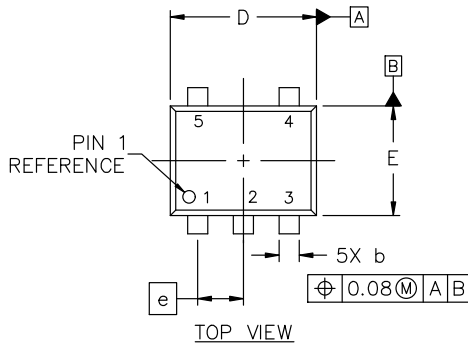
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



SOT-553-5 1.60x1.20x0.55, 0.50P
CASE 463B
ISSUE D

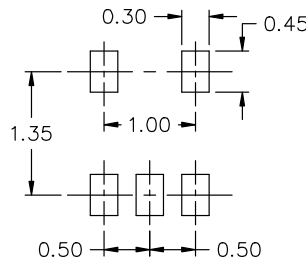
DATE 21 FEB 2024



NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.50 | 0.55 | 0.60 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.08 | 0.13 | 0.18 |
| D | 1.55 | 1.60 | 1.65 |
| E | 1.15 | 1.20 | 1.25 |
| e | 0.50 BSC | | |
| H | 1.55 | 1.60 | 1.65 |
| L | 0.10 | 0.20 | 0.30 |



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
 PIN 1. BASE
 2. EMITTER
 3. BASE
 4. COLLECTOR
 5. COLLECTOR

STYLE 2:
 PIN 1. CATHODE
 2. COMMON ANODE
 3. CATHODE 2
 4. CATHODE 3
 5. CATHODE 4

STYLE 3:
 PIN 1. ANODE 1
 2. N/C
 3. ANODE 2
 4. CATHODE 2
 5. CATHODE 1

STYLE 4:
 PIN 1. SOURCE 1
 2. DRAIN 1/2
 3. SOURCE 1
 4. GATE 1
 5. GATE 2

STYLE 5:
 PIN 1. ANODE
 2. EMITTER
 3. BASE
 4. COLLECTOR
 5. CATHODE

STYLE 6:
 PIN 1. EMITTER 2
 2. BASE 2
 3. EMITTER 1
 4. COLLECTOR 1
 5. COLLECTOR 2/BASE 1

STYLE 7:
 PIN 1. BASE
 2. EMITTER
 3. BASE
 4. COLLECTOR
 5. COLLECTOR

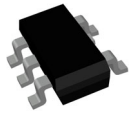
STYLE 8:
 PIN 1. CATHODE
 2. COLLECTOR
 3. N/C
 4. BASE
 5. EMITTER

STYLE 9:
 PIN 1. ANODE
 2. CATHODE
 3. ANODE
 4. ANODE
 5. ANODE

| | | |
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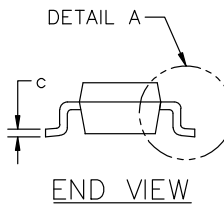
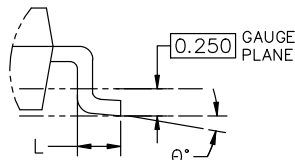
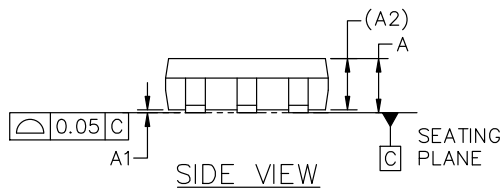
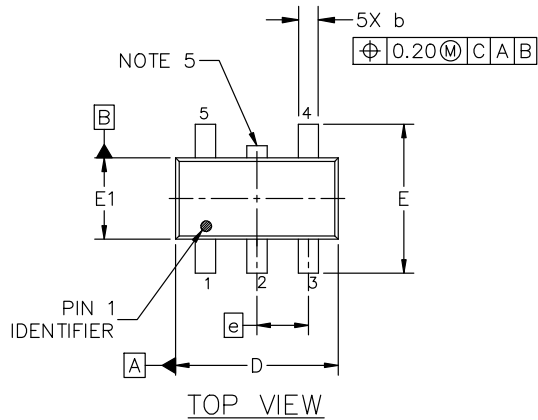
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TSOP-5 3.00x1.50x0.95, 0.95P CASE 483 ISSUE P

DATE 01 APR 2024

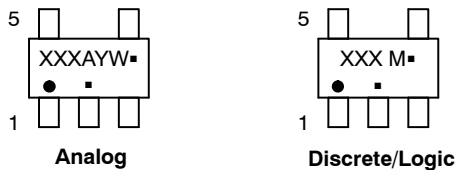


NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

| DIM | MILLIMETERS | | |
|-----|-------------|-------|-------|
| | MIN. | NOM. | MAX. |
| A | 0.900 | 1.000 | 1.100 |
| A1 | 0.010 | 0.055 | 0.100 |
| A2 | 0.950 REF. | | |
| b | 0.250 | 0.375 | 0.500 |
| c | 0.100 | 0.180 | 0.260 |
| D | 2.850 | 3.000 | 3.150 |
| E | 2.500 | 2.750 | 3.000 |
| E1 | 1.350 | 1.500 | 1.650 |
| e | 0.950 BSC | | |
| L | 0.200 | 0.400 | 0.600 |
| θ | 0° | 5° | 10° |

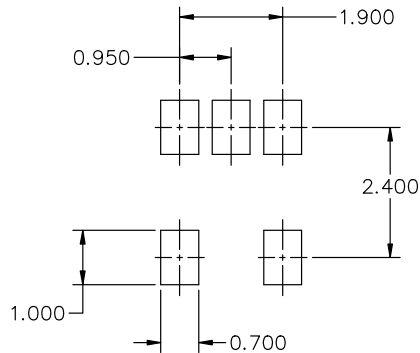
GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code XXX = Specific Device Code
 A = Assembly Location M = Date Code
 Y = Year ▪ = Pb-Free Package
 W = Work Week

▪ = Pb-Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

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| DESCRIPTION: | TSOP-5 3.00x1.50x0.95, 0.95P | PAGE 1 OF 1 |

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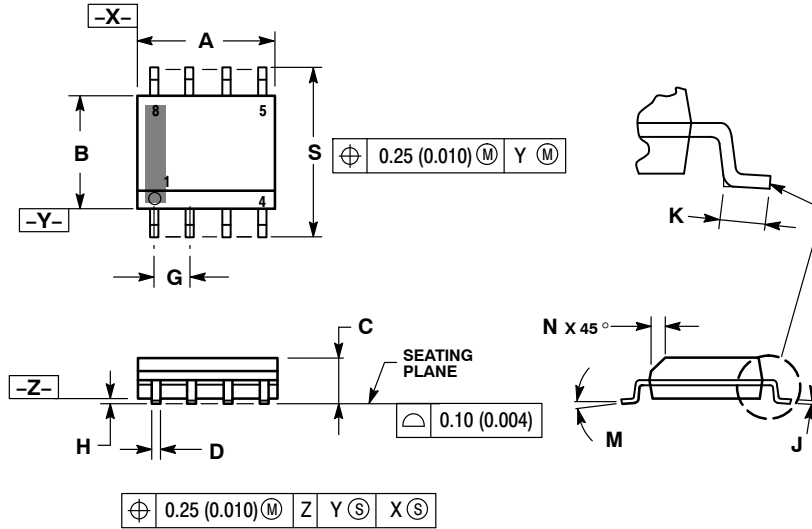
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

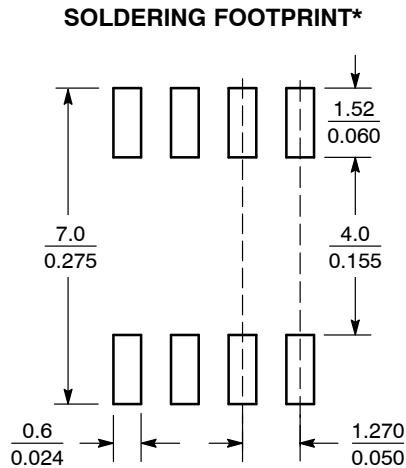
DATE 16 FEB 2011



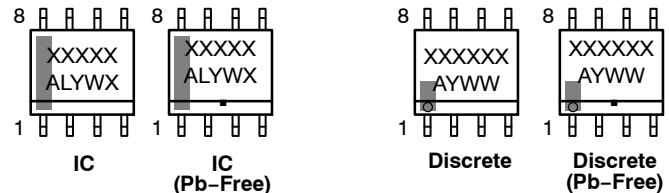
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

GENERIC MARKING DIAGRAM*



SCALE 6:1 ($\frac{\text{mm}}{\text{inches}}$)



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|--|---|---|---|
| <p>STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER</p> | <p>STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1</p> | <p>STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1</p> | <p>STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE</p> |
| <p>STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE</p> | <p>STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE</p> | <p>STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd</p> | <p>STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1</p> |
| <p>STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON</p> | <p>STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND</p> | <p>STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1</p> | <p>STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> | <p>STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN</p> | <p>STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON</p> | <p>STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC</p> | <p>STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE</p> | <p>STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1</p> | <p>STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6</p> | <p>STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND</p> | <p>STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT</p> | <p>STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT</p> | <p>STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC</p> | <p>STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN</p> | <p>STYLE 28: PIN 1. SW_TO_GND 2. DASIC OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN</p> |
| <p>STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1</p> | <p>STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1</p> | | |

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| DESCRIPTION: | SOIC-8 NB | PAGE 2 OF 2 |

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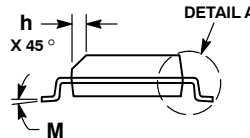
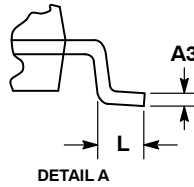
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0° | 7° | 0° | 7° |

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

| | | |
|------------------|-------------|--|
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SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 2:
 CANCELLED

STYLE 3:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON CATHODE

STYLE 4:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 5:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 6:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

STYLE 7:
 PIN 1. ANODE/CATHODE
 2. COMMON ANODE
 3. COMMON CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. COMMON CATHODE
 12. COMMON ANODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

STYLE 8:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

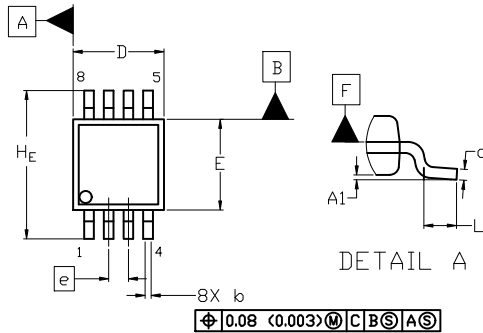
ON Semiconductor®



SCALE 2:1

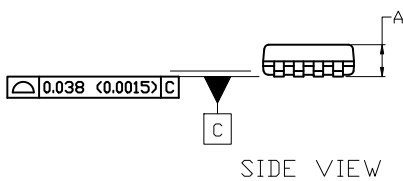
Micro8 CASE 846A-02 ISSUE K

DATE 16 JUL 2020

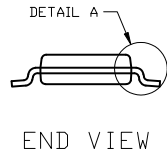


TOP VIEW

NOTE 3



SIDE VIEW



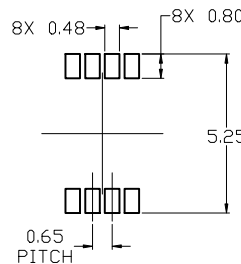
END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS *D* AND *E* DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION *E* DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS *D* AND *E* ARE DETERMINED AT DATUM *F*.
5. DATUMS *A* AND *B* ARE TO BE DETERMINED AT DATUM *F*.
6. *A1* IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

$\phi 0.08$ (0.003) M C B S A S

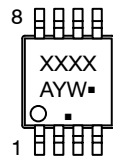
| DIM | MILLIMETERS | | |
|----------------------|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | --- | --- | 1.10 |
| A1 | 0.05 | 0.08 | 0.15 |
| <i>b</i> | 0.25 | 0.33 | 0.40 |
| <i>c</i> | 0.13 | 0.18 | 0.23 |
| <i>D</i> | 2.90 | 3.00 | 3.10 |
| <i>E</i> | 2.90 | 3.00 | 3.10 |
| <i>e</i> | 0.65 BSC | | |
| <i>H_E</i> | 4.75 | 4.90 | 5.05 |
| <i>L</i> | 0.40 | 0.55 | 0.70 |



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

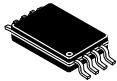
STYLE 3:

1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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| DESCRIPTION: | MICRO8 | PAGE 1 OF 1 |

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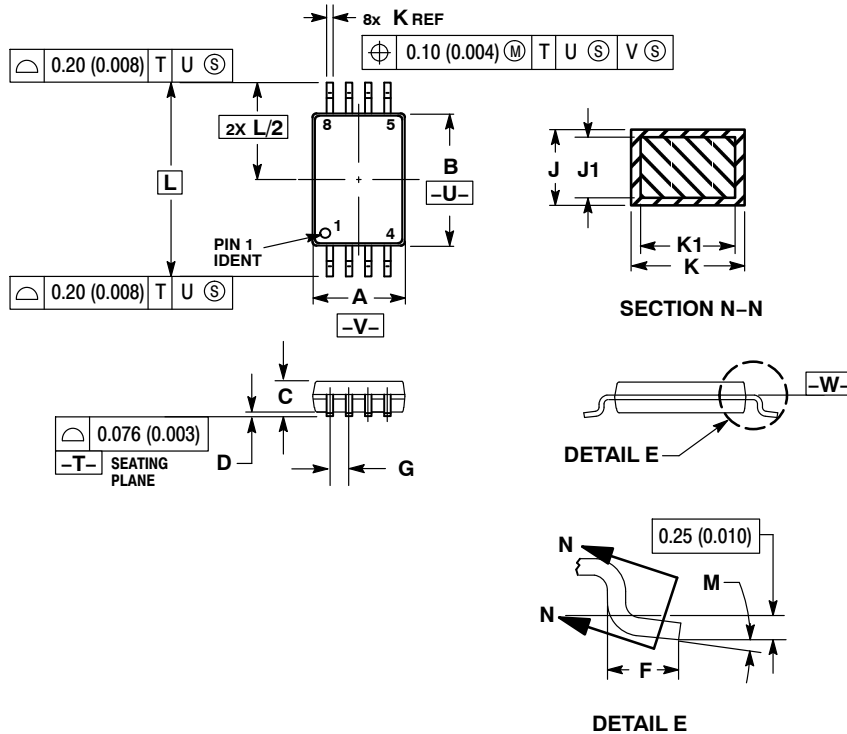
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

TSSOP-8
CASE 948S
ISSUE C

DATE 20 JUN 2008

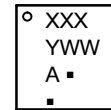


NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.114 | 0.122 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.10 | --- | 0.043 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.70 | 0.020 | 0.028 |
| G | 0.65 BSC | | 0.026 BSC | |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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