



**THE DATASHEET OF
74HCT273PW-Q100J**



74HC273-Q100; 74HCT273-Q100

Octal D-type flip-flop with reset; positive-edge trigger

Rev. 2 — 3 September 2020

Product data sheet

1. General description

The 74HC273-Q100; 74HCT273-Q100 is an octal positive-edge triggered D-type flip-flop. The device features clock (CP) and master reset (\overline{MR}) inputs. The outputs Qn will assume the state of their corresponding Dn inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A LOW on \overline{MR} forces the outputs LOW independently of clock and data inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

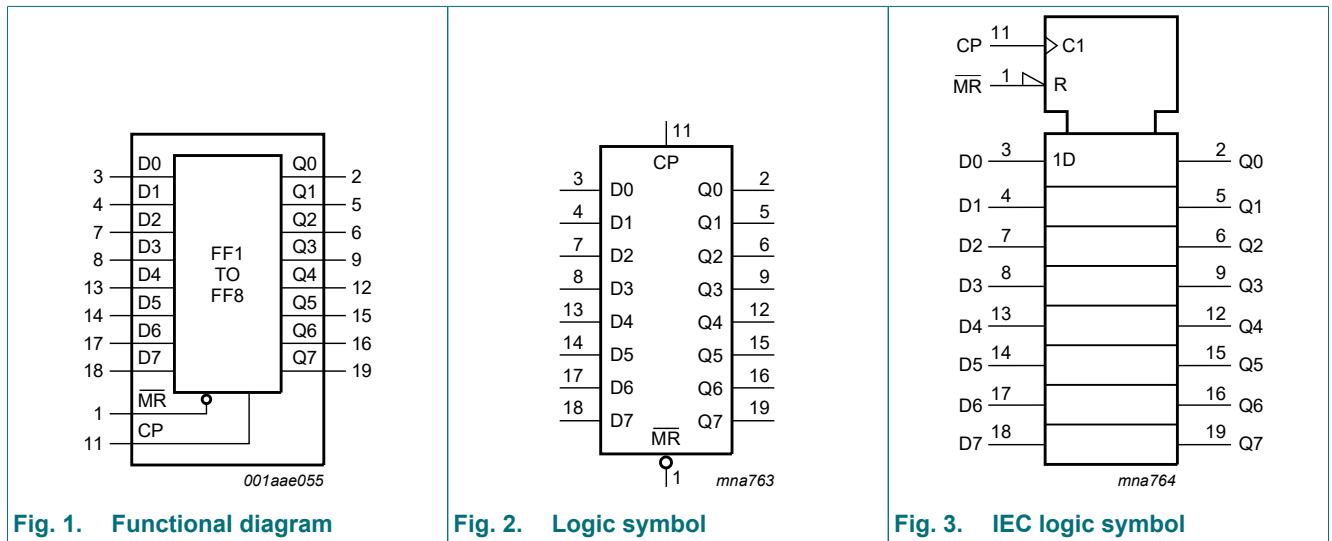
- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- Input levels:
 - For 74HC273-Q100: CMOS level
 - For 74HCT273-Q100: TTL level
- Common clock and master reset
- Eight positive edge-triggered D-type flip-flops
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC273D-Q100	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HCT273D-Q100				
74HC273PW-Q100	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74HCT273PW-Q100				
74HC273BQ-Q100	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1
74HCT273BQ-Q100				

4. Functional diagram



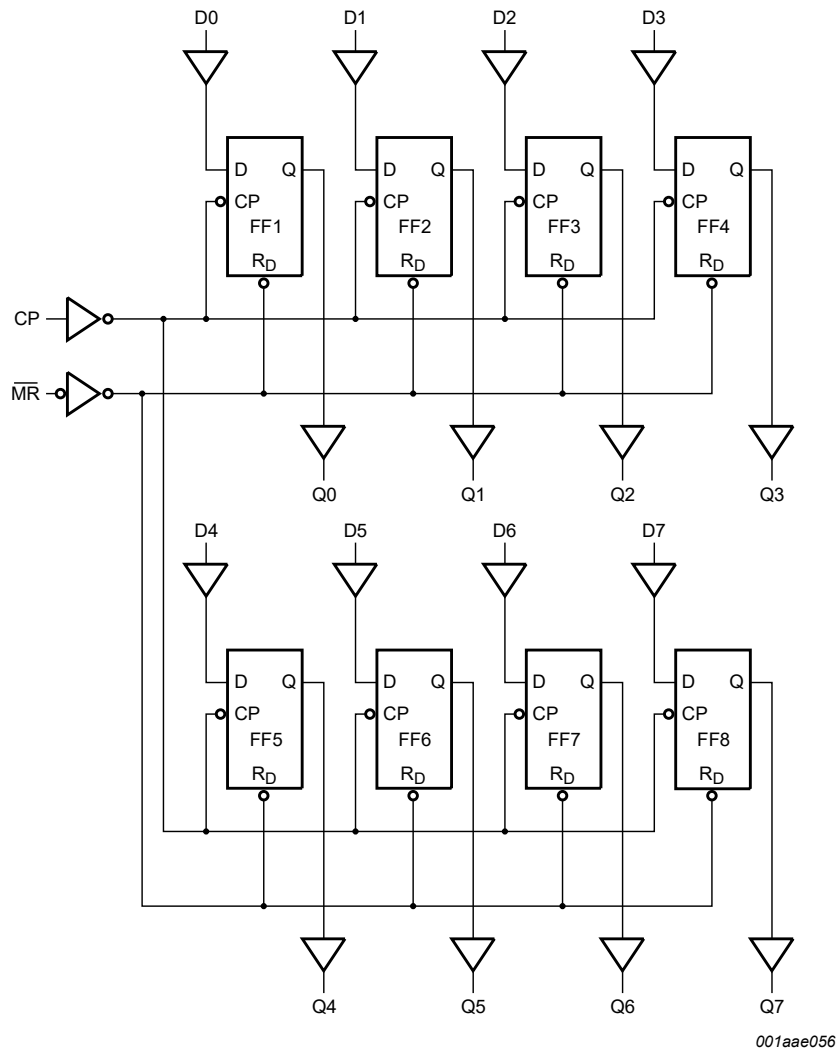
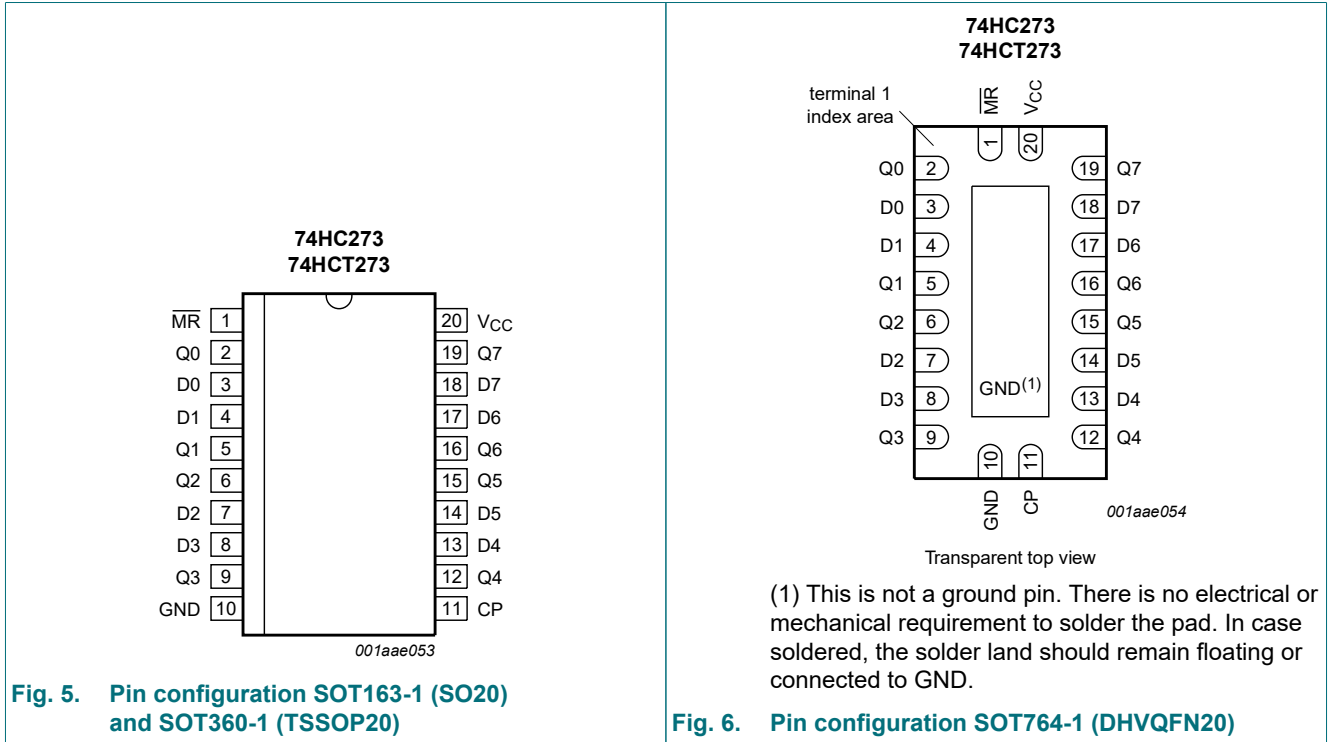


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
MR	1	master reset input (active LOW)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	2, 5, 6, 9, 12, 15, 16, 19	flip-flop output
D0, D1, D2, D3, D4, D5, D6, D7	3, 4, 7, 8, 13, 14, 17, 18	data input
GND	10	ground (0 V)
CP	11	clock input (LOW-to-HIGH, edge-triggered)
VCC	20	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
X = don't care; ↑ = LOW-to-HIGH clock transition.

Operating modes	Inputs			Outputs
	MR	CP	Dn	Qn
reset (clear)	L	X	X	L
load "1"	H	↑	h	H
load "0"	H	↑	l	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V [1]	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V [1]	-	±20	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C.

For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.

For SOT764-1 (DHVQFN20) package: P_{tot} derates linearly with 12.9 mW/K above 111 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC273-Q100			74HCT273-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC273-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V		
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V		
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

Octal D-type flip-flop with reset; positive-edge trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT273-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 5.2 mA; V _{CC} = 5.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1	-	±1	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V								
		MR input	-	100	360	-	450	-	490	µA
		CP input	-	175	630	-	787.5	-	857.5	µA
		Dn input	-	15	54	-	67.5	-	73.5	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Fig. 10

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC273-Q100										
t _{pd}	propagation delay	CP to Qn; see Fig. 7 [1]								
		V _{CC} = 2.0 V	-	41	150	-	185	-	225	ns
		V _{CC} = 4.5 V	-	15	30	-	37	-	45	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	15	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	13	26	-	31	-	38	ns
t _{PHL}	HIGH to LOW propagation delay	MR to Qn; see Fig. 8								
		V _{CC} = 2.0 V	-	44	150	-	185	-	225	ns
		V _{CC} = 4.5 V	-	16	30	-	37	-	45	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	15	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	14	26	-	31	-	38	ns

Octal D-type flip-flop with reset; positive-edge trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_t	transition time	Qn output; see Fig. 7 [2]								
		$V_{CC} = 2.0\text{ V}$	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5\text{ V}$	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0\text{ V}$	-	6	13	-	15	-	19	ns
t_W	pulse width	CP input HIGH or LOW; see Fig. 7								
		$V_{CC} = 2.0\text{ V}$	80	14	-	100	-	120	-	ns
		$V_{CC} = 4.5\text{ V}$	16	5	-	20	-	24	-	ns
		$V_{CC} = 6.0\text{ V}$	14	4	-	17	-	20	-	ns
		MR input LOW; see Fig. 8								
		$V_{CC} = 2.0\text{ V}$	60	17	-	75	-	90	-	ns
		$V_{CC} = 4.5\text{ V}$	12	6	-	15	-	18	-	ns
$V_{CC} = 6.0\text{ V}$	10	5	-	13	-	15	-	ns		
t_{rec}	recovery time	MR to CP; see Fig. 8								
		$V_{CC} = 2.0\text{ V}$	50	-6	-	65	-	75	-	ns
		$V_{CC} = 4.5\text{ V}$	10	-2	-	13	-	15	-	ns
		$V_{CC} = 6.0\text{ V}$	9	-2	-	11	-	13	-	ns
t_{su}	set-up time	Dn to CP; see Fig. 9								
		$V_{CC} = 2.0\text{ V}$	60	11	-	75	-	90	-	ns
		$V_{CC} = 4.5\text{ V}$	12	4	-	15	-	18	-	ns
		$V_{CC} = 6.0\text{ V}$	10	3	-	13	-	15	-	ns
t_h	hold time	Dn to CP; see Fig. 9								
		$V_{CC} = 2.0\text{ V}$	3	-6	-	3	-	3	-	ns
		$V_{CC} = 4.5\text{ V}$	3	-2	-	3	-	3	-	ns
		$V_{CC} = 6.0\text{ V}$	3	-2	-	3	-	3	-	ns
f_{max}	maximum frequency	CP input; see Fig. 7								
		$V_{CC} = 2.0\text{ V}$	6	20.6	-	4.8	-	4	-	MHz
		$V_{CC} = 4.5\text{ V}$	30	103	-	24	-	20	-	MHz
		$V_{CC} = 5.0\text{ V}; C_L = 15\text{ pF}$	-	66	-	-	-	-	-	MHz
		$V_{CC} = 6.0\text{ V}$	35	122	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	per package; $V_I = \text{GND to } V_{CC}$ [3]	-	20	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT273-Q100										
t _{pd}	propagation delay	CP to Qn; see Fig. 7 [1]								
		V _{CC} = 4.5 V	-	16	30	-	38	-	45	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	15	-	-	-	-	-	ns
t _{PHL}	HIGH to LOW propagation delay	MR to Qn; see Fig. 8								
		V _{CC} = 4.5 V	-	23	34	-	43	-	51	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	20	-	-	-	-	-	ns
t _t	transition time	Qn output; see Fig. 7 [2]								
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t _W	pulse width	CP input; see Fig. 7								
		V _{CC} = 4.5 V	16	9	-	20	-	24	-	ns
		MR input LOW; see Fig. 8								
t _{rec}	recovery time	MR to CP; see Fig. 8								
		V _{CC} = 4.5 V	10	-2	-	13	-	15	-	ns
t _{su}	set-up time	Dn to CP; see Fig. 9								
		V _{CC} = 4.5 V	12	5	-	15	-	18	-	ns
t _h	hold time	Dn to CP; see Fig. 9								
		V _{CC} = 4.5 V	3	-4	-	3	-	3	-	ns
f _{max}	maximum frequency	CP input; see Fig. 7								
		V _{CC} = 4.5 V	30	56	-	24	-	20	-	MHz
		V _{CC} = 5.0 V; C _L = 15 pF	-	36	-	-	-	-	-	MHz
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} - 1.5 V [3]	-	23	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

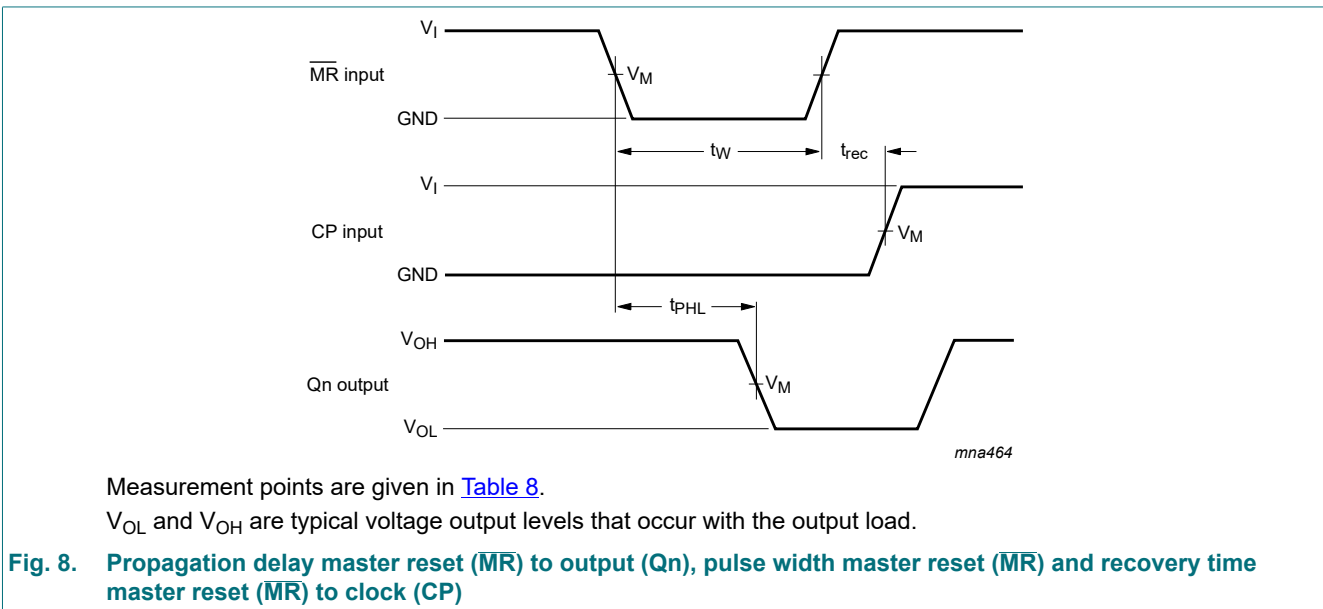
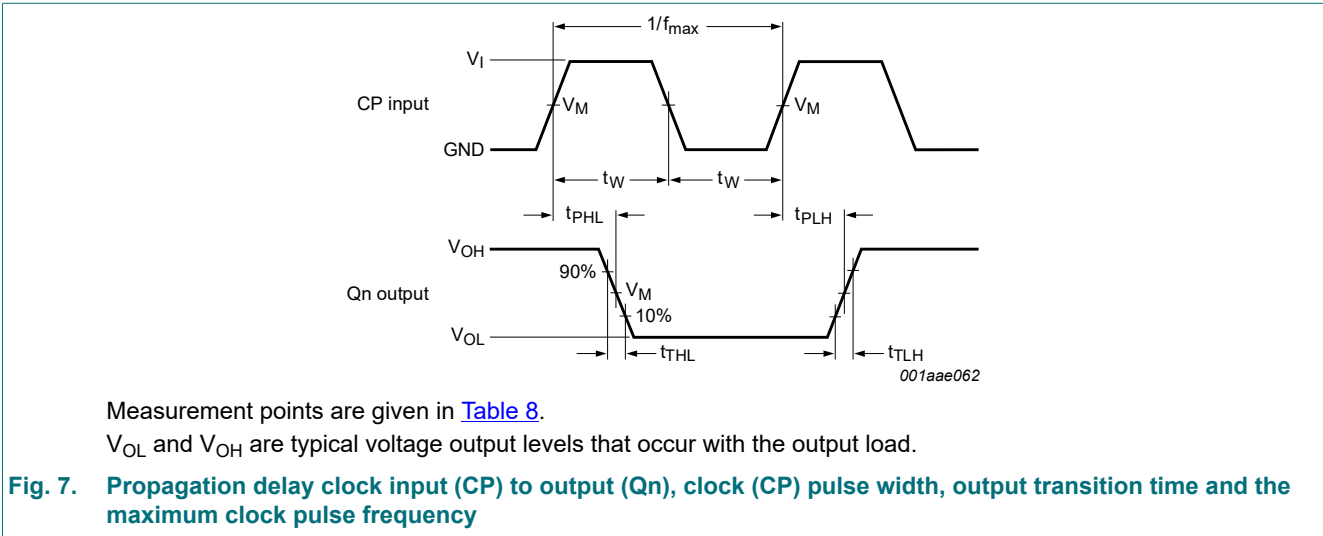
f_o = output frequency in MHz;

∑ (C_L × V_{CC}² × f_o) = sum of outputs;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V.

10.1. Waveforms and test circuit



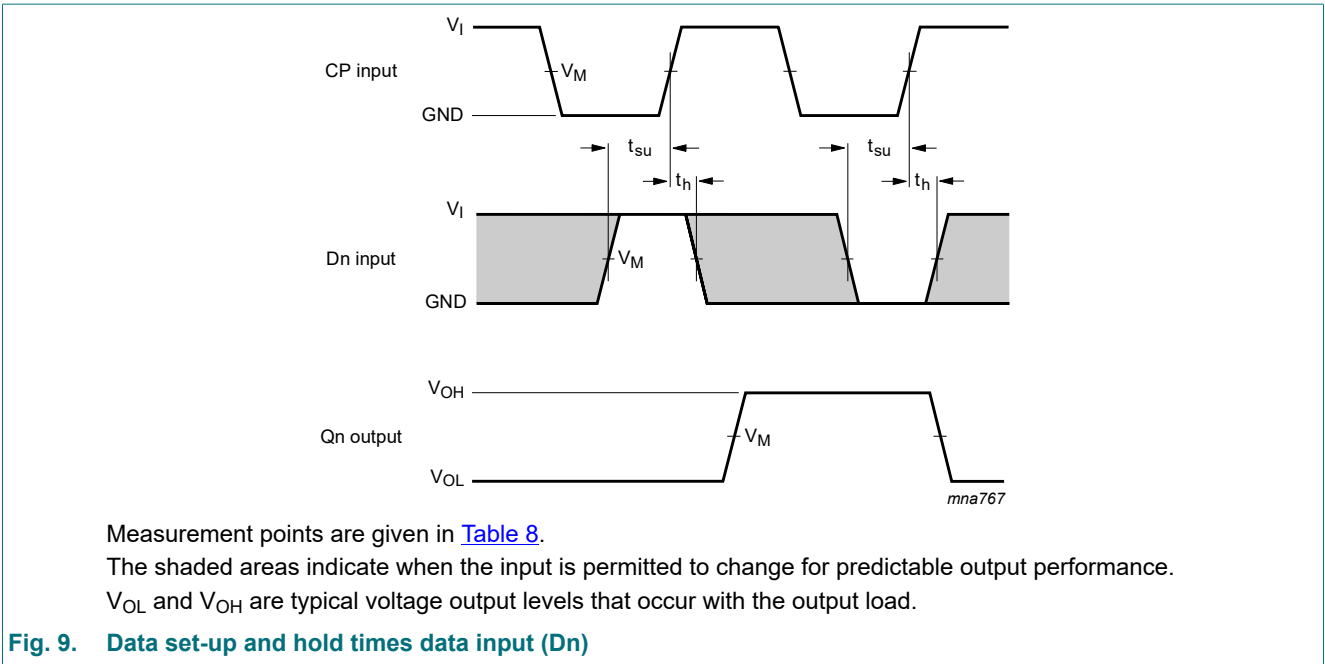


Table 8. Measurement points

Type	Input		Output
	V_I	V_M	V_M
74HC273-Q100	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$
74HCT273-Q100	3 V	1.3 V	1.3 V

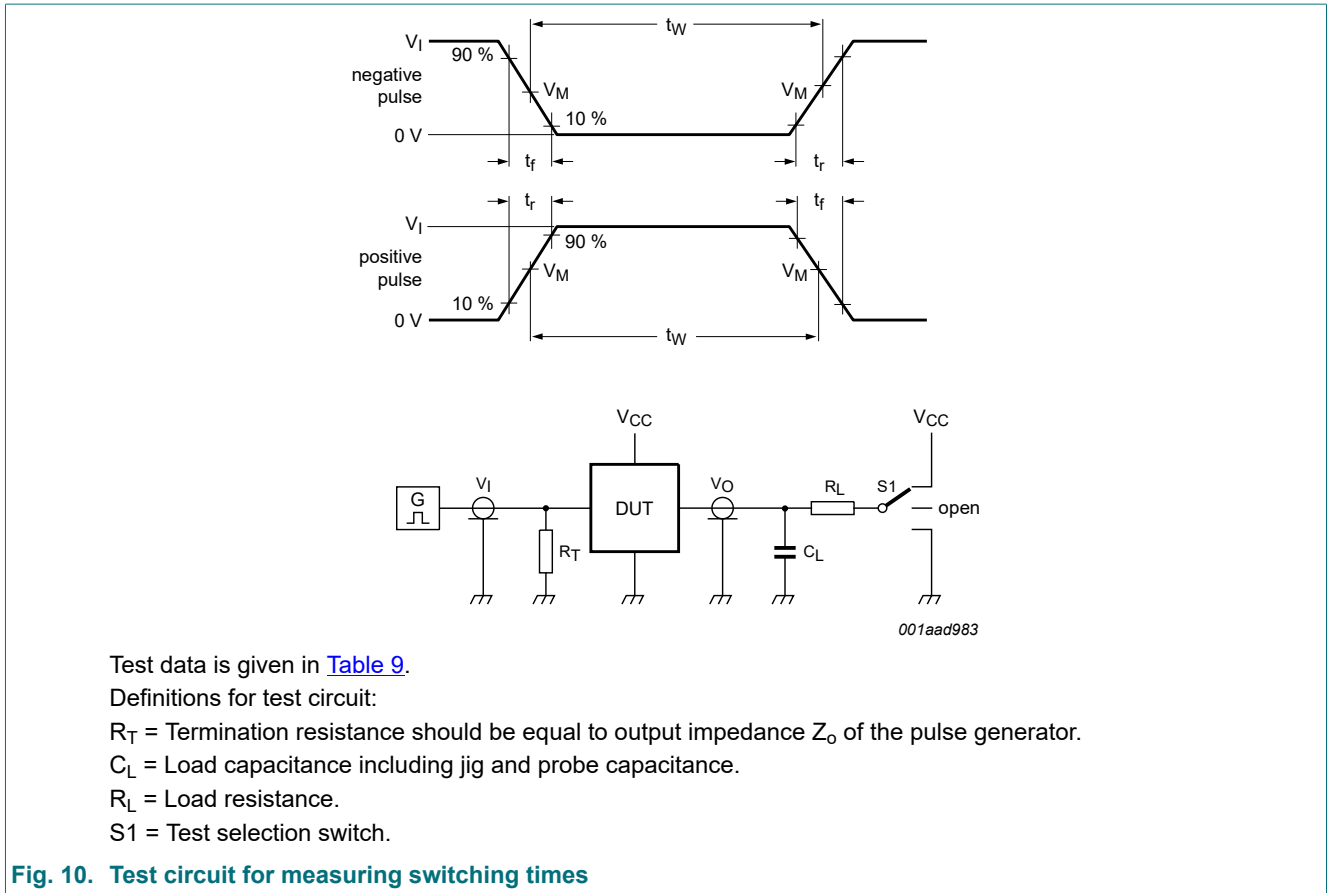


Table 9. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC273-Q100	V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	open
74HCT273-Q100	3 V	6 ns	15 pF, 50 pF	1 k Ω	open

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

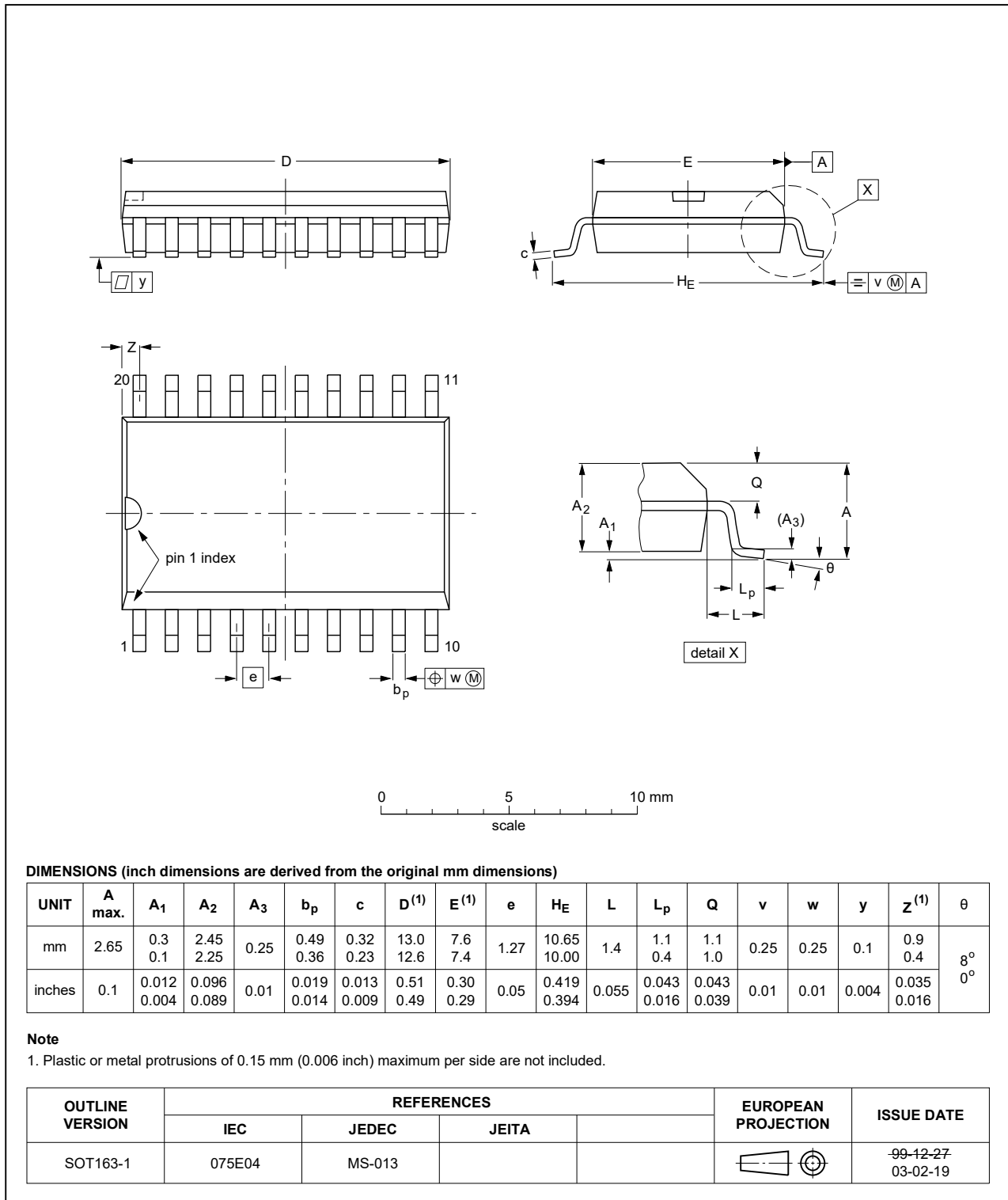


Fig. 11. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

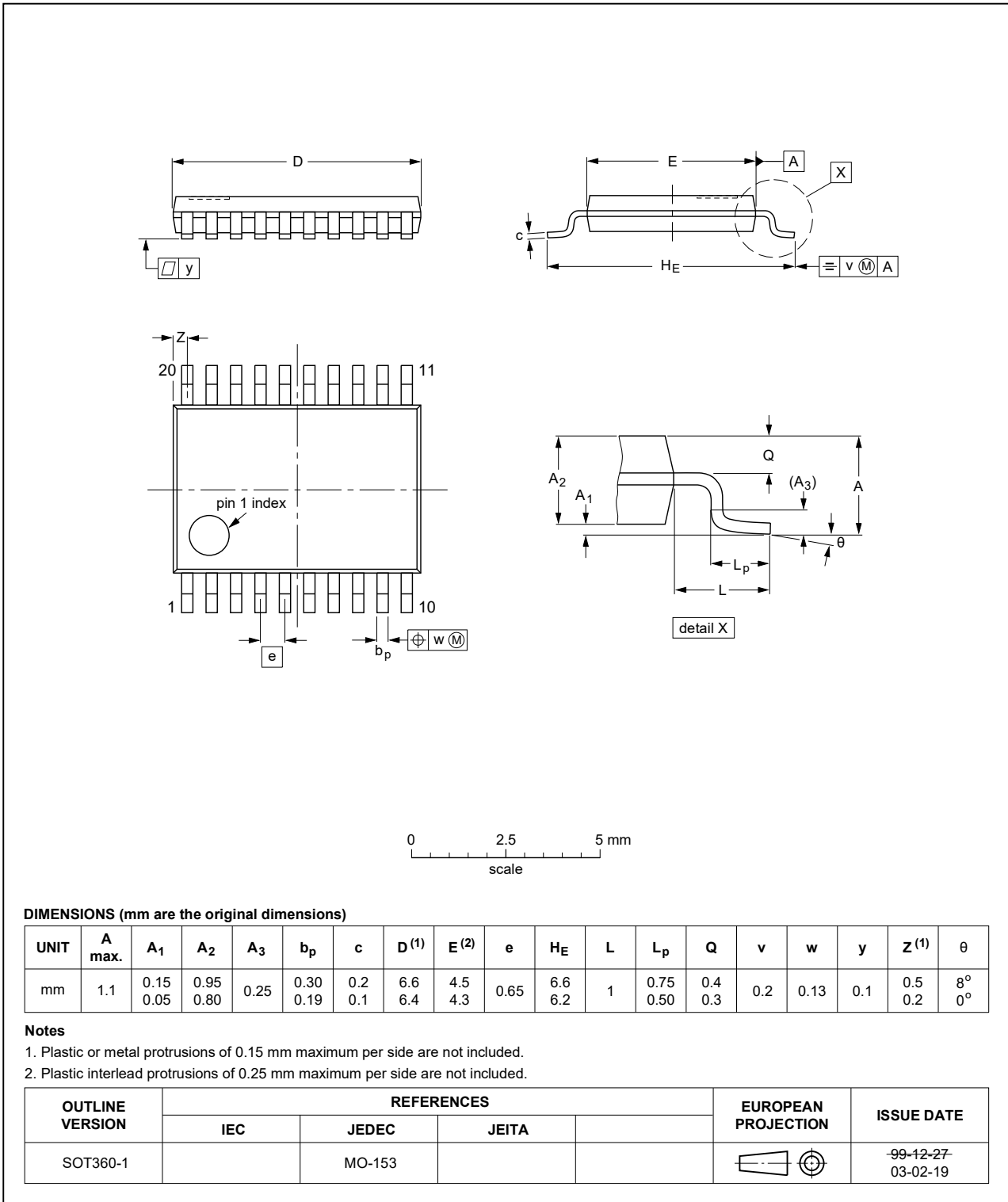


Fig. 12. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

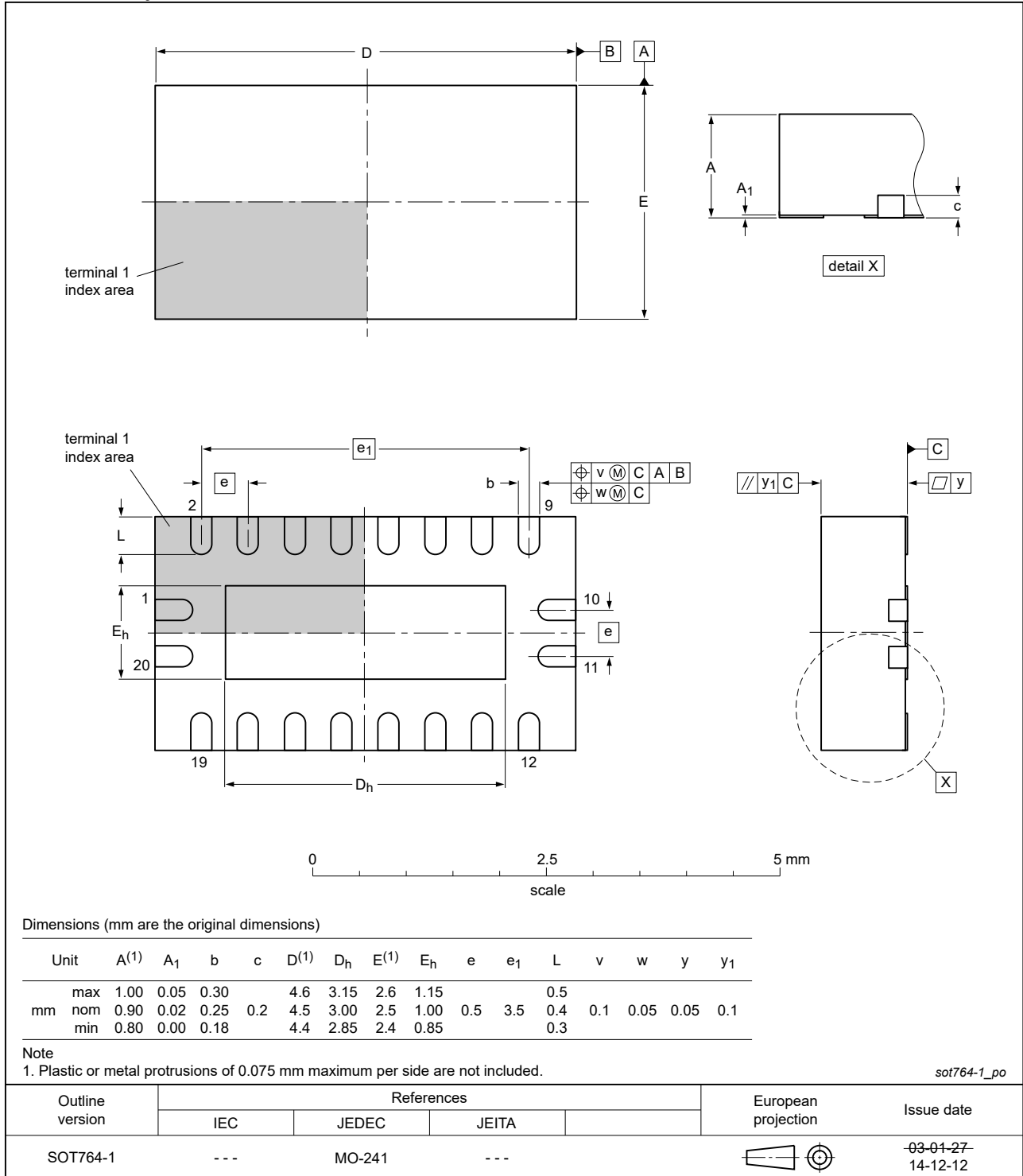


Fig. 13. Package outline SOT764-1 (DHVQFN20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT273_Q100 v.2	20200903	Product data sheet	-	74HC_HCT273_Q100 v.1
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 2 updated. Table 4: Derating values for P_{tot} total power dissipation have been updated. Package outline drawing of SOT764-1 (Fig. 13) updated. 			
74HC_HCT273_Q100 v.1	20130619	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Contents

1. General description	1
2. Features and benefits	1
3. Ordering information	2
4. Functional diagram	2
5. Pinning information	4
5.1. Pinning.....	4
5.2. Pin description.....	4
6. Functional description	5
7. Limiting values	5
8. Recommended operating conditions	5
9. Static characteristics	6
10. Dynamic characteristics	7
10.1. Waveforms and test circuit.....	10
11. Package outline	13
12. Abbreviations	16
13. Revision history	16
14. Legal information	17

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