



THE DATASHEET OF BUK9K13-60RAX





BUK9K13-60RA

Dual N-channel 60 V, 12.5 mOhm logic level MOSFET in LFPAK56D using Repetitive Avalanche technology

2 December 2020

Product data sheet

1. General description

Dual, logic level N-channel MOSFET in an LFPAK56D package, using Application Specific (ASFET) repetitive avalanche silicon technology. This product has been designed and qualified to AEC-Q101 for use in repetitive avalanche applications.

2. Features and benefits

- Fully automotive qualified to AEC-Q101 at 175 °C
- Repetitive Avalanche rated to 30 °C T_j rise:
 - Tested to 1 Bn avalanche events
- LFPAK copper clip package technology:
 - High robustness and reliability
 - Gull wing leads for high manufacturability and AOI

3. Applications

- 12 V, 24 V and 48 V automotive systems
- Repetitive avalanche topologies
- Engine control
- Transmission control
- Actuator and auxiliary loads

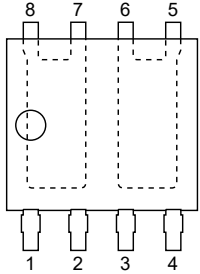
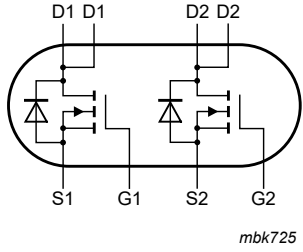
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	60	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	40	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	64	W
Static characteristics FET1 and FET2						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 10\text{ A}$; $T_j = 25\text{ °C}$; Fig. 14	6.1	10	12.5	mΩ
Dynamic characteristics FET1 and FET2						
Q_{GD}	gate-drain charge	$I_D = 10\text{ A}$; $V_{DS} = 48\text{ V}$; $V_{GS} = 5\text{ V}$; $T_j = 25\text{ °C}$; Fig. 16 ; Fig. 17	-	7.9	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>LFAK56D; Dual LFAK (SOT1205)</p>	 <p>mbk725</p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK9K13-60RA	LFAK56D; Dual LFAK	plastic, single ended surface mounted package (LFAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9K13-60RA	91360RA

8. Limiting values

Table 5. Limiting values

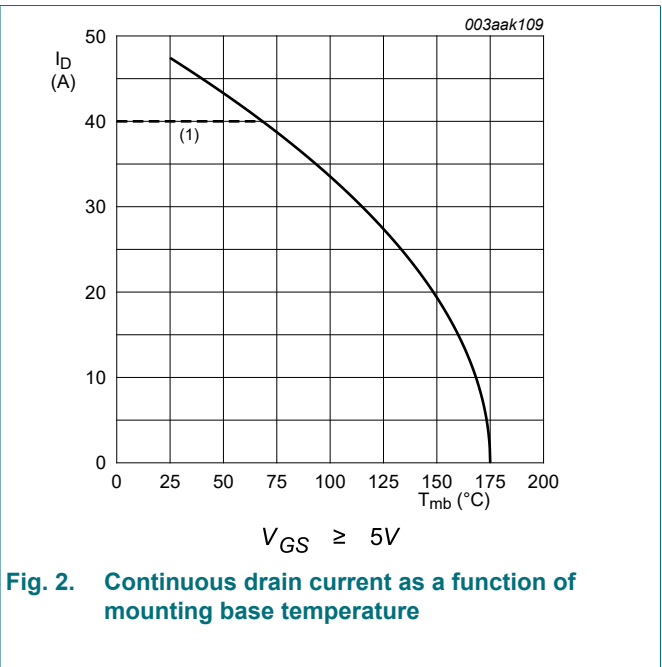
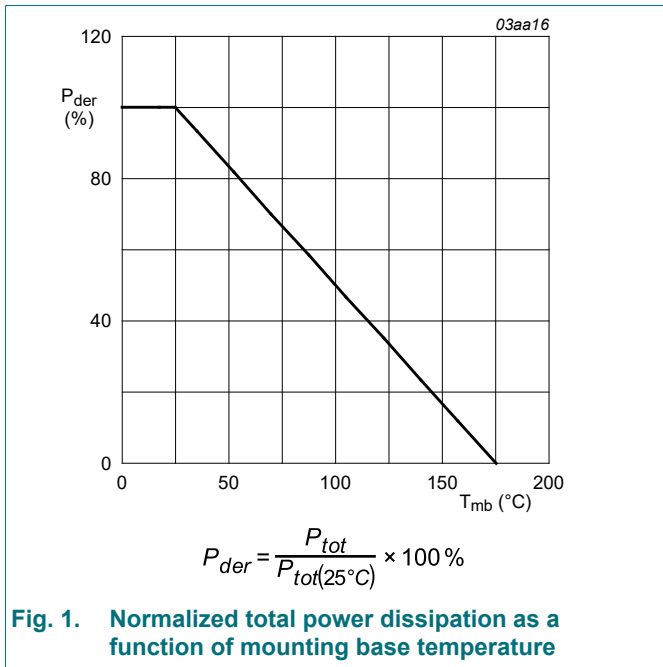
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	60	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	60	V
V_{GS}	gate-source voltage	DC; $T_j \leq 175\text{ °C}$	-10	10	V
		Pulsed; $T_j \leq 175\text{ °C}$	[1] [2] -15	15	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	64	W
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	40	A
		$V_{GS} = 5\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	-	33	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	190	A
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
I_S	source current	$T_{mb} = 25\text{ °C}$	-	40	A

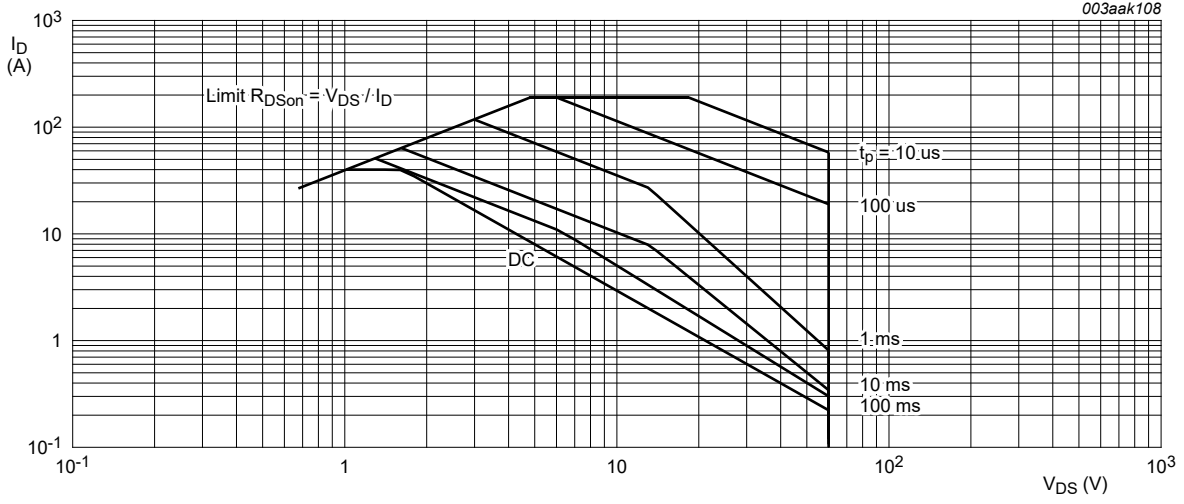
Dual N-channel 60 V, 12.5 mOhm logic level MOSFET in LPAK56D using Repetitive Avalanche technology

Symbol	Parameter	Conditions	Min	Max	Unit
I_{SM}	peak source current	pulsed; $t_p \leq 10 \mu s$; $T_{mb} = 25 \text{ }^\circ\text{C}$	-	190	A
Avalanche ruggedness					
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	$I_D = 1.92 \text{ A}$; $V_{sup} \leq 60 \text{ V}$; $R_{GS} = 10 \Omega$; $V_{GS} = 10 \text{ V}$; $T_{j(rise)} \leq 30 \text{ }^\circ\text{C}$; unclamped; Fig. 4; Fig. 5; Fig. 6	[3] [4] [5]	-	75.2 mJ
Avalanche Ruggedness FET1 and FET2					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 40 \text{ A}$; $V_{sup} \leq 60 \text{ V}$; $R_{GS} = 50 \Omega$; $V_{GS} = 5 \text{ V}$; $T_{j(init)} = 25 \text{ }^\circ\text{C}$; unclamped; Fig. 7	[6] [7]	-	82 mJ

- [1] Accumulated Pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T_j and or V_{GS} .
- [3] Repetitive avalanche rating is limited by maximum junction temperature of 175 °C and junction rise of 30 °C
- [4] Refer to Fig. 5 for the limiting number of avalanche events
- [5] Refer to Fig. 6 R_{dson} at $V_{gs}=5V$ will increase as a function of repetitive avalanche cycles
- [6] Refer to application note AN10273 for further information
- [7] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C

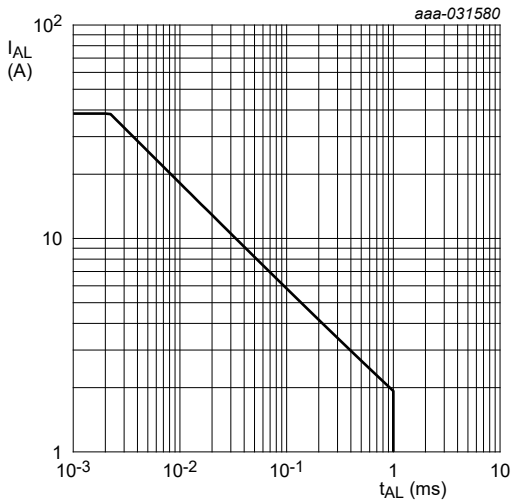


Dual N-channel 60 V, 12.5 mOhm logic level MOSFET in LPAK56D using Repetitive Avalanche technology



$T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



T_j is limited to $175^{\circ}C$ and $T_{j(rise)}$ is limited to $30^{\circ}C$

Fig. 4. Repetitive avalanche rating; avalanche current as a function of avalanche time

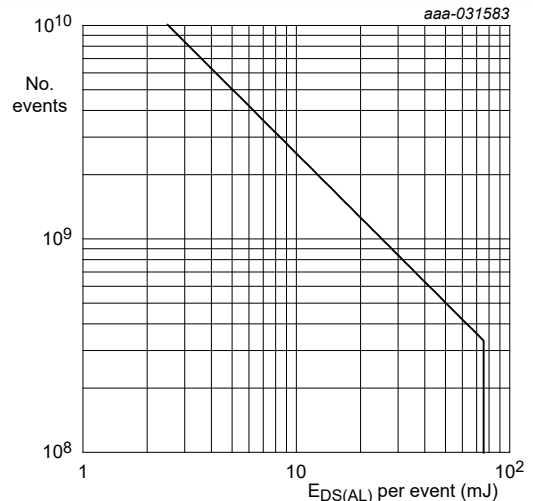


Fig. 5. Repetitive avalanche rating; maximum number of avalanche events as a function of avalanche energy

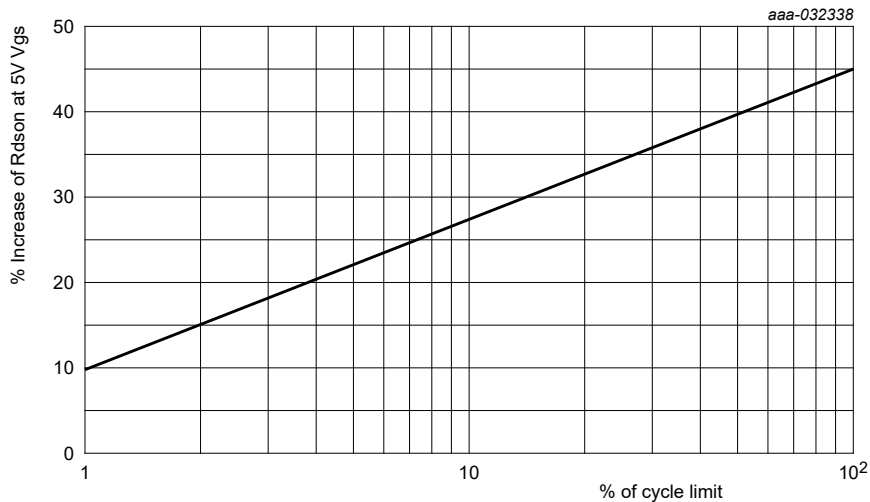
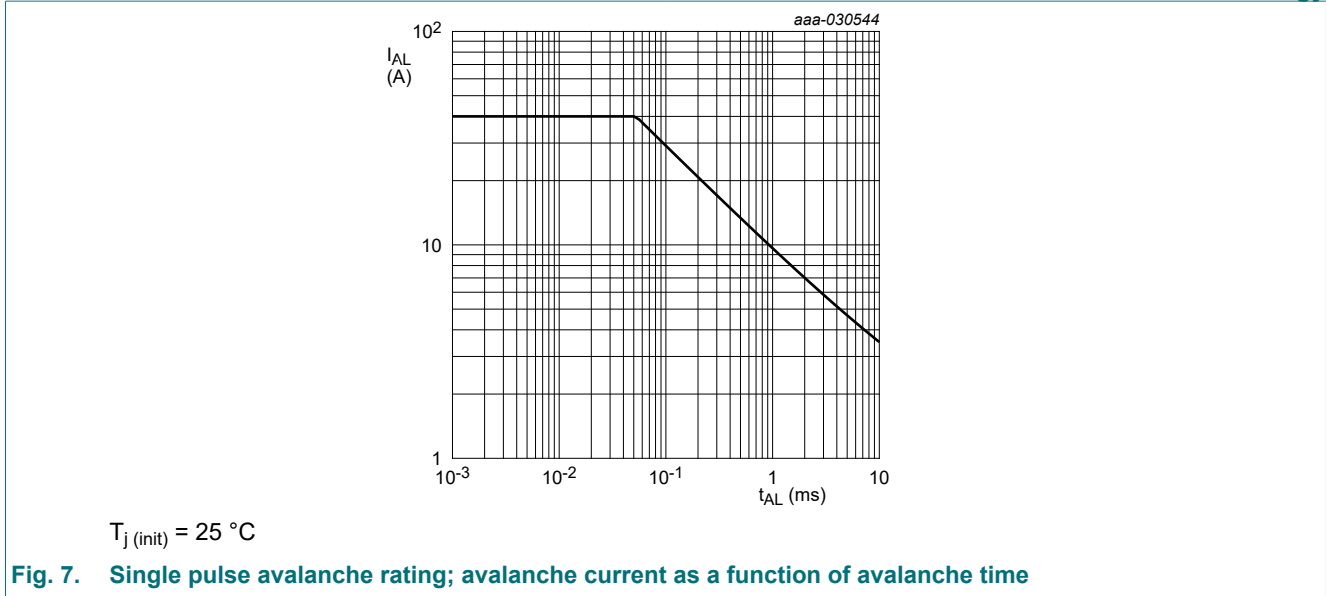


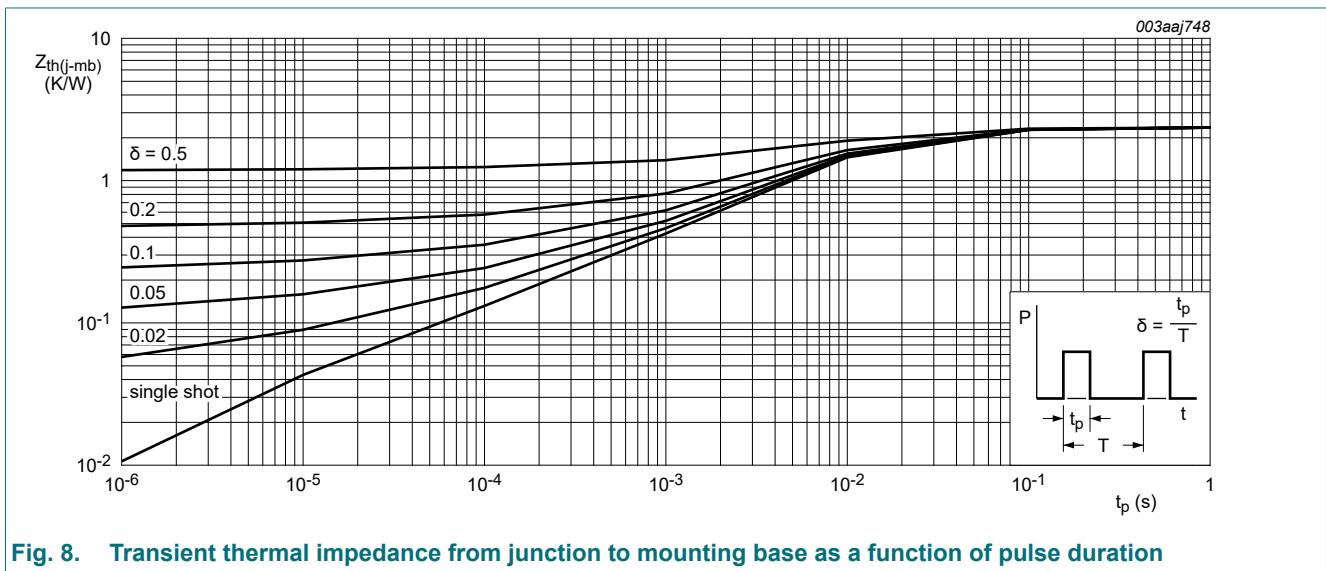
Fig. 6. Percentage $R_{ds(on)}$ at 5V increase as a function of avalanche cycles



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 8	-	-	2.36	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics FET1 and FET2						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	54	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 12 ; Fig. 13	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ Fig. 12	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ Fig. 12	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	1	μA
		$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 14	6.1	10	12.5	m Ω
		$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ Fig. 14 ; Fig. 15	-	22	28.3	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 14	5.4	9	11.2	m Ω
Dynamic characteristics FET1 and FET2						
$Q_{G(tot)}$	total gate charge	$I_D = 10 \text{ A}; V_{DS} = 48 \text{ V}; V_{GS} = 5 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 16 ; Fig. 17	-	22.4	-	nC
Q_{GS}	gate-source charge		-	5.2	-	nC
Q_{GD}	gate-drain charge		-	7.9	-	nC
C_{iss}	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 18	-	2215	2953	pF
C_{oss}	output capacitance		-	225	270	pF
C_{rss}	reverse transfer capacitance		-	116	159	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 48 \text{ V}; R_L = 5 \text{ } \Omega; V_{GS} = 5 \text{ V}; R_{G(ext)} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	13	-	ns
t_r	rise time		-	22.1	-	ns
$t_{d(off)}$	turn-off delay time		-	30.5	-	ns
t_f	fall time		-	21.8	-	ns
Source-drain diode FET1 and FET2						
V_{SD}	source-drain voltage	$I_S = 10 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 19	-	0.78	1.2	V
t_{rr}	reverse recovery time	$I_S = 10 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	22.7	-	ns
Q_r	recovered charge		-	18.9	-	nC

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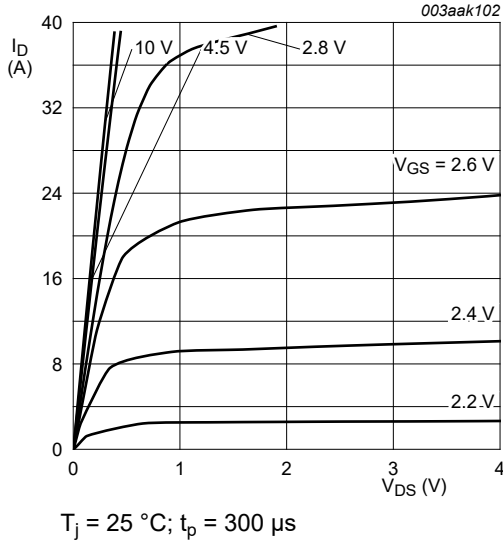


Fig. 9. Output characteristics; drain current as a function of drain-source voltage; typical values

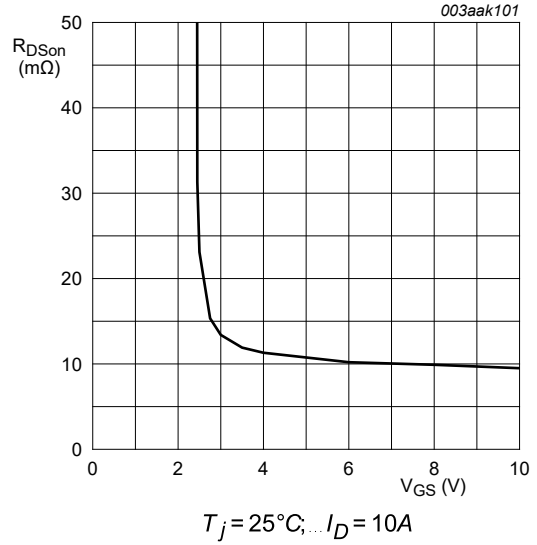


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values

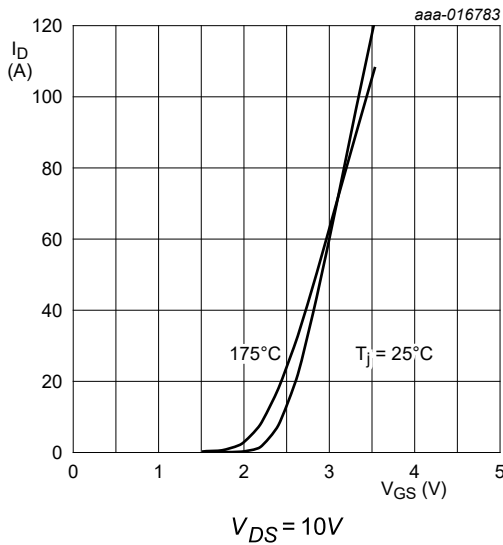


Fig. 11. Transfer characteristics; drain current as a function of gate-source voltage; typical values

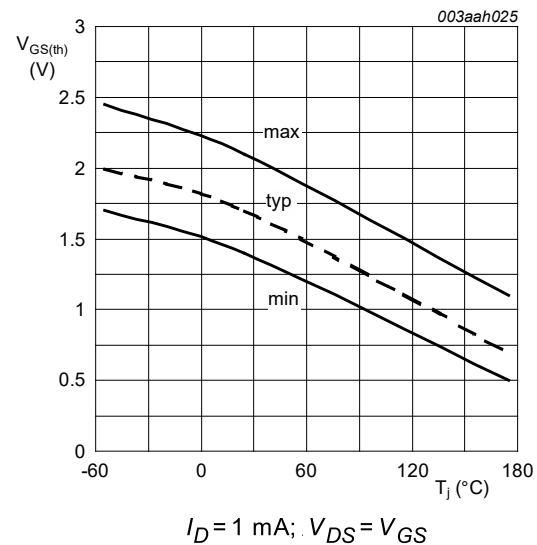


Fig. 12. Gate-source threshold voltage as a function of junction temperature

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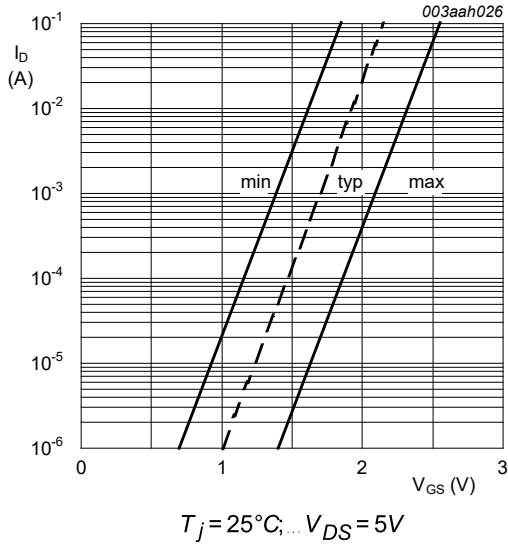


Fig. 13. Sub-threshold drain current as a function of gate-source voltage

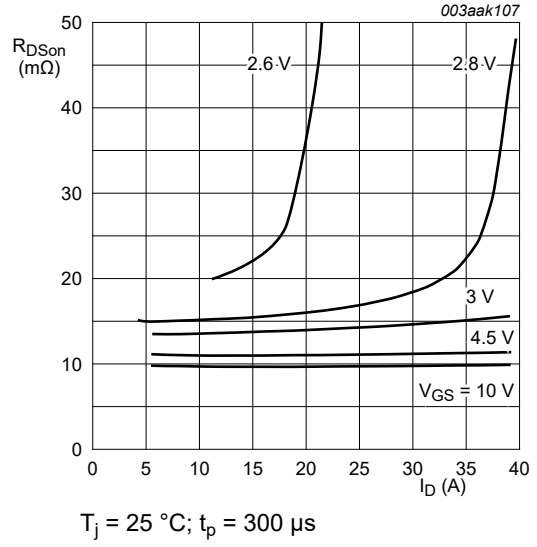


Fig. 14. Drain-source on-state resistance as a function of drain current; typical values

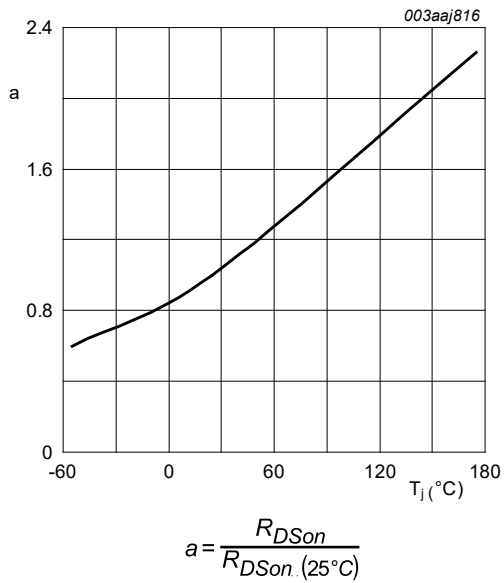


Fig. 15. Normalized drain-source on-state resistance factor as a function of junction temperature

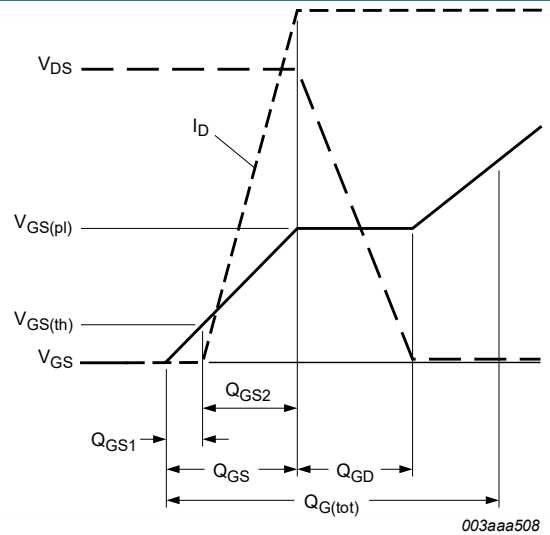


Fig. 16. Gate charge waveform definitions

Dual N-channel 60 V, 12.5 mOhm logic level MOSFET in LPAK56D using Repetitive Avalanche technology

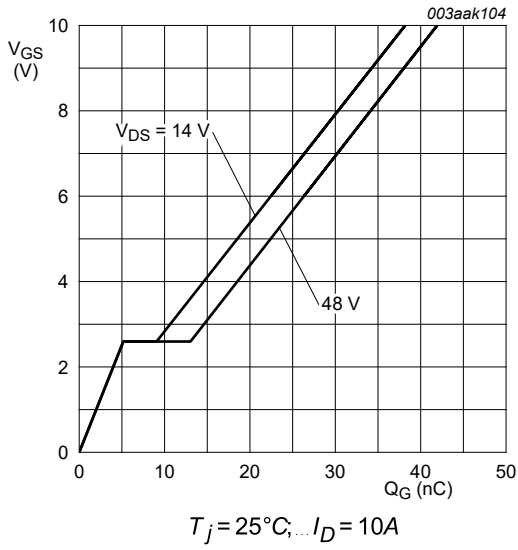


Fig. 17. Gate-source voltage as a function of gate charge; typical values

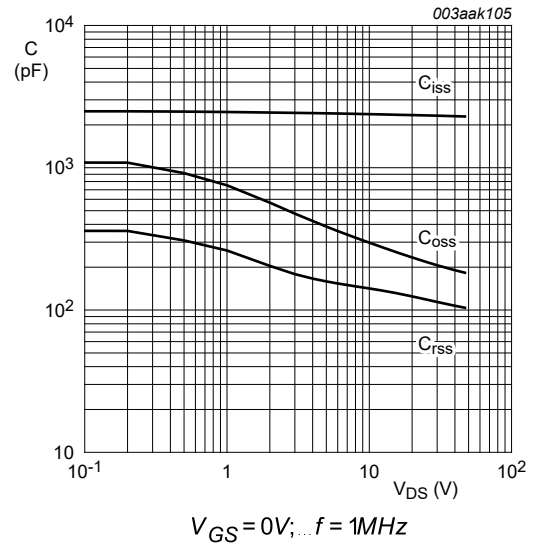


Fig. 18. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

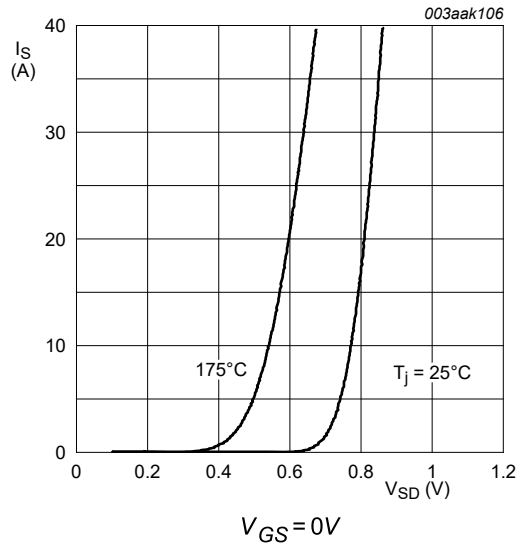


Fig. 19. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

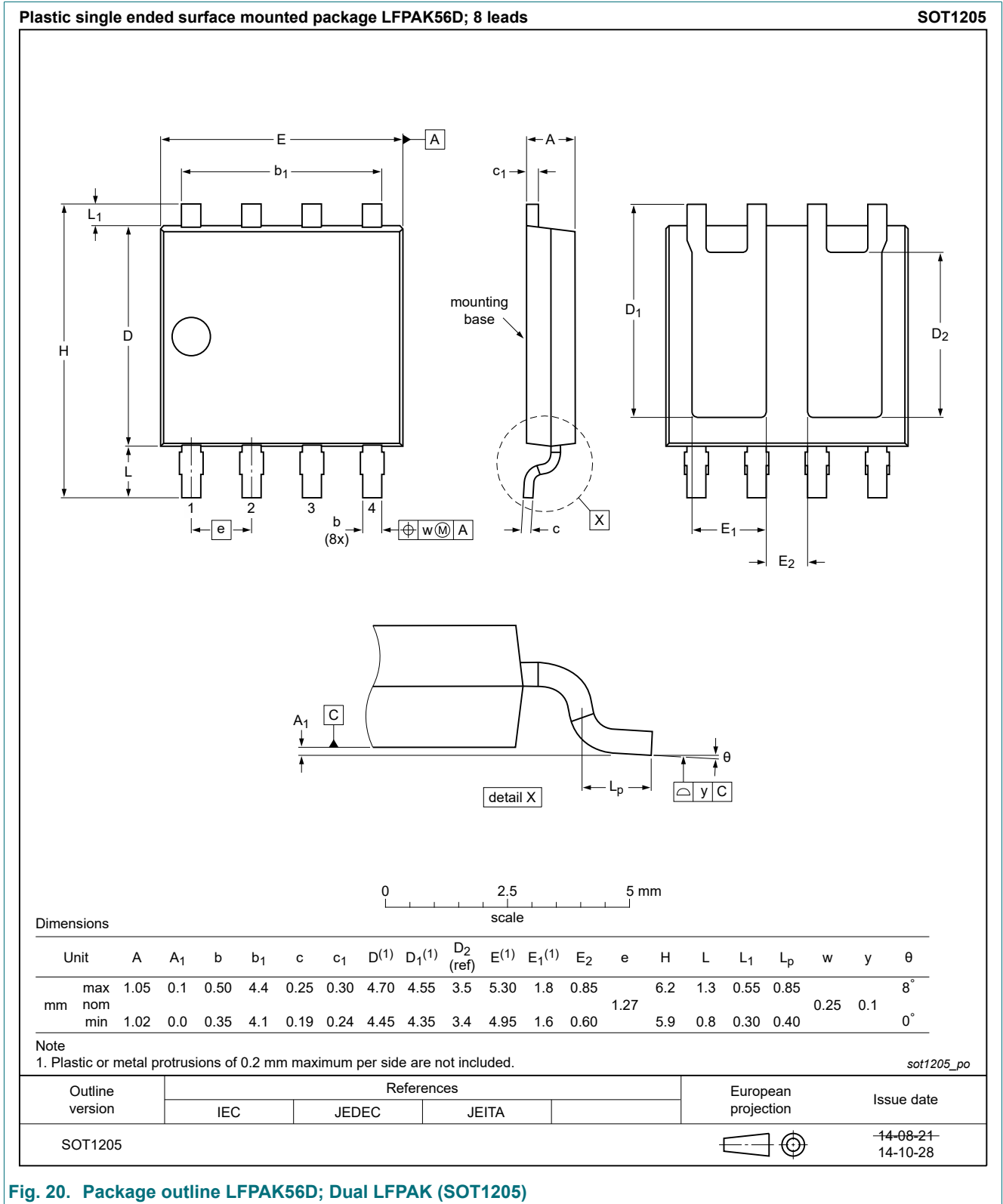


Fig. 20. Package outline LPAK56D; Dual LPAK (SOT1205)

12. Soldering

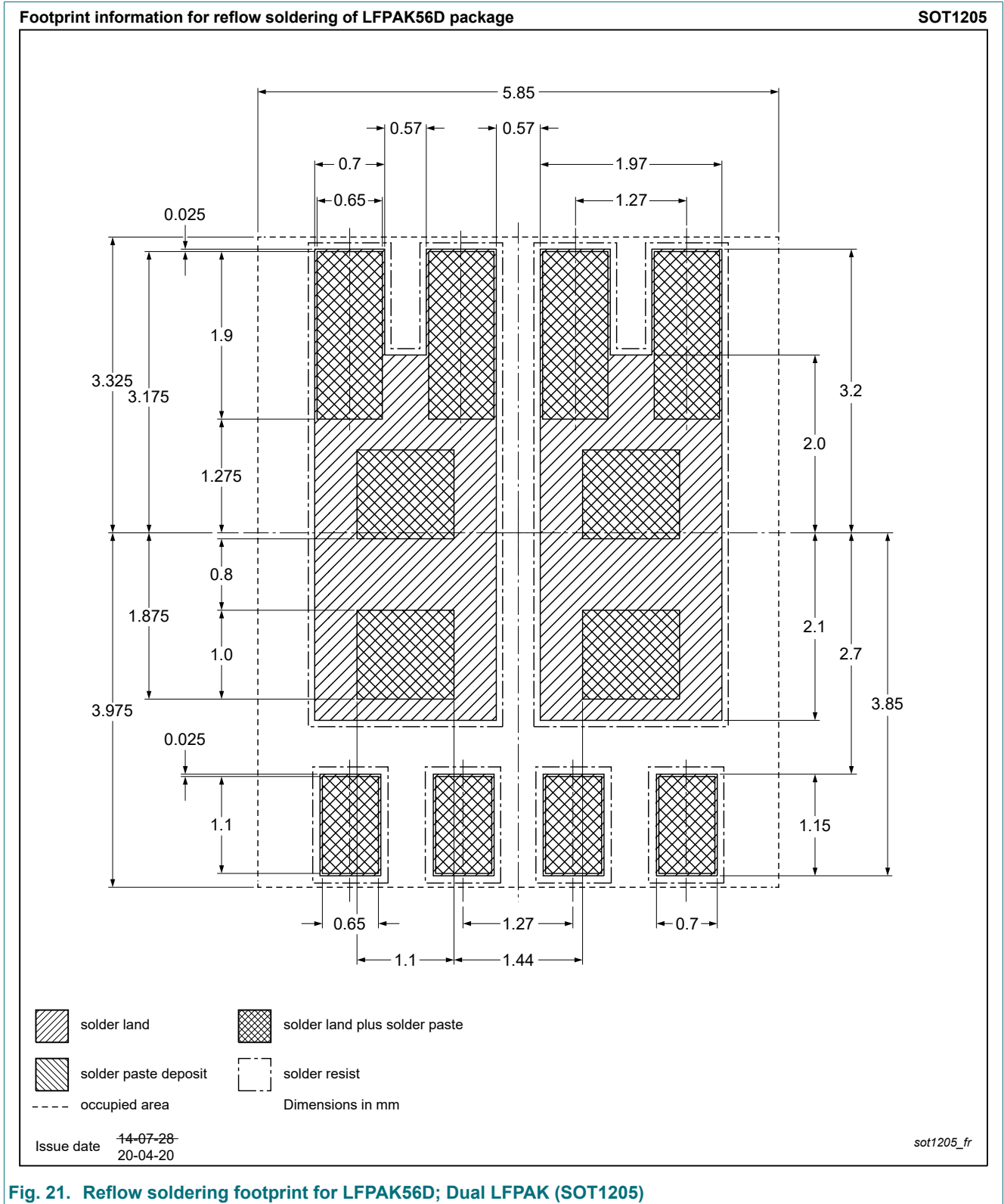


Fig. 21. Reflow soldering footprint for LPAK56D; Dual LPAK (SOT1205)

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13. Legal information

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Document status [1][2]	Product status [3]	Definition
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