



**THE DATASHEET OF
ADRV9002BBCZ**



Dual Narrow-Band and Wideband RF Transceiver

FEATURES

- ▶ 2 × 2 highly integrated transceiver
- ▶ Frequency range of 30 MHz to 6000 MHz
- ▶ Transmitter and receiver bandwidth from 12 kHz to 40 MHz
- ▶ Two fully integrated, fractional-N, RF synthesizers
- ▶ LVDS and CMOS synchronous serial data interface options
- ▶ Low power monitor and sleep modes
- ▶ Multichip synchronization capabilities
- ▶ Fast frequency hopping
- ▶ Dynamic profile switching for dynamic data rates and sample rates
- ▶ Fully integrated DPD for narrow-band and wideband waveforms
- ▶ Fully programmable via a 4-wire SPI
- ▶ 12 mm × 12 mm, 196-ball CSP_BGA

APPLICATIONS

- ▶ Mission critical communications
- ▶ Very high frequency (VHF), ultrahigh frequency (UHF), and cellular to 6 GHz
- ▶ Time division duplexing (TDD) and frequency division duplexing (FDD) applications

GENERAL DESCRIPTION

The ADRV9002 is a highly integrated RF transceiver that has dual-channel transmitters, dual-channel receivers, integrated synthesizers, and digital signal processing functions.

The ADRV9002 is a high performance, highly linear, high dynamic range transceiver designed for performance vs. power consumption system optimization. The device is configurable and ideally suited to demanding, low power, portable and battery powered equipment. The ADRV9002 operates from 30 MHz to 6000 MHz and covers the UHF, VHF, industrial, scientific, and medical (ISM) bands, and cellular frequency bands in narrow-band (kHz) and wideband operation up to 40 MHz. The ADRV9002 is capable of both TDD and FDD operation.

The transceiver consists of direct conversion signal paths with state-of-the-art noise figure and linearity. Each complete receiver and transmitter subsystem includes dc offset correction, quadrature error correction (QEC), and programmable digital filters, which eliminate the need for these functions in the digital baseband. In addition, several auxiliary functions, such as auxiliary analog-to-digital converters (ADCs), auxiliary digital-to-analog converters (DACs), and general-purpose inputs/outputs (GPIOs), are integrated to provide additional monitoring and control capability.

The fully integrated phase-locked loops (PLLs) provide high performance, low power, fractional-N frequency synthesis for the transmitter, receiver, and clock sections. Careful design and layout techniques provide the isolation required in high performance personal radio applications.

All voltage controlled oscillator (VCO) and loop filter components are integrated to minimize the external component count. The local oscillators (LOs) have flexible configuration options and include fast lock modes.

The transceiver includes low power sleep and monitor modes to save power and extend the battery life of portable devices while monitoring communications.

The fully integrated, low power digital predistortion (DPD) is optimized for both narrow-band and wideband signals and enables linearization of high efficiency power amplifiers.

The ADRV9002 core can be powered directly from 1.0 V, 1.3 V, and 1.8 V regulators and is controlled via a standard 4-wire serial port. Other voltage supplies are used to provide proper digital interface levels and to optimize the receiver, transmitter, and auxiliary converter performance.

High data rate and low data rate interfaces are supported using configurable CMOS or low voltage differential signaling (LVDS) serial synchronous interface (SSI) choice.

The ADRV9002 is packaged in a 12 mm × 12 mm, 196-ball chip scale package ball grid array (CSP_BGA).

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REVISION HISTORY**6/2022—Rev. 0 to Rev. A**

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| Changes to Table 2..... | 6 |
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4/2021—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

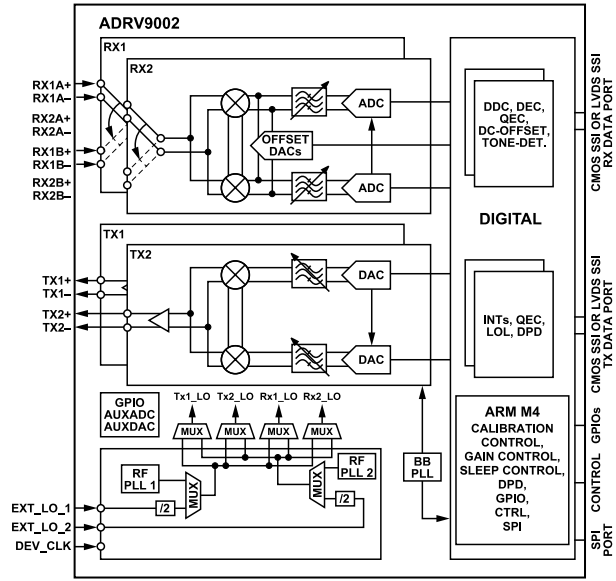


Figure 1.

SPECIFICATIONS

Electrical characteristics are at the operating ambient temperature range, VDDA_1P0 = 1.0 V, VDDA_1P3 = 1.3 V, VDDA_1P8 = 1.8 V, VDD_1P0 = 1.0 V, and VDD_1P8 = 1.8 V.

TRANSMITTER SPECIFICATIONS

Table 1. Transmitters (Tx1 and Tx2)

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|--------|-------|------|------|-----------------------|---|
| CENTER FREQUENCY | | 30 | | 6000 | MHz | |
| TRANSMITTER SYNTHESIS BANDWIDTH | | 0.012 | | 40 | MHz | Zero-IF mode, see the DPD section for more information |
| BANDWIDTH FLATNESS | | | 0.1 | | dB | 10 MHz bandwidth span, including digital compensation |
| DEVIATION FROM LINEAR PHASE | | | 1 | | Degrees | 40 MHz bandwidth |
| POWER CONTROL RANGE | | | | | | |
| In-Phase (I) and Quadrature (Q) Mode | | | 42 | | dB | |
| Direct Modulation Mode | | | 12 | | dB | |
| POWER CONTROL RESOLUTION | | | | | | |
| I and Q Mode | | | 0.05 | | dB | |
| Direct Modulation Mode | | | 0.5 | | dB | |
| IN BAND NOISE FLOOR | | | -154 | | dBFS ¹ /Hz | 0 dB attenuation, in band noise falls 1 dB for each dB of attenuation for attenuation settings between 0 dB and 20 dB |
| OUT OF BAND NOISE FLOOR | | | -156 | | dBFS/Hz | 0 dB attenuation with 3 × bandwidth/2 offset |
| Tx1 TO Tx2 ISOLATION | | | | | | |
| 30 MHz | | | 98 | | dB | |
| 470 MHz | | | 97 | | dB | |
| 900 MHz | | | 93 | | dB | |
| 2400 MHz | | | 93 | | dB | |
| 3500 MHz | | | 79 | | dB | |
| 5800 MHz | | | 70 | | dB | |
| IMAGE REJECTION WITH INITIALIZATION CALIBRATION ONLY | | | | | | |
| Wideband | | | | | | Up to 20 dB transmitter attenuation, 40 MHz bandwidth, 0 dB observation receiver attenuation, 18 MHz continuous wave ² signal input, QEC ³ tracking calibration is disabled |
| 50 MHz | | | 55 | | dBc | |
| 470 MHz | | | 63 | | dBc | |
| 900 MHz | | | 59 | | dBc | |
| 2400 MHz | | | 60 | | dBc | |
| 3500 MHz | | | 57 | | dBc | |
| 5800 MHz | | | 55 | | dBc | |
| Narrow-Band | | | | | | Up to 20 dB transmitter attenuation, 25 kHz bandwidth, 0 dB observation receiver attenuation, 2.1 kHz continuous wave ² signal input, QEC tracking calibration is disabled |
| 30 MHz | | | 61 | | dBc | |
| 470 MHz | | | 68 | | dBc | |
| 900 MHz | | | 65 | | dBc | |
| 2400 MHz | | | 60 | | dBc | |
| 3500 MHz | | | 50 | | dBc | |
| 5800 MHz | | | 50 | | dBc | |

SPECIFICATIONS

Table 1. Transmitters (Tx1 and Tx2)

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|--------------------|-----|-----|-----|------|---|
| IMAGE REJECTION WITH INITIALIZATION CALIBRATION AND TRACKING CALIBRATION Wideband | | | | | | 0 dB transmitter attenuation, 40 MHz bandwidth, -0.2 dBFS, 18 MHz continuous wave ² signal input, 50 Ω load, 0 dB observation receiver attenuation, QEC is active |
| 50 MHz | | | 57 | | dBc | |
| 470 MHz | | | 66 | | dBc | |
| 900 MHz | | | 63 | | dBc | |
| 2400 MHz | | | 60 | | dBc | |
| 3500 MHz | | | 61 | | dBc | |
| 5800 MHz | | | 57 | | dBc | |
| CONTINUOUS WAVE FULL-SCALE OUTPUT POWER | | | | | | -0.2 dBFS, 18 MHz continuous wave ² signal input, 50 Ω load, 0 dB transmitter attenuation |
| 30 MHz | | | 7.3 | | dBm | |
| 470 MHz | | | 7.3 | | dBm | |
| 900 MHz | | | 7.6 | | dBm | |
| 2400 MHz | | | 7.4 | | dBm | |
| 3500 MHz | | | 7.8 | | dBm | |
| 5800 MHz | | | 7.2 | | dBm | |
| OUTPUT IMPEDANCE | Z _{OUT} | | 50 | | Ω | Differential, see the ADRV9001 system development user guide for more information |
| MAXIMUM OUTPUT LOAD VOLTAGE STANDING WAVE RATIO (VSWR) | | | | 3 | | Use the maximum value to ensure adequate calibration |
| OUTPUT RETURN LOSS | | | | | | Single-ended return loss measured with balun in place on board |
| 30 MHz | | | 17 | | dB | |
| 470 MHz | | | 18 | | dB | |
| 900 MHz | | | 17 | | dB | |
| 2400 MHz | | | 23 | | dB | |
| 3500 MHz | | | 13 | | dB | |
| 5800 MHz | | | 10 | | dB | |
| OUTPUT THIRD-ORDER INTERCEPT POINT | | | | | | 0 dB transmitter attenuation, 40 MHz bandwidth, 17 MHz and 18 MHz continuous wave ² signal input, digital backoff = 11 dBFS/tone, calibrated at the device output |
| Wideband | OIP _{3WB} | | | | | |
| 50 MHz | | | 31 | | dBm | |
| 470 MHz | | | 31 | | dBm | |
| 900 MHz | | | 30 | | dBm | |
| 2400 MHz | | | 28 | | dBm | |
| 3500 MHz | | | 29 | | dBm | |
| 5800 MHz | | | 27 | | dBm | |
| Narrow-Band | OIP _{3NB} | | | | | 0 dB transmitter attenuation, 25 kHz bandwidth, 2.1 kHz and 3.1 kHz continuous wave ² signal input, digital backoff = 5 dBFS/tone, calibrated at the device output |
| 30 MHz | | | 30 | | dBm | |
| 470 MHz | | | 31 | | dBm | |
| 900 MHz | | | 30 | | dBm | |
| 2400 MHz | | | 28 | | dBm | |
| 3500 MHz | | | 27 | | dBm | |
| 5800 MHz | | | 25 | | dBm | |

SPECIFICATIONS

Table 1. Transmitters (Tx1 and Tx2)

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|--------|-----|-----|-----|------|--|
| CARRIER LEAKAGE WITH INITIALIZATION CALIBRATION ONLY | | | | | | LO leakage tracking calibration disabled, 0 dB transmitter attenuation, scales dB for dB with attenuation, input tone backoff = 6 dBFS |
| Wideband | | | | | | |
| 50 MHz | | | -68 | | dBm | |
| 470 MHz | | | -65 | | dBm | |
| 900 MHz | | | -67 | | dBm | |
| 2400 MHz | | | -68 | | dBm | |
| 3500 MHz | | | -62 | | dBm | |
| 5800 MHz | | | -56 | | dBm | |
| Narrow-Band | | | | | | |
| 30 MHz | | | -70 | | dBm | |
| 470 MHz | | | -72 | | dBm | |
| 900 MHz | | | -74 | | dBm | |
| 2400 MHz | | | -71 | | dBm | |
| 3500 MHz | | | -71 | | dBm | |
| 5800 MHz | | | -58 | | dBm | |

¹ dBFS represents the ratio of the actual output signal to the maximum possible output level for a continuous wave output signal at the given RF attenuation setting.

² A continuous wave is a single frequency signal.

³ Quadrature error correction (QEC) is the system for minimizing quadrature images of a desired signal.

RECEIVER SPECIFICATIONS

Table 2. Receivers (Rx1A, Rx1B, Rx2A, and Rx2B)

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|--------|-----|-----|------|------|--|
| CENTER FREQUENCY | | 30 | | 6000 | MHz | |
| MAXIMUM GAIN | | | | | | |
| Wideband | | | | | | High performance receiver ADCs, 0 dB attenuation, 5.6 MHz baseband frequency |
| 50 MHz | | | 21 | | dB | |
| 470 MHz | | | 22 | | dB | |
| 900 MHz | | | 22 | | dB | |
| 2400 MHz | | | 22 | | dB | |
| 3500 MHz | | | 21 | | dB | |
| 5800 MHz | | | 21 | | dB | |
| Narrow-Band | | | | | | High performance receiver ADCs, 0 dB attenuation, 2.1 kHz baseband frequency |
| 30 MHz | | | 21 | | dB | |
| 470 MHz | | | 22 | | dB | |
| 900 MHz | | | 22 | | dB | |
| 2400 MHz | | | 22 | | dB | |
| 3500 MHz | | | 21 | | dB | |
| 5800 MHz | | | 21 | | dB | |
| ATTENUATION RANGE FROM MAXIMUM GAIN | | | 34 | | dB | |
| Attenuation Accuracy | | | | | | |
| Gain Step | | | 0.5 | | dB | Attenuator steps from 0 dB to 30 dB |
| | | | 1.0 | | dB | Attenuator steps from 30 dB to 34 dB |
| Gain Step Error | | | 0.1 | | dB | Attenuation step from 0 dB to 30 dB, LO from 30 MHz to 3 GHz |
| | | | 0.2 | | dB | Attenuation step from 0 dB to 30 dB, LO from 3 GHz to 6 GHz |

SPECIFICATIONS

Table 2. Receivers (Rx1A, Rx1B, Rx2A, and Rx2B)

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|------------------|-------|-------|-----|------|---|
| | | | 0.1 | | dB | Attenuation step from 30 dB to 34 dB |
| FREQUENCY RESPONSE | | | | | | |
| Peak-to-Peak Gain Deviation | | | 1 | | dB | 40 MHz bandwidth including digital compensation |
| | | | 0.2 | | dB | Any 10 MHz span including digital compensation |
| RECEIVER BANDWIDTH | | 0.012 | | 40 | MHz | Zero-IF mode, the analog low-pass filter (LPF) bandwidth is 5 MHz minimum, the programmable finite impulse response (FIR) filter bandwidth is configurable over the entire range |
| RECEIVER ALIAS BAND REJECTION | | 80 | | | dB | This performance is achieved because of the digital filters |
| CONTINUOUS WAVE FULL-SCALE INPUT POWER ¹ | FSIP | | -11.4 | | dBm | This continuous wave signal level corresponds to the input power at maximum gain that produces 0 dBFS at the ADC output, this level increases dB for dB with attenuation, backoff by at least -2 dBFS is required |
| INPUT IMPEDANCE | | | 100 | | Ω | Differential, see the ADRV9001 system development user guide for more information |
| INPUT PORT RETURN LOSS | | | | | | Single-ended return loss measured with balun in place on board |
| 30 MHz | | | 20 | | dB | |
| 470 MHz | | | 21 | | dB | |
| 900 MHz | | | 20 | | dB | |
| 2400 MHz | | | 22 | | dB | |
| 3500 MHz | | | 9 | | dB | |
| 5800 MHz | | | 10 | | dB | |
| NOISE FIGURE | | | | | | |
| High Performance Receiver ADCs | | | | | | |
| Wideband | NF _{WB} | | | | | 0 dB attenuation at the device under test (DUT) receive port, integrated bandwidth from 8 MHz to 9 MHz |
| 50 MHz | | | 11.6 | | dB | |
| 470 MHz | | | 10.6 | | dB | |
| 900 MHz | | | 10.5 | | dB | |
| 2400 MHz | | | 11.4 | | dB | |
| 3500 MHz | | | 12.5 | | dB | |
| 5800 MHz | | | 12.6 | | dB | |
| Narrow-Band | NF _{NB} | | | | | 0 dB attenuation at the device under test (DUT) receive port, integrated bandwidth from 4 kHz to 8 kHz, 18 dB interface gain, intermediate frequency (IF) = 490 kHz |
| 30 MHz | | | 13.8 | | dB | |
| 470 MHz | | | 11.8 | | dB | |
| 900 MHz | | | 11.8 | | dB | |
| 2400 MHz | | | 12.3 | | dB | |
| 3500 MHz | | | 14.2 | | dB | |
| 5800 MHz | | | 15.1 | | dB | |
| Low Power Receiver ADCs | | | | | | |
| Wideband | NF _{WB} | | | | | 0 dB attenuation at the DUT receive port, integrated bandwidth from 8 MHz to 9 MHz |
| 50 MHz | | | 13.1 | | dB | |
| 470 MHz | | | 11.9 | | dB | |
| 900 MHz | | | 12.0 | | dB | |
| 2400 MHz | | | 12.6 | | dB | |
| 3500 MHz | | | 13.6 | | dB | |
| 5800 MHz | | | 13.9 | | dB | |
| Narrow-Band | NF _{NB} | | | | | 0 dB attenuation at the DUT receive port, integrated bandwidth from 4 kHz to 8 kHz, 18 dB interface gain, IF = 490 kHz |

SPECIFICATIONS

Table 2. Receivers (Rx1A, Rx1B, Rx2A, and Rx2B)

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|--------------------|-----|------|-----|------|---|
| 30 MHz | | | 16.7 | | dB | |
| 470 MHz | | | 14.8 | | dB | |
| 900 MHz | | | 15.1 | | dB | |
| 2400 MHz | | | 15.6 | | dB | |
| 3500 MHz | | | 17.0 | | dB | |
| 5800 MHz | | | 17.5 | | dB | |
| SECOND-ORDER INPUT INTERMODULATION INTERCEPT POINT | | | | | | |
| High Performance Receiver ADCs | | | | | | |
| Wideband | IIP2 _{WB} | | | | | 0 dB receiver attenuation, 1 dB cutoff frequency (f_{1dB}) of the transimpedance amplifier (TIA) = 20 MHz, two continuous wave tones at 17 MHz and 18 MHz, for LO = 50 MHz, tone output power is -11.6 dBFS/tone, for all other LOs, tone output power is -8.1 dBFS/tone |
| 50 MHz | | | 79 | | dBm | |
| 470 MHz | | | 81 | | dBm | |
| 900 MHz | | | 85 | | dBm | |
| 2400 MHz | | | 73 | | dBm | |
| 3500 MHz | | | 60 | | dBm | |
| 5800 MHz | | | 60 | | dBm | |
| Narrow-Band | IIP2 _{NB} | | | | | 0 dB receiver attenuation, 3 dB cutoff frequency (f_{3dB}) of the first-order transimpedance amplifier (TIA) = 4 MHz, two continuous wave tones at 1.0061 MHz and 2.0061 MHz, for LO = 30 MHz, 470 MHz, 900 MHz and 2400 MHz, tone output power is -11.6 dBFS/tone, for LO = 3500 MHz and 5800 MHz, tone output power is -6.6 dBFS/tone |
| 30 MHz | | | 90 | | dBm | |
| 470 MHz | | | 89 | | dBm | |
| 900 MHz | | | 85 | | dBm | |
| 2400 MHz | | | 68 | | dBm | |
| 3500 MHz | | | 73 | | dBm | |
| 5800 MHz | | | 67 | | dBm | |
| Low Power Receiver ADCs | | | | | | |
| Wideband | IIP2 _{WB} | | | | | 0 dB receiver attenuation, f_{1dB} of the TIA = 20 MHz, two continuous wave tones at 17 MHz and 18 MHz, for LO = 50 MHz, tone output power is -11.6 dBFS/tone, for all other LOs, tone output power is -8.1 dBFS/tone |
| 50 MHz | | | 70 | | dBm | |
| 470 MHz | | | 74 | | dBm | |
| 900 MHz | | | 72 | | dBm | |
| 2400 MHz | | | 65 | | dBm | |
| 3500 MHz | | | 59 | | dBm | |
| 5800 MHz | | | 60 | | dBm | |
| Narrow-Band | IIP2 _{NB} | | | | | 0 dB receiver attenuation, 3 dB cutoff frequency (f_{3dB}) of the first-order transimpedance amplifier (TIA) = 4 MHz, two continuous wave tones at 1.0061 MHz and 2.0061 MHz, for LO = 30 MHz, 470 MHz, 900 MHz and 2400 MHz, tone output power is -11.6 dBFS/tone, for LO = 3500 MHz and 5800 MHz, tone output power is -6.6 dBFS/tone |
| 30 MHz | | | 82 | | dBm | |
| 470 MHz | | | 84 | | dBm | |
| 900 MHz | | | 81 | | dBm | |
| 2400 MHz | | | 70 | | dBm | |
| 3500 MHz | | | 71 | | dBm | |
| 5800 MHz | | | 67 | | dBm | |

SPECIFICATIONS

Table 2. Receivers (Rx1A, Rx1B, Rx2A, and Rx2B)

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|--------------------|-----|-----|-----|------|---|
| THIRD-ORDER INPUT INTERMODULATION INTERCEPT POINT, DIFFERENCE PRODUCT | | | | | | |
| High Performance Receiver ADCs | | | | | | |
| Wideband | IIP3 _{WB} | | | | | 0 dB receiver attenuation, f_{1dB} of the TIA = 20 MHz, two continuous wave tones at 17 MHz and 18 MHz, for LO = 50 MHz, tone output power is -11.6 dBFS/tone, for all other LOs, tone output power is -8.1 dBFS/tone |
| 50 MHz | | | 22 | | dBm | |
| 470 MHz | | | 26 | | dBm | |
| 900 MHz | | | 27 | | dBm | |
| 2400 MHz | | | 28 | | dBm | |
| 3500 MHz | | | 26 | | dBm | |
| 5800 MHz | | | 25 | | dBm | |
| Narrow-Band | IIP3 _{NB} | | | | | 0 dB receiver attenuation, for LO = 30 MHz, second-order TIA is used and f_{1dB} of the TIA = 7 MHz, for all others, first-order TIA is used and f_{1dB} of the TIA = 4 MHz, two continuous wave tones at 1.0061 MHz and 2.0061 MHz, for LO = 30 MHz and 900 MHz, tone output power is -15.1 dBFS/tone, for LO = 470 MHz and 2400 MHz, tone output power is -13.6 dBFS/tone, for LO = 3500 MHz, tone output power is -12.6 dBFS/tone, for LO = 5800 MHz, tone output power is -14 dBFS/tone |
| 30 MHz | | | 31 | | dBm | |
| 470 MHz | | | 33 | | dBm | |
| 900 MHz | | | 29 | | dBm | |
| 2400 MHz | | | 26 | | dBm | |
| 3500 MHz | | | 27 | | dBm | |
| 5800 MHz | | | 23 | | dBm | |
| Low Power Receiver ADCs | | | | | | |
| Wideband | IIP3 _{WB} | | | | | 0 dB receiver attenuation, f_{1dB} of the TIA = 20 MHz, two continuous wave tones at 17 MHz and 18 MHz, for LO = 50 MHz, tone output power is -11.6 dBFS/tone, for all other LOs, tone output power is -8.1 dBFS/tone |
| 50 MHz | | | 21 | | dBm | |
| 470 MHz | | | 22 | | dBm | |
| 900 MHz | | | 22 | | dBm | |
| 2400 MHz | | | 21 | | dBm | |
| 3500 MHz | | | 23 | | dBm | |
| 5800 MHz | | | 20 | | dBm | |
| Narrow-Band | IIP3 _{NB} | | | | | 0 dB receiver attenuation, for LO = 30 MHz, second-order TIA is used and f_{1dB} of the TIA = 7 MHz, for all others, first-order TIA is used and f_{1dB} of the TIA = 4 MHz, two continuous wave tones at 1.0061 MHz and 2.0061 MHz, for LO = 30 MHz and 900 MHz, tone output power is -15.1 dBFS/tone, for LO = 470 MHz and 2400 MHz, tone output power is -13.6 dBFS/tone, for LO = 3500 MHz, tone output power is -12.6 dBFS/tone, for LO = 5800 MHz, tone output power is -14 dBFS/tone |
| 30 MHz | | | 23 | | dBm | |
| 470 MHz | | | 23 | | dBm | |
| 900 MHz | | | 21 | | dBm | |
| 2400 MHz | | | 22 | | dBm | |
| 3500 MHz | | | 26 | | dBm | |
| 5800 MHz | | | 21 | | dBm | |
| THIRD-ORDER HARMONIC DISTORTION | | | | | | |
| High Performance Receiver ADCs | | | | | | |

SPECIFICATIONS

Table 2. Receivers (Rx1A, Rx1B, Rx2A, and Rx2B)

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|----------------------------------|-------------------|-----|------|-----|------|--|
| Wideband | HD3 _{WB} | | | | | -20 dBm input power continuous wave tone at 5.6 MHz at maximum gain at Rx input port, f_{1dB} of the TIA = 20 MHz, HD3 product at 16.8 MHz |
| 50 MHz | | | -84 | | dBc | |
| 470 MHz | | | -74 | | dBc | |
| 900 MHz | | | -82 | | dBc | |
| 2400 MHz | | | -92 | | dBc | |
| 3500 MHz | | | -93 | | dBc | |
| 5800 MHz | | | -89 | | dBc | |
| Narrow-Band | HD3 _{NB} | | | | | -20 dBm input power continuous wave tone at 2.1 kHz at maximum gain at Rx input port, f_{1dB} of the TIA = 2 MHz, HD3 product at 6.3 kHz |
| 30 MHz | | | -102 | | dBc | |
| 470 MHz | | | -97 | | dBc | |
| 900 MHz | | | -89 | | dBc | |
| 2400 MHz | | | -79 | | dBc | |
| 3500 MHz | | | -80 | | dBc | |
| 5800 MHz | | | -72 | | dBc | |
| Low Power Receiver ADCs | | | | | | |
| Wideband | HD3 _{WB} | | | | | -20 dBm input power continuous wave tone at 5.6 MHz at maximum gain at Rx input port, f_{1dB} of the TIA = 20 MHz, HD3 product at 16.8 MHz |
| 50 MHz | | | -90 | | dBc | |
| 470 MHz | | | -71 | | dBc | |
| 900 MHz | | | -79 | | dBc | |
| 2400 MHz | | | -81 | | dBc | |
| 3500 MHz | | | -82 | | dBc | |
| 5800 MHz | | | -84 | | dBc | |
| Narrow-Band | HD3 _{NB} | | | | | -20 dBm input power continuous wave tone at 2.1 kHz at maximum gain at Rx input port, f_{1dB} of the TIA = 2 MHz, HD3 product at 6.3 kHz |
| 30 MHz | | | -108 | | dBc | |
| 470 MHz | | | -95 | | dBc | |
| 900 MHz | | | -89 | | dBc | |
| 2400 MHz | | | -81 | | dBc | |
| 3500 MHz | | | -80 | | dBc | |
| 5800 MHz | | | -71 | | dBc | |
| SECOND-ORDER HARMONIC DISTORTION | | | | | | |
| High Performance Receiver ADCs | | | | | | |
| Wideband | HD2 _{WB} | | | | | -20 dBm input power continuous wave tone at 5.6 MHz at maximum gain at Rx input port, f_{1dB} of the TIA = 20 MHz, HD2 product at 11.2 MHz |
| 50 MHz | | | -91 | | dBc | |
| 470 MHz | | | -93 | | dBc | |
| 900 MHz | | | -93 | | dBc | |
| 2400 MHz | | | -89 | | dBc | |
| 3500 MHz | | | -83 | | dBc | |
| 5800 MHz | | | -82 | | dBc | |
| Narrow-Band | HD2 _{NB} | | | | | -20 dBm input power continuous wave tone at 2.1 kHz at maximum gain at Rx input port, f_{1dB} of the TIA = 2 MHz, HD2 product at 4.2 kHz |
| 30 MHz | | | -102 | | dBc | |
| 470 MHz | | | -96 | | dBc | |
| 900 MHz | | | -90 | | dBc | |
| 2400 MHz | | | -79 | | dBc | |

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Table 2. Receivers (Rx1A, Rx1B, Rx2A, and Rx2B)

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-------------------|-----|------|-----|------|--|
| 3500 MHz | | | -80 | | dBc | |
| 5800 MHz | | | -71 | | dBc | |
| Low Power Receiver ADCs | | | | | | |
| Wideband | HD2 _{WB} | | | | | -20 dBm input power continuous wave tone at 5.6 MHz at maximum gain at Rx input port, f_{1dB} of the TIA = 20 MHz, HD2 product at 11.2 MHz |
| 50 MHz | | | -92 | | dBc | |
| 470 MHz | | | -92 | | dBc | |
| 900 MHz | | | -91 | | dBc | |
| 2400 MHz | | | -89 | | dBc | |
| 3500 MHz | | | -84 | | dBc | |
| 5800 MHz | | | -79 | | dBc | |
| Narrow-Band | HD2 _{NB} | | | | | -20 dBm input power continuous wave tone at 2.1 kHz at maximum gain at Rx input port, f_{1dB} of the TIA = 2 MHz, HD2 product at 4.2 kHz |
| 30 MHz | | | -109 | | dBc | |
| 470 MHz | | | -94 | | dBc | |
| 900 MHz | | | -90 | | dBc | |
| 2400 MHz | | | -81 | | dBc | |
| 3500 MHz | | | -80 | | dBc | |
| 5800 MHz | | | -70 | | dBc | |
| IMAGE REJECTION WITH INITIALIZATION CALIBRATION AND HARDWARE TRACKING ONLY | | | | | | |
| High Performance Receiver ADCs | | | | | | |
| Wideband | | | | | | Software QEC disabled, 40 MHz receiver bandwidth, maximum receiver gain index, -20 dBm input power continuous wave tone at 5.6 MHz |
| 50 MHz | | | 84 | | dBc | |
| 470 MHz | | | 83 | | dBc | |
| 900 MHz | | | 82 | | dBc | |
| 1900 MHz | | | 81 | | dBc | |
| 3500 MHz | | | 82 | | dBc | |
| 5800 MHz | | | 78 | | dBc | |
| Narrow-Band | | | | | | 25 KHz receiver bandwidth, maximum receiver gain index, -20 dBm input power continuous wave tone at 2100 KHz |
| 30 MHz | | | 102 | | dBc | |
| 470 MHz | | | 96 | | dBc | |
| 900 MHz | | | 95 | | dBc | |
| 2400 MHz | | | 92 | | dBc | |
| 3500 MHz | | | 89 | | dBc | |
| 5800 MHz | | | 86 | | dBc | |
| Low Power Receiver ADCs | | | | | | |
| Wideband | | | | | | Software QEC disabled, 40 MHz receiver bandwidth, maximum receiver gain index, -20 dBm input power continuous wave tone at 5.6 MHz |
| 50 MHz | | | 87 | | dBc | |
| 470 MHz | | | 90 | | dBc | |
| 900 MHz | | | 86 | | dBc | |
| 1900 MHz | | | 84 | | dBc | |
| 3500 MHz | | | 82 | | dBc | |
| 5800 MHz | | | 75 | | dBc | |
| Narrow-Band | | | | | | 25 KHz receiver bandwidth, maximum receiver gain index, -20 dBm input power continuous wave tone at 2100 KHz |

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Table 2. Receivers (Rx1A, Rx1B, Rx2A, and Rx2B)

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|--------|-----|-----|-----|------|--|
| 30 MHz | | | 99 | | dBc | |
| 470 MHz | | | 98 | | dBc | |
| 900 MHz | | | 98 | | dBc | |
| 2400 MHz | | | 93 | | dBc | |
| 3500 MHz | | | 89 | | dBc | |
| 5800 MHz | | | 87 | | dBc | |
| RECEIVER INPUT LO LEAKAGE AT MAXIMUM GAIN | | | | | | Leakage decreased dB for dB with attenuation for the first 12 dB |
| 50 MHz | | | -66 | | dBm | |
| 470 MHz | | | -66 | | dBm | |
| 900 MHz | | | -66 | | dBm | |
| 2400 MHz | | | -66 | | dBm | |
| 3500 MHz | | | -62 | | dBm | |
| 5800 MHz | | | -60 | | dBm | |
| SIGNAL ISOLATION | | | | | | |
| Tx1 to Rx1A or Rx1B Signal Isolation and Tx2 to Rx2A or Rx2B Signal Isolation | | | | | | Isolation between Tx and Rx port, isolation changes dB for dB with Rx gain |
| 30 MHz | | | 100 | | dB | |
| 470 MHz | | | 85 | | dB | |
| 900 MHz | | | 78 | | dB | |
| 2400 MHz | | | 77 | | dB | |
| 3500 MHz | | | 62 | | dB | |
| 5800 MHz | | | 64 | | dB | |
| Tx1 to Rx2A or Rx2B Isolation and Tx2 to Rx1A or Rx2B Signal Isolation | | | | | | Isolation between Tx and Rx port, isolation changes dB for dB with Rx gain |
| 30 MHz | | | 120 | | dB | |
| 470 MHz | | | 110 | | dB | |
| 900 MHz | | | 100 | | dB | |
| 2400 MHz | | | 90 | | dB | |
| 3500 MHz | | | 74 | | dB | |
| 5800 MHz | | | 81 | | dB | |
| Rx1A or Rx1B to Rx2A or Rx2B Signal Isolation | | | | | | |
| 30 MHz | | | 106 | | dB | |
| 470 MHz | | | 103 | | dB | |
| 900 MHz | | | 98 | | dB | |
| 2400 MHz | | | 92 | | dB | |
| 3500 MHz | | | 83 | | dB | |
| 5800 MHz | | | 71 | | dB | |
| Rx1A to Rx1B and Rx2A to Rx2B Signal Isolation | | | | | | |
| 30 MHz | | | 99 | | dB | |
| 470 MHz | | | 97 | | dB | |
| 900 MHz | | | 90 | | dB | |
| 2400 MHz | | | 86 | | dB | |
| 3500 MHz | | | 84 | | dB | |

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Table 2. Receivers (Rx1A, Rx1B, Rx2A, and Rx2B)

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|-----------|--------|-----|-----|-----|------|--------------------------|
| 5800 MHz | | | 70 | | dB | |

¹ Note that the input signal power limit does not correspond to 0 dBFS at the digital output because of the nature of the continuous time Σ - Δ ADCs. Unlike the hard clipping characteristic of pipeline ADCs, these converters exhibit a soft overload behavior when the input approaches the maximum level.

INTERNAL LO, EXTERNAL LO, AND DEVICE CLOCK

Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments | |
|---|-------------|-----|----------------|-------|----------|--|---|
| LO | | | | | | | |
| Frequency Step | | | | 2.2 | Hz | For 38.4 MHz DEV_CLK ¹ , use the equation $DEV_CLK / ((2^{23} - 15) \times 2)$ to calculate, assuming the LO divider is 2 LO < 1 GHz, PLL bandwidth = 300 kHz | |
| Reference Spurs | | | -80 | | dBc | | |
| LO WITH HIGH PERFORMANCE MODE | | | | | | | |
| Integrated Phase Noise | | | | | | Integrated from 100 Hz to 50 MHz PLL bandwidth = 300 kHz | |
| 30 MHz LO | | | 0.008 | | °rms | | |
| 470 MHz LO | | | 0.04 | | °rms | | |
| 900 MHz LO | | | 0.08 | | °rms | | |
| 2400 MHz LO | | | 0.22 | | °rms | | |
| 3500 MHz LO | | | 0.27 | | °rms | | |
| 5800 MHz LO | | | 0.6 | | °rms | | |
| Phase Noise | | | | | | | DEV_CLK = 38.4 MHz, typical performance |
| 30 MHz LO | | | See Figure 354 | | | | PLL bandwidth = 300 kHz |
| 470 MHz LO | | | See Figure 355 | | | | PLL bandwidth = 300 kHz |
| 900 MHz LO | | | See Figure 356 | | | | PLL bandwidth = 300 kHz |
| 2400 MHz LO | | | See Figure 357 | | | | PLL bandwidth = 300 kHz |
| 3500 MHz LO | | | See Figure 358 | | | | PLL bandwidth = 300 kHz |
| 5800 MHz LO | | | See Figure 359 | | | PLL bandwidth = 300 kHz | |
| LO PHASE SYNCHRONIZATION | | | | | | | |
| Initial Phase Synchronization Accuracy | | | 3 | | Degrees | | |
| EXTERNAL LO INPUT | | | | | | | |
| Input Frequency | | | | | | Input frequency must be 2× or higher than the desired frequency for the LO frequency (f_{LO}), a 1× multiplier is available for an LO range from 500 MHz to 1 GHz | |
| | f_{EXTLO} | 60 | | 12000 | MHz | | |
| Input Signal Power | | -6 | 0 | +6 | dBm | 50 Ω matching at the source | |
| Input Signal Differential Phase Balance | | | | 20 | Degrees | | |
| Input Signal Differential Amplitude Balance | | | | 1 | dB | Do not exceed 20 degrees to ensure adequate quadrature error correction | |
| Input Signal Duty Cycle | | | | 2.5 | % | | |
| Input Impedance | | | | 100 | Ω | Differential, see the ADRV9001 system development user guide for more information | |
| | | | | | | | |
| REFERENCE CLOCK (DEV_CLK_IN SIGNAL) | | | | | | | |
| Differential mode | | | | | | | |
| Frequency Range | | 10 | | 1000 | MHz | | |

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Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|-----------------------------------|--------|-----|-----|-----|-------|--|
| Signal Level | | 0.2 | | 0.4 | V p-p | AC-coupled, for optimal spurious performance and to meet the specified PLL performance parameters, use a 400 mV p-p (800 mV p-p differential) input clock. |
| Single-Ended Mode | | | | | | |
| Frequency Range | | 10 | | 80 | MHz | |
| Signal Level | | 0.2 | | 1 | V p-p | AC-coupled, for optimal spurious performance and to meet the specified PLL performance parameters, use a 1 V p-p input clock. |
| REFERENCE CLOCK (XTAL) | | | | | | |
| Frequency Range | | 20 | | 80 | MHz | |
| CLOCK OUTPUT (DEV_CLK_OUT SIGNAL) | | | | | | |
| Frequency Range | | 10 | | 80 | MHz | |

¹ DEV_CLK is the device clock frequency rate.

DIGITAL INTERFACES AND AUXILIARY CONVERTERS

Table 4.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-------------------|------------------------------|-------------------|------|--------------------------|
| AUXILIARY ADC CONVERTERS | | | | | |
| Resolution | | 10 | | Bits | |
| Input Voltage | | | | | |
| Minimum | | 0.05 | | V | |
| Maximum | | 0.95 | | V | |
| AUXILIARY DAC CONVERTERS | | | | | |
| Resolution | | 12 | | Bits | |
| Output Voltage | | | | | |
| Minimum | | 0.05 | | V | |
| Maximum | | VDDA_1P8 ¹ - 0.05 | | V | |
| Drive Capability | | 10 | | mA | |
| DIGITAL SPECIFICATIONS (CMOS SSI SIGNALS) | | | | | |
| Logic Inputs | | | | | |
| Input Voltage | | | | | |
| High Level | VDIGIO_1P8 × 0.65 | | VDIGIO_1P8 + 0.18 | V | |
| Low Level | -0.30 | | VDIGIO_1P8 × 0.35 | V | |
| Logic Outputs | | | | | |
| Output Voltage | | | | | |
| High Level | VDIGIO_1P8 - 0.45 | | | V | |
| Low Level | | | 0.45 | V | |
| Drive Capability | | 10 | | mA | |
| DIGITAL SPECIFICATIONS (DIGITAL GPIO SIGNALS) | | | | | |
| Logic Inputs | | | | | |

SPECIFICATIONS

Table 4.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|------------------------------|-------|------------------------------|----------|---|
| Input Voltage | | | | | |
| High Level | $V_{DIGIO_1P8} \times 0.65$ | | $V_{DIGIO_1P8} + 0.18$ | V | |
| Low Level | -0.30 | | $V_{DIGIO_1P8} \times 0.35$ | V | |
| Logic Outputs | | | | | |
| Output Voltage | | | | | |
| High Level | $V_{DIGIO_1P8} - 0.45$ | | | V | |
| Low Level | | | 0.45 | V | |
| Drive Capability | | 10 | | mA | |
| DATAPORT SPECIFICATIONS (LVDS SSI, MCS+ and MCS-) | | | | | |
| Logic Inputs | | | | | |
| Input Voltage Range | 825 | | 1675 | mV | Each differential input in the pair |
| Input Differential Voltage Threshold | -100 | | +100 | mV | |
| Receiver Differential Input Impedance | | 100 | | Ω | Internal termination enabled |
| Logic Outputs | | | | | |
| Output Voltage | | | | | |
| High Level | | | 1390 | mV | |
| Low Level | 1000 | | | mV | |
| Differential | | 300 | | mV | |
| Offset | | 1200 | | mV | |
| Output Current | | | 17 | mA | Drivers are shorted to ground, there is no internal termination available, an off-chip 100 Ω termination is required |
| Clock Signal Duty Cycle | 45 | 50 | 55 | % | 500 MHz |
| Output Rise and Fall Time | | 0.371 | | ns | 300 mV p-p swing |
| DIGITAL SPECIFICATIONS (ANALOG GPIO SIGNALS) | | | | | |
| Logic Inputs | | | | | |
| Input Voltage | | | | | |
| High Level | $V_{DDA_1P8} \times 0.65$ | | $V_{DDA_1P8} + 0.18$ | V | |
| Low Level | -0.30 | | $V_{DDA_1P8} \times 0.35$ | V | |
| Logic Outputs | | | | | |
| Output Voltage | | | | | |
| High Level | $V_{DDA_1P8} - 0.45$ | | | V | |
| Low Level | | | 0.45 | V | |
| Drive Capability | | 10 | | mA | |

¹ V_{DDA_1P8} refers to all analog 1.8 V supplies including V_{CONV_1P8} , V_{AGPIO_1P8} , V_{ANA2_1P8} , and V_{ANA1_1P8} .

POWER SUPPLY SPECIFICATIONS

Table 5.

| Parameter | Min | Typ | Max | Unit |
|---|-------|-----|-------|------|
| SUPPLY CHARACTERISTICS | | | | |
| V_{DDA_1P0} ¹ Analog Supplies | 0.975 | 1.0 | 1.025 | V |
| V_{DD_1P0} ² Digital Supply | 0.95 | 1.0 | 1.05 | V |

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Table 5.

| Parameter | Min | Typ | Max | Unit |
|---------------------------------------|-------|-----|------|------|
| VDDA_1P3 ³ Analog Supplies | 1.267 | 1.3 | 1.33 | V |
| VDDA_1P8 Analog Supplies | 1.71 | 1.8 | 1.89 | V |
| VDD_1P8 ⁴ Digital Supply | 1.71 | 1.8 | 1.89 | V |

¹ VDDA_1P0 refers to all analog 1.0 V supplies that operate with the internal low dropout (LDO) regulator bypassed. The power domain that allows the internal LDO regulator bypass includes VRFL02_1P0, VRFL01_1P0, VRX2LO_1P3, VRX1LO_1P3, VTX2LO_1P3, VCONV_1P3, and VTX1LO_1P3.

² VDD_1P0 refers to all digital 1.0 V supplies including VDIG_1P0.

³ VDDA_1P3 refers to all analog 1.3 V supplies including VRFVCO2_1P3, VRFVCO1_1P3, VANA2_1P3, VANA1_1P3, VRX2LO_1P3, VCLKSYN_1P3, VRFSYN2_1P3, VRFSYN1_1P3, VAUXSYN_1P3, VRX1LO_1P3, VTX2LO_1P3, VCLKVCO_1P3, VAUXVCO_1P3, VTX1LO_1P3, and VCONV_1P3.

⁴ VDD_1P8 refers to all digital 1.8 V supplies including VDIGIO_1P8.

CURRENT CONSUMPTION ESTIMATES (TYPICAL VALUES)

No external VDDA_1P0 1.0 V power domain is used in Table 6 to Table 11. In all following modes described, the ADRV9002 operates with internal LDO regulators used to produce an on-chip, 1.0 V analog power domain.

Sleep Mode

Table 6. Digital Mobile Radio (DMR) CMOS SSI

| ADRV9002 Mode Conditions | Supply (mA) | | | | | Total Average Power (W) |
|---|--------------------------|------------------------|--------------------------|--------------------------|------------------------|-------------------------|
| | VDDA_1P0 Analog Supplies | VDD_1P0 Digital Supply | VDDA_1P3 Analog Supplies | VDDA_1P8 Analog Supplies | VDD_1P8 Digital Supply | |
| Receiver, Transmitter, Clock PLL, and LDO Regulator Powered Down, Internal Microprocessor Active, CMOS SSI Interface Off, DEV_CLK_OUT Off, and Auxiliary DACs Off | Not used | 18.9 | 8.2 | 9.7 | 1.3 | 0.049 |
| Receiver, Transmitter, Clock PLL, LDO Regulator, and Internal Microprocessor Powered Down, CMOS SSI Interface Off, DEV_CLK_OUT Off, and Auxiliary DACs Off | Not used | 2.3 | 6.9 | 9.7 | 1.3 | 0.031 |

Table 7. Long-Term Evolution (LTE) Dual Transmitter and Dual Receiver LVDS SSI

| ADRV9002 Mode Conditions | Supply (mA) | | | | | Total Average Power (W) |
|---|--------------------------|------------------------|--------------------------|--------------------------|------------------------|-------------------------|
| | VDDA_1P0 Analog Supplies | VDD_1P0 Digital Supply | VDDA_1P3 Analog Supplies | VDDA_1P8 Analog Supplies | VDD_1P8 Digital Supply | |
| Receiver, Transmitter, Clock PLL, and LDO Regulator Powered Down, Internal Microprocessor Active, LVDS SSI Interface Off, DEV_CLK_OUT Off, and Auxiliary DACs Off | Not used | 24.6 | 12.4 | 11.3 | 1.3 | 0.066 |
| Receiver, Transmitter, Clock PLL, LDO Regulator, and Internal Microprocessor Powered Down, LVDS SSI Interface Off, DEV_CLK_OUT Off, and Auxiliary DACs Off | Not used | 2.3 | 10.3 | 10.6 | 1.3 | 0.037 |

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TDD Operation

Table 8. DMR, 4× External LO, LO = 470 MHz, Low Power Mode Clock PLL, Processor Clock Divisor = 4, CMOS SSI

| ADRV9002 Mode Conditions | Supply (mA) | | | | | Total Average Power (W) |
|--|--------------------------|------------------------|--------------------------|--------------------------|------------------------|-------------------------|
| | VDDA_1P0 Analog Supplies | VDD_1P0 Digital Supply | VDDA_1P3 Analog Supplies | VDDA_1P8 Analog Supplies | VDD_1P8 Digital Supply | |
| 1 × Receiver Low Power ADC, Low IF, 12.5 kHz Receiver Bandwidth, 24 kSPS Data Rate, Receiver QEC Enabled, QEC Engine Active, and Transmitter Powered Down | Not used | 92 | 171 | 26 | 3 | 0.367 |
| 1 × Transmitter RF Attenuation = 0 dB, Full-Scale Continuous Wave 12.5 kHz Transmitter Bandwidth, 96 kSPS Data Rate, Direct Modulation (DM) Mode, Transmitter QEC Disabled, QEC Engine Inactive, and Receiver Powered Down | Not used | 62 | 257 | 100 | 3 | 0.582 |
| 1 × Transmitter RF Attenuation = 6 dB, Full-Scale Continuous Wave 12.5 kHz Transmitter Bandwidth, 96 kSPS Data Rate, DM Mode, Transmitter QEC Disabled, QEC Engine Inactive, and Receiver Powered Down | Not used | 62 | 257 | 58 | 3 | 0.506 |

Table 9. LTE40 Two Transmitters and Two Receivers (2T2R), LO = 2.5 GHz, High Performance Clock PLL, LVDS SSI

| ADRV9002 Mode Conditions | Supply (mA) | | | | | Total Average Power (W) |
|--|--------------------------|------------------------|--------------------------|--------------------------|------------------------|-------------------------|
| | VDDA_1P0 Analog Supplies | VDD_1P0 Digital Supply | VDDA_1P3 Analog Supplies | VDDA_1P8 Analog Supplies | VDD_1P8 Digital Supply | |
| 2 × Receiver Low Power ADC Low Rate, 40 MHz Receiver Bandwidth, 61.44 MSPS Data Rate, Receiver QEC Enabled, QEC Engine Active, and Transmitter in Primed State | Not used | 446 | 546 | 64 | 53 | 1.366 |
| 2 × Transmitter RF Attenuation = 0 dB, Full-Scale Continuous Wave 40 MHz Transmitter Bandwidth, 61.44 MSPS Data Rate, Transmitter QEC Disabled, QEC Engine Inactive, and Receiver in Primed State | Not used | 225 | 701 | 276 | 52 | 1.727 |
| 2 × Transmitter RF Attenuation = 10 dB, Full-Scale Continuous Wave 40 MHz Transmitter Bandwidth, 61.44 MSPS Data Rate, Transmitter QEC Disabled, QEC Engine Inactive, and Receiver in Primed State | Not used | 225 | 701 | 120 | 52 | 1.446 |
| 2 × Transmitter RF Attenuation = 0 dB, Full-Scale Continuous Wave 40 MHz Transmitter Bandwidth, 61.44 MSPS Data Rate, Transmitter QEC Disabled, QEC Engine Active, Receiver in Primed State, Transmitter QEC Tracking Always On, Observation Receiver Continuously On, and Transmitter Tracking Duty Cycled (Practical Scenario) | Not used | 397 | 1136 | 296 | 52 | 2.500 |
| 2 × Transmitter RF Attenuation = 10 dB, Full-Scale Continuous Wave 40 MHz Transmitter Bandwidth, 61.44 MSPS Data Rate, Transmitter QEC Enabled, QEC Engine Active, Receiver in Primed State, Transmitter QEC Tracking Always On, Observation Receiver Continuously On, and Transmitter Tracking Duty Cycled (Practical Scenario) | Not used | 395 | 1126 | 144 | 52 | 2.212 |

Table 10. LTE40 One Transmitter and One Receiver (1T1R), LO = 2.5 GHz, High Performance Clock PLL, LVDS SSI

| ADRV9002 Mode Conditions | Supply (mA) | | | | | Total Average Power (W) |
|--|--------------------------|------------------------|--------------------------|--------------------------|------------------------|-------------------------|
| | VDDA_1P0 Analog Supplies | VDD_1P0 Digital Supply | VDDA_1P3 Analog Supplies | VDDA_1P8 Analog Supplies | VDD_1P8 Digital Supply | |
| 1 × Receiver Low Power ADC Low Rate, 40 MHz Receiver Bandwidth, 61.44 MSPS Data Rate, Receiver QEC Enabled, QEC Engine Active, and Transmitter in Primed State | Not used | 258 | 406 | 39 | 28 | 0.906 |

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Table 10. LTE40 One Transmitter and One Receiver (1T1R), LO = 2.5 GHz, High Performance Clock PLL, LVDS SSI

| ADRV9002 Mode Conditions | Supply (mA) | | | | | Total Average Power (W) |
|---|--------------------------|------------------------|--------------------------|--------------------------|------------------------|-------------------------|
| | VDDA_1P0 Analog Supplies | VDD_1P0 Digital Supply | VDDA_1P3 Analog Supplies | VDDA_1P8 Analog Supplies | VDD_1P8 Digital Supply | |
| 1 × Transmitter RF Attenuation = 0 dB, Full-Scale Continuous Wave 40 MHz Transmitter Bandwidth, 61.44 MSPS Data Rate, Transmitter QEC Disabled, QEC Engine Inactive, and Receiver in Primed State | Not used | 140 | 486 | 143 | 28 | 1.080 |
| 1 × Transmitter RF Attenuation = 10 dB, Full-Scale Continuous Wave 40 MHz Transmitter Bandwidth, 61.44 MSPS Data Rate, Transmitter QEC Disabled, QEC Engine Inactive, and Receiver in Primed State | Not used | 141 | 486 | 66 | 28 | 0.942 |
| 1 × Transmitter RF Attenuation = 0 dB, Full-Scale Continuous Wave 40 MHz Transmitter Bandwidth, 61.44 MSPS Data Rate, Transmitter QEC Enabled, QEC Engine Active, Receiver in Primed State, Transmitter QEC Tracking Always On, Observation Receiver Continuously On, and Transmitter Tracking is Duty Cycled (Practical Scenario) | Not used | 232 | 754 | 156 | 28 | 1.543 |
| 1 × Transmitter RF Attenuation = 10 dB, Full-Scale Continuous Wave 40 MHz Transmitter Bandwidth, 61.44 MSPS Data Rate, Transmitter QEC Enabled, QEC Engine Active, Receiver in Primed State, Transmitter QEC Tracking Always On, Observation Receiver Continuously On, and Transmitter Tracking is Duty Cycled (Practical Scenario) | Not used | 231 | 755 | 79 | 28 | 1.405 |

FDD Operation

Transmit channel enabled, 40 MHz transmitter bandwidth, 61.44 MSPS data rate, transmitter internal LO = 2.4 GHz, transmit QEC disabled, QEC engine inactive, LVDS SSI. Receive channel enabled, 40 MHz receiver bandwidth, 61.44 MSPS data rate, receiver internal LO = 2.5 GHz, high performance clock PLL, high performance receiver ADC low rate, receive QEC enabled, and QEC engine active. Using a low power ADC decreases power consumption by approximately 110 mW per receiver channel. No auxiliary DACs or auxiliary ADCs are enabled.

Table 11. FDD Modes

| ADRV9002 Mode Conditions | Supply (mA) | | | | | Total Average Power (W) |
|--|--------------------------|------------------------|--------------------------|--------------------------|------------------------|-------------------------|
| | VDDA_1P0 Analog Supplies | VDD_1P0 Digital Supply | VDDA_1P3 Analog Supplies | VDDA_1P8 Analog Supplies | VDD_1P8 Digital Supply | |
| 1 × Receiver, 1 × Transmitter RF Attenuation = 0 dB, Full-Scale Continuous Wave | Not used | 298 | 835 | 179 | 28 | 1.756 |
| 1 × Receiver, 1 × Transmitter RF Attenuation = 10 dB, Full-Scale Continuous Wave | Not used | 298 | 835 | 103 | 28 | 1.619 |
| 2 × Receiver, 2 × Transmitter RF Attenuation = 0 dB, Full-Scale Continuous Wave | Not used | 507 | 1234 | 344 | 53 | 2.826 |
| 2 × Receiver, 2 × Transmitter RF Attenuation = 10 dB, Full-Scale Continuous Wave | Not used | 507 | 1234 | 190 | 53 | 2.549 |

TIMING SPECIFICATIONS

Table 12.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----|-----|-----|------|---|
| SERIAL PERIPHERAL INTERFACE (SPI) TIMING | | | | | |
| t _{CP} | 28 | | | ns | SPI_CLK period, 3-wire mode |
| | 22 | | | ns | SPI_CLK period, 4-wire mode |
| t _{MP} | 10 | | | ns | SPI_CLK pulse width |
| t _{SC} | 3 | | | ns | SPI_EN setup to first SPI_CLK rising edge |

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Table 12.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|------|-----|----------|---------|--|
| t_{HC} | 0 | | | ns | Last SPI_CLK falling edge to SPI_EN hold |
| t_S | 2 | | | ns | SPI_DIO data input setup to SPI_CLK |
| t_H | 0 | | | ns | SPI_DIO data input hold to SPI_CLK |
| t_{CO} | 3 | | 15 | ns | SPI_CLK falling edge to output data delay (3-wire mode) |
| | 3 | | 10 | ns | SPI_CLK falling edge to output data delay (4-wire mode) |
| t_{HZM} | | | t_H | ns | Bus turnaround time after the baseband processor drives the last address bit |
| t_{HZS} | 0 | | t_{CO} | ns | Bus turnaround time after the ADRV9002 drives the last address bit, not shown in Figure 2 |
| DIGITAL TIMING ¹ | | | | | |
| TX1_ENABLE or TX2_ENABLE Pulse Width | 10 | | | μ s | |
| RX1_ENABLE or RX2_ENABLE Pulse Width | 10 | | | μ s | |
| TX1_ENABLE or TX2_ENABLE Valid Data | | 2 | | μ s | |
| RX1_ENABLE or RX2_ENABLE Valid Data | | 2 | | μ s | |
| DIGITAL DATA TIMING (LVDS SSI) | | | | | |
| TXx_DCLK_IN \pm , RXx_DCLK_OUT \pm and TXx_DCLK_OUT \pm Clock Period | 2 | | | ns | Zero on-chip lane skew and an adjustable delay of ± 300 ps available per lane 500 MHz |
| TXx_DCLK_IN \pm , RXx_DCLK_OUT \pm and TXx_DCLK_OUT \pm Pulse Width | 1 | | | ns | |
| Transmitter Data | | | | | |
| TXx_IDATA_IN \pm or TXx_QDATA_IN or TXx_STROBE_IN \pm Setup to TXx_DCLK_IN \pm | 0.22 | | | ns | |
| TXx_IDATA_IN \pm or TXx_QDATA_IN \pm or TXx_STROBE_IN \pm Hold to TXx_DCLK_IN \pm | 0.39 | | | ns | |
| Receiver Data | | | | | |
| RXx_DCLK_OUT \pm to RXx_IDATA_OUT \pm or RXx_QDATA_OUT \pm or RXx_STROBE_OUT \pm Delay | | | 0.2 | ns | DC-coupled |
| DIGITAL DATA TIMING (CMOS-SSI) | | | | | |
| TXx_DCLK_IN \pm , RXx_DCLK_OUT \pm and TXx_DCLK_OUT \pm Clock Period | 12.5 | | | ns | 80 MHz |
| TXx_DCLK_IN \pm , RXx_DCLK_OUT \pm and TXx_DCLK_OUT \pm Pulse Width | 6.25 | | | ns | |
| Transmitter Data | | | | | |
| TXx_DATA_IN \pm or TXx_STROBE_IN \pm Setup to TXx_DCLK_IN \pm | 2 | | | ns | |
| TXx_DATA_IN \pm or TXx_STROBE_IN \pm Hold to TXx_DCLK_IN \pm | 2 | | | ns | |
| Receiver Data | | | | | |
| RXx_DCLK_OUT \pm to RXx_DATA_OUT \pm or RXx_STROBE_OUT \pm Delay | | | 4.5 | ns | DC-coupled |
| MULTICHIP SYNCHRONIZATION (MCS) TIMING | | | | | |
| LVDS Setup | | | 0.62 | ns | |
| LVDS Hold | | | 0 | ns | |
| CMOS Setup | | | 1 | ns | |
| CMOS Hold | | | 3 | ns | |

¹ TX1_ENABLE, TX2_ENABLE, RX1_ENABLE, and RX2_ENABLE are the channel enabling and disabling signals.

SPECIFICATIONS

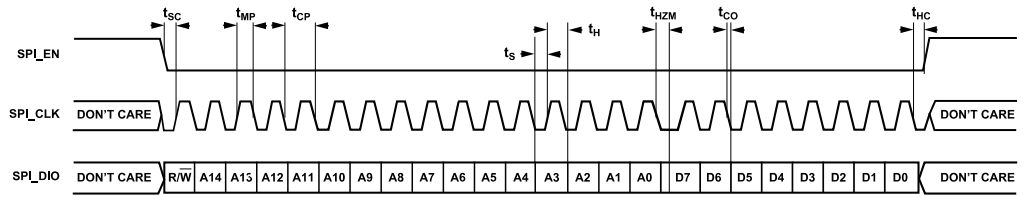


Figure 2. 3-Wire SPI Timing with Parameter Labels, SPI Read

ABSOLUTE MAXIMUM RATINGS

Table 13.

| Parameter | Rating |
|--|---|
| VDDA_1P0 to VSSA | -0.2 V to +1.2 V |
| VDDA_1P3 to VSSA | -0.2 V to +1.5 V |
| VDDA_1P8 to VSSA | -0.3 V to +2.2 V |
| VDD_1P0 to VSSD | -0.2 V to +1.2 V |
| VDD_1P8 to VSSD | -0.3 V to +2.2 V |
| Input Current to Any Pin Except Supplies | ±10 mA |
| Maximum Input Power into RF Ports | See Table 14 for limits vs. survival time |
| Junction Temperature Range | -40°C to +110°C |
| Storage Temperature Range | -65°C to +150°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 14. Maximum Input Power into RF Ports vs. Lifetime

| RF Port Input Power, Continuous Wave Signal (dBm) | Lifetime | |
|---|--|---------------------------------------|
| | 30 dB of Attenuation from Maximum Gain | 0 dB of Attenuation from Maximum Gain |
| 7 | >10 years | >10 years |
| 10 | >10 years | 20000 hours |
| 20 | >10 years | 14 hours |
| 23 | >10 years | 110 minutes |
| 25 | >7 years | 60 minutes |

REFLOW PROFILE

The ADRV9002 reflow profile is in accordance with the JEDEC JESD20 criteria for Pb-free devices. The maximum reflow temperature is 260°C.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

The thermal resistance values specified in Table 15 are calculated based on JEDEC specifications (unless specified otherwise) and must be used in compliance with JESD51-12. Note that using enhanced heat removal techniques (PCB, heat sink, airflow, and so on) improves thermal resistance.

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

θ_{JC_TOP} is the thermal resistance from the junction to the top of the package case.

Table 15. Thermal Resistance Values^{1, 2}

| Package Type | θ_{JA} | θ_{JC_TOP} | θ_{JB} | Ψ_{JC} | Ψ_{JB} | Unit |
|--------------|---------------|--------------------|---------------|-------------|-------------|------|
| BC-196-16 | 18.21 | 0.04 | 3.96 | 0.02 | 3.63 | °C/W |

¹ For test, 100 μ m thermal interface material (TIM) is used. TIM is assumed to have 3.6 W/mK.

² Using enhanced heat removal (PCB, heat sink, airflow, and so on) techniques improve thermal resistance values.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADRV9002

Table 16. ADRV9002, 196-Ball CSP_BGA

| ESD Model | Withstand Threshold (V) | Class |
|--------------------------|-------------------------|-------|
| HBM | 2000 | 2 |
| CDM | 350 | C1 |
| CDM (Excluding AUXADC_2) | 500 | C2A |

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
|---|-----------------|-----------------|----------------|----------------|------------------------|------------------------|---------------|---------------|------------------------|------------------------|----------------|----------------|-----------------|-----------------|
| A | VSSA | VSSA | EXT_LO2+ | EXT_LO2- | VRVFCO2_1P3 | VRFLO2_1P0 | MODEA | RBIAS | VRFLO1_1P0 | VRVFCO1_1P3 | EXT_LO1- | EXT_LO1+ | VSSA | VSSA |
| B | RX2A- | VSSA | VSSA | VSSA | VSSA | VRVFCO2_1P0 | AUXADC_2 | AUXADC_1 | VRVFCO1_1P0 | VSSA | VSSA | VSSA | VSSA | RX1A- |
| C | RX2A+ | VSSA | RX2B+ | RX2B- | VSSA | VANA2_1P0 | VANA2_1P3 | VANA1_1P3 | VANA1_1P0 | VSSA | RX1B- | RX1B+ | VSSA | RX1A+ |
| D | VSSA | VSSA | VSSA | VSSA | VSSA | VSSA | MCS+ | MCS- | VSSA | VSSA | VSSA | VSSA | VSSA | VSSA |
| E | VRX2LO_1P0 | VRX2LO_1P3 | AGPIO_2 | VRFSYN2_1P3 | VCLKSYN_1P3 | VSSA | DEV_CLK_IN+ | DEV_CLK_IN- | VSSA | VAUXSYN_1P3 | VRFSYN1_1P3 | AGPIO_0 | VRX1LO_1P3 | VRX1LO_1P0 |
| F | VSSA | VSSA | VSSA | AGPIO_4 | AGPIO_3 | VSSA | VSSA | VSSA | VSSA | AGPIO_1 | AGPIO_10 | VSSA | VSSA | VSSA |
| G | TX2+ | VSSA | VTX2LO_1P3 | AGPIO_5 | VCLKVCO_1P3 | AGPIO_6 | VCONV_1P8 | VAGPIO_1P8 | AGPIO_8 | VAUXVCO_1P3 | AGPIO_11 | VTX1LO_1P3 | VSSA | TX1+ |
| H | TX2- | VANA2_1P8 | VTX2LO_1P0 | AUXADC_5 | VCLKVCO_1P0 | AGPIO_7 | VCONV_1P0 | VCONV_1P3 | AGPIO_9 | VAUXVCO_1P0 | AUXADC_0 | VTX1LO_1P0 | VANA1_1P8 | TX1- |
| J | VSSA | VSSA | VSSA | VSSA | VSSA | VSSA | VSSA | VSSA | VSSA | VSSA | VSSA | VSSA | VSSA | VSSA |
| K | SPI_CLK | SPI_DIO | RX2_EN | VSSA/TES_TCK+ | VSSA/TES_TCK- | DGPIO_0 | DGPIO_1 | DGPIO_2 | DGPIO_3 | DGPIO_4 | DGPIO_5 | RX1_EN | RESETB | GP_INT |
| L | SPI_EN | SPI_DO | TX2_EN | DGPIO_6 | DGPIO_7 | DGPIO_8 | VDIG_1P0 | VDIG_1P0 | DGPIO_9 | DGPIO_10 | DGPIO_11 | TX1_EN | MODE | DEV_CLK_OUT |
| M | RX2_IDAT_A_OUT- | RX2_IDAT_A_OUT+ | RX2_DCLK_OUT- | RX2_DCLK_OUT+ | DGPIO_15/TX2_DCLK_OUT+ | DGPIO_14/TX2_DCLK_OUT- | VDIGIO_1P8 | VDIG_0P9 | DGPIO_12/TX1_DCLK_OUT- | DGPIO_13/TX1_DCLK_OUT+ | RX1_DCLK_OUT+ | RX1_DCLK_OUT- | RX1_IDAT_A_OUT+ | RX1_IDAT_A_OUT- |
| N | RX2_STROBE_OUT- | RX2_STROBE_OUT+ | RX2_QDATA_OUT- | RX2_QDATA_OUT+ | TX2_DCLK_IN+ | TX2_DCLK_IN- | VSSD | VSSD | TX1_DCLK_IN- | TX1_DCLK_IN+ | RX1_QDATA_OUT+ | RX1_QDATA_OUT- | RX1_STROBE_OUT+ | RX1_STROBE_OUT- |
| P | VSSD | TX2_STROBE_IN+ | TX2_STROBE_IN- | TX2_QDATA_IN- | TX2_QDATA_IN+ | TX2_IDATA_IN+ | TX2_IDATA_IN- | TX1_IDATA_IN- | TX1_IDATA_IN+ | TX1_QDATA_IN- | TX1_QDATA_IN+ | TX1_STROBE_IN- | TX1_STROBE_IN+ | VSSD |

RF PORTS

ANALOG GND

DIGITAL GND

POWER 1.8V

POWER 1.3V

POWER 1.0V

DIGITAL GPIO

ANALOG GPIO

MULTIFUNCTION GPIO

SPI, ENABLES, RESET, MODE, DEV_CLK_OUT

SYNCHRONOUS SERIAL INTERFACE PORTS

AUX ADC

Figure 3. Pin Configuration

Table 17. Pin Function Descriptions

| Pin No. | Type | Mnemonic | Description |
|---|------------------|--------------------|---|
| A1, A2, A13, A14, B2 to B5, B10 to B13, C2, C5, C10, C13, D1 to D6, D9 to D14, E6, E9, F1 to F3, F6 to F9, F12 to F14, G2, G13, J1 to J14 | Input | VSSA | Analog Ground (V _{SSA}). |
| A3, A4 | Input | EXT_LO2+, EXT_LO2- | Differential External LO Input 1 (LO1). If EXT_LO2+ and EXT_LO2- are used for the external LO1, the input frequency must be 2x or higher than the desired carrier frequency. For an LO range from 500 MHz to 1 GHz, a 1x multiplier is available. If unused, connect EXT_LO2+ and EXT_LO2- to VSSA. |
| A5 | Input | VRVFCO2_1P3 | 1.3 V Internal LDO Regulator Input Supply for RF External LO Input 2 (LO2) VCO and LO Generation Circuitry. VRVFCO2_1P3 is sensitive to supply noise. |
| A6 | Input and Output | VRFLO2_1P0 | 1.0 V Internal Supply Node for RF LO2 LO Generation Circuitry. Connect VRFLO2_1P0 together with VRFVCO2_1P0 and bypass with a 4.7 μF capacitor when the internal LDO regulator operated from the VRFVCO2_1P3 input is in use. Provide a 1.0 V supply to VRFLO2_1P0 when the internal LDO regulator that is operated from VRFVCO2_1P3 is not in use. |
| A7 | Input | MODEA | Use MODEA to configure the boot up option for the DEV_CLK_IN± inputs and the DEV_CLK_OUT output. Connect MODEA to VSSA to enable the differential clock receiver at the DEV_CLK_IN± pins. Connect MODEA to a voltage level higher than any VSSA to enable either the single-ended clock at DEV_CLK_IN+ or the crystal oscillator resonator at both of the DEV_CLK_IN± pins. |

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 17. Pin Function Descriptions

| Pin No. | Type | Mnemonic | Description |
|--|------------------|--------------------------|---|
| A8 | Input | RBIAS | Bias Resistor Connection. RBIAS generates an internal current based on an external 1% resistor. Connect a 4.99 kΩ resistor between RBIAS and VSSA (analog ground) . |
| A9 | Input and Output | VRFLO1_1P0 | 1.0 V Internal Supply Node for RF LO1 LO Generation Circuitry. Connect VRFLO1_1P0 together with VRFVCO1_1P0 and bypass with a 4.7 μF capacitor when the internal LDO regulator operated from the VRFVCO1_1P3 input is in use. Provide a 1.0 V supply to VRFLO1_1P0 when the internal LDO regulator operated from VRFVCO1_1P3 is not in use. |
| A10 | Input | VRFVCO1_1P3 | 1.3 V Internal LDO Input Supply for RF LO1 VCO and LO Generation Circuitry. VRFVCO1_1P3 is sensitive to supply noise. |
| A11, A12 | Input | EXT_LO1-, EXT_LO1+ | Differential External LO Input 2. If EXT_LO1+ and EXT_LO1- are used for the external LO2, the input frequency must be 2× or higher than the desired carrier frequency. For an LO range from 500 MHz to 1 GHz, a 1× multiplier is available. If unused, connect EXT_LO1+ and EXT_LO1- to VSSA. |
| B1, C1 | Input | RX2A-, RX2A+ | Differential Input A for Rx2. If unused, connect RX2A- and RX2A+ to VSSA. |
| B6 | Output | VRFVCO2_1P0 | 1.0 V Internal Supply Node for RF LO2 VCO Circuitry. Connect this VRFVCO2_1P0 together with VRFLO2_1P0 and bypass with a 4.7 μF capacitor when the internal LDO regulator operated from the VRFVCO2_1P3 input is in use. |
| B7 | Input | AUXADC_2 | Input 2 to Auxiliary ADC Input Multiplexer. If unused, do not connect AUXADC_2. |
| B8 | Input | AUXADC_1 | Input 1 to Auxiliary ADC Input Multiplexer. If unused, do not connect AUXADC_1. |
| B9 | Output | VRFVCO1_1P0 | 1.0 V Internal Supply node for RF LO1 VCO Circuitry. Connect VRFVCO1_1P0 together with VRFLO1_1P0 and bypass with a 4.7 μF capacitor when the internal LDO regulator operated from the VRFVCO1_1P3 input is in use. |
| B14, C14 | Input | RX1A-, RX1A+ | Differential Input A for Rx1. If unused, connect RX1A- and RX1A+ to VSSA. |
| C3, C4 | Input | RX2B+, RX2B- | Differential Input B for Rx2. If unused, connect RX2B+ and RX2B- to VSSA. |
| C6 | Input and Output | VANA2_1P0 | 1.0 V Internal Supply Node for Tx2 and Rx2 Baseband Circuits, TIA, Transmitter Transconductance (GM) Baseband Filters, and Auxiliary DACs and ADCs. For normal operation, leave VANA2_1P0 unconnected. |
| C7 | Input | VANA2_1P3 | 1.3 V Internal LDO Input Supply for Tx2 and Rx2 Baseband Circuits, TIA, Transmitter GM, Baseband Filters, and Auxiliary DACs and ADCs. VANA2_1P3 is sensitive to supply noise. |
| C8 | Input | VANA1_1P3 | 1.3 V Internal LDO Input Supply for Tx1 and Rx1 Baseband Circuits, TIA, Transmitter GM and Baseband Filters. VANA1_1P3 is sensitive to supply noise. |
| C9 | Input and Output | VANA1_1P0 | 1.0 V Internal Supply Node for Tx1 and Rx1 Baseband Circuits, TIA, Transmitter GM and Baseband Filters. For normal operation, leave VANA1_1P0 unconnected. |
| C11, C12 | Input | RX1B-, RX1B+ | Differential Input B for Rx1. If unused, connect RX1B- and RX1B+ to VSSA. |
| D7, D8 | Input | MCS+, MCS- | Multichip Synchronization Reference Inputs. If unused, connect MCS+ and MCS- to VSSA. |
| E1 | Output | VRX2LO_1P0 | 1.0 V Internal Supply Node for Rx2 LO Buffers and Mixers. VRX2LO_1P0 is sensitive to supply noise. Bypass VRX2LO_1P0 with a 4.7 μF capacitor. |
| E2 | Input | VRX2LO_1P3 | 1.3 V Internal LDO Input Supply for Rx2 LO Buffers and Mixers. Provide a 1.0 V supply to VRX2LO_1P3 when the internal LDO regulator is not used. VRX2LO_1P3 is sensitive to supply noise. |
| E3, E12, F4, F5, F10, F11, G4, G6, G9, G11, H6, H9 | Input and Output | AGPIO_xx | GPIOs Signals Referenced to VAGPIO_1P8 1.8 V Supply. See Table 18 to match the ball location to the AGPIO_xx signal name. Some AGPIO_xx pins can also function as auxiliary DAC outputs. See Table 18 for mapping between AGPIO_xx and the auxiliary DAC signals. If unused, do not connect AGPIO_xx. |
| E4 | Input | VRFSYN2_1P3 | 1.3 V Supply for RF LO2 Synthesizer. VRFSYN2_1P3 is sensitive to supply noise. |
| E5 | Input | VCLKSYN_1P3 | 1.3 V Supply for Clock Synthesizer. VCLKSYN_1P3 is sensitive to supply noise. |
| E7, E8 | Input | DEV_CLK_IN+, DEV_CLK_IN- | Device Clock Input. DEV_CLK_IN± can operate as differential, single-ended, or be connected to the external crystal oscillator. In single-ended mode, apply the clock signal to the DEV_CLK_IN+ pin and leave the DEV_CLK_IN- pin unconnected. |
| E10 | Input | VAUXSYN_1P3 | 1.3 V Supply for Auxiliary Synthesizer. VAUXSYN_1P3 is sensitive to supply noise. |
| E11 | Input | VRFSYN1_1P3 | 1.3 V Supply for RF LO1 Synthesizer. VRFSYN1_1P3 is sensitive to supply noise. |
| E13 | Input | VRX1LO_1P3 | 1.3 V Internal LDO Input Supply for Rx1 LO Buffers and Mixers. Provide a 1.0 V supply to VRX1LO_1P3 when the internal LDO regulator is not used. VRX1LO_1P3 is sensitive to supply noise. |
| E14 | Output | VRX1LO_1P0 | 1.0 V Internal Supply Node for Rx1 LO Buffers and Mixers. VRX1LO_1P0 is sensitive to supply noise. Bypass VRX1LO_1P0 with a 4.7 μF capacitor. |
| G1, H1 | Output | TX2+, TX2- | Differential Output for Transmitter Channel 2. If unused, do not connect TX2+ and TX2-. |

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 17. Pin Function Descriptions

| Pin No. | Type | Mnemonic | Description |
|--------------------------------|------------------|--------------|---|
| G3 | Input | VTX2LO_1P3 | 1.3 V Supply for Tx2 LO Buffers, Upconverter, and LO Delay. Provide a 1.0 V supply to VTX2LO_1P3 when the internal LDO is not used. VTX2LO_1P3 is sensitive to supply noise. |
| G5 | Input | VCLKVCO_1P3 | 1.3 V Internal LDO Input Supply for Clock LO VCO and LO Generation Circuitry. VCLKVCO_1P3 is sensitive to supply noise. |
| G7 | Input | VCONV_1P8 | 1.8 V Supply for Tx1 and Tx2 DAC and Rx1 and Rx2 ADC. |
| G8 | Input | VAGPIO_1P8 | 1.8 V Supply for Auxiliary DACs, Auxiliary ADCs, and AGPIO Signals. |
| G10 | Input | VAUXVCO_1P3 | 1.3 V Internal LDO Input Supply for Auxiliary LO VCO and LO Generation Circuitry. VAUXVCO_1P3 is sensitive to supply noise. |
| G12 | Input | VTX1LO_1P3 | 1.3 V Internal LDO Input Supply for Tx1 LO Buffers, Upconverter, and LO Delay. Provide a 1.0 V supply to VTX1LO_1P3 when the internal LDO regulator is not used. VTX1LO_1P3 is sensitive to supply noise. |
| G14, H14 | Output | TX1+, TX1- | Differential Output for Transmitter Channel 1. If unused, do not connect TX1+ and TX1-. |
| H2 | Input | VANA2_1P8 | 1.8 V Supply for Rx2 Mixer, Rx2 TIA, Tx2 LPF, and Internal References. |
| H3 | Output | VTX2LO_1P0 | 1.0 V Internal Supply Node for Tx2 LO Buffers, Upconverter, and LO Delay. For normal operation, leave VTX2LO_1P0 unconnected. |
| H4 | Input | AUXADC_3 | Input 3 to Auxiliary ADC Input Multiplexer. If unused, do not connect AUXADC_3. |
| H5 | Output | VCLKVCO_1P0 | 1.0 V Internal Supply Node for Clock LO VCO and LO Generation Circuitry. Bypass VCLKVCO_1P0 with a 4.7 μ F capacitor. |
| H7 | Output | VCONV_1P0 | 1.0 V Internal Supply Node for Receiver ADCs and Transmitter DACs. Bypass VCONV_1P0 with a 4.7 μ F capacitor. |
| H8 | Input | VCONV_1P3 | 1.3 V Internal LDO Input Supply for Receiver ADCs and Transmitter DACs. Provide a 1.0 V supply to VCONV_1P3 when the internal LDO regulator is not used. VCONV_1P3 is sensitive to supply noise. |
| H10 | Output | VAUXVCO_1P0 | 1.0 V Internal Supply Node for Auxiliary LO VCO and LO Generation Circuitry. Bypass VAUXVCO_1P0 with a 4.7 μ F Capacitor. |
| H11 | Input | AUXADC_0 | Input 0 to Auxiliary ADC Input Multiplexer. If unused, do not connect AUXADC_0. |
| H12 | Output | VTX1LO_1P0 | 1.0 V Internal Supply Node for Tx1 LO Buffers, Upconverter, and LO Delay. For normal operation, leave VTX1LO_1P0 unconnected. |
| H13 | Input | VANA1_1P8 | 1.8 V Supply for Rx1 Mixer, Rx1 TIA, Tx1 LPF, Crystal Oscillator, DEV_CLK Circuitry, and Internal References. |
| K1 | Input | SPI_CLK | Serial Data Bus Clock Input. |
| K2 | Input and Output | SPI_DIO | Serial Data Input in 4-Wire Mode or Input and Output in 3-Wire Mode. |
| K3 | Input | RX2_EN | Enable Input for Rx2. If unused, do not connect RX2_EN. |
| K4 | Input | VSSA/TESTCK+ | Connect VSSA/TESTCK+ to VSSA for normal operation. |
| K5 | Input | VSSA/TESTCK- | Connect VSSA/TESTCK- to VSSA for normal operation. |
| K6 to K11, L4 to L6, L9 to L11 | Input and Output | DGPIO_xx | Digital GPIO. VDIGO_1P8 supplies 1.8 V to DGPIO_xx. See Table 18 to match the pin location to the DGPIO_xx signal name. If unused, do not connect DGPIO_xx. |
| K12 | Input | RX1_EN | Enable Input for Rx1. If unused, do not connect RX1_EN. |
| K13 | Input | RESETB | Active Low Chip Reset. |
| K14 | Output | GP_INT | General-Purpose Digital Interrupt Output Signal. If unused, do not connect GP_INT. |
| L1 | Input | SPI_EN | Active Low Serial Data Bus Chip Select. |
| L2 | Output | SPI_DO | Serial Data Output. If unused in SPI 3-wire mode, do not connect SPI_DO. |
| L3 | Input | TX2_EN | Enable Input for Transmitter Channel 2. If unused, do not connect TX2_EN. |
| L7, L8 | Input | VDIG_1P0 | 1.0 V Digital Core. Connect Pin L7 and Pin L8 together. Use a wide trace to connect the VDIG_1P0 pins to a separate power supply domain. Provide reservoir capacitance close to the chip. |
| L12 | Input | TX1_EN | Enable Input for Transmitter Channel 1. If unused, do not connect TX1_EN. |
| L13 | Input | MODE | Joint Test Action Group (JTAG) Boundary Scan Pin. See Table 19 for more information. If unused, connect MODE to VSSA. |
| L14 | Output | DEV_CLK_OUT | Single-Ended Device Clock Output. DEV_CLK_OUT provides a DEV_CLK signal or the divided version to the baseband IC. If unused, do not connect DEV_CLK_OUT. |

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 17. Pin Function Descriptions

| Pin No. | Type | Mnemonic | Description |
|-----------------|------------------|------------------------|--|
| M1 | Output | RX2_IDATA_OUT- | In LVDS SSI mode, RX2_IDATA_OUT- is the Rx2 I sample data output on the negative side or the Rx2 I and Q sample data output on the negative side. In CMOS SSI mode, RX2_IDATA_OUT- is the Rx2 Data Output 0 or the Rx2 I and Q sample data output. If unused, do not connect RX2_IDATA_OUT-. |
| M2 | Output | RX2_IDATA_OUT+ | In LVDS SSI mode, RX2_IDATA_OUT+ is the Rx2 I sample data output positive side of the differential pair or the Rx2 I and Q sample data output positive side of the differential pair. In CMOS SSI mode, RX2_IDATA_OUT+ is the Rx2 Data Output 1. If unused, do not connect RX2_IDATA_OUT+. |
| M3 | Output | RX2_DCLK_OUT- | In LVDS SSI mode, RX2_DCLK_OUT- is the Rx2 data clock output negative side. In CMOS SSI mode, RX2_DCLK_OUT- is not used. If unused, do not connect RX2_DCLK_OUT-. |
| M4 | Output | RX2_DCLK_OUT+ | In LVDS SSI mode, RX2_DCLK_OUT+ is the Rx2 data clock output positive side. In CMOS SSI mode, RX2_DCLK_OUT+ is the Rx2 data clock output. If unused, do not connect RX2_DCLK_OUT+. |
| M5 | Input and Output | DGPIO_15/TX2_DCLK_OUT+ | Digital GPIO 15. VDIGIO_1P8 supplies 1.8 V to DGPIO_15/TX2_DCLK_OUT+. Alternative function of DGPIO_15/TX2_DCLK_OUT+ is to provide the positive side of the reference clock output for the Tx2 data port in LVDS SSI mode. If unused, do not connect DGPIO_15/TX2_DCLK_OUT+. |
| M6 | Input and Output | DGPIO_14/TX2_DCLK_OUT- | Digital GPIO 14. VDIGIO_1P8 supplies 1.8 V to DGPIO_14/TX2_DCLK_OUT-. The alternative function of DGPIO_14/TX2_DCLK_OUT- is to provide the negative side of the reference clock output for the Tx2 data port in LVDS SSI mode. If unused, do not connect DGPIO_14/TX2_DCLK_OUT-. |
| M7 | Input | VDIGIO_1P8 | 1.8 V Supply Input for Data Port Interface (CMOS-SSI and LVDS SSI Mode), SPI Signals, Control Input and Output Signals, and DGPIO Interface. |
| M8 | Output | VDIG_0P9 | 1.0 V Internal Supply Node for Digital Circuitry. Bypass VDIG_0P9 with a 4.7 μ F capacitor. |
| M9 | Input and Output | DGPIO_12/TX1_DCLK_OUT- | Digital GPIO 12. VDIGIO_1P8 supplies 1.8 V to DGPIO_12/TX1_DCLK_OUT-. The alternative function of DGPIO_12/TX1_DCLK_OUT- is to provide the negative side of the reference clock output for the Tx1 data port in LVDS SSI mode. If unused, do not connect DGPIO_12/TX1_DCLK_OUT-. |
| M10 | Input and Output | DGPIO_13/TX1_DCLK_OUT+ | Digital GPIO 13. VDIGIO_1P8 supplies 1.8 V to DGPIO_13/TX1_DCLK_OUT+. The alternative function of DGPIO_13/TX1_DCLK_OUT+ is to provide the positive side of the reference clock output for the Tx1 data port in LVDS SSI mode. If unused, do not connect DGPIO_13/TX1_DCLK_OUT+. |
| M11 | Output | RX1_DCLK_OUT+ | In LVDS SSI mode, RX1_DCLK_OUT+ is the Rx1 data clock output positive side. In CMOS SSI mode, RX1_DCLK_OUT+ is the Rx1 data clock output. If unused, do not connect RX1_DCLK_OUT+. |
| M12 | Output | RX1_DCLK_OUT- | In LVDS SSI mode, RX1_DCLK_OUT- is the Rx1 data clock output negative side. In CMOS SSI mode, RX1_DCLK_OUT- is not used. If unused, do not connect RX1_DCLK_OUT-. |
| M13 | Output | RX1_IDATA_OUT+ | In LVDS SSI mode, RX1_IDATA_OUT+ is the Rx1 I sample data output positive side or the Rx1 I and Q sample data output positive side. In CMOS SSI mode, RX1_IDATA_OUT+ is the Rx1 Data Output 1. |
| M14 | Output | RX1_IDATA_OUT- | In LVDS SSI mode, RX1_IDATA_OUT- is the Rx1 I sample data output negative side or the Rx1 I and Q sample data output negative side. In CMOS SSI mode, RX1_IDATA_OUT- is the Rx1 Data Output 0 or the Rx1 I and Q sample data output. |
| N1 | Output | RX2_STROBE_OUT- | In LVDS SSI mode, RX2_STROBE_OUT- is the Rx2 strobe output negative side. In CMOS SSI mode, RX2_STROBE_OUT- is not used. If unused, do not connect RX2_STROBE_OUT-. |
| N2 | Output | RX2_STROBE_OUT+ | In LVDS SSI mode, RX2_STROBE_OUT+ is the Rx2 strobe output positive side. In CMOS SSI mode, RX2_STROBE_OUT+ is the Rx2 strobe output. If unused, do not connect RX2_STROBE_OUT+. |
| N3 | Output | RX2_QDATA_OUT- | In LVDS SSI mode, RX2_QDATA_OUT- is the Rx2 Q sample data output positive side. In CMOS SSI mode, RX2_QDATA_OUT- is the Rx2 Data Output 2. If unused, do not connect RX2_QDATA_OUT-. |
| N4 | Output | RX2_QDATA_OUT+ | In LVDS SSI mode, RX2_QDATA_OUT+ is the Rx2 Q sample data output positive side. In CMOS SSI mode, RX2_QDATA_OUT+ is the Rx2 Data Output 3. If unused, do not connect RX2_QDATA_OUT+. |
| N5 | Input | TX2_DCLK_IN+ | In LVDS SSI mode, TX2_DCLK_IN+ is the Tx2 data clock input positive side. In CMOS SSI mode, TX2_DCLK_IN+ is the Tx2 data clock input. If unused, do not connect TX2_DCLK_IN+. |
| N6 | Input | TX2_DCLK_IN- | In LVDS SSI mode, TX2_DCLK_IN- is the Tx2 data clock input negative side. In CMOS SSI mode, TX2_DCLK_IN- is not used. If unused, do not connect TX2_DCLK_IN-. |
| N7, N8, P1, P14 | Input | VSSD | Digital Supply Voltage (V_{SSD}). |
| N9 | Input | TX1_DCLK_IN- | In LVDS SSI mode, TX1_DCLK_IN- is the Tx1 data clock input negative side. In CMOS SSI mode, TX1_DCLK_IN- is not used. If unused, do not connect TX1_DCLK_IN-. |
| N10 | Input | TX1_DCLK_IN+ | In LVDS SSI mode, TX1_DCLK_IN+ is the Tx1 data clock input positive side. In CMOS SSI mode, TX1_DCLK_IN+ is the Tx1 data clock input. If unused, do not connect TX1_DCLK_IN+. |
| N11 | Output | RX1_QDATA_OUT+ | In LVDS SSI mode, RX1_QDATA_OUT+ is the Rx1 Q sample data output positive side. In CMOS SSI mode, RX1_QDATA_OUT+ is the Rx1 Data Output 3. If unused, do not connect RX1_QDATA_OUT+. |

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 17. Pin Function Descriptions

| Pin No. | Type | Mnemonic | Description |
|---------|------------------|-----------------|---|
| N12 | Output | RX1_QDATA_OUT- | In LVDS SSI mode, RX1_QDATA_OUT- is the Rx1 Q sample data output positive side. In CMOS SSI mode, RX1_QDATA_OUT- is the Rx1 Data Output 2. If unused, do not connect RX1_QDATA_OUT-. |
| N13 | Output | RX1_STROBE_OUT+ | In LVDS SSI mode, RX1_STROBE_OUT+ is the Rx1 strobe output positive side. In CMOS SSI mode, RX1_STROBE_OUT+ is the Rx1 strobe output. If unused, do not connect RX1_STROBE_OUT+. |
| N14 | Output | RX1_STROBE_OUT- | In LVDS SSI mode, RX1_STROBE_OUT- is the Rx1 strobe output negative side. In CMOS SSI mode, RX1_STROBE_OUT- is not used. If unused, do not connect RX1_STROBE_OUT-. |
| P2 | Input | TX2_STROBE_IN+ | In LVDS SSI mode, TX2_STROBE_IN+ is the Tx2 strobe input positive side. In CMOS SSI mode, TX2_STROBE_IN+ is the Tx2 strobe input. If unused, do not connect TX2_STROBE_IN+. |
| P3 | Input and Output | TX2_STROBE_IN- | In LVDS SSI mode, TX2_STROBE_IN- is the Tx2 strobe input negative side. In CMOS SSI mode, TX2_STROBE_IN- is the Tx2 reference data clock output. If unused, do not connect TX2_STROBE_IN-. |
| P4 | Input | TX2_QDATA_IN- | In LVDS SSI mode, TX2_QDATA_IN- is the Tx2 Q sample data input negative side. In CMOS SSI mode, TX2_QDATA_IN- is the Tx2 Data Input 2. If unused, do not connect TX2_QDATA_IN-. |
| P5 | Input | TX2_QDATA_IN+ | In LVDS SSI mode, TX2_QDATA_IN+ is the Tx2 Q sample data input positive side. In CMOS SSI mode, TX2_QDATA_IN+ is the Tx2 Data Input 3. If unused, do not connect TX2_QDATA_IN+. |
| P6 | Input | TX2_IDATA_IN+ | In LVDS SSI mode, TX2_IDATA_IN+ is the Tx2 I sample data input positive side or the Tx2 I and Q sample data input positive side. In CMOS SSI mode, TX2_IDATA_IN+ is the Tx2 Data Input 1. If unused, do not connect TX2_IDATA_IN+. |
| P7 | Input | TX2_IDATA_IN- | In LVDS SSI mode, TX2_IDATA_IN- is the Tx2 I sample data input negative side or the Tx2 I and Q sample data input negative side. In CMOS SSI mode, TX2_IDATA_IN- is the Tx2 Data Input 0 or the Tx2 I and Q sample data input. If unused, do not connect TX2_IDATA_IN-. |
| P8 | Input | TX1_IDATA_IN- | In LVDS SSI mode, TX1_IDATA_IN- is the Tx1 I sample data input negative side or the Tx1 I and Q sample data input negative side. In CMOS SSI mode, TX1_IDATA_IN- is the Tx1 Data Input 0 or the Tx1 I and Q sample data input. If unused, do not connect TX1_IDATA_IN-. |
| P9 | Input | TX1_IDATA_IN+ | In LVDS SSI mode, TX1_IDATA_IN+ is the Tx1 I sample data input positive side or the Tx1 I and Q sample data input positive side. In CMOS SSI mode, TX1_IDATA_IN+ is the Tx1 Data Input 1. If unused, do not connect TX1_IDATA_IN+. |
| P10 | Input | TX1_QDATA_IN+ | In LVDS SSI mode, TX1_QDATA_IN+ is the Tx1 Q sample data input positive side. In CMOS SSI mode, TX1_QDATA_IN+ is the Tx1 Data Input 3. If unused, do not connect TX1_QDATA_IN+. |
| P11 | Input | TX1_QDATA_IN- | In LVDS SSI mode, TX1_QDATA_IN- is the Tx1 Q sample data input negative side. In CMOS SSI mode, TX1_QDATA_IN- is the Tx1 Data Input 2. If unused, do not connect TX1_QDATA_IN-. |
| P12 | Input and Output | TX1_STROBE_IN- | In LVDS SSI mode, TX1_STROBE_IN- is the Tx1 strobe input negative side. In CMOS SSI mode, TX1_STROBE_IN- is the Tx1 reference data clock output. If unused, do not connect TX1_STROBE_IN-. |
| P13 | Input | TX1_STROBE_IN+ | In LVDS SSI mode, TX1_STROBE_IN+ is the Tx1 strobe input positive side. In CMOS SSI mode, TX1_STROBE_IN+ is the Tx1 strobe input. If unused, do not connect TX1_STROBE_IN+. |

TYPICAL PERFORMANCE CHARACTERISTICS

The ADRV9002 supports a signal bandwidth from 12 kHz to 40 MHz. The bandwidth of 1 MHz is the boundary to distinguish between narrow-band and wideband profiles. If the signal bandwidth is less than 1 MHz, it is considered a narrow-band profile. Otherwise, it is considered a wideband profile. The performance of the ADRV9002 is measured for both wideband and narrow-band profiles.

WIDEBAND

Device configuration profile: receiver = 40 MHz bandwidth, I/Q rate = 61.44 MHz, transmitter = 40 MHz bandwidth, I/Q rate = 61.44 MHz, device clock = 38.4 MHz, and an internal LO is used for all measurements. Measurements are at nominal power supply voltages. All RF specifications are based on measurements that include PCB and matching circuit losses, unless otherwise noted. Specifications are applicable over the lifetime of the device.

50 MHz LO

The temperature settings refer to the die temperature. All LO frequencies are set to 50 MHz, unless otherwise noted.

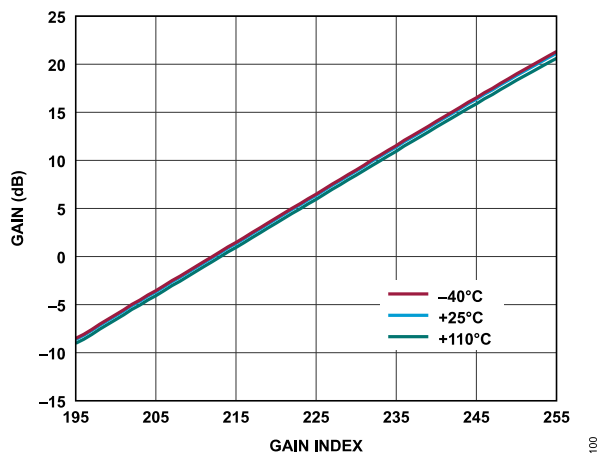


Figure 4. Receiver Absolute Gain (Complex) vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance, $P_{OUT} = -9.6$ dBFS

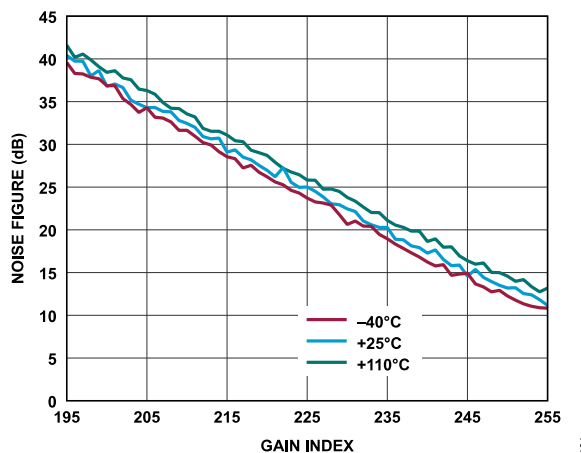


Figure 6. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

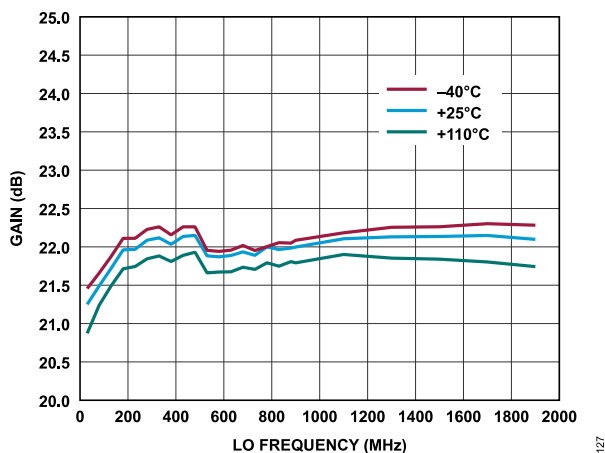


Figure 5. Receiver Absolute Gain (Complex) vs. LO Frequency, Baseband Frequency = 5.6 MHz, ADC = High Performance, $P_{OUT} = -9.6$ dBFS

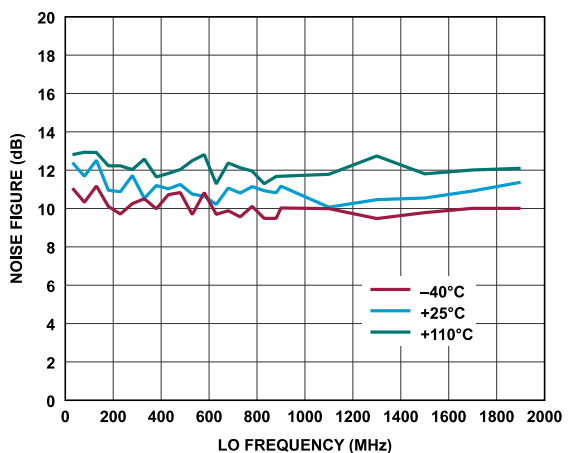


Figure 7. Receiver Noise Figure vs. LO Frequency, Baseband Frequency = 5.6 MHz, ADC = High Performance

TYPICAL PERFORMANCE CHARACTERISTICS

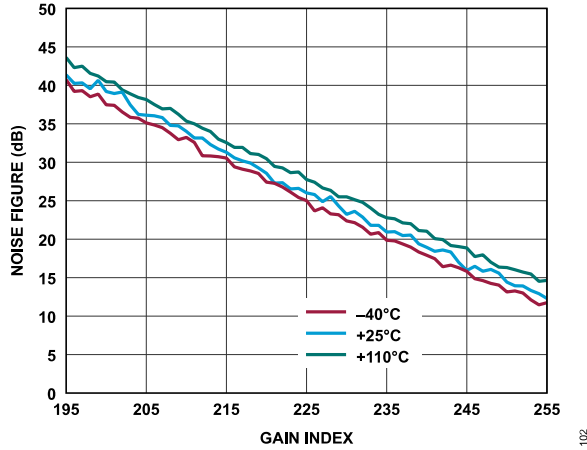


Figure 8. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = Low Power

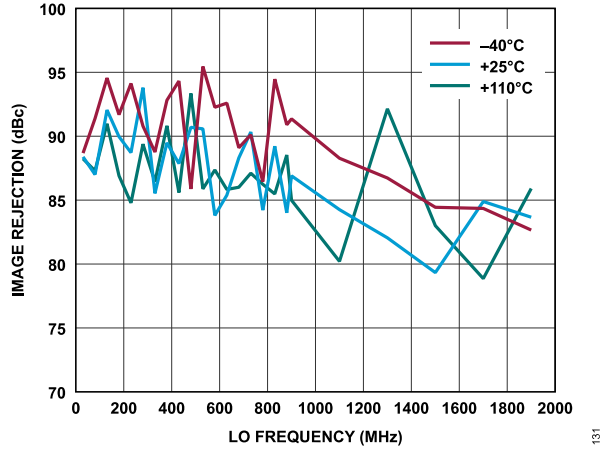


Figure 11. Receiver Image Rejection vs. LO Frequency, Baseband Frequency = 5.6 MHz, ADC = Low Power, Initialization Calibration and Hardware Tracking Calibration Only

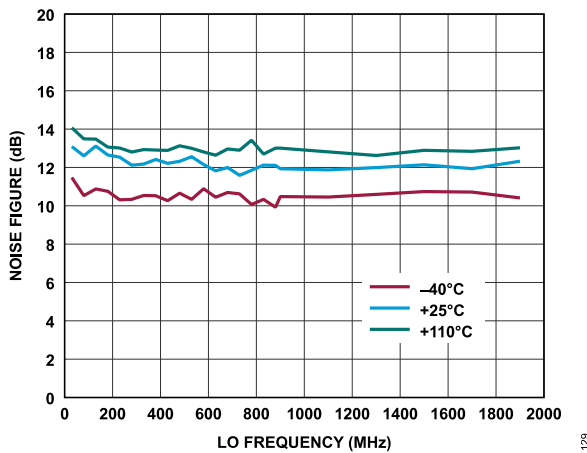


Figure 9. Receiver Noise Figure vs. LO Frequency, Baseband Frequency = 5.6 MHz, ADC = Low Power

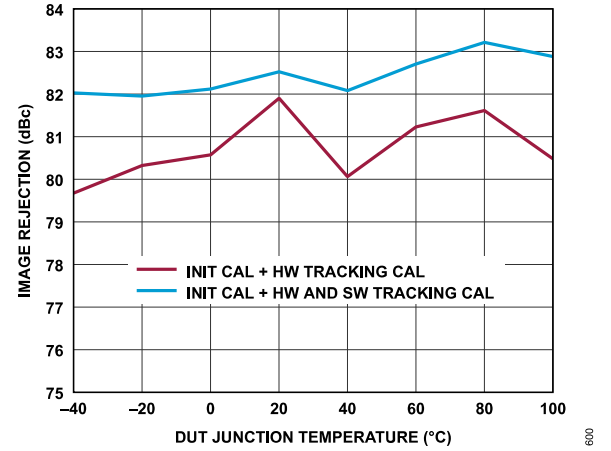


Figure 12. Receiver Image Rejection vs. DUT Junction Temperature (Low to High), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = High Performance, $P_{OUT} = -15.1$ dBFS

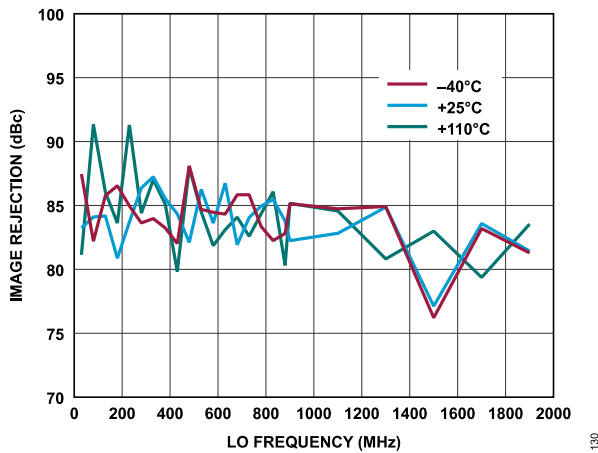


Figure 10. Receiver Image Rejection vs. LO Frequency, Baseband Frequency = 5.6 MHz, ADC = High Performance, Initialization Calibration and Hardware Tracking Calibration Only

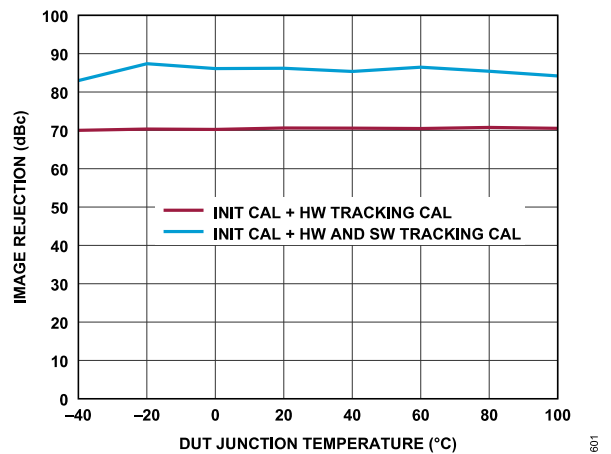


Figure 13. Receiver Image Rejection vs. DUT Junction Temperature (Low to High), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = Low Power, $P_{OUT} = -15.1$ dBFS

TYPICAL PERFORMANCE CHARACTERISTICS

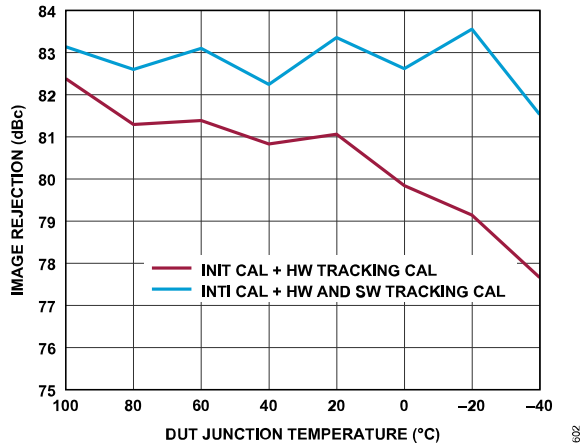


Figure 14. Receiver Image Rejection vs. DUT Junction Temperature (High to Low), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = High Performance, $P_{OUT} = -15.1$ dBFS

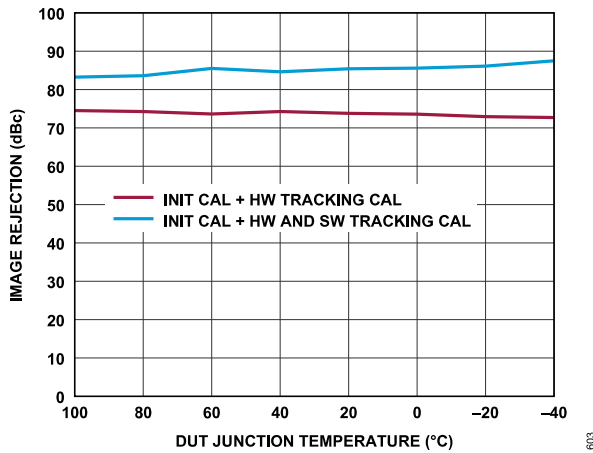


Figure 15. Receiver Image Rejection vs. DUT Junction Temperature (High to Low), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = Low Power, $P_{OUT} = -15.1$ dBFS

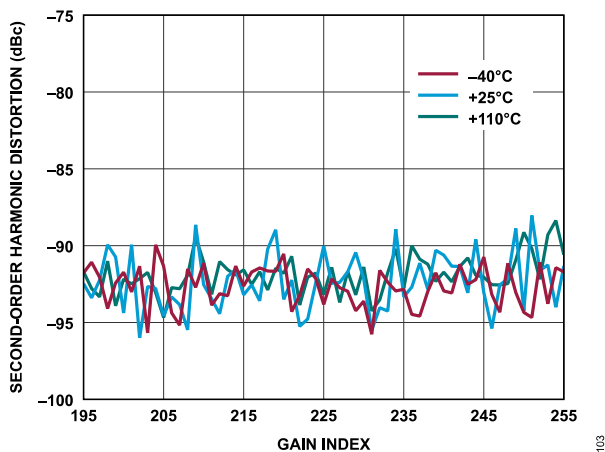


Figure 16. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

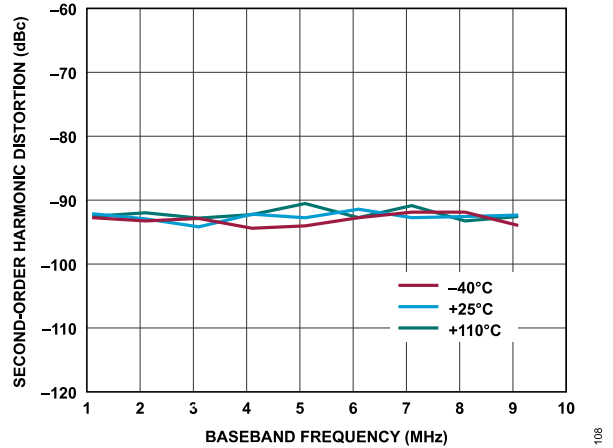


Figure 17. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

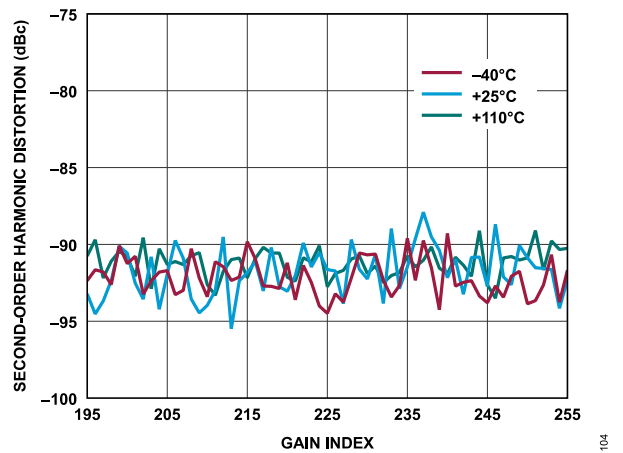


Figure 18. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = Low Power

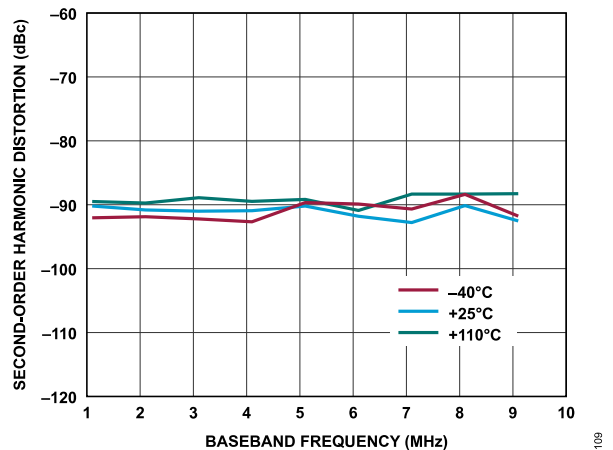


Figure 19. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = Low Power

TYPICAL PERFORMANCE CHARACTERISTICS

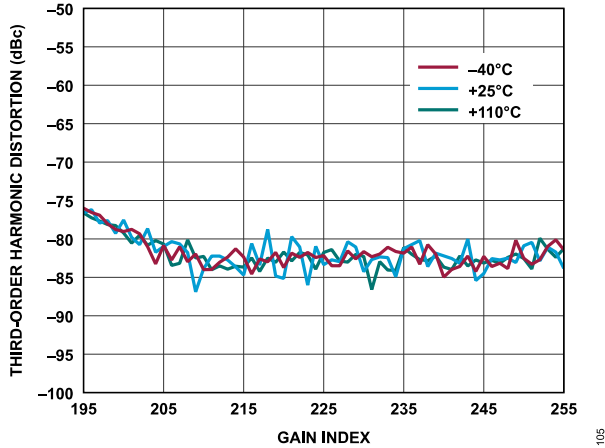


Figure 20. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

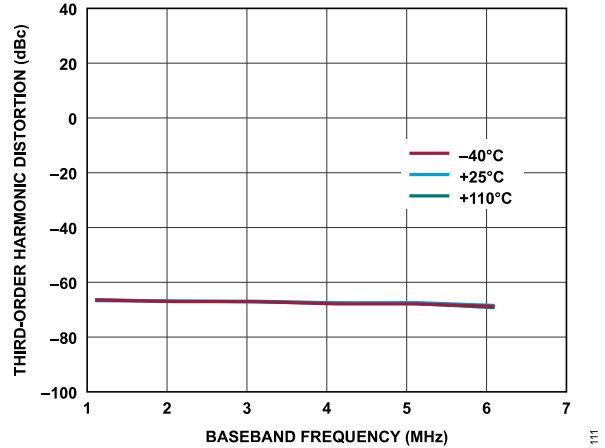


Figure 23. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = Low Power

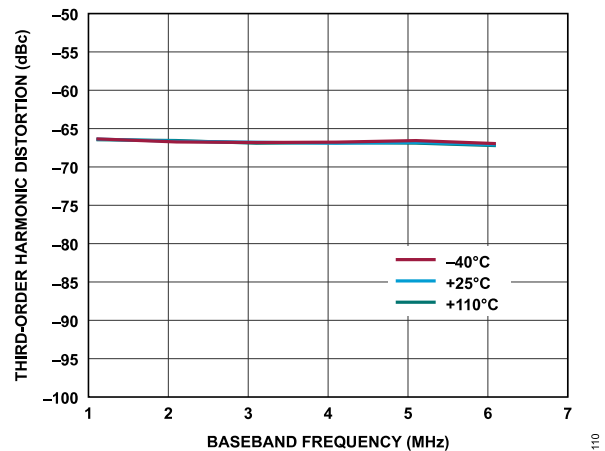


Figure 21. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

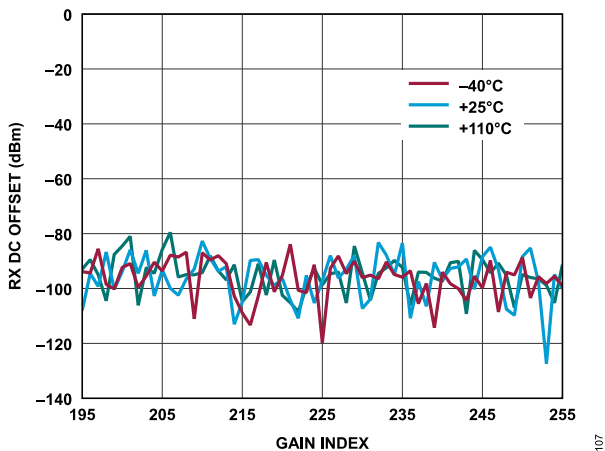


Figure 24. Receiver DC Offset vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

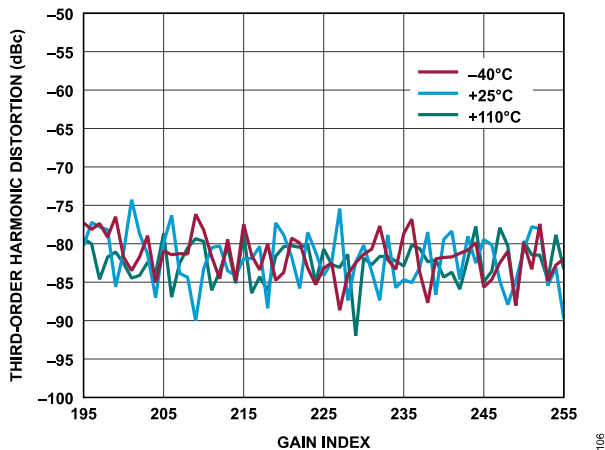


Figure 22. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = Low Power

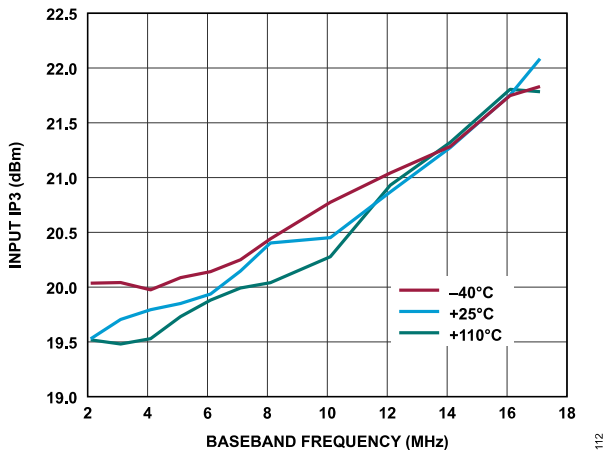


Figure 25. Receiver Input IP3 vs. Baseband Frequency, ADC = High Performance, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz, Gain Index = 255

TYPICAL PERFORMANCE CHARACTERISTICS

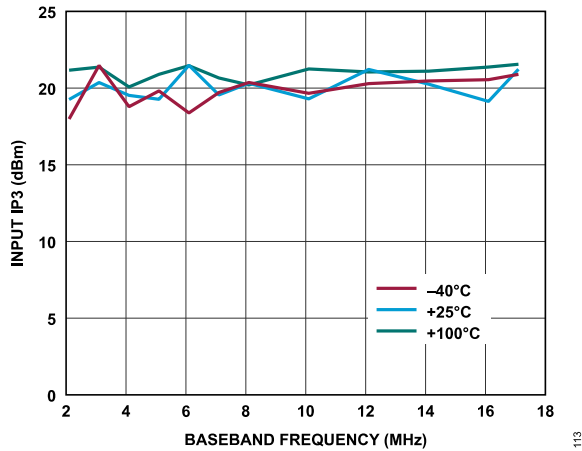


Figure 26. Receiver Input IP3 vs. Baseband Frequency, ADC = Low Power, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz, Gain Index = 255

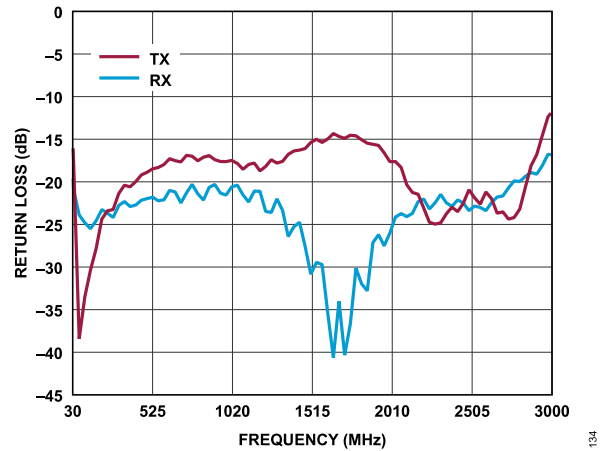


Figure 29. Receiver and Transmitter Return Loss vs. Frequency (For LO = 30 MHz to 3 GHz)

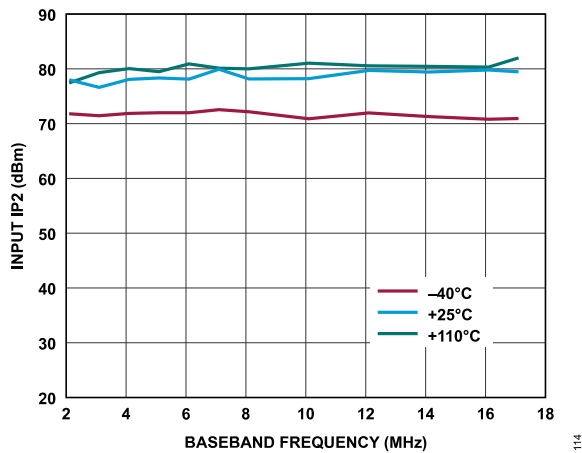


Figure 27. Receiver Input IP2 vs. Baseband Frequency, ADC = High Performance, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz, Gain Index = 255

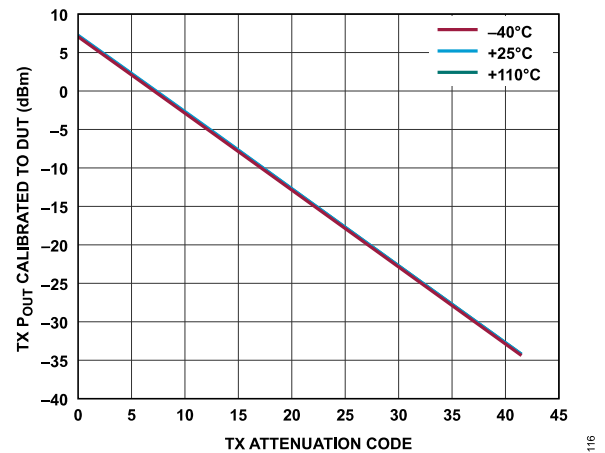


Figure 30. Transmitter Absolute Power vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

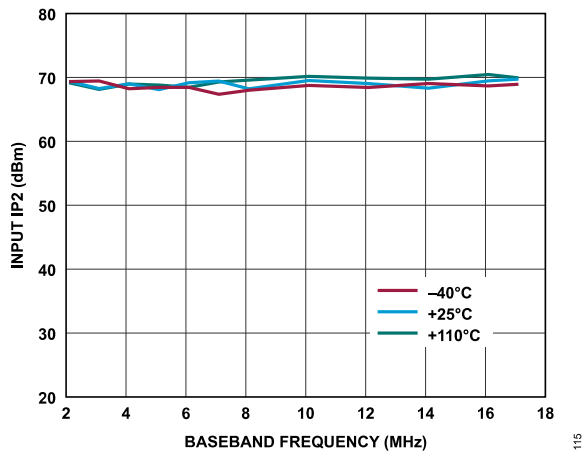


Figure 28. Receiver Input IP2 vs. Baseband Frequency, ADC = Low Power, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz, Gain Index = 255

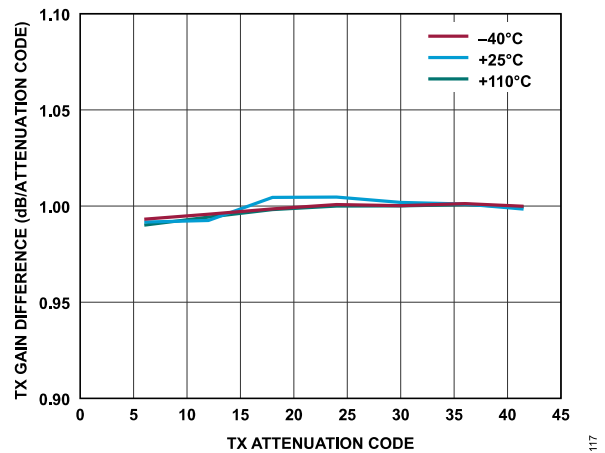


Figure 31. Transmitter Attenuation Delta (Error) vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

TYPICAL PERFORMANCE CHARACTERISTICS

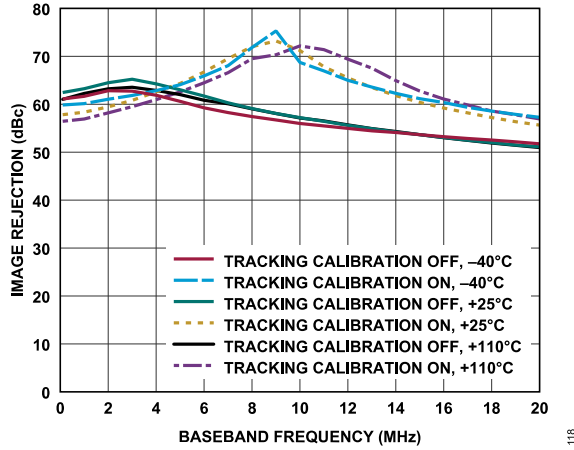


Figure 32. Transmitter Image Rejection vs. Baseband Frequency, Tracking Calibration On vs. Tracking Calibration Off, Transmitter Attenuation Code = 0

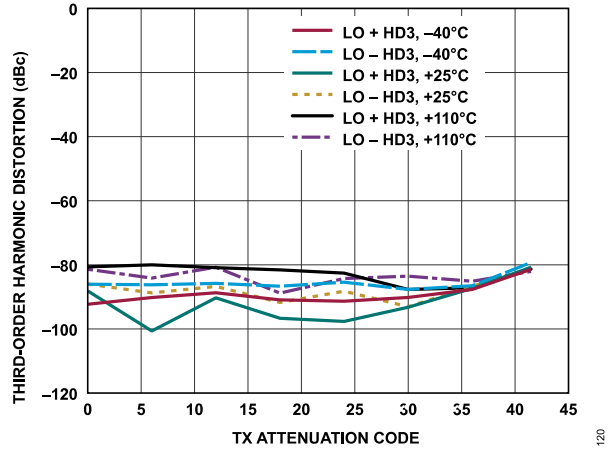


Figure 35. Transmitter Third-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

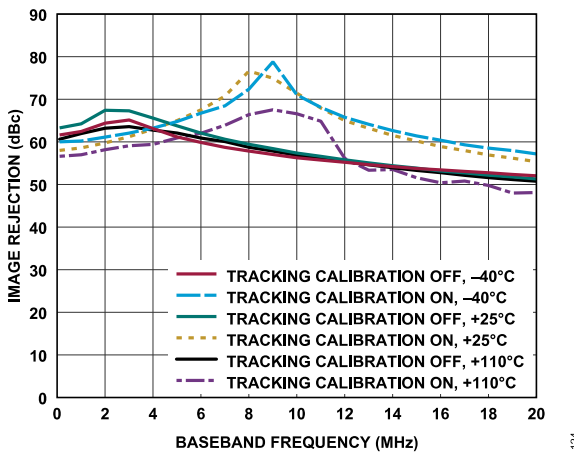


Figure 33. Transmitter Image Rejection vs. Baseband Frequency, Tracking Calibration On vs. Tracking Calibration Off, Transmitter Attenuation Code = 20

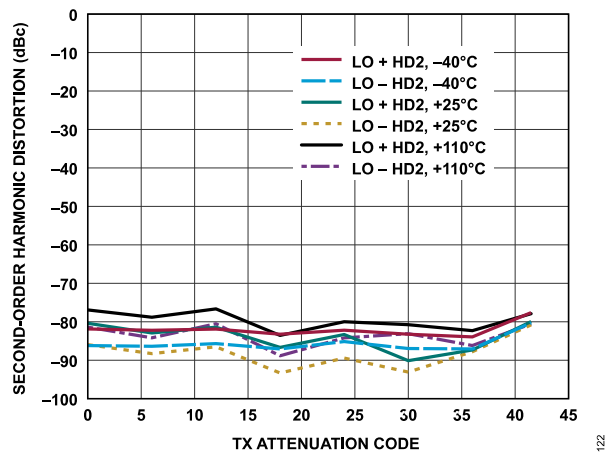


Figure 36. Transmitter Second-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

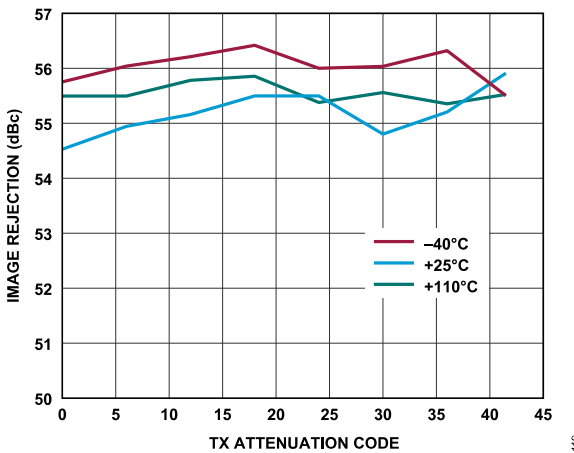


Figure 34. Transmitter Image Rejection vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS, Initialization Calibration Only

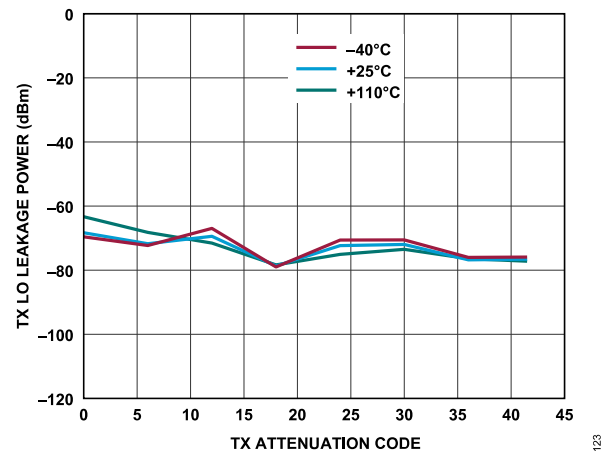


Figure 37. Transmitter LO Leakage Power vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 6 dBFS, Initialization Calibration Only

TYPICAL PERFORMANCE CHARACTERISTICS

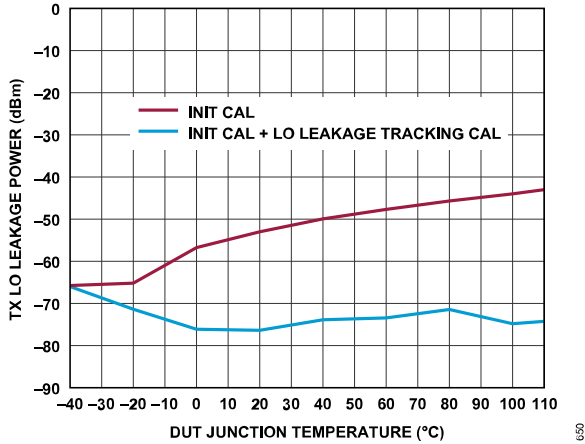


Figure 38. Transmitter LO Leakage Power vs. DUT Junction Temperature (Low to High), Baseband Frequency = 4 MHz, Backoff = 0.5 dBFS, Attenuation Code = 0

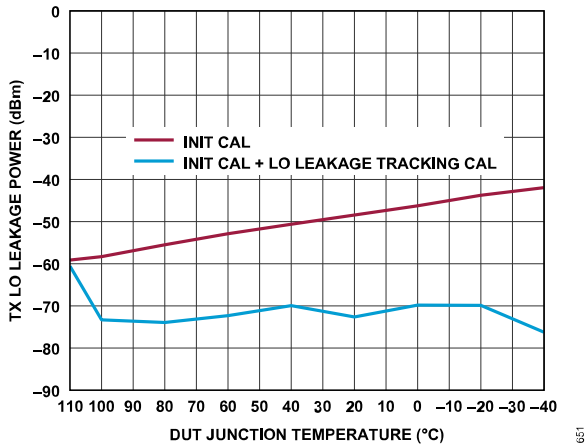


Figure 39. Transmitter LO Leakage Power vs. DUT Junction Temperature (High to Low), Baseband Frequency = 4 MHz, Backoff = 0.5 dBFS, Attenuation Code = 0

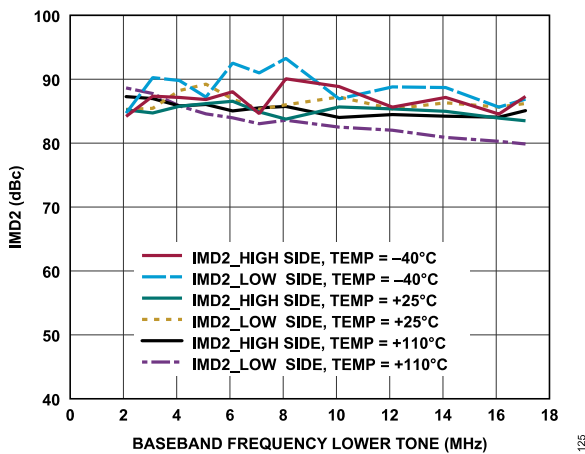


Figure 40. Transmitter Second-Order Intermodulation Distortion (IMD2) vs. Baseband Frequency, Transmitter Attenuation Code = 0, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz

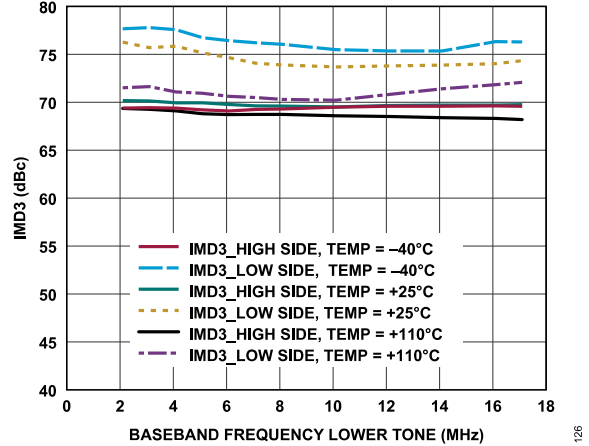


Figure 41. Transmitter Third-Order Intermodulation Distortion (IMD3) vs. Baseband Frequency, Transmitter Attenuation Code = 0, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz

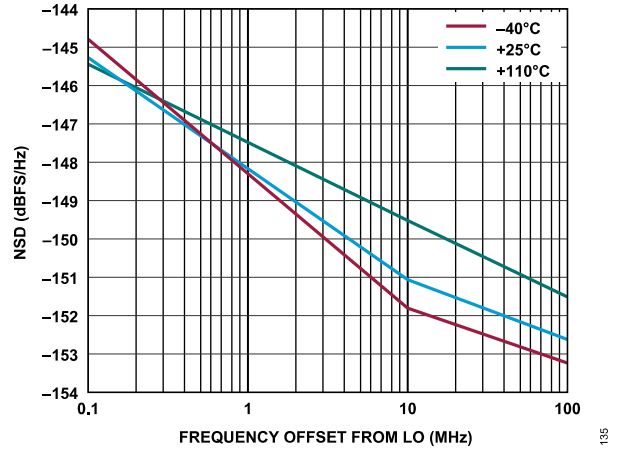


Figure 42. Transmitter NSD vs. Frequency Offset from LO, Baseband Frequency = 5.6 MHz, Transmitter Channel = Ch1

TYPICAL PERFORMANCE CHARACTERISTICS

470 MHz LO

The temperature settings refer to the die temperature. All LO frequencies set to 470 MHz, unless otherwise noted.

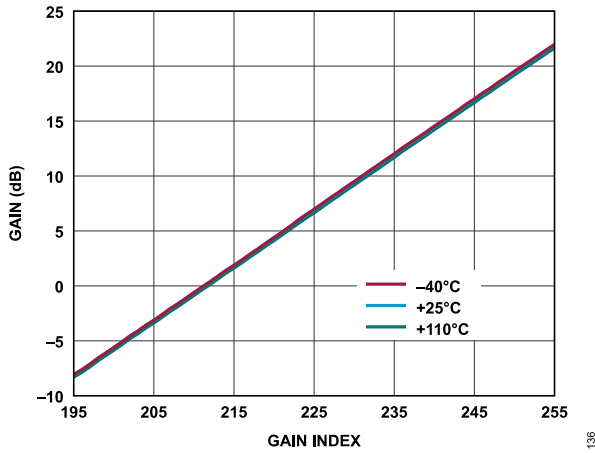


Figure 43. Receiver Absolute Gain (Complex) vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance, $P_{OUT} = -9.6$ dBFS

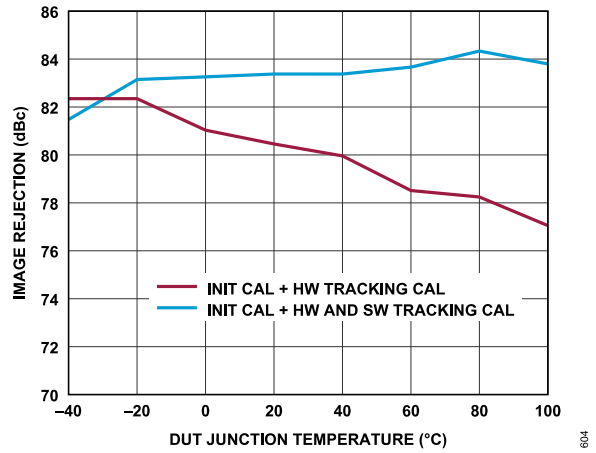


Figure 46. Receiver Image Rejection vs. DUT Junction Temperature (Low to High), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = High Performance, $P_{OUT} = -11.1$ dBFS

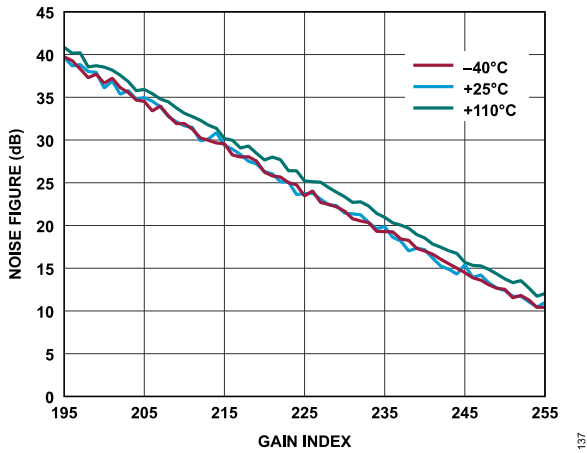


Figure 44. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

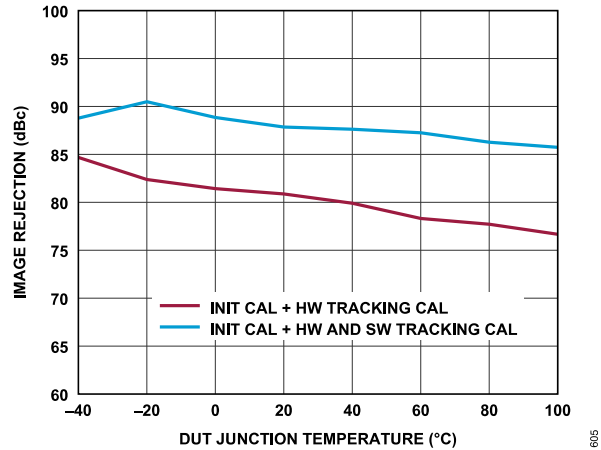


Figure 47. Receiver Image Rejection vs. DUT Junction Temperature (Low to High), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = Low Power, $P_{OUT} = -11.1$ dBFS

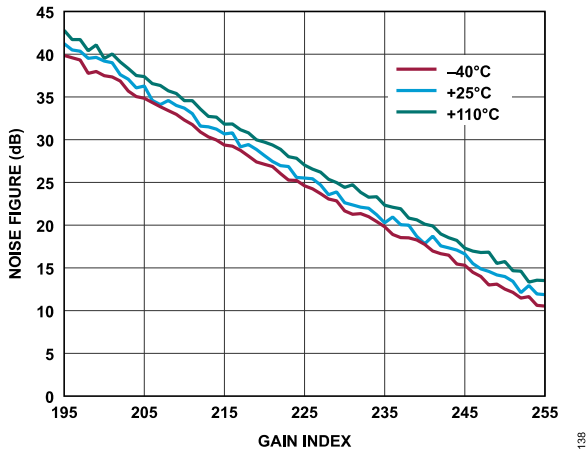


Figure 45. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = Low Power

TYPICAL PERFORMANCE CHARACTERISTICS

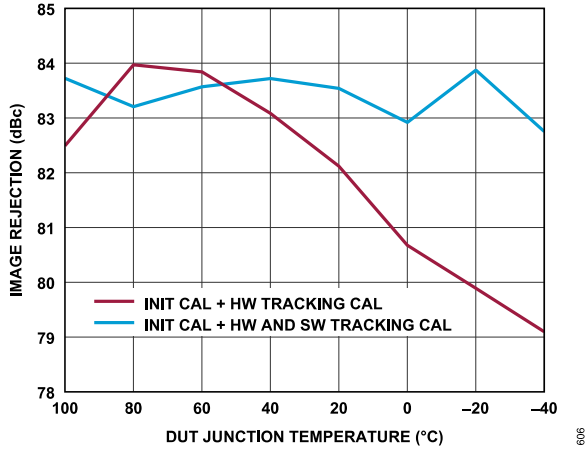


Figure 48. Receiver Image Rejection vs. DUT Junction Temperature (High to Low), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = High Performance, $P_{OUT} = -11.1$ dBFS

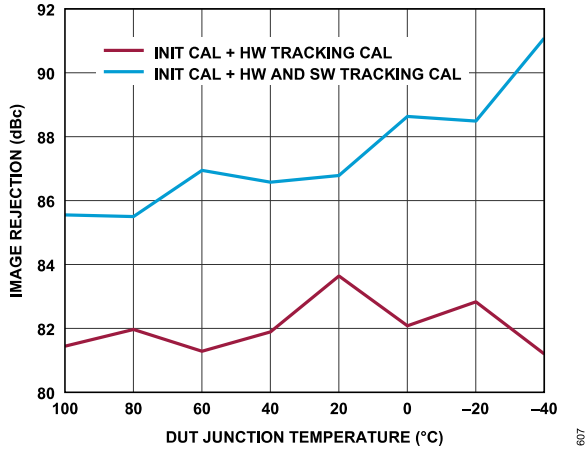


Figure 49. Receiver Image Rejection vs. DUT Junction Temperature (High to Low), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = Low Power, $P_{OUT} = -11.1$ dBFS

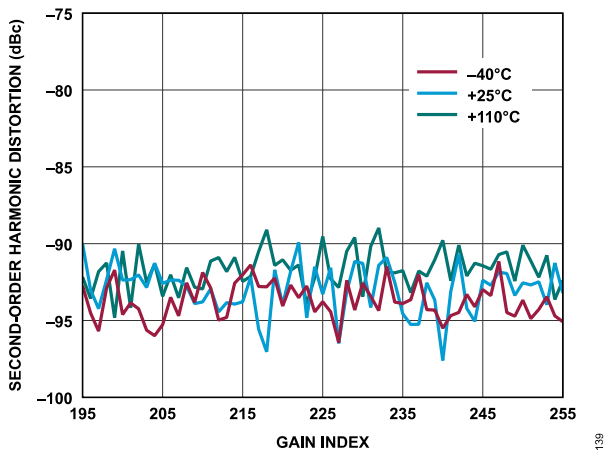


Figure 50. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

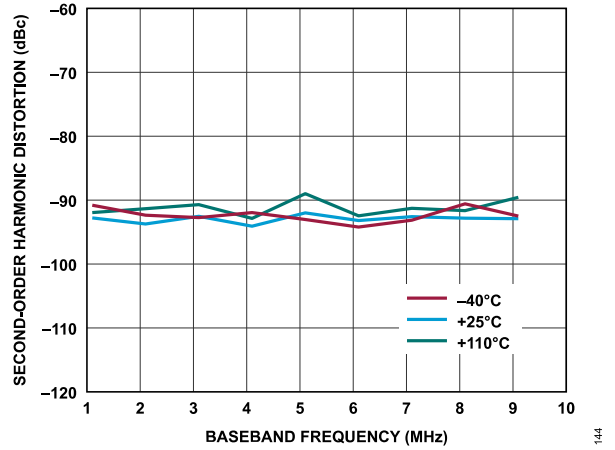


Figure 51. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

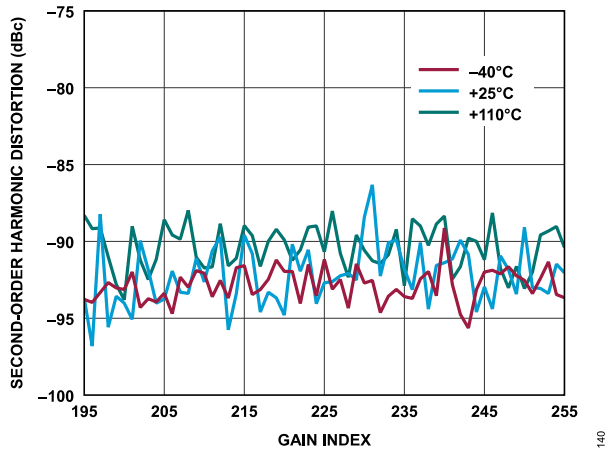


Figure 52. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = Low Power

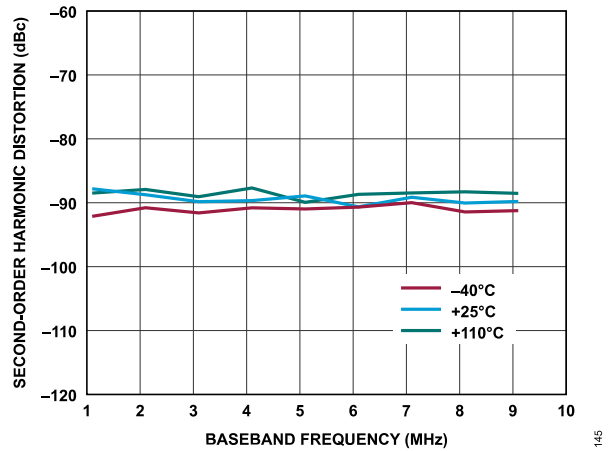


Figure 53. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = Low Power

TYPICAL PERFORMANCE CHARACTERISTICS

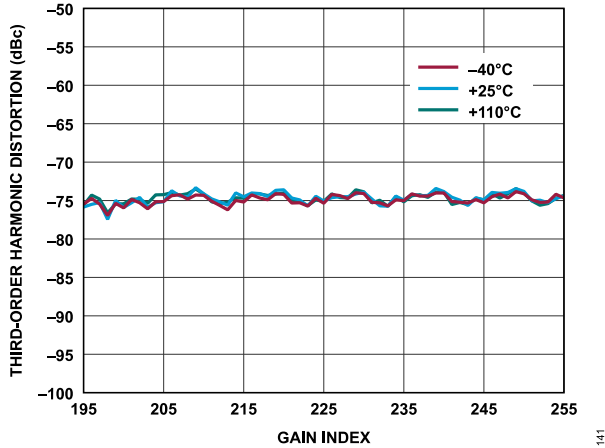


Figure 54. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

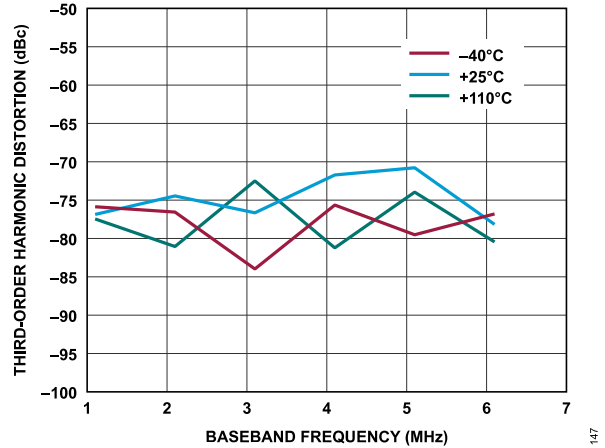


Figure 57. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = Low Power

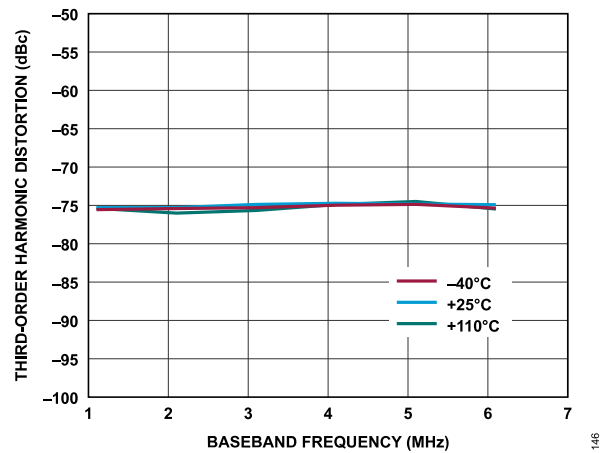


Figure 55. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

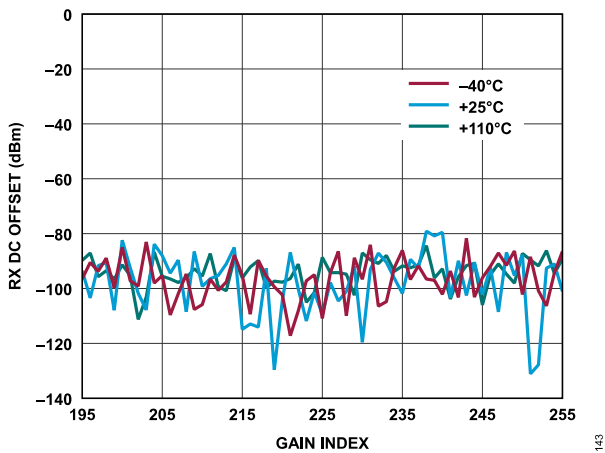


Figure 58. Receiver DC Offset vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

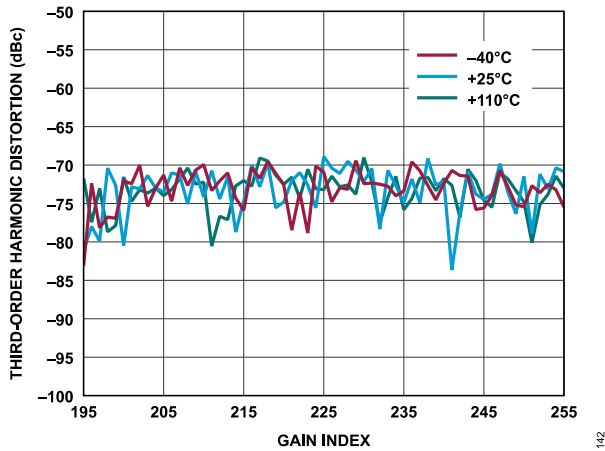


Figure 56. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = Low Power

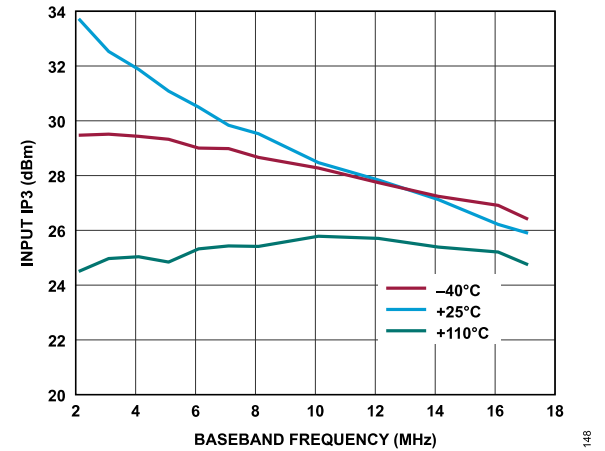


Figure 59. Receiver Input IP3 vs. Baseband Frequency, ADC = High Performance, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz, Gain Index = 255

TYPICAL PERFORMANCE CHARACTERISTICS

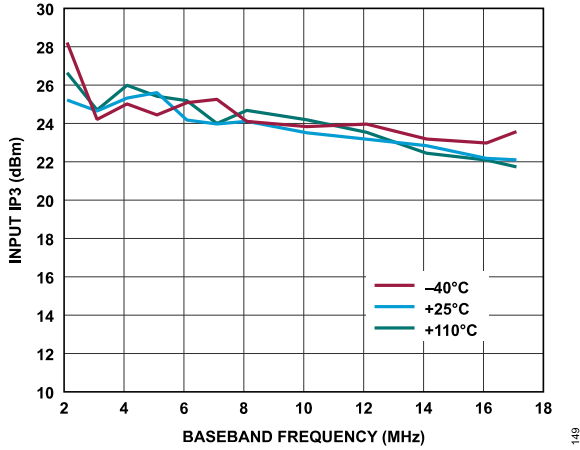


Figure 60. Receiver Input IP3 vs. Baseband Frequency, ADC = Low Power, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz, Gain Index = 255

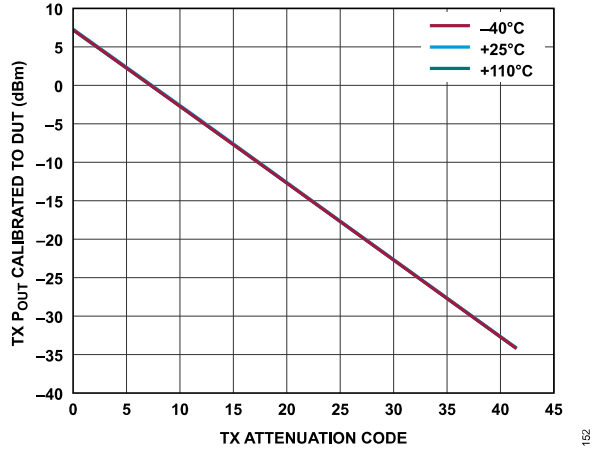


Figure 63. Transmitter Absolute Power vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

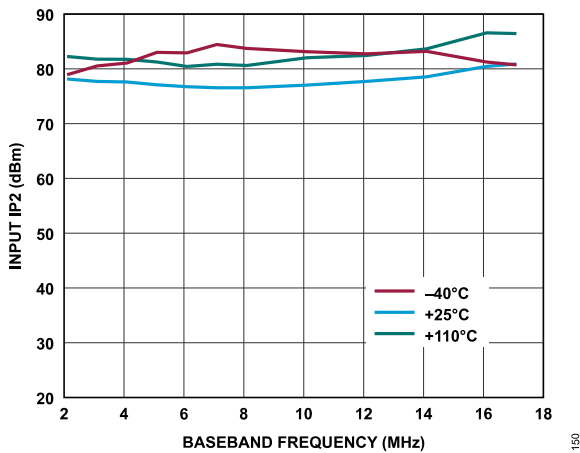


Figure 61. Receiver Input IP2 vs. Baseband Frequency, ADC = High Performance, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz, Gain Index = 255

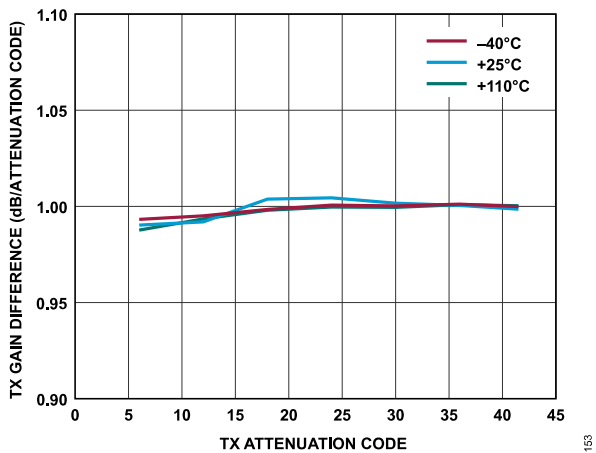


Figure 64. Transmitter Attenuation Delta (Error) vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

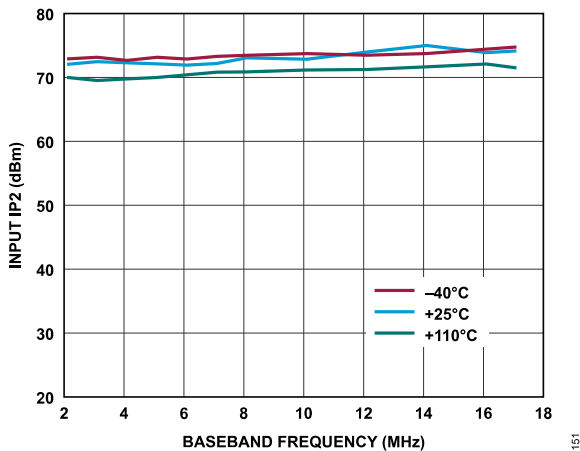


Figure 62. Receiver Input IP2 vs. Baseband Frequency, ADC = Low Power, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz, Gain Index = 255

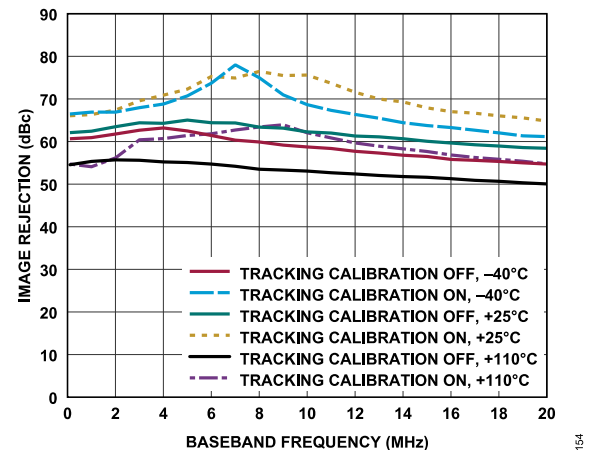


Figure 65. Transmitter Image Rejection vs. Baseband Frequency, Tracking Calibration On vs. Tracking Calibration Off, Transmitter Attenuation Code = 0

TYPICAL PERFORMANCE CHARACTERISTICS

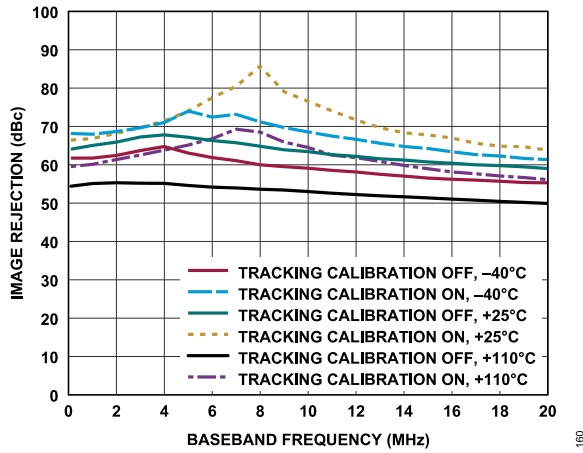


Figure 66. Transmitter Image Rejection vs. Baseband Frequency, Tracking Calibration On vs. Tracking Calibration Off, Transmitter Attenuation Code = 20

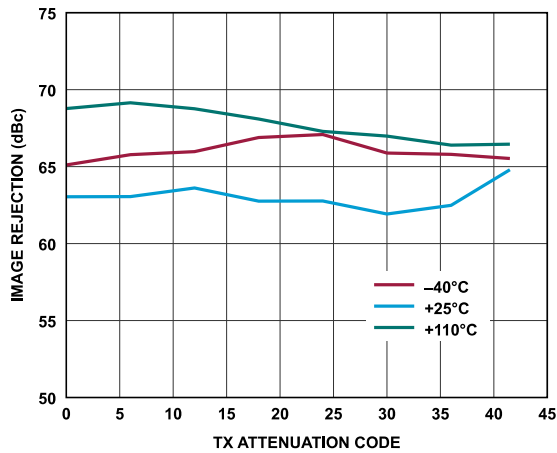


Figure 67. Transmitter Image Rejection vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS, Initialization Calibration Only

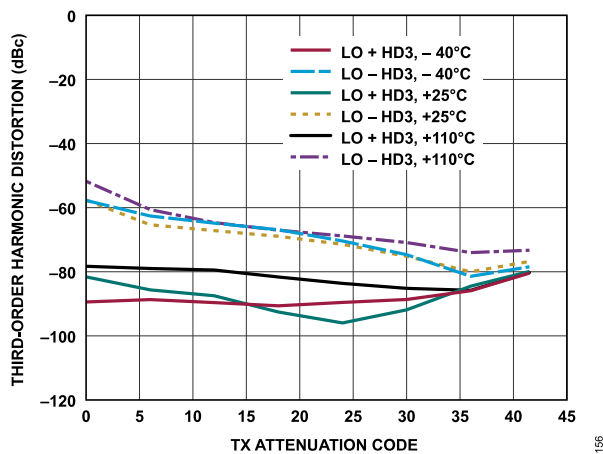


Figure 68. Transmitter Third-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

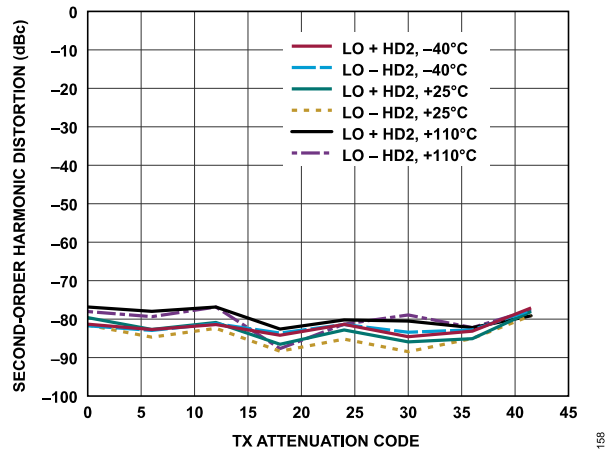


Figure 69. Transmitter Second-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

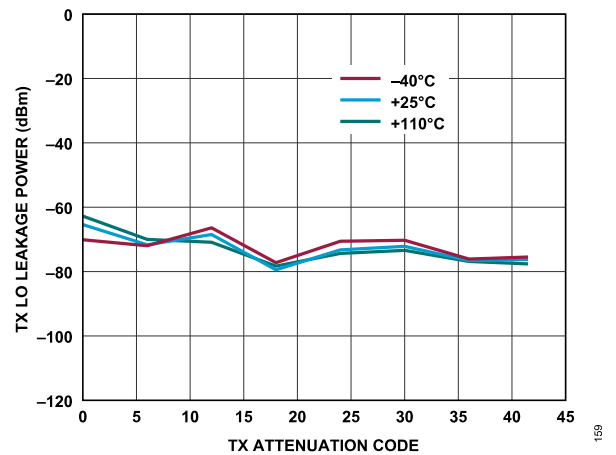


Figure 70. Transmitter LO Leakage Power vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 6 dBFS, Initialization Calibration Only

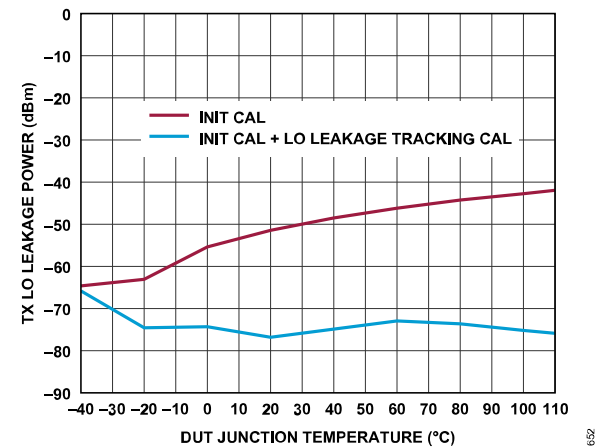


Figure 71. Transmitter LO Leakage Power vs. DUT Junction Temperature (Low to High), Baseband Frequency = 4 MHz, Backoff = 0.5 dBFS, Attenuation Code = 0

TYPICAL PERFORMANCE CHARACTERISTICS

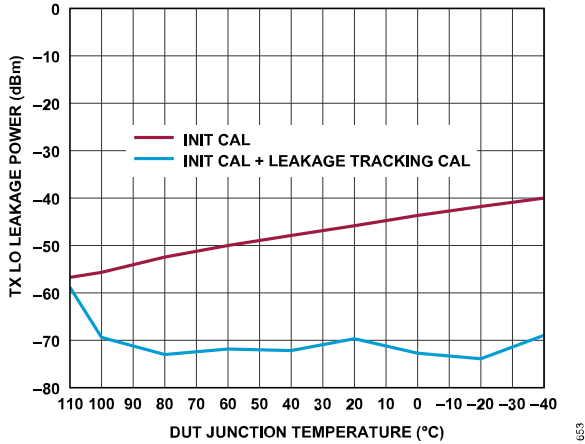


Figure 72. Transmitter LO Leakage Power vs. DUT Junction Temperature (High to Low), Baseband Frequency = 4 MHz, Backoff = 0.5 dBFS, Attenuation Code = 0

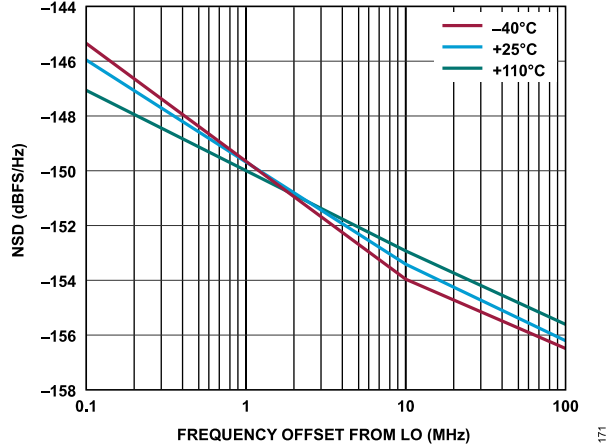


Figure 75. Transmitter NSD vs. Frequency Offset from LO, Baseband Frequency = 5.6 MHz, Transmitter Channel = Ch1

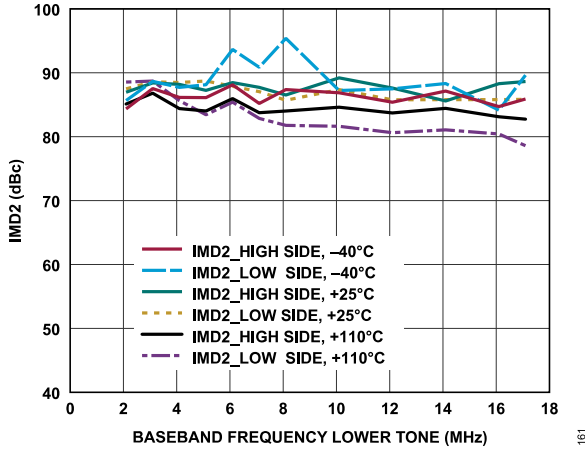


Figure 73. Transmitter IMD2 vs. Baseband Frequency, Transmitter Attenuation Code = 0, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz

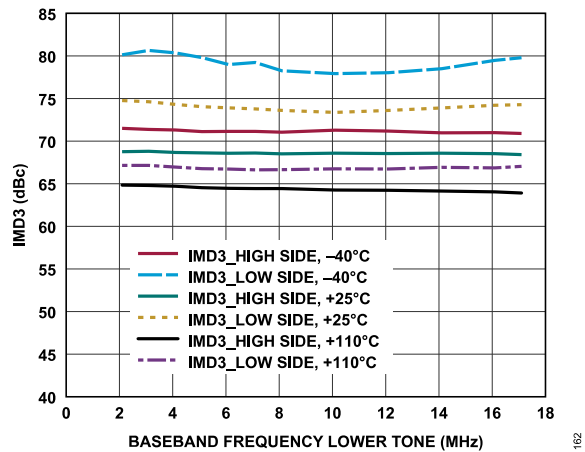


Figure 74. Transmitter IMD3 vs. Baseband Frequency, Transmitter Attenuation Code = 0, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

900 MHz LO

The temperature settings refer to the die temperature. All LO frequencies set to 900 MHz, unless otherwise noted.

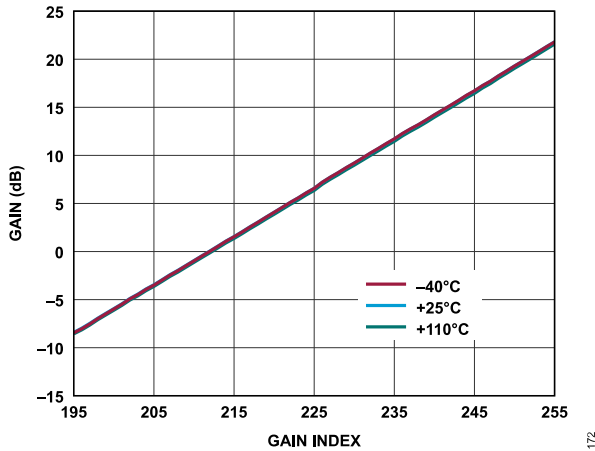


Figure 76. Receiver Absolute Gain (Complex) vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance, $P_{OUT} = -9.6$ dBFS

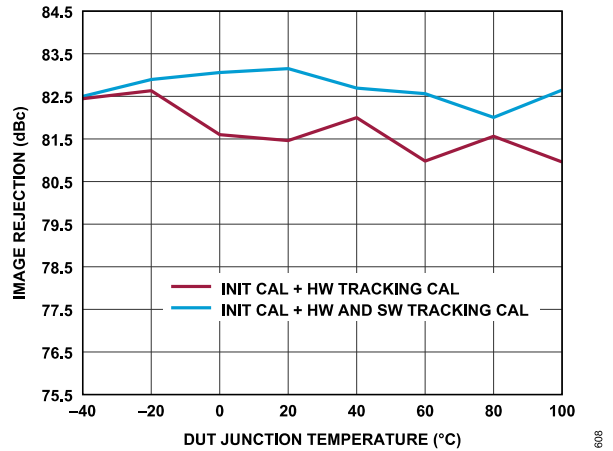


Figure 79. Receiver Image Rejection vs. DUT Junction Temperature (Low to High), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = High Performance, $P_{OUT} = -11.1$ dBFS

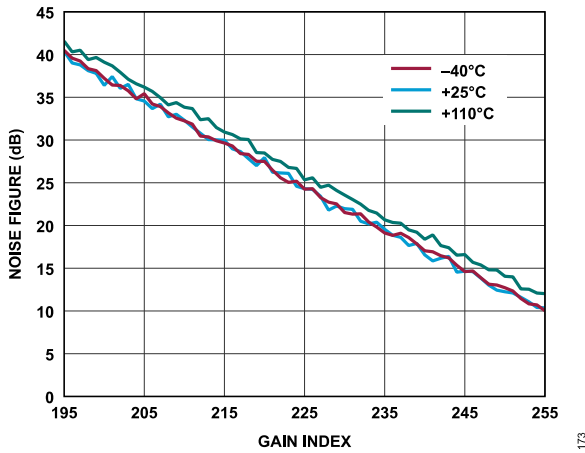


Figure 77. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

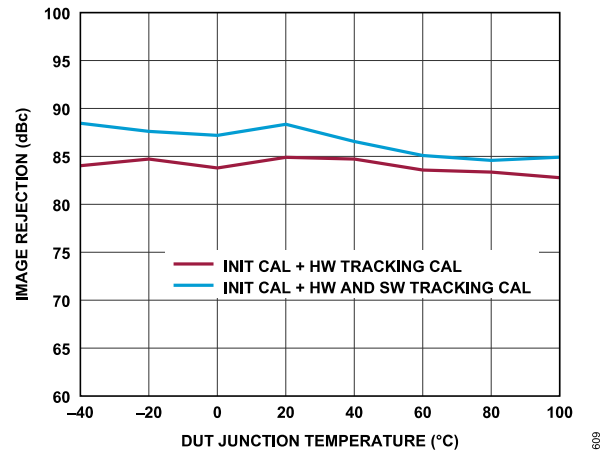


Figure 80. Receiver Image Rejection vs. DUT Junction Temperature (Low to High), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = Low Power, $P_{OUT} = -11.1$ dBFS

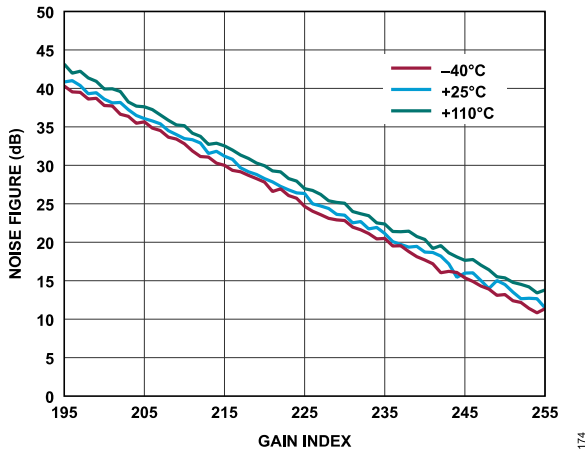


Figure 78. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = Low Power

TYPICAL PERFORMANCE CHARACTERISTICS

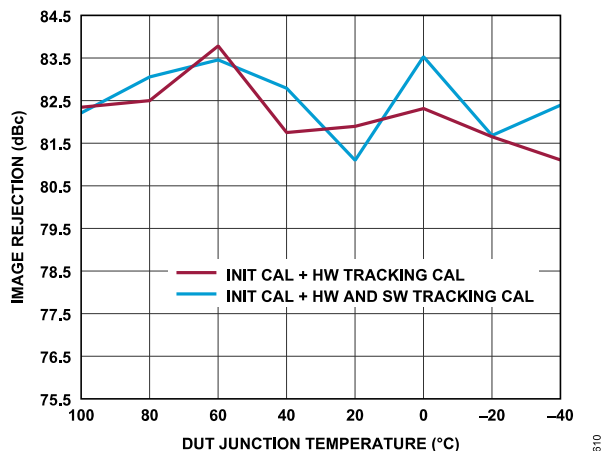


Figure 81. Receiver Image Rejection vs. DUT Junction Temperature (High to Low), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = High Performance, $P_{OUT} = -11.1$ dBFS

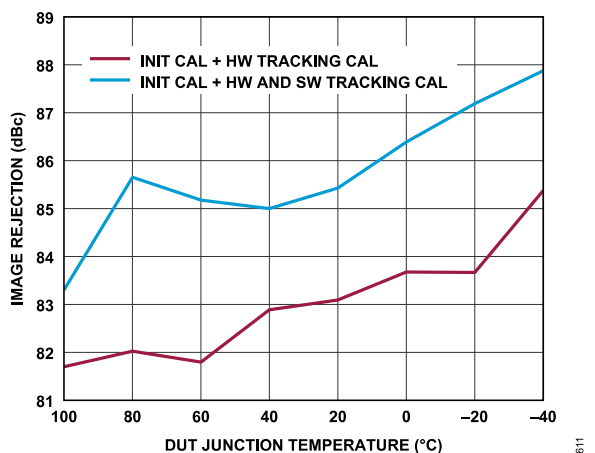


Figure 82. Receiver Image Rejection vs. DUT Junction Temperature (High to Low), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = Low Power, $P_{OUT} = -11.1$ dBFS

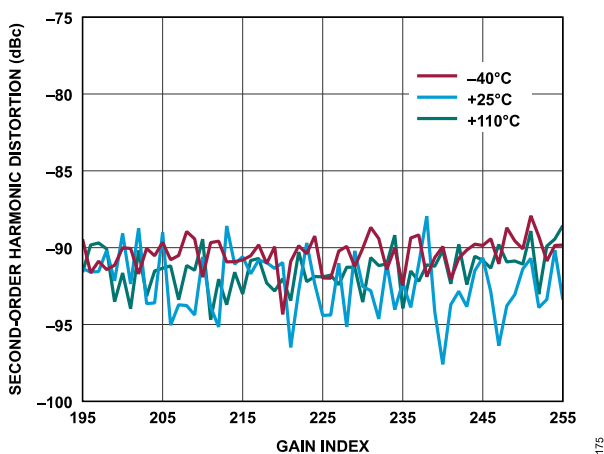


Figure 83. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

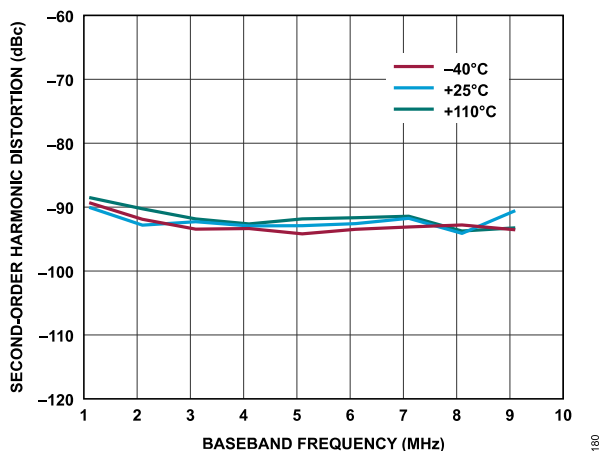


Figure 84. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

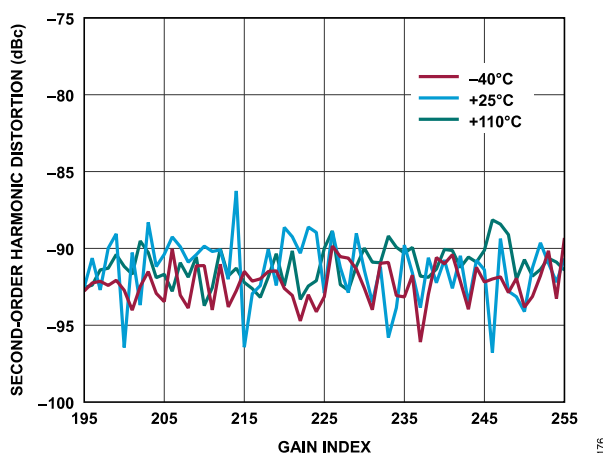


Figure 85. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = Low Power

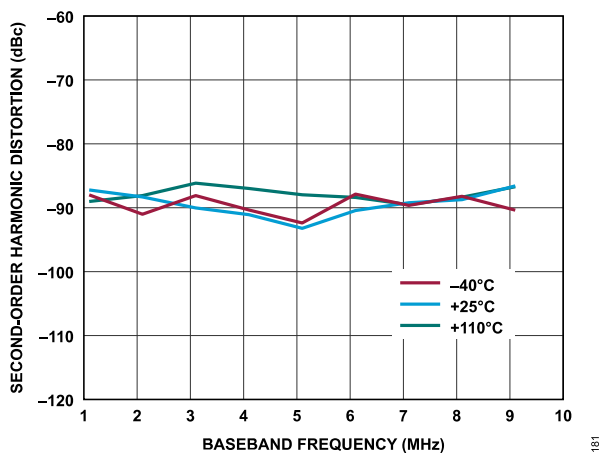


Figure 86. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = Low Power

TYPICAL PERFORMANCE CHARACTERISTICS

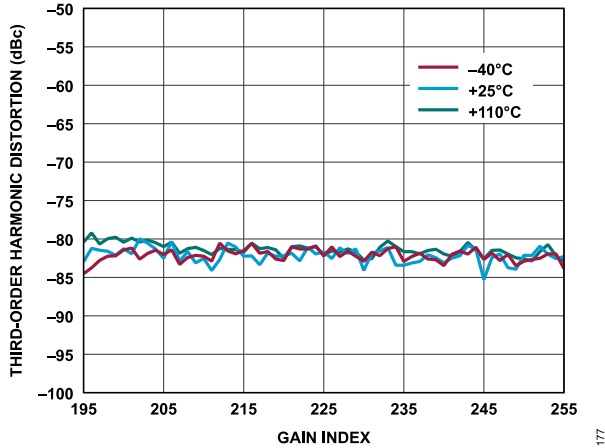


Figure 87. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

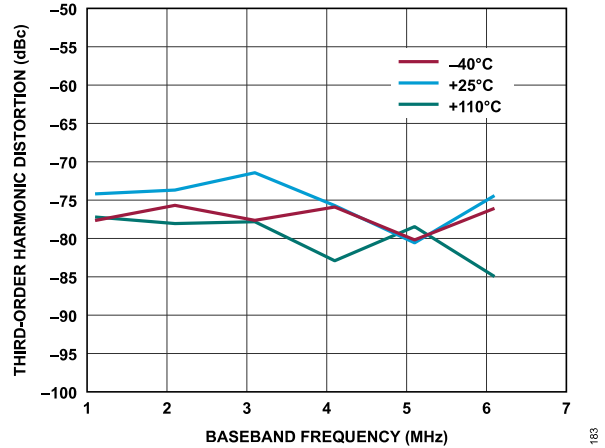


Figure 90. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = Low Power

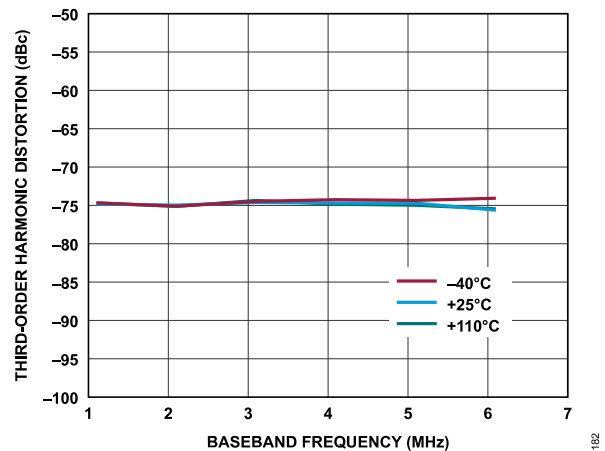


Figure 88. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

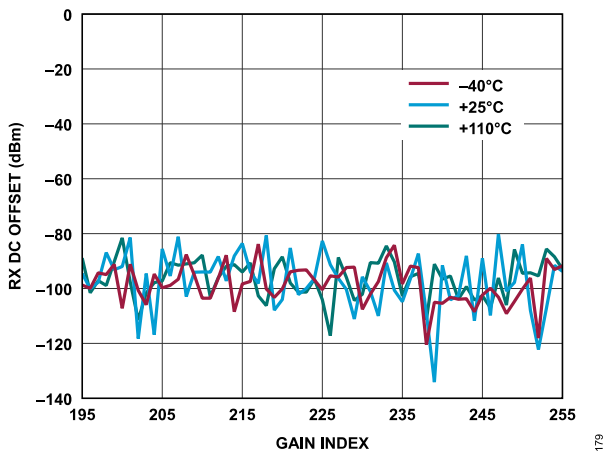


Figure 91. Receiver DC Offset vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

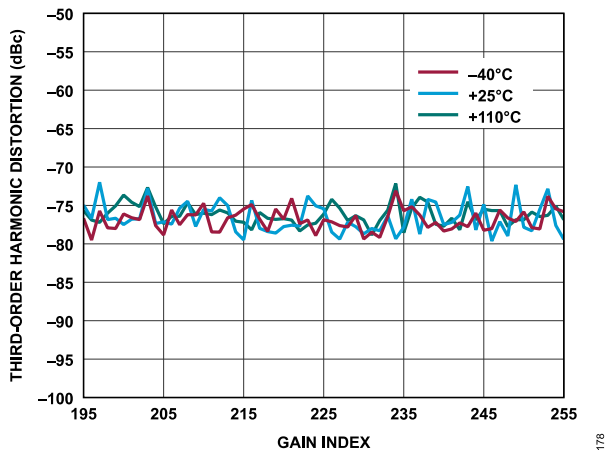


Figure 89. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = Low Power

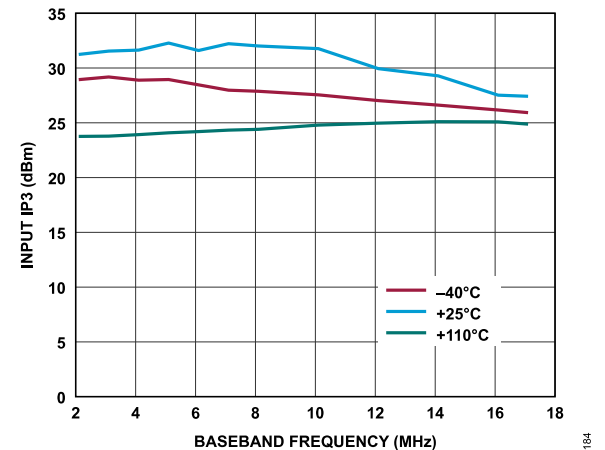


Figure 92. Receiver Input IP3 vs. Baseband Frequency, ADC = High Performance, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz, Gain Index = 255

TYPICAL PERFORMANCE CHARACTERISTICS

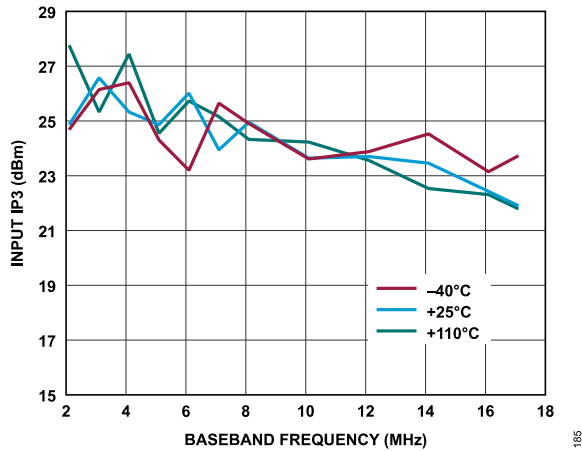


Figure 93. Receiver Input IP3 vs. Baseband Frequency, ADC = Low Power, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz, Gain Index = 255

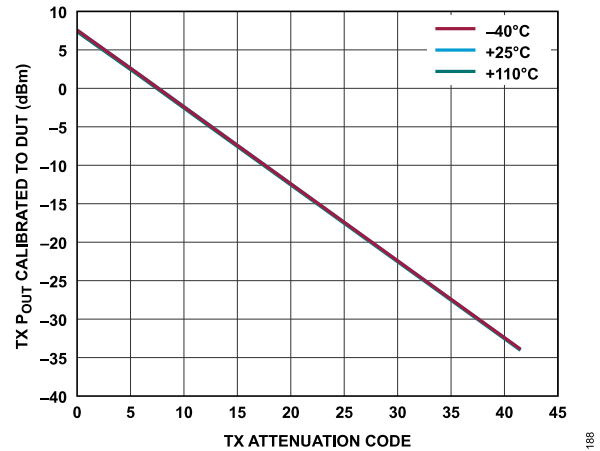


Figure 96. Transmitter Absolute Power vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

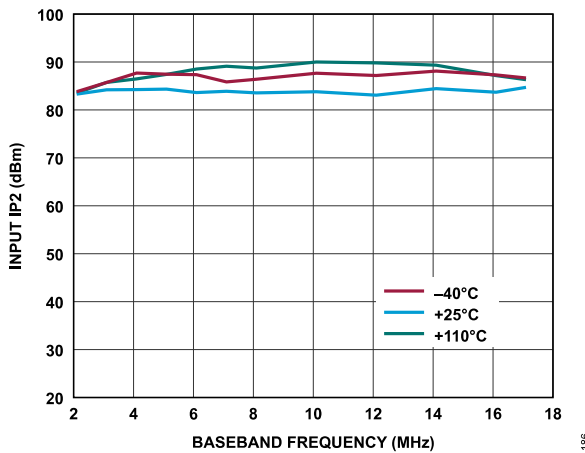


Figure 94. Receiver Input IP2 vs. Baseband Frequency, ADC = High Performance, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz, Gain Index = 255

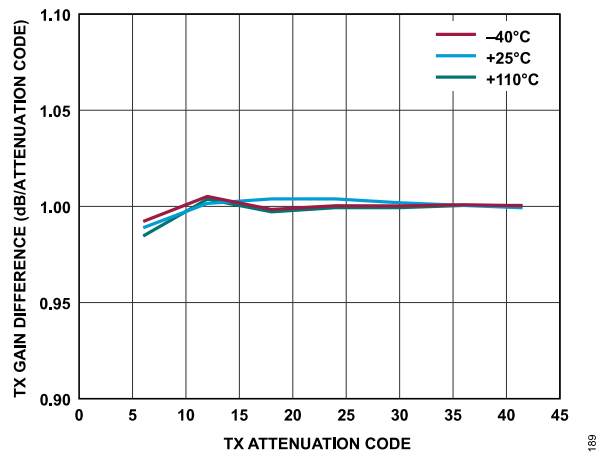


Figure 97. Transmitter Attenuation Delta (Error) vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

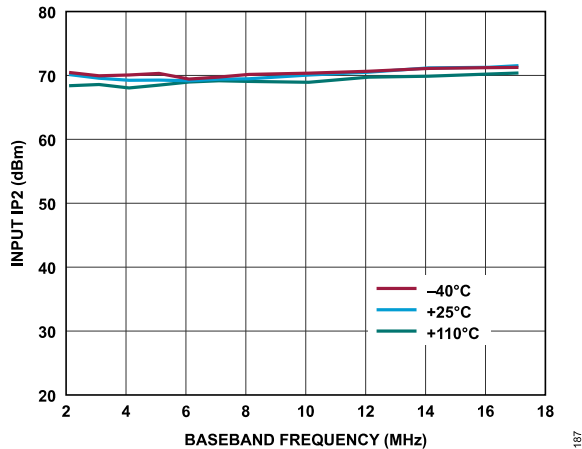


Figure 95. Receiver Input IP2 vs. Baseband Frequency, ADC = Low Power, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz, Gain Index = 255

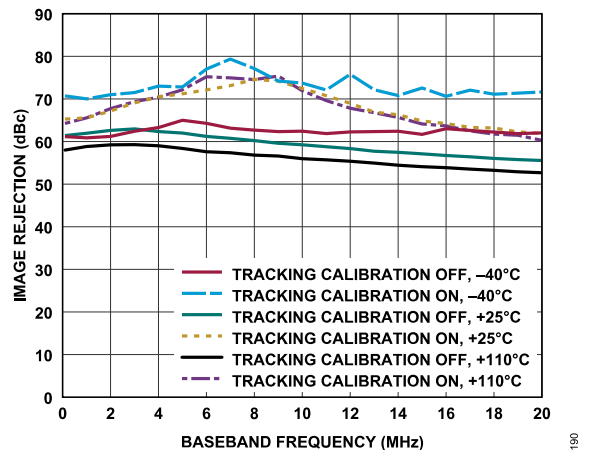


Figure 98. Transmitter Image Rejection vs. Baseband Frequency, Tracking Calibration On vs. Tracking Calibration Off, Transmitter Attenuation Code = 0

TYPICAL PERFORMANCE CHARACTERISTICS

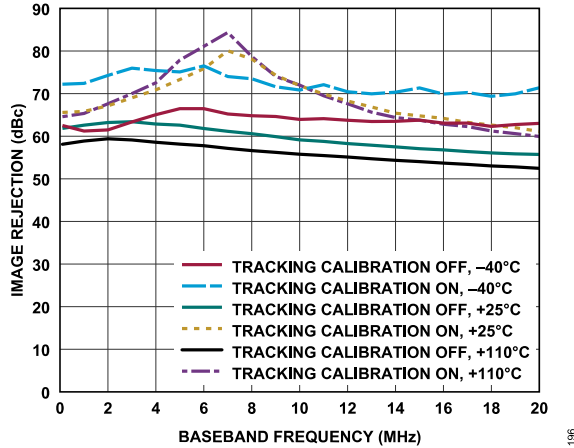


Figure 99. Transmitter Image Rejection vs. Baseband Frequency, Tracking Calibration On vs. Tracking Calibration Off, Transmitter Attenuation Code = 20

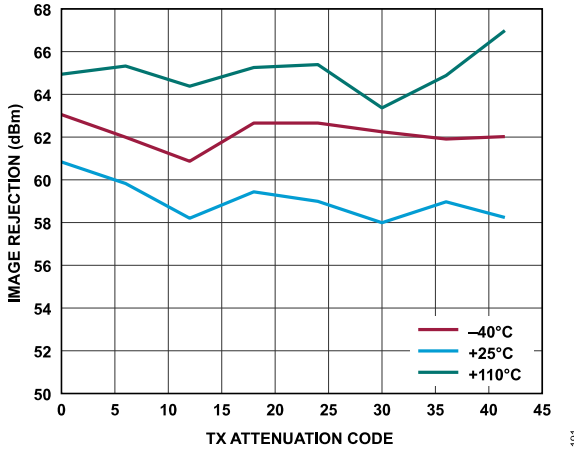


Figure 100. Transmitter Image Rejection vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS, Initialization Calibration Only

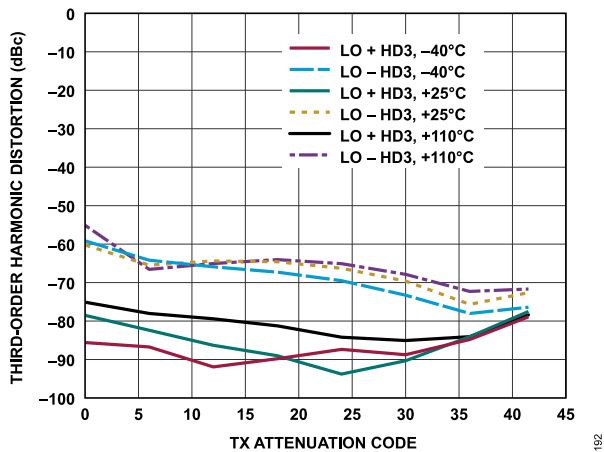


Figure 101. Transmitter Third-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

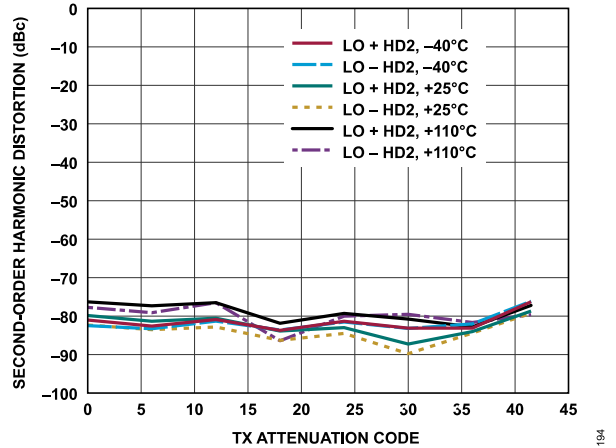


Figure 102. Transmitter Second-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

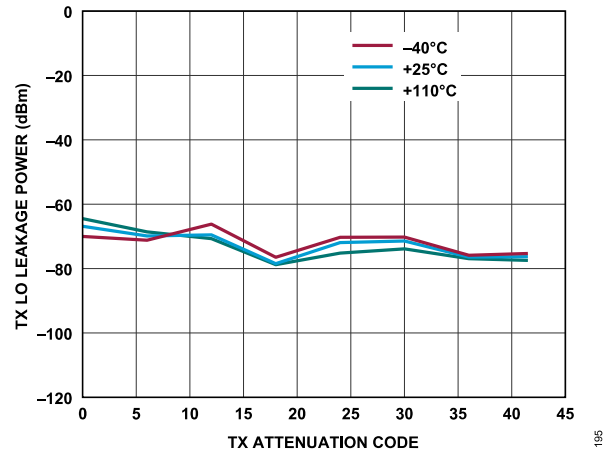


Figure 103. Transmitter LO Leakage Power vs. Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 6 dBFS, Initialization Calibration Only

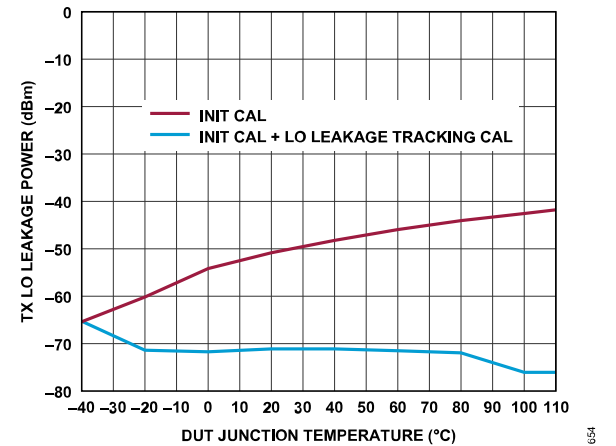


Figure 104. Transmitter LO Leakage Power vs. DUT Junction Temperature (Low to High), Baseband Frequency = 4 MHz, Backoff = 0.5 dBFS, Attenuation Code = 0

TYPICAL PERFORMANCE CHARACTERISTICS

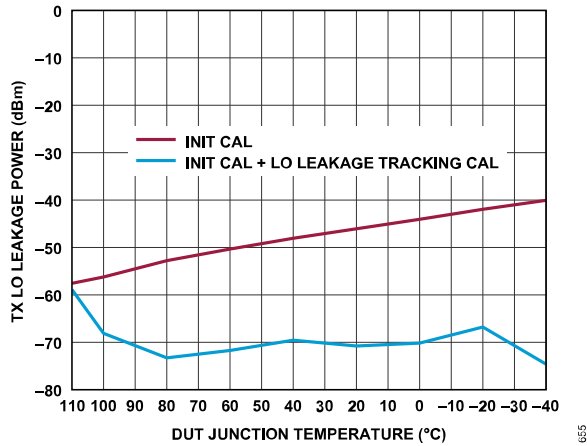


Figure 105. Transmitter LO Leakage Power vs. DUT Junction Temperature (High to Low), Baseband Frequency = 4 MHz, Backoff = 0.5 dBFS, Attenuation Code = 0

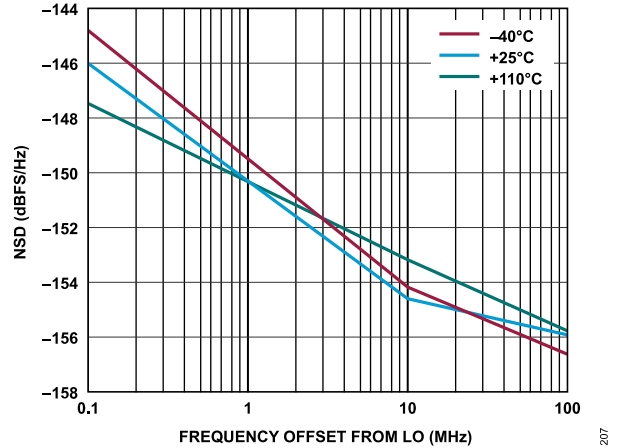


Figure 108. Transmitter NSD vs. Frequency Offset from LO, Baseband Frequency = 5.6 MHz, Transmitter Channel = Ch1

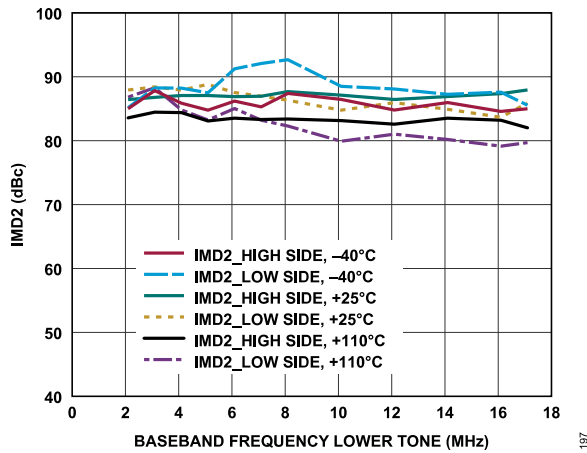


Figure 106. Transmitter IMD2 vs. Baseband Frequency, Transmitter Attenuation Code = 0, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz

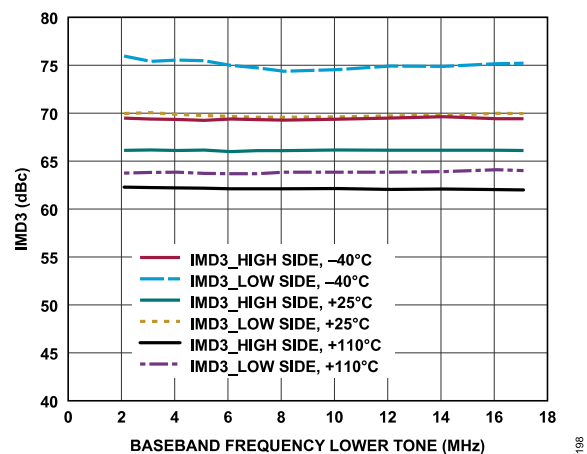


Figure 107. Transmitter IMD3 vs. Baseband Frequency, Transmitter Attenuation Code = 0, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

2400 MHz LO

The temperature settings refer to the die temperature. All LO frequencies set to 2400 MHz, unless otherwise noted.

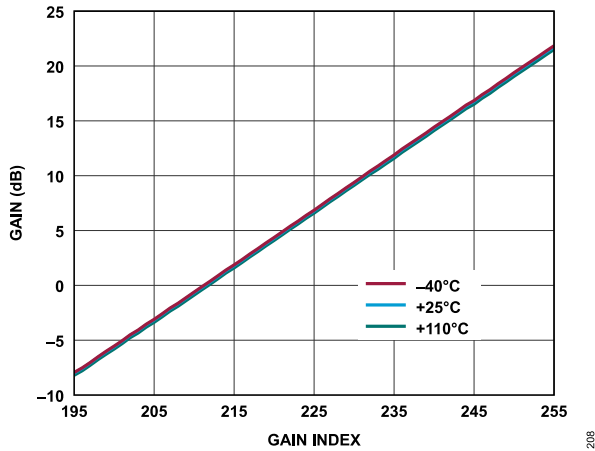


Figure 109. Receiver Absolute Gain (Complex) vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance, $P_{OUT} = -9.6$ dBFS

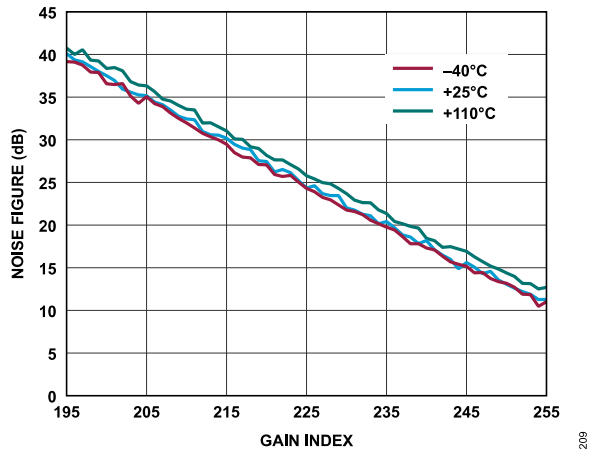


Figure 110. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

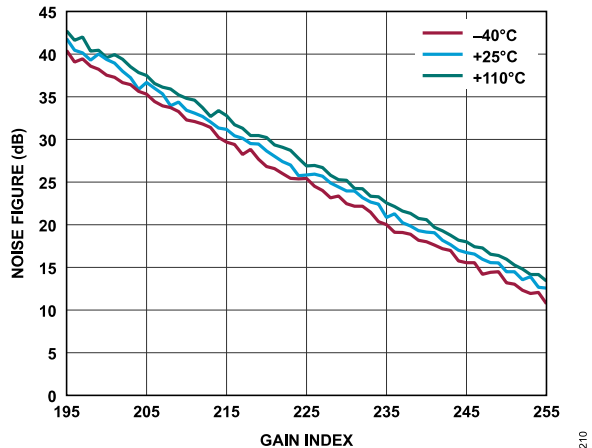


Figure 111. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = Low Power

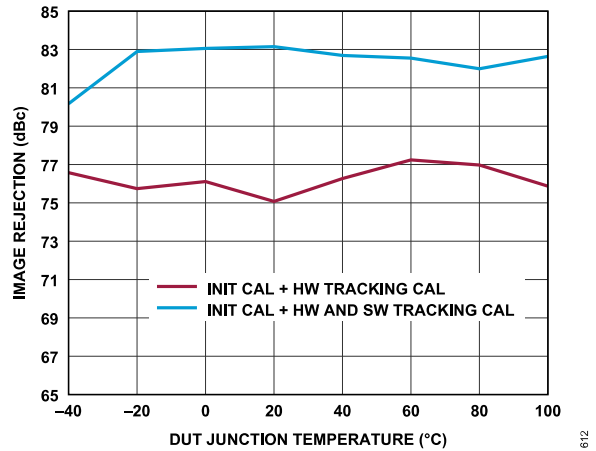


Figure 112. Receiver Image Rejection vs. DUT Junction Temperature (Low to High), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = High Performance, $P_{OUT} = -11.1$ dBFS

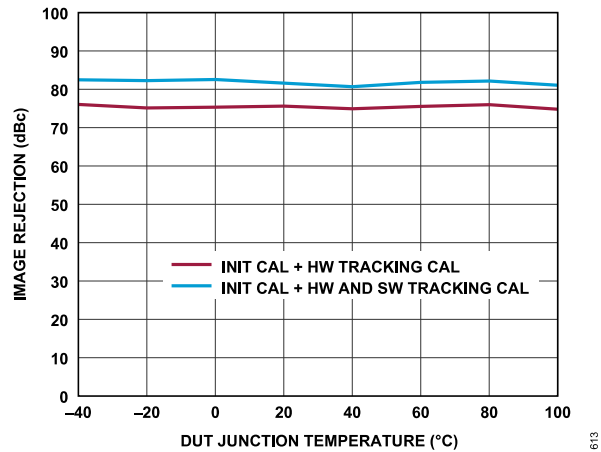


Figure 113. Receiver Image Rejection vs. DUT Junction Temperature (Low to High), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = Low Power, $P_{OUT} = -11.1$ dBFS

TYPICAL PERFORMANCE CHARACTERISTICS

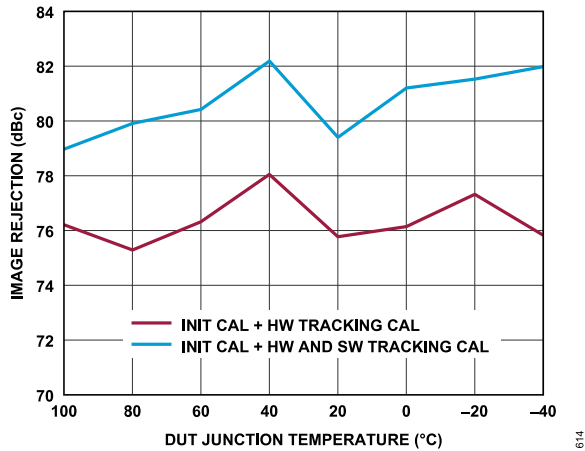


Figure 114. Receiver Image Rejection vs. DUT Junction Temperature (High to Low), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = High Performance, $P_{OUT} = -11.1$ dBFS

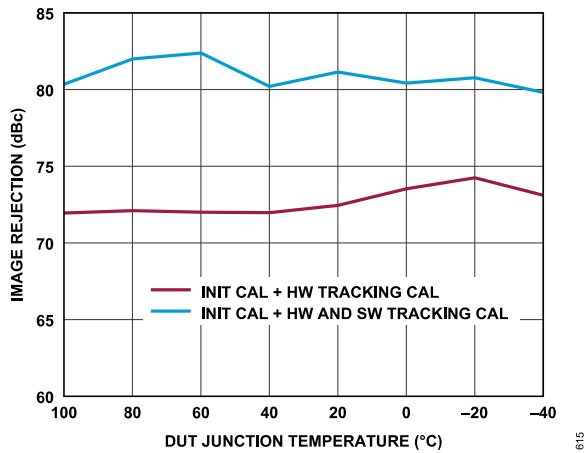


Figure 115. Receiver Image Rejection vs. DUT Junction Temperature (High to Low), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = Low Power, $P_{OUT} = -11.1$ dBFS

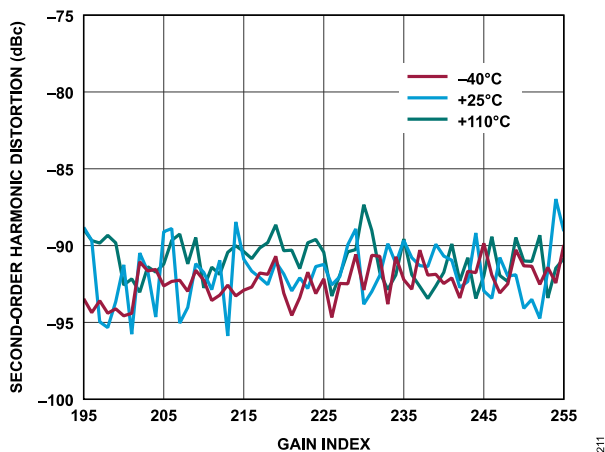


Figure 116. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

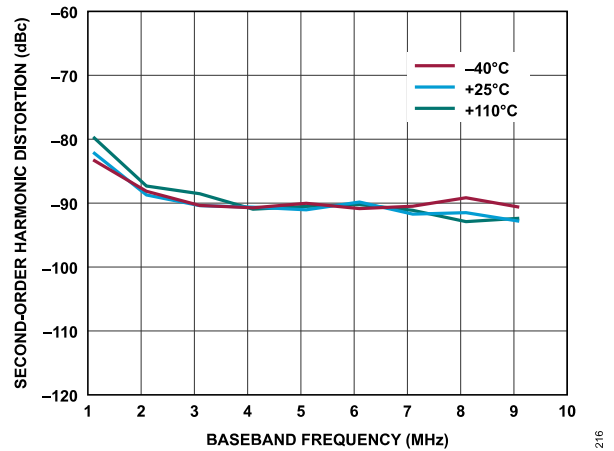


Figure 117. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

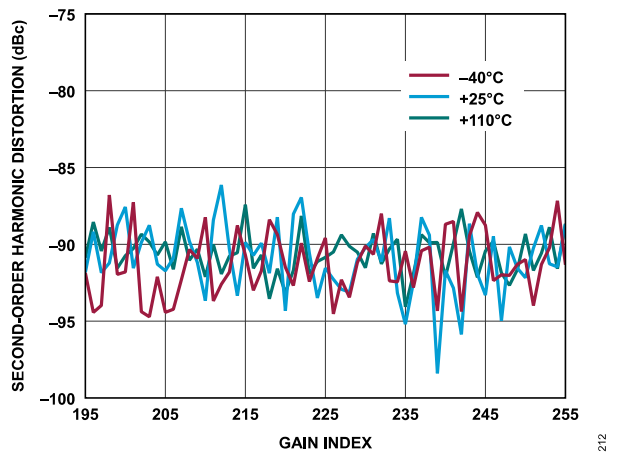


Figure 118. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = Low Power

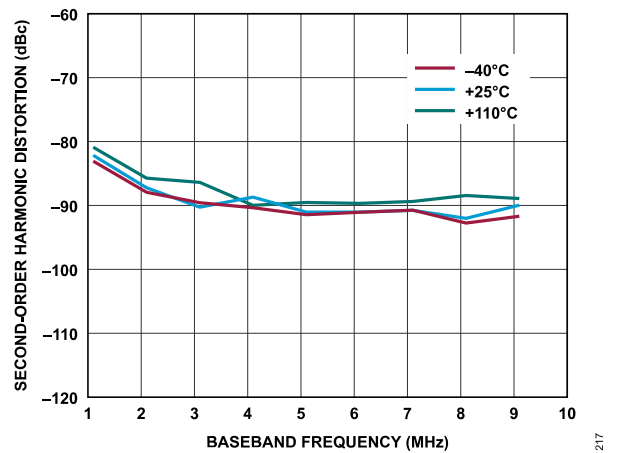


Figure 119. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = Low Power

TYPICAL PERFORMANCE CHARACTERISTICS

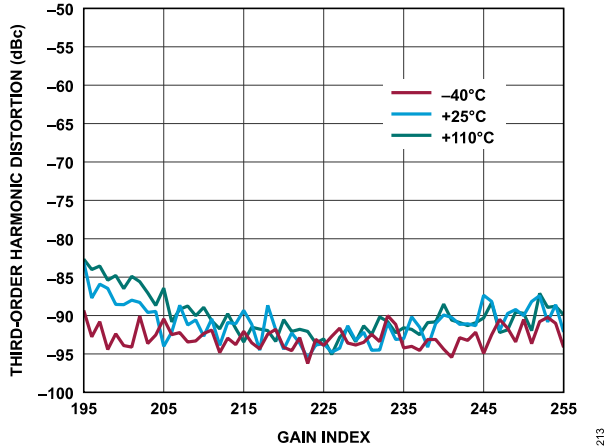


Figure 120. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

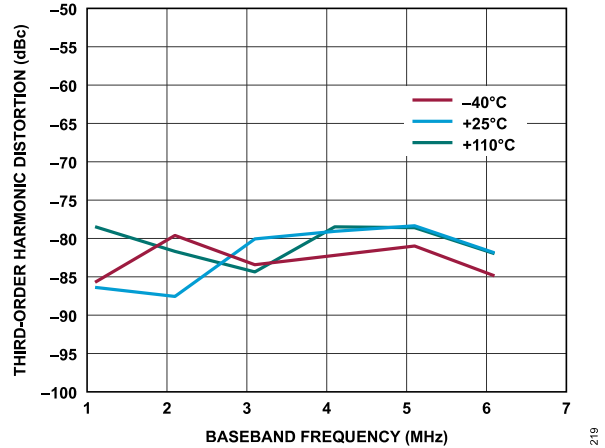


Figure 123. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = Low Power

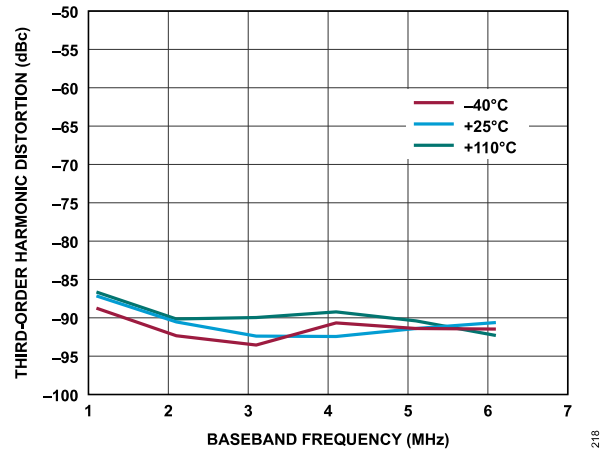


Figure 121. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

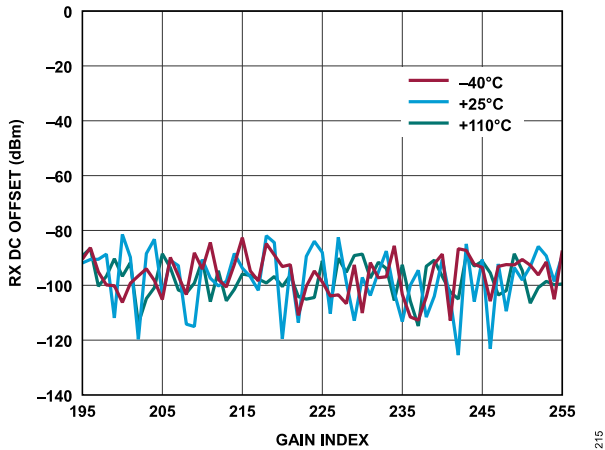


Figure 124. Receiver DC Offset vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

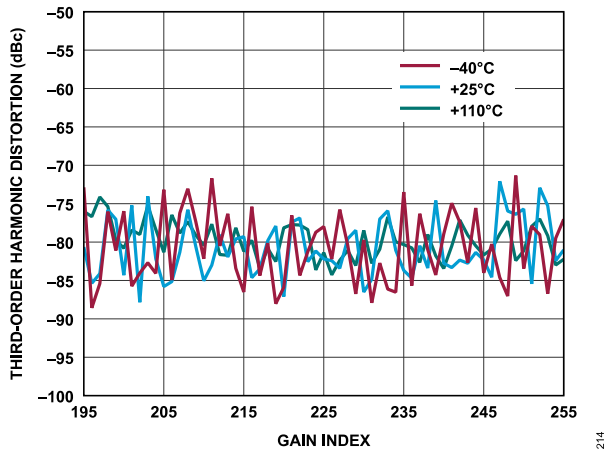


Figure 122. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = Low Power

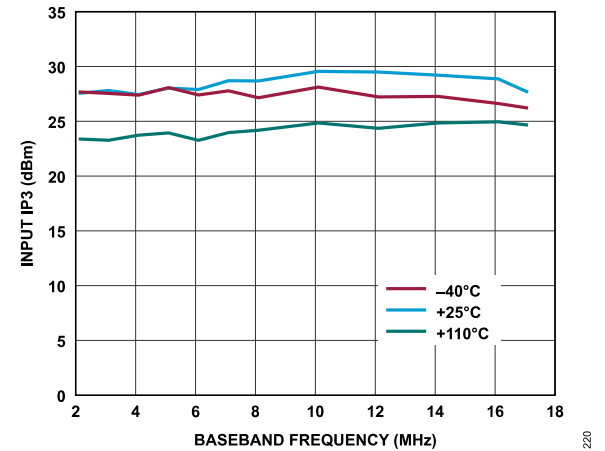


Figure 125. Receiver Input IP3 vs. Baseband Frequency, ADC = High Performance, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz, Gain Index = 255

TYPICAL PERFORMANCE CHARACTERISTICS

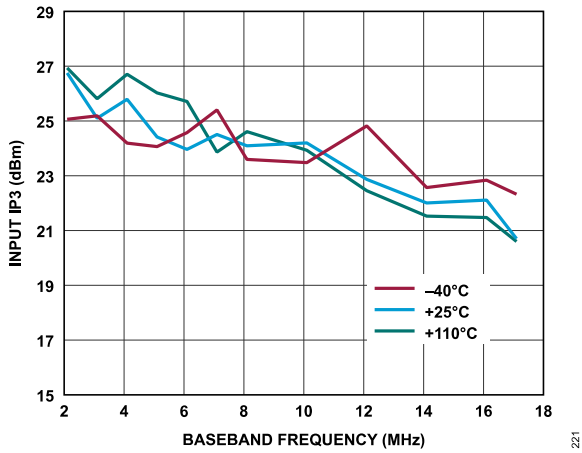


Figure 126. Receiver Input IP3 vs. Baseband Frequency, ADC = Low Power, f1 = Baseband Frequency, f2 = Baseband Frequency + 1 MHz, Gain Index = 255

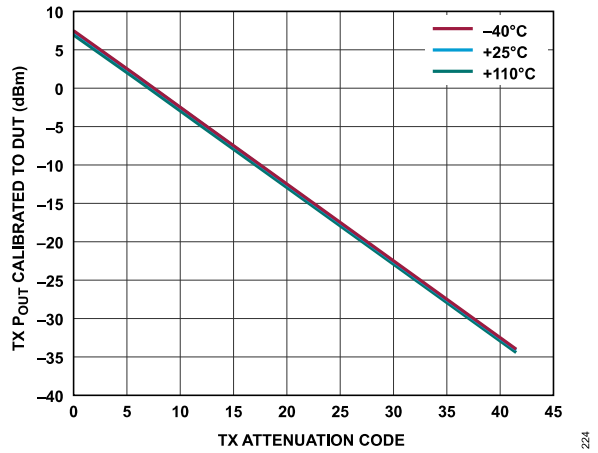


Figure 129. Transmitter Absolute Power vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

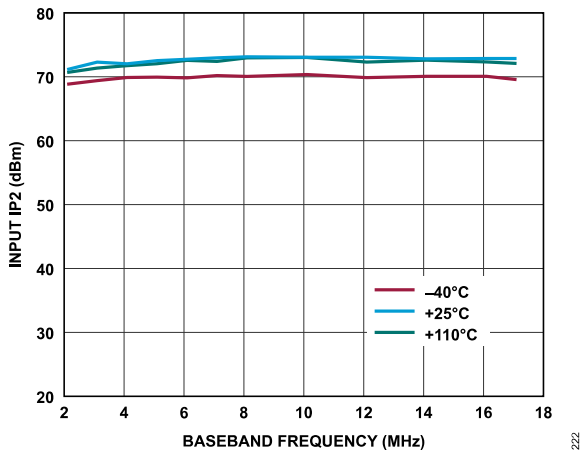


Figure 127. Receiver Input IP2 vs. Baseband Frequency, ADC = High Performance, f1 = Baseband Frequency, f2 = Baseband Frequency + 1 MHz, Gain Index = 255

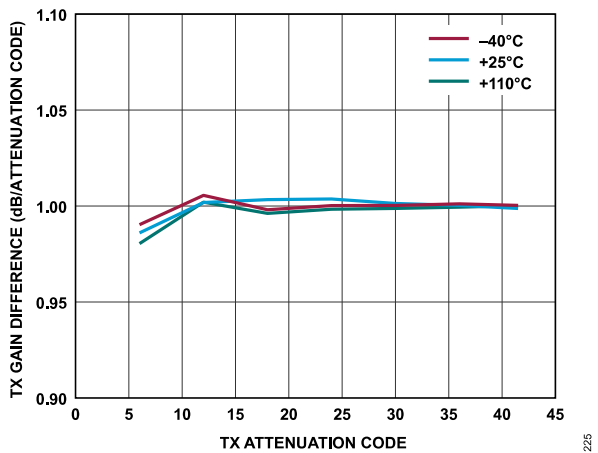


Figure 130. Transmitter Attenuation Delta (Error) vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

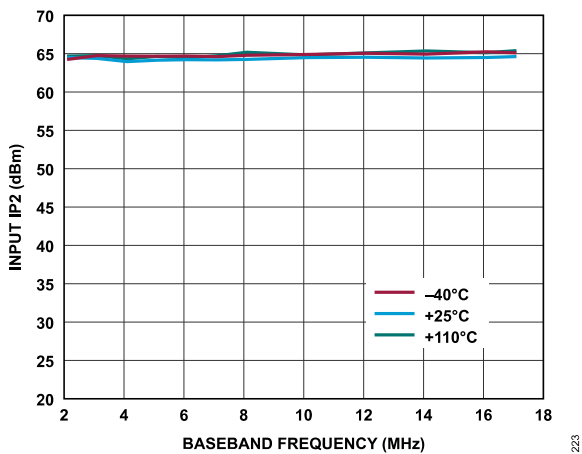


Figure 128. Receiver Input IP2 vs. Baseband Frequency, ADC = Low Power, f1 = Baseband Frequency, f2 = Baseband Frequency + 1 MHz, Gain Index = 255

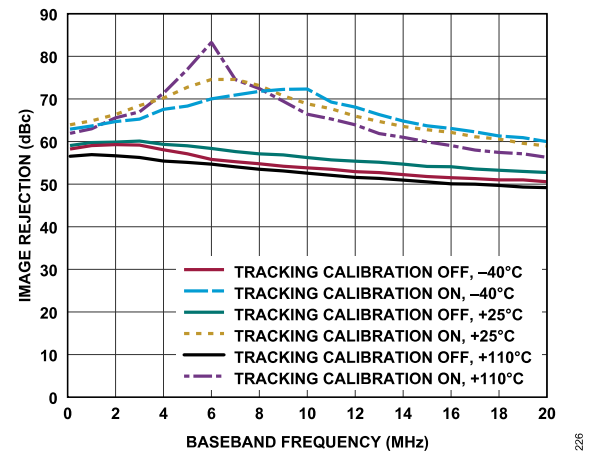


Figure 131. Transmitter Image Rejection vs. Baseband Frequency, Tracking Calibration On vs. Tracking Calibration Off, Transmitter Attenuation Code = 0

TYPICAL PERFORMANCE CHARACTERISTICS

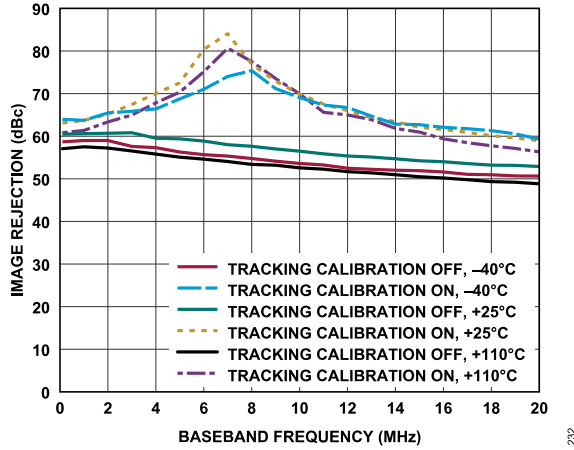


Figure 132. Transmitter Image Rejection vs. Baseband Frequency, Tracking Calibration On vs. Tracking Calibration Off, Transmitter Attenuation Code = 20

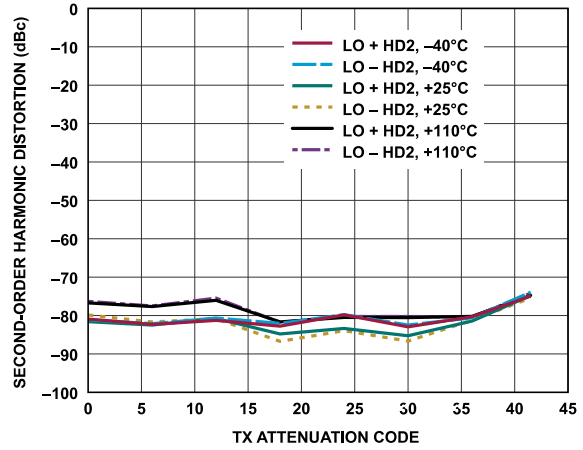


Figure 135. Transmitter Second-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

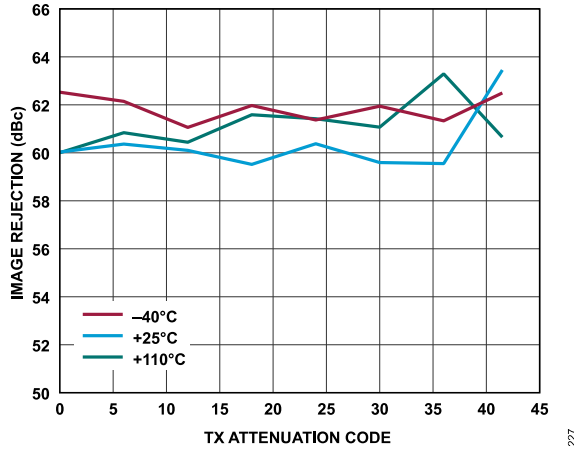


Figure 133. Transmitter Image Rejection vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS, Initialization Calibration Only

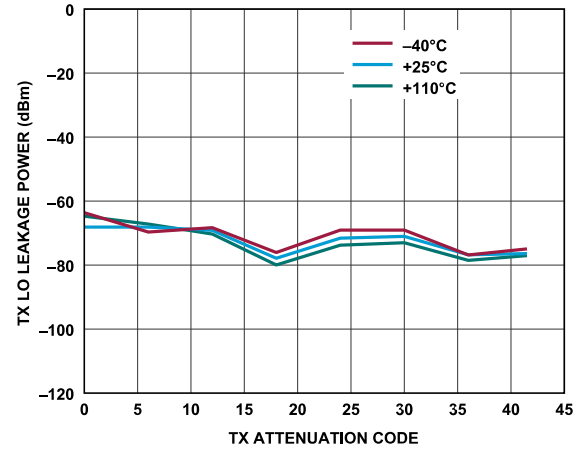


Figure 136. Transmitter LO Leakage Power vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 6 dBFS, Initialization Calibration Only

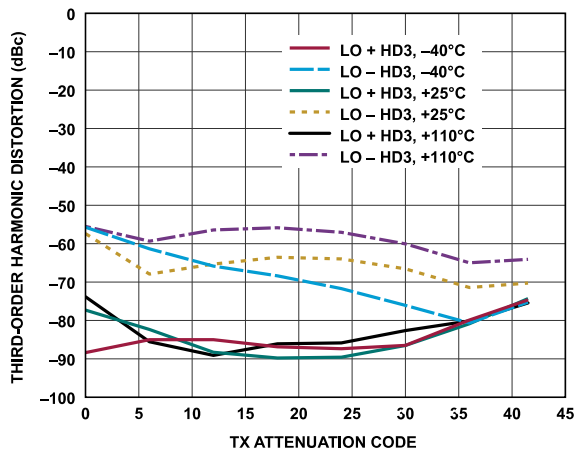


Figure 134. Transmitter Third-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

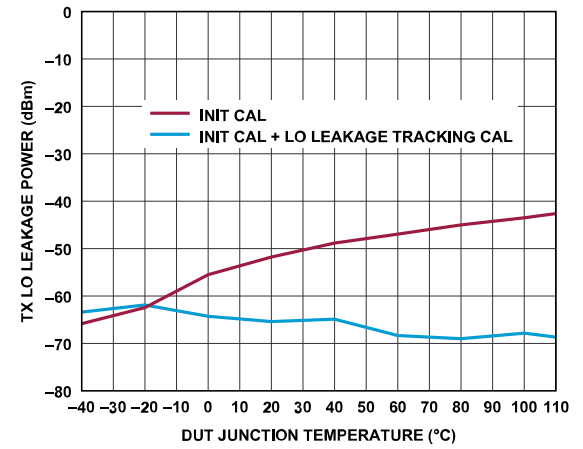


Figure 137. Transmitter LO Leakage Power vs. DUT Junction Temperature (Low to High), Baseband Frequency = 4 MHz, Backoff = 0.5 dBFS, Attenuation Code = 0

TYPICAL PERFORMANCE CHARACTERISTICS

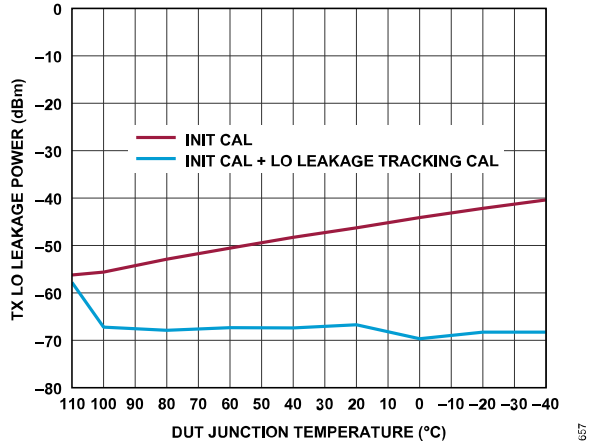


Figure 138. Transmitter LO Leakage Power vs. DUT Junction Temperature (High to Low), Baseband Frequency = 4 MHz, Backoff = 0.5 dBFS, Attenuation Code = 0

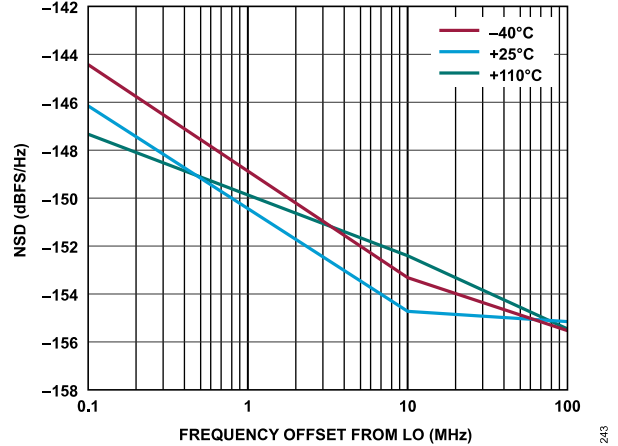


Figure 141. Transmitter NSD vs. Frequency Offset from LO, Baseband Frequency = 5.6 MHz, Transmitter Channel = Ch1

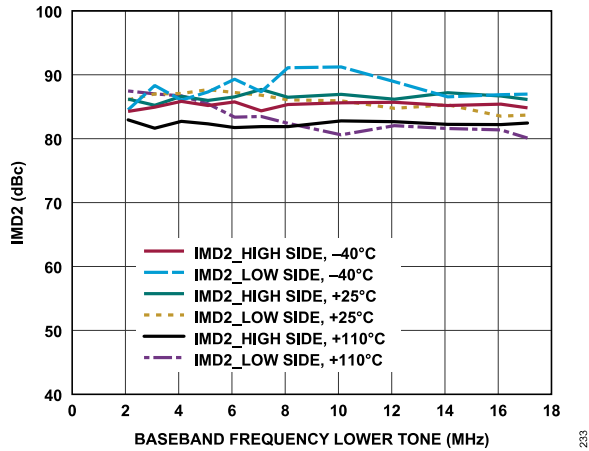


Figure 139. Transmitter IMD2 vs. Baseband Frequency, Transmitter Attenuation Code = 0, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz

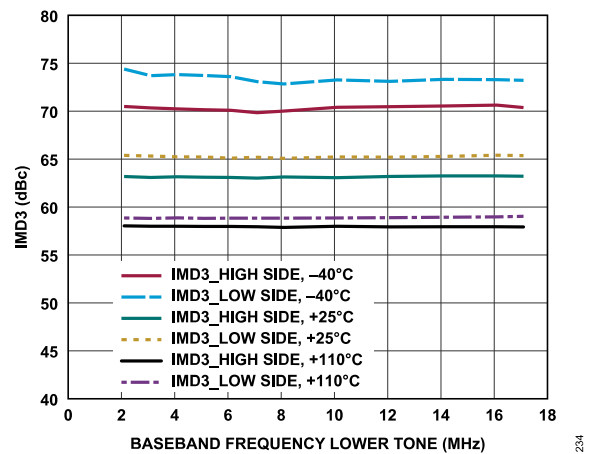


Figure 140. Transmitter IMD3 vs Baseband Frequency, Transmitter Attenuation Code = 0, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

3500 MHz LO

The temperature settings refer to the die temperature. All LO frequencies set to 3500 MHz, unless otherwise noted.

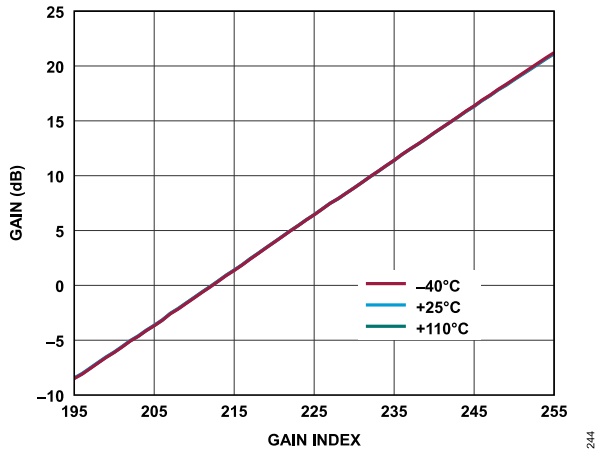


Figure 142. Receiver Absolute Gain (Complex) vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance, $P_{OUT} = -9.6$ dBFS

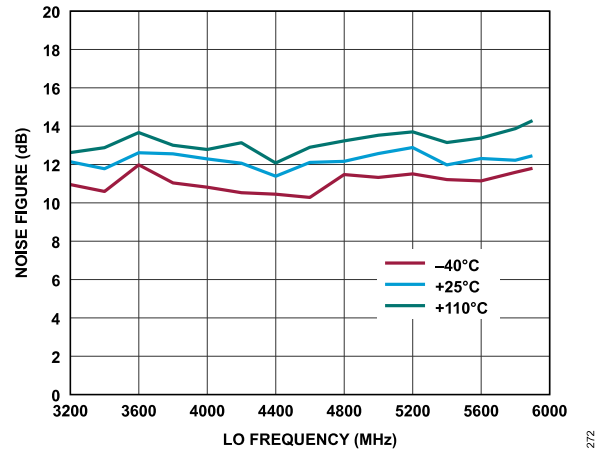


Figure 145. Receiver Noise Figure vs. LO Frequency, Baseband Frequency = 5.6 MHz, ADC = High Performance

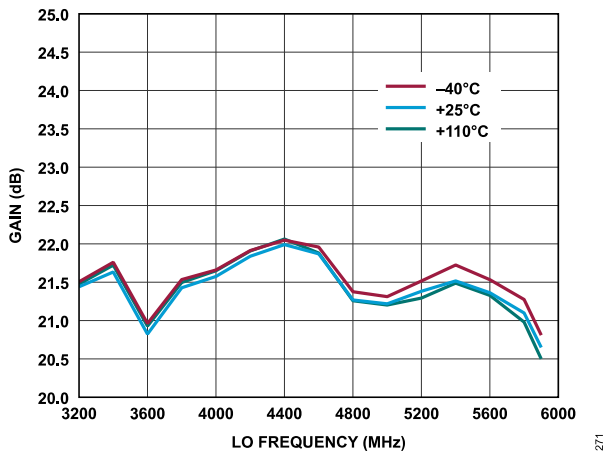


Figure 143. Receiver Absolute Gain (Complex) vs. LO Frequency, Baseband Frequency = 5.6 MHz, ADC = High Performance, $P_{OUT} = -9.6$ dBFS

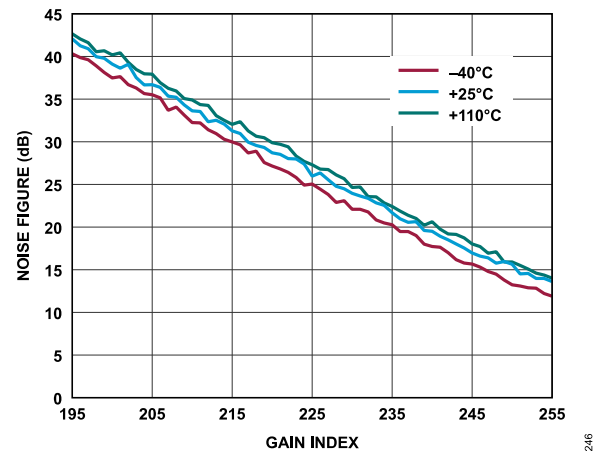


Figure 146. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = Low Power

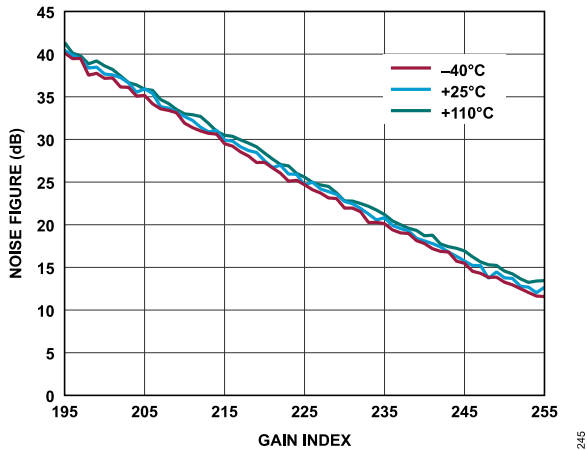


Figure 144. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

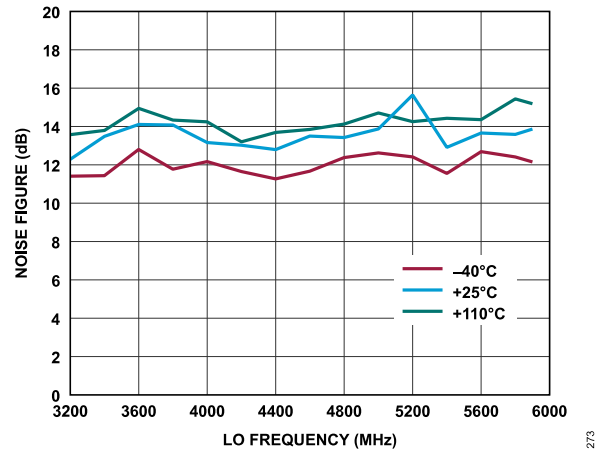


Figure 147. Receiver Noise Figure vs. LO Frequency, Baseband Frequency = 5.6 MHz, ADC = Low Power

TYPICAL PERFORMANCE CHARACTERISTICS

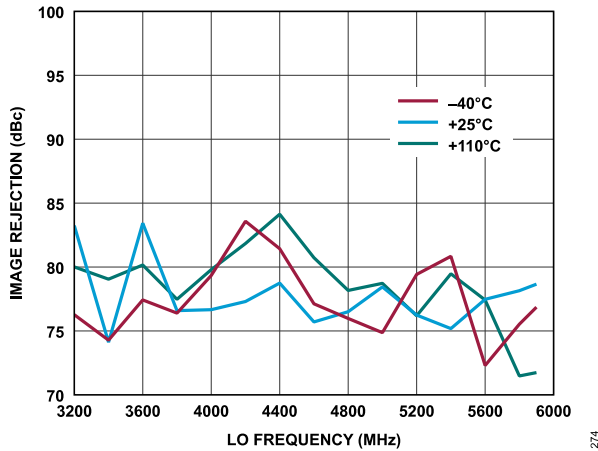


Figure 148. Receiver Image Rejection vs. LO Frequency, Baseband Frequency = 5.6 MHz, ADC = High Performance, Initialization Calibration and Hardware Tracking Calibration Only

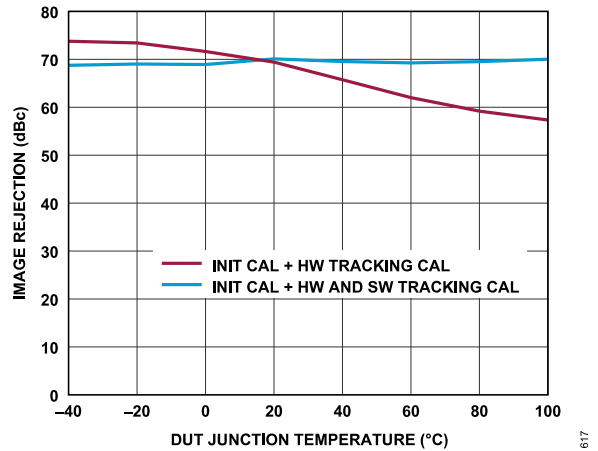


Figure 151. Receiver Image Rejection vs. DUT Junction Temperature (Low to High), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = Low Power, $P_{OUT} = -11.1$ dBFS

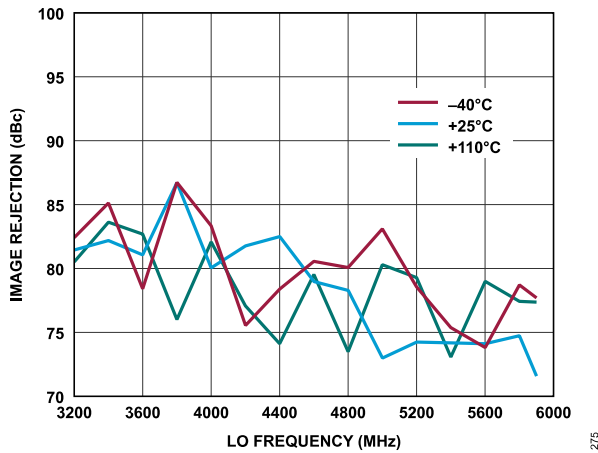


Figure 149. Receiver Image Rejection vs. LO Frequency, Baseband Frequency = 5.6 MHz, ADC = Low Power, Initialization Calibration and Hardware Tracking Calibration Only

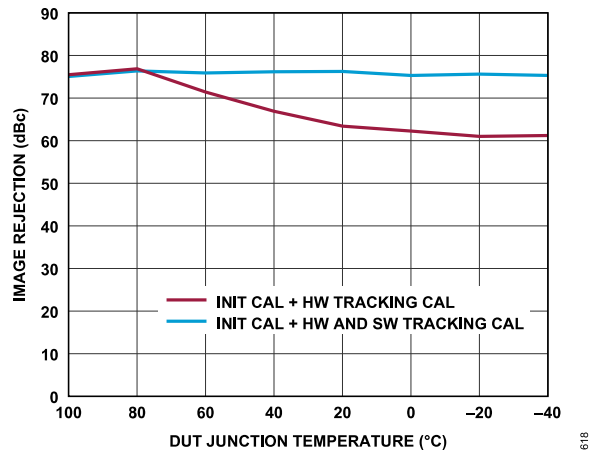


Figure 152. Receiver Image Rejection vs. DUT Junction Temperature (High to Low), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = High Performance, $P_{OUT} = -11.1$ dBFS

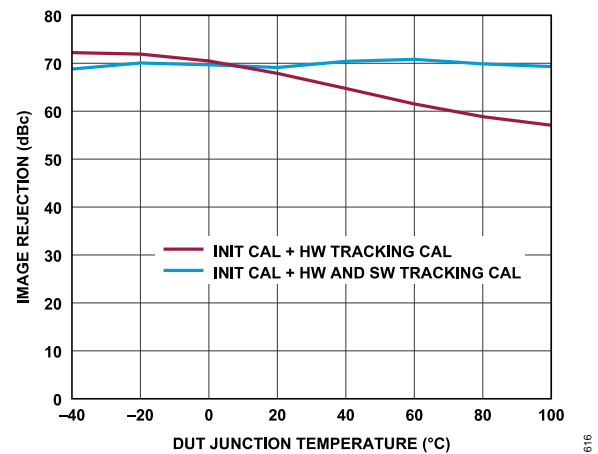


Figure 150. Receiver Image Rejection vs. DUT Junction Temperature (Low to High), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = High Performance, $P_{OUT} = -11.1$ dBFS

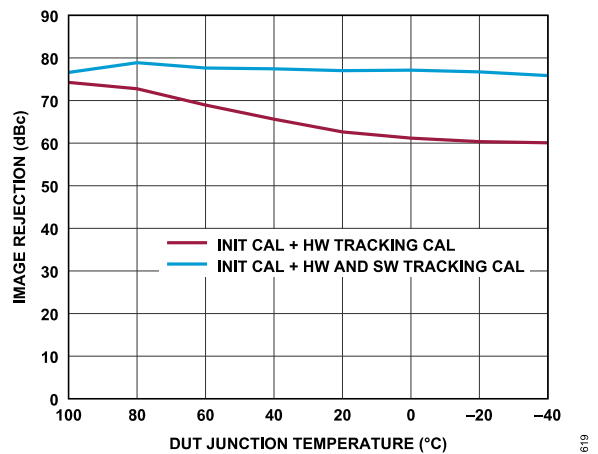


Figure 153. Receiver Image Rejection vs. DUT Junction Temperature (High to Low), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = Low Power, $P_{OUT} = -11.1$ dBFS

TYPICAL PERFORMANCE CHARACTERISTICS

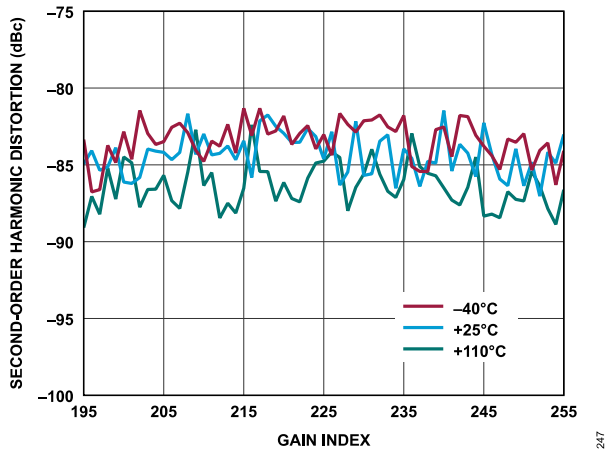


Figure 154. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

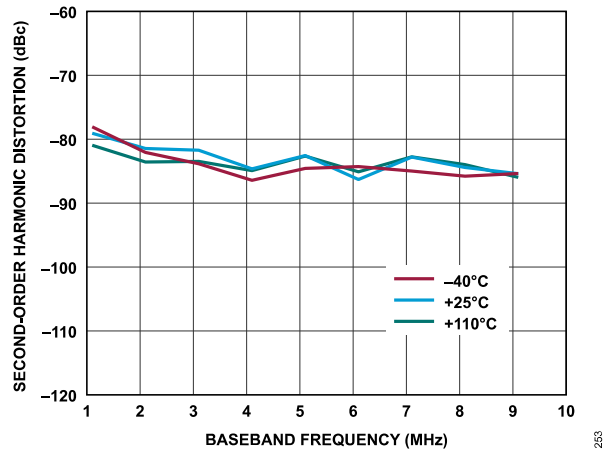


Figure 157. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = Low Power

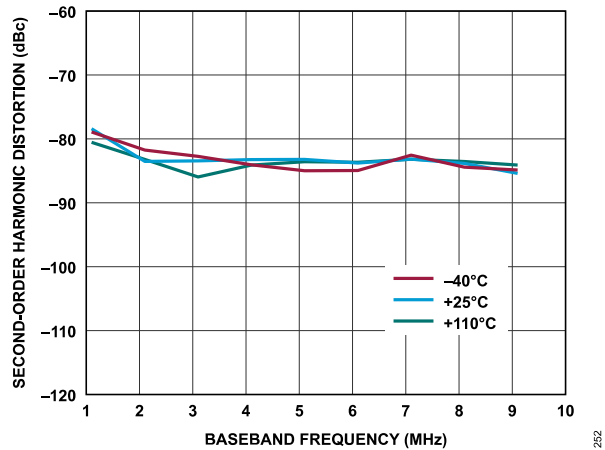


Figure 155. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

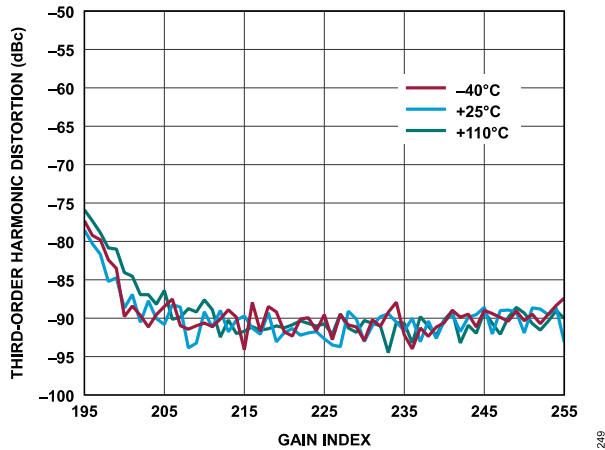


Figure 158. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

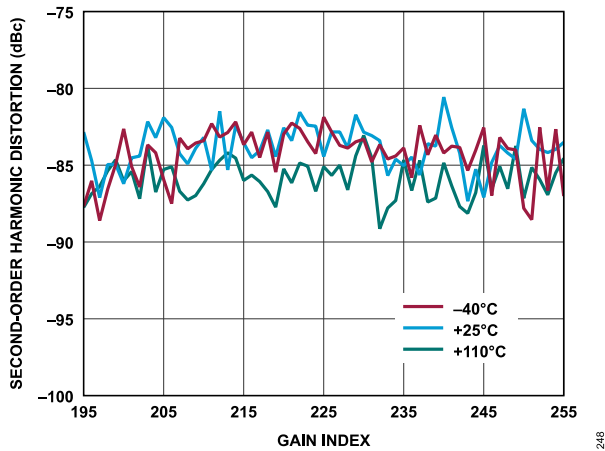


Figure 156. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = Low Power

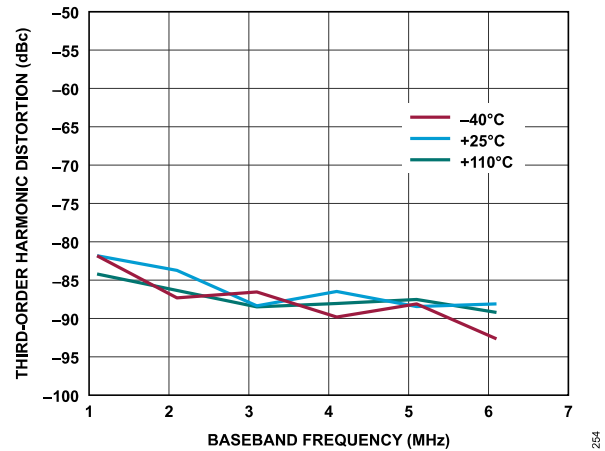


Figure 159. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

TYPICAL PERFORMANCE CHARACTERISTICS

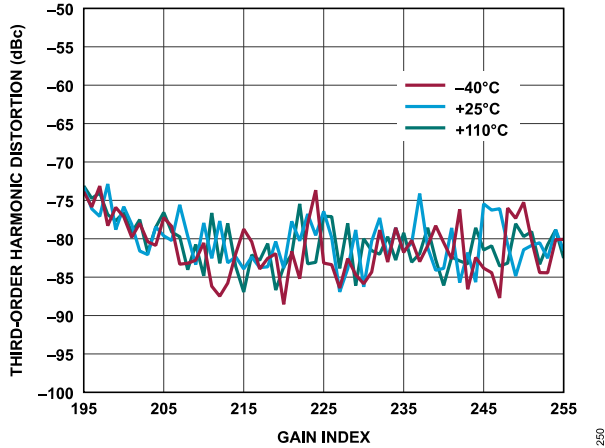


Figure 160. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = Low Power

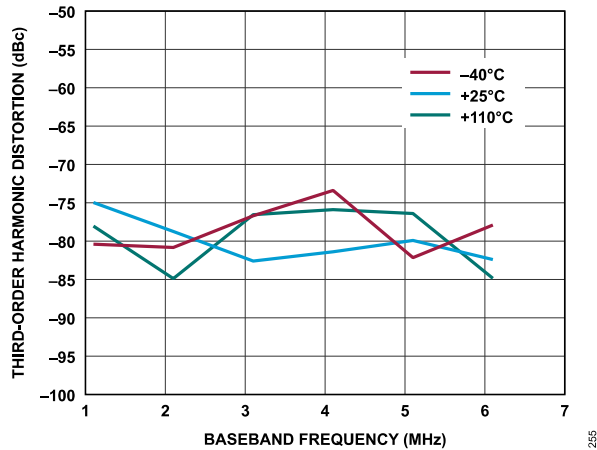


Figure 161. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain index = 255, ADC = Low Power

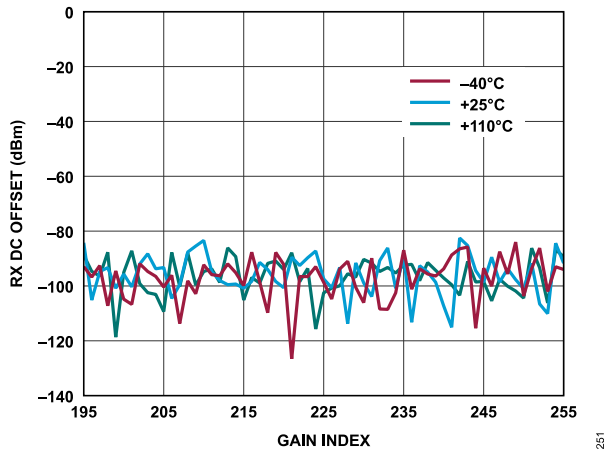


Figure 162. Receiver DC Offset vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

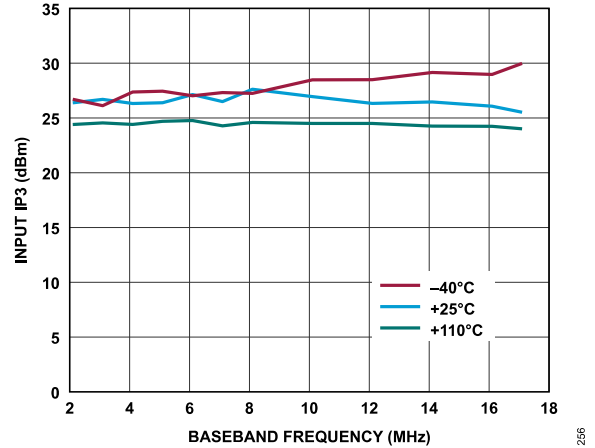


Figure 163. Receiver Input IP3 vs. Baseband Frequency, ADC = High Performance, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz, Gain Index = 255

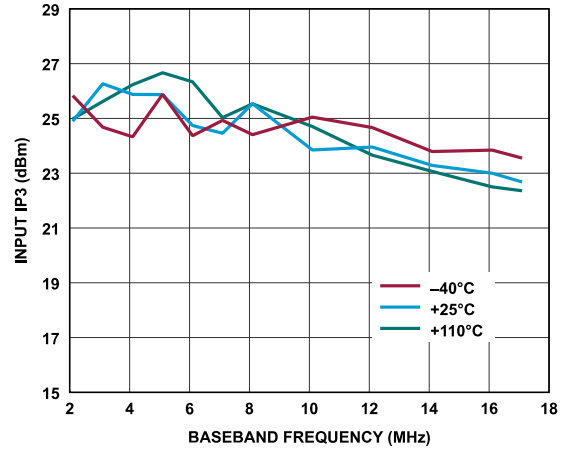


Figure 164. Receiver Input IP3 vs. Baseband Frequency, ADC = Low Power, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz, Gain Index = 255

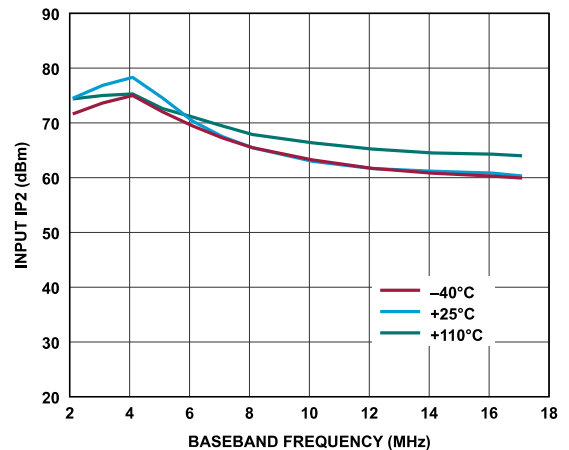


Figure 165. Receiver Input IP2 vs. Baseband Frequency, ADC = High Performance, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz, Gain Index = 255

TYPICAL PERFORMANCE CHARACTERISTICS

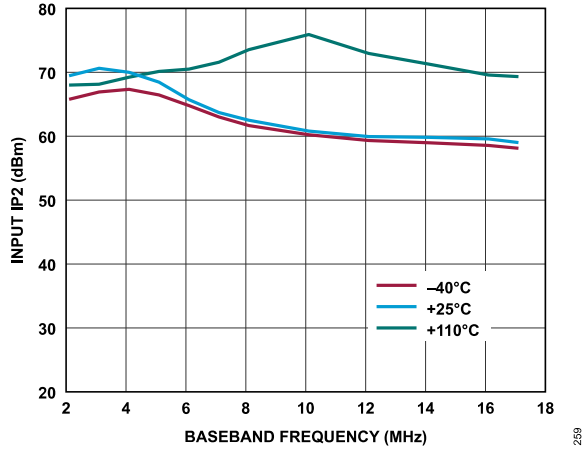


Figure 166. Receiver Input IP2 vs. Baseband Frequency, ADC = Low Power, f1 = Baseband Frequency, f2 = Baseband Frequency + 1 MHz, Gain Index = 255

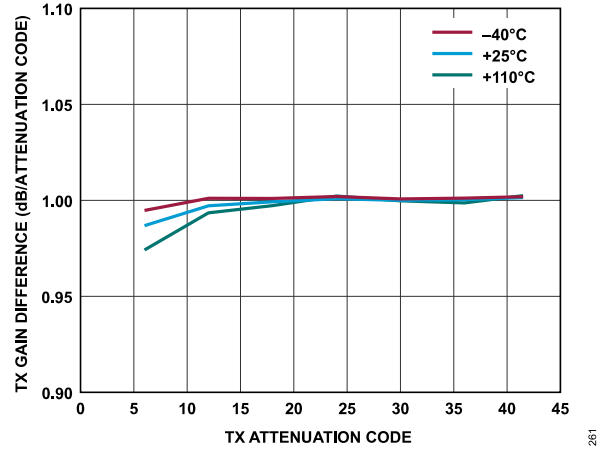


Figure 169. Transmitter Attenuation Delta (Error) vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

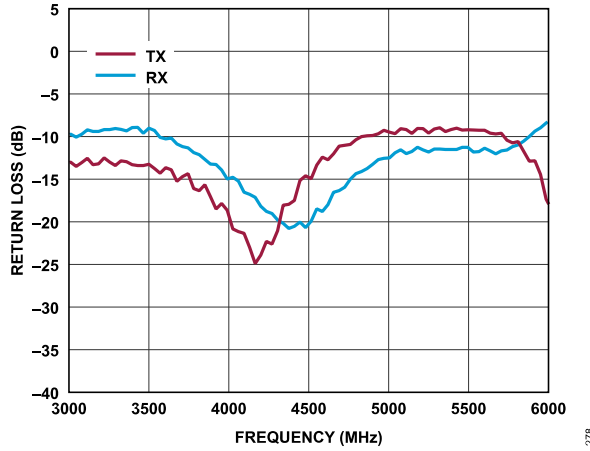


Figure 167. Receiver and Transmitter Return Loss vs. Frequency (For LO = 3 GHz to 6 GHz)

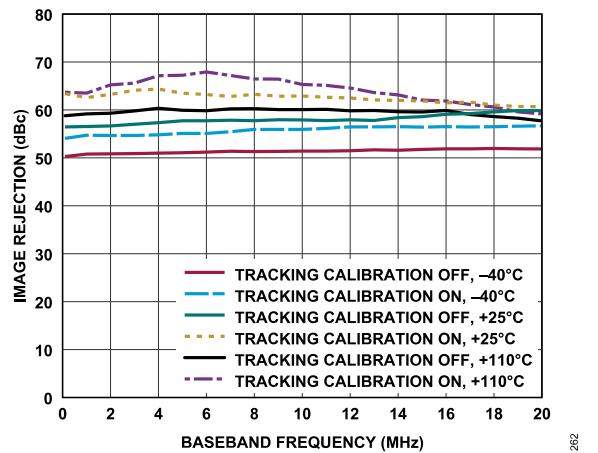


Figure 170. Transmitter Image Rejection vs. Baseband Frequency, Tracking Calibration On vs. Tracking Calibration Off, Transmitter Attenuation Code = 0

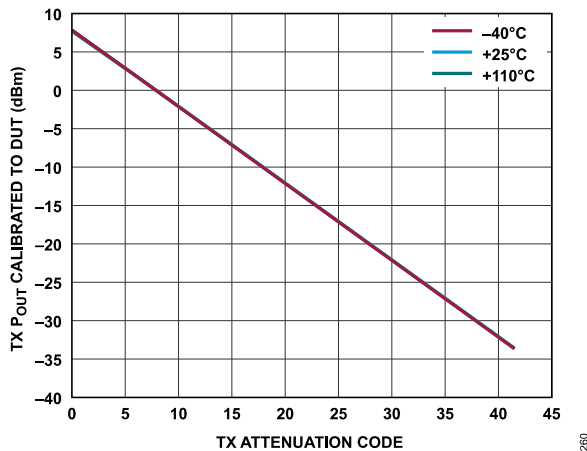


Figure 168. Transmitter Absolute Power vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

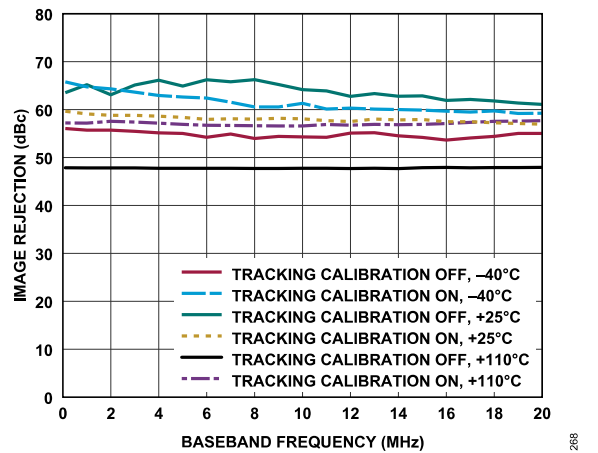


Figure 171. Transmitter Image Rejection vs. Baseband Frequency, Tracking Calibration On vs. Tracking Calibration Off, Transmitter Attenuation Code = 20

TYPICAL PERFORMANCE CHARACTERISTICS

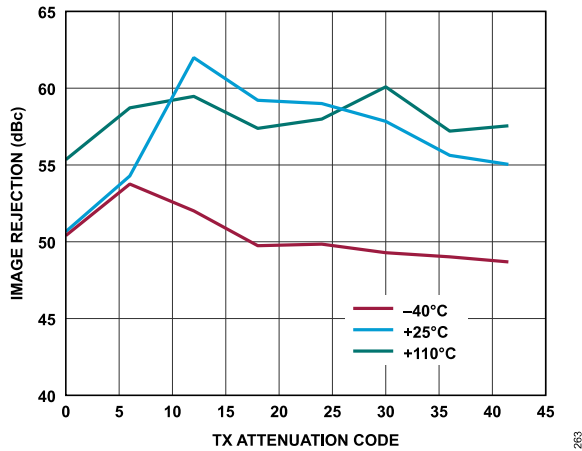


Figure 172. Transmitter Image Rejection vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS, Initialization Calibration Only

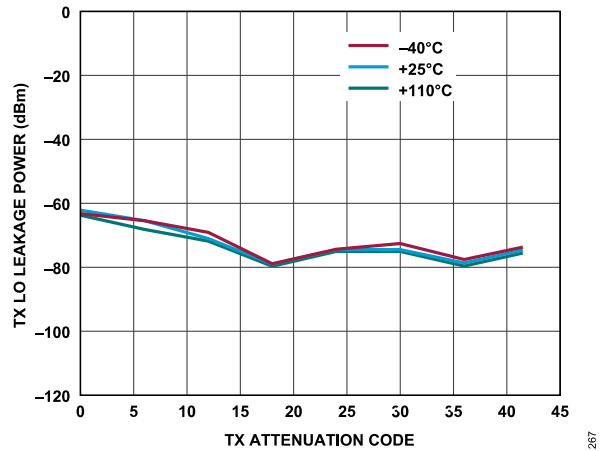


Figure 175. Transmitter LO Leakage Power vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 6 dBFS, Initialization Calibration Only

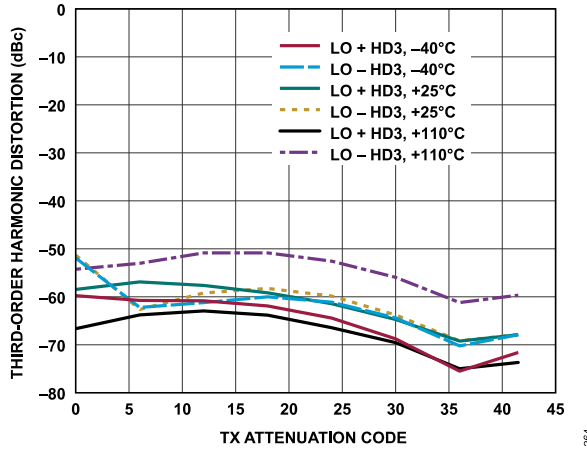


Figure 173. Transmitter Third-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

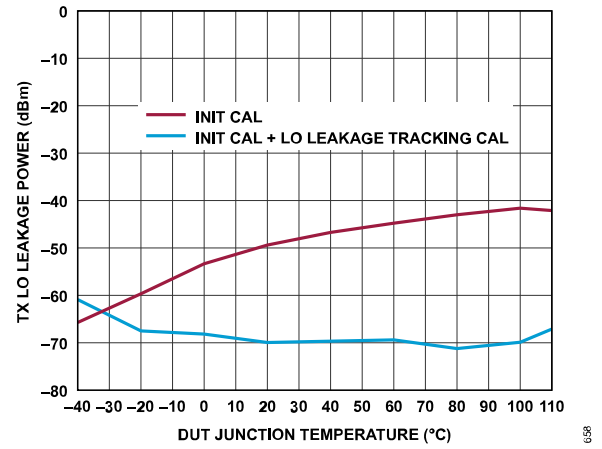


Figure 176. Transmitter LO Leakage Power vs. DUT Junction Temperature (Low to High), Baseband Frequency = 4 MHz, Backoff = 0.5 dBFS, Attenuation Code = 0

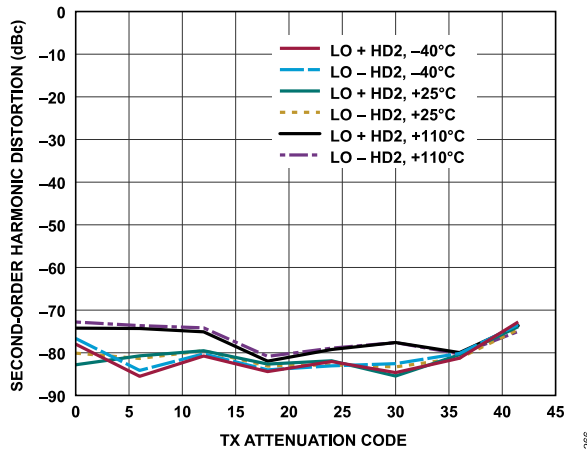


Figure 174. Transmitter Second-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

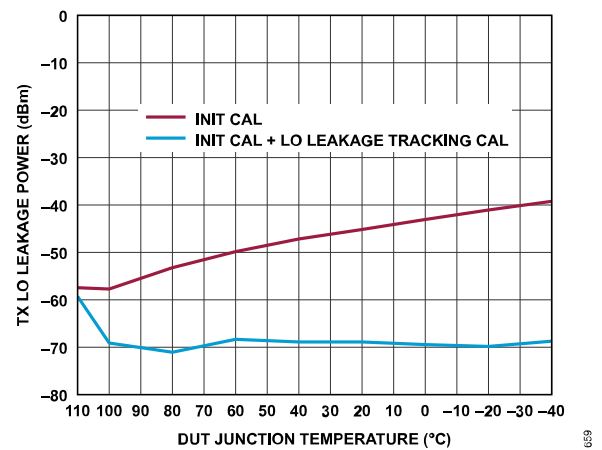


Figure 177. Transmitter LO Leakage Power vs. DUT Junction Temperature (High to Low), Baseband Frequency = 4 MHz, Backoff = 0.5 dBFS, Attenuation Code = 0

TYPICAL PERFORMANCE CHARACTERISTICS

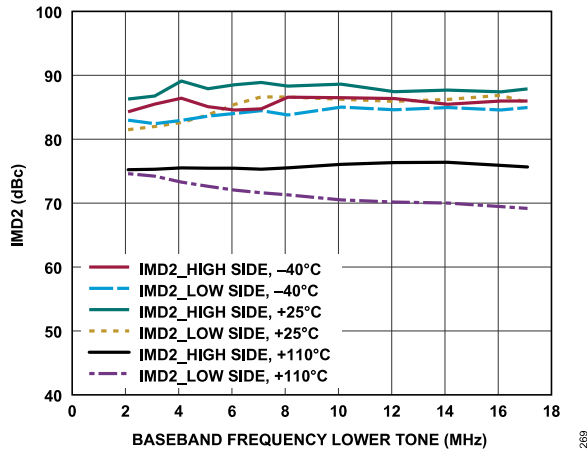


Figure 178. Transmitter IMD2 vs. Baseband Frequency, Transmitter Attenuation Code = 0, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz

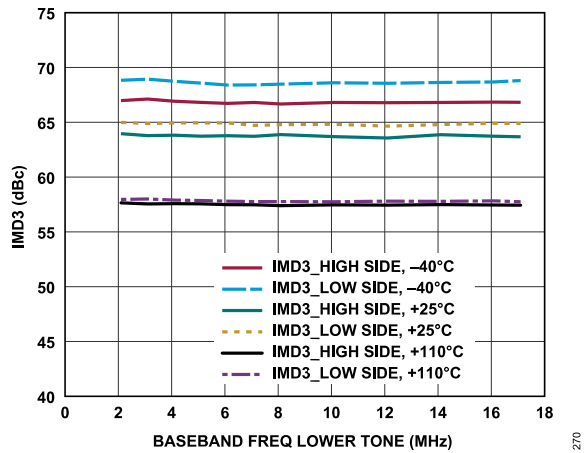


Figure 179. Transmitter IMD3 vs. Baseband Frequency, Transmitter Attenuation Code = 0, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz

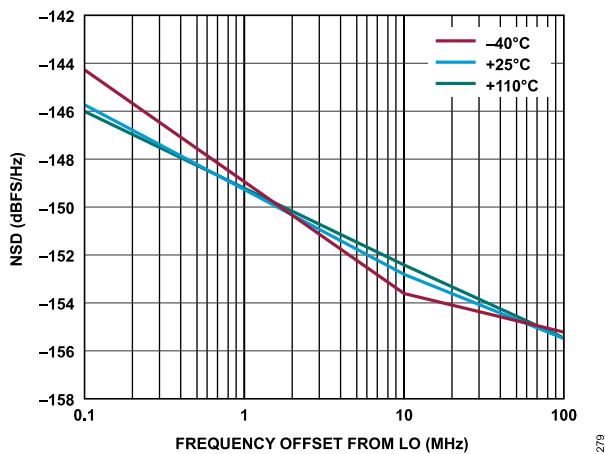


Figure 180. Transmitter NSD vs. Frequency Offset from LO, Baseband Frequency = 5.6 MHz, Transmitter Channel = Ch1

TYPICAL PERFORMANCE CHARACTERISTICS

5800 MHz LO

The temperature settings refer to the die temperature. All LO frequencies set to 5800 MHz, unless otherwise noted.

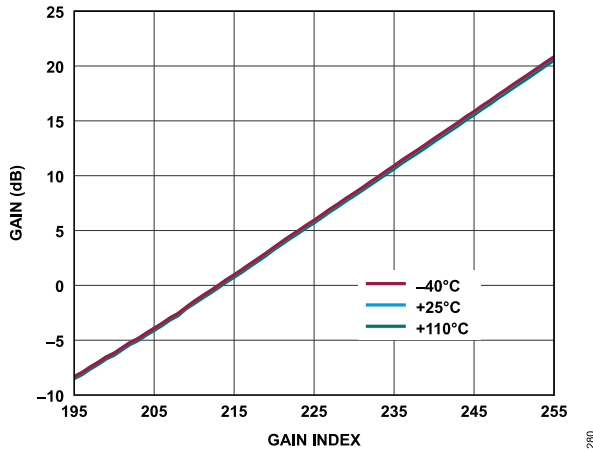


Figure 181. Receiver Absolute Gain (Complex) vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance, $P_{OUT} = -9.6$ dBFS

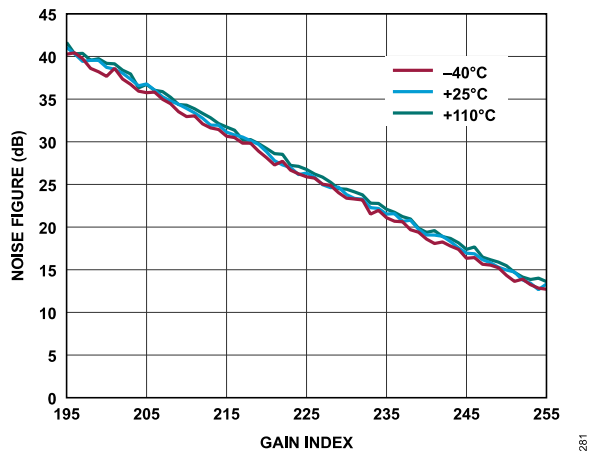


Figure 182. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

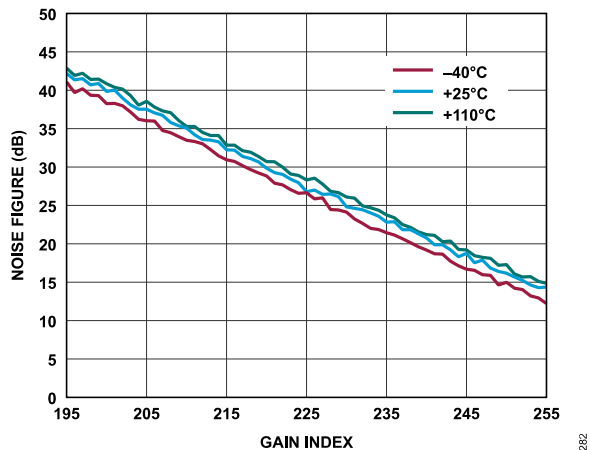


Figure 183. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = Low Power

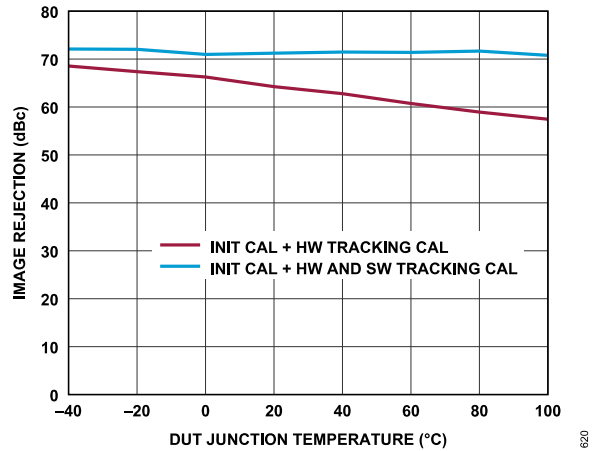


Figure 184. Receiver Image Rejection vs. DUT Junction Temperature (Low to High), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = High Performance, $P_{OUT} = -11.1$ dBFS

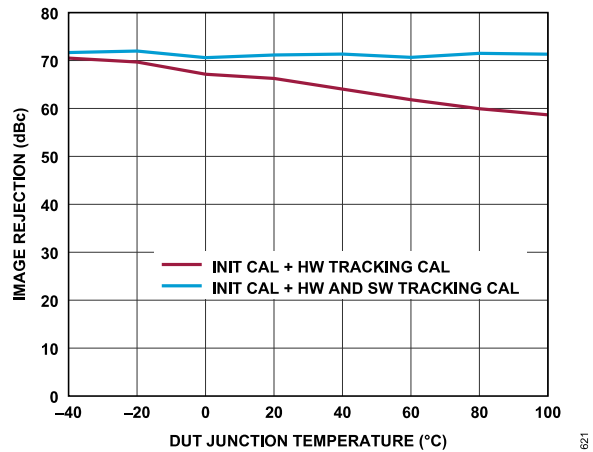


Figure 185. Receiver Image Rejection vs. DUT Junction Temperature (Low to High), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = Low Power, $P_{OUT} = -11.1$ dBFS

TYPICAL PERFORMANCE CHARACTERISTICS

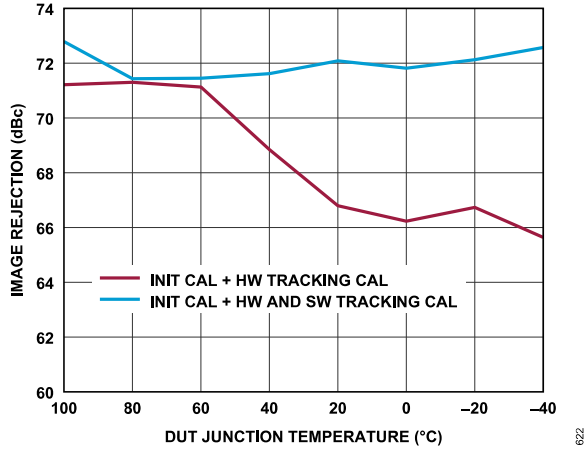


Figure 186. Receiver Image Rejection vs. DUT Junction Temperature (High to Low), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = High Performance, $P_{OUT} = -11.1$ dBFS

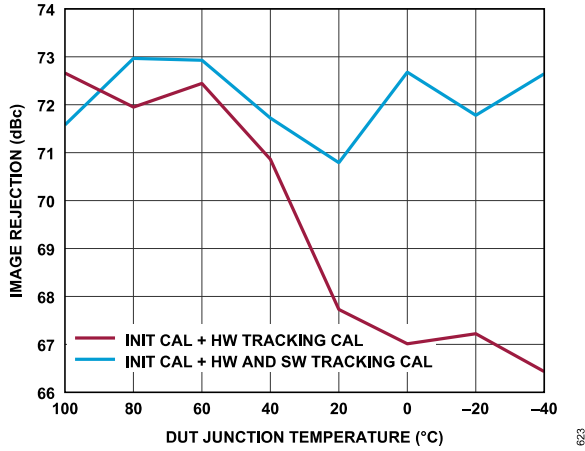


Figure 187. Receiver Image Rejection vs. DUT Junction Temperature (High to Low), Tone 1 Baseband Frequency = -5.1 MHz, Tone 2 Baseband Frequency = 13.9 MHz, ADC = Low Power, $P_{OUT} = -11.1$ dBFS

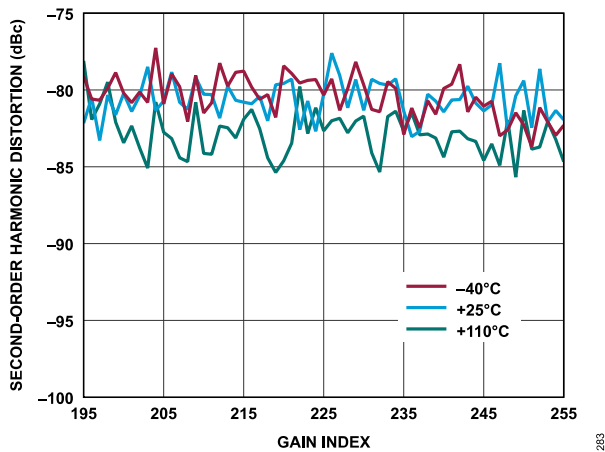


Figure 188. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

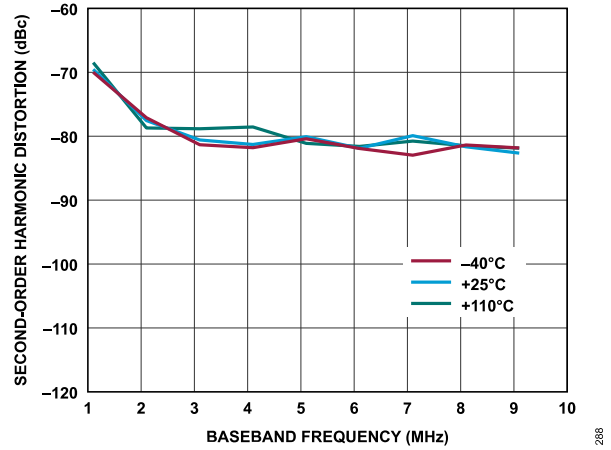


Figure 189. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

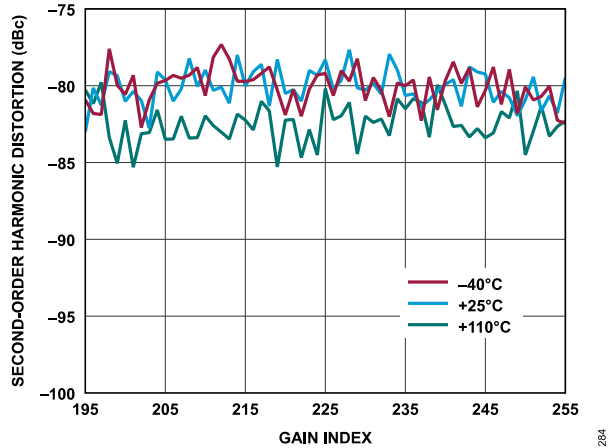


Figure 190. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = Low Power

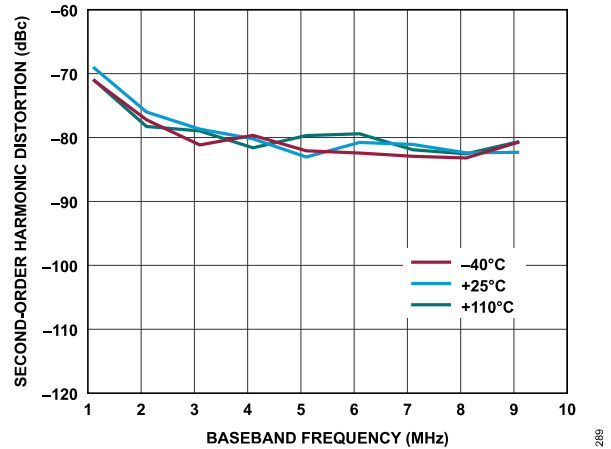


Figure 191. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = Low Power

TYPICAL PERFORMANCE CHARACTERISTICS

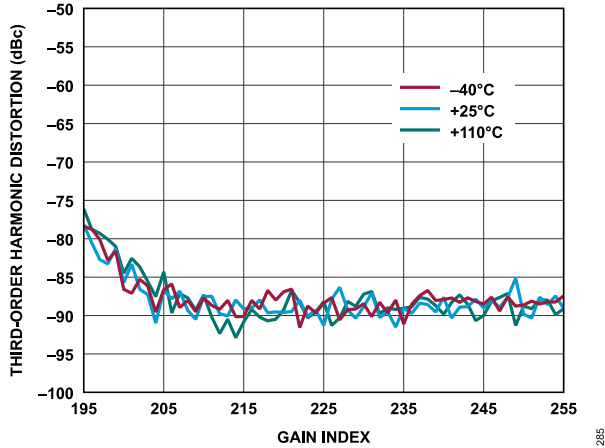


Figure 192. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

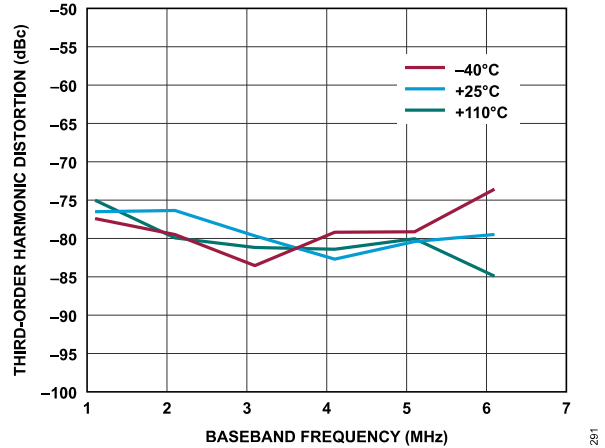


Figure 195. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain index = 255, ADC = Low Power

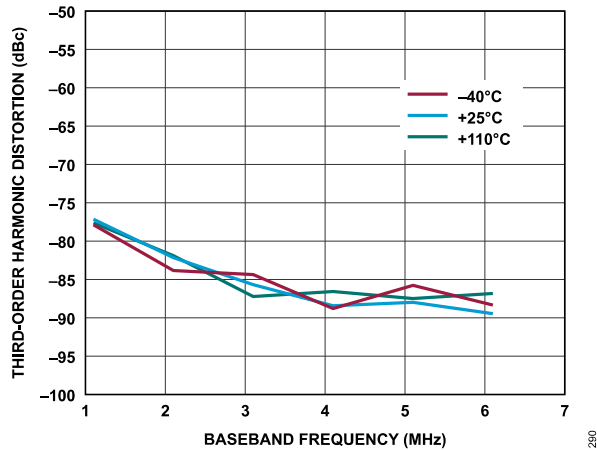


Figure 193. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

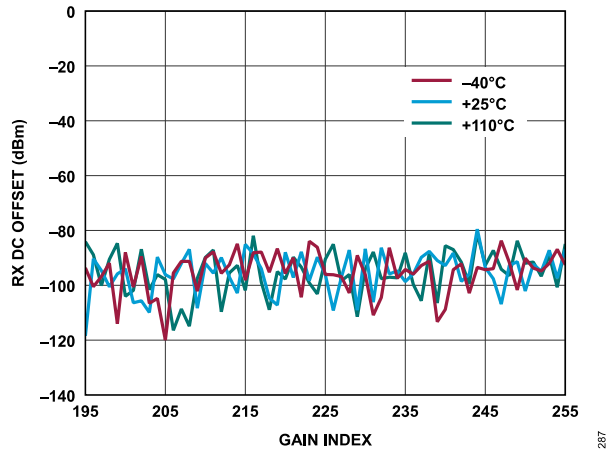


Figure 196. Receiver DC Offset vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = High Performance

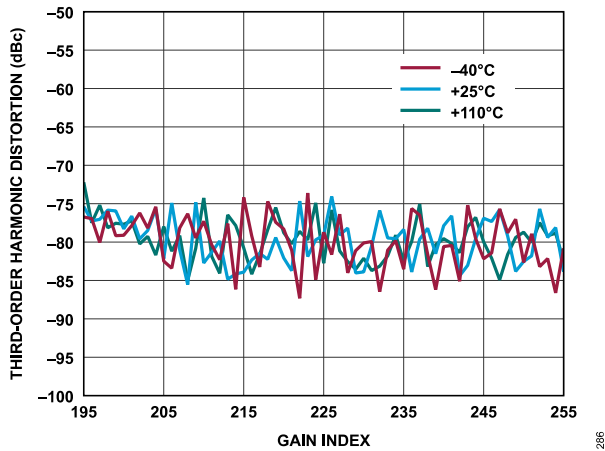


Figure 194. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 5.6 MHz, ADC = Low Power

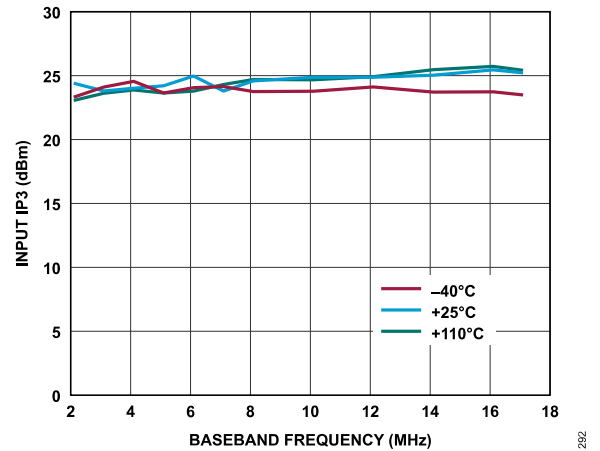


Figure 197. Receiver Input IP3 vs. Baseband Frequency, ADC = High Performance, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz, Gain Index = 255

TYPICAL PERFORMANCE CHARACTERISTICS

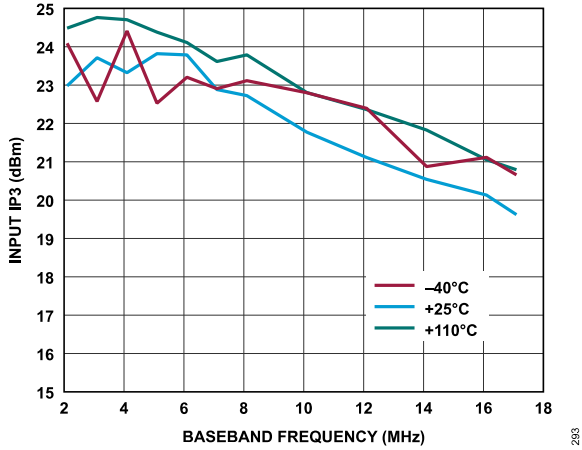


Figure 198. Receiver Input IP3 vs. Baseband Frequency, ADC = Low Power, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz, Gain Index = 255

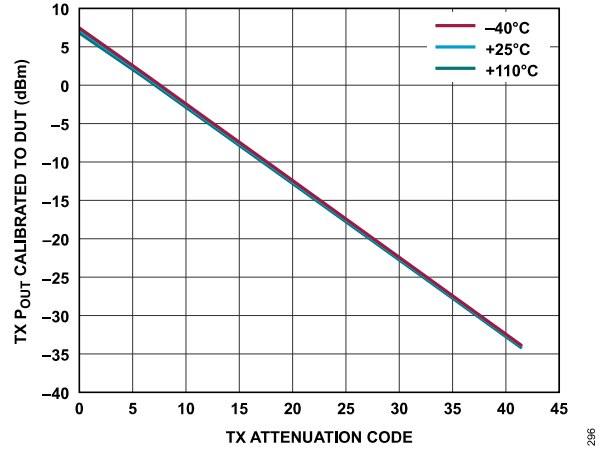


Figure 201. Transmitter Absolute Power vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

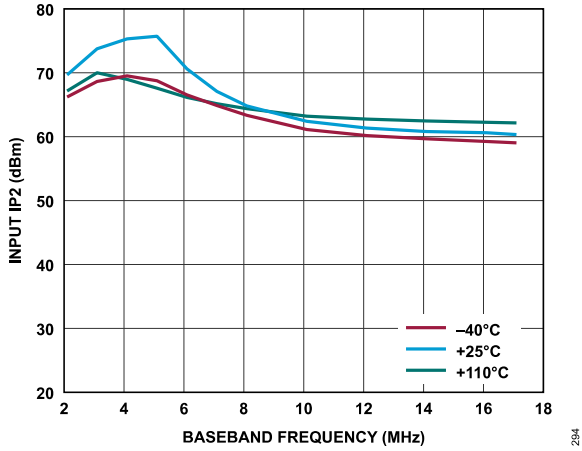


Figure 199. Receiver Input IP2 vs. Baseband Frequency, ADC = High Performance, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz, Gain Index = 255

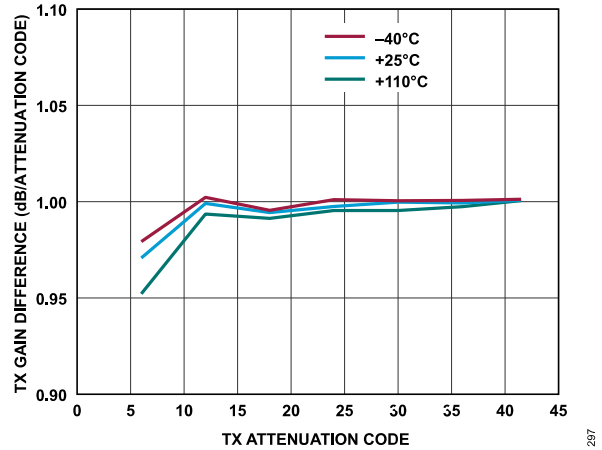


Figure 202. Transmitter Attenuation Delta (Error) vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

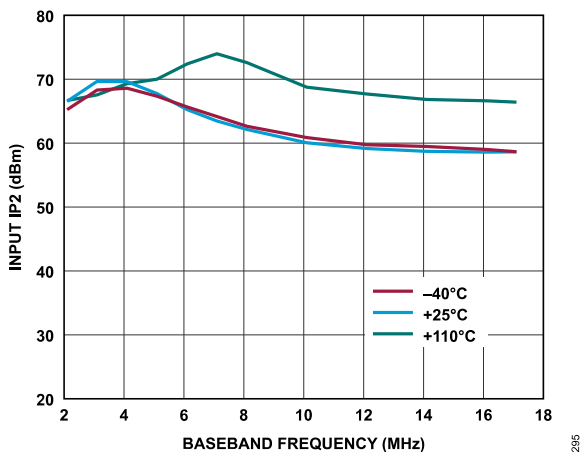


Figure 200. Receiver Input IP2 vs. Baseband Frequency, ADC = Low Power, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz, Gain Index = 255

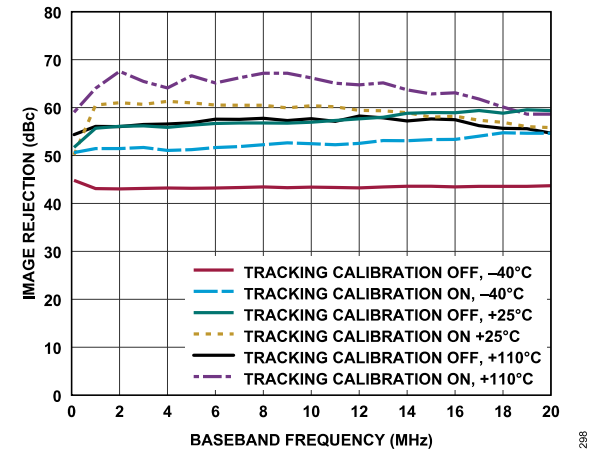


Figure 203. Transmitter Image Rejection vs. Baseband Frequency, Tracking Calibration On vs. Tracking Calibration Off, Transmitter Attenuation Code = 0

TYPICAL PERFORMANCE CHARACTERISTICS

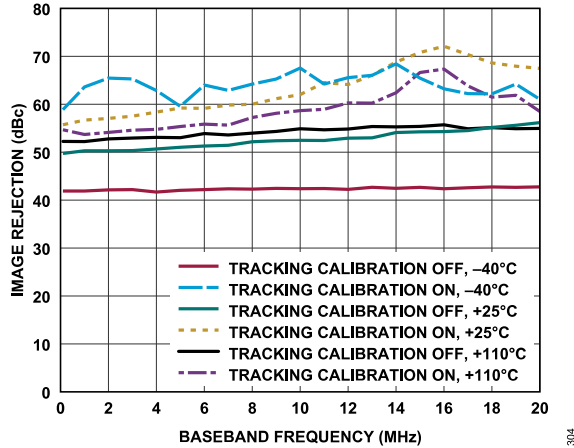


Figure 204. Transmitter Image Rejection vs. Baseband Frequency, Tracking Calibration On vs. Tracking Calibration Off, Transmitter Attenuation Code = 20

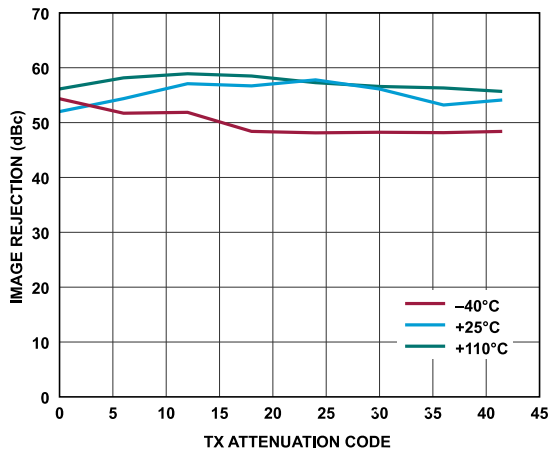


Figure 205. Transmitter Image Rejection vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS, Initialization Calibration Only

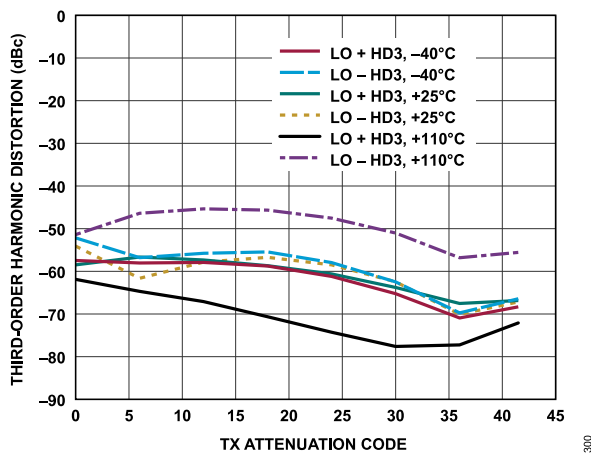


Figure 206. Transmitter Third-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

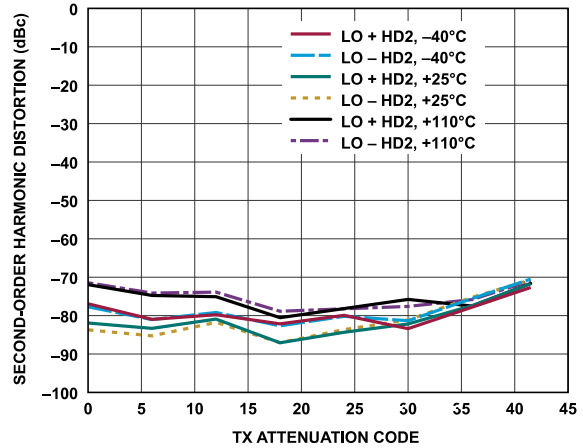


Figure 207. Transmitter Second-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 0.2 dBFS

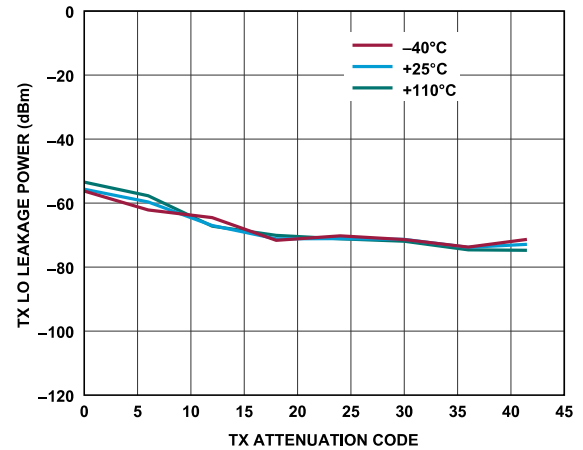


Figure 208. Transmitter LO Leakage Power vs. Transmitter Attenuation Code, Baseband Frequency = 18 MHz, Backoff = 6 dBFS, Initialization Calibration Only

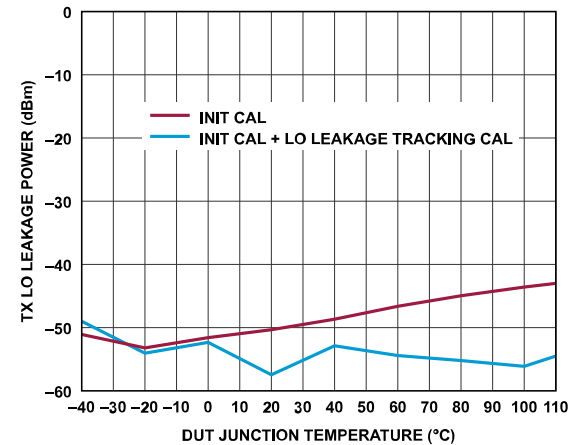


Figure 209. Transmitter LO Leakage Power vs. DUT Junction Temperature (Low to High), Baseband Frequency = 4 MHz, Backoff = 0.5 dBFS, Attenuation Code = 0

TYPICAL PERFORMANCE CHARACTERISTICS

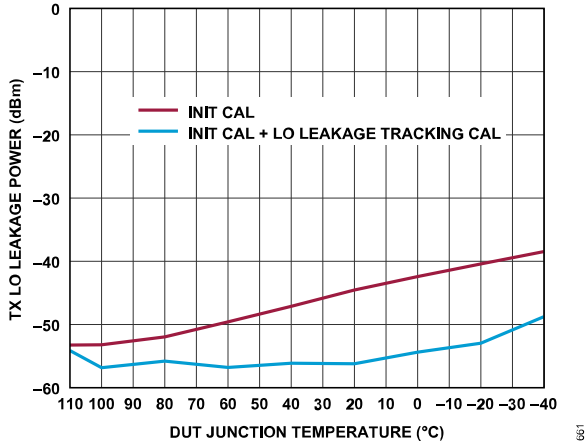


Figure 210. Transmitter LO Leakage Power vs. DUT Junction Temperature (High to Low), Baseband Frequency = 4 MHz, Backoff = 0.5 dBFS, Attenuation Code = 0

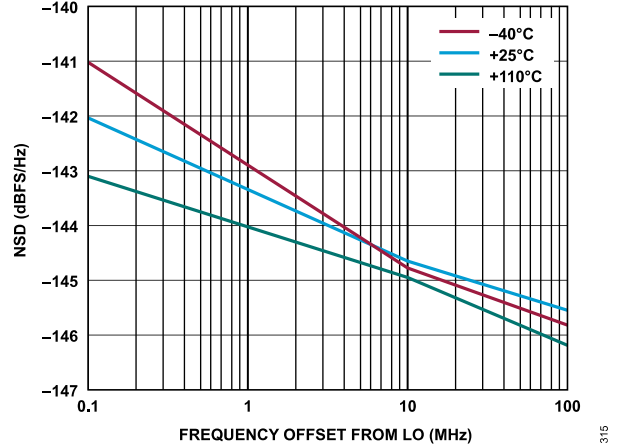


Figure 213. Transmitter NSD vs. Frequency Offset from LO, Baseband Frequency = 5.6 MHz, Transmitter Channel = Ch1

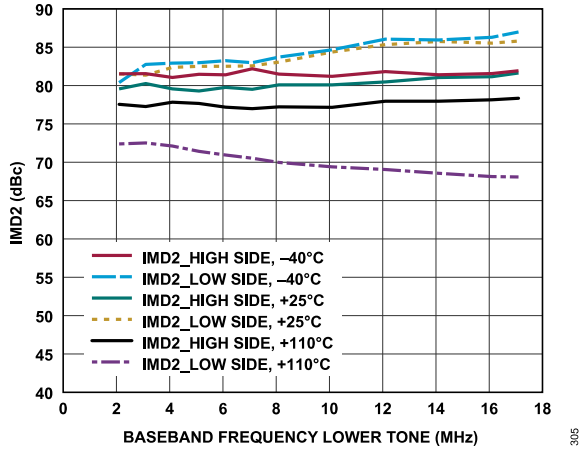


Figure 211. Transmitter IMD2 vs. Baseband Frequency, Transmitter Attenuation Code = 0, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz

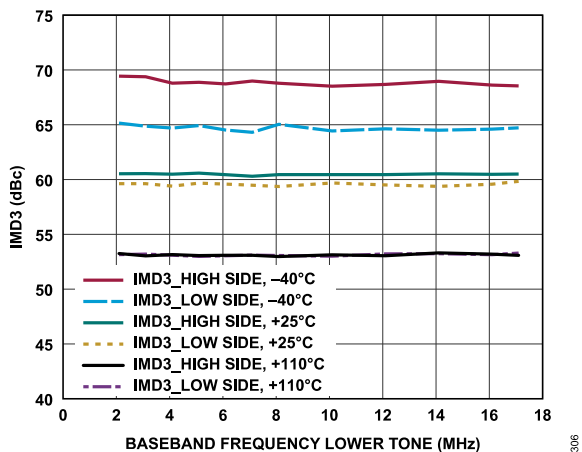


Figure 212. Transmitter IMD3 vs. Baseband Frequency, Transmitter Attenuation Code = 0, f_1 = Baseband Frequency, f_2 = Baseband Frequency + 1 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

NARROW-BAND

Device configuration profile: receiver = 25 kHz bandwidth, receiver IF = 490 kHz, I/Q rate = 144 kHz, transmitter = 25 kHz bandwidth, I/Q rate = 144 kHz, device clock = 38.4 MHz, and an internal LO is used for all measurements. Measurements are at nominal power supply voltages. All RF specifications are based on measurements that include PCB and matching circuit losses, unless otherwise noted. Specifications are applicable over the lifetime of the device.

30 MHz LO

The temperature settings refer to the die temperature. All LO frequencies are set to 30 MHz, unless otherwise noted.

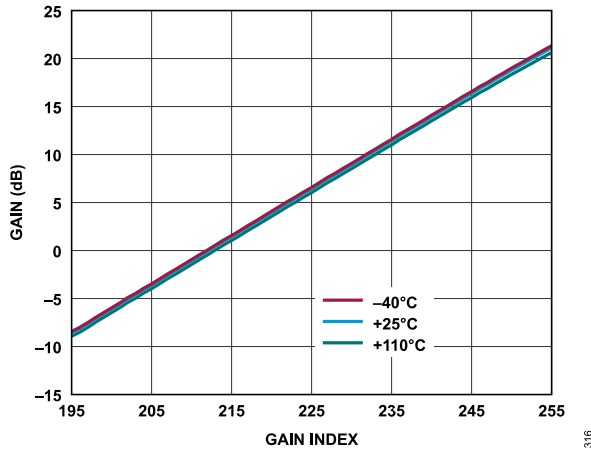


Figure 214. Receiver Absolute Gain (Complex) vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance, $P_{OUT} = -9.6$ dBFS

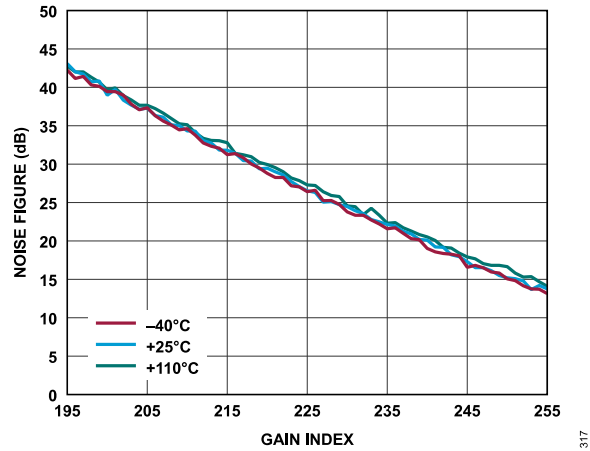


Figure 216. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

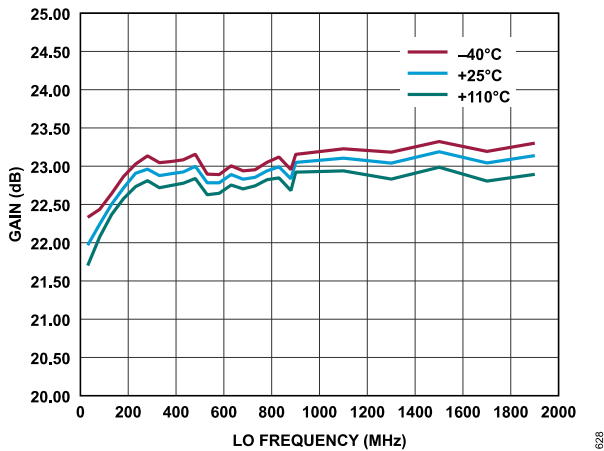


Figure 215. Receiver Absolute Gain (Complex) vs. LO Frequency, Baseband Frequency = 2.1 kHz, ADC = High Performance, $P_{OUT} = -9.6$ dBFS

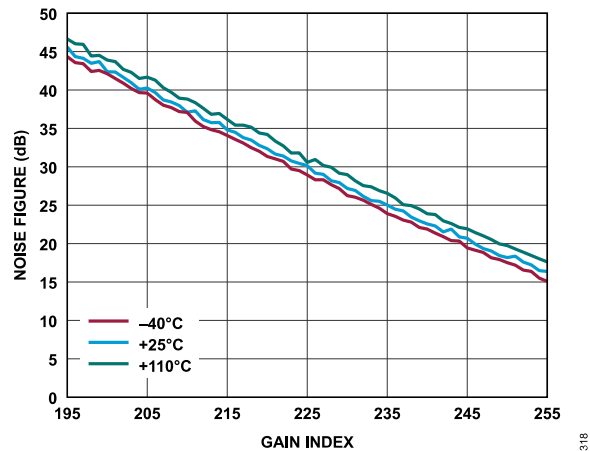


Figure 217. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = Low Power

TYPICAL PERFORMANCE CHARACTERISTICS

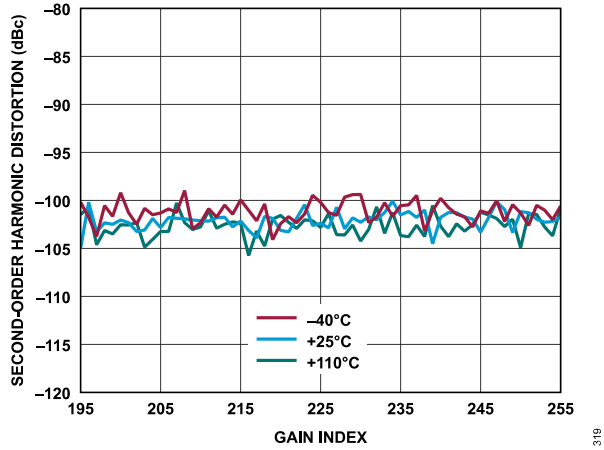


Figure 218. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

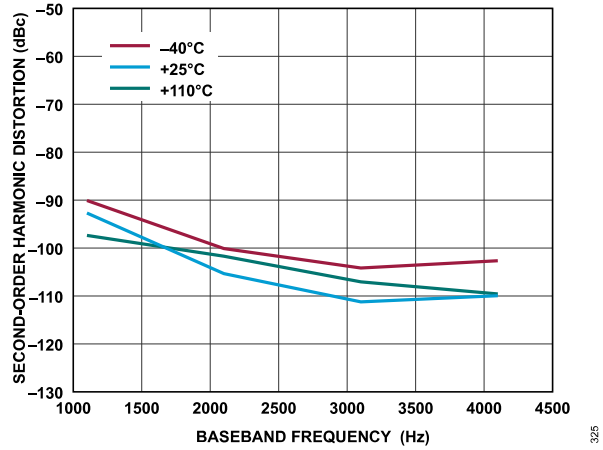


Figure 221. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = Low Power

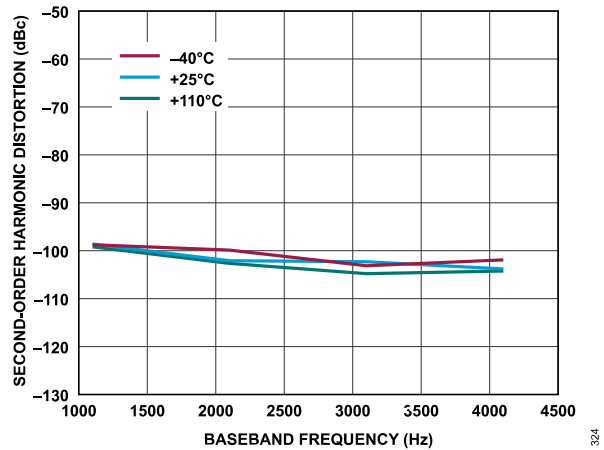


Figure 219. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

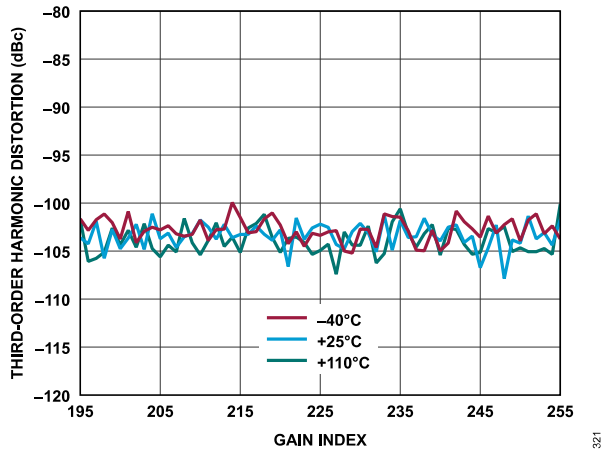


Figure 222. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

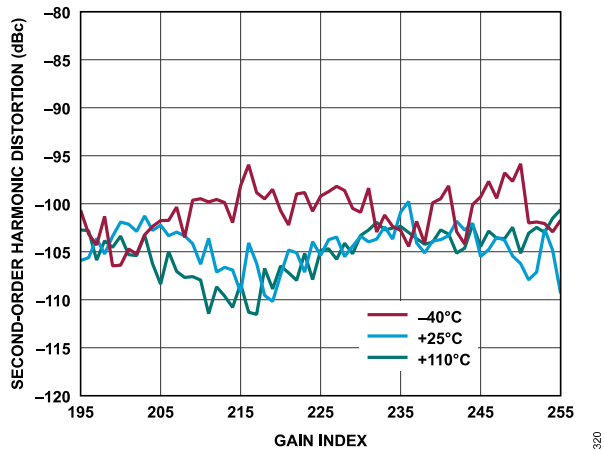


Figure 220. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = Low Power

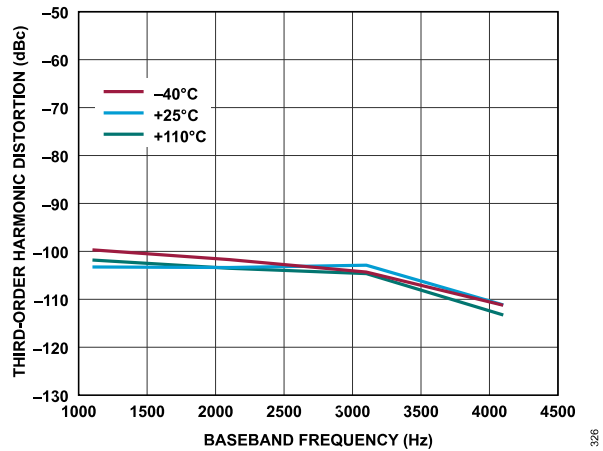


Figure 223. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

TYPICAL PERFORMANCE CHARACTERISTICS

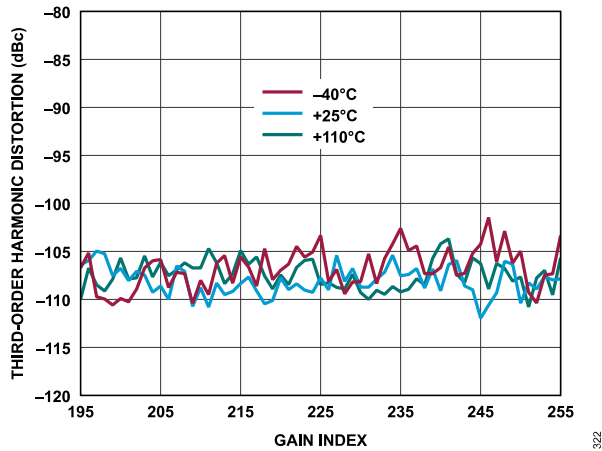


Figure 224. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = Low Power

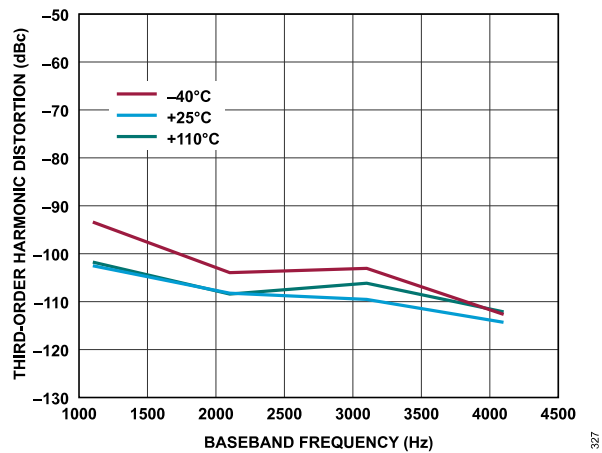


Figure 225. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = Low Power

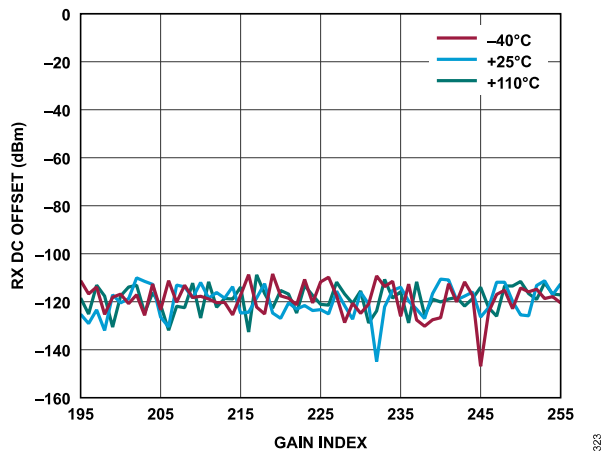


Figure 226. Receiver DC Offset vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

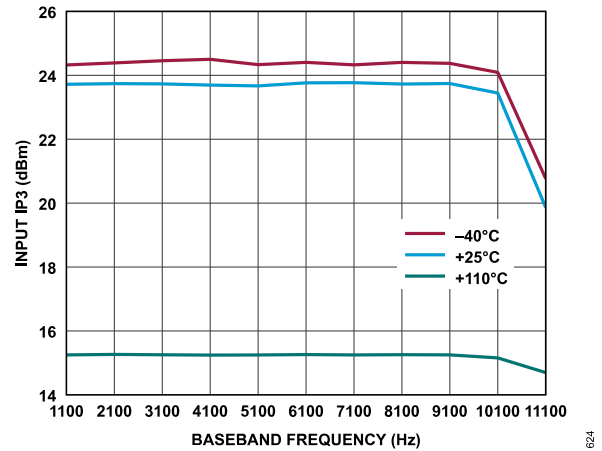


Figure 227. Receiver Input IP3 vs. Baseband Frequency, ADC = High Performance, $f_1 = \text{Baseband Frequency} + 1 \text{ MHz}$, $f_2 = \text{Baseband Frequency} + 2 \text{ MHz}$, Gain Index = 255, First-Order TIA with $f_{1dB} = 4 \text{ MHz}$, $P_{OUT} = -15.1 \text{ dBFS}$ at -40°C and $+25^\circ\text{C}$, $P_{OUT} = -18.1 \text{ dBFS}$ at $+110^\circ\text{C}$

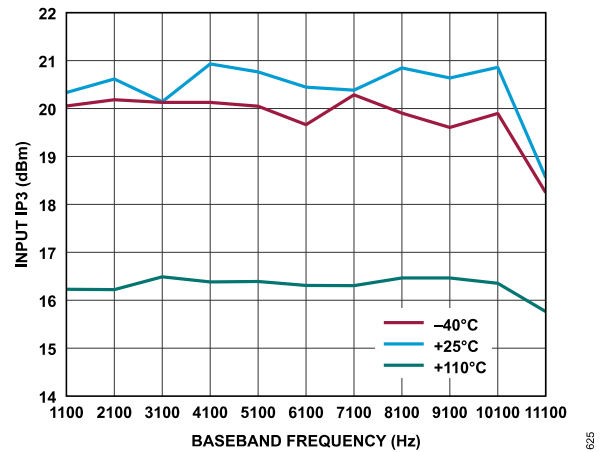


Figure 228. Receiver Input IP3 vs. Baseband Frequency, ADC = Low Power, $f_1 = \text{Baseband Frequency} + 1 \text{ MHz}$, $f_2 = \text{Baseband Frequency} + 2 \text{ MHz}$, Gain Index = 255, First-Order TIA with $f_{1dB} = 4 \text{ MHz}$, $P_{OUT} = -15.1 \text{ dBFS}$ at -40°C and $+25^\circ\text{C}$, $P_{OUT} = -18.1 \text{ dBFS}$ at $+110^\circ\text{C}$

TYPICAL PERFORMANCE CHARACTERISTICS

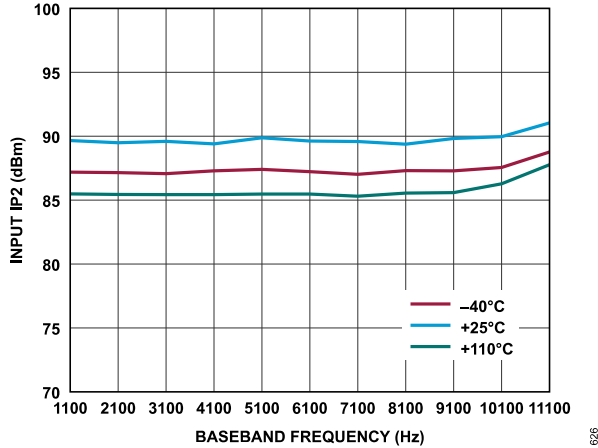


Figure 229. Receiver Input IP2 vs. Baseband Frequency, ADC = High Performance, f_1 = Baseband Frequency + 1 MHz, f_2 = Baseband Frequency + 2 MHz, Gain Index = 255, First-Order TIA with f_{3dB} = 4 MHz, P_{OUT} = -11.6 dBFS

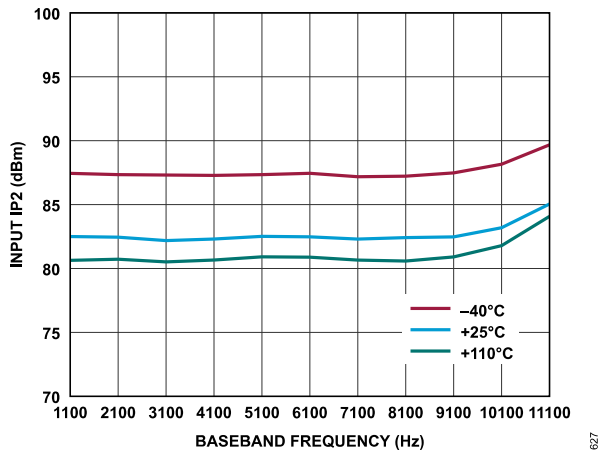


Figure 230. Receiver Input IP2 vs. Baseband Frequency, ADC = Low Power, f_1 = Baseband Frequency + 1 MHz, f_2 = Baseband Frequency + 2 MHz, Gain Index = 255, First-Order TIA with f_{3dB} = 4 MHz, P_{OUT} = -11.6 dBFS

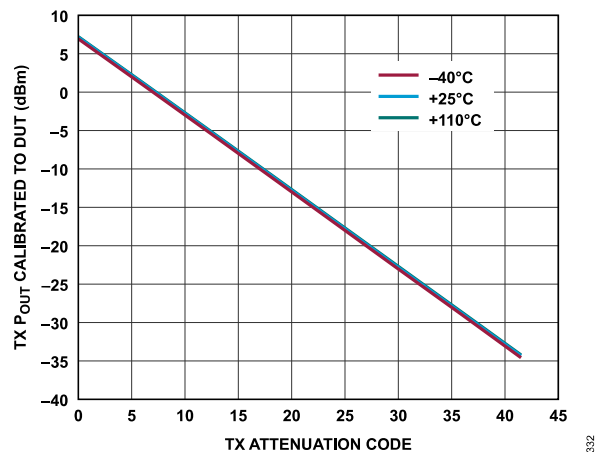


Figure 231. Transmitter Absolute Power vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

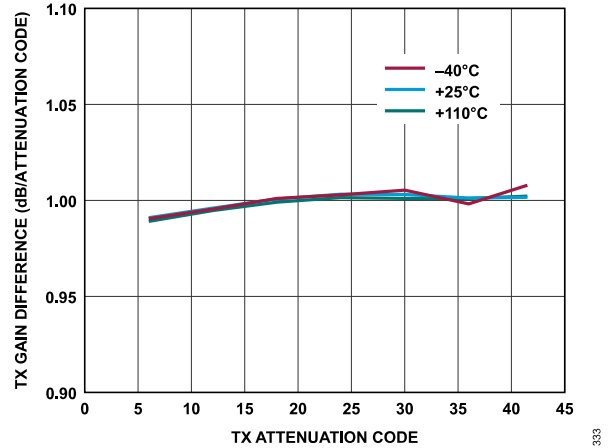


Figure 232. Transmitter Attenuation Delta (Error) vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

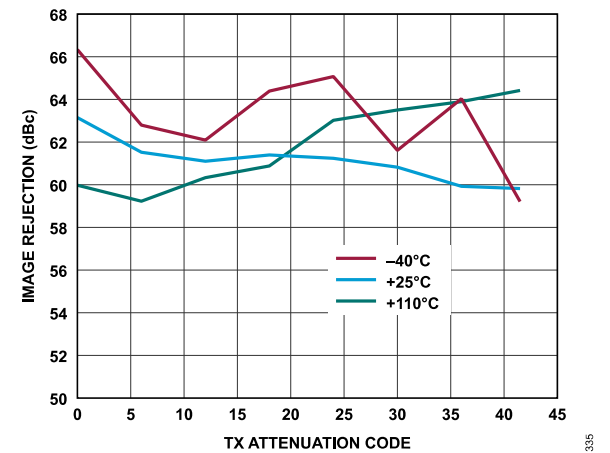


Figure 233. Transmitter Image Rejection vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

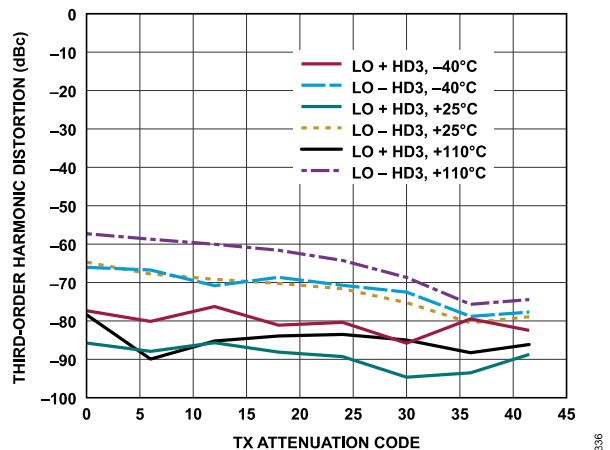


Figure 234. Transmitter Third-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS, Initialization Calibration Only

TYPICAL PERFORMANCE CHARACTERISTICS

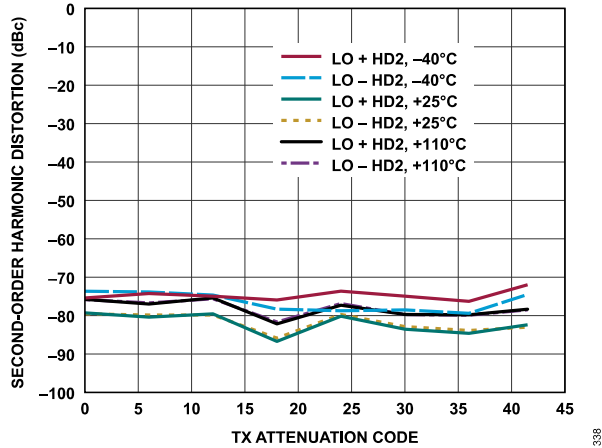


Figure 235. Transmitter Second-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

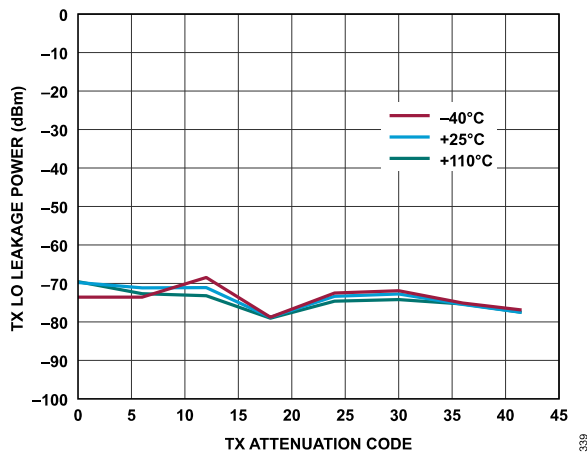


Figure 236. Transmitter LO Leakage Power vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 6 dBFS, Initialization Calibration Only

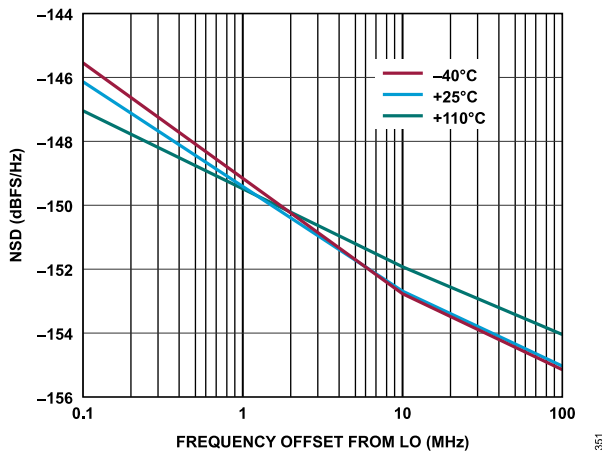


Figure 237. Transmitter NSD vs. Frequency Offset from LO, Baseband Frequency = 2.1 kHz, Transmitter Channel = Channel 1

TYPICAL PERFORMANCE CHARACTERISTICS

470 MHz LO

The temperature settings refer to the die temperature. All LO frequencies set to 470 MHz, unless otherwise noted.

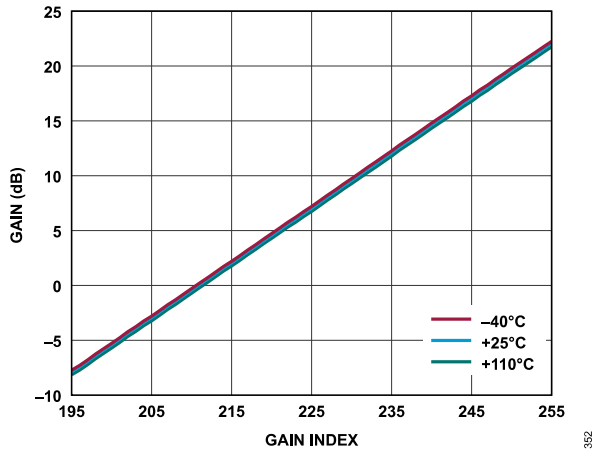


Figure 238. Receiver Absolute Gain (Complex) vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance, $P_{OUT} = -9.6$ dBFS

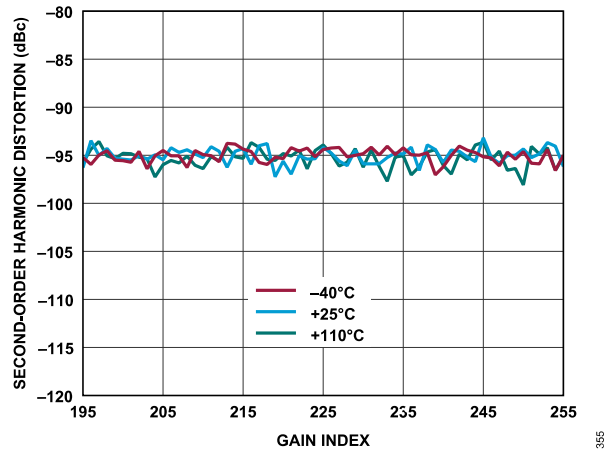


Figure 241. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

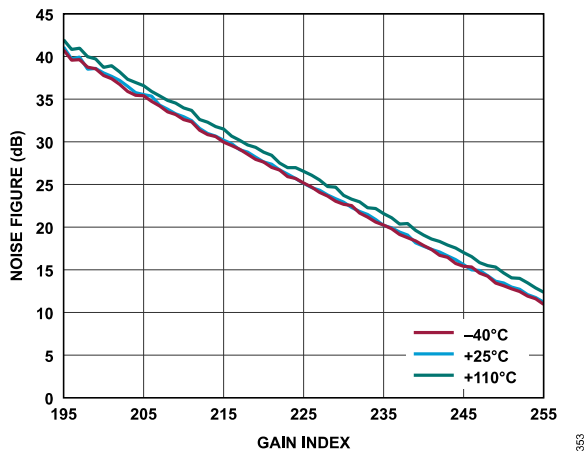


Figure 239. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

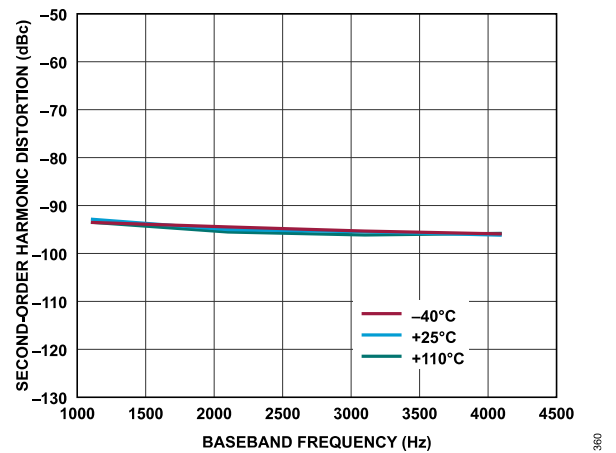


Figure 242. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

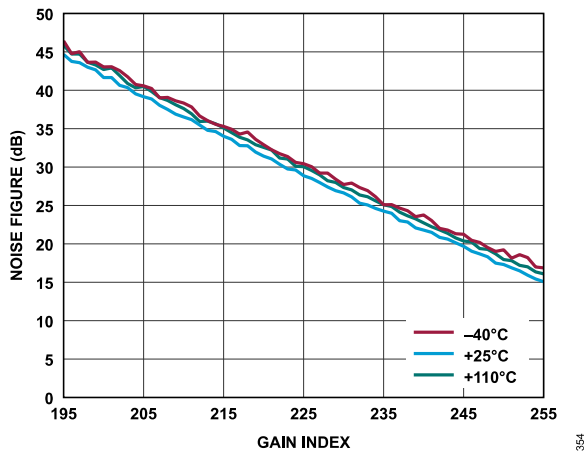


Figure 240. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = Low Power

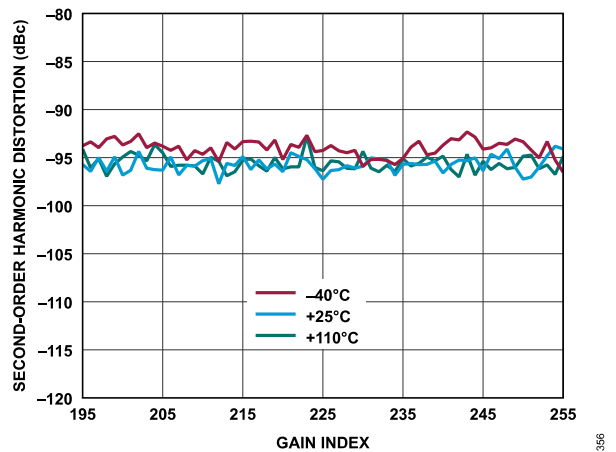


Figure 243. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = Low Power

TYPICAL PERFORMANCE CHARACTERISTICS

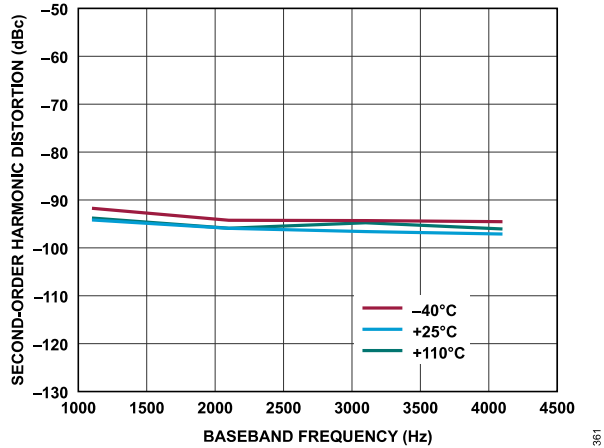


Figure 244. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = Low Power

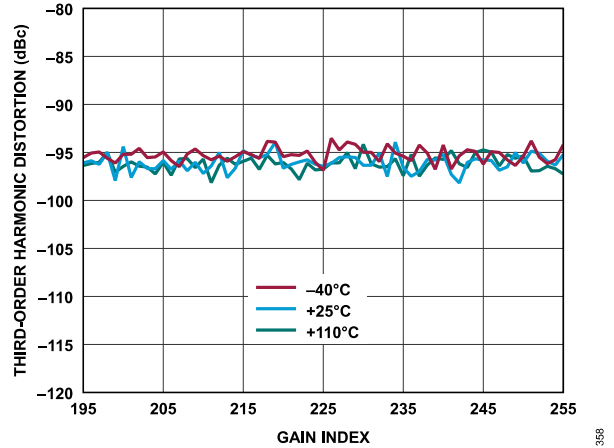


Figure 247. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = Low Power

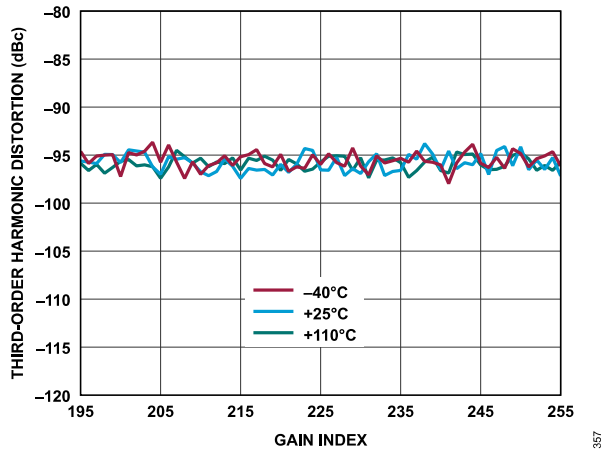


Figure 245. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

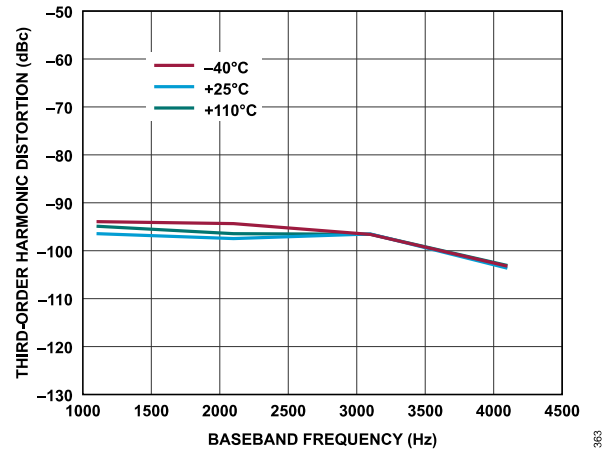


Figure 248. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = Low Power

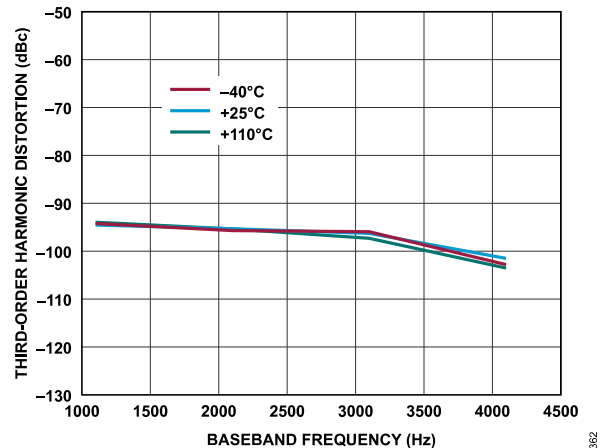


Figure 246. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

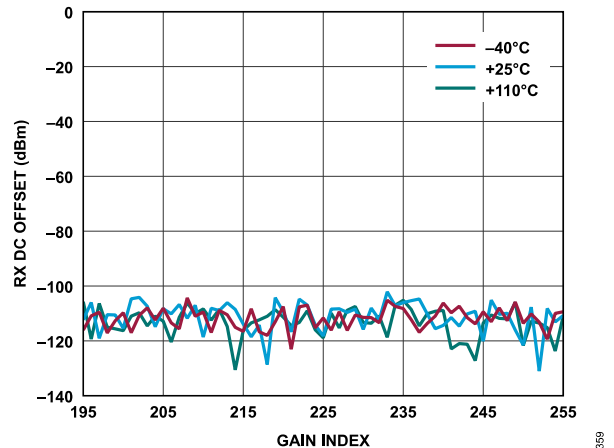


Figure 249. Receiver DC Offset vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

TYPICAL PERFORMANCE CHARACTERISTICS

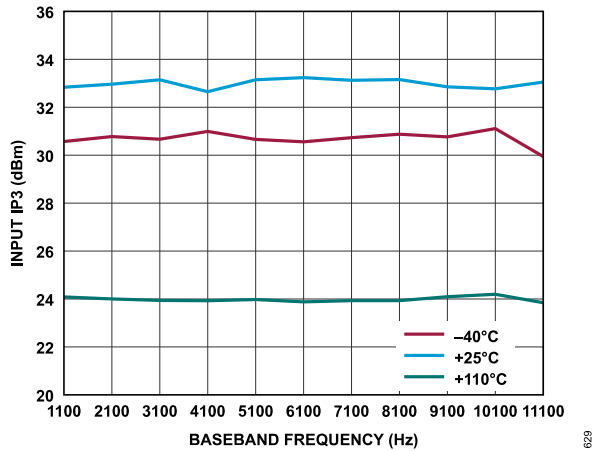


Figure 250. Receiver Input IP3 vs. Baseband Frequency, ADC = High Performance, $f_1 = \text{Baseband Frequency} + 1 \text{ MHz}$, $f_2 = \text{Baseband Frequency} + 2 \text{ MHz}$, Gain Index = 255, First-Order TIA with $f_{1dB} = 4 \text{ MHz}$, $P_{OUT} = -13.6 \text{ dBFS}$ at -40°C and $+25^\circ\text{C}$, $P_{OUT} = -16.6 \text{ dBFS}$ at $+110^\circ\text{C}$

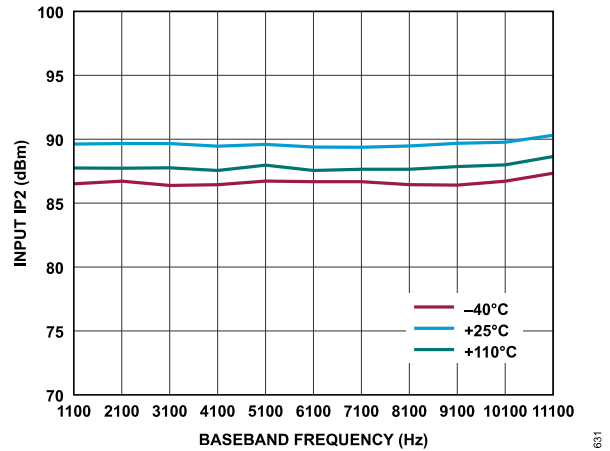


Figure 252. Receiver Input IP2 vs. Baseband Frequency, ADC = High Performance, $f_1 = \text{Baseband Frequency} + 1 \text{ MHz}$, $f_2 = \text{Baseband Frequency} + 2 \text{ MHz}$, Gain Index = 255, First-Order TIA with $f_{3dB} = 4 \text{ MHz}$, $P_{OUT} = -11.6 \text{ dBFS}$

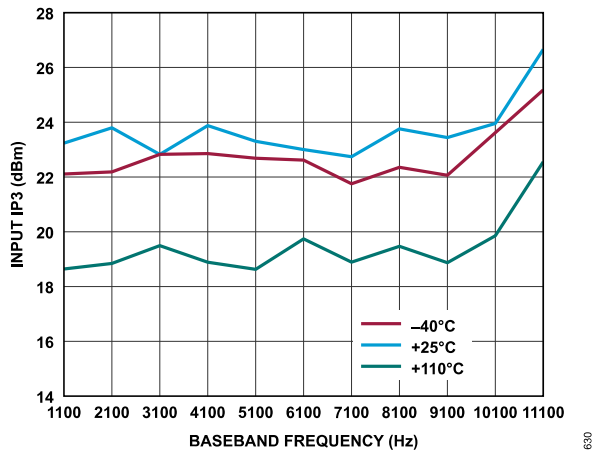


Figure 251. Receiver Input IP3 vs. Baseband Frequency, ADC = Low Power, $f_1 = \text{Baseband Frequency} + 1 \text{ MHz}$, $f_2 = \text{Baseband Frequency} + 2 \text{ MHz}$, Gain Index = 255, First-Order TIA with $f_{1dB} = 4 \text{ MHz}$, $P_{OUT} = -13.6 \text{ dBFS}$ at -40°C and $+25^\circ\text{C}$, $P_{OUT} = -16.6 \text{ dBFS}$ at $+110^\circ\text{C}$

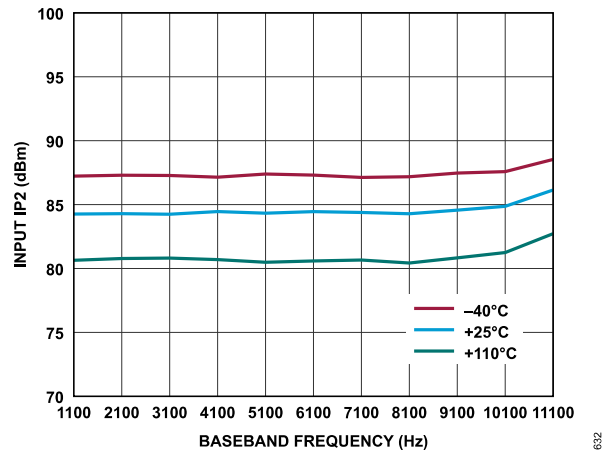


Figure 253. Receiver Input IP2 vs. Baseband Frequency, ADC = Low Power, $f_1 = \text{Baseband Frequency} + 1 \text{ MHz}$, $f_2 = \text{Baseband Frequency} + 2 \text{ MHz}$, Gain Index = 255, First-Order TIA with $f_{3dB} = 4 \text{ MHz}$, $P_{OUT} = -11.6 \text{ dBFS}$

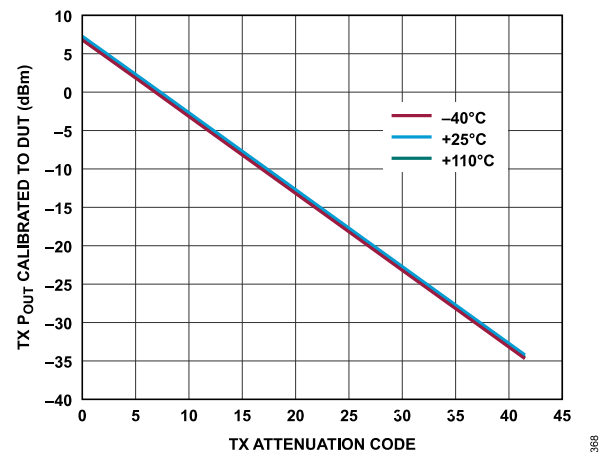


Figure 254. Transmitter Absolute Power vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

TYPICAL PERFORMANCE CHARACTERISTICS

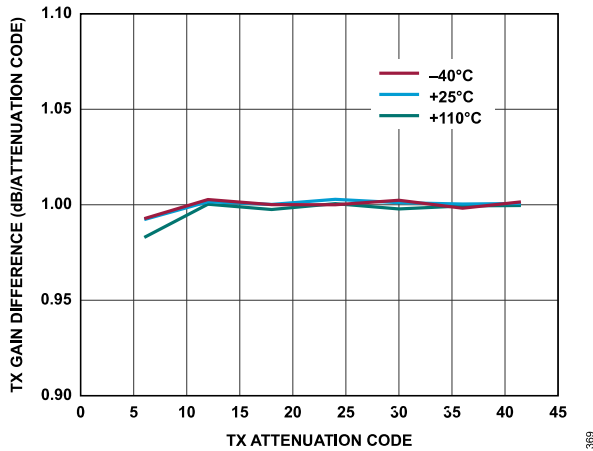


Figure 255. Transmitter Attenuation Delta (Error) vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

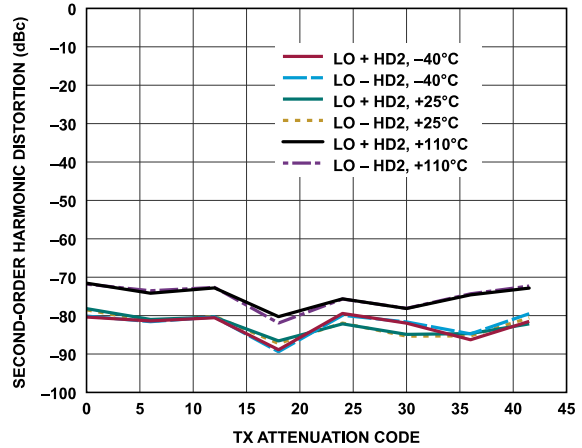


Figure 258. Transmitter Second-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

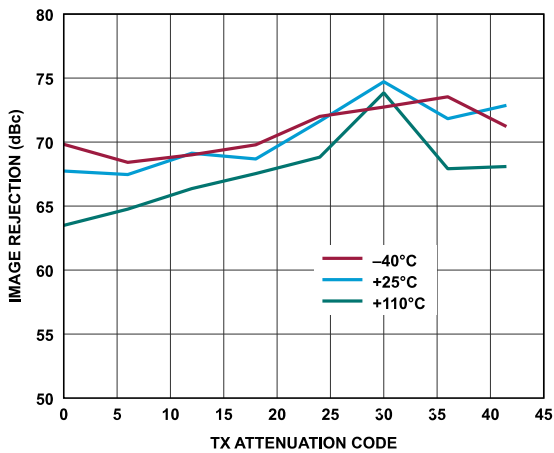


Figure 256. Transmitter Image Rejection vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS, Initialization Calibration Only

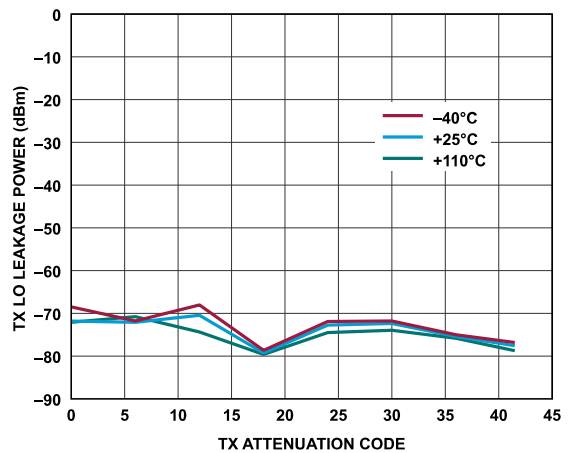


Figure 259. Transmitter LO Leakage Power vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 6 dBFS, Initialization Calibration Only

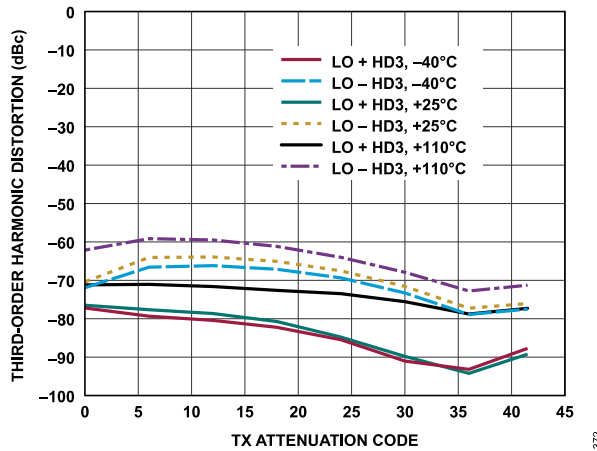


Figure 257. Transmitter Third-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

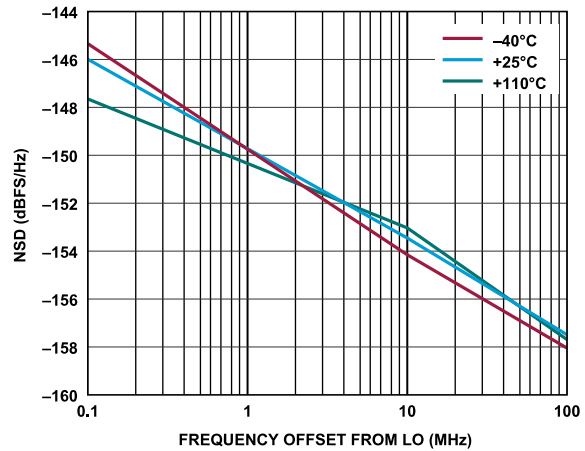


Figure 260. Transmitter NSD vs. Frequency Offset from LO, Baseband Frequency = 2.1 kHz, Transmitter Channel = Channel 1

TYPICAL PERFORMANCE CHARACTERISTICS

900 MHz LO

The temperature settings refer to the die temperature. All LO frequencies set to 900 MHz, unless otherwise noted.

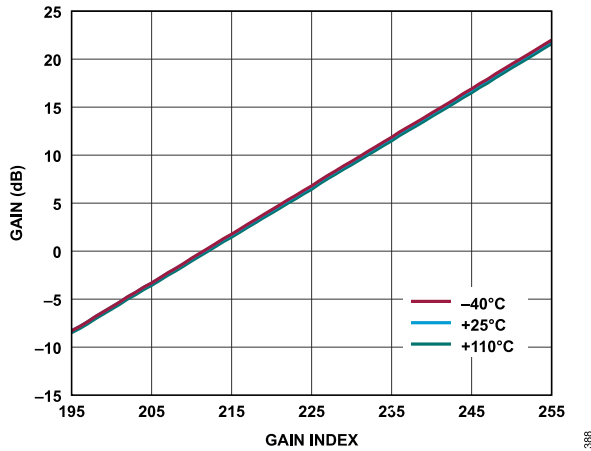


Figure 261. Receiver Absolute Gain (Complex) vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance, $P_{OUT} = -9.6$ dBFS

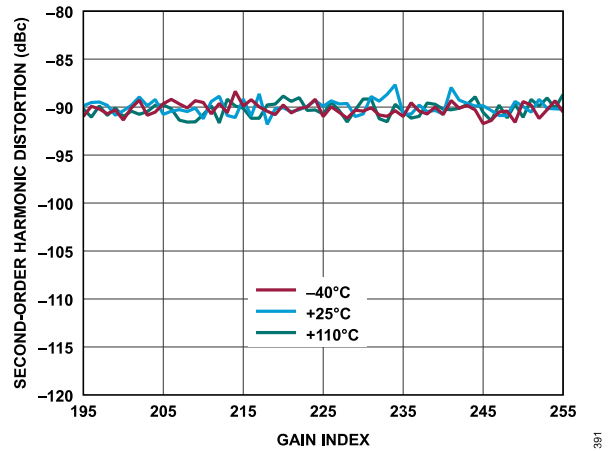


Figure 264. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

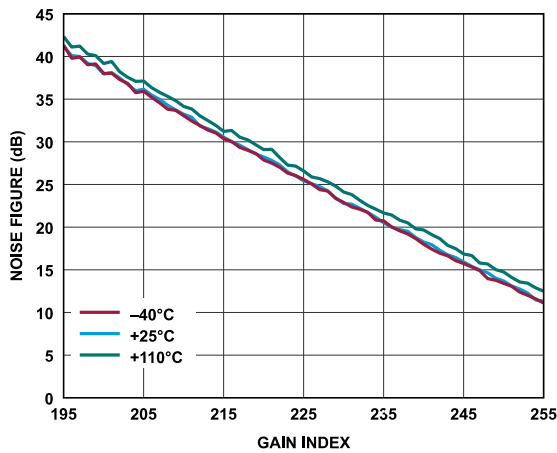


Figure 262. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

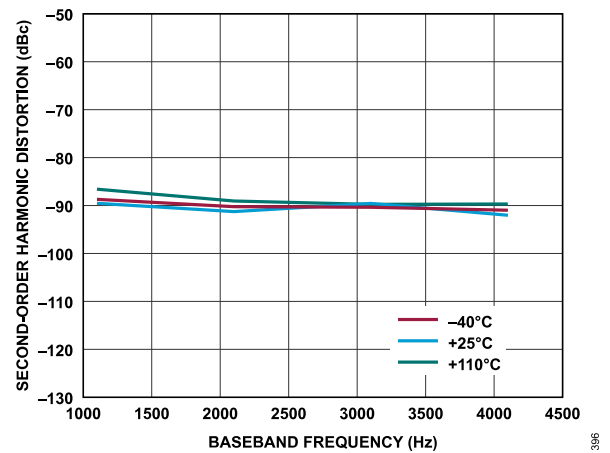


Figure 265. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

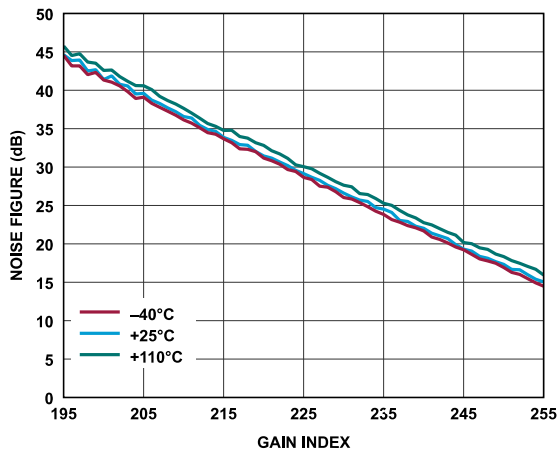


Figure 263. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = Low Power

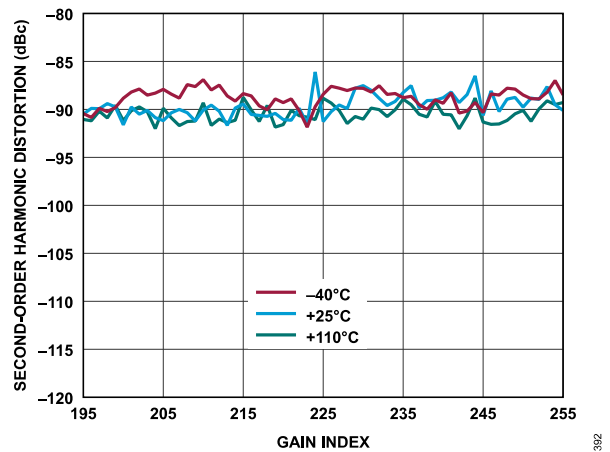


Figure 266. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = Low Power

TYPICAL PERFORMANCE CHARACTERISTICS

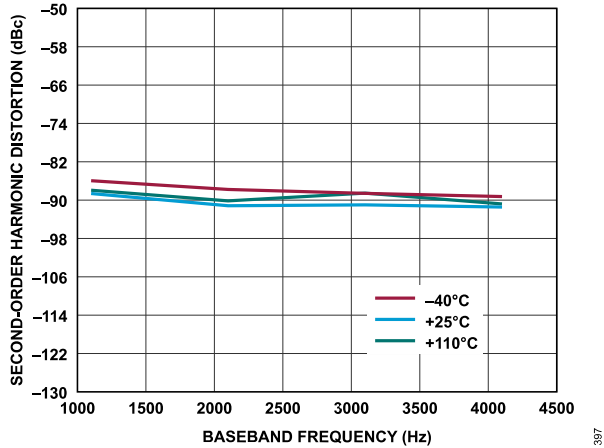


Figure 267. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = Low Power

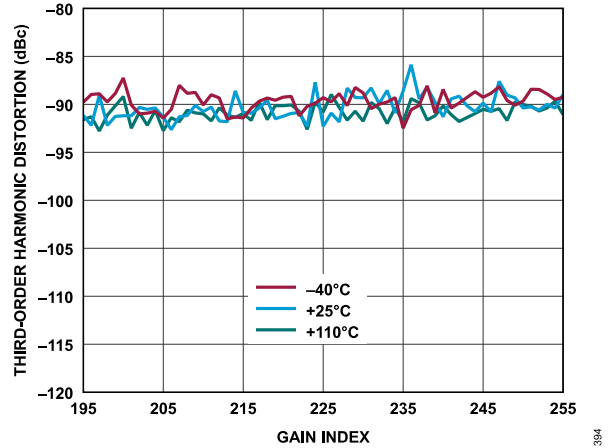


Figure 270. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = Low Power

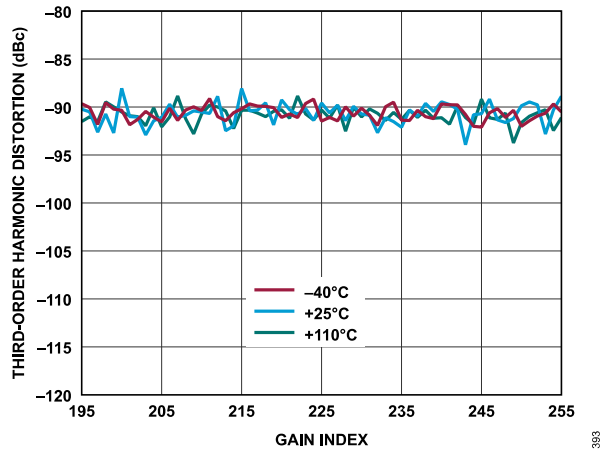


Figure 268. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

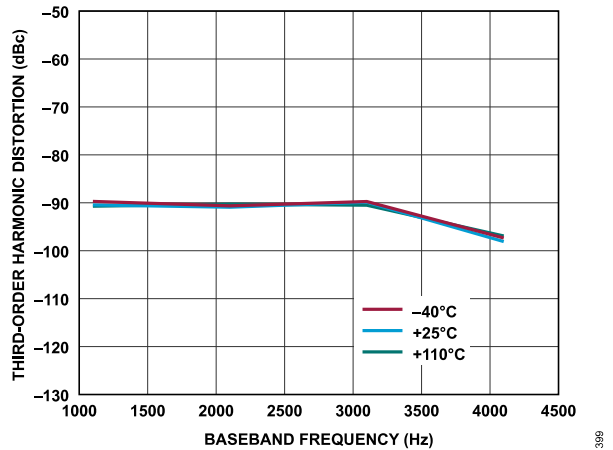


Figure 271. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = Low Power

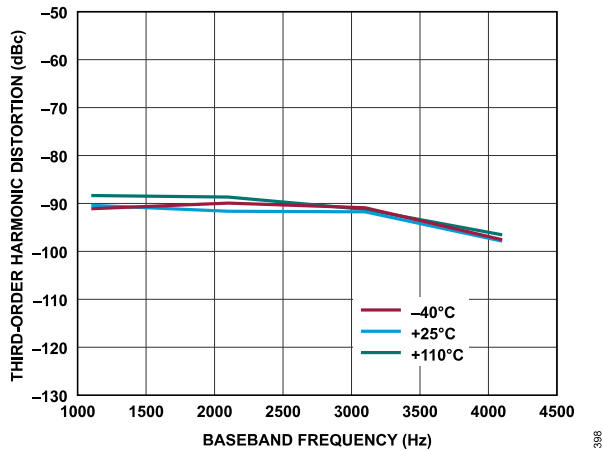


Figure 269. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

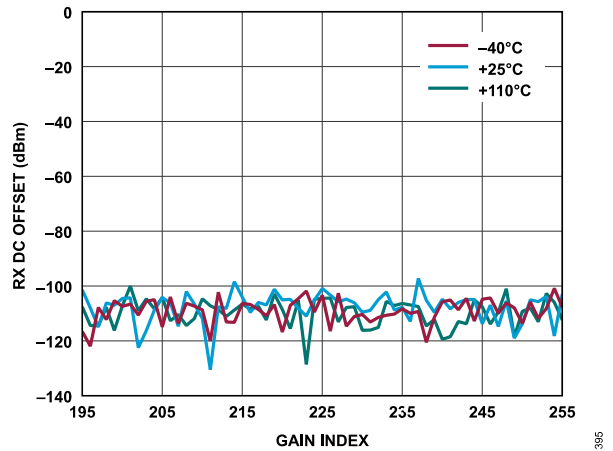


Figure 272. Receiver DC Offset vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

TYPICAL PERFORMANCE CHARACTERISTICS

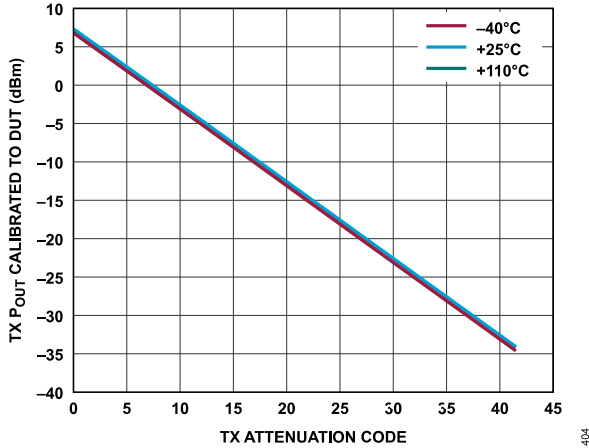


Figure 273. Transmitter Absolute Power vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

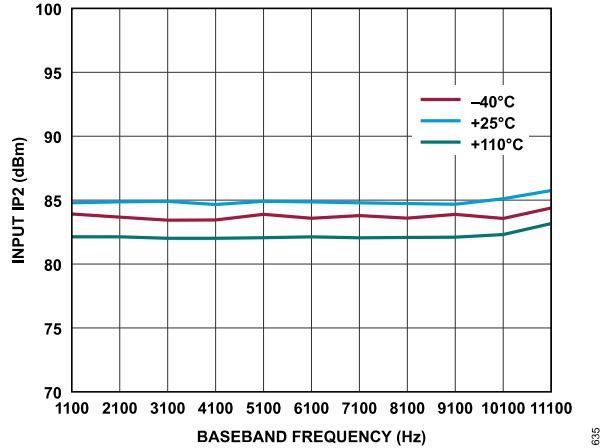


Figure 276. Receiver Input IP2 vs. Baseband Frequency, ADC = High Performance, f_1 = Baseband Frequency + 1 MHz, f_2 = Baseband Frequency + 2 MHz, Gain Index = 255, First-Order TIA with f_{3dB} = 4 MHz, P_{OUT} = -11.6 dBFS

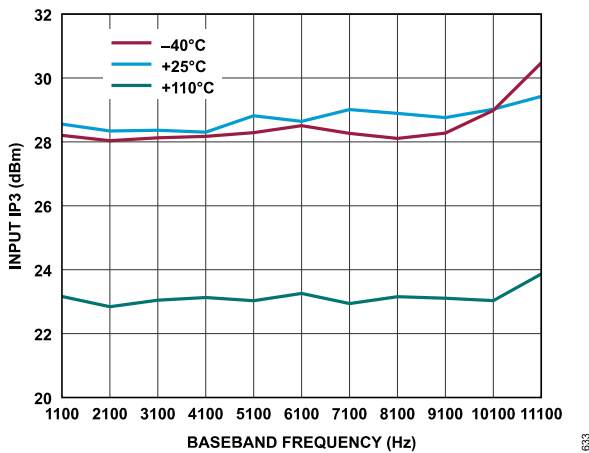


Figure 274. Receiver Input IP3 vs. Baseband Frequency, ADC = High Performance, f_1 = Baseband Frequency + 1 MHz, f_2 = Baseband Frequency + 2 MHz, Gain Index = 255, First-Order TIA with f_{1dB} = 4 MHz, P_{OUT} = -15.1 dBFS at -40°C and +25°C, P_{OUT} = -18.1 dBFS at +110°C

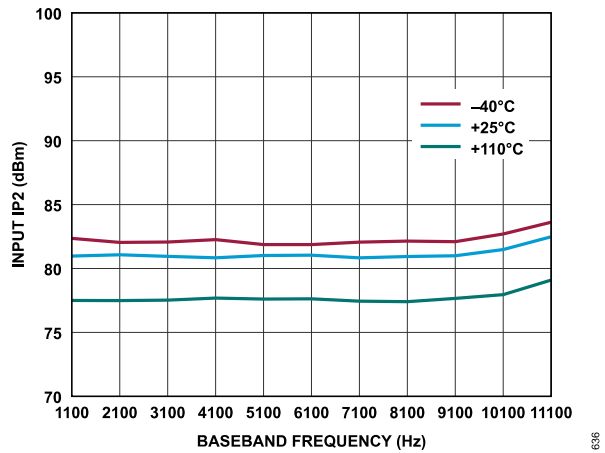


Figure 277. Receiver Input IP2 vs. Baseband Frequency, ADC = Low Power, f_1 = Baseband Frequency + 1 MHz, f_2 = Baseband Frequency + 2 MHz, Gain Index = 255, First-Order TIA with f_{3dB} = 4 MHz, P_{OUT} = -11.6 dBFS

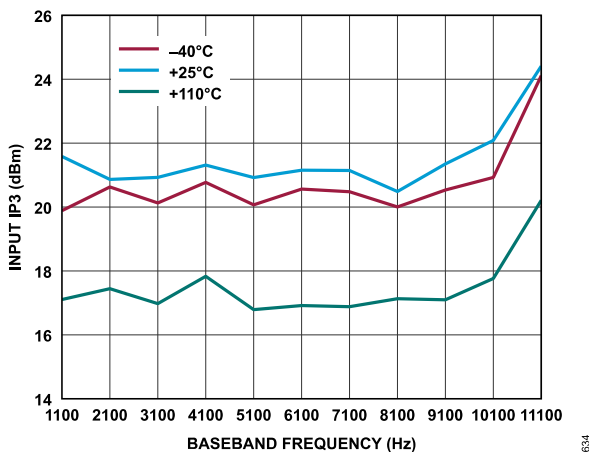


Figure 275. Receiver Input IP3 vs. Baseband Frequency, ADC = Low Power, f_1 = Baseband Frequency + 1 MHz, f_2 = Baseband Frequency + 2 MHz, Gain Index = 255, First-Order TIA with f_{1dB} = 4 MHz, P_{OUT} = -15.1 dBFS at -40°C and +25°C, P_{OUT} = -18.1 dBFS at +110°C

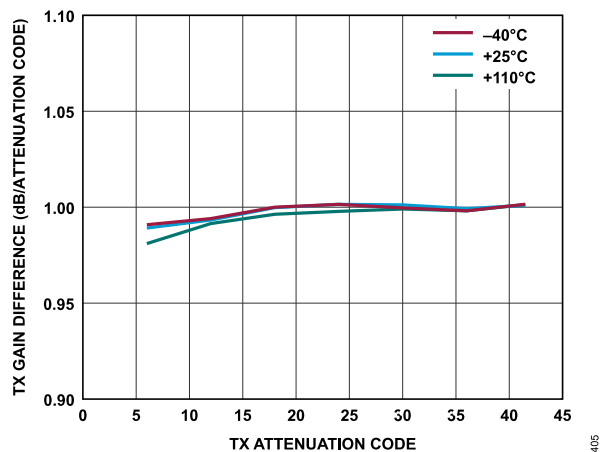


Figure 278. Transmitter Attenuation Delta (Error) vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

TYPICAL PERFORMANCE CHARACTERISTICS

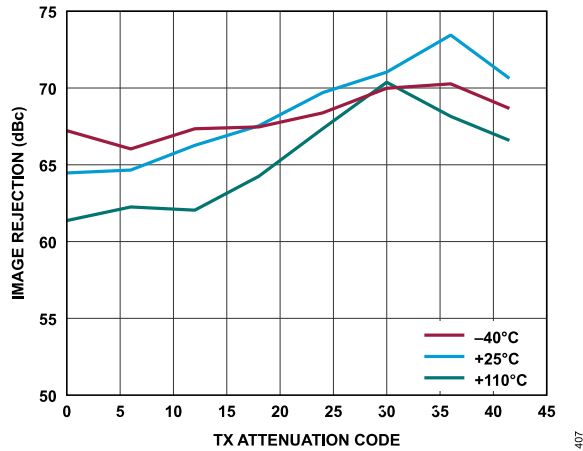


Figure 279. Transmitter Image Rejection vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS, Initialization Calibration Only

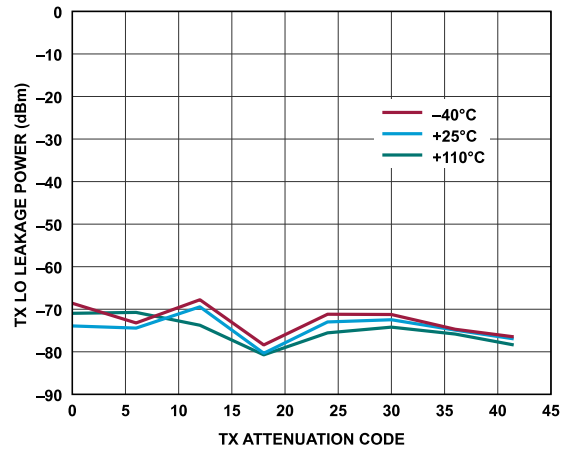


Figure 282. Transmitter LO Leakage Power vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 6 dBFS, Initialization Calibration Only

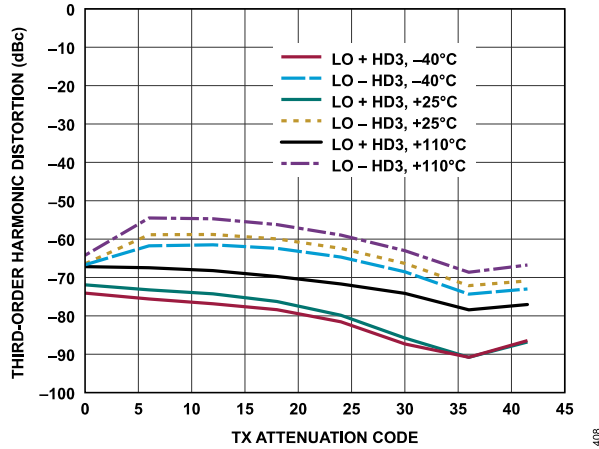


Figure 280. Transmitter Third-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

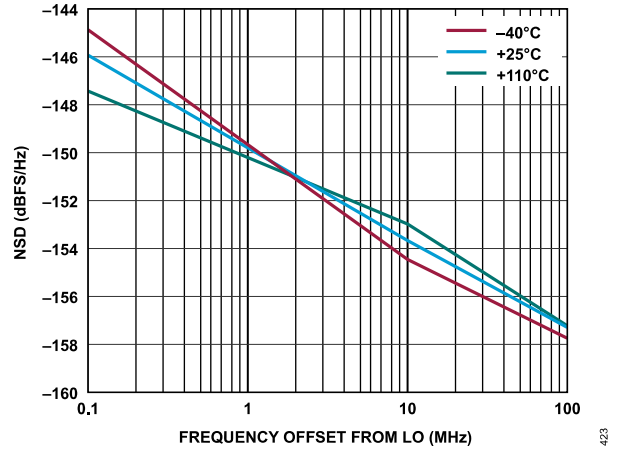


Figure 283. Transmitter NSD vs. Frequency Offset from LO, Baseband Frequency = 2.1 kHz, Transmitter Channel = Channel 1

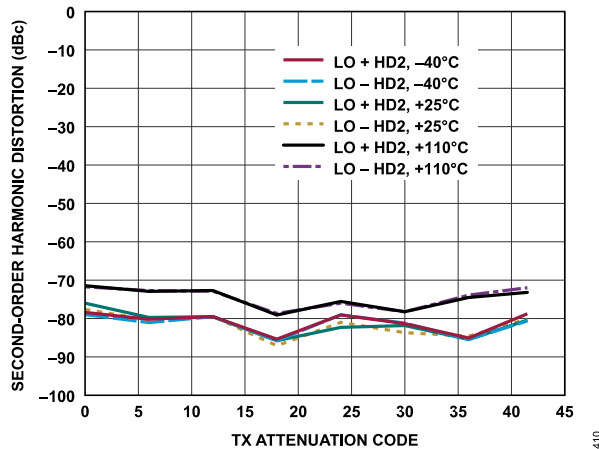


Figure 281. Transmitter HD2 vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

TYPICAL PERFORMANCE CHARACTERISTICS

2400 MHz LO

The temperature settings refer to the die temperature. All LO frequencies set to 2400 MHz, unless otherwise noted.

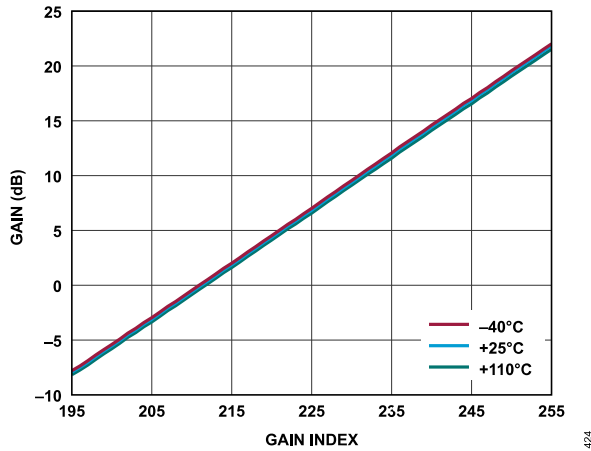


Figure 284. Receiver Absolute Gain (Complex) vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance, $P_{OUT} = -9.6$ dBFS

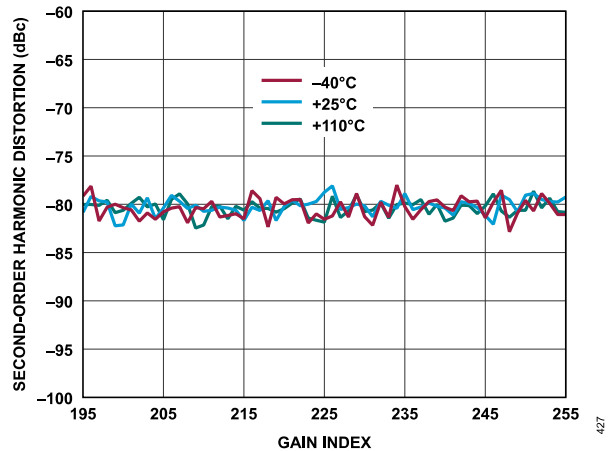


Figure 287. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

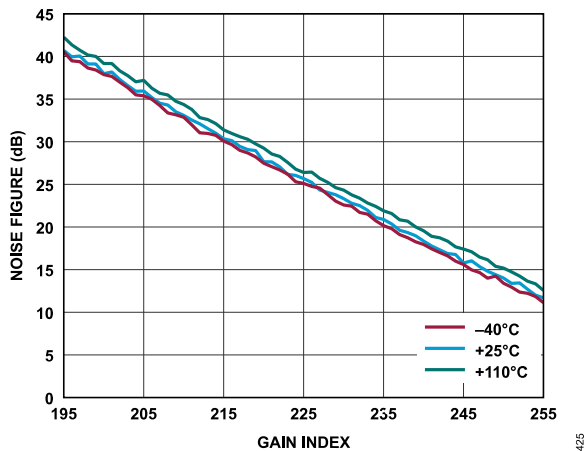


Figure 285. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

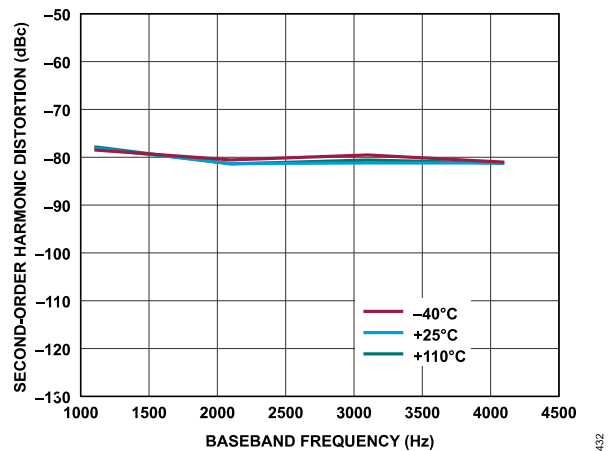


Figure 288. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

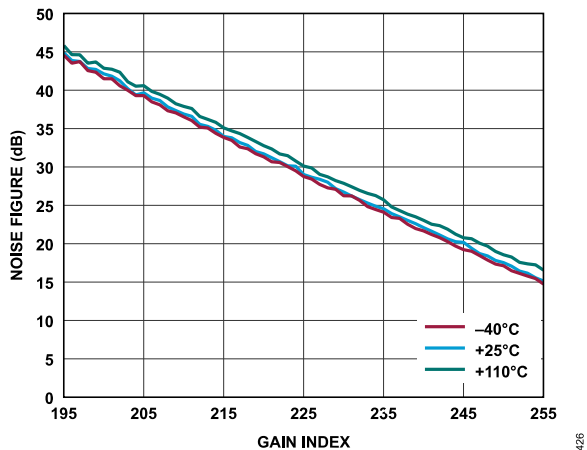


Figure 286. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = Low Power

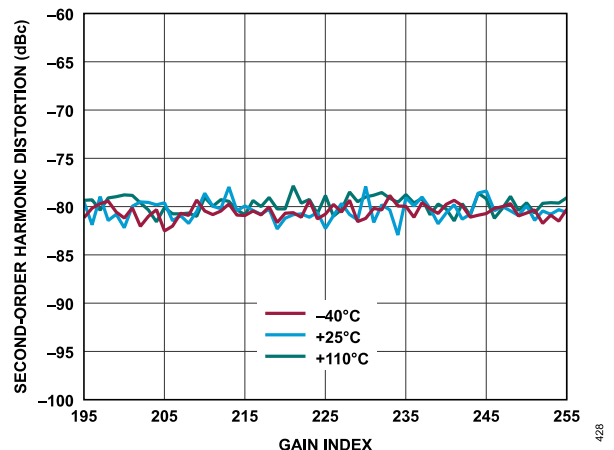


Figure 289. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = Low Power

TYPICAL PERFORMANCE CHARACTERISTICS

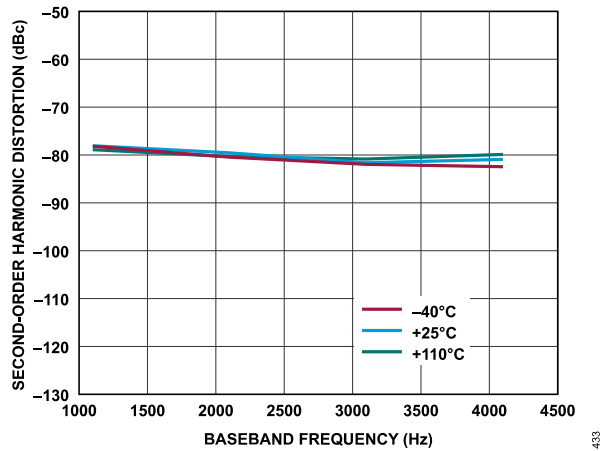


Figure 290. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = Low Power

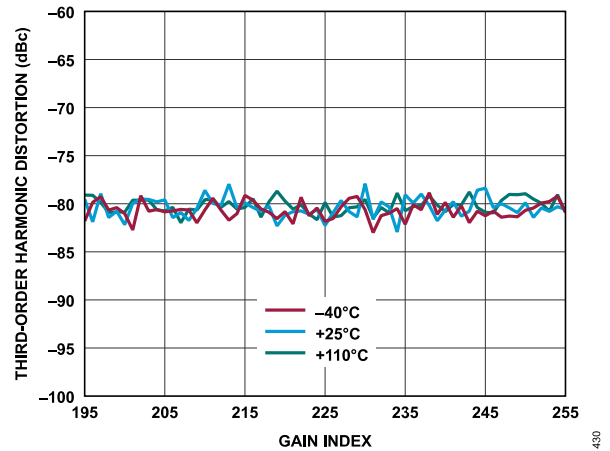


Figure 293. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = Low Power

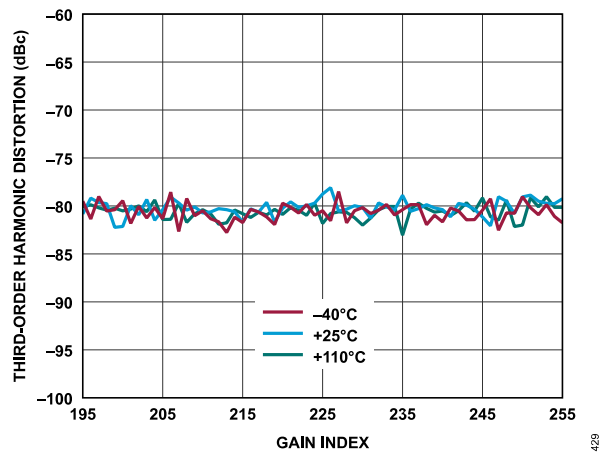


Figure 291. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

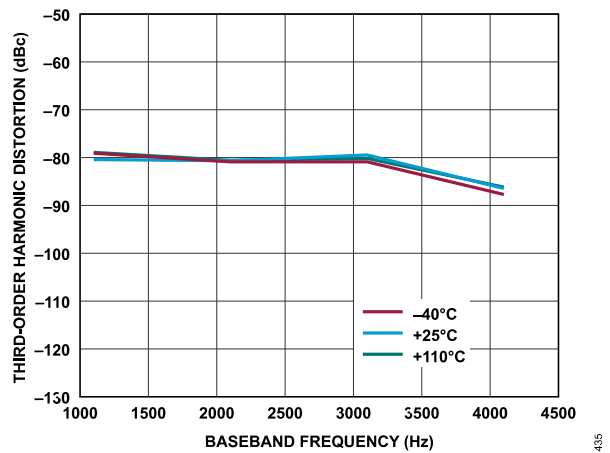


Figure 294. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = Low Power

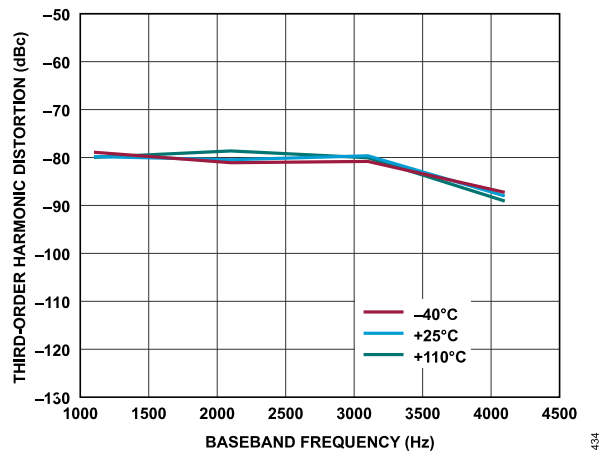


Figure 292. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

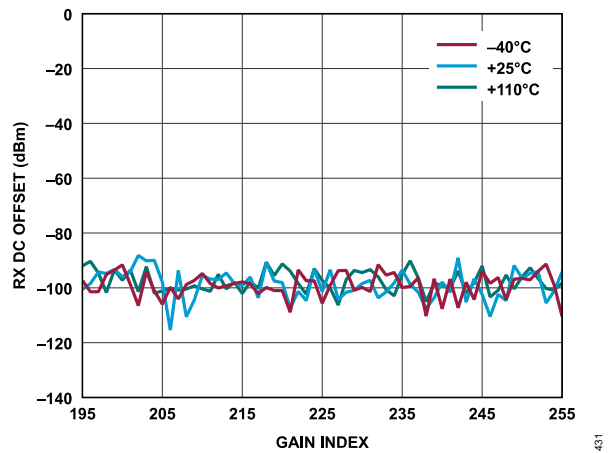


Figure 295. Receiver DC Offset vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

TYPICAL PERFORMANCE CHARACTERISTICS

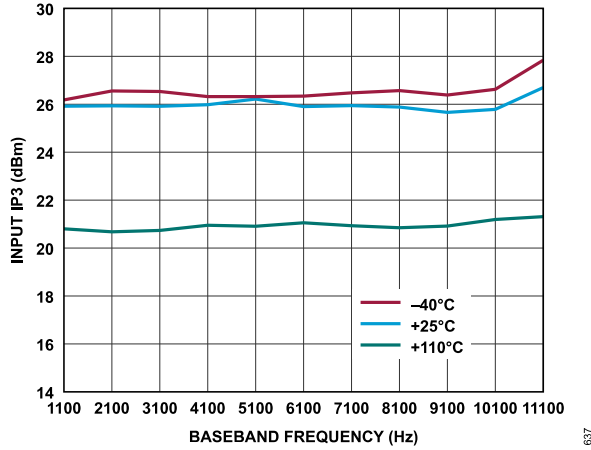


Figure 296. Receiver Input IP3 vs. Baseband Frequency, ADC = High Performance, f_1 = Baseband Frequency + 1 MHz, f_2 = Baseband Frequency + 2 MHz, Gain Index = 255, First-Order TIA with f_{1dB} = 4 MHz, P_{OUT} = -13.6 dBFS at -40°C and +25°C, P_{OUT} = -16.6 dBFS at +110°C

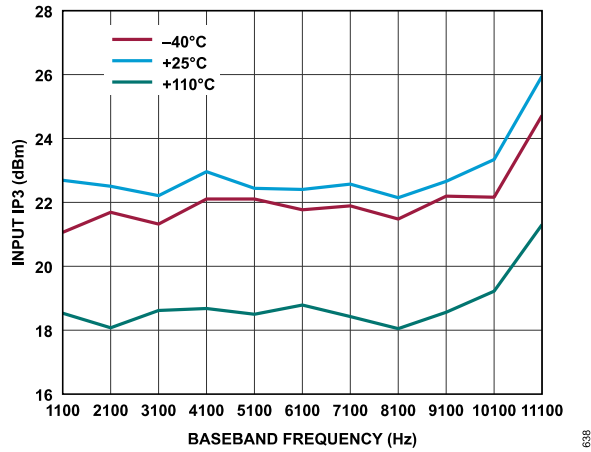


Figure 297. Receiver Input IP3 vs. Baseband Frequency, ADC = Low Power, f_1 = Baseband Frequency + 1 MHz, f_2 = Baseband Frequency + 2 MHz, Gain Index = 255, First-Order TIA with f_{1dB} = 4 MHz, P_{OUT} = -13.6 dBFS at -40°C and +25°C, P_{OUT} = -16.6 dBFS at +110°C

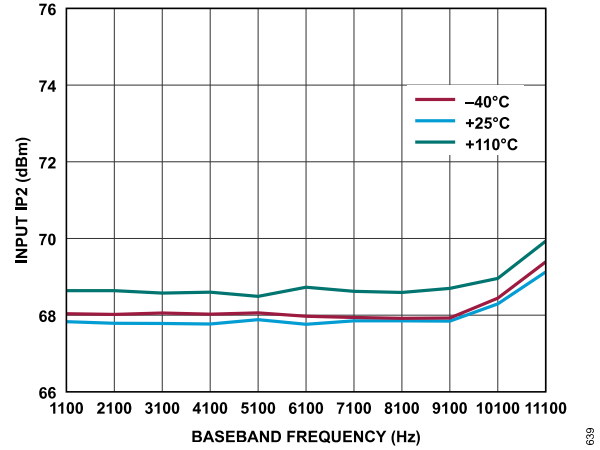


Figure 298. Receiver Input IP2 vs. Baseband Frequency, ADC = High Performance, f_1 = Baseband Frequency + 1 MHz, f_2 = Baseband Frequency + 2 MHz, Gain Index = 255, First-Order TIA with f_{3dB} = 4 MHz, P_{OUT} = -11.6 dBFS

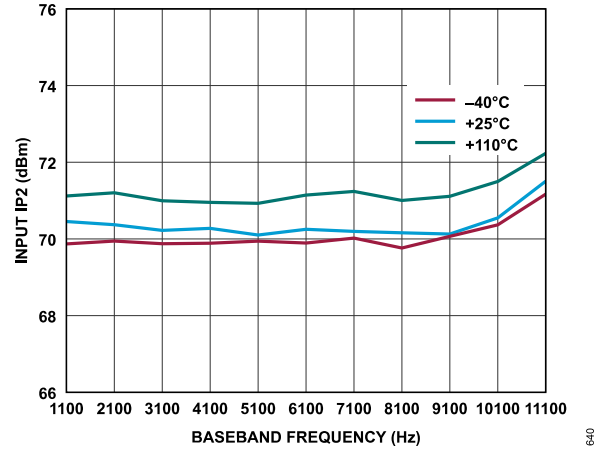


Figure 299. Receiver Input IP2 vs. Baseband Frequency, ADC = Low Power, f_1 = Baseband Frequency + 1 MHz, f_2 = Baseband Frequency + 2 MHz, Gain Index = 255, First-Order TIA with f_{3dB} = 4 MHz, P_{OUT} = -11.6 dBFS

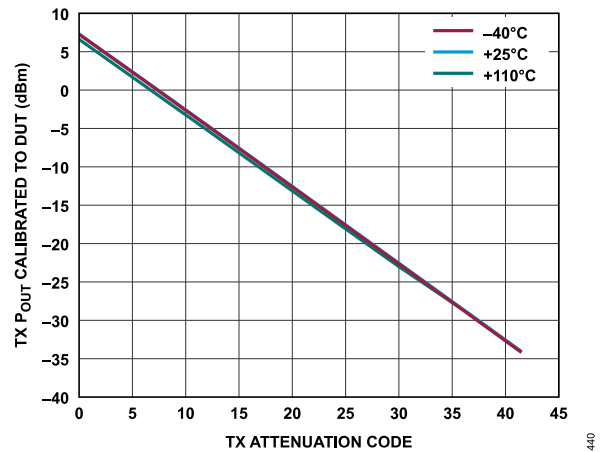


Figure 300. Transmitter Absolute Power vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

TYPICAL PERFORMANCE CHARACTERISTICS

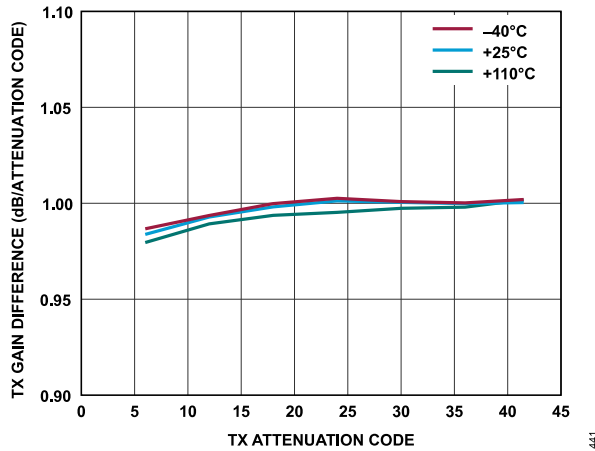


Figure 301. Transmitter Attenuation Delta (Error) vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

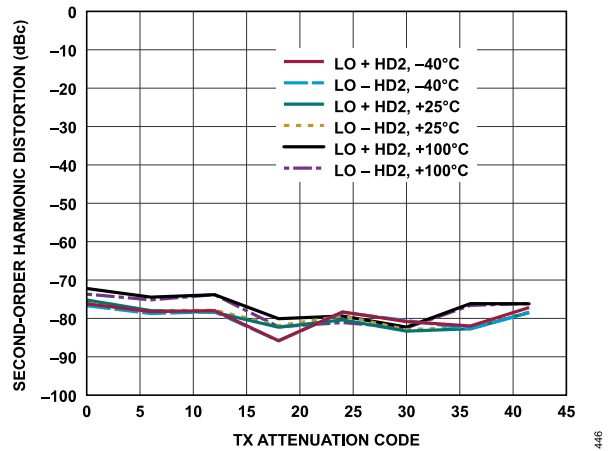


Figure 304. Transmitter Second-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

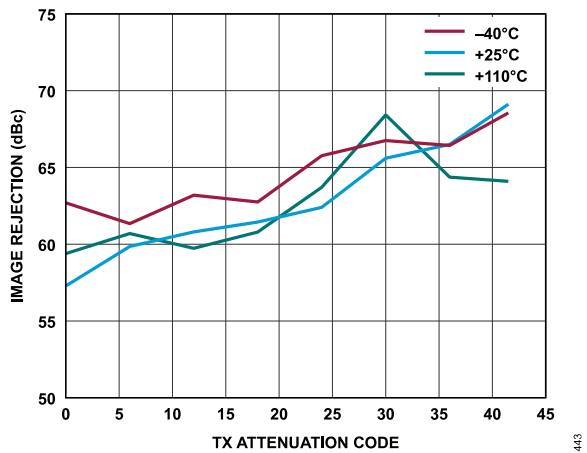


Figure 302. Transmitter Image Rejection vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS, Initialization Calibration Only

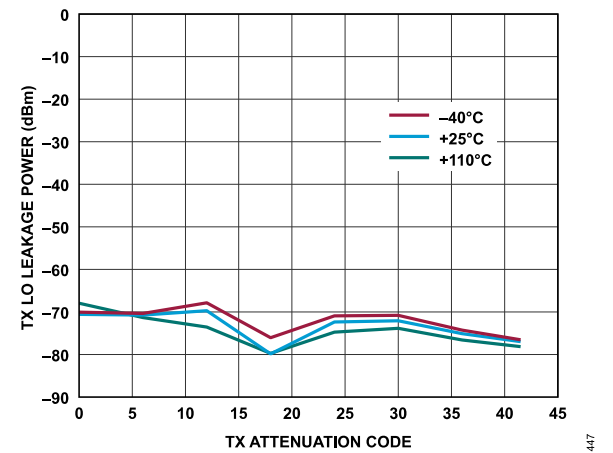


Figure 305. Transmitter LO Leakage Power vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 6 dBFS, Initialization Calibration Only

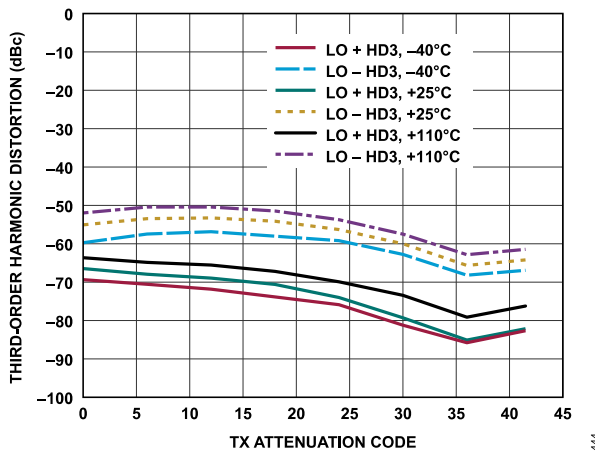


Figure 303. Transmitter Third-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

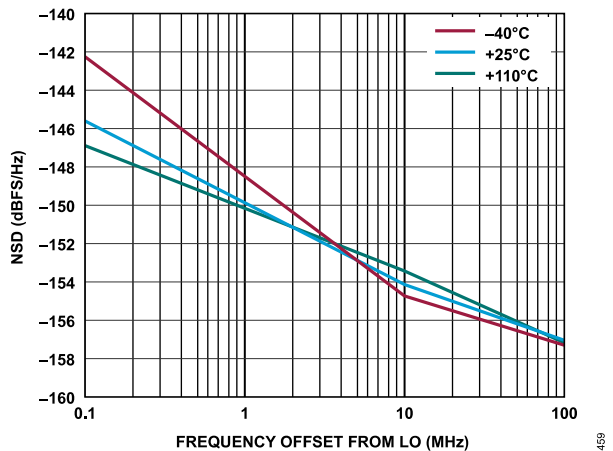


Figure 306. Transmitter NSD vs. Frequency Offset from LO, Baseband Frequency = 2.1 kHz, Transmitter Channel = Channel 1

TYPICAL PERFORMANCE CHARACTERISTICS

3500 MHz LO

The temperature settings refer to the die temperature. All LO frequencies set to 3500 MHz, unless otherwise noted.

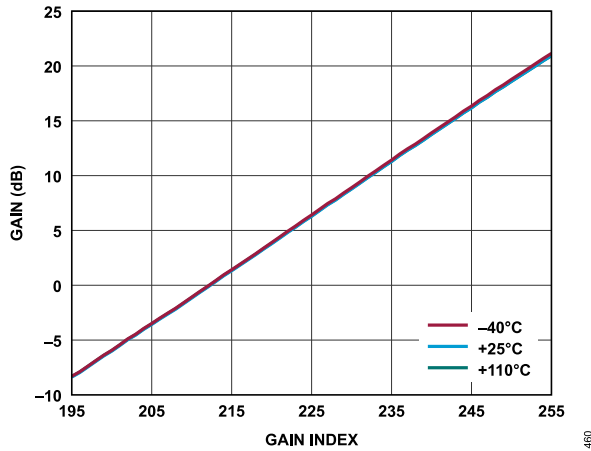


Figure 307. Receiver Absolute Gain (Complex) vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance, $P_{OUT} = -9.6$ dBFS

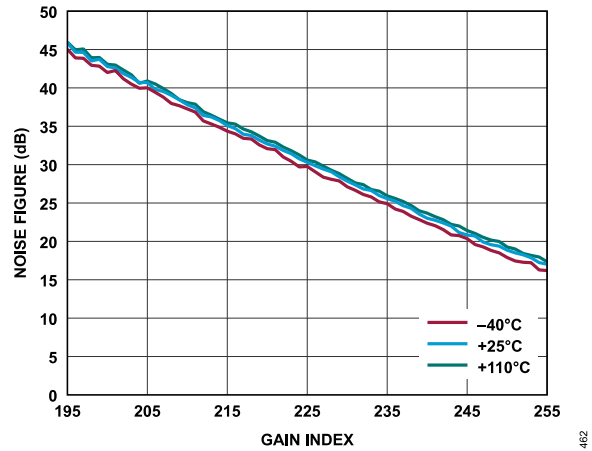


Figure 310. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = Low Power

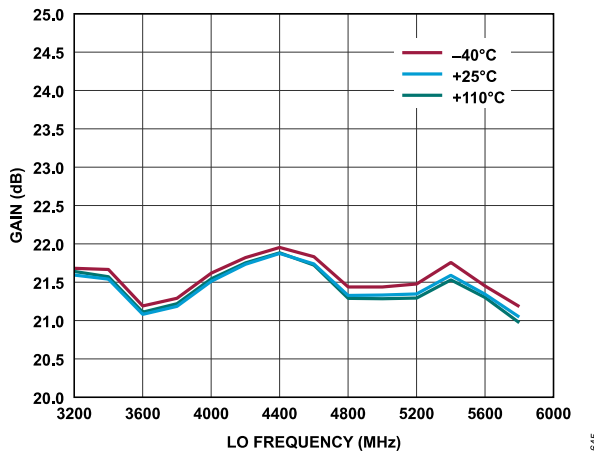


Figure 308. Receiver Absolute Gain (Complex) vs. LO Frequency, Baseband Frequency = 2.1 kHz, ADC = High Performance, $P_{OUT} = -9.6$ dBFS

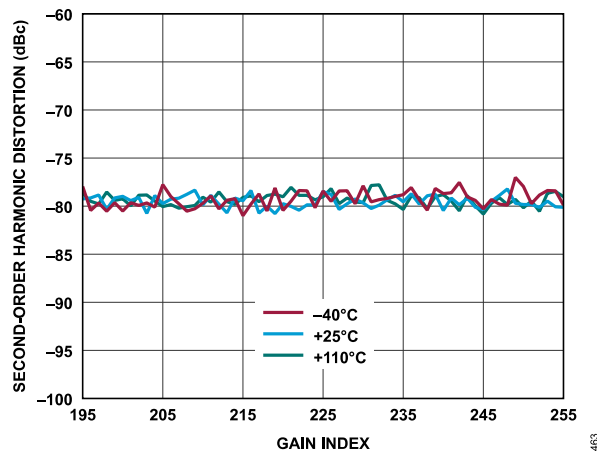


Figure 311. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

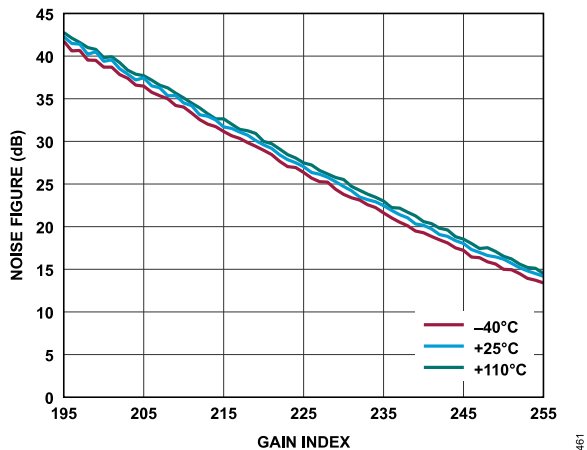


Figure 309. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

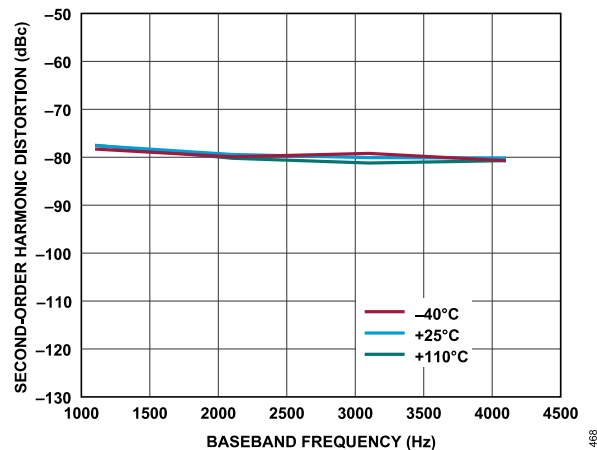


Figure 312. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

TYPICAL PERFORMANCE CHARACTERISTICS

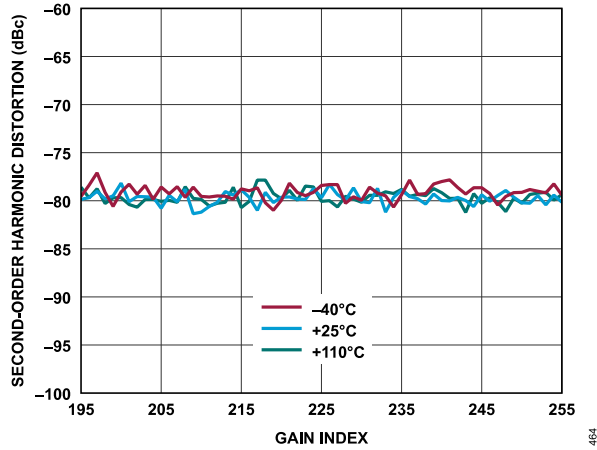


Figure 313. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = Low Power

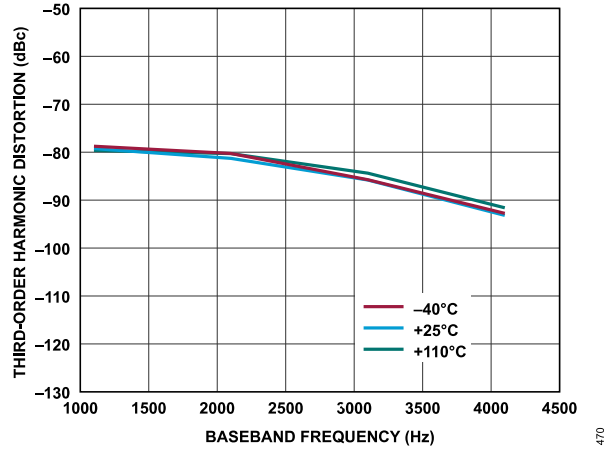


Figure 316. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

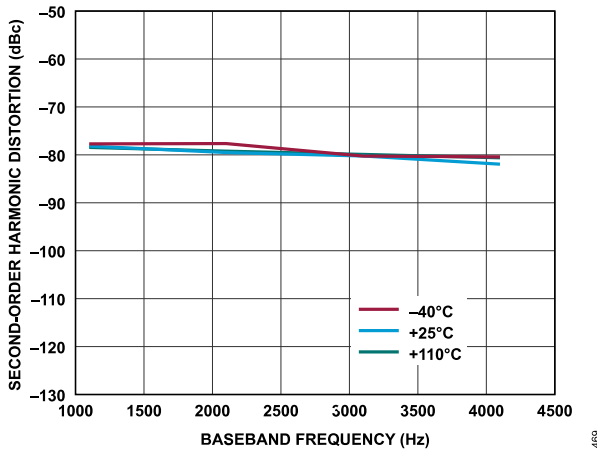


Figure 314. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = Low Power

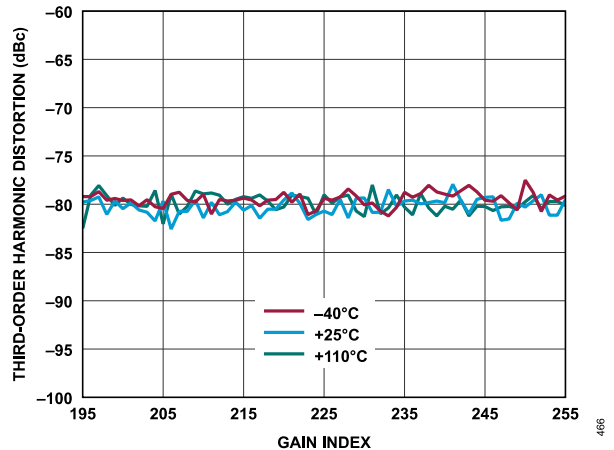


Figure 317. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = Low Power

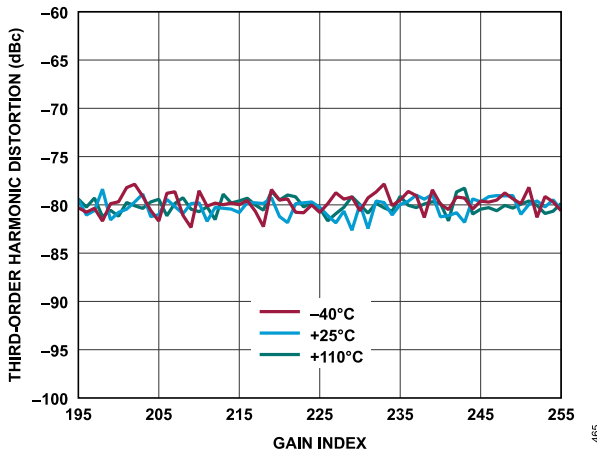


Figure 315. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

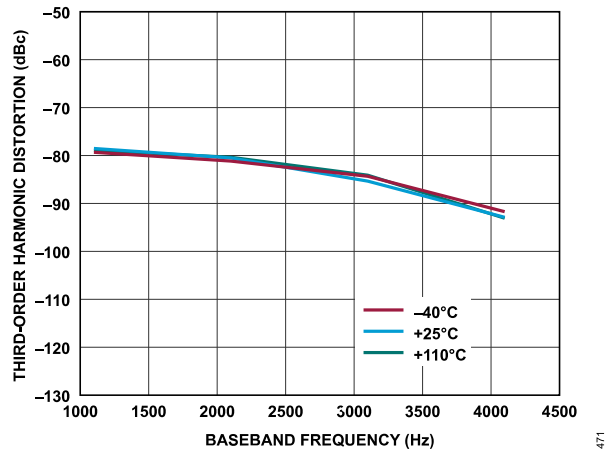


Figure 318. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = Low Power

TYPICAL PERFORMANCE CHARACTERISTICS

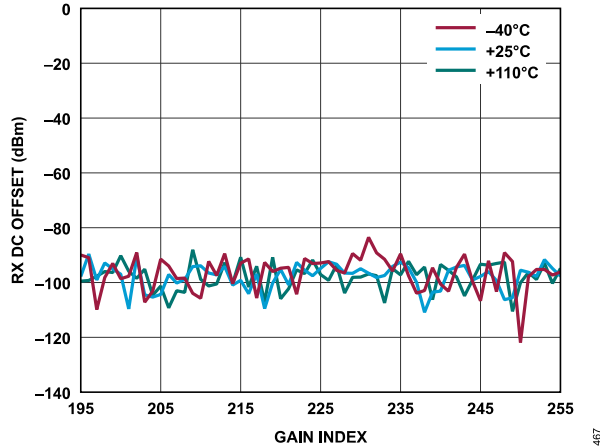


Figure 319. Receiver DC Offset vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

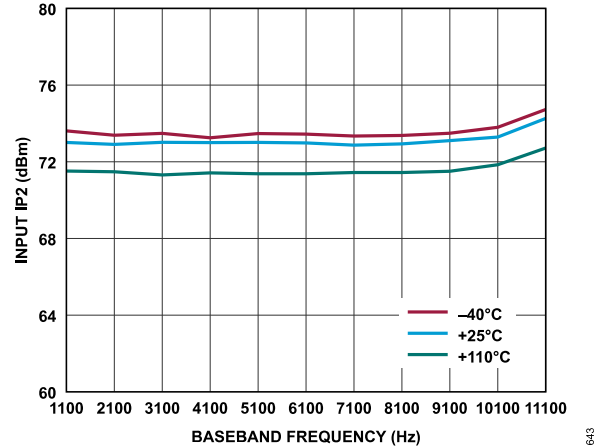


Figure 322. Receiver Input IP2 vs. Baseband Frequency, ADC = High Performance, f_1 = Baseband Frequency + 1 MHz, f_2 = Baseband Frequency + 2 MHz, Gain Index = 255, First-Order TIA with f_{3dB} = 4 MHz, P_{OUT} = -6.6 dBFS

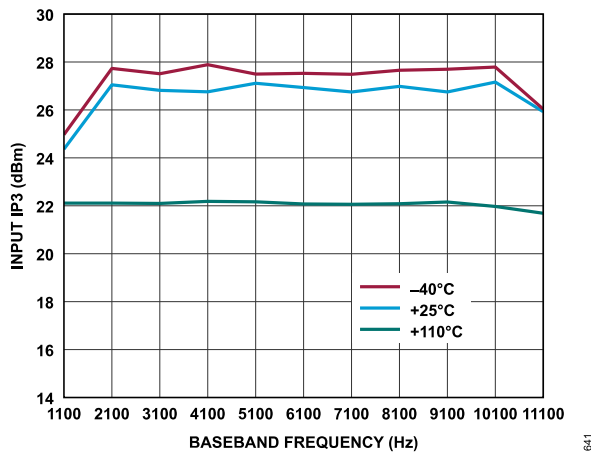


Figure 330. Receiver Input IP3 vs. Baseband Frequency, ADC = High Performance, f_1 = Baseband Frequency + 1 MHz, f_2 = Baseband Frequency + 2 MHz, Gain Index = 255, First-Order TIA with f_{1dB} = 4 MHz, P_{OUT} = -12.6 dBFS at -40°C and +25°C, P_{OUT} = -15.6 dBFS at +110°C

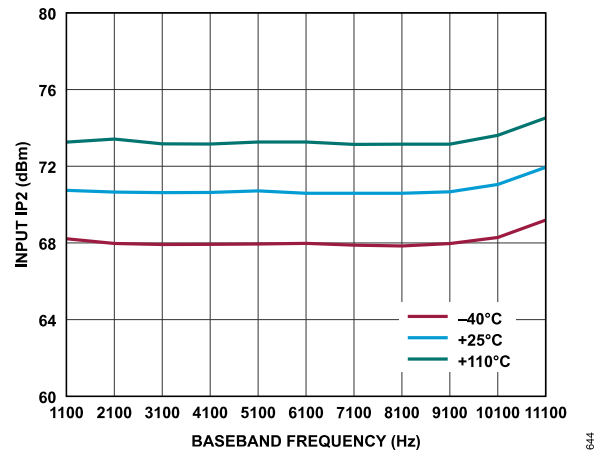


Figure 323. Receiver Input IP2 vs. Baseband Frequency, ADC = Low Power, f_1 = Baseband Frequency + 1 MHz, f_2 = Baseband Frequency + 2 MHz, Gain Index = 255, First-Order TIA with f_{3dB} = 4 MHz, P_{OUT} = -6.6 dBFS

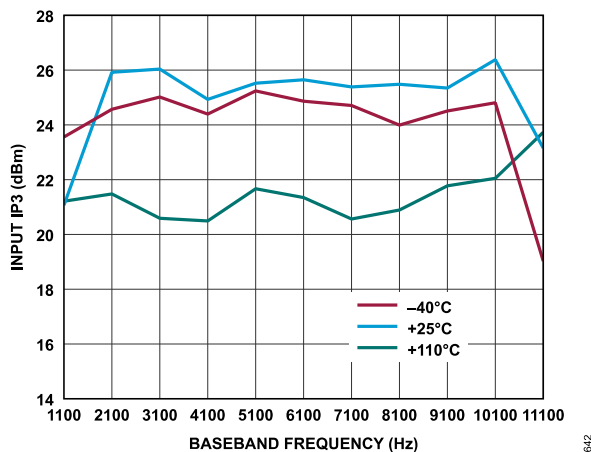


Figure 331. Receiver Input IP3 vs. Baseband Frequency, ADC = Low Power, f_1 = Baseband Frequency + 1 MHz, f_2 = Baseband Frequency + 2 MHz, Gain Index = 255, First-Order TIA with f_{1dB} = 4 MHz, P_{OUT} = -12.6 dBFS at -40°C and +25°C, P_{OUT} = -15.6 dBFS at +110°C

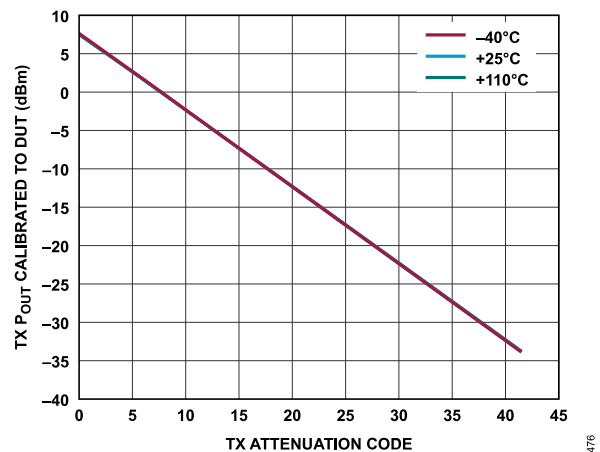


Figure 324. Transmitter Absolute Power vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

TYPICAL PERFORMANCE CHARACTERISTICS

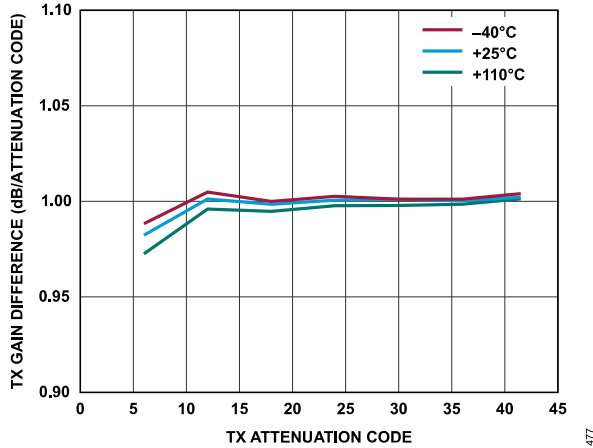


Figure 325. Transmitter Attenuation Delta (Error) vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

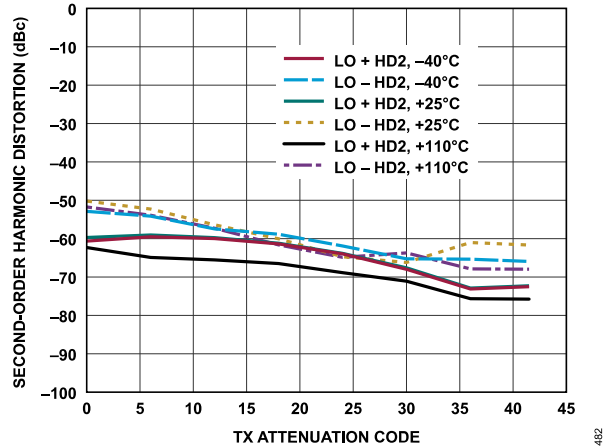


Figure 328. Transmitter Second-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

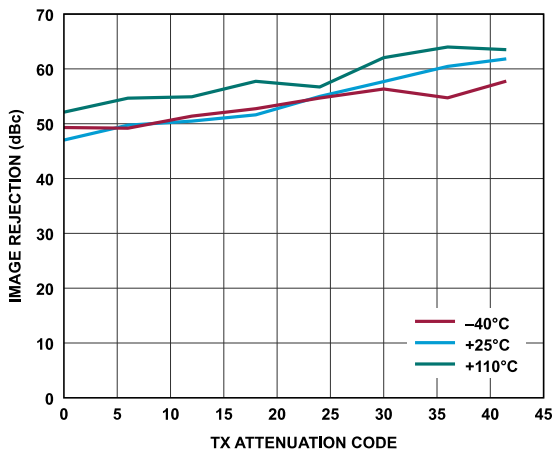


Figure 326. Transmitter Image Rejection vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS, Initialization Calibration Only

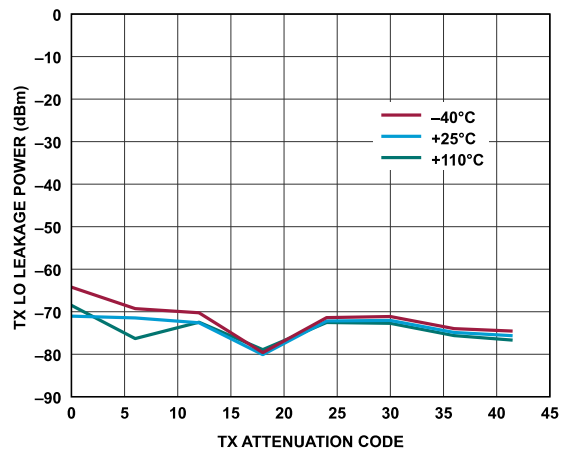


Figure 329. Transmitter LO Leakage Power vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 6 dBFS, Initialization Calibration Only

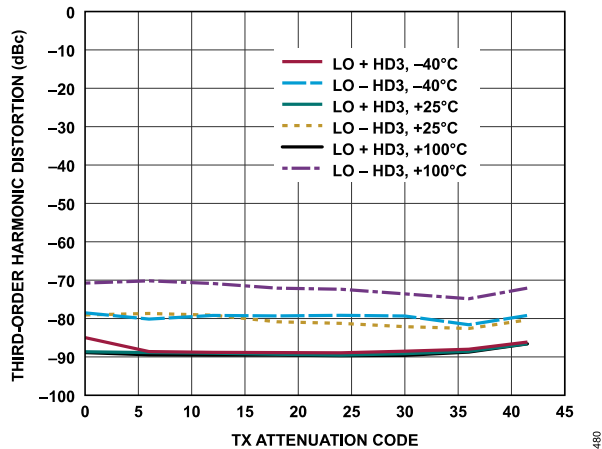


Figure 327. Transmitter Third-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

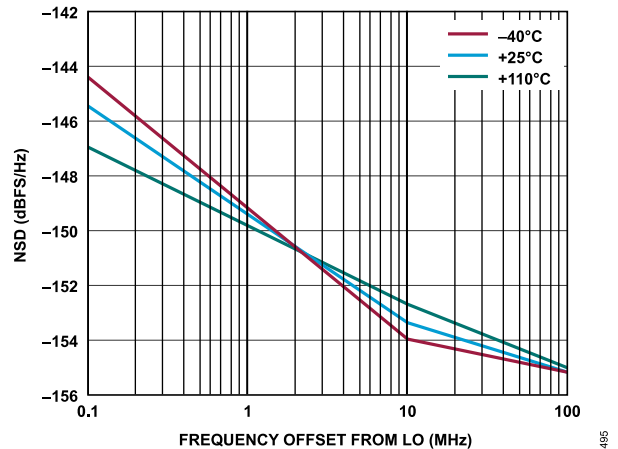


Figure 330. Transmitter NSD vs. Frequency Offset from LO, Baseband Frequency = 2.1 kHz, Transmitter Channel = Channel 1

TYPICAL PERFORMANCE CHARACTERISTICS

5800 MHz LO

The temperature settings refer to the die temperature. All LO frequencies set to 5800 MHz, unless otherwise noted.

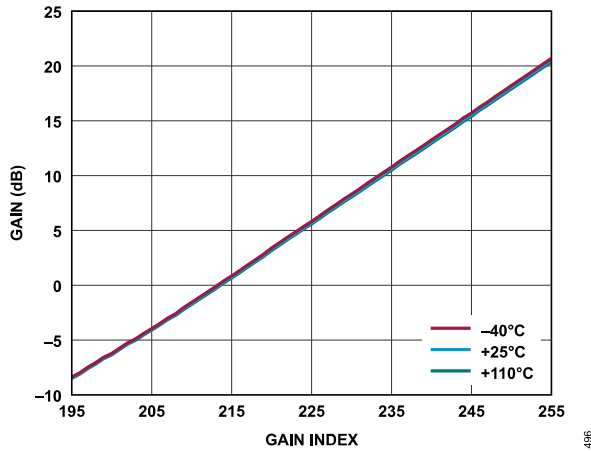


Figure 331. Receiver Absolute Gain (Complex) vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance, $P_{OUT} = -9.6$ dBFS

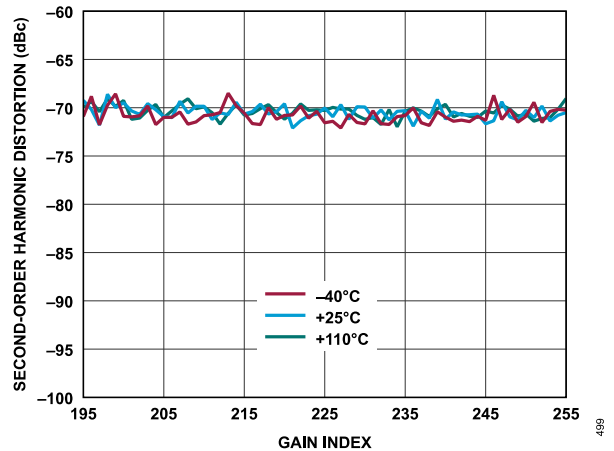


Figure 334. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

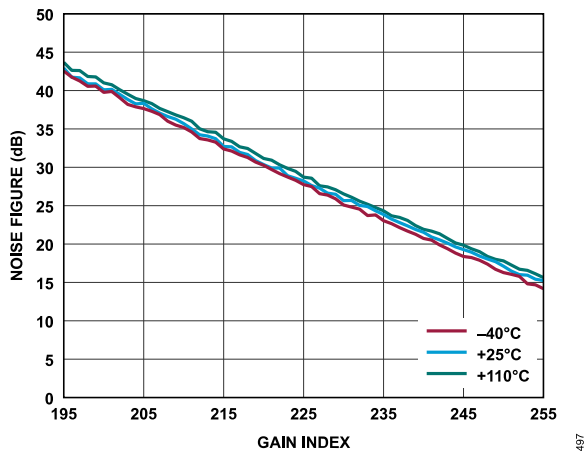


Figure 332. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

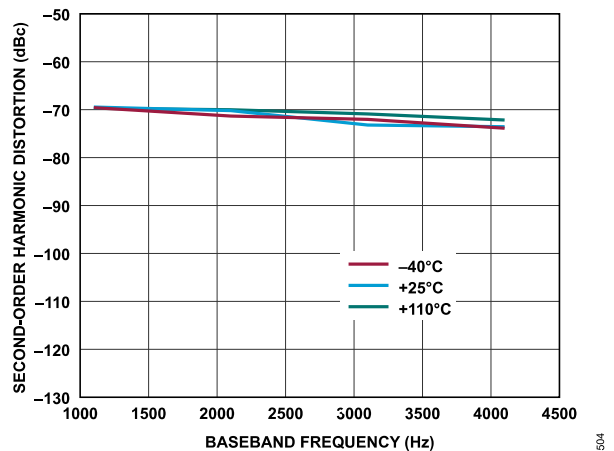


Figure 335. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

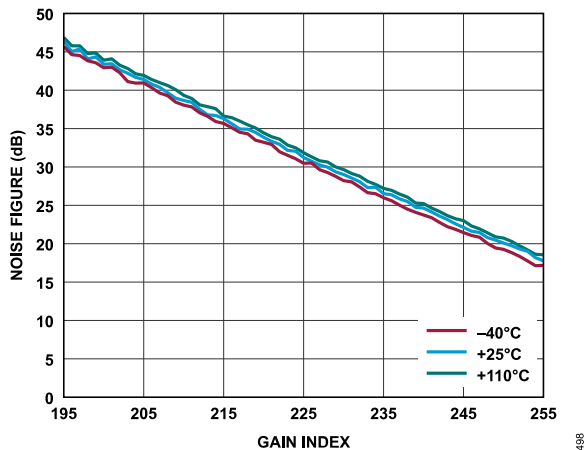


Figure 333. Receiver Noise Figure vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = Low Power

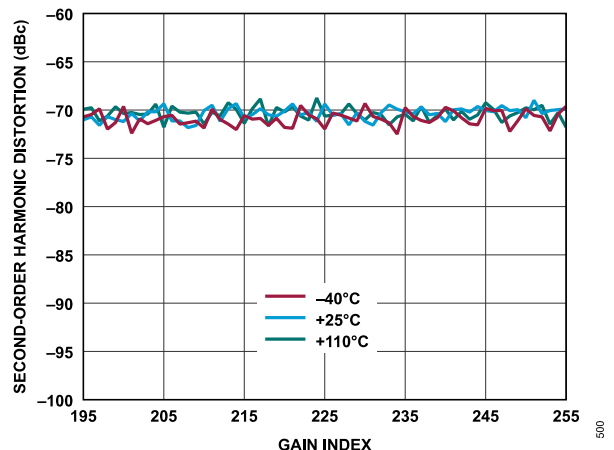


Figure 336. Receiver Second-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = Low Power

TYPICAL PERFORMANCE CHARACTERISTICS

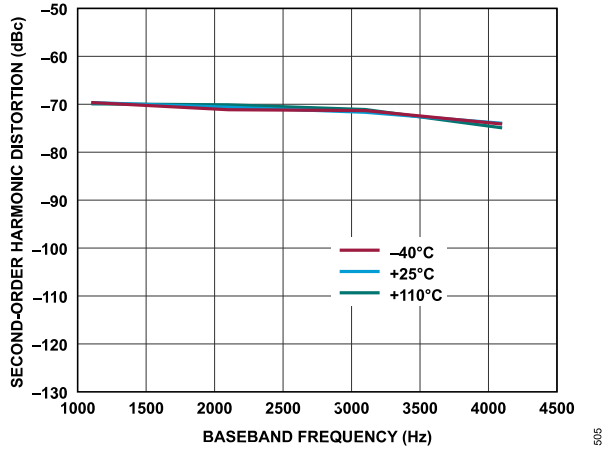


Figure 337. Receiver Second-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = Low Power

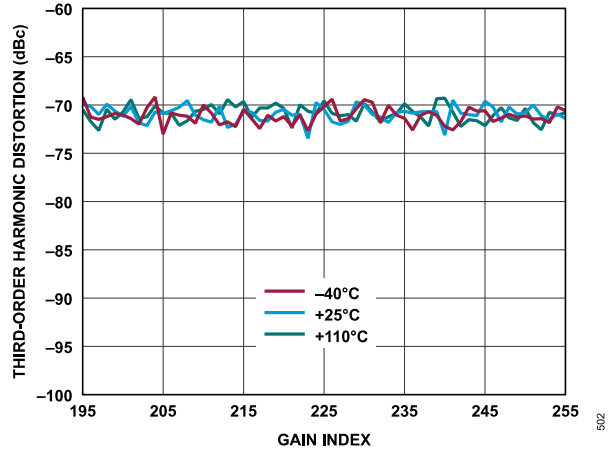


Figure 340. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = Low Power

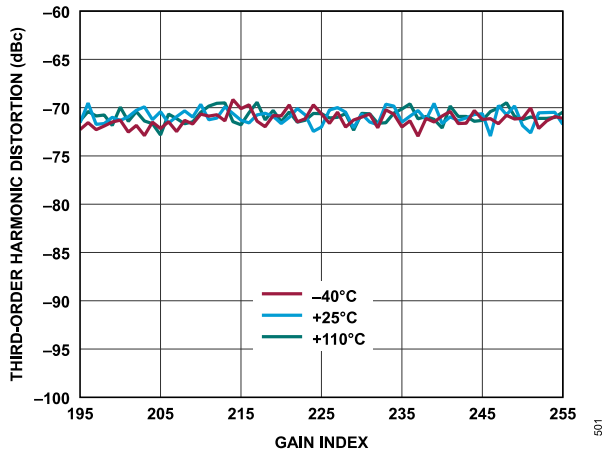


Figure 338. Receiver Third-Order Harmonic Distortion vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

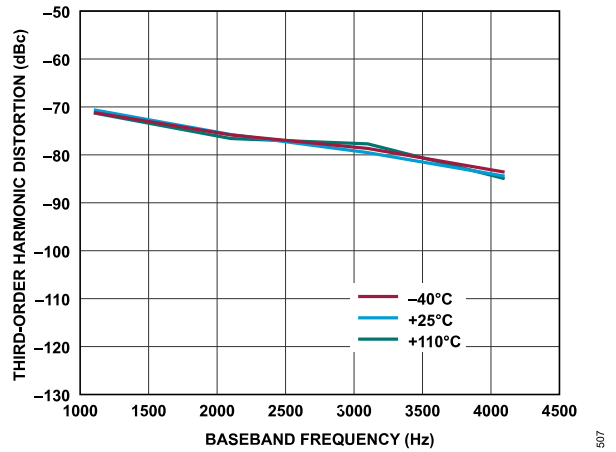


Figure 341. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = Low Power

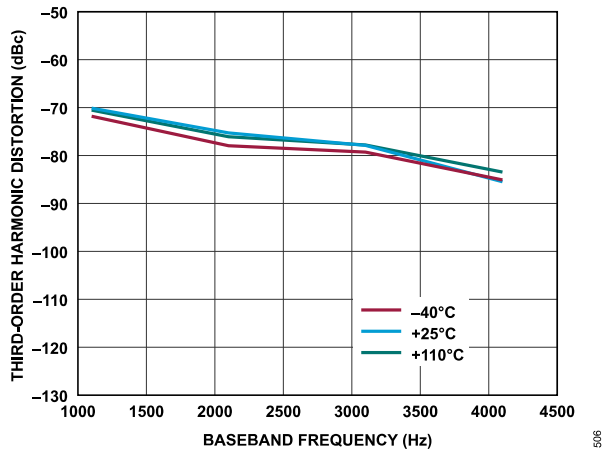


Figure 339. Receiver Third-Order Harmonic Distortion vs. Baseband Frequency, Gain Index = 255, ADC = High Performance

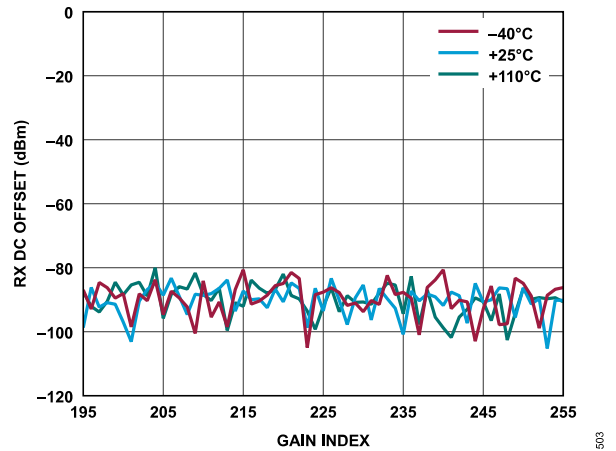


Figure 342. Receiver DC Offset vs. Gain Index, Baseband Frequency = 2.1 kHz, ADC = High Performance

TYPICAL PERFORMANCE CHARACTERISTICS

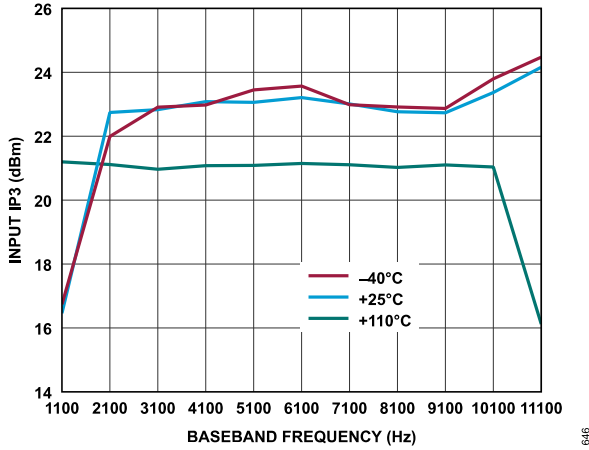


Figure 343. Receiver Input IP3 vs. Baseband Frequency, ADC = High Performance, f_1 = Baseband Frequency + 1 MHz, f_2 = Baseband Frequency + 2 MHz, Gain Index = 255, First-Order TIA with f_{1dB} = 4 MHz, P_{OUT} = -14 dBFS at -40°C and +25°C, P_{OUT} = -12 dBFS at +110°C

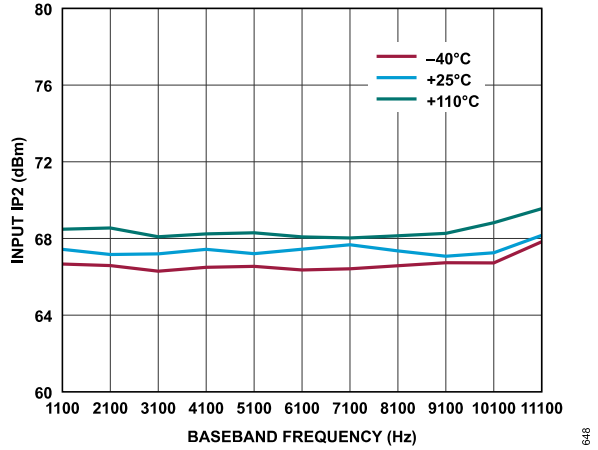


Figure 345. Receiver Input IP2 vs. Baseband Frequency, ADC = High Performance, f_1 = Baseband Frequency + 1 MHz, f_2 = Baseband Frequency + 2 MHz, Gain Index = 255, First-Order TIA with f_{3dB} = 4 MHz, P_{OUT} = -6.6 dBFS

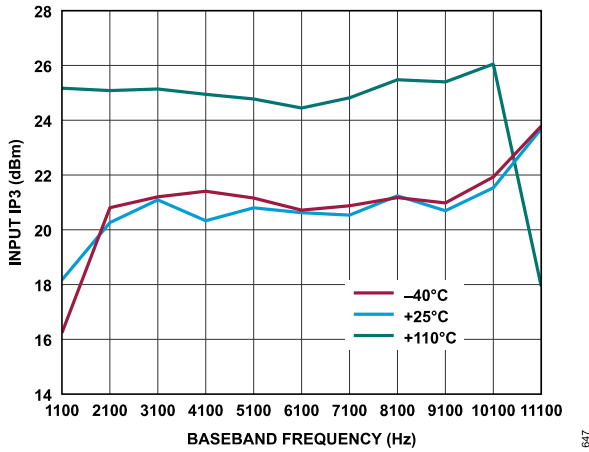


Figure 344. Receiver Input IP3 vs. Baseband Frequency, ADC = Low Power, f_1 = Baseband Frequency + 1 MHz, f_2 = Baseband Frequency + 2 MHz, Gain Index = 255, First-Order TIA with f_{1dB} = 4 MHz, P_{OUT} = -14 dBFS at -40°C and +25°C, P_{OUT} = -12 dBFS at +110°C

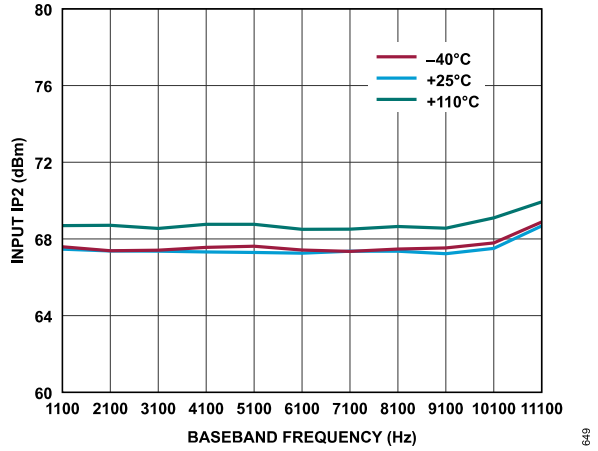


Figure 346. Receiver Input IP2 vs. Baseband Frequency, ADC = Low Power, f_1 = Baseband Frequency + 1 MHz, f_2 = Baseband Frequency + 2 MHz, Gain Index = 255, First-Order TIA with f_{3dB} = 4 MHz, P_{OUT} = -6.6 dBFS

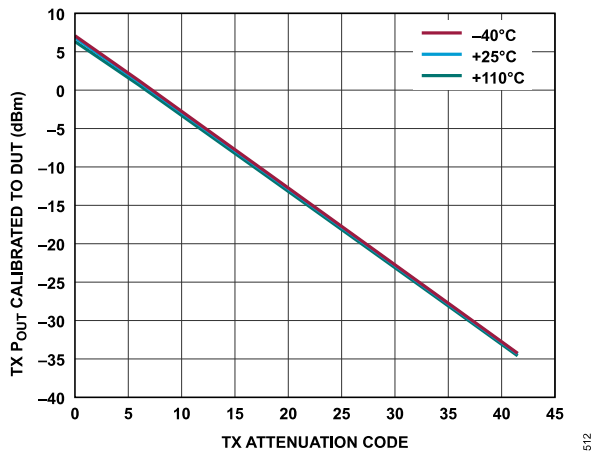


Figure 347. Transmitter Absolute Power vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

TYPICAL PERFORMANCE CHARACTERISTICS

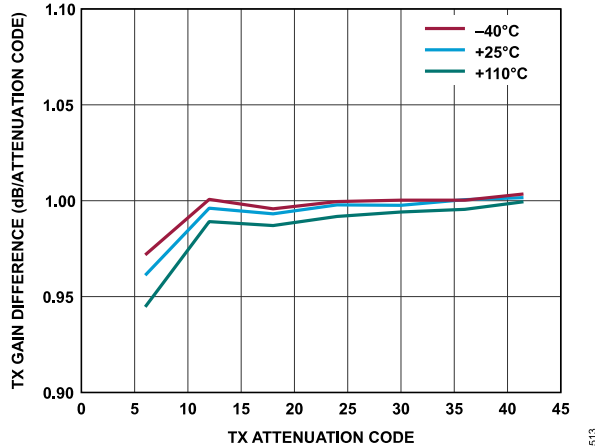


Figure 348. Transmitter Attenuation Delta (Error) vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

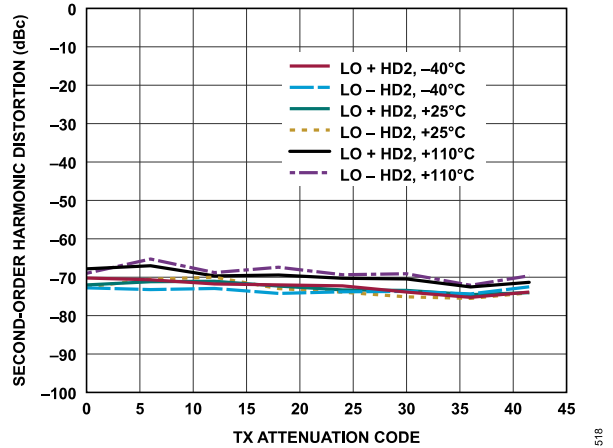


Figure 351. Transmitter Second-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

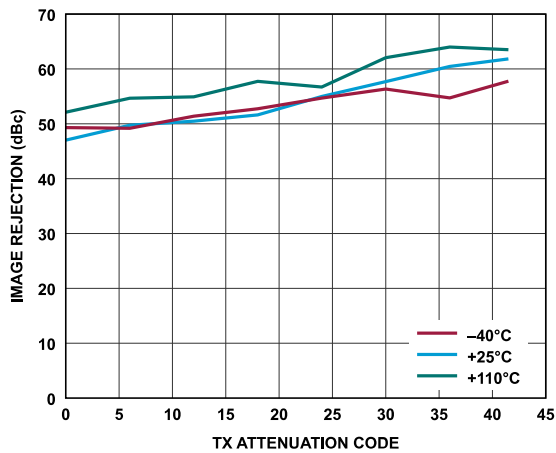


Figure 349. Transmitter Image Rejection vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS, Initialization Calibration Only

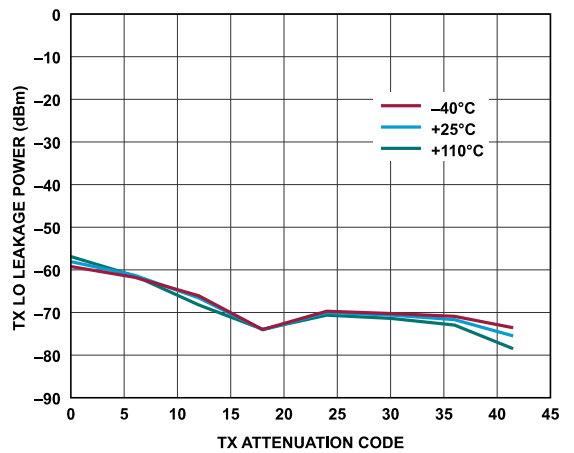


Figure 352. Transmitter LO Leakage Power vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 6 dBFS, Initialization Calibration Only

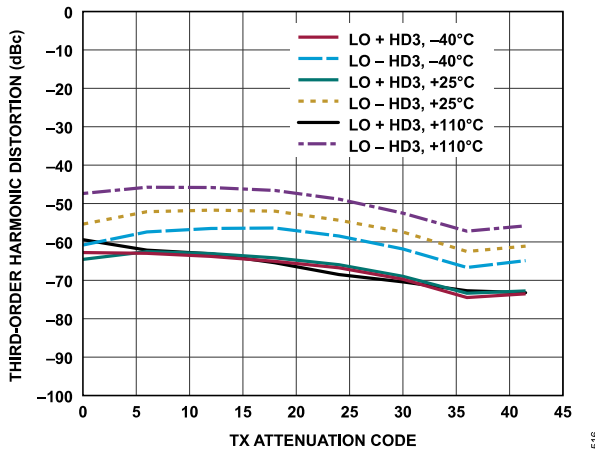


Figure 350. Transmitter Third-Order Harmonic Distortion vs. Transmitter Attenuation Code, Baseband Frequency = 2.1 kHz, Backoff = 0.2 dBFS

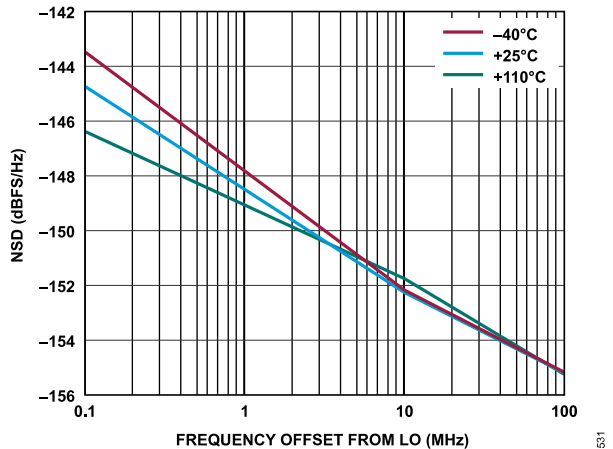


Figure 353. Transmitter NSD vs. Frequency Offset from LO, Baseband Frequency = 2.1 kHz, Transmitter Channel = Channel 1

TYPICAL PERFORMANCE CHARACTERISTICS

PHASE NOISE

PLL bandwidth = 300 kHz. DEV_CLK = 38.4 MHz. Narrow-band or wideband profile with IQ mode. A high performance, low noise, Wenzel type oscillator is used as a reference clock.

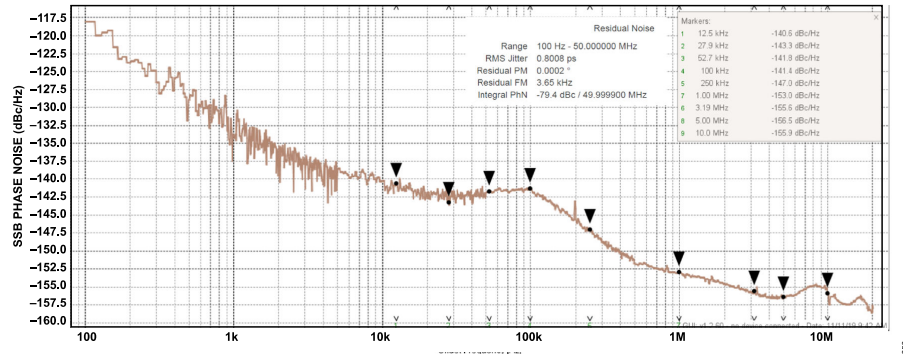


Figure 354. Internal Local Oscillator Phase Noise at 30 MHz LO

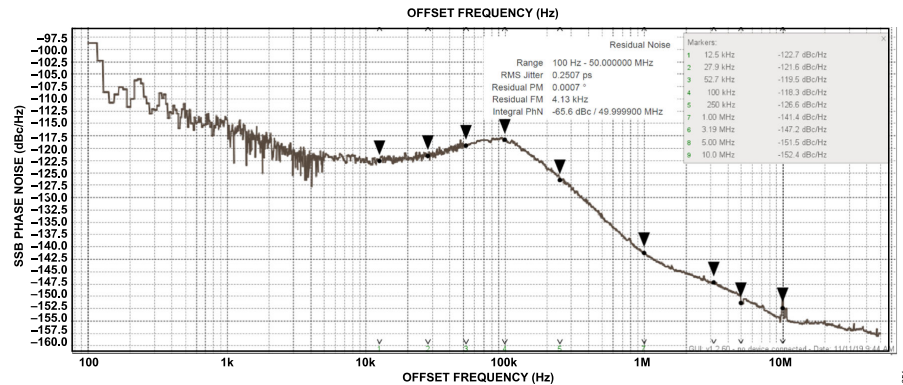


Figure 355. Internal Local Oscillator Phase Noise at 470 MHz LO

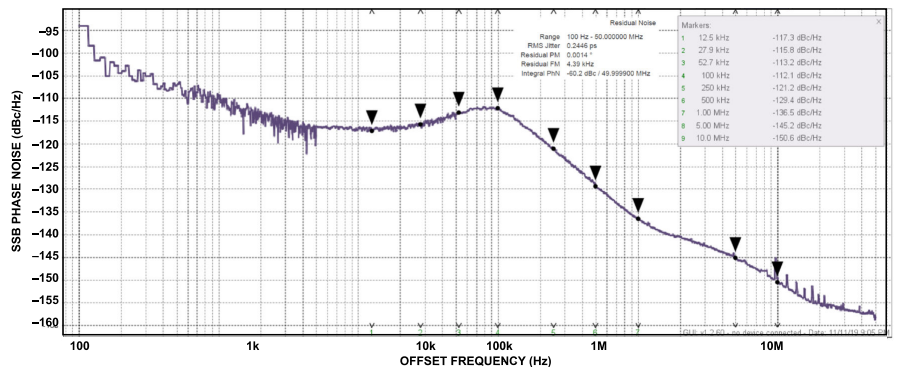


Figure 356. Internal Local Oscillator Phase Noise at 900 MHz LO

TYPICAL PERFORMANCE CHARACTERISTICS

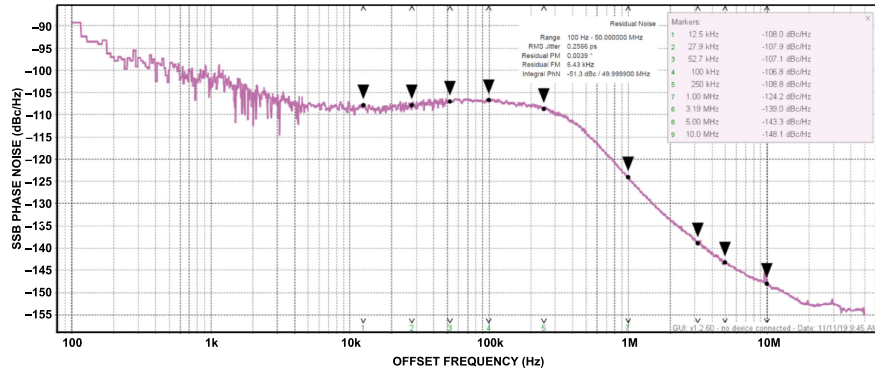


Figure 357. Internal Local Oscillator Phase Noise at 2400 MHz LO

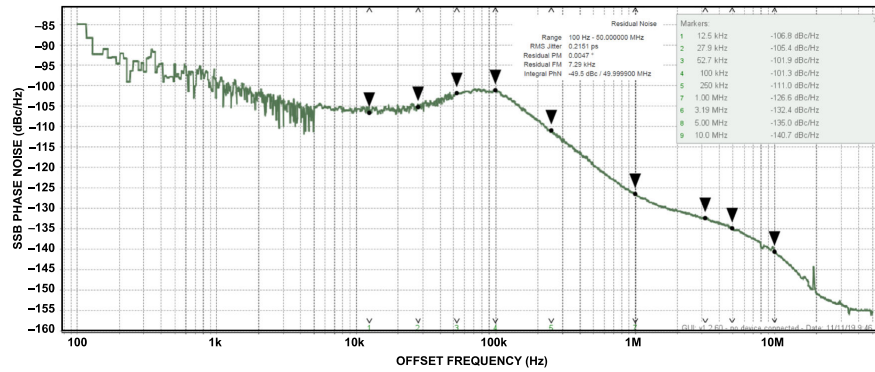


Figure 358. Internal Local Oscillator Phase Noise at 3500 MHz LO

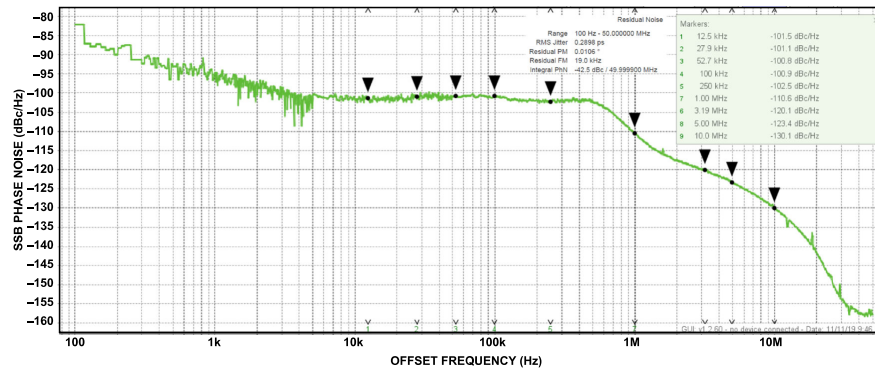


Figure 359. Internal Local Oscillator Phase Noise at 5800 MHz LO

THEORY OF OPERATION

The ADRV9002 is a highly integrated RF transceiver that can be configured for a wide range of applications. The device integrates all RF, mixed-signal, and digital blocks necessary to provide transmit and receive functions in a single device. Programmability allows the two receiver channels and two transmitter channels to be used in TDD and FDD systems for mobile radio and cellular standards.

The ADRV9002 contains serial interface links that consist of LVDS and a CMOS synchronous serial interface (CSSI). Both receiver and transmitter channels provide a low pin count and reliable data interface to a field-programmable gate array (FPGA) or other integrated baseband solutions.

The ADRV9002 provides self calibration for dc offset, LO leakage, and QEC using an integrated microcontroller core to maintain a high performance level under varying temperatures and input signal conditions. Firmware is supplied with the device to schedule all calibrations with no user interaction.

TRANSMITTER

The ADRV9002 uses a direct conversion transmitter architecture that consists of two identical and independently controlled channels

that provide all digital processing, mixed signals, PLLs, and RF blocks necessary to implement a direct conversion system. Refer to [Figure 360](#) for the transmitter data path overview.

The ADRV9002 has an optional, fully programmable, 128-tap FIR. The FIR output is sent to a series of interpolation filters that provide additional filtering and data rate interpolation prior to reaching the DAC. Each DAC has an adjustable sample rate and is linear up to full scale.

The DAC output produces baseband analog signals. The I and Q signals are first filtered to remove sampling artifacts and then fed to the upconversion mixers. At the mixer stage, the I and Q signals are recombined and modulated onto the carrier frequency for transmission to the output stage. Each transmit chain provides a wide attenuation adjustment range with fine granularity to help designers optimize the signal-to-noise ratio (SNR).

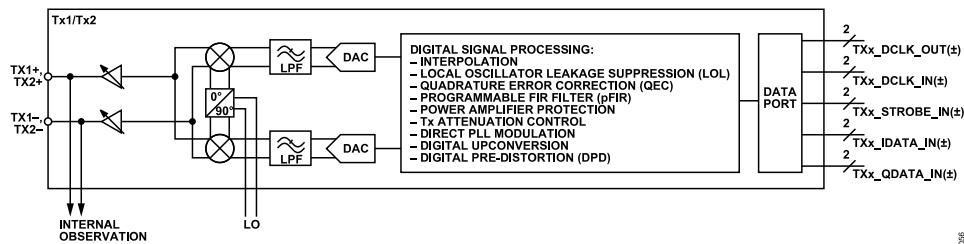


Figure 360. Transmitter Architecture

THEORY OF OPERATION

RECEIVER

Figure 361 shows a simplified block diagram of the ADRV9002 receiver. It is a fully integrated, direct conversion, low IF receiver signal chain. The receiver subsystem consists of a resistive input network for gain control followed by a current mode passive mixer. The output current of the mixer is converted to a voltage by a transimpedance amplifier and then digitized. There are two sets of ADCs, a high performance Σ - Δ ADC and a low power ADC. The digital baseband that provides the required filtering and decimation follows these ADCs.

There are two RF inputs for each receiver to match different bands in one reference design. The mixer architecture is linear and inherently wideband, which facilitates impedance matching. The differential input impedance of the receiver inputs is 100 Ω .

To achieve gain control, a programmed gain index map is implemented. This gain map distributes attenuation among the various receiver blocks for optimal performance at each power level. The gain range is 34 dB. Additional support is available for both automatic and manual gain control modes.

The receive LPFs can be reconfigured to help provide antialias filtering and improve out of band blockers. The ADRV9002 is a wideband architecture transceiver that relies on the ADC high dynamic range to receive signals and interference at the same time. Filtering provided by the receive LPF attenuates ADC alias images. The receive LPF characteristic is flat and not intended to provide rejection of close in blockers. The baseband filter supports a baseband bandwidth from 5 MHz to 50 MHz.

The receiver includes two ADC pairs. One pair consists of high performance Σ - Δ ADCs to provide maximum interferer tolerance, and the second pair consists of ADCs for significant power reduction. The extra pair of ADCs allow a smart trade-off between power and performance.

The ADC output can be conditioned further by a series of decimation filters and a fully programmable, 128-tap FIR filter with additional decimation settings. The sample rate of each digital filter block automatically adjusts with each change of the decimation factors to produce the desired output data rate.

For standards that demand low phase noise performance, the ADRV9002 can operate in low IF mode. The ADRV9002 can receive signals offset from the carrier, as with an IF downconversion scheme. A digital NCO and mixer that follow the analog receive path can downconvert the IF signal to baseband. Downconverting the signal to baseband allows a lower sample rate on the data bus. The ADRV9002 makes no assumptions about high-side or low-side injection.

Monitor Mode

The ADRV9002 receiver signal chain can be configured to monitor the radio channel signal level in duty cycle detection and sleep fashion. Monitor mode allows the digital baseband processor to power down until the ADRV9002 detects a signal. Monitor mode provides overall system power saving. The timing of detection and sleep mode is fully programmable. Alternatively, the ADRV9002 can be under full control of the baseband processor during monitor mode.

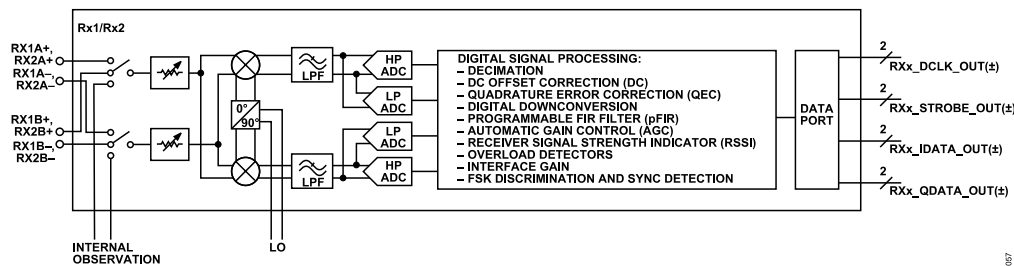


Figure 361. Receiver Architecture

THEORY OF OPERATION

DPD

The ADRV9002 provides a fully integrated DPD function that alters the digital waveform to compensate for nonlinearities in the power amplifier response, which linearizes the output of the power amplifier of the transmit system. The internal DPD block is optimized for both narrow-band and wideband signals. The DPD actuator and coefficient calculation engine are both integrated. This functionality uses the receive channel to monitor the output of the power amplifier and calculates the appropriate predistortion to linearize the output. The integrated DPD capability allows the system to drive the power amplifier closer to saturation, enabling a higher efficiency power amplifier while maintaining linearity.

Receiver as an Observation Receiver

In FDD type applications where only one receiver is used or in the TDD type applications during transmitter time slots, unused receiver inputs can be used to perform transmitter observation. The observation receiver operates in a similar manner to the main receivers.

Use the observation receiver channel to perform the following:

- ▶ Monitor the transmitter channels and implement transmitter local oscillator leakage (LOL) correction and transmitter QEC.
- ▶ Monitor signal levels after the power amplifier output. This data can be used by a fully integrated low power DPD block. The integrated DPD is optimized for both narrow-band and wideband signals and enables linearization of high efficiency power amplifiers.
- ▶ Monitor signal levels after the power amplifier output for further data processing in the external baseband processor.

In cases where the observation receiver path is used for DPD operation, there is a limit to the maximum bandwidth of the transmitter signal the DPD can support. For example, if the DPD observation factor is $5\times$, the transmitter signal bandwidth is limited to $1/5$ of the DPD observation bandwidth. When using the ADRV9002 internal DPD block, the largest transmitter bandwidth that the internal DPD can support is 20 MHz because of the largest internal DPD observation bandwidth of 100 MHz. When external DPD is used, the largest DPD observation bandwidth is limited by the transmitter and observation receiver RF bandwidth. 40 MHz is the largest RF bandwidth that can be received and sent over the digital data port to the baseband processor, which implies that 8 MHz represents the largest transmitter bandwidth that the DPD implemented externally to the ADRV9002 can support.

CLOCK INPUT

The reference clock inputs provide a low frequency clock from which all internal ADRV9002 clocks are derived. The ADRV9002 offers multiple reference input clocking options. The reference input clock pins on the device are labeled DEV_CLK_IN±.

For optimal performance, drive the reference clock differentially via an external source or from an external crystal. If a differential input clock is provided, the clock signal must be ac-coupled with the input range limited from 10 MHz to 1 GHz. The ADRV9002 can also accept an external crystal (XTAL) as a clock source. The frequency range of the supported crystal is between 20 MHz to 80 MHz. The external crystal connection must be dc-coupled.

If a differential clock is not available, a single-ended, ac-coupled, 1 V p-p (maximum) CMOS signal can be applied to the DEV_CLK_IN+ pin with the DEV_CLK_IN- pin unconnected. The maximum clock frequency in this mode is limited to 80 MHz.

SYNTHESIZERS

The ADRV9002 offers two distinct PLL paths, an RF PLL for the high frequency RF path and a baseband PLL for the digital and sampling clocks of the data converters.

RF PLL

The PLL structure in the ADRV9002 is unique in the sense that instead of having one dedicated PLL for the receive data path and a dedicated PLL for the transmit data path, two RF PLLs are in the device and both PLLs can source the receiver, the transmitter, both paths, or neither. This flexibility enables the ADRV9002 to meet various applications that require versatility.

The RF PLL supports the use of both internal and external LO signals. The internal LO is generated by an on-chip VCO, which is tunable over a frequency range of 6.5 GHz to 13 GHz. The output of the VCO is phase-locked to an external reference clock through a fractional-N PLL that is programmable through the API command. The VCO outputs are steered through a combination of frequency dividers to produce in-phase and quadrature phase LO signals in the 30 MHz to 6 GHz frequency range.

Alternatively, an external LO signal can be applied to the external LO inputs of the ADRV9002 to generate the LO signals in quadrature for the RF path. If the external LO path is chosen, the input frequency range is between 60 MHz and 12 GHz.

PLL synthesizers are fractional-N designs that incorporate completely integrated VCOs and loop filters. In TDD mode, LO distribution paths and receive and transmit data paths turn on and off as appropriate for the receive and transmit frames. In FDD mode, the transmit PLL and the receive PLL can be activated simultaneously. These PLLs require no external components. The RF LO generation circuits offer a trade-off between performance and power consumption.

THEORY OF OPERATION

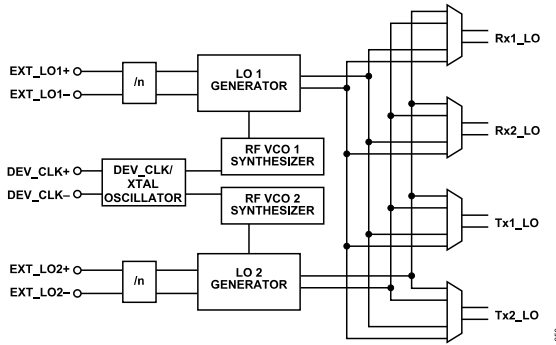


Figure 362. RF LO

The ADRV9002 supports various forms of fast frequency hopping (FFH) with the frequency dwell time and transition time as the main distinguishing factors between these forms. The RF PLL phase noise and the QEC and LOL algorithm performance degrade as a function of decreasing frequency transition times. FFH mode supports hop frequencies that are preloaded at power-up or streamed by the user onto the ADRV9002. Hopping between the frequencies in FFH mode can be triggered by toggling a GPIO pin or executing an API command.

Baseband PLL

The ADRV9002 contains a baseband PLL synthesizer that generates all baseband and data port related clocks. Two options are provided for a high performance baseband PLL and a low power baseband PLL. A high performance baseband PLL offers greater flexibility in generating clocks to support a wider range of sample rates. A low power baseband PLL has a limitation in supporting certain sample rates but consumes less power. Both high performance and low power baseband PLLs are automatically programmed based on the data rate and sample rate requirements of the system.

SPI

The ADRV9002 uses an SPI to communicate with the baseband processor. This interface can be configured either as a 4-wire interface with dedicated receive and transmit ports, or as a 3-wire interface with a bidirectional data communications port. This bus allows the baseband processor to set all device control parameters using a simple address data serial bus protocol.

Write commands follow a 24-bit format. The first bit sets the bus direction of the bus transfer. The next 15 bits set the address where the data is written. The final eight bits contain the data transferred to the specific register address. Read commands follow a similar format with the exception that the first 16 bits are transferred on the SPI_DIO pin and the final eight bits are read from the ADRV9002 either on the SPI_DO pin in 4-wire mode or on the SPI_DIO pin in 3-wire mode.

GPIO PINS

Digital General-Purpose Inputs/Outputs (DGPIOs)

The ADRV9002 GPIO signals referenced to the VDIGIO_1P8 supply are intended to interface with digital circuitry and can be configured for numerous functions. Some of these pins, when configured as outputs, are used by the baseband processor as real-time signals to provide a number of internal settings and measurements. This configuration allows the baseband processor to monitor receiver performance in different situations. Signals used for manual gain mode, calibration flags, state machine states, and various receiver parameters are among the outputs that can be monitored on these pins. In addition, certain pins can be configured as inputs and used in various functions, such as setting the receiver gain or transmitter attenuation in real time.

Analog General-Purpose Inputs/Outputs (AGPIOs)

The AGPIO pins are intended to interface with system blocks that perform analog functions. The AGPIO pins referenced to the VAGPIO_1P8 supply provide control signals to the external components, such as the low noise amplifier (LNA) or digital step attenuator (DSA). The selected AGPIO pins provide an alternate auxiliary DAC functionality. See [Table 18](#) for more details on pin mapping.

AUXILIARY CONVERTERS

Auxiliary ADC Inputs (AUXADC_x)

The ADRV9002 contains four auxiliary ADCs with the corresponding inputs connected to four dedicated input pins (AUXADC_x). This block can monitor system voltages without additional components. The auxiliary ADC is 10 bits with an input voltage range of 0.05 V to 0.95 V. When enabled, the auxiliary ADC is free running. An API function allows the user to read back the last value latched by the ADC.

Auxiliary DACs Outputs (AUXDAC_x)

The ADRV9002 contains four identical auxiliary DACs (AUXDAC_x) that can supply bias voltages, analog control voltages, or other system functionality. The auxiliary DACs (AUXDAC_0 to AUXDAC_3) are multiplexed with the AGPIO_xx pins, as shown in [Table 18](#). The auxiliary DACs are 12 bits and have an output voltage range of approximately 0.05 V to VDDA_1P8 - 0.05 V and have a current drive of 10 mA. The auxiliary DACs generate ramp up and ramp down patterns that can be loaded into the ADRV9002 and then triggered based on state of dedicated DGPIO pin.

THEORY OF OPERATION

JTAG BOUNDARY SCAN

The ADRV9002 provides support for a JTAG boundary scan. There are five dual function pins associated with the JTAG interface. These pins, as shown in [Table 19](#), are used to access the on-chip

test access port. To enable the JTAG functionality, set the DGPIO_8 pin through DGPIO_11 pin and the MODE pin, as shown in [Table 19](#).

Table 18. Pin Number to AGPIO_xx Mapping and AUXDAC_x

| Pin Number | Primary Function | Alternate Function |
|------------|------------------|--------------------|
| E12 | AGPIO_0 | AUXDAC_0 |
| F10 | AGPIO_1 | AUXDAC_1 |
| E3 | AGPIO_2 | AUXDAC_2 |
| F5 | AGPIO_3 | AUXDAC_3 |
| F4 | AGPIO_4 | Not applicable |
| G4 | AGPIO_5 | Not applicable |
| G6 | AGPIO_6 | Not applicable |
| H6 | AGPIO_7 | Not applicable |
| G9 | AGPIO_8 | Not applicable |
| H9 | AGPIO_9 | Not applicable |
| F11 | AGPIO_10 | Not applicable |
| G11 | AGPIO_11 | Not applicable |

Table 19. Pin Number to DGPIO_xx Mapping and JTAG Function

| Pin Number | Primary Function | JTAG Function, Boundary Scan CMOS Mode | JTAG Function, Boundary Scan LVDS Mode |
|------------|------------------------|--|--|
| K6 | DGPIO_0 | Not applicable | Not applicable |
| K7 | DGPIO_1 | Not applicable | Not applicable |
| K8 | DGPIO_2 | Not applicable | Not applicable |
| K9 | DGPIO_3 | TDO | TDO |
| K10 | DGPIO_4 | $\overline{\text{TRST}}$ | $\overline{\text{TRST}}$ |
| K11 | DGPIO_5 | TDI | TDI |
| L4 | DGPIO_6 | TMS | TMS |
| L5 | DGPIO_7 | TCLK | TCLK |
| L6 | DGPIO_8 | User sets to 0 | User sets to 1 |
| L9 | DGPIO_9 | User sets to 0 | User sets to 0 |
| L10 | DGPIO_10 | User sets to 0 | User sets to 0 |
| L11 | DGPIO_11 | User sets to 0 | User sets to 0 |
| M9 | DGPIO_12/TX1_DCLK_OUT- | Not applicable | Not applicable |
| M10 | DGPIO_13/TX1_DCLK_OUT+ | Not applicable | Not applicable |
| M6 | DGPIO_14/TX2_DCLK_OUT- | Not applicable | Not applicable |
| M5 | DGPIO_15/TX2_DCLK_OUT+ | Not applicable | Not applicable |
| L13 | MODE Pin | User sets to 1 | User sets to 1 |

APPLICATIONS INFORMATION

POWER SUPPLY SEQUENCE

The ADRV9002 requires a specific power-up sequence to avoid undesired power-up currents. The optimal power-on sequence requires VDD_1P0 to power up first. The VDDA_1P3 and VDDA_1P8 supplies must then power up after the VDD_1P0 supply. If VDDA_1P0 is used, VDDA_1P0 must be powered up after VDDA_1P3 and VDDA_1P8 are enabled.

The user must toggle the $\overline{\text{RESET}}$ signal after power has stabilized prior to configuration.

DIGITAL DATA INTERFACE

The ADRV9002 data interface supports both CMOS and LVDS electrical interfaces. The CSSI is intended for narrow RF signal bandwidths, and the LVDS synchronous serial interface (LSSI) can support the full RF bandwidth of the ADRV9002. [Table 20](#) provides a high level overview. For more details, refer to the [ADRV9001](#) system development user guide.

All signal lanes support both electrical interfaces, but concurrent operation of both interfaces is not supported. Additionally, each receive and transmit channel has a dedicated set of lanes for transferring information. The receive and transmit channels cannot be reconfigured to an alternative ball configuration that is different from how it has been assigned by design.

CSSI

The CSSI supports two modes of operation, 1-lane serialized data or 4-lane data. In either case, the maximum clock frequency supported by the CMOS configuration is 80 MHz.

For the CSSI in 1-lane data mode, 16 bits of I data and 16 bits of Q data (a total of 32 data bits) are serialized on a single lane. [Figure 363](#) shows a graphical overview of the CSSI in 1-lane data mode.

For the CSSI in 4-lane data mode, the I and Q digital data is spread across four data lanes. The 16 bits of I data and 16 bits of Q data are split into 8 bits and sent over one of four data lanes. For example, Lane 0 would have 8 LSB bits of I data, Lane 1 would have 8 MSB bits of I data, Lane 2 would have 8 LSB bits of Q data, and Lane 3 would have 8 MSB bits of Q data.

The CSSI in 4-lane data mode supports both a full rate clock and a double data rate (DDR) clock. The DDR clock mode allows data to be latched on both the rising and falling edges, which enables twice the available RF bandwidth, as shown in [Figure 364](#).

CSSI Receive

In the receive CMOS configuration, two additional signal lanes are required for the strobe and clock signals in addition to the data

lane requirement as described for the CSSI in 1-lane mode and the CSSI in 4-lane mode, which allows a total of three signal lanes for the CSSI in 1-lane data mode and six total signal lanes for the CSSI in 4-lane data mode.

RXx_DCLK_OUT is an output clock signal that synchronizes the data and strobe output signals. RXx_STROBE_OUT is a strobe output signal that indicates the first bit of the serial data stream. The RXx_STROBE_OUT signal can be configured to indicate the start of the I and Q samples. For a 16-bit data sample, the RXx_STROBE_OUT signal is high for one clock cycle and low for 31 clock cycles. Alternatively, the RXx_STROBE_OUT signal can be configured to be high for I data duration and low for Q data duration. In this case, for a 16-bit data sample, the RXx_STROBE_OUT signal is high for 16 clock cycles (I data) and low for 16 clock cycles (Q data).

CSSI Transmit

For the transmit CMOS configuration, three additional signal lanes are required for the strobe, clock input, and clock output in addition to the data lane requirement as described for the CSSI in 1-lane data mode and the CSSI in 4-lane data mode, which allows a total of four signal lanes for the CSSI in 1-lane data mode and seven total signal lanes for the CSSI in 4-lane data mode.

TXx_DCLK_IN is an input clock to the ADRV9002 that synchronizes to the data inputs (TXx_DATA_IN) and strobe inputs (TXx_STROBE_IN). TXx_STROBE_IN is an input signal that indicates the first bit of the serial data sample. Similar to the receive path, the transmit strobe has two configuration options. The TXx_DCLK_OUT is an output clock from the ADRV9002 to the external baseband device to generate the TXx_DCLK_IN, TXx_STROBE_IN, and TXx_DATA_IN signals.

LSSI

The LSSI supports the higher RF channel bandwidths and requires differential signal pairs. In LSSI mode, there are two data transfer formats, 1-lane data mode, where both the I and Q data are serialized on a single differential pair, or 2-lane data mode, where the I and Q data occupy separate differential pairs. The selection of either 1-lane data mode or 2-lane data mode depends on the RF channel bandwidth. To capture the maximum 40 MHz RF bandwidth of the ADRV9002, select the LSSI in 2-lane data mode. In either case, the maximum clock frequency supported by the LSSI configuration is 491.52 MHz and the clock type is DDR. Refer to [Figure 365](#) for more details.

APPLICATIONS INFORMATION

Table 20. ADRV9002 Data Port Interface Modes

| Interface Mode | Data Lanes per Channel | Serialization Factor per Data Lane | Maximum Data Lane Rate (MHz) | Maximum Clock Rate (MHz) | Maximum RF Bandwidth (MHz) | Sample Rate for I and Q Data (MHz) | Data Type ¹ | Figure Reference |
|---------------------|------------------------|------------------------------------|------------------------------|--------------------------|----------------------------|------------------------------------|------------------------|------------------|
| CSSI in 1-Lane Data | 1 | 32 | 80 | 80 | 1.25 | 2.5 | Normal | Figure 363 |
| CSSI in 1-Lane Data | 1 | 32 | 160 | 80 | 2.5 | 5 | DDR | |
| CSSI in 4-Lane Data | 4 | 8 | 80 | 80 | 5 | 10 | Normal | |
| CSSI in 4-Lane Data | 4 | 8 | 160 | 80 | 10 | 20 | DDR | Figure 364 |
| LSSI in 1-Lane Data | 1 | 32 | 983.04 | 491.52 | 20 | 30.72 | DDR | |
| LSSI in 2-Lane Data | 2 | 16 | 983.04 | 491.52 | 40 | 61.44 | DDR | Figure 365 |
| LSSI in 2-Lane Data | 2 | 12 | 737.28 | 368.64 | 40 | 61.44 | DDR | |

¹ Normal data type refers to data on the rising edges, and DDR is double data rate, where data is available on the rising and falling edges of the input clock.

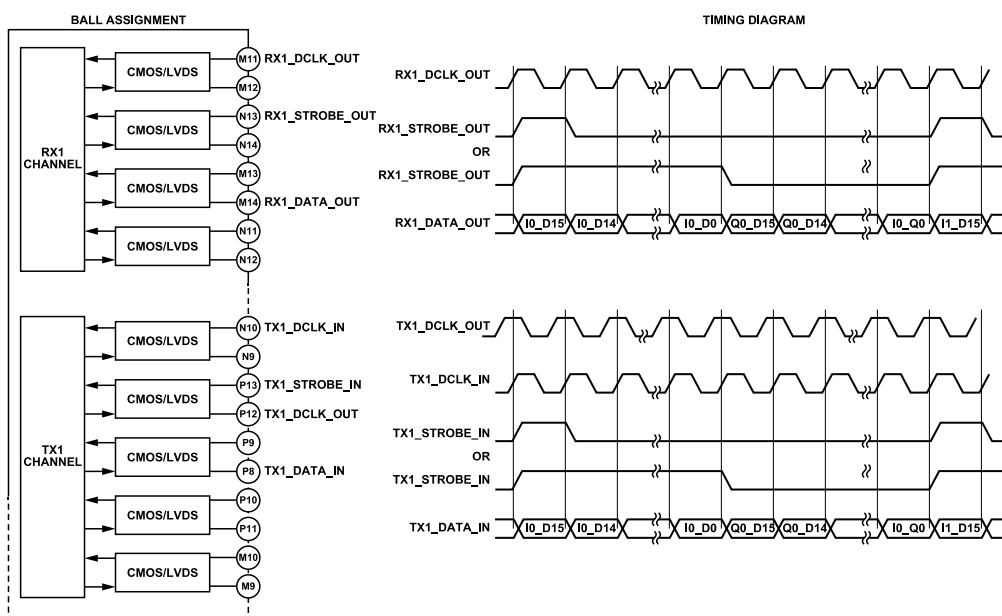


Figure 363. CSSI in 1-Lane Data Mode

APPLICATIONS INFORMATION

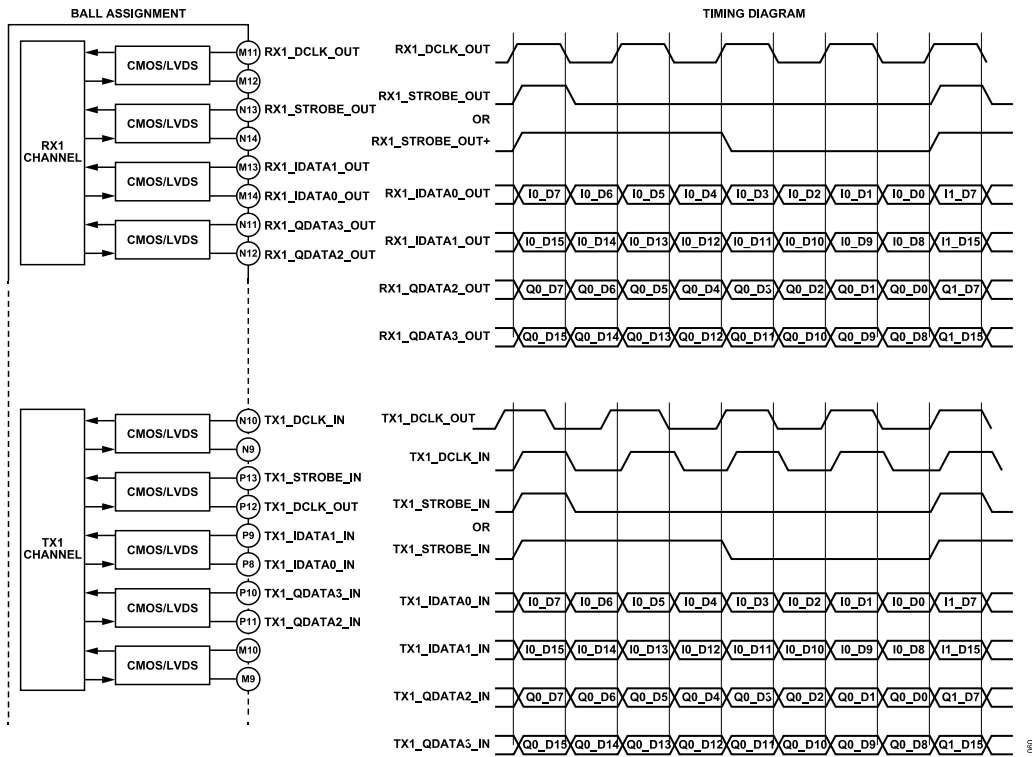


Figure 364. CSSI in 4-Lane Data Mode, DDR

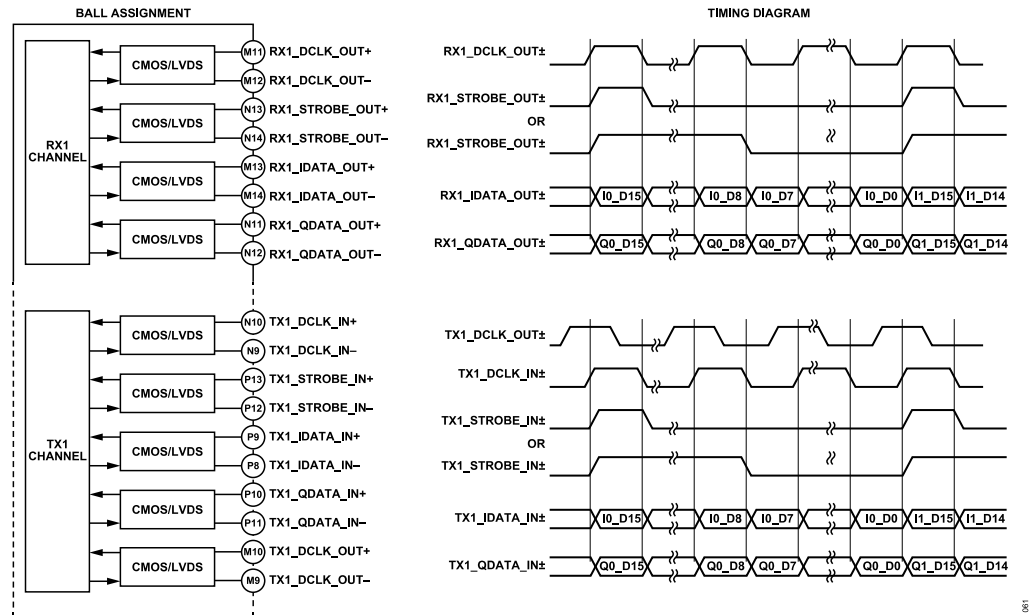


Figure 365. LSSI in 2-Lane Data Mode, DDR

OUTLINE DIMENSIONS

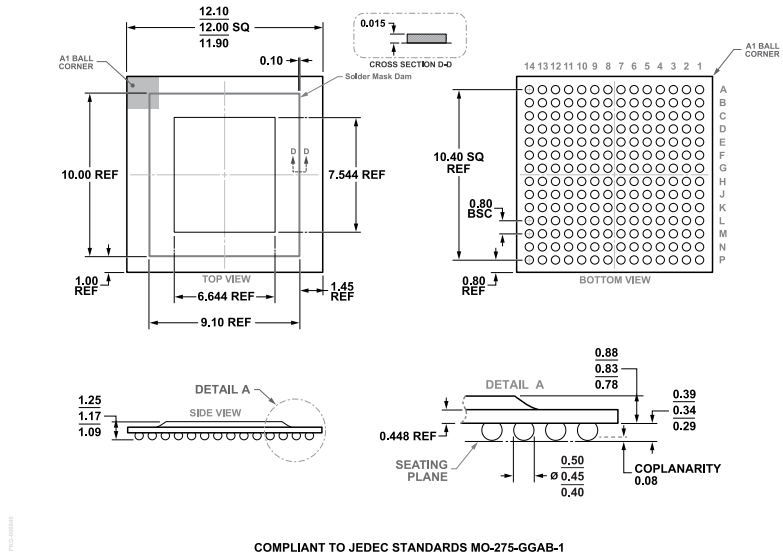


Figure 366. 196-Ball Chip Scale Package Ball Grid Array [CSP_BGA] (BC-196-16)
Dimensions shown in millimeters

Updated: January 28, 2022

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Packing Quantity | Package Option |
|--------------------|-------------------|---------------------|------------------|----------------|
| ADRV9002BBCZ | -40°C to +85°C | CHIP SCALE BGA | | BC-196-16 |
| ADRV9002BBCZ-RL | -40°C to +85°C | CHIP SCALE BGA | Reel, 1500 | BC-196-16 |

¹ Z = RoHS Compliant Part.

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