THE DATASHEET OF

DS1200S

DS1200
Serial RAM Chip

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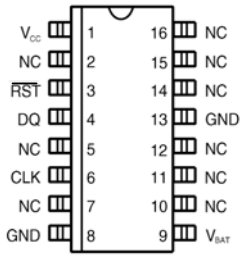
FEATURES

- 1024 Bits of Read/Write Memory
- Low Data Retention Current for Battery Backup Applications
- Four Million Bits/Second Data Rate
- Single-Byte or Multiple-Byte Data Transfer Capability
- No Restrictions on the Number of Write Cycles
- Low-Power CMOS Circuitry

APPLICATIONS

- Software Authorization
- Computer Identification
- System Access Control
- Secure Personnel Areas
- Calibration
- Automatic System Setup
- Traveling Work Record

PIN ASSIGNMENT



16-Pin SO (300mil)
See Mech. Drawings Section

PIN DESCRIPTION

V_{CC}	- +5V
$\overline{RST}$	- Reset
DQ	- Data Input/Output
CLK	- Clock
GND	- Ground
V_{BAT}	- Battery (+)
NC	- No Connection

DESCRIPTION

The DS1200 serial RAM chip is a miniature read/write memory that can randomly access individual 8-bit strings (bytes) or sequentially access the entire 1024-bit contents (burst). Interface cost to a microprocessor is minimized by on-chip circuitry, which permits data transfers with only three signals: CLK, $\overline{RST}$, and DQ.

Nonvolatility can be achieved by connecting a battery of 2V to 4V at the battery input V_{BAT}. A load of 0.5µA should be used to size the external battery for the required data retention time. If nonvolatility is not required the V_{BAT} pin should be grounded.

Figure 1. ELECTRONIC TAG BLOCK DIAGRAM

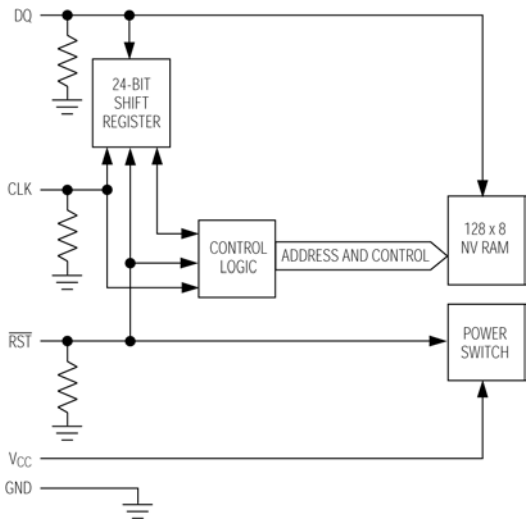
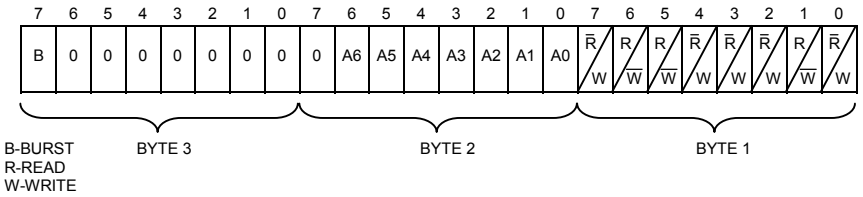


Figure 2. ADDRESS/COMMAND



OPERATION

The block diagram (Figure 1) illustrates the main elements of the device: shift register, control logic, NV RAM, and power switch. To initiate a memory cycle, $\overline{RST}$ is taken high and 24 bits are loaded into the shift register, providing both address and command information. Each bit is input serially on the rising edge of the CLK input. Seven address bits specify one of the 128 RAM locations. The remaining command bits specify read/write and byte/burst mode. After the first 24 clocks, which load the shift register, additional clocks will output data for a read or input data for a write. The number of clock pulses equal 24 plus 8 for byte mode or 24 plus 1024 for burst mode.

For hardwired applications, active power is supplied by the V_{CC} pin. Alternatively, for user-insertable applications, power can be supplied by the $\overline{RST}$ pin.

ADDRESS/COMMAND

Each memory transfer consists of a 3-byte input called the address/command. The address/command is shown in Figure 2. As defined, the first byte of the address/command specifies whether the memory is written or read. If any one of the bits of the first byte of the address/command fail to meet the exact pattern of read or write, the cycle is aborted and all future inputs to the tag are ignored until $\overline{RST}$ is brought low and then high again to begin a new cycle. The 8-bit pattern for read is 10011101. The second byte of the address/command describes address inputs A0 in bit 0 through A6 in bit 6. Bit 7 of the second byte of the address/command word must be set to logic 0. If bit 7 does not equal logic 0, the cycle is aborted and all future inputs to the tag are ignored until $\overline{RST}$ is brought low and then high again to begin a new cycle. The third byte of the address/command (bits 0 through 6) must be set to logic 0 or the cycle is aborted and all future inputs are ignored until $\overline{RST}$ is brought low and then high again to begin a new cycle. Bit 7 of byte 3 of the address/command is used along with address bits A0 through A6 to define burst mode. When A0 through A6 equals logic 0 and bit 7 of byte 3 of the address command equals logic 1, the tag will enter the burst mode after the address/command sequence is complete.

BURST MODE

Burst mode is when all address bits (A0 to A6) of the address/command are set to logic 0 and bit 7 of byte 3 to logic 1. The burst mode causes 128 consecutive bytes to be read or written. Burst mode terminates when the $\overline{RST}$ input is driven low.

RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ input serves three functions. First, $\overline{RST}$ turns on the control logic, which allows access to the shift register for the address/command sequence. Second, the $\overline{RST}$ signal provides a power source for the cycle to follow. To meet this requirement, a drive source for $\overline{RST}$ of 2mA at 3.8V is required. However if the V_{CC} pin is connected to a 5V source within nominal limits, then the $\overline{RST}$ pin is not used as a source of power and input levels revert to normal V_{IH} and V_{IL} inputs with a drive current requirement of 500μA. Finally, the $\overline{RST}$ signal provides a method of terminating either single byte or multiple byte data transfers. A clock cycle is a sequence of falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of the clock cycle. Address/command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfer terminates if the $\overline{RST}$ input is low and DQ pin goes to a high-impedance state. When data transfer to the serial RAM chip is terminated using, $\overline{RST}$, the transition of $\overline{RST}$ must occur while the clock is at high level to avoid disturbing the last bit of data. Data transfer is illustrated in Figure 3.

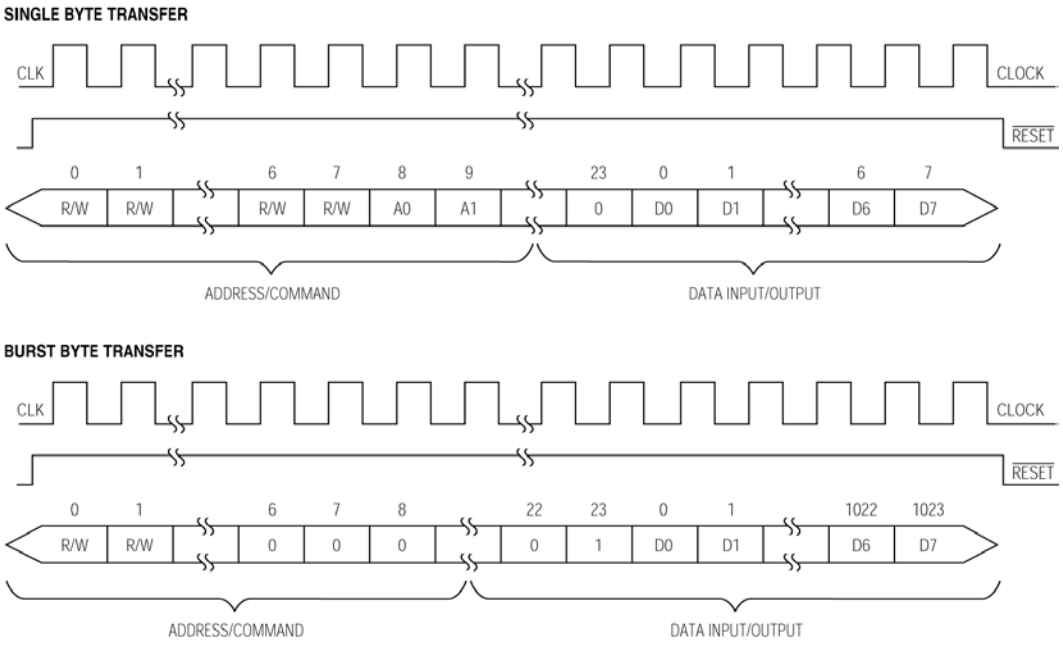
DATA INPUT

Following the 24 clock cycles that input an address/command, a data byte is input on the rising edge of the next eight clock cycles, assuming that the read/write and write/read bits are properly set (for data input byte 1, bit 0 = 1; bit 1 = 0; bit 2 = 1; bit 3 = 1; bit 4 = 1; bit 5 = 0; bit 6 = 0; bit 7 = 1).

DATA OUTPUT

Following the 24 clock cycles that input the read mode, a data byte is output on the falling edge of the next eight clock cycles (for data output byte 1, bit 0 = 0; bit 1 = 1; bit 2 = 0; bit 3= 0; bit 4 = 0; bit 5 = 1; bit 6 = 1; bit 7 = 0).

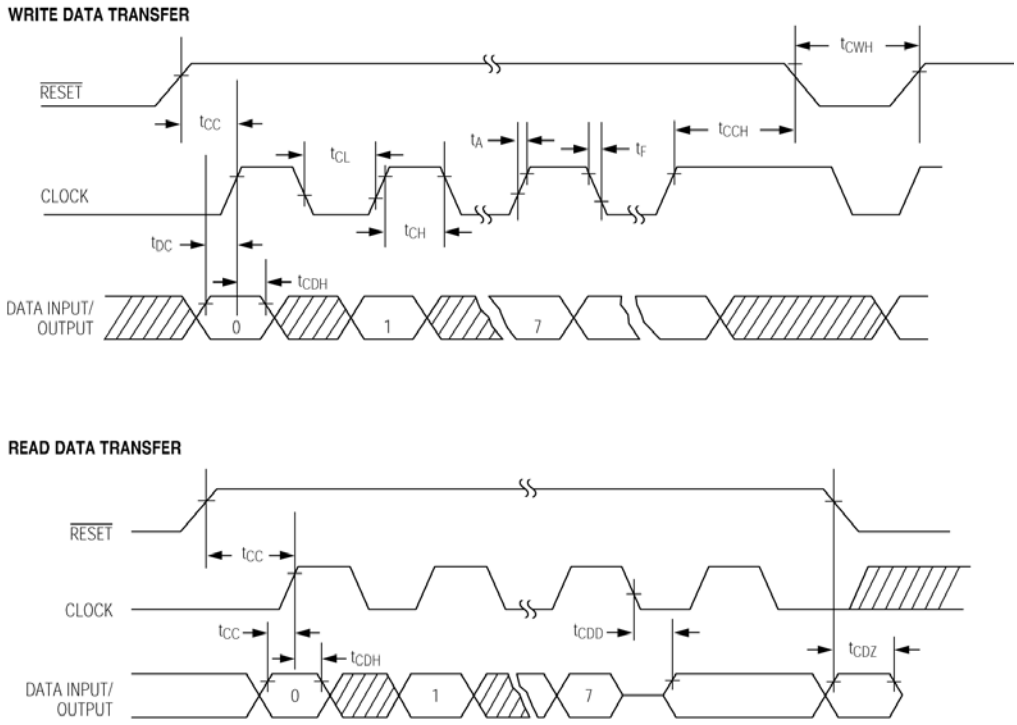
Figure 3. DATA TRANSFER



NOTES:

1) Data input sampled on rising edge of clock cycle.
2) Data output changes on falling edge of clock.

Figure 4. READ/WRITE DATA TRANSFER



ABSOLUTE MAXIMUM RATING*

Voltage Range on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-40°C to +70°C

* *This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.*

RECOMMENDED DC OPERATING CONDITIONS

(0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0			V	1, 2, 10
Logic 0	V_{IL}	-0.3		0.8	V	1
$\overline{RST}$ Logic 1	V_{IHE}	3.8				1, 7, 11
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Battery Voltage	V_{BAT}	2.0		4.0	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to +70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_L			+500	µA	5
Output Leakage	I_{LO}			+500	µA	5
Output Current at 2.4V	I_{OH}	-1			mA	
Output Current at 0.4V	I_{OL}			+2	mA	
$\overline{RST}$ Input Resistance	Z_{RST}	10		40	kΩ	1
DQ Input Resistance	Z_{DQ}	10		40	kΩ	1
CLK Input Resistance	Z_{CLK}	10		40	kΩ	1
Active Current	I_{CC1}			6	mA	8
Standby Current	I_{CC2}			2.5	mA	8
$\overline{RST}$ Current	I_{RST}	2			mA	7, 8, 13

CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS (0ºC to +70ºC; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	3, 9
Data to CLK Hold	t_{CDH}	40			ns	3, 9
Data to CLK Delay	t_{CDD}			125	ns	3, 4, 6, 9
CLK Low Time	t_{CL}	125			ns	3, 9
CLK High Time	t_{CH}	125			ns	3, 9
CLK Frequency	f_{CLK}	DC		4.0	MHz	3, 9
CLK Rise and Fall	t_R, t_F			500	ns	9
$\overline{RST}$ to Clock Setup	t_{CC}	1			µs	3, 9
CLK to RST Hold	t_{CCH}	40			ns	3, 9
$\overline{RST}$ Inactive Time	t_{CWH}	125			ns	3, 9, 14
$\overline{RST}$ to I/O High-Z	t_{CDZ}			50	ns	3, 9

NOTES:

1) All voltages and resistances are referenced to ground.
2) Input levels apply to CLK, DQ, and $\overline{RST}$ while V_{CC} is not connected to the tag, then $\overline{RST}$ input reverts to V_{IHE}.
3) Measured at V_{IH} = 2.0 or V_{IL} = 0.8V and 10ns maximum rise and fall time.
4) Measured at V_{OH} = 2.4V and V_{OL} = 0.4V.
5) For CLK, DQ, $\overline{RST}$, and V_{CC} at 5V.
6) Load capacitance = 50pF.
7) Applies to $\overline{RST}$ when V_{CC} < 3.8V.
8) Measured with outputs open.
9) Measured at VIH of $\overline{RST}$ greater than or equal to 3.8V when $\overline{RST}$ supplies power.
10) Logic 1 maximum is V_{CC} + 0.3V if the V_{CC} pin supplies power and $\overline{RST}$ +0.3V if the $\overline{RST}$ pin supplies power.
11) $\overline{RST}$ logic 1 maximum is V_{CC} + 0.3V if the V_{CC} pin supplies power and 5.5V maximum if $\overline{RST}$ supplies power.
12) Each DS1200 is marked with a four-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
13) Average AC $\overline{RST}$ current can be determined using the following formula:

$$I_{TOTAL} = 2 + I_{LOAD}\ DC + (4 \times 10^{-3})(CL + 140)f$$

I_{TOTAL} and I_{LOAD} are in mA; CL is in pF; f is in MHz.

Applying the above formula, a load capacitance of 50pF running at a frequency of 4.0MHz gives an I_{TOTAL} current of 5mA.

14) When $\overline{RST}$ is supplying power, t_{CWH} must be increased to 100ms.

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