THE DATASHEET OF

DS1021S-50

DS1021
Programmable 8-Bit Silicon Delay Line

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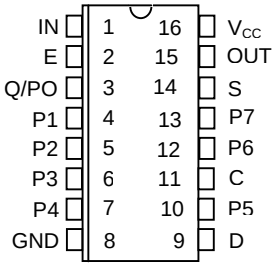
FEATURES

- All-silicon time delay
- Models with 0.25 ns and 0.5 ns steps
- Programmable using 3-wire serial port or 8-bit parallel port
- Leading and trailing edge accuracy
- Economical
- Auto-insertable, low profile, 16-pin SOIC package
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable

PIN ASSIGNMENT



DS1021S 16-Pin SOIC (300-mil)
See Mech. Drawings Section

PIN DESCRIPTION

IN	- Delay Input
P0-P7	- Parallel Program Pins
GND	- Ground
OUT	- Delay Output
V_{CC}	- +5 Volts
S	- Mode Select
E	- Enable
C	- Serial Port Clock
Q	- Serial Data Output
D	- Serial Data Input

DESCRIPTION

The DS1021 Programmable 8-Bit Silicon Delay Line consists of an 8-bit, user-programmable CMOS silicon integrated circuit. Delay values, programmed using either the 3-wire serial port or the 8-bit parallel port, can be varied over 256 equal steps. The faster model (-25) offers a maximum delay of 73.75 ns with an incremental delay of 0.25 ns, while the slower model (-50) has a maximum delay of 137.5 ns with an incremental delay of 0.5 ns. Both models have an inherent (step zero) delay of 10 ns. After the user-determined delay, the input logic state is reproduced at the output without inversion. The DS1021 is TTL- and CMOS-compatible, capable of driving 10 74LS-type loads, and features both rising and falling edge accuracy.

The all-CMOS DS1021 integrated circuit has been designed as a reliable, economic alternative to hybrid programmable delay lines. It is offered in a space-saving surface mount 16-pin SOIC.

PARALLEL MODE (S = 1)

In the PARALLEL programming mode, the output of the DS1021 will reproduce the logic state of the input after a delay determined by the state of the 8 program input pins P0 - P7. The parallel inputs can be programmed using DC levels or computer-generated data. For infrequent modification of the delay value, jumpers may be used to connect the input pins to V_{CC} and ground. For applications requiring frequent timing adjustment, DIP switches should be used. The enable pin (E) must be at a logic 1 in hardwired implementations.

Maximum flexibility is obtained when the 8 parallel programming bits are set using computer-generated data. When the data setup (t_{DSE}) and data hold (t_{DHE}) requirements are observed, the enable pin can be used to latch data supplied on an 8-bit bus. Enable must be held at a logic 1 if it is not used to latch the data. After each change in delay value, a settling time (t_{EDV} or t_{PDV}) is required before input logic levels are accurately delayed.

Since the DS1021 is a CMOS design, unused input pins (D and C) must be connected to well-defined logic levels; they must not be allowed to float.

SERIAL MODE (S = 0)

In the SERIAL programming mode, the output of the DS1021 will reproduce the logic state of the input after a delay time determined by an 8-bit value clocked into serial port D. While observing data setup (t_{DSC}) and data hold (t_{DHC}) requirements, timing data is loaded in MSB-to-LSB order by the rising edge of the serial clock (C). The enable pin (E) must be at a logic 1 to load or read the internal 8-bit input register, during which time the delay is determined by the last value activated. Data transfer ends and the new delay value is activated when enable (E) returns to a logic 0. After each change, a settling time (t_{EDV}) is required before the delay is accurate.

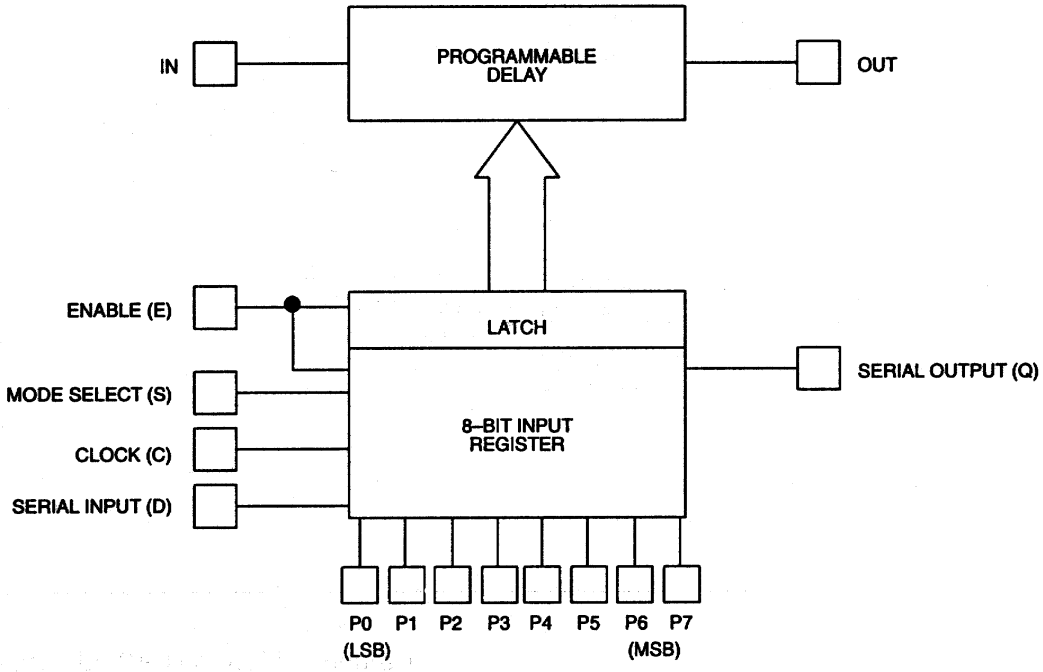
As timing values are shifted into the serial data input (D), the previous contents of the 8-bit input register are shifted out of the serial output pin (Q) in MSB-to-LSB order. By connecting the serial output of one DS1021 to the serial input of a second DS1021, multiple devices can be daisy-chained (cascaded) for programming purposes (Figure 3). The total number of serial bits must be eight times the number of units daisy-chained and each group of 8 bits must be sent in MSB-to-LSB order.

Applications can read the setting of the DS1021 delay line by connecting the serial output pin (Q) to the serial input (D) through a resistor with a value of 1K to 10K ohms (Figure 2). Since the read process is destructive, the resistor restores the value read and provides isolation when writing to the device. The resistor must connect the serial output (Q) of the last device to the serial input (D) of the first device of a daisy-chain (Figure 3). For serial readout with automatic restoration through a resistor, the device used to write serial data must go to a high impedance state.

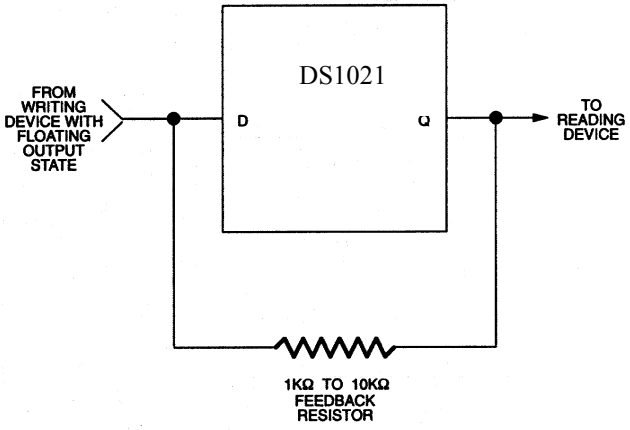
To initiate a serial read, enable (E) is taken to a logic 1 while serial clock (C) is at a logic 0. After a waiting time (t_{EQV}), bit 7 (MSB) appears on the serial output (Q). On the first rising ($0 \rightarrow 1$) transition of the serial clock (C), bit 7 (MSB) is rewritten and bit 6 appears on the output after a time t_{CQV}. To restore the input register to its original state, this clocking process must be repeated eight times. In the case of a daisy-chain, the process must be repeated eight times per package. If the value read is restored before enable (E) is returned to logic 0, no settling time (t_{EDV}) is required and the programmed delay remains unchanged.

Since the DS1021 is a CMOS design, unused input pins (P1 - P7) must be connected to well-defined logic levels; they must not be allowed to float. Serial output Q/P0 should be allowed to float if unused.

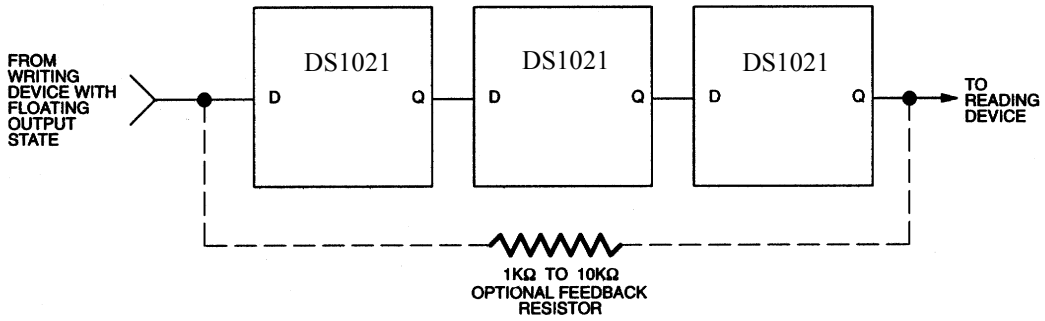
FUNCTION BLOCK DIAGRAM Figure 1



SERIAL READOUT Figure 2



CASCADING MULTIPLE DEVICES (DAISY CHAIN) Figure 3



PART NUMBER TABLE Table 1

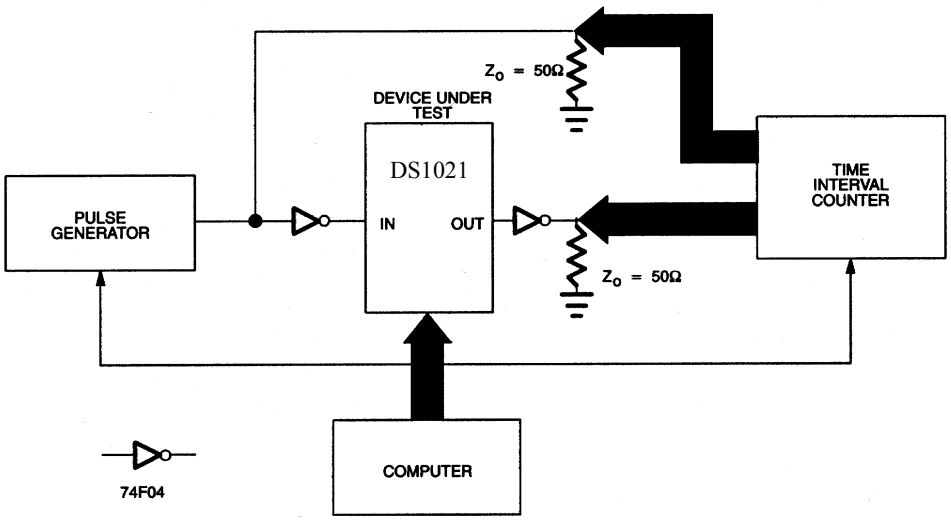
DELAYS AND TOLERANCES (IN ns)				
PART NUMBER	**STEP ZERO DELAY TIME**	**MAX DELAY TIME (NOM)**	**DELAY CHANGE PER STEP (NOM)**	**MAX DEVIATION FROM PROGRAMMED DELAY**
DS1020-25	10 ± 2	73.75	0.25	±6
DS1020-50	10 ± 2	137.5	0.5	±8

DELAY VS. PROGRAMMED VALUE Table 2

	MIN DELAY (STEP ZERO)						∫∫			**MAX DELAY**	**PARALLEL PORT**	**SERIAL PORT**
BINARY PROGRAMMED VALUE	0	0	0	0	0	0		1	1	1	P7	MSB
	0	0	0	0	0	0		1	1	1	P6	
	0	0	0	0	0	0		1	1	1	P5	
	0	0	0	0	0	0		1	1	1	P4	
	0	0	0	0	0	0		1	1	1	P3	
	0	0	0	0	1	1		1	1	1	P2	
PART NUMBER	0	0	1	1	0	0		0	1	1	P1	
	0	1	0	1	0	1		1	0	1	P0	LSB
DS1021-25	10.00	10.25	10.50	10.75	11.00	11.25		73.25	73.50	73.75		
DS1021-50	10.0	10.5	11.0	11.5	12.0	12.5	∫∫	136.5	137.0	137.5		

All delays in nanoseconds, referenced to input pin.

DALLAS SEMICONDUCTOR TEST CIRCUIT Figure 4



TEST SETUP DESCRIPTION

Figure 4 illustrates the hardware configuration used for measuring the timing parameters of the DS1021. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1021 serial and parallel ports are controlled by interfaces to a central computer. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohms max.
Rise and Fall Time:	3.0 ns max.
	(measured between 0.6V and 2.4V)
Pulse Width:	500 ns (DS1021–25)
	2 µs (DS1021–50)
Period:	1 µs (DS1021–25)
	4 µs (DS1021–50)

NOTE: Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

OUTPUT:
Output is loaded with a 74F04. Delay is measured between the 1.5V level of the rising edge of the input signal and the 1.5V level of the corresponding edge of the output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	µA	
Active Current	I_{CC}	V_{CC}=MAX; Period=1 µs			30.0	mA	3
High Level Output Current	I_{OH}	V_{CC}=MIN. V_{OH}=2.7V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC}=MIN. V_{OL}=0.5V	8			mA	4

AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f_C			10	MHz	
Enable Width	t_{EW}	50			ns	Fig. 7, 8
Clock Width	t_{CW}	50			ns	Fig. 8
Data Setup to Clock	t_{DSC}	30			ns	Fig. 8
Data Hold from Clock	t_{DHC}	10			ns	Fig. 8
Data Setup to Enable	t_{DSE}	30			ns	Fig. 7
Data Hold from Enable	t_{DHE}	20			ns	Fig. 7
Enable to Serial Output Valid	t_{EQV}			50	ns	Fig. 8
Enable to Serial Output High Z	t_{EQZ}	0		50	ns	Fig. 8
Clock to Serial Output Valid	t_{CQV}			50	ns	Fig. 8
Clock to Serial Output Invalid	t_{CQX}	10			ns	Fig. 8
Enable Setup to Clock	t_{ES}	50			ns	Fig. 8
Enable Hold from Clock	t_{EH}	50			ns	Fig. 8
Parallel Input Valid to Delay Valid	t_{PDV}			50	µs	Fig. 6

(cont'd)

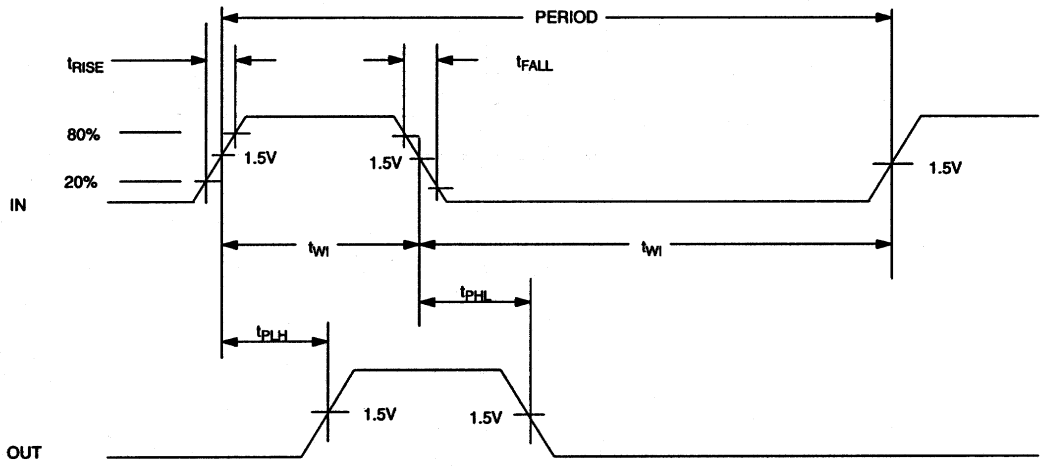
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Parallel Input Change to Delay Invalid	t_{PDX}	0			ns	
Enable to Delay Valid	t_{EDV}			50	µs	
Enable to Delay Invalid	t_{EDX}	0			ns	
V_{CC} Valid to Device Functional	t_{PU}			100	ms	
V_{CC} Rise Time	t_{VR}	20			ms	
Input Pulse Width	t_{WI}	100% of Output Delay			ns	
Input to Output Delay	t_{PLH}, t_{PHL}		Table 2		ns	2
Input Period	Period	2 (t_{WI})			ns	

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	

TIMING DIAGRAM: SILICON DELAY LINE Figure 5



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

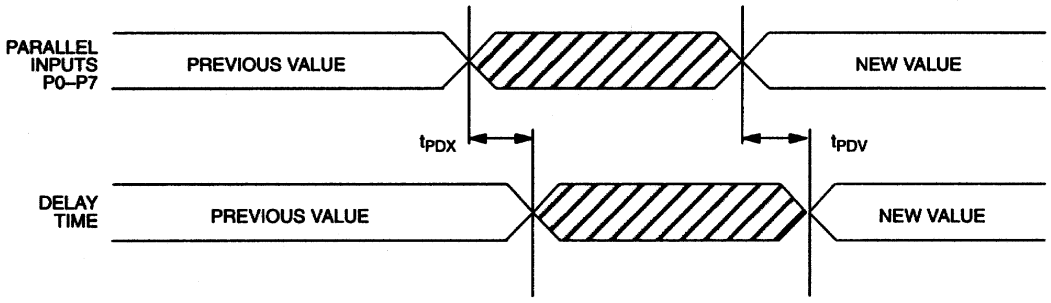
t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

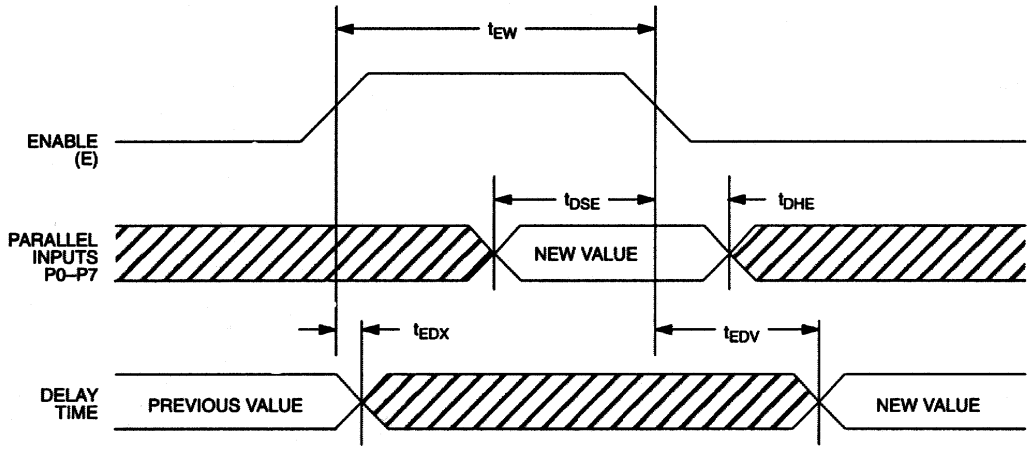
t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the corresponding output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of the output pulse.

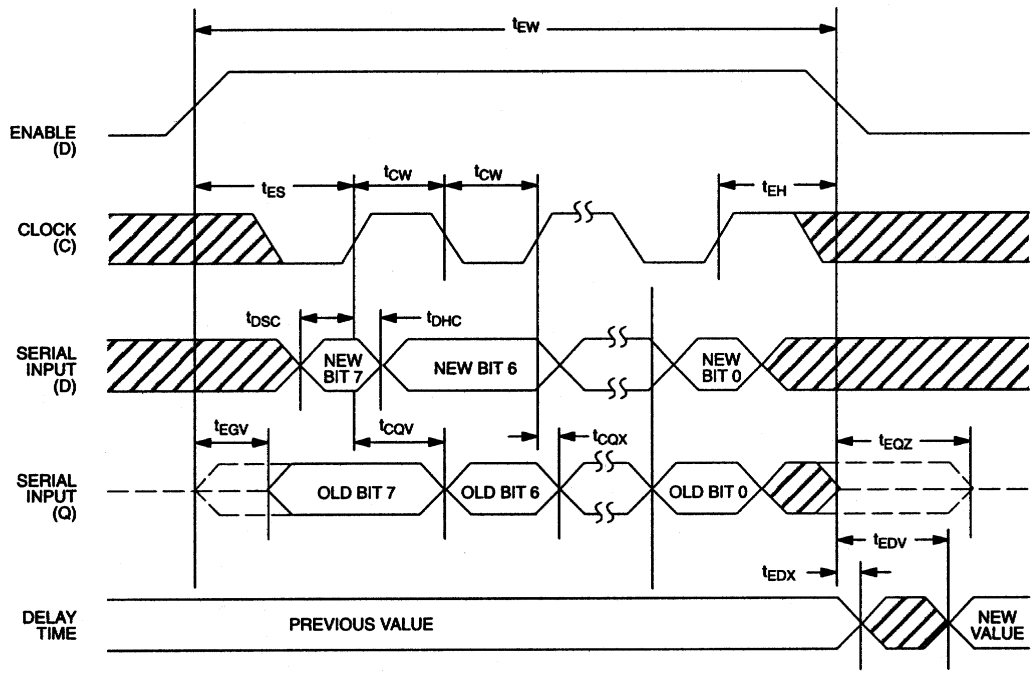
TIMING DIAGRAM: NON-LATCHED PARALLEL MODE (S = 1, E = 1) Figure 6



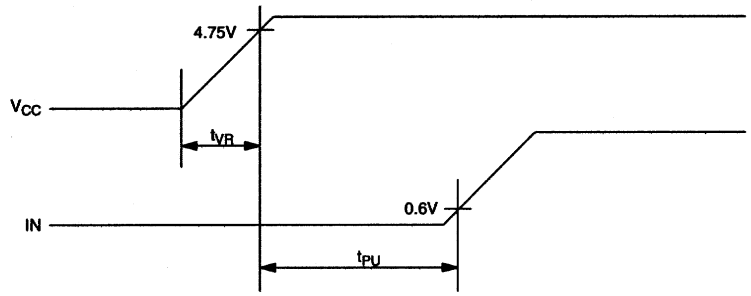
TIMING DIAGRAM: LATCHED PARALLEL MODE (S=1) Figure 7



TIMING DIAGRAM: SERIAL MODE (S = 0) Figure 8



TIMING DIAGRAM: POWER-UP Figure 9



NOTES:

1. All voltages are referenced to ground.

2. @ V_{CC} = 5V and 25°C. Delay accurate on both rising and falling edges within tolerances given in Table 1.

3. Measured with output open.

4. The "Q" output will only source 4 mA. This pin is only intended to drive other DS1021s.

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