



**THE DATASHEET OF  
BLP25RFE001E**



# BLP25RFE001

Signal generator for RF energy solutions

Rev. 2 — 26 January 2018

AMPLEON

Product data sheet

## 1. General description

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The product provides an all-in-one solution for the small signal generation in the RF energy solutions such as cooking and lighting markets.

The product facilitates RF energy design by:

- Allowing on-board integration
- Providing flexibility in system solution development

## 2. Features and benefits

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- Support from 2400 MHz to 2483.5 MHz, from 902 MHz to 928 MHz and from 433 MHz to 434.8 MHz ISM bands
- Single 3.3 V supply voltage
- SPI-bus interface up to 20 MHz
- Fully integrated LC-VCO operating in the range from 6.6 GHz to 10 GHz and used with a  $\Sigma\Delta$  PLL to generate the frequency
- Very fast tuning and hopping time PLL
- High frequency daisy chaining allowing coherent excitation of multiple RF amplifier chains
- 360° phase shifter with 1.4° steps
- Medium Power Amplifier (MPA) delivering an output up to +27 dBm peak power (max. +24 dBm for continuous use)
- Low Power Amplifier (PPA) delivering an output up to +7 dBm
- Integrated 20 dB gain control
- Integrated RF switch allowing PWM control
- Temperature sensor indicates the junction temperature of the die
- RoHS compliant

## 3. Applications

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- Solid-state cooking
- Solid-state lighting

## 4. Ordering information

Table 1. Ordering information

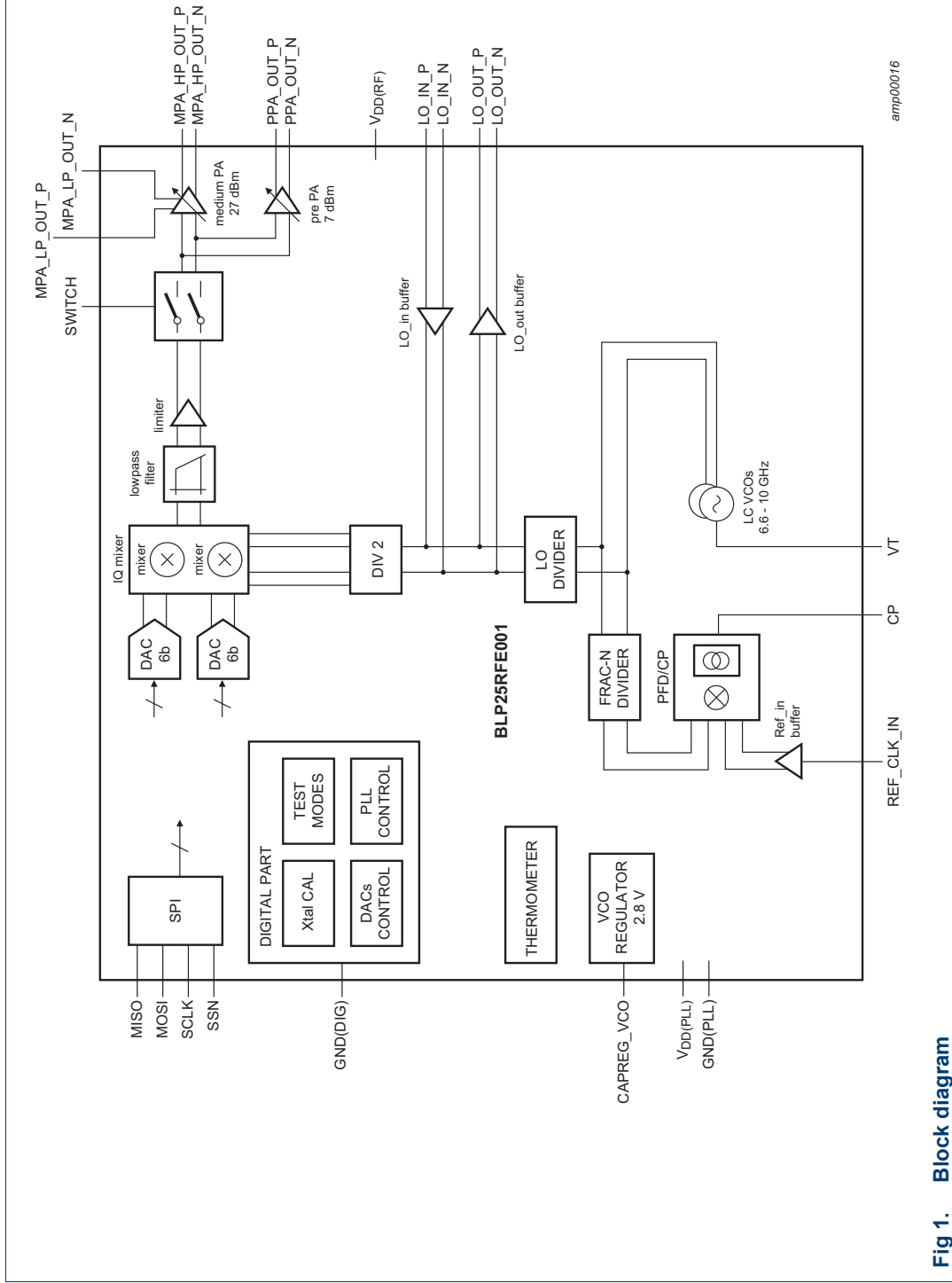
Type number	Package		
	Name	Description	Version
BLP25RFE001	HVQFN28	plastic thermal enhanced very thin quad flat package; no leads; 28 terminals; body 5 × 5 × 0.85 mm	SOT993-3

## 5. Marking

Table 2. Marking codes

Type number	Marking code
BLP25RFE001	E2501

## 6. Block diagram



amp00016

Fig 1. Block diagram

## 7. Pinning information

### 7.1 Pinning

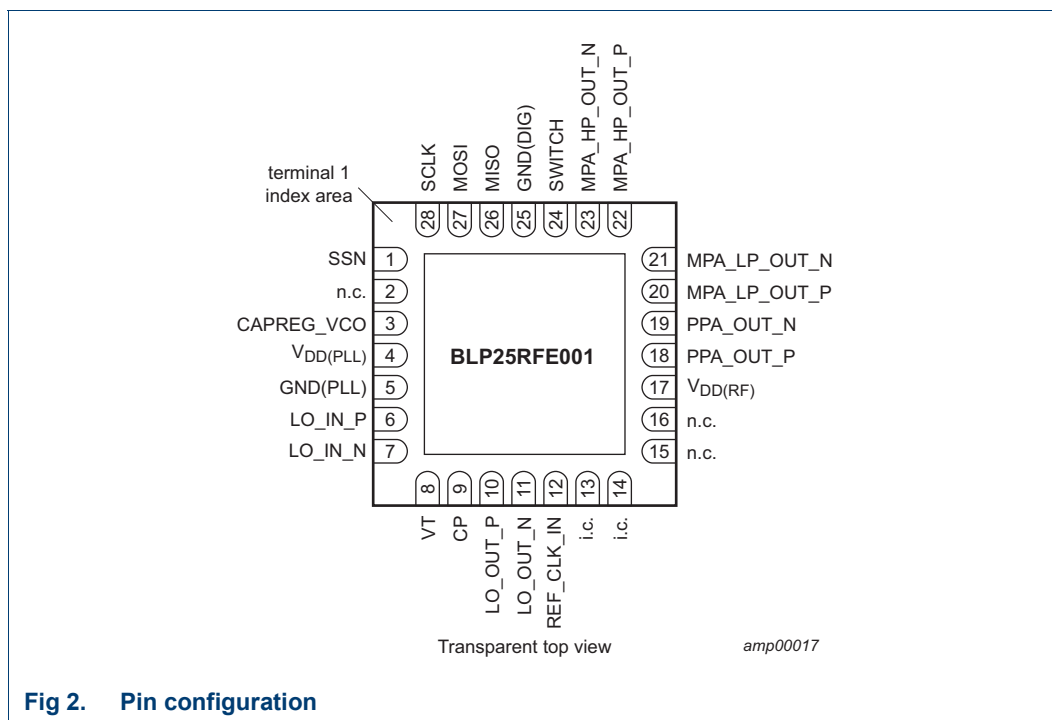


Fig 2. Pin configuration

### 7.2 Pin description

Table 3. BLP25RFE001 pin description

Symbol	Pin	Description
SSN	1	SPI-bus: Slave Select Not (from master)
n.c.	2	not connected
CAPREG_VCO	3	VCO internal regulator filtering input
V <sub>DD</sub> (PLL)	4	PLL supply voltage; 3.3 V
GND(PLL)	5	PLL ground
LO_IN_P	6	high frequency daisy chaining positive input
LO_IN_N	7	high frequency daisy chaining negative input
VT	8	VCO input voltage
CP	9	charge pump output
LO_OUT_P	10	high frequency daisy chaining positive output
LO_OUT_N	11	high frequency daisy chaining negative output
REF_CLK_IN	12	external reference clock input
i.c.	13	internally connected
i.c.	14	internally connected
n.c.	15	not connected
n.c.	16	not connected

Table 3. BLP25RFE001 pin description ...continued

Symbol	Pin	Description
V <sub>DD(RF)</sub>	17	RF power supply; 3.3 V
PPA_OUT_P	18	RF low-power positive output
PPA_OUT_N	19	RF low-power negative output
MPA_LP_OUT_P	20	RF Intermediate supply for high-power first stage MPA positive path
MPA_LP_OUT_N	21	RF Intermediate supply for high-power first stage MPA negative path
MPA_HP_OUT_P	22	medium-power RF amplifier positive output
MPA_HP_OUT_N	23	medium-power RF amplifier negative output
SWITCH	24	RF switch control
GND(DIG)	25	digital ground
MISO	26	SPI-bus: Master Input Slave Output
MOSI	27	SPI-bus: Master Output Slave Input
SCLK	28	SPI-bus: Serial Clock (from master)
Exposed die pad	-	connect to RF ground

## 8. Functional description

General purpose 4 wires SPI-bus with a dedicated integrated oscillator for the digital clock, enabling high-speed SPI-bus.

Very high frequency LC oscillator running at  $4 \times F_{out}$  for lowest pulling sensitivity.

Fractional-N PLL enabling 10 kHz steps at  $F_{out}$  with a very low PLL settling time.

ADC on  $V_{tune}$  for an easy estimation via SPI-bus of the PLL locking point.

High frequency daisy chaining operation enabling coherent frequencies to all the circuits in the application.

360° phase shifter with small and accurately controlled steps (1.4° typical).

Medium RF power output: up to +27 dBm peak power (max. +24 dBm for continuous use).

Low RF power output up to 7 dBm adjustable.

Integrated RF switch (dedicated control pin SWITCH) allowing PWM control of the RF outputs (MPA/PPA).

### 8.1 Medium Power Amplifier (MPA)

The medium power amplifier (MPA) consists of 3 cascaded gain stages. The last 2 stages have open collector which must be DC supplied through adequate reactive circuitry to optimize power and efficiency. The third stage is able to drive up to +27 dBm peak power (max. +24 dBm for continuous use) into 50 Ω. The output matching network is for impedance transformation (from 40 Ω to 50 Ω) and also acts as a low pass filter that attenuates harmonics.

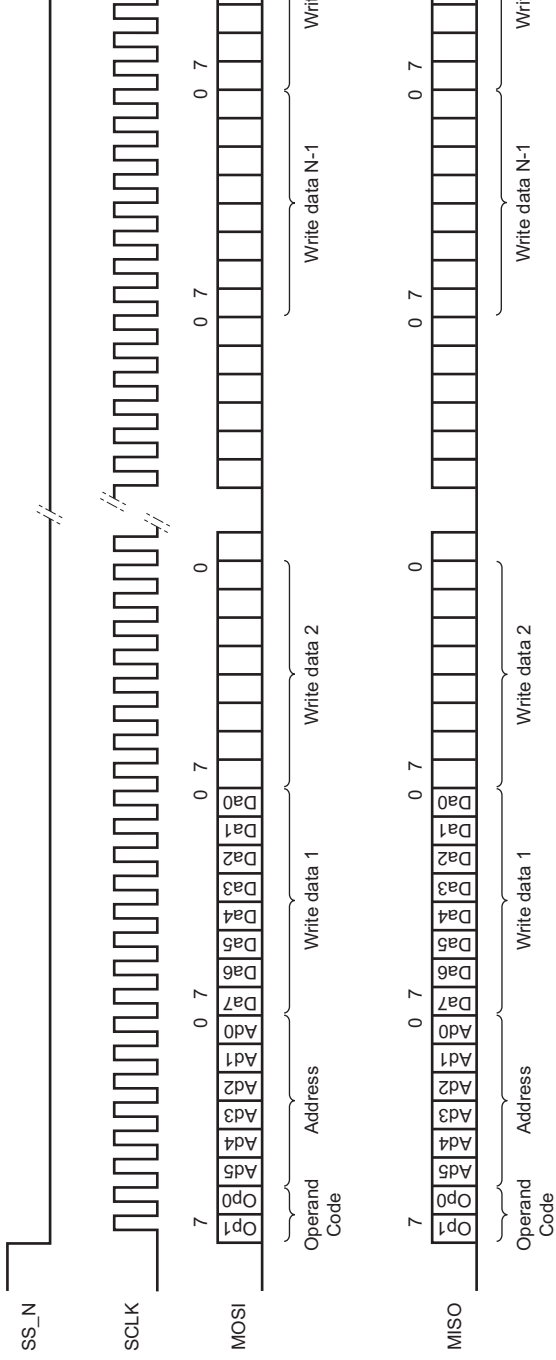
## 8.2 Low-Power Amplifier (PPA)

The low power amplifier (PPA) consists of 2 cascaded gain stages. The last stage have open collector which must be DC supplied through adequate reactive circuitry to optimize power and efficiency. The third stage is able to drive up to 7 dBm into 50  $\Omega$ . The output matching network is for impedance transformation (from 200  $\Omega$  to 50  $\Omega$ ) and also acts as a low pass filter that attenuates harmonics.

## 8.3 SPI-bus interface

- The SPI-bus protocol used on BLP25RFE001 IC is composed of:
  - 2 operand code bits (00: write, 01: read, 1x: reserved)
  - 6 address bits
  - 8 data bits
- A burst mode, in write and read mode, is implemented (an auto-increment of the address is used to manage this mode)
- The SPI-bus frequency up to 20 MHz
- MISO output pin is not tri-state and cannot be connected with an other BLP25RFE001 IC

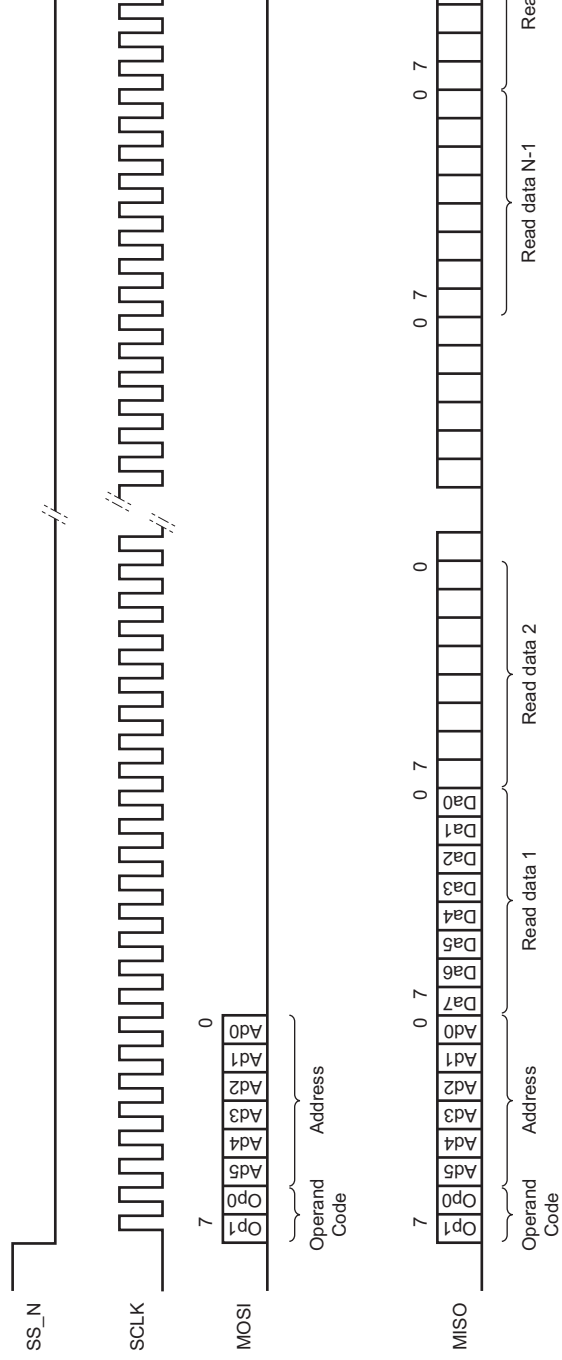
### 8.3.1 SPI-bus write protocol burst mode



Operand Code Op[1:0] = 00.

**Fig 3. SPI-bus write protocol burst mode**

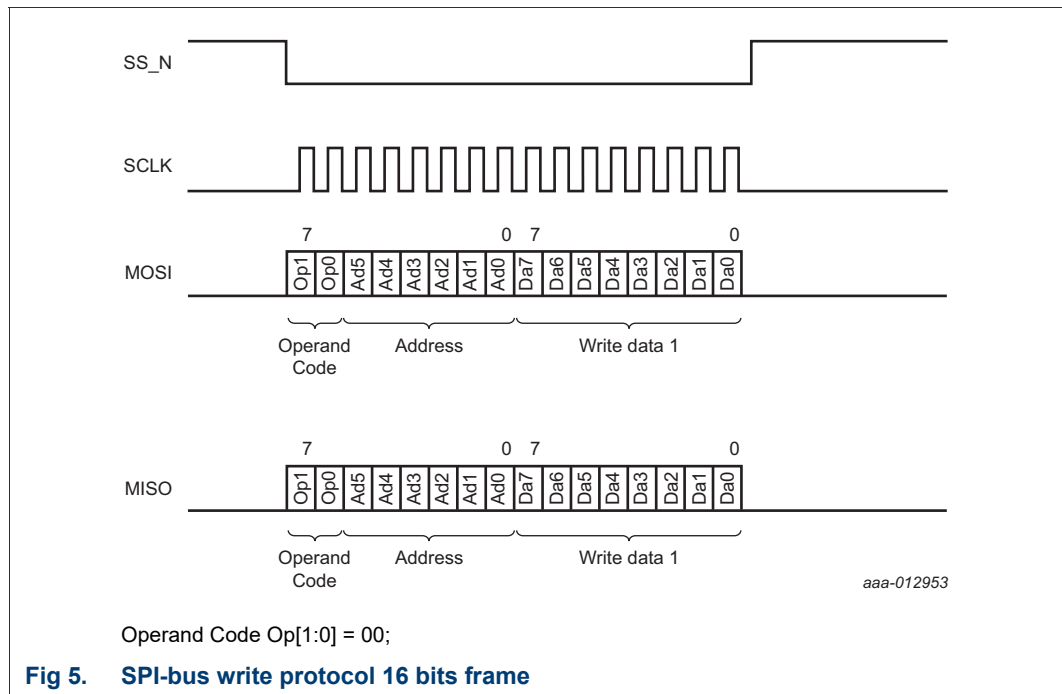
### 8.3.2 SPI-bus read protocol burst mode



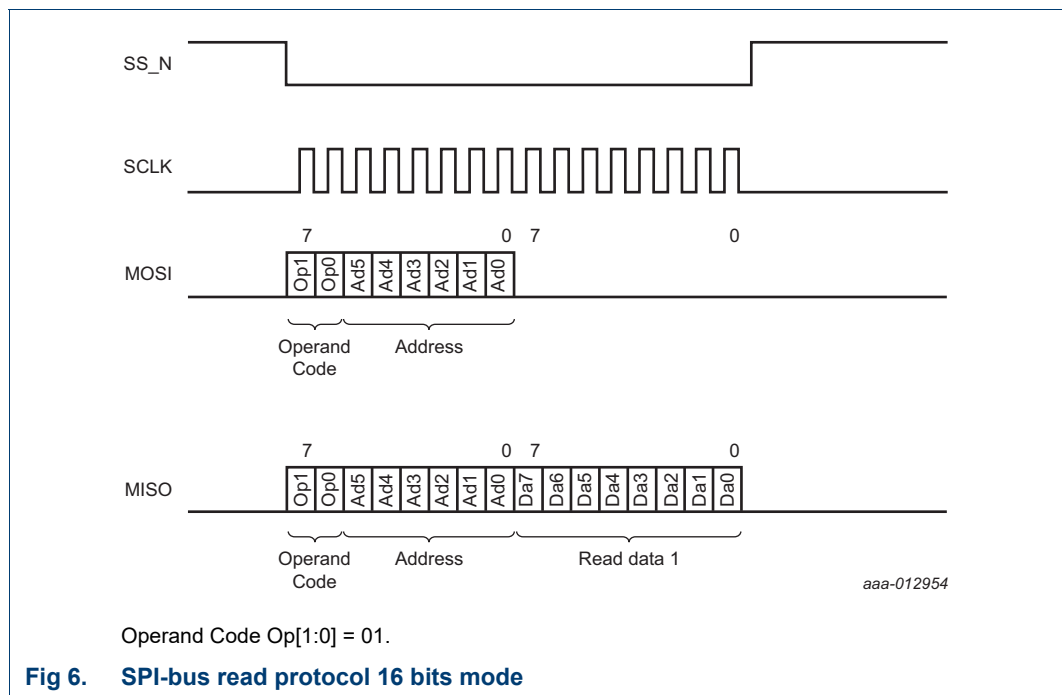
Operand Code Op[1:0] = 01.

**Fig 4. SPI-bus read protocol burst mode**

### 8.3.3 SPI-bus write protocol 16 bits frame



### 8.3.4 SPI-bus read protocol 16 bits mode



### 8.3.5 SPI-bus timings

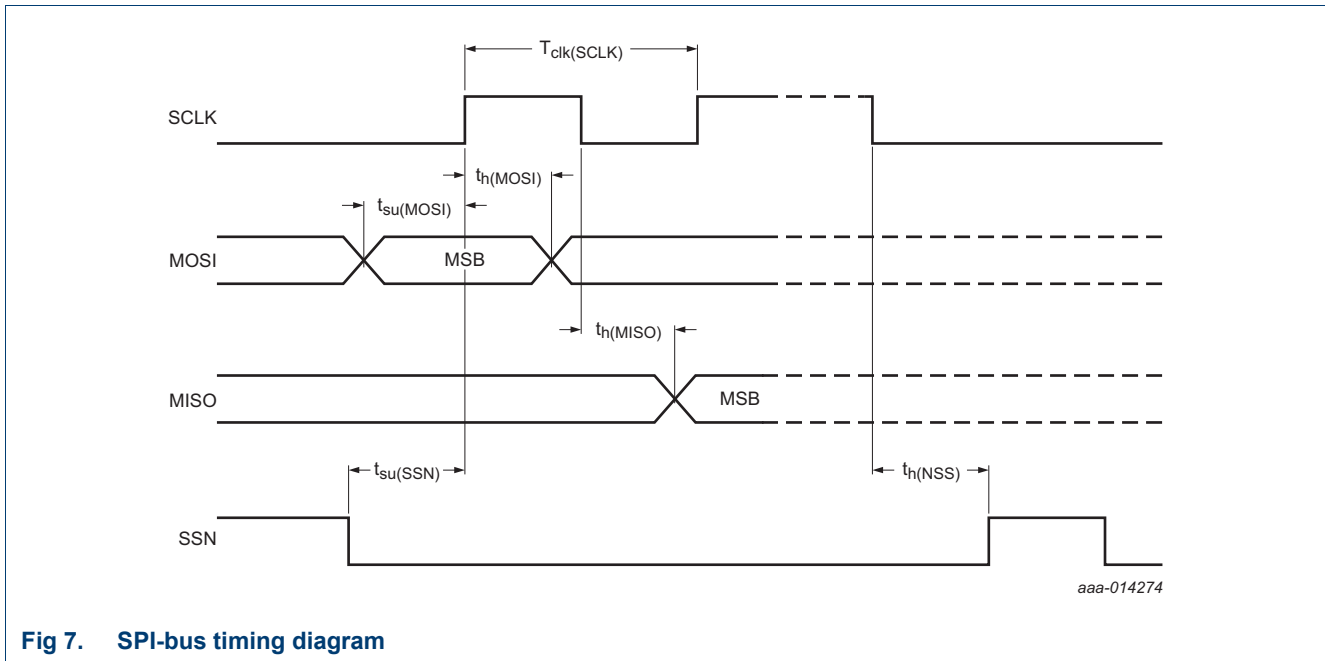


Fig 7. SPI-bus timing diagram

Table 4. SPI-bus timings specification

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{clk}(SCLK)$	clock period on pin SCLK		50	-	ns
$t_{su}(MOSI)$	MOSI set-up time		12	-	ns
$t_h(MOSI)$	MOSI hold time		0	-	ns
$t_h(MISO)$	MISO hold time		-	0	ns
$t_h(SSN)$	SSN hold time		0	-	ns
$t_{su}(SSN)$	SSN set-up time		12	-	ns

### 8.4 Temperature sensor

The temperature sensor indicates the junction temperature of the die via SPI-bus interface. This feature has been implemented to provide an indicator for the soldering process. If the exposed die pad is not properly soldered, the thermal dissipation is affected, leading to a junction temperature increase.

The sensor provides the junction temperature in the range from 22 °C to 127 °C.

## 9. Control interface

### 9.1 Register table description

Table 5. Register table description

Address (h)	Name	Bit						
		7	6	5	4	3	2	1
00	ID_1							MINOR_REV
01	POWER_STATUS_1	LO_Lock	MAJOR_REV[3:0]					
02	VCO_LOG	-	LO_forced_lock	adc_vtune[2:0]				
04	LO_CALIB_1	-	-		LO_calib_counter_1[5:0]			
05	LO_CALIB_2				LO_calib_counter_2[7:0]			
07	THERMO_1	-			TM_D [6:0]			
08	IRQ_status		-					VCO_Fr
09	IRQ_enable		-					VCO_Fre
0A	IRQ_clear		-					VCO_Fr
0B	IRQ_set		-					VCO_F
0C	THERMO_2		-					
0D	XT_OUT		-					
0E	XT_CAL_2	XT_In_Force	XT_Cal_Bypass	XT_cal_timer [1:0]				XT_Dac_For
0F	POWER_DOWN_1	pd_lotest	pd_Synthe	pd_adc_vtune	pd_rf_mpa	pd_rf_ppa	1	pd_data
10	POWER_DOWN_2		-				0	
11	POWER_SAVING_MODE_1		-					
12	RF_LO_DRIVER		-					
13	DAISY_CHAIN_1		-		lomux_to_daisy	0	1	
14	RF_PHASE_SHIFTER_1		rf_load_capa[3:0]					
15	RF_PHASE_SHIFTER_2				rf_phase_selector[7:0]			
16	RF_PHASE_SHIFTER_3		-					
19	RF_PPA_MPA_1		-					rf_mpa_power[5:0]
1A	RF_PPA_MPA_2			0	rf_mpa_bias_ctr[1:0]			
1B	LO_CHAIN	ckdiv2_reset	ckdiv2_start	ckdiv2_invert	PLL_Div2_Highfreq			LoChain_rati



Table 6. ID\_1 bit descriptions

Address	Register	Bit	Symbol	Access	Value (b)	Description
00	ID_1	7 to 4	MAJOR_REV[3:0]	R	0001	major revision of the IC
		3 to 0	MINOR_REV[3:0]	R	0000	minor revision of the IC

Table 7. POWER\_STATUS\_1 bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
01	POWER_STATUS_1	7	LO_Lock	R		PLL lock status indicator
					0	PLL unlocked
					1	PLL locked
		6	LO_forced_lock	R		forces PLL Lock bit if not present after 5 ms
					0	LO_lock_force not triggered (LO_lock was present before 5 ms)
					1	LO_lock_force triggered (LO_lock was not present before 5 ms)
		0	POR	R		Power-On Reset
					0	the chip supply voltage did not fall below the POR threshold voltage since the previous read operation of this bit
					1	the chip supply voltage fell below the POR threshold voltage (an HW reset has occurred). So the IC must be initialized before any further action. Reading this bit resets it

Table 8. VCO\_LOG bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
02	VCO_LOG	6 to 4	adc_vtune[2:0]	R		output value of ADC connected to Vtune
					0	0 V to 0.33 V
					1	0.33 V to 0.45 V
					2	0.45 V to 0.58 V
					3	0.58 V to 1.05 V
					4	1.05 V to 1.62 V
					5	1.62 V to 1.84 V
					6	1.84 V to 2.1 V
7	> 2.1 V					

Table 9. LO\_CALIB\_1 bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
04	LO_CALIB_1	5 to 0	LO_calib_counter_1[5:0]	R	[1]	current VCO frequency measurement result (MSB)

[1] VCO frequency measurement result (kHz) =  $125 / 16 \times \text{decimal}(\text{LO\_calib\_counter}[13:0])$ , with  $\text{LO\_calib\_counter}[13:0] = 2^8 \times \text{LO\_calib\_counter}_1[5:0] + \text{LO\_calib\_counter}_2[7:0]$ .

Table 10. LO\_CALIB\_2 bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
05	LO_CALIB_2	7 to 0	LO_calib_counter_2[7:0]	R	[1]	current VCO frequency measurement result (LSB)

[1] VCO frequency measurement result (kHz) =  $125 / 16 \times \text{decimal}(\text{LO\_calib\_counter}[13:0])$ , with  $\text{LO\_calib\_counter}[13:0] = 2^8 \times \text{LO\_calib\_counter\_1}[5:0] + \text{LO\_calib\_counter\_2}[7:0]$ .

Table 11. THERMO\_1 bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
07	THERMO_1	6 to 0	TM_D[6:0]	R		junction temperature measurement
					[000 0000: 001 0101]	junction temperature < 22 °C
					[001 0110: 111 1110]	22 °C ≤ junction temperature = decimal(TM_DA[6:0]) < 127 °C
					111 1111	junction temperature ≥ 127 °C

Table 12. IRQ\_status bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
08	IRQ_status	1	VCO_Freq_End	R		VCO frequency measurement end IRQ

Table 13. IRQ\_enable bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
09	IRQ_enable	1	VCO_Freq_Enable	RW		VCO frequency measurement IRQ enable

Table 14. IRQ\_clear bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
0A	IRQ_clear	1	VCO_Freq_Clear	RW		VCO frequency measurement IRQ clear

Table 15. IRQ\_set bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
0B	IRQ_set	1	VCO_Freq_Set	RW		VCO frequency measurement IRQ set

Table 16. THERMO\_2 bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
0C	THERMO_2	0	TM_ON	RW		temperature sensor ON or OFF
					0	disable the temperature sensor
					1	enable the temperature sensor

Table 17. XT\_CAL\_2 bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description	
0E	XT_CAL_2	7	XT_In_Force	RW		Xtal oscillator Master/Slave mode	
					0	Xtal Osc Master mode (forbidden)	
					1	Xtal Osc Slave mode (External 16MHz signal to be provided)	
		6	XT_Cal_Bypass	RW			allow bypass of the Xtal calibration value with XT_Dac_Force[3:0] from SPI-bus
					0	XT_Cal_Bypass OFF	
					1	XT_Cal bypassed with XT_Dac_Force value	
		5 to 4	XT_cal_timer[1:0]	RW			Xtal oscillator calibration timer selection
					0	5.12 ms	
					1	10.24 ms	
					2	20.48 ms	
		3 to 0	XT_Dac_Force[3:0]	RW		[0:15]	Xtal Osc Amplitude Control value

Table 18. POWER\_DOWN\_1 bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description		
0F	POWER_DOWN_1	7	pd_lotest	RW		LO test input buffer enable/disable		
					0	LO test buffer disabled		
					1	LO test buffer enabled		
		6	pd_Synthe	RW			PLL enable/disable (excluding LO Chain)	
					0	PLL disabled		
		5	pd_adc_vtune	RW			enables/disables the ADC connected on Vtune	
					0	ADC Vtune disabled		
		4	pd_rf_mpa	RW			MPA ON/OFF	
					0	MPA disabled		
		3	pd_rf_ppa	RW			Pre PA ON/OFF	
					0	Pre PA disabled		
		1	pd_rf_tx	RW			phase shifter ON/OFF	
					0	phase shifter disabled		
		0	pd_lochain	RW			LOCHAIN ON/OFF	
					0	LO Chain disabled		
							1	LO Chain enabled

Table 19. POWER\_DOWN\_2 bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
10	POWER_DOWN_2	1	pd_daisy_out	RW		daisy chaining output buffer enable/disable
					0	daisy output buffer disabled
					1	daisy output buffer enabled
		0	pd_daisy_in	RW		daisy chaining input buffer enable/disable
					0	daisy input buffer disabled
					1	daisy input buffer enabled

Table 20. DAISY\_CHAIN\_1 bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
13	DAISY_CHAIN_1	4	lomux_to_daisy	RW		allow LO signal to Daisy output buffer
					0	no signal to daisy output buffer
					1	allow LO to daisy output buffer

Table 21. RF\_PHASE\_SHIFTER\_1 bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
14	RF_PHASE_SHIFTER_1	7 to 4	rf_load_capa[7:4]	RW		RF phase shifter filtering capacitor
					1	ISM band from 2.4 GHz to 2.483 GHz
					5	ISM band from 902 MHz to 928 MHz
					10	ISM band from 433 MHz to 435 MHz

Table 22. RF\_PHASE\_SHIFTER\_2 bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
15	RF_PHASE_SHIFTER_2	7 to 0	rf_phase_selector[7:0]	RW	[0:255] <sup>[1]</sup>	RF phase shifter control; from 0° to 360° with 1.4° step

[1] Do not set the values 0, 64, 128 and 192.

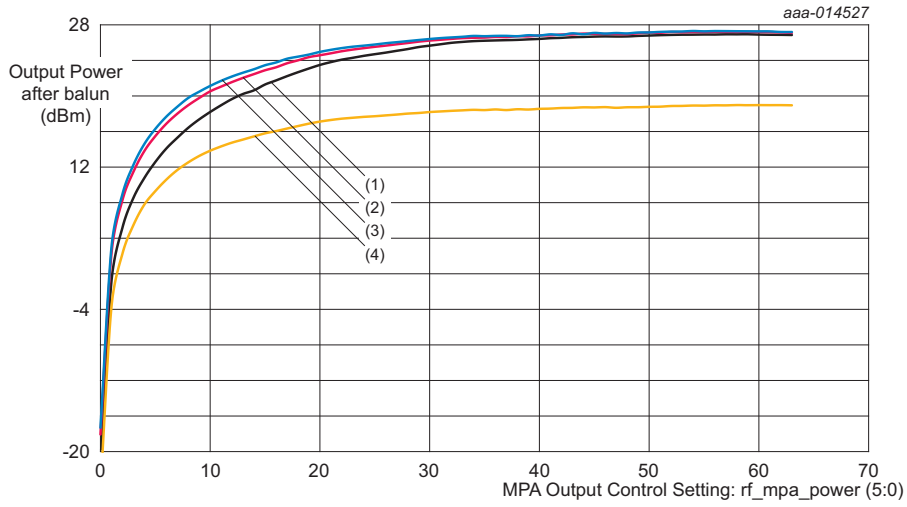
Table 23. RF\_PPA\_MPA\_1 bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
19	RF_PPA_MPA_1	5 to 0	rf_mpa_power[5:0]	RW		MPA/PPA output power control
					0	do not use
					from 1 to 62	<sup>[1]</sup>
					63	<sup>[2]/[3]</sup>

[1] See [Figure 8](#).

[2] See [Table 37](#) for P<sub>o(max)</sub> in MPA.

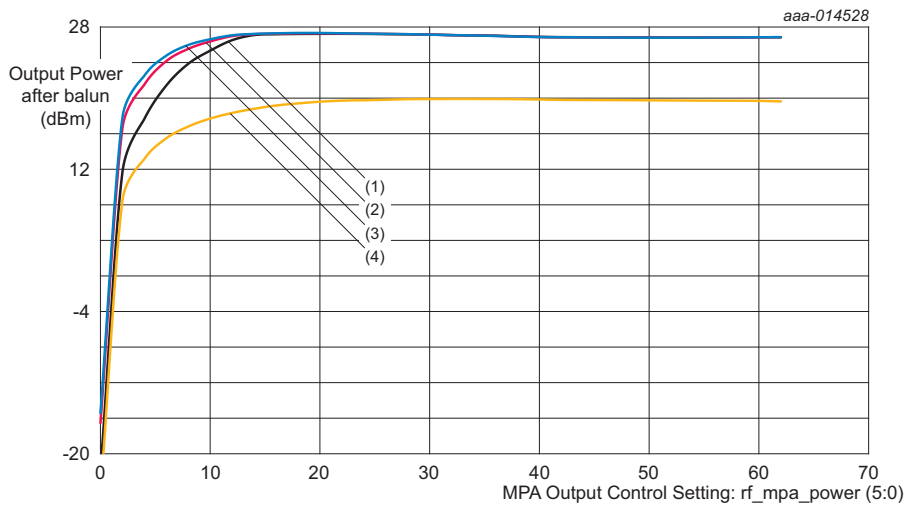
[3] See [Table 37](#) for P<sub>o(max)</sub> in PPA.



- (1) MPA\_bias\_ctrl = 0.
- (2) MPA\_bias\_ctrl = 1.
- (3) MPA\_bias\_ctrl = 2.
- (4) MPA\_bias\_ctrl = 3.

V<sub>DD</sub> = 3.3 V.  
 t<sub>amb</sub> = 25 °C.

**Fig 8. MPA output power at 2.4 GHz (typical)**



- (1) MPA\_bias\_ctrl = 0.
- (2) MPA\_bias\_ctrl = 1.
- (3) MPA\_bias\_ctrl = 2.
- (4) MPA\_bias\_ctrl = 3.

V<sub>DD</sub> = 3.3 V.  
 t<sub>amb</sub> = 25 °C.

**Fig 9. MPA output power at 915 MHz (typical)**

Table 24. RF\_PPA\_MPA\_2 bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
1A	RF_PPA_MPA_2	3 to 2	rf_mpa_bias_ctrl[1:0]	RW		MPA first and second stage bias current control
					0	+27 dBm / 150 $\mu$ A / 300 $\mu$ A
					1	+27 dBm / 200 $\mu$ A / 400 $\mu$ A
					2	+27 dBm / 250 $\mu$ A / 500 $\mu$ A
					3	+21 dBm / 150 $\mu$ A / 300 $\mu$ A

Table 25. LO\_CHAIN bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description	
1B	LO_CHAIN	7	ckdiv2_reset	RW		force reset of phase shifter div2 (used to synchronize Generator and Daisy)	
					0	div2 running	
					1	div2 output frozen	
		6	ckdiv2_start	RW			allow clock to IQ div2. Used to synchronize Generator and Daisy
					0	no clock to IQ div2	
					1	clock to IQ div2 allowed	
		5	ckdiv2_invert	RW			phase selection of clock to IQ div2 (0°/180°). Used to synchronize Generator and Daisy.
					0	clock phase = 0°	
					1	clock phase = 180°	
		4	PLL_Div2_Highfreq	RW			PLL Div 2 HIGH frequency biasing current
					0	biasing to be used for ISM bands 433 MHz and 915 MHz	
					1	biasing to be used for ISM band 2450 MHz	
		3 to 0	LoChain_ratio[3:0]	RW			Lo divider ratio
					0	2 used for ISM band 2450 MHz	
					1	do not use	
2	4 used for ISM band 915 MHz						
3	do not use						
4	do not use						
5	do not use						
6	do not use						
7	do not use						
8	8 used for ISM band 433 MHz						
9	do not use						
10	do not use						
11	do not use						
12	do not use						
13	do not use						
14	do not use						
15	daisy in						

Table 26. SD\_1 bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
1C	SD_1	6 to 0	LO_Int[7:0]	RW	[0:255]	PLL integer part N

Table 27. SD\_2 bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
1D	SD_2	7 to 0	LO_Frac_2[7:0]	RW	[0:127]	PLL $\Sigma\Delta$ modulator byte 2 corresponds to K[15:8]

Table 28. SD\_3 bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
1E	SD_3	7 to 0	LO_Frac_1[7:0]	RW	[0:255]	PLL $\Sigma\Delta$ modulator byte 1 corresponds to K[22:9]

Table 29. CP bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
1F	CP	6	ICP_Force_Sink	RW		enable/disable charge-pump forced sinking current
					0	no action
					1	charge pump forced to sink current
		5	ICP_Force_Src	RW		enable/disable charge-pump forced sourcing current
					0	no action
					1	charge pump forced to source current
		4	cpleak0	RW		charge-pump offset current ON/OFF
					0	charge-pump offset current enabled
					1	charge-pump offset current disabled
		3	cpleak05	RW		proportional CP offset current
					0	10 % offset current
					1	5 % offset current

Table 30. VCO bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
21	VCO	1 to 0	VCO_Select[1:0]	RW		VCO selection
					0	all OFF
					1	forbidden
					2	VCO MID
					3	VCO HIGH

Table 31. RESERVED\_0 bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
3E	RESERVED_0	4 to 0	reserved_0[4:0]	RW	-	POR bit control

Table 32. RESERVED\_1 bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
3E	RESERVED_1	4 to 0	reserved_1[1:0]	RW	-	page selection; default page = 0; page 1 used only for debug

## 10. Limiting values

**Table 33. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.3	+3.6	V
V <sub>I</sub>	input voltage	V <sub>CC</sub> < 3.3 V	-0.3	V <sub>CC</sub> + 0.3	V
		V <sub>CC</sub> > 3.3 V	-0.3	+3.6	V
T <sub>stg</sub>	storage temperature		-40	+150	°C
T <sub>j</sub>	junction temperature		-	105	°C
T <sub>amb</sub>	ambient temperature		-20	+85 <sup>[1]</sup>	°C
V <sub>ESD</sub>	electrostatic discharge voltage	EIA/JESD22-A114 (HBM)	-2	+2	kV
		EIA/JESD22-C101-C (FCDM) class III <sup>[2]</sup>	500	-	V

[1] The maximum allowed ambient temperature T<sub>amb(max)</sub> depends on the assembly conditions of the package and especially on the design of the Printed-Circuit Board (PCB) and die connection. The application mounting must be done in such a way that the maximum junction temperature is never exceeded. The junction temperature can be obtained by reading the temperature sensor bit via SPI-bus. The junction temperature: T<sub>j</sub> = T<sub>amb</sub> + ΔT<sub>j-c</sub>, where ΔT<sub>j-c</sub> = power × R<sub>th</sub>.

[2] Class III: > 500 V to 1000 V.

## 11. Thermal characteristics

**Table 34. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient		-	-	32.6	K/W

## 12. Characteristics

**Table 35. General characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		3.13	3.30	3.47	V
I <sub>CC</sub>	supply current	at 27 dBm output power; daisy chaining output buffer ON	-	450	-	mA
		with power amplifier OFF; V <sub>SWITCH</sub> = 0 V	-	120	-	mA
		in Standby mode	-	2.5	-	mA

**Table 36. Characteristics**

T<sub>amb</sub> = 25 °C; V<sub>dd</sub> = 3.3 V; for ISM bands: 433 MHz, 915 MHz and 2450 MHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Digital levels (SPI-bus)</b>						
f <sub>SPI_CLK(SCLK)</sub>	SPI_CLK frequency on pin SCLK		-	-	20	MHz
V <sub>IL</sub>	LOW-level input voltage		-	-	0.3V <sub>CC</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>CC</sub>	-	-	V

**Table 36. Characteristics ...continued**

$T_{amb} = 25\text{ °C}$ ;  $V_{dd} = 3.3\text{ V}$ ; for ISM bands: 433 MHz, 915 MHz and 2450 MHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OL}$	LOW-level output voltage		-	-	$0.3V_{CC}$	V
$V_{OH}$	HIGH-level output voltage		$0.7V_{CC}$	-	-	V
<b>PLL</b>						
$f_{step}$	step frequency		10	-	-	kHz
$f_{clk(ref)}$	reference clock frequency	external reference clock	-	16	-	MHz
$V_{clk(ref)}$	reference clock voltage	external reference clock	$0.7V_{CC}$	-	$V_{CC}$	V

**Table 37. Characteristics**

$T_{amb} = 25\text{ °C}$ ;  $V_{dd} = 3.3\text{ V}$ ; for ISM bands: 2450 MHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>PLL</b>						
$f_{range}$	frequency range		2400	-	2483.5	MHz
$t_{set}$	setting time		-	-	50	$\mu\text{s}$
$t_{s(f)}$	frequency settling time	from one frequency to another	-	5	10	$\mu\text{s}$
$\varphi_n$	phase noise	at 2483.5 MHz; at 100 kHz frequency offset	-	-87	-	dBc/Hz
<b>Phase shifter</b>						
$\Delta\varphi_{step}$	phase shift step		-	1.4	-	$^\circ$
$\varphi_{RF}$	RF phase	[1]	0	-	360	$^\circ$
$E_\varphi$	phase error	absolute value step size error	0	0.5	1	$^\circ$
		cumulative phase error	[2]	5	-	$^\circ$
<b>MPA</b>						
$P_{o(max)}$	maximum output power		-	24	27	dBm
$\alpha_{sp(ob)}$	out-band spurious attenuation	consider second and third harmonics only	-	-30	-	dBc
$P_{ob}$	out-band power	integrated power outside the band of interest; $f_{VCO(max)} = f_{range\ max} - 1\text{ MHz}$ ; $f_{VCO(min)} = f_{range\ min} + 1\text{ MHz}$ ; $rf\_mpa\_power[5:0] = 42$	-	-45	-	dBc
$P_{o(range)}$	output power range		-	20	-	dB
$\alpha_{isol}$	isolation	ON/OFF switch isolation	-	40	-	dB
$t_{sw}$	switching time	OFF/ON ramping transition	[3]	700	-	ns
$Z_o$	output impedance		-	40	-	$\Omega$
<b>PPA</b>						
$P_{o(max)}$	maximum output power	$rf\_mpa\_power[5:0] = 63$	-	7	-	dBm
$P_o$	output power	$rf\_mpa\_power[5:0] = 42$	-	5	-	dBm
$P_{o(range)}$	output power range		-	30	-	dB
$Z_o$	output impedance		-	200	-	$\Omega$

[1] Phase range =  $360^\circ$  (maximum phase  $\varphi_{RF} = 360^\circ$  minus minimum phase  $\varphi_{RF} = 0^\circ$ ).

[2] See [Figure 10](#).

[3] See [Figure 11](#).

**Table 38. Characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $V_{dd} = 3.3\text{ V}$ ; for ISM bands: 915 MHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>PLL</b>						
$f_{range}$	frequency range		902	-	928	MHz
$t_{set}$	setting time		-	-	50	$\mu\text{s}$
$t_{s(f)}$	frequency settling time	from one frequency to another	-	5	10	$\mu\text{s}$
<b>Phase shifter</b>						
$\Delta\phi_{step}$	phase shift step		-	1.4	-	$^{\circ}$
$\phi_{RF}$	RF phase		[1] 0	-	360	$^{\circ}$
$E_{\phi}$	phase error	absolute value step size error	0	0.5	1	$^{\circ}$
		cumulative phase error [2]	-	5	-	$^{\circ}$
<b>MPA</b>						
$P_{o(max)}$	maximum output power		-	24	27	dBm
$P_{o(range)}$	output power range		-	20	-	dB
$\alpha_{isol}$	isolation	ON/OFF switch isolation	-	40	-	dB
$t_{sw}$	switching time	OFF/ON ramping transition [3]	-	700	-	ns
$Z_o$	output impedance		-	40	-	$\Omega$
<b>PPA</b>						
$P_{o(max)}$	maximum output power	rf_mpa_power[5:0] = 63	-	7	-	dBm
$P_o$	output power	rf_mpa_power[5:0] = 42	-	5	-	dBm
$P_{o(range)}$	output power range		-	30	-	dB
$Z_o$	output impedance		-	200	-	$\Omega$

[1] Phase range =  $360^{\circ}$  (maximum phase  $\phi_{RF} = 360^{\circ}$  minus minimum phase  $\phi_{RF} = 0^{\circ}$ ).

[2] See [Figure 10](#).

[3] See [Figure 11](#).

**Table 39. Characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $V_{dd} = 3.3\text{ V}$ ; for ISM bands: 433 MHz; unless otherwise specified.

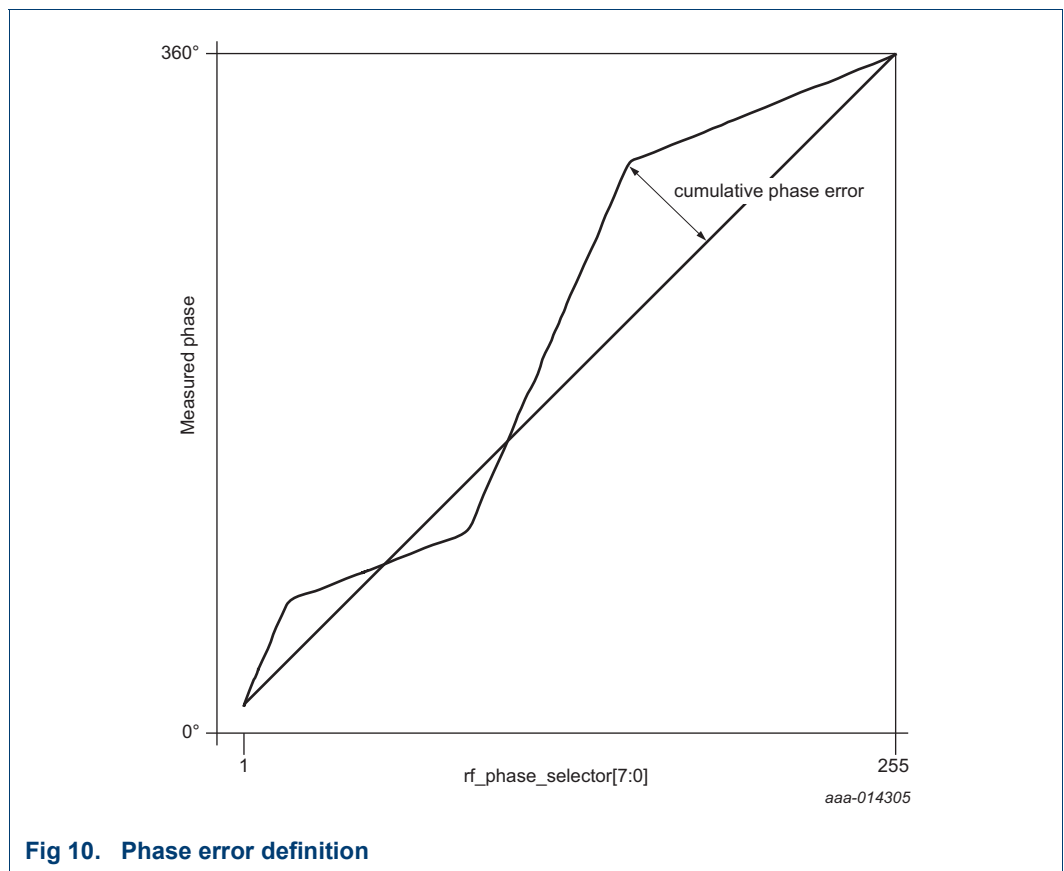
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>PLL</b>						
$f_{range}$	frequency range		433.0	-	434.8	MHz
$t_{set}$	setting time		-	-	50	$\mu\text{s}$
$t_{s(f)}$	frequency settling time	from one frequency to another	-	5	10	$\mu\text{s}$
<b>MPA</b>						
$P_{o(max)}$	maximum output power		-	24	27	dBm
$P_{o(range)}$	output power range		-	20	-	dB
$\alpha_{isol}$	isolation	ON/OFF switch isolation	-	40	-	dB
$t_{sw}$	switching time	OFF/ON ramping transition [1]	-	700	-	ns

**Table 39. Characteristics ...continued**

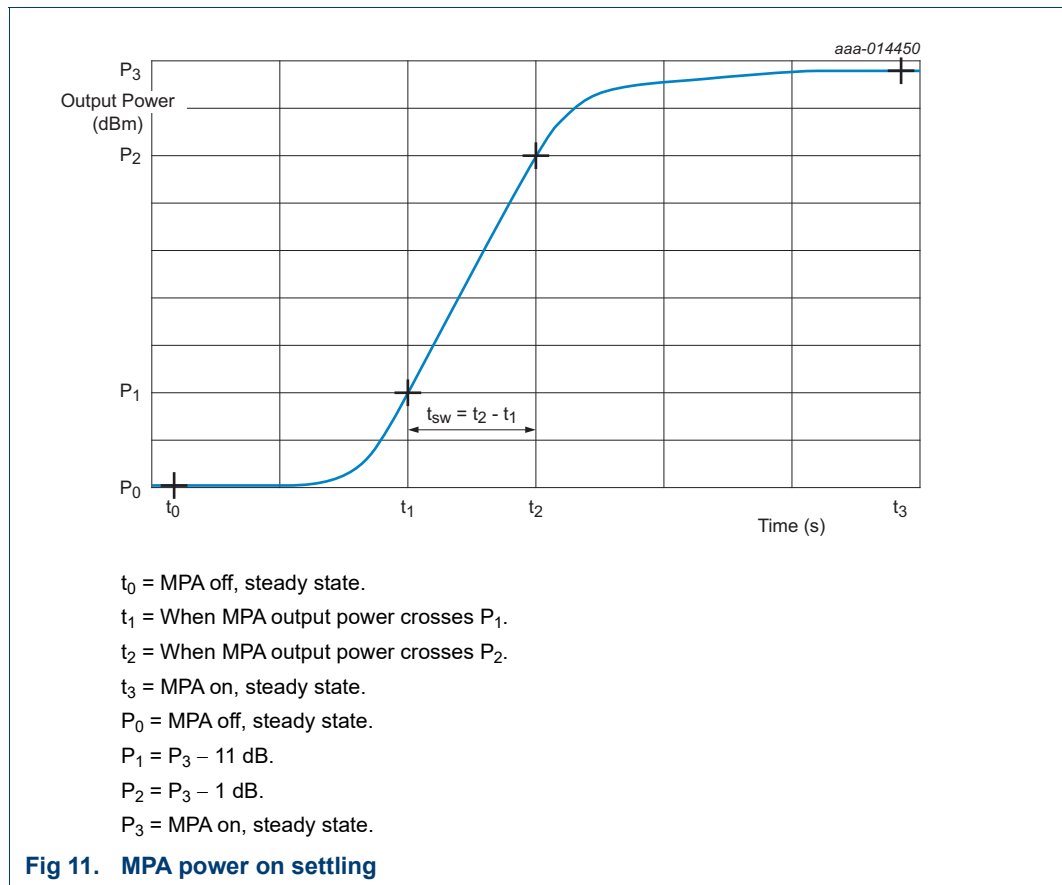
$T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $V_{dd} = 3.3\text{ V}$ ; for ISM bands: 433 MHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Z_o$	output impedance		-	40	-	$\Omega$
<b>PPA</b>						
$P_{o(max)}$	maximum output power	rf_mpa_power[5:0] = 63	-	7	-	dBm
$P_o$	output power	rf_mpa_power[5:0] = 42	-	5	-	dBm
$P_{o(range)}$	output power range		-	30	-	dB
$Z_o$	output impedance		-	200	-	$\Omega$

[1] See [Figure 11](#).

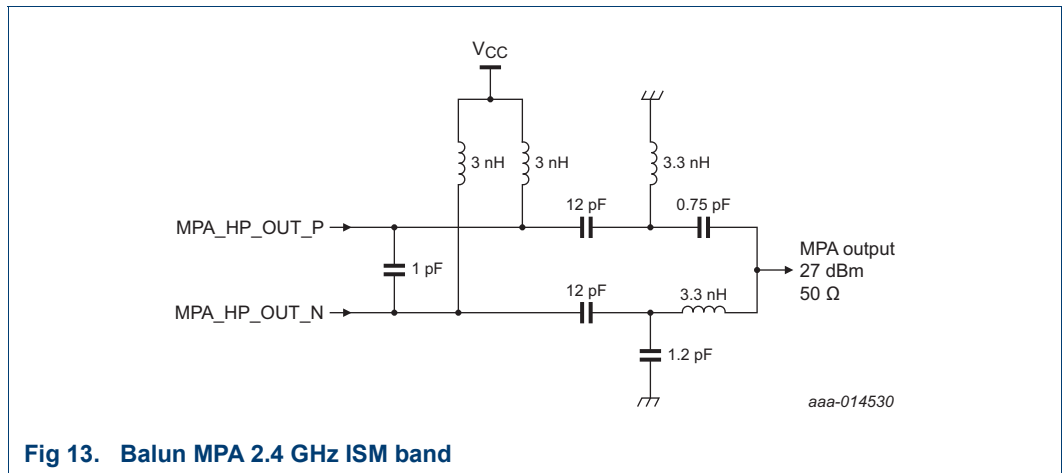
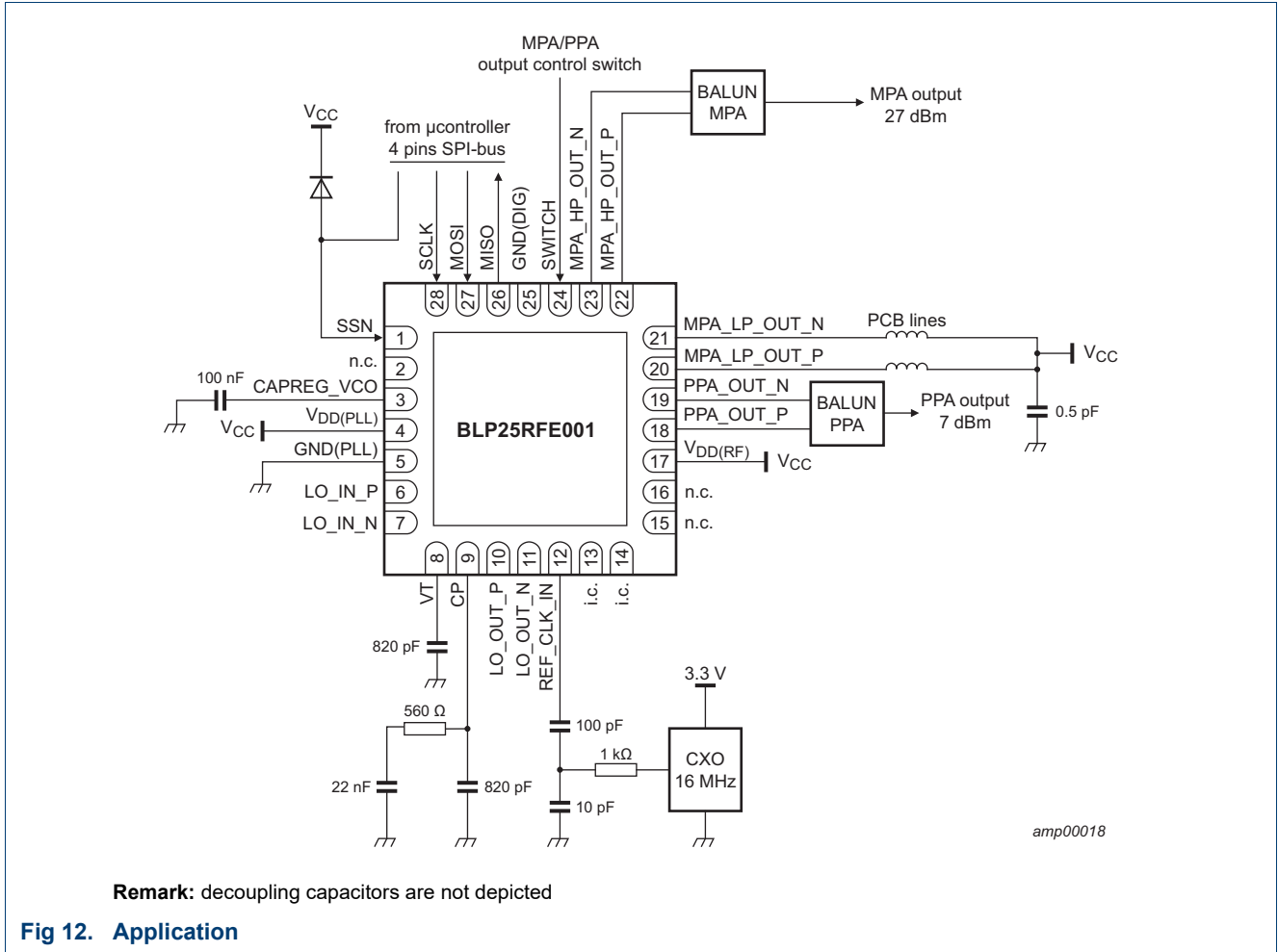


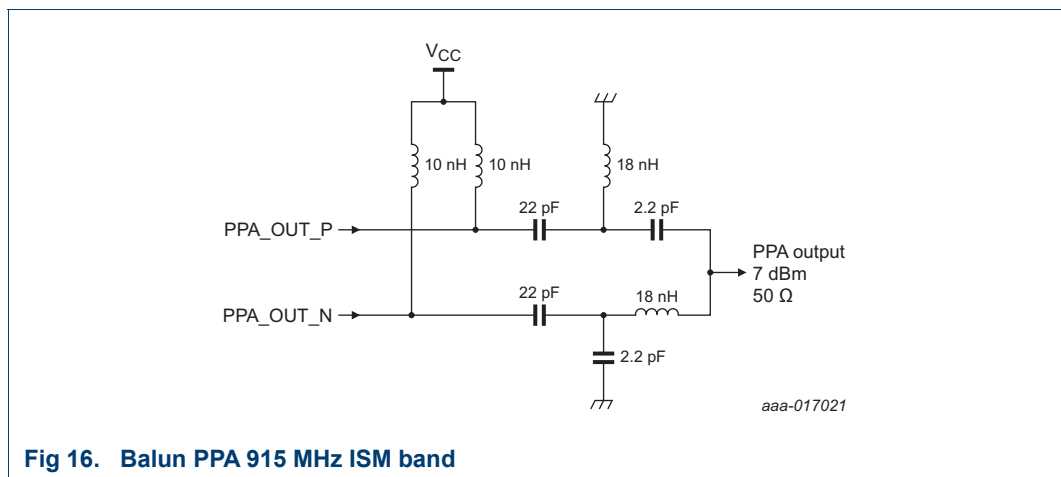
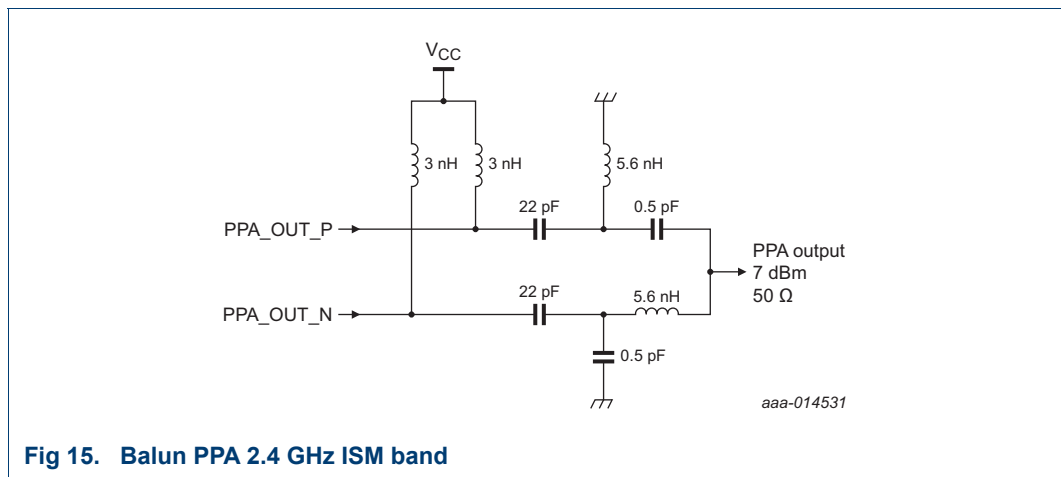
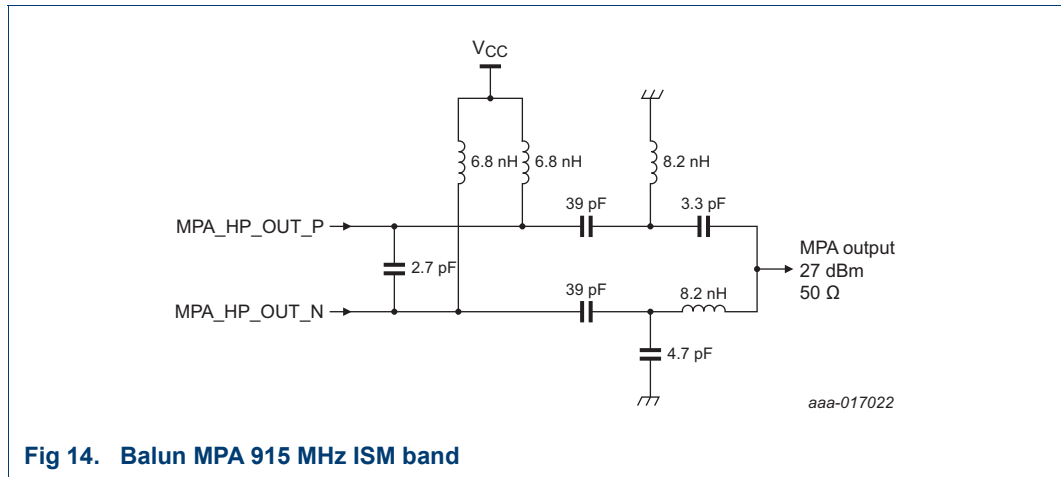
**Fig 10. Phase error definition**



### 13. Application information

#### 13.1 Application





13.2 Typical cooking application

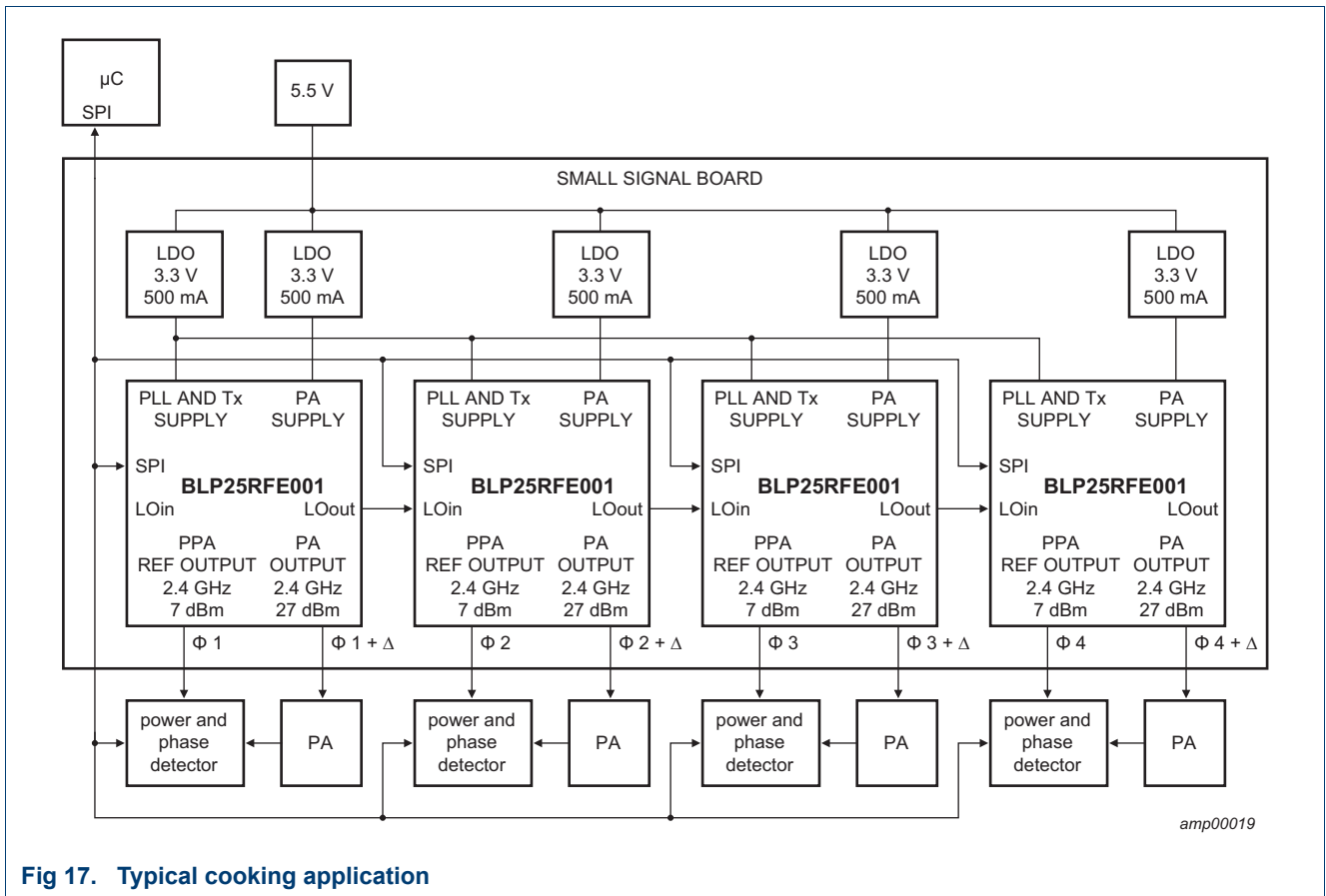


Fig 17. Typical cooking application

13.3 Typical lighting application

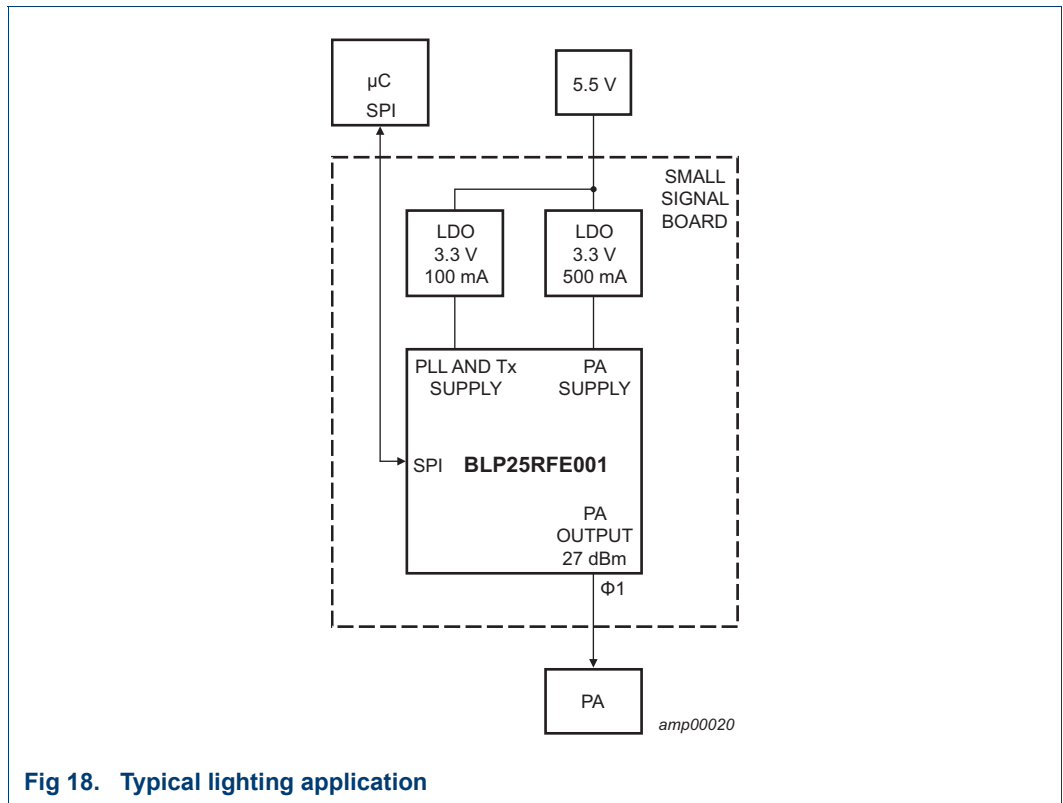


Fig 18. Typical lighting application

### 14. Package outline

HVQFN28: plastic thermal enhanced very thin quad flat package; no leads; 28 terminals; body 5 x 5 x 0.85 mm

SOT993-3

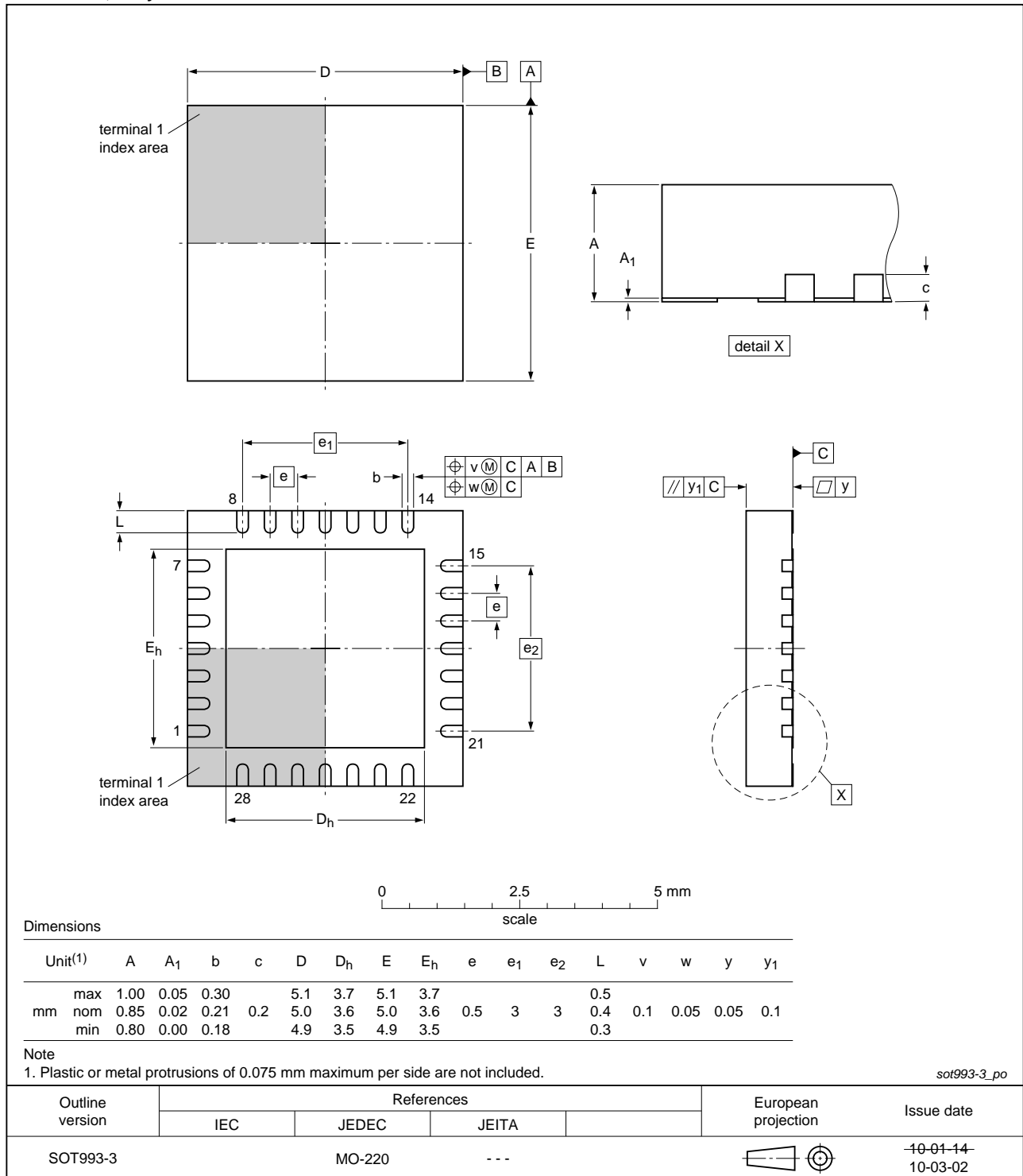


Fig 19. Package outline SOT993-3 (HVQFN28)

## 15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 20](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 40](#) and [41](#)

**Table 40. SnPb eutectic process (from J-STD-020D)**

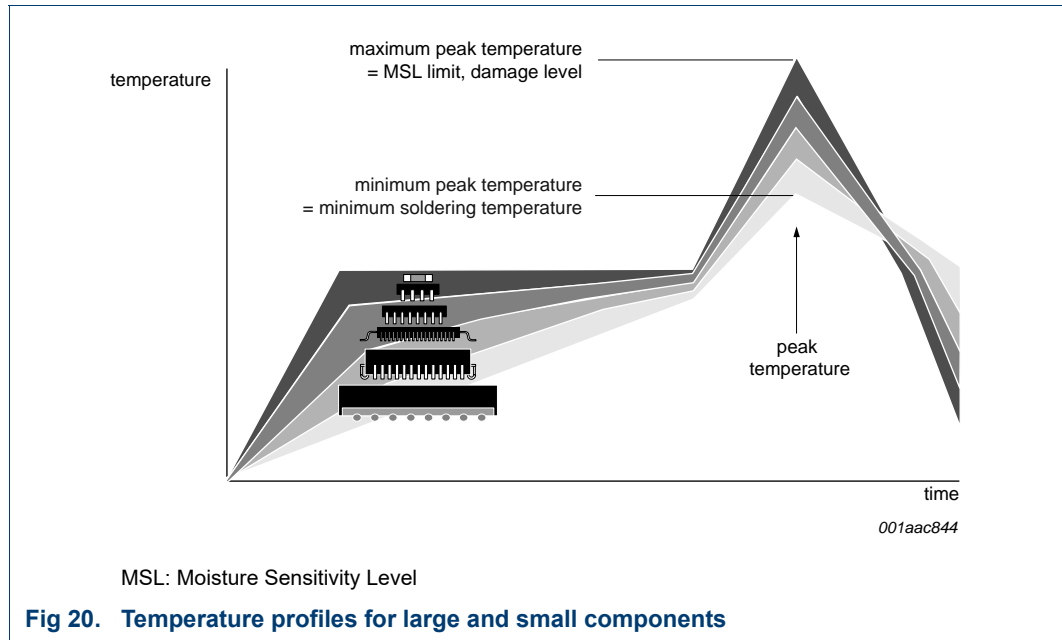
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 41. Lead-free process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 20](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 16. Abbreviations

Table 42. Abbreviations

Acronym	Description
BOM	Bill Of Material
FCDM	Field-induced Charge Device Model
IC	Integrated Circuit
ISM	Industrial Scientific Medical
LC-VCO	Inductors and Capacitors - Voltage Controlled Oscillator
LO	Local Oscillator
LSB	Least Significant Bit
MainDiv	Main Divider
MPA	Medium Power Amplifier
MSB	Most Significant Bit
MSL	Moisture Sensibility Level
PA	Power Amplifier
PCB	Printed-Circuit Board
PFD	Phase Frequency Detector
PLL	Phase-Locked Loop
PPA	Pre-Power Amplifier
PWM	Pulse Width Modulation
RoHS	Restriction of Hazardous Substances

## 17. Revision history

Table 43. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP25RFE001 v.2	20180126	Product data sheet	-	BLP25RFE001 v.1.0
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 2 on page 1</a>: changed text of list item 8</li> <li>• <a href="#">Section 8 on page 5</a>: changed text of paragraph 7</li> <li>• <a href="#">Section 8.1 on page 5</a>: changed text of third sentence</li> <li>• <a href="#">Table 37 on page 22</a>: changed values of maximum output power MPA</li> <li>• <a href="#">Table 38 on page 23</a>: changed values of maximum output power MPA</li> <li>• <a href="#">Table 39 on page 23</a>: changed values of maximum output power MPA</li> </ul>			
BLP25RFE001 v.1.0	20180109	Product data sheet	-	-

## 18. Legal information

### 18.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.ampleon.com>.

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## 20. Tables

Table 1. Ordering information . . . . .	2	Table 23. RF_PPA_MPA_1 bit descriptions . . . . .	16
Table 2. Marking codes . . . . .	2	Table 24. RF_PPA_MPA_2 bit descriptions . . . . .	18
Table 3. BLP25RFE001 pin description . . . . .	4	Table 25. LO_CHAIN bit descriptions . . . . .	19
Table 4. SPI-bus timings specification . . . . .	10	Table 26. SD_1 bit descriptions . . . . .	19
Table 5. Register table description . . . . .	11	Table 27. SD_2 bit descriptions . . . . .	20
Table 6. ID_1 bit descriptions . . . . .	13	Table 28. SD_3 bit descriptions . . . . .	20
Table 7. POWER_STATUS_1 bit descriptions . . . . .	13	Table 29. CP bit descriptions . . . . .	20
Table 8. VCO_LOG bit descriptions . . . . .	13	Table 30. VCO bit descriptions . . . . .	20
Table 9. LO_CALIB_1 bit descriptions . . . . .	13	Table 31. RESERVED_0 bit descriptions . . . . .	20
Table 10. LO_CALIB_2 bit descriptions . . . . .	14	Table 32. RESERVED_1 bit descriptions . . . . .	20
Table 11. THERMO_1 bit descriptions . . . . .	14	Table 33. Limiting values . . . . .	21
Table 12. IRQ_status bit descriptions . . . . .	14	Table 34. Thermal characteristics . . . . .	21
Table 13. IRQ_enable bit descriptions . . . . .	14	Table 35. General characteristics . . . . .	21
Table 14. IRQ_clear bit descriptions . . . . .	14	Table 36. Characteristics . . . . .	21
Table 15. IRQ_set bit descriptions . . . . .	14	Table 37. Characteristics . . . . .	22
Table 16. THERMO_2 bit descriptions . . . . .	14	Table 38. Characteristics . . . . .	23
Table 17. XT_CAL_2 bit descriptions . . . . .	15	Table 39. Characteristics . . . . .	23
Table 18. POWER_DOWN_1 bit descriptions . . . . .	15	Table 40. SnPb eutectic process (from J-STD-020D) . . . . .	32
Table 19. POWER_DOWN_2 bit descriptions . . . . .	16	Table 41. Lead-free process (from J-STD-020D) . . . . .	32
Table 20. DAISY_CHAIN_1 bit descriptions . . . . .	16	Table 42. Abbreviations . . . . .	33
Table 21. RF_PHASE_SHIFTER_1 bit descriptions . . . . .	16	Table 43. Revision history . . . . .	34
Table 22. RF_PHASE_SHIFTER_2 bit descriptions . . . . .	16		

## 21. Figures

Fig 1. Block diagram . . . . .	3
Fig 2. Pin configuration . . . . .	4
Fig 3. SPI-bus write protocol burst mode . . . . .	7
Fig 4. SPI-bus read protocol burst mode . . . . .	8
Fig 5. SPI-bus write protocol 16 bits frame . . . . .	9
Fig 6. SPI-bus read protocol 16 bits mode . . . . .	9
Fig 7. SPI-bus timing diagram . . . . .	10
Fig 8. MPA output power at 2.4 GHz (typical) . . . . .	17
Fig 9. MPA output power at 915 MHz (typical) . . . . .	17
Fig 10. Phase error definition . . . . .	24
Fig 11. MPA power on settling . . . . .	25
Fig 12. Application . . . . .	26
Fig 13. Balun MPA 2.4 GHz ISM band . . . . .	26
Fig 14. Balun MPA 915 MHz ISM band . . . . .	27
Fig 15. Balun PPA 2.4 GHz ISM band . . . . .	27
Fig 16. Balun PPA 915 MHz ISM band . . . . .	27
Fig 17. Typical cooking application . . . . .	28
Fig 18. Typical lighting application . . . . .	29
Fig 19. Package outline SOT993-3 (HVQFN28) . . . . .	30
Fig 20. Temperature profiles for large and small components . . . . .	33

**22. Contents**

<b>1</b>	<b>General description</b> . . . . .	<b>1</b>	<b>22</b>	<b>Contents</b> . . . . .	<b>38</b>
<b>2</b>	<b>Features and benefits</b> . . . . .	<b>1</b>			
<b>3</b>	<b>Applications</b> . . . . .	<b>1</b>			
<b>4</b>	<b>Ordering information</b> . . . . .	<b>2</b>			
<b>5</b>	<b>Marking</b> . . . . .	<b>2</b>			
<b>6</b>	<b>Block diagram</b> . . . . .	<b>3</b>			
<b>7</b>	<b>Pinning information</b> . . . . .	<b>4</b>			
7.1	Pinning . . . . .	4			
7.2	Pin description . . . . .	4			
<b>8</b>	<b>Functional description</b> . . . . .	<b>5</b>			
8.1	Medium Power Amplifier (MPA) . . . . .	5			
8.2	Low-Power Amplifier (PPA) . . . . .	6			
8.3	SPI-bus interface . . . . .	6			
8.3.1	SPI-bus write protocol burst mode . . . . .	7			
8.3.2	SPI-bus read protocol burst mode . . . . .	8			
8.3.3	SPI-bus write protocol 16 bits frame . . . . .	9			
8.3.4	SPI-bus read protocol 16 bits mode . . . . .	9			
8.3.5	SPI-bus timings . . . . .	10			
8.4	Temperature sensor . . . . .	10			
<b>9</b>	<b>Control interface</b> . . . . .	<b>11</b>			
9.1	Register table description . . . . .	11			
<b>10</b>	<b>Limiting values</b> . . . . .	<b>21</b>			
<b>11</b>	<b>Thermal characteristics</b> . . . . .	<b>21</b>			
<b>12</b>	<b>Characteristics</b> . . . . .	<b>21</b>			
<b>13</b>	<b>Application information</b> . . . . .	<b>26</b>			
13.1	Application . . . . .	26			
13.2	Typical cooking application . . . . .	28			
13.3	Typical lighting application . . . . .	29			
<b>14</b>	<b>Package outline</b> . . . . .	<b>30</b>			
<b>15</b>	<b>Soldering of SMD packages</b> . . . . .	<b>31</b>			
15.1	Introduction to soldering . . . . .	31			
15.2	Wave and reflow soldering . . . . .	31			
15.3	Wave soldering . . . . .	31			
15.4	Reflow soldering . . . . .	32			
<b>16</b>	<b>Abbreviations</b> . . . . .	<b>33</b>			
<b>17</b>	<b>Revision history</b> . . . . .	<b>34</b>			
<b>18</b>	<b>Legal information</b> . . . . .	<b>35</b>			
18.1	Data sheet status . . . . .	35			
18.2	Definitions . . . . .	35			
18.3	Disclaimers . . . . .	35			
18.4	Trademarks . . . . .	36			
<b>19</b>	<b>Contact information</b> . . . . .	<b>36</b>			
<b>20</b>	<b>Tables</b> . . . . .	<b>37</b>			
<b>21</b>	<b>Figures</b> . . . . .	<b>37</b>			

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