



**THE DATASHEET OF  
HEF4051BTT-Q100,11**



# HEF4051B-Q100

## 8-channel analog multiplexer/demultiplexer

Rev. 3 — 29 July 2021

Product data sheet

## 1. General description

The HEF4051B-Q100 is a single-pole octal-throw analog switch (SP8T) suitable for use in analog or digital 8:1 multiplexer/demultiplexer applications. The switch features three digital select inputs (S1, S2 and S3), eight independent inputs/outputs (Yn), a common input/output (Z) and a digital enable input (E). When E is HIGH, the switches are turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - MIL-STD-883C, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pf, R = 0 Ω)

## 3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

## 4. Ordering information

**Table 1. Ordering information**

All types operate from -40 °C to +125 °C.

Type number	Package		
	Name	Description	Version
HEF4051BT-Q100	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
HEF4051BTT-Q100	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Functional diagram

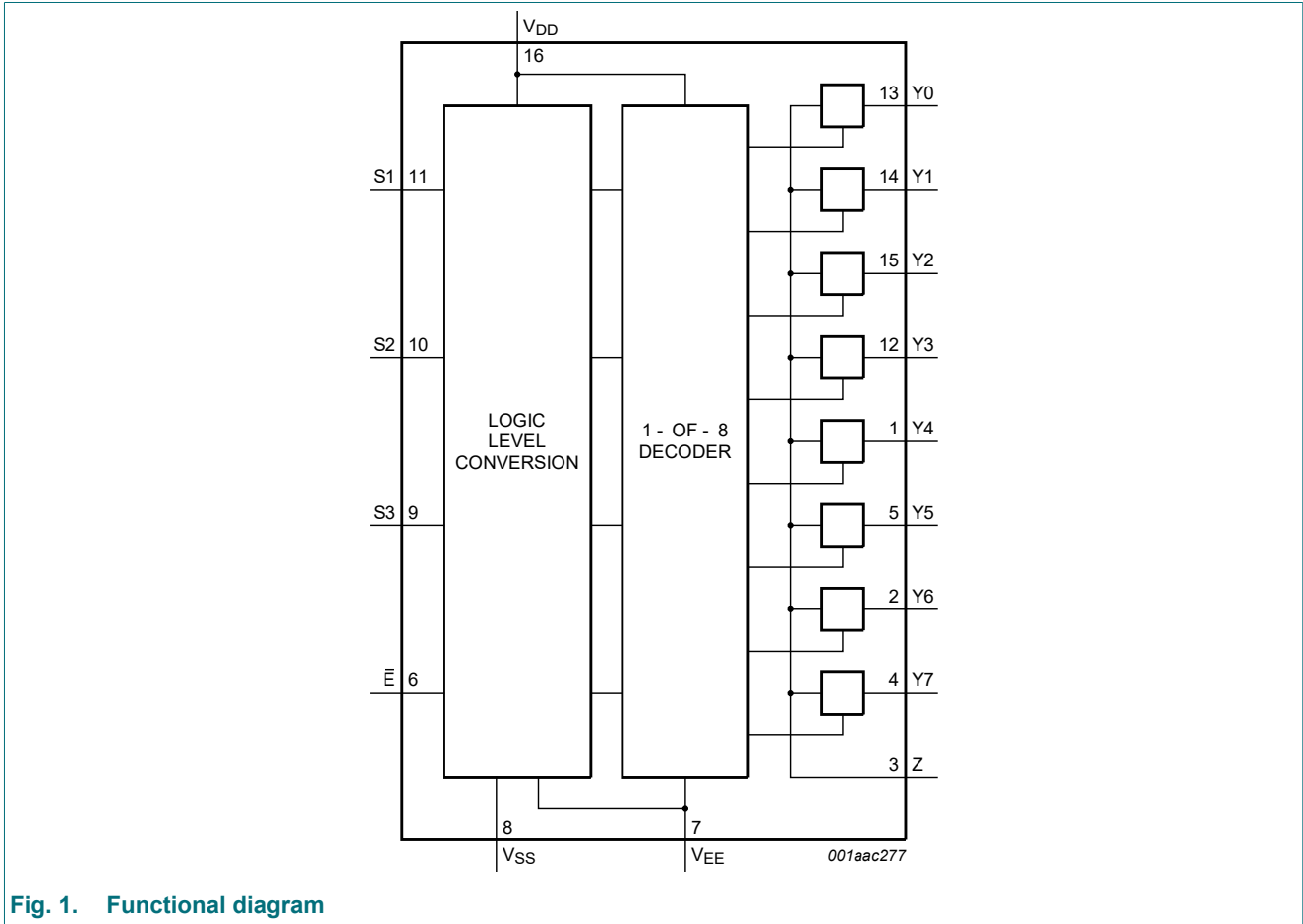


Fig. 1. Functional diagram

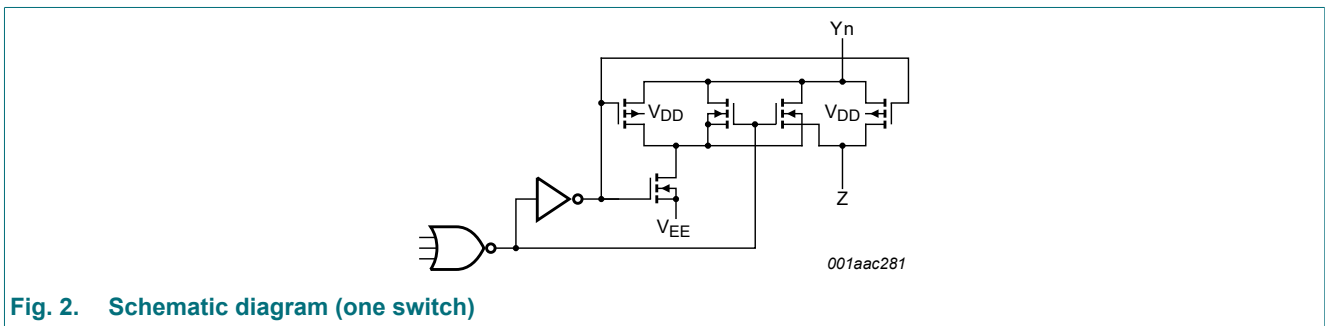


Fig. 2. Schematic diagram (one switch)

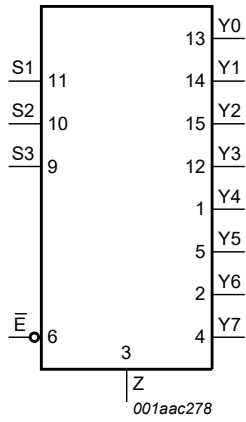


Fig. 3. Logic symbol

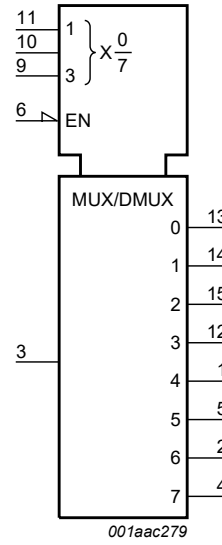


Fig. 4. IEC logic symbol

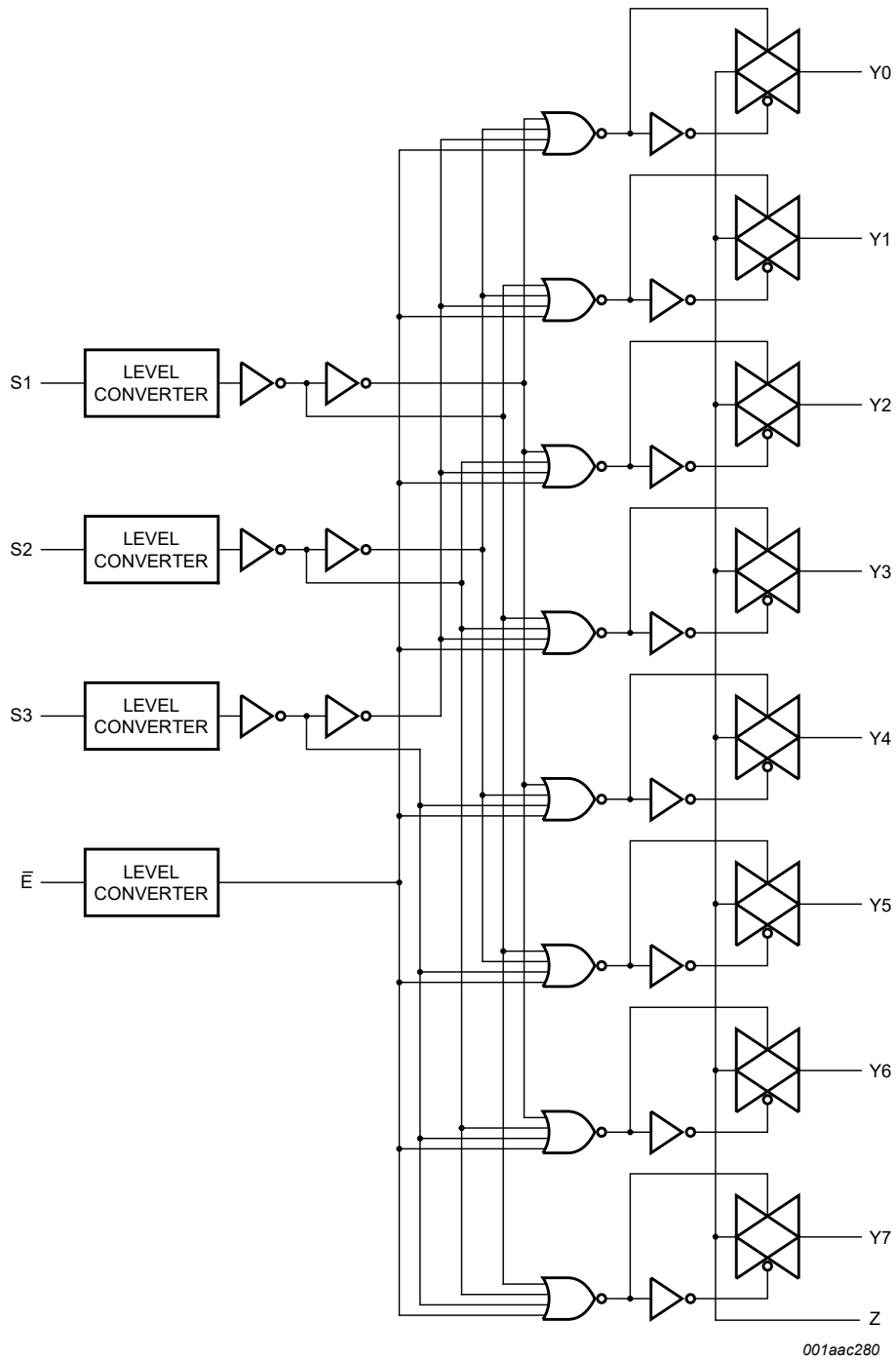


Fig. 5. Logic diagram

## 6. Pinning information

### 6.1. Pinning

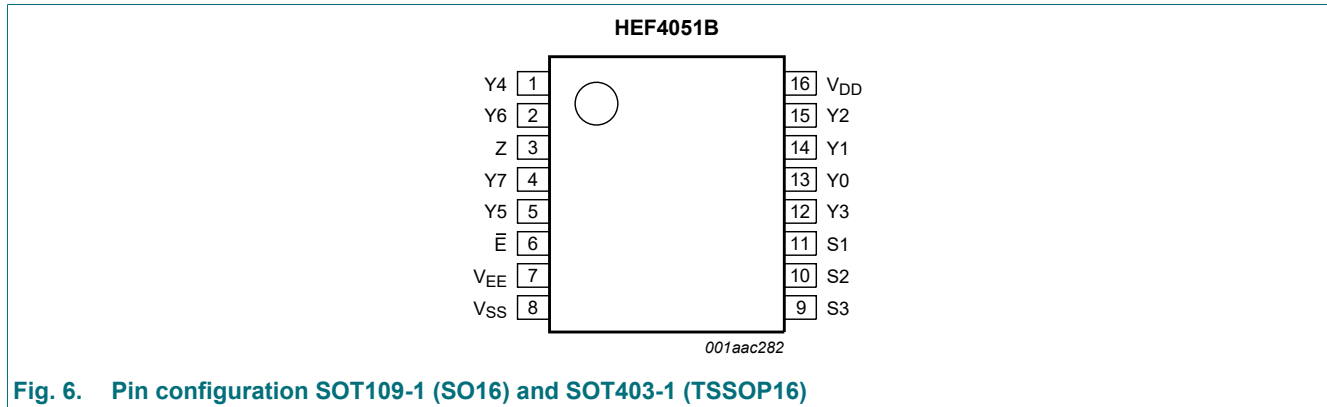


Fig. 6. Pin configuration SOT109-1 (SO16) and SOT403-1 (TSSOP16)

### 6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\bar{E}$	6	enable input (active LOW)
$V_{EE}$	7	supply voltage
$V_{SS}$	8	ground supply voltage
S1, S2, S3	11, 10, 9	select input
Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7	13, 14, 15, 12, 1, 5, 2, 4	independent input or output
Z	3	common output or input
$V_{DD}$	16	supply voltage

## 7. Functional description

Table 3. Function table

*H = HIGH voltage level; L = LOW voltage level; X = don't care.*

Input				Channel ON
$\bar{E}$	S3	S2	S1	
L	L	L	L	Y0 to Z
L	L	L	H	Y1 to Z
L	L	H	L	Y2 to Z
L	L	H	H	Y3 to Z
L	H	L	L	Y4 to Z
L	H	L	H	Y5 to Z
L	H	H	L	Y6 to Z
L	H	H	H	Y7 to Z
H	X	X	X	switches off

## 8. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to  $V_{SS} = 0\text{ V}$  (ground).

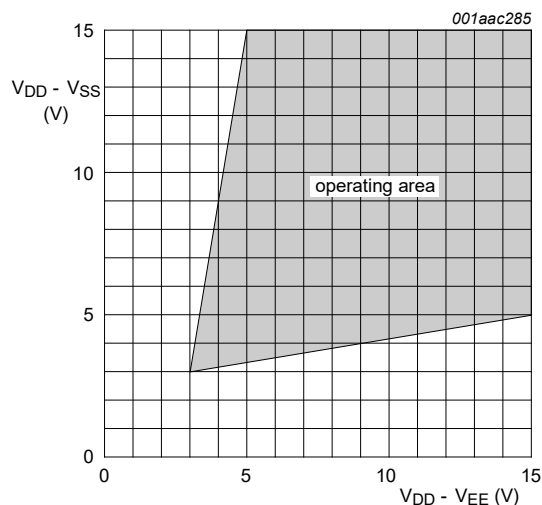
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$V_{EE}$	supply voltage	referenced to $V_{DD}$ [1]	-18	+0.5	V
$I_{IK}$	input clamping current	pins Sn and E; $V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{I/O}$	input/output current		-	$\pm 10$	mA
$I_{DD}$	supply current		-	50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+125	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2]	-	500	mW
$P$	power dissipation	per output	-	100	mW

- [1] To avoid drawing  $V_{DD}$  current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no  $V_{DD}$  current will flow out of terminals Y, and in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed  $V_{DD}$  or  $V_{EE}$ .
- [2] For SOT109-1 (SO16) package:  $P_{tot}$  derates linearly with 12.4 mW/K above 110 °C.  
For SOT403-1 (TSSOP16) package:  $P_{tot}$  derates linearly with 8.5 mW/K above 91 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage	see Fig. 7	3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$



**Fig. 7. Operating area as a function of the supply voltages**

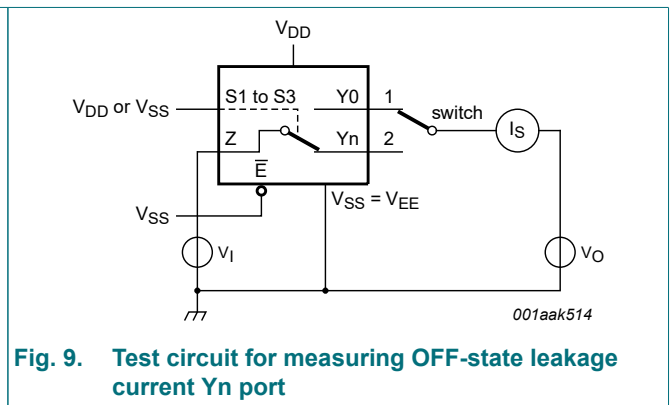
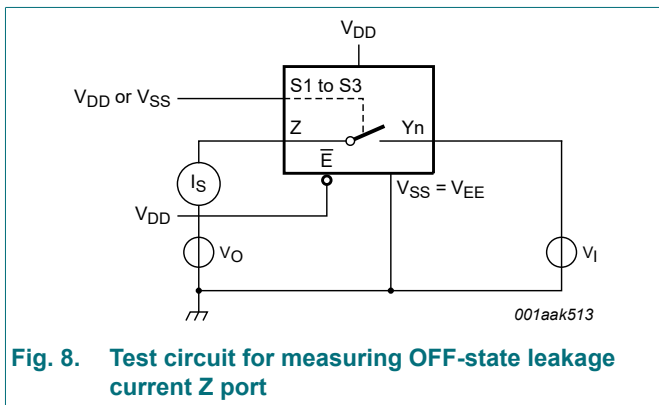
## 10. Static characteristics

**Table 6. Static characteristics**

$V_{SS} = V_{EE} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	V <sub>DD</sub>	T <sub>amb</sub> = -40 °C		T <sub>amb</sub> = 25 °C		T <sub>amb</sub> = 85 °C		T <sub>amb</sub> = 125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	I <sub>O</sub>   < 1 μA	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V <sub>IL</sub>	LOW-level input voltage	I <sub>O</sub>   < 1 μA	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
I <sub>I</sub>	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>S(OFF)</sub>	OFF-state leakage current	Z port; all channels OFF; see Fig. 8	15 V	-	-	-	1000	-	-	-	-	nA
		Y port; per channel; see Fig. 9	15 V	-	-	-	200	-	-	-	-	nA
I <sub>DD</sub>	supply current	I <sub>O</sub> = 0 A	5 V	-	5	-	5	-	150	-	150	μA
			10 V	-	10	-	10	-	300	-	300	μA
			15 V	-	20	-	20	-	600	-	600	μA
C <sub>I</sub>	input capacitance	S <sub>n</sub> , E inputs	-	-	-	-	7.5	-	-	-	-	pF

### 10.1. Test circuits



10.2. ON resistance

Table 7. ON resistance

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $I_{SW} = 200\text{ }\mu\text{A}$ ;  $V_{SS} = V_{EE} = 0\text{ V}$ .

Symbol	Parameter	Conditions	$V_{DD} - V_{EE}$	Typ	Max	Unit
$R_{ON(peak)}$	ON resistance (peak)	$V_I = 0\text{ V to }V_{DD} - V_{EE}$ ; see Fig. 10 and Fig. 11	5 V	350	2500	$\Omega$
			10 V	80	245	$\Omega$
			15 V	60	175	$\Omega$
$R_{ON(rail)}$	ON resistance (rail)	$V_I = 0\text{ V}$ ; see Fig. 10 and Fig. 11	5 V	115	340	$\Omega$
			10 V	50	160	$\Omega$
			15 V	40	115	$\Omega$
		$V_I = V_{DD} - V_{EE}$ ; see Fig. 10 and Fig. 11	5 V	120	365	$\Omega$
			10 V	65	200	$\Omega$
			15 V	50	155	$\Omega$
$\Delta R_{ON}$	ON resistance mismatch between channels	$V_I = 0\text{ V to }V_{DD} - V_{EE}$ ; see Fig. 10	5 V	25	-	$\Omega$
			10 V	10	-	$\Omega$
			15 V	5	-	$\Omega$

10.2.1. ON resistance waveform and test circuit

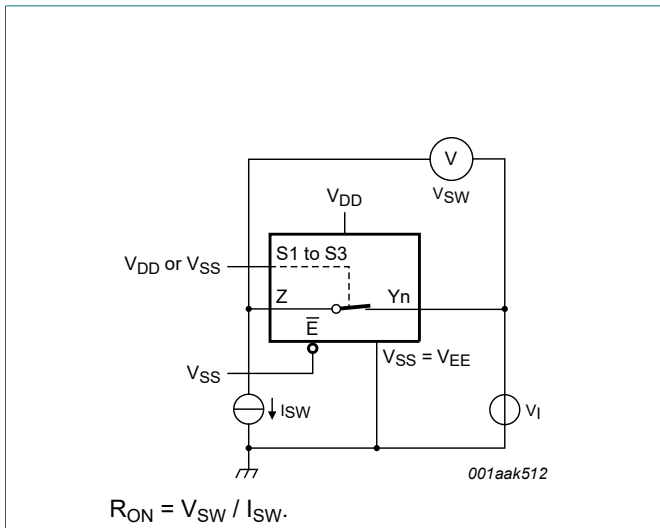


Fig. 10. Test circuit for measuring  $R_{ON}$

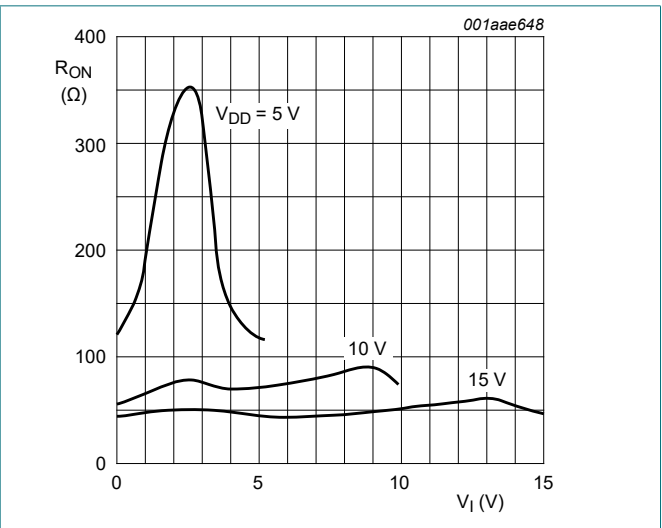


Fig. 11. Typical  $R_{ON}$  as a function of input voltage

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $V_{SS} = V_{EE} = 0\text{ V}$ ; for test circuit see [Fig. 15](#).

Symbol	Parameter	Conditions	V <sub>DD</sub>	Typ	Max	Unit
t <sub>PHL</sub>	HIGH to LOW propagation delay	Y <sub>n</sub> , Z to Z, Y <sub>n</sub> ; see <a href="#">Fig. 12</a>	5 V	15	30	ns
			10 V	5	10	ns
			15 V	5	10	ns
		S <sub>n</sub> to Y <sub>n</sub> , Z; see <a href="#">Fig. 13</a>	5 V	150	300	ns
			10 V	60	120	ns
			15 V	45	90	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	Y <sub>n</sub> , Z to Z, Y <sub>n</sub> ; see <a href="#">Fig. 12</a>	5 V	15	30	ns
			10 V	5	10	ns
			15 V	5	10	ns
		S <sub>n</sub> to Y <sub>n</sub> , Z; see <a href="#">Fig. 13</a>	5 V	150	300	ns
			10 V	65	130	ns
			15 V	45	90	ns
t <sub>PHZ</sub>	HIGH to OFF-state propagation delay	$\bar{E}$ to Y <sub>n</sub> , Z; see <a href="#">Fig. 14</a>	5 V	120	240	ns
			10 V	90	180	ns
			15 V	85	170	ns
t <sub>PZH</sub>	OFF-state to HIGH propagation delay	$\bar{E}$ to Y <sub>n</sub> , Z; see <a href="#">Fig. 14</a>	5 V	140	280	ns
			10 V	55	110	ns
			15 V	40	80	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	$\bar{E}$ to Y <sub>n</sub> , Z; see <a href="#">Fig. 14</a>	5 V	145	290	ns
			10 V	120	240	ns
			15 V	115	230	ns
t <sub>PZL</sub>	OFF-state to LOW propagation delay	$\bar{E}$ to Y <sub>n</sub> , Z; see <a href="#">Fig. 14</a>	5 V	140	280	ns
			10 V	55	110	ns
			15 V	40	80	ns

11.1. Waveforms and test circuit

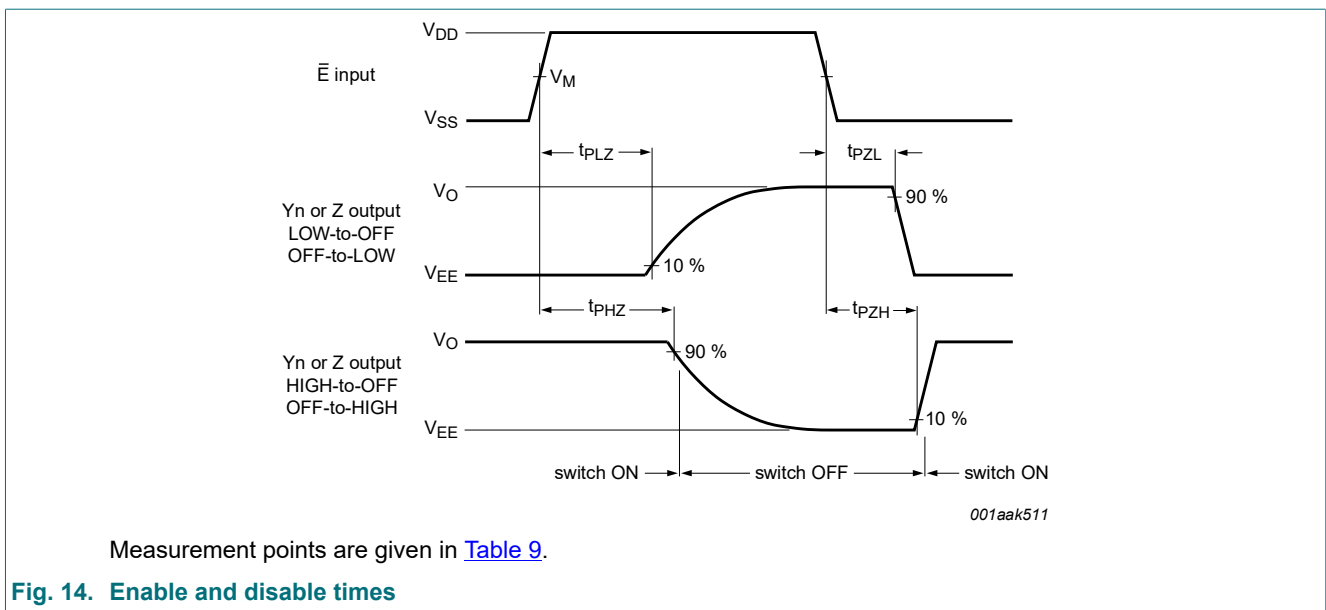
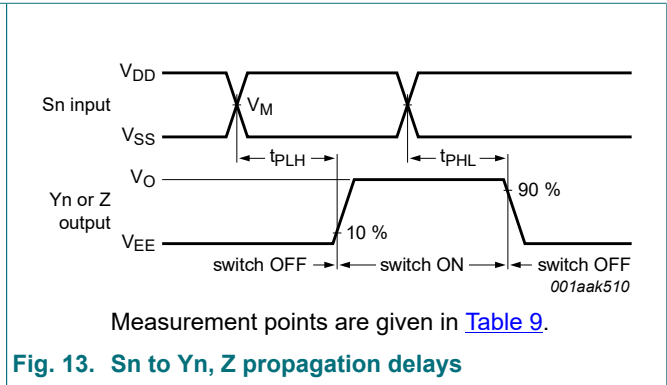
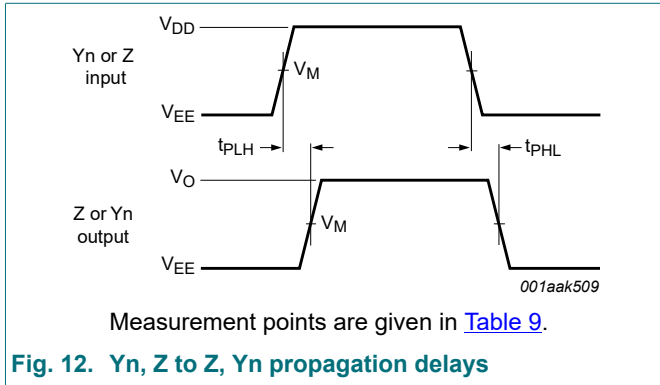
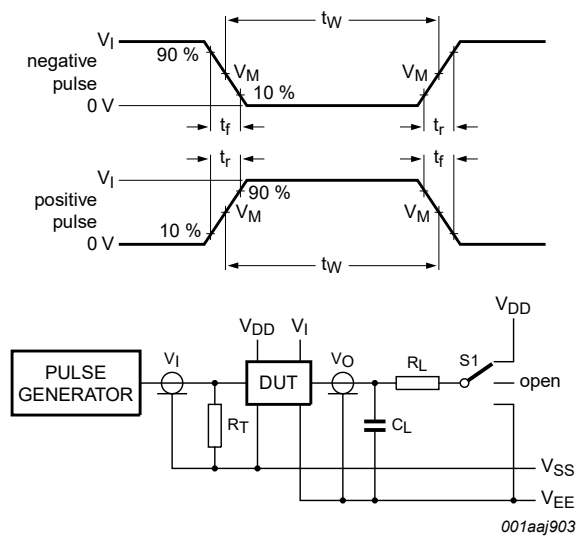


Table 9. Measurement points

Supply voltage	Input	Output
V <sub>DD</sub>	V <sub>M</sub>	V <sub>M</sub>
5 V to 15 V	0.5V <sub>DD</sub>	0.5V <sub>DD</sub>



Test data is given in [Table 10](#).

Definitions:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including test jig and probe.

$R_L$  = Load resistance.

**Fig. 15. Test circuit for measuring switching times**

**Table 10. Test data**

Input				Load		S1 position				
Yn, Z	Sn and $\bar{E}$	$t_r, t_f$	$V_M$	$C_L$	$R_L$	$t_{PHL}$ [1]	$t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$	other
$V_{DD}$ or $V_{EE}$	$V_{DD}$ or $V_{SS}$	$\leq 20$ ns	$0.5V_{DD}$	50 pF	10 k $\Omega$	$V_{DD}$ or $V_{EE}$	$V_{EE}$	$V_{EE}$	$V_{DD}$	$V_{EE}$

[1] For Yn to Z or Z to Yn propagation delays use  $V_{EE}$ . For Sn to Yn or Z propagation delays use  $V_{DD}$ .

## 11.2. Additional dynamic parameters

**Table 11. Additional dynamic characteristics**

$V_{SS} = V_{EE} = 0$  V;  $T_{amb} = 25$  °C.

Symbol	Parameter	Conditions	$V_{DD}$	Typ	Max	Unit
THD	total harmonic distortion	see <a href="#">Fig. 16</a> ; $R_L = 10$ k $\Omega$ ; $C_L = 15$ pF; channel ON; $V_I = 0.5V_{DD}$ (p-p); $f_i = 1$ kHz	5 V	[1] 0.25	-	%
			10 V	[1] 0.04	-	%
			15 V	[1] 0.04	-	%
$f_{(-3dB)}$	-3 dB frequency response	see <a href="#">Fig. 17</a> ; $R_L = 1$ k $\Omega$ ; $C_L = 5$ pF; channel ON; $V_I = 0.5V_{DD}$ (p-p)	5 V	[1] 13	-	MHz
			10 V	[1] 40	-	MHz
			15 V	[1] 70	-	MHz
$\alpha_{iso}$	isolation (OFF-state)	see <a href="#">Fig. 18</a> ; $f_i = 1$ MHz; $R_L = 1$ k $\Omega$ ; $C_L = 5$ pF; channel OFF; $V_I = 0.5V_{DD}$ (p-p)	10 V	[1] -50	-	dB
$V_{ct}$	crosstalk voltage	digital inputs to switch; see <a href="#">Fig. 19</a> ; $R_L = 10$ k $\Omega$ ; $C_L = 15$ pF; $\bar{E}$ or Sn = $V_{DD}$ (square-wave)	10 V	50	-	mV
Xtalk	crosstalk	between switches; see <a href="#">Fig. 20</a> ; $f_i = 1$ MHz; $R_L = 1$ k $\Omega$ ; $V_I = 0.5V_{DD}$ (p-p)	10 V	[1] -50	-	dB

[1]  $f_i$  is biased at  $0.5 V_{DD}$ ;  $V_I = 0.5V_{DD}$  (p-p).

Table 12. Dynamic power dissipation  $P_D$

$P_D$  can be calculated from the formulas shown;  $V_{EE} = V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ .

Symbol	Parameter	$V_{DD}$	Typical formula for $P_D$ ( $\mu\text{W}$ )	where:
$P_D$	dynamic power dissipation	5 V	$P_D = 1000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_i$ = input frequency in MHz; $f_o$ = output frequency in MHz; $C_L$ = output load capacitance in pF; $V_{DD}$ = supply voltage in V; $\Sigma(C_L \times f_o)$ = sum of the outputs.
		10 V	$P_D = 5500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 15000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

11.2.1. Test circuits

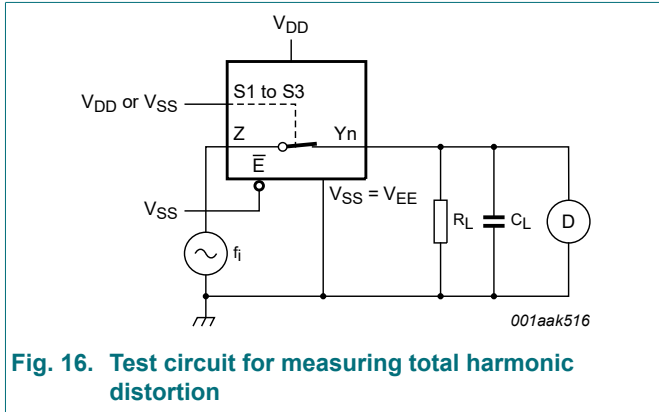


Fig. 16. Test circuit for measuring total harmonic distortion

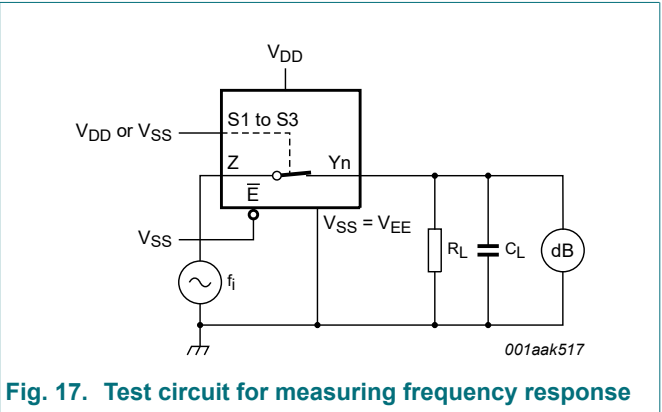


Fig. 17. Test circuit for measuring frequency response

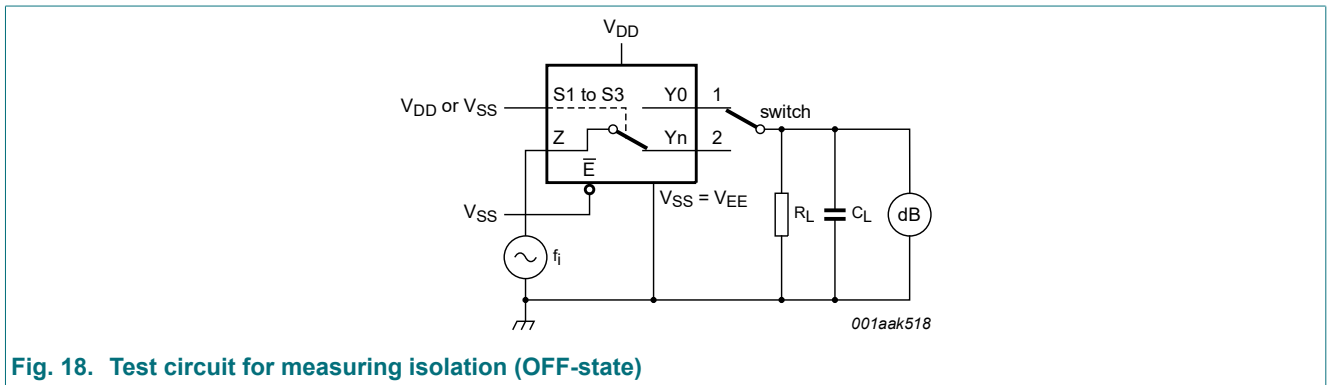


Fig. 18. Test circuit for measuring isolation (OFF-state)

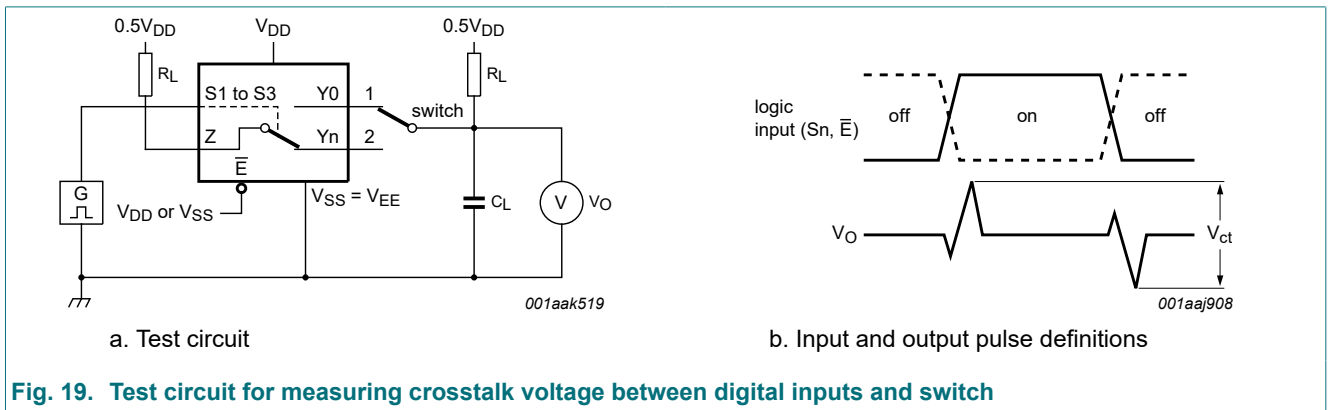
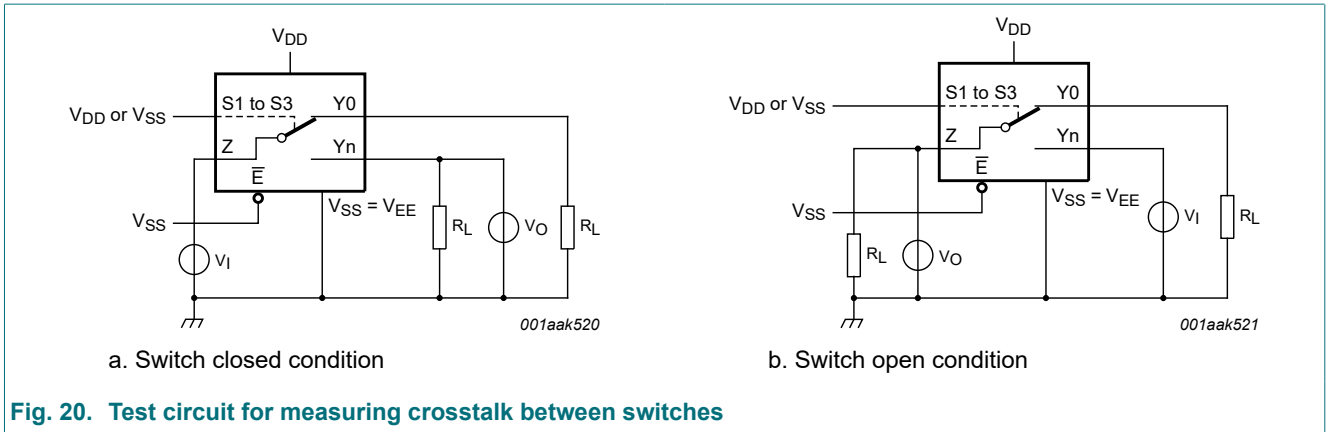


Fig. 19. Test circuit for measuring crosstalk voltage between digital inputs and switch



12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

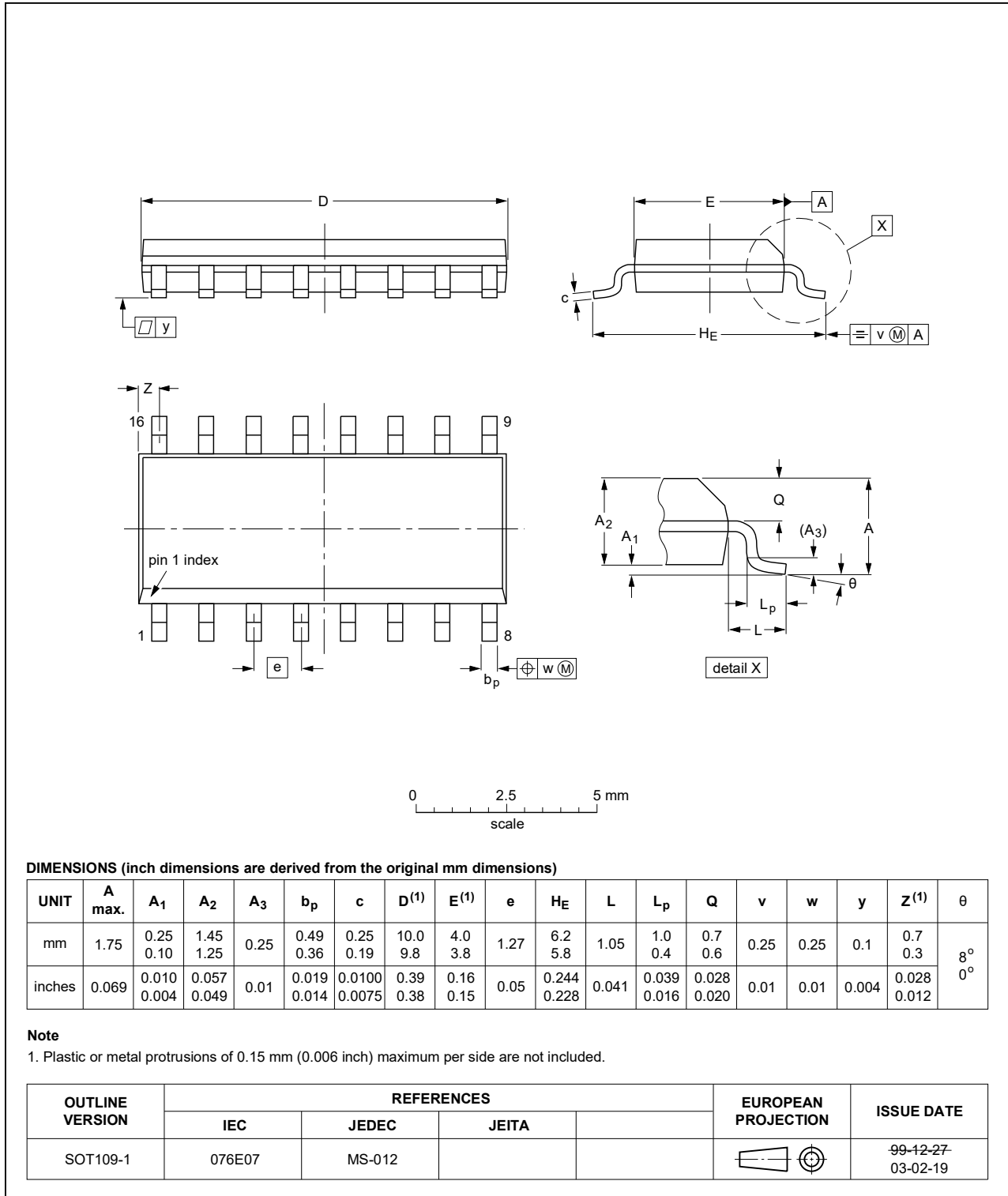


Fig. 21. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

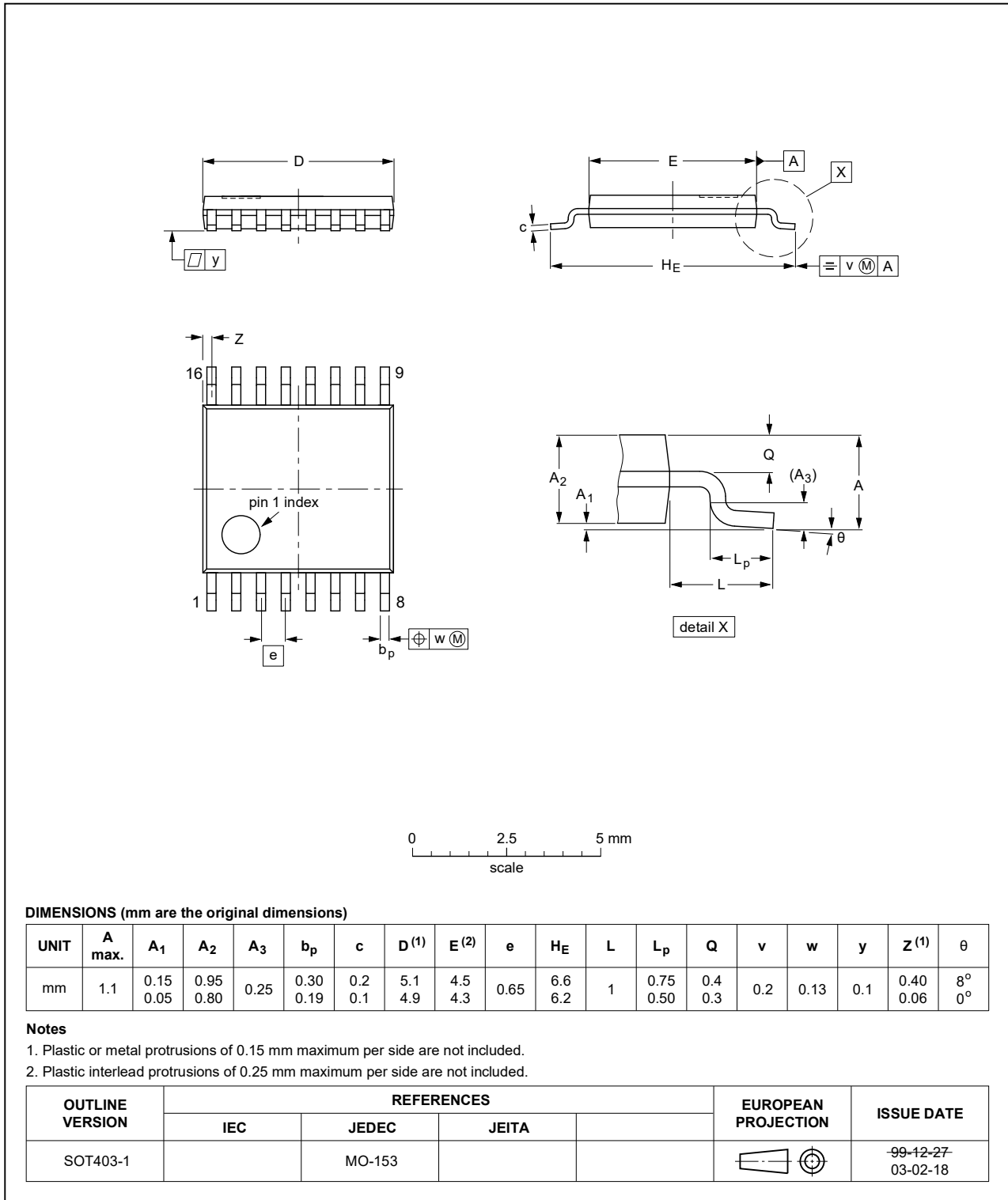


Fig. 22. Package outline SOT403-1 (TSSOP16)

## 13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model

## 14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4051B_Q100 v.3	20210729	Product data sheet	-	HEF4051B_Q100 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li><a href="#">Section 8</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
HEF4051B_Q100 v.2	20140911	Product data sheet	-	HEF4051B_Q100 v.1
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Fig. 19</a>: Test circuit modified</li> </ul>			
HEF4051B_Q100 v.1	20120712	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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