THE DATASHEET OF

DS1374U-3+

19-5484; Rev 4; 8/10

DALLAS SEMICONDUCTOR MAXIM

I²C, 32-Bit Binary Counter Watchdog RTC with Trickle Charger and Reset Input/Output

DS1374

General Description

The DS1374 is a 32-bit binary counter designed to continuously count time in seconds. An additional counter generates a periodic alarm or serves as a watchdog timer. If disabled, this counter can be used as 3 bytes of nonvolatile (NV) RAM. Separate output pins are provided for an interrupt and a square wave at one of four selectable frequencies. A precision temperature-compensated reference and comparator circuit monitor the status of V_{CC} to detect power failures, provide a reset output, and automatically switch to the backup supply when necessary. Additionally, the reset pin is monitored as a pushbutton input for externally generating a reset. The device is programmed serially through an I²C serial interface.

Applications

Portable Instruments

Point-of-Sale Equipment

Medical Equipment

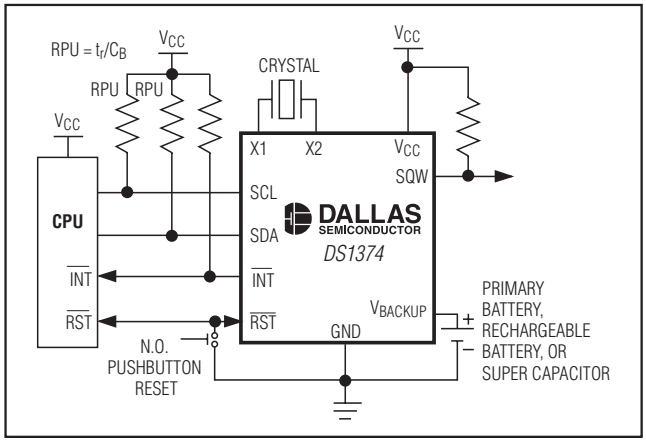
Telecommunications

Pin Configurations appear at the end of the data sheet.

Features

- **32-Bit Binary Counter**
- **Second Binary Counter Provides Time-of-Day Alarm, Watchdog Timer, or NV RAM**
- **Separate Square-Wave and Interrupt Output Pins**
- **I²C Serial Interface**
- **Automatic Power-Fail Detect and Switch Circuitry**
- **Single-Pin Pushbutton Reset Input/Open-Drain Reset Output**
- **Low-Voltage Operation**
- **Trickle-Charge Capability**
- **-40°C to +85°C Operating Temperature Range**
- **10-Pin µSOP, 16-Pin SO**
- **Available in a Surface-Mount Package with an Integrated Crystal (DS1374C)**
- **Underwriters Laboratories (UL) Recognized**

Typical Operating Circuit



Ordering Information

PART	TEMP RANGE	VOLTAGE (V)	PIN-PACKAGE	TOP MARK**
DS1374C-18#	-40°C to +85°C	1.8	16 SO (300 mils)	DS1374C-18
DS1374C-3#	-40°C to +85°C	3.0	16 SO (300 mils)	DS1374C-3
DS1374C-33#	-40°C to +85°C	3.3	16 SO (300 mils)	DS1374C-33
DS1374U-18+	-40°C to +85°C	1.8	10 µSOP	DS1374-18
DS1374U-3+	-40°C to +85°C	3.0	10 µSOP	DS1374-3
DS1374U-33+	-40°C to +85°C	3.3	10 µSOP	DS1374-33

#Denotes a RoHS-compliant device that may include lead that is exempt under RoHS requirements. The lead finish is JESD97 category e3, and is compatible with both lead-based and lead-free soldering processes.

+Denotes a lead(Pb)-free/RoHS-compliant package.

***A "#" anywhere on the top mark denotes a RoHS-compliant package. A "+" anywhere on the top mark denotes a lead(Pb)-free package.*

I²C, 32-Bit Binary Counter Watchdog RTC with Trickle Charger and Reset Input/Output

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC} Pin Relative to Ground .....-0.3V to +6.0V
Voltage Range on SDA or SCL
Relative to Ground .....-0.3V to V_{CC} + 0.3V
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)
16-Pin SO .....73°C/W
10-Pin µSOP .....221°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 1)
16-Pin SO .....23°C/W
10-Pin µSOP .....39°C/W
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Lead Temperature (soldering, 10s) .....+260°C
Soldering Temperature (reflow) .....+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Notes 3, 4)	V_{CC}	DS1374-33	2.97	3.3	5.50	V
		DS1374-3	2.7	3.0	3.3	
		DS1374-18	1.71	1.8	1.89	
Input Logic 1	V_{IH}	(Note 3)	0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0	V_{IL}	(Note 3)	-0.3		+0.3 x V_{CC}	V
Pullup Resistor Voltage ($\overline{INT}$, SQW, SDA, SCL), V_{CC} = 0V	V_{PU}	(Note 3)			5.5	V
Power-Fail Voltage (Note 3)	V_{PF}	DS1374-33	2.70	2.88	2.97	V
		DS1374-3	2.45	2.6	2.7	
		DS1374-18	1.51	1.6	1.71	
Backup Supply Voltage (Notes 3, 4, 5)	V_{BACKUP}	DS1374-33	1.3	3.0	V_{CC} (MAX)	V
		DS1374-3, DS1374-18	1.3	3.0	3.7	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Trickle-Charge Current-Limiting Resistors	R1	(Note 6)		250		Ω
	R2	(Note 7)		2000		
	R3	(Note 8)		4000		
Input Leakage	I_{LI}	(Note 9)	-1		+1	µA
I/O Leakage	I_{LO}	(Note 10)	-1		+1	
$\overline{RST}$ Pin I/O Leakage	I_{LORST}	(Note 11)	-200		+1	
SDA Logic 0 Output (V_{OL} = 0.4V)	I_{OLSDA}				3.0	mA
$\overline{RST}$, SQW, and $\overline{INT}$ Logic 0 Outputs (Note 12)	I_{OL1}	V_{CC} > 2V; V_{OL} = 0.4V			3.0	mA
		1.71V < V_{CC} < 2V; V_{OL} = 0.2 V_{CC}			3.0	
		1.3V < V_{CC} < 1.71V; V_{OL} = 0.2 V_{CC}			250	µA
Active Supply Current (Notes 12, 13)	I_{CCA}	DS1374-18		75	150	µA
		DS1374-3		110	200	
		DS1374-33		180	300	
Standby Current (Notes 12, 14)	I_{CCS}	DS1374-18		60	100	µA
		DS1374-3		80	125	
		DS1374-33		115	175	
V_{BACKUP} Leakage Current (V_{BACKUP} = 3.7V)	$I_{BACKUPLKG}$				100	nA

DC ELECTRICAL CHARACTERISTICS

(**V_{CC} = 0V, V_{BACKUP} = 3.7V**, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MAX	TYP	MAX	UNITS
V_{BACKUP} Current (OSC ON); SQW OFF	I_{BKOSC1}	(Note 15)		400	700	nA
V_{BACKUP} Current (OSC ON); SQW ON (32kHz)	I_{BKOSC2}	(Notes 15, 16)		600	1000	nA
V_{BACKUP} Data-Retention Current (OSC OFF)	$I_{BACKUPDR}$			25	100	nA

I²C, 32-Bit Binary Counter Watchdog RTC with Trickle Charger and Reset Input/Output

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2) (Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency (Note 17)	f_{SCL}	Fast mode	100		400	kHz
		Standard mode	0		100	
Bus Free Time Between STOP and START Conditions	t_{BUF}	Fast mode	1.3			µs
		Standard mode	4.7			
Hold Time (Repeated) START Condition (Note 18)	$t_{HD:STA}$	Fast mode	0.6			µs
		Standard mode	4.0			
Low Period of SCL Clock	t_{LOW}	Fast mode	1.3			µs
		Standard mode	4.7			
High Period of SCL Clock	t_{HIGH}	Fast mode	0.6			µs
		Standard mode	4.0			
Data Hold Time (Notes 19, 20)	$t_{HD:DAT}$	Fast mode	0		0.9	µs
		Standard mode	0		0.9	
Data Setup Time (Note 21)	$t_{SU:DAT}$	Fast mode	100			ns
		Standard mode	250			
Start Setup Time	$t_{SU:STA}$	Fast mode	0.6			µs
		Standard mode	4.7			
Rise Time of Both SDA and SCL Signals (Note 17)	t_R	Fast mode	20 + 0.1C_B		300	ns
		Standard mode			1000	
Fall Time of Both SDA and SCL Signals (Note 17)	t_F	Fast mode	20 + 0.1C_B		300	ns
		Standard mode			300	
Setup Time for STOP Condition	$t_{SU:STO}$	Fast mode	0.6			µs
		Standard mode	4.7			
Capacitive Load for Each Bus Line	C_B	(Note 17)			400	pF
I/O Capacitance (SDA, SCL)	$C_{I/O}$	(Note 22)			10	pF
Pulse Width of Spikes That Must be Suppressed by the Input Filter	t_{SP}	Fast mode		30		ns
Pushbutton Debounce	PB_{DB}	(Figure 2)		250		ms
Reset Active Time	t_{RST}	(Figure 2)		250		ms
Oscillator Stop Flag (OSF) Delay	t_{OSF}	(Note 23)		100		ms

POWER-UP/POWER-DOWN CHARACTERISTICS

(T_A = -40°C to +85°C) (Figure 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Detect to Recognize Inputs (V_{CC} Rising)	t_{RPU}	(Note 24)		250		ms
V_{CC} Fall Time; $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F		300			µs
V_{CC} Rise Time; $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R		0			µs

WARNING: Under no circumstances are negative undershoots, of any amplitude, allowed when the device is in write protection.

Note 2: Limits at -40°C are guaranteed by design and not production tested.
Note 3: All voltages are referenced to ground.
Note 4: V_{BACKUP} should not exceed V_{CC} MAX or 3.7V, whichever is greater.
Note 5: The use of the 250Ω trickle-charge resistor is not allowed at V_{CC} > 3.63V and should not be enabled.
Note 6: Measured at V_{CC} = typ, V_{BACKUP} = 0V, register 09h = A5h.
Note 7: Measured at V_{CC} = typ, V_{BACKUP} = 0V, register 09h = A6h.
Note 8: Measured at V_{CC} = typ, V_{BACKUP} = 0V, register 09h = A7h.
Note 9: SCL only.
Note 10: SDA and SQW and $\overline{INT}$.
Note 11: The $\overline{RST}$ pin has an internal 50kΩ pullup resistor to V_{CC}.
Note 12: Trickle charger disabled.
Note 13: I_{CCA}—SCL clocking at max frequency = 400kHz.
Note 14: Specified with I^2C bus inactive.
Note 15: Measured with a 32.768kHz crystal attached to the X1 and X2 pins.
Note 16: WDSTR = 1. BBSQW = 1 is required for operation when V_{CC} is below the power-fail trip point (or absent).
Note 17: C_B—total capacitance of one bus line in pF.
Note 18: After this period, the first clock pulse is generated.
Note 19: The maximum $t_{HD:DAT}$ only has to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.
Note 20: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to as the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 21: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geq$ to 250ns must be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{R\ max} + t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.
Note 22: Guaranteed by design. Not production tested.
Note 23: The parameter t_{OSF} is the period of time the oscillator must be stopped for the OSF flag to be set over the voltage range of $0V \leq V_{CC} \leq V_{CC\ MAX}$ and $1.3V \leq V_{BACKUP} \leq 3.7V$.
Note 24: This delay applies only if the oscillator is enabled and running. If the $\overline{EOSC}$ bit is 1, the startup time of the oscillator is added to this delay.

I2C, 32-Bit Binary Counter Watchdog RTC with Trickle Charger and Reset Input/Output

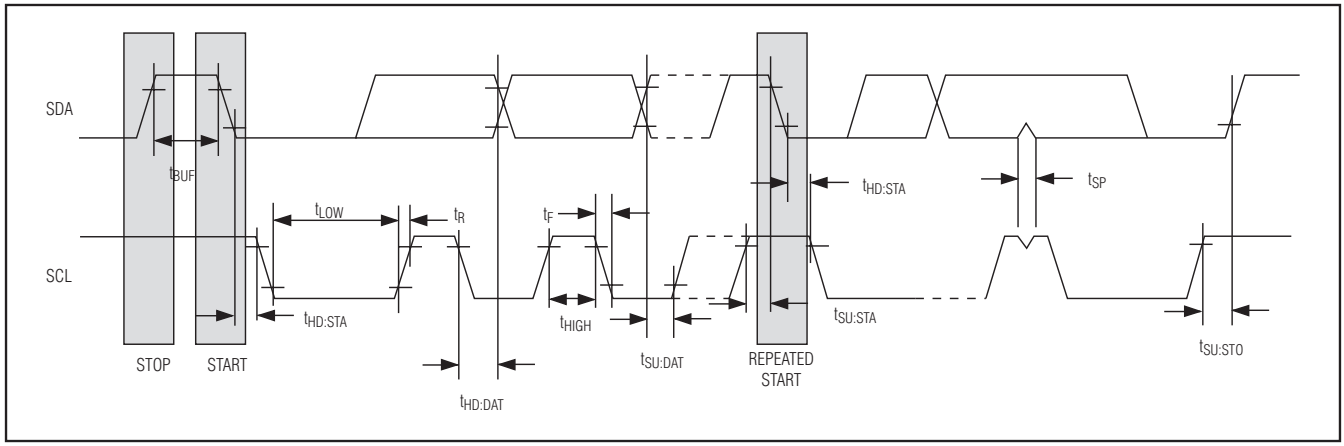


Figure 1. Data Transfer on I2C Serial Bus

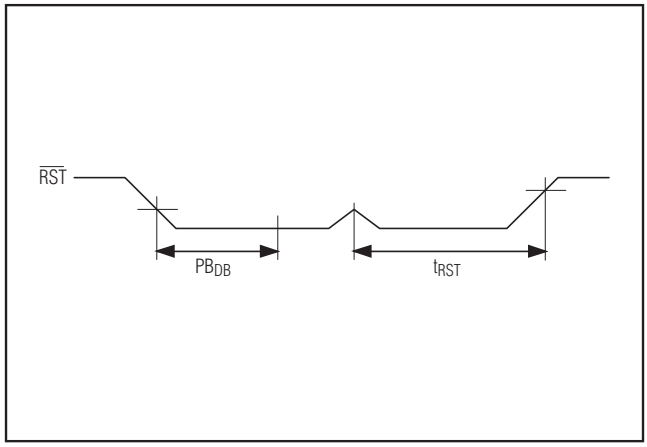


Figure 2. Pushbutton Reset Timing

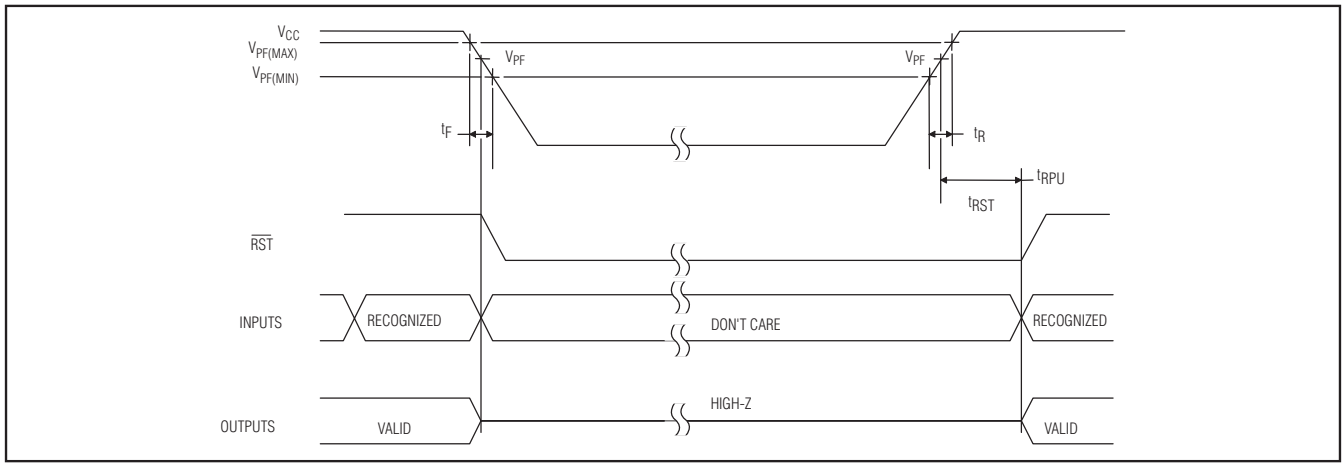
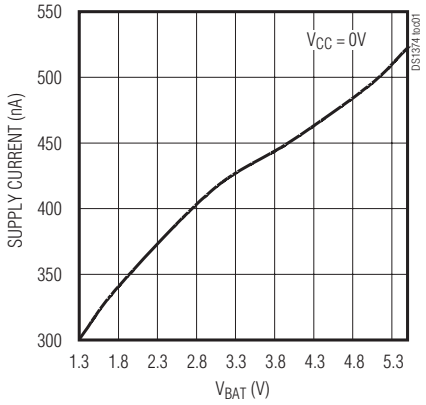


Figure 3. Power-Up/Power-Down Timing

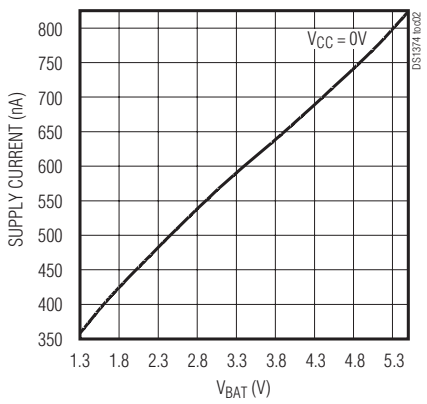
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

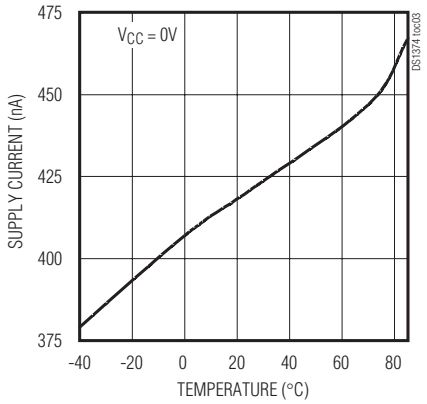
$I_{BATOSC1}$ vs. V_{BAT} SQUARE-WAVE OFF



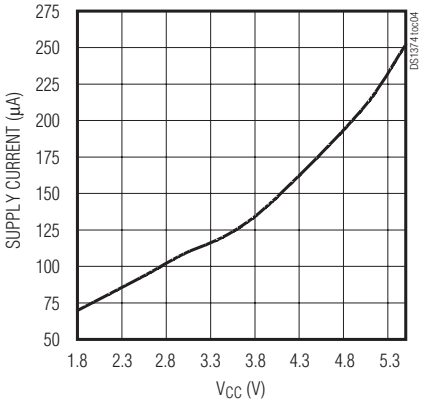
$I_{BATOSC2}$ vs. V_{BAT} SQUARE-WAVE ON



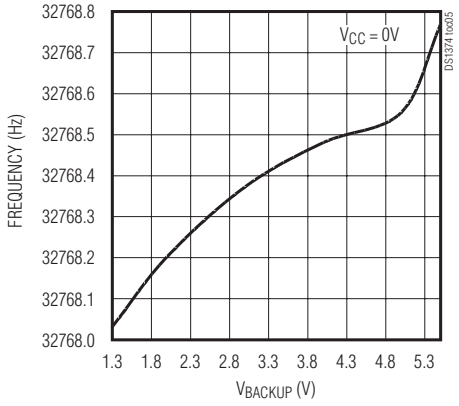
$I_{BATOSC1}$ vs. TEMPERATURE V_{BAT} = 3.0V



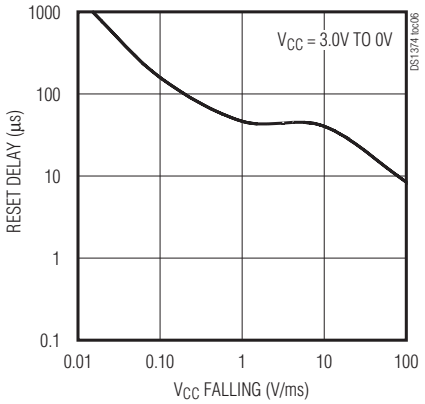
I_{CCA} vs. V_{CC} (SQUARE-WAVE ON)



OSCILLATOR FREQUENCY vs. V_{BACKUP}



V_{CC} FALLING vs. $\overline{RST}$ DELAY



I²C, 32-Bit Binary Counter Watchdog RTC with Trickle Charger and Reset Input/Output

Pin Description

PIN		NAME	FUNCTION
µSOP	SO		
1, 2	—	X1, X2	Connections for a Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6pF. Pin X1 is the input to the oscillator and can optionally be connected to an external 32.768kHz oscillator. The output of the internal oscillator, pin X2, is left unconnected if an external oscillator is connected to pin X1.
3	13	V_{BACKUP}	Connection for a Secondary Power Supply. This supply is used to operate the oscillator and counters when V_{CC} is absent. Supply voltage must be held between 1.3V and 3.7V (-18 and -3) or 1.3V and 5.5V (-33) for proper operation. This pin can be connected to a primary cell such as a lithium cell. Additionally, this pin can be connected to a rechargeable cell or a super cap when used with the trickle-charge feature. UL recognized to ensure against reverse charging when used with a lithium battery. This pin must be grounded if not used.
4	14	$\overline{RST}$	Active-Low, Open-Drain Output with a Debounced Pushbutton Input. This pin can be activated by a pushbutton reset request, a watchdog alarm condition, or a power-fail event. It has an internal 50kΩ pullup resistor. No external resistors should be connected. If the crystal oscillator is disabled, the startup time of the oscillator is added to the t_{RST} delay.
5	15	GND	Ground
6	16	SDA	Serial Data Input/Output. SDA is the input/output for the 2-wire serial interface. The SDA pin is open drain and requires an external pullup resistor.
7	1	SCL	Serial Clock Input. SCL is the clock input for the 2-wire serial interface and is used to synchronize data movement on the serial interface.
8	2	$\overline{INT}$	Interupt. This pin is used to output the alarm interrupt or the watchdog reset signal. It is active-low open drain and requires an external pullup resistor.
9	3	SQW	Square-Wave Output. This pin is used to output the programmable square-wave signal. It is open drain and requires an external pullup resistor.
10	4	V_{CC}	DC Power for Primary Power Supply
—	5–12	N.C.	No Connection. Must be connected to ground.

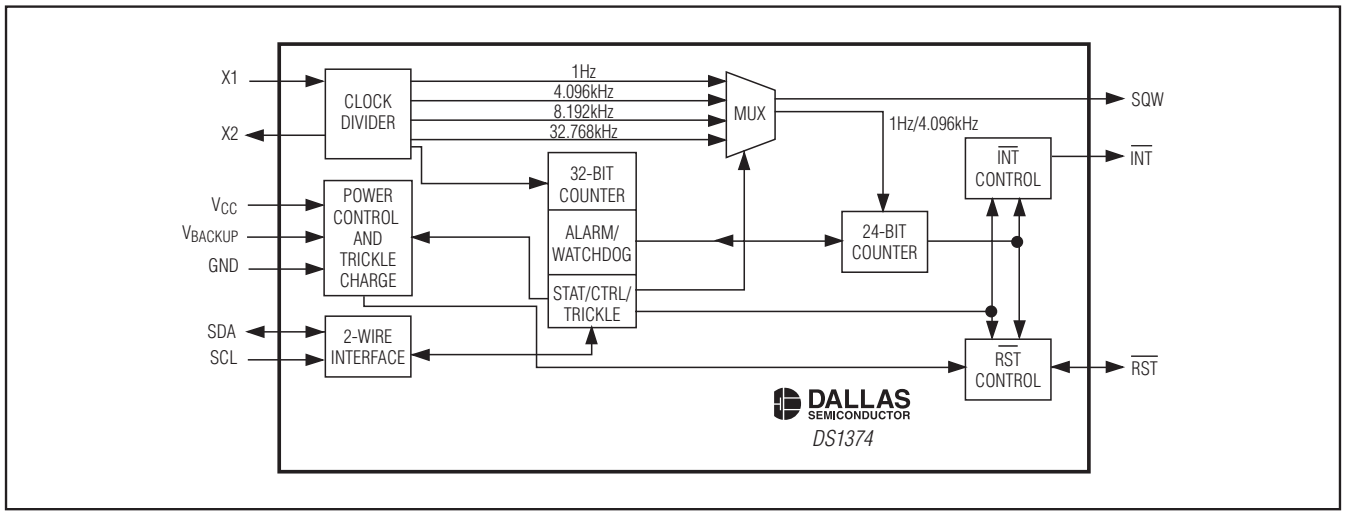


Figure 4. Functional Diagram

Table 1. Crystal Specifications*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O		32.768		kHz
Series Resistance	ESR			45	kΩ
Load Capacitance	C_L		6		pF

**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to* Application Note 58: Crystal Considerations for Dallas Real-Time Clocks *for additional specifications.*

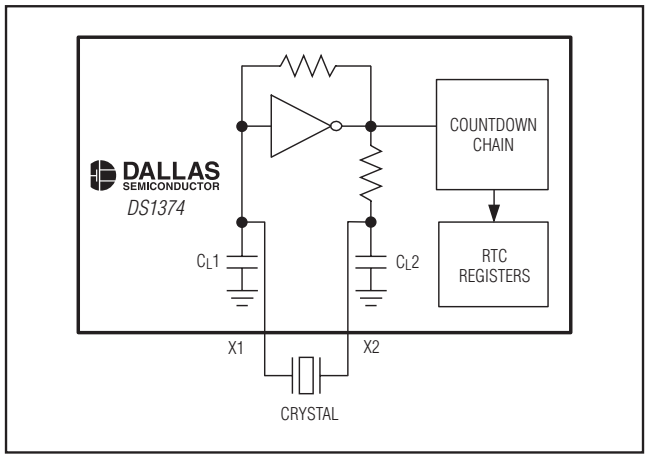


Figure 5. Oscillator Circuit Showing Internal Bias Network

Detailed Description

The DS1374 is a real-time clock with an I²C serial interface. It provides elapsed seconds from a user-defined starting point in a 32-bit counter (Figure 4). A 24-bit counter can be configured as either a watchdog counter or an alarm counter. An on-chip oscillator circuit uses a customer-supplied 32.768kHz crystal to keep time. A power-control circuit switches operation from V_{CC} to V_{BACKUP} and back when power on V_{CC} is cycled. The oscillator and counters continue to operate when powered by either supply. If a rechargeable backup supply is used, a trickle charger can be enabled to charge the backup supply while V_{CC} is on.

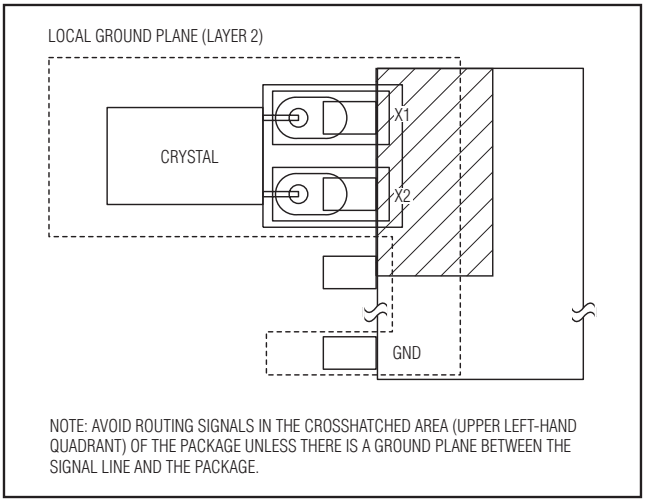


Figure 6. Layout Example

Oscillator Circuit

The DS1374 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 1 specifies several crystal parameters for the external crystal. Figure 5 shows a functional schematic of the oscillator circuit. The startup time is usually less than 1 second when using a crystal with the specified characteristics.

Clock Accuracy

Clock accuracy is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error is added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 6 shows a typical PC board layout for isolating the crystal and oscillator from noise. Refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks* for detailed information.

DS1374C Only

The DS1374C integrates a standard 32,768Hz crystal into the package. Typical accuracy at nominal V_{CC} and 25°C is approximately 10ppm. See *Application Note 58* for information about crystal accuracy vs. temperature.

I²C, 32-Bit Binary Counter Watchdog RTC with Trickle Charger and Reset Input/Output

Power Control

The power-control function is provided by a precise, temperature-compensated voltage reference and a comparator circuit that monitors the V_{CC} level. The device is fully accessible and data can be written and read when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below V_{PF}, the internal clock registers are blocked from any access. If V_{PF} is less than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{BACKUP}. The registers are maintained from the V_{BACKUP} source until V_{CC} is returned to nominal levels (Table 1). After V_{CC} returns above V_{PF}, read and write access is allowed after $\overline{RST}$ goes high (Figure 1).

Table 2. Power Control

SUPPLY CONDITION	READ/WRITE ACCESS	POWERED BY
$V_{CC} < V_{PF}$, $V_{CC} < V_{BACKPUP}$	No	V_{BACKUP}
$V_{CC} < V_{PF}$, $V_{CC} > V_{BACKUP}$	No	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} < V_{BACKUP}$	Yes	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} > V_{BACKUP}$	Yes	V_{CC}

Address Map

Table 3 shows the address map for the DS1374 registers. During a multibyte access, the address pointer wraps around to location 00h when it reaches the end of the register space (08h). On an I²C START, STOP, or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. These secondary registers read the time information, while the clock continues to run. This eliminates the need to reread the registers in case of an update of the main registers during a read.

Time-of-Day Counter

The time-of-day counter is a 32-bit up counter that increments once per second when the oscillator is running. The contents can be read or written by accessing the address range 00h–03h. When the counter is read, the current time of day is latched into a register, which is output on the serial data line while the counter continues to increment.

Note: Writing to any TOD register will reset the 1Hz square wave output.

Table 3. Address Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION
00H	TOD Counter Byte 0								Time-of-Day Counter
01H	TOD Counter Byte 1								Time-of-Day Counter
02H	TOD Counter Byte 2								Time-of-Day Counter
03H	TOD Counter Byte 3								Time-of-Day Counter
04H	WD/$\overline{ALM}$ Counter Byte 0								Watchdog/Alarm Counter
05H	WD/$\overline{ALM}$ Counter Byte 1								Watchdog/Alarm Counter
06H	WD/$\overline{ALM}$ Counter Byte 2								Watchdog/Alarm Counter
07H	$\overline{EOSC}$	WACE	WD/$\overline{ALM}$	BBSQW	WDSTR	RS2	RS1	AIE	Control
08H	OSF	0	0	0	0	0	0	AF	Status
09H	TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	Trickle Charger

Note: *Unless otherwise specified, the state of the registers is not defined when power is first applied.*

Watchdog/Alarm Counter

The contents of the watchdog/alarm counter, which is a separate 24-bit down counter, are accessed in the address range 04h–06h. When this counter is written, the counter and a seed register are loaded with the desired value. When the counter is to be reloaded, it uses the value in the seed register. When the counter is read, the current counter value is latched into a register, which is output on the serial data line while the counter continues to decrement.

IIf the counter is not needed, it can be disabled and used as a 24-bit cache of NV RAM by setting the WACE bit in the control register to logic 0. If all 24 bits of the watchdog/alarm counter are written to zero, the counter is disabled, independent of the WACE bit setting. When the watchdog counter is is written to a nonzero value, and WACE is written to logic 1, the function of the counter is determined by the WD/$\overline{ALM}$ bit.

When the WD/$\overline{ALM}$ bit in the control register is set to logic 0, the WD/$\overline{ALM}$ counter decrements every second until it reaches zero. At this point, the AF bit in the status register is set to 1 and the counter is reloaded and restarted. AF remains set until cleared by writing it to 0. If AIE = 1, the $\overline{INT}$ pin goes active whenever AF = 1. WDSTR does not affect operation when WD/$\overline{ALM}$ = 0.

When the WD/$\overline{ALM}$ bit is set to logic 1, the WD/$\overline{ALM}$ counter decrements every 1/4096 of a second (approximately every 244us) until it reaches zero. When any of the watchdog counters bytes are read, the seed value is reloaded and the counter restarts. Writing to the watchdog counter updates the seed value and reloads the counter with the new seed value. When the counter reaches zero, the AF bit is set and the counter stops.

If WDSTR = 0, the $\overline{RST}$ pin pulses low for 250ms, and accesses to the device are inhibited. At the end of the 250ms pulse, the AF bit is cleared to zero, the $\overline{RST}$ pin becomes high impedance, and read/write access to the device is enabled.

If WDSTR = 1 and the counter reaches zero, the AF bit is set and the counter stops. If AIE = 0, AF remains set until cleared by writing it to 0. If AIE = 1, the $\overline{INT}$ pin pulses low for 250ms. At the end of the 250ms pulse, the AF bit is cleared and $\overline{INT}$ becomes high impedance.

The 250ms pulse on $\overline{INT}$ or $\overline{RST}$ cannot be truncated by writing either AF or AIE to zero during the low time. If the $\overline{INT}$ counter is written during the 250ms pulse, the counter starts decrementing upon the pulse completion.

The watchdog and alarm function operates from V_{CC} or V_{BAT}. When the AF bit is set, $\overline{INT}$ is pulled low when the device is powered by V_{CC} or V_{BAT}.

Note: WACE must be toggled from logic 0 to logic 1 after the watchdog counter is written from a zero to a nonzero value.

Power-Up/Power-Down Reset and Pushbutton Reset Functions

A precision temperature-compensated reference and comparator circuit monitors the status of V_{CC}. When an out-of-tolerance condition occurs, an internal power-fail signal is generated that forces the $\overline{RST}$ pin low and blocks read/write access to the DS1374. When V_{CC} returns to an in-tolerance condition, the $\overline{RST}$ pin is held low for 250ms to allow the power supply to stabilize. If the $\overline{EOSC}$ bit is set to a logic 1 (to disable the oscillator in battery-backup mode), the reset signal is kept active for 250ms plus the startup time of the oscillator.

The DS1374 provides for a pushbutton switch to be connected to the $\overline{RST}$ output pin. When the DS1374 is not in a reset cycle, it continuously monitors the $\overline{RST}$ signal for a low-going edge. If an edge is detected, the DS1374 debounces the switch by pulling the $\overline{RST}$ pin low and inhibits read/write access. After the internal 250ms timer has expired, the device continues to monitor the $\overline{RST}$ line. If the line is still low, the DS1374 continues to monitor the line, looking for a rising edge. Upon detecting release, the DS1374 forces the $\overline{RST}$ pin low and holds it low for an additional 250ms.

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Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{EOSC}$	WACE	WD/$\overline{ALM}$	BBSQW	WDSTR	RS2	RS1	AIE

Special Purpose Registers

The DS1374 has two additional registers (07h–08h) that control the WD/$\overline{ALM}$ counter and the square-wave, interrupt, and reset outputs.

Control Register (07h)

Bit 7/Enable Oscillator ($\overline{EOSC}$). When set to logic 0, the oscillator is started. When set to logic 1, the oscillator is stopped. When this bit is set to logic 1, the oscillator is stopped and the DS1374 is placed into a low-power standby mode (I_{DDR}). This bit is clear (logic 0) when power is first applied. When the DS1374 is powered by V_{CC}, the oscillator is always on regardless of the state of the $\overline{EOSC}$ bit.

Bit 6/WD/$\overline{ALM}$ Counter Enable (WACE). When set to logic 1, the WD/$\overline{ALM}$ counter is enabled. When set to logic 0, the WD/$\overline{ALM}$ counter is disabled, and the 24 bits can be used as NV RAM. This bit is clear (logic 0) when power is first applied.

Bit 5/WD/$\overline{ALM}$ Counter Select (WD/$\overline{ALM}$). When set to logic 0, the counter decrements every second until it reaches zero and is then reloaded and restarted. When set to logic 1, the WD/$\overline{ALM}$ counter decrements every 1/4096 of a second (approximately every 244µs) until it reaches zero, sets the AF bit in the status register, and stops. If any of the WD/$\overline{ALM}$ counter registers are accessed before the counter reaches zero, the counter is reloaded and restarted. This bit is clear (logic 0) when power is first applied.

Bit 4/Battery-Backed Square-Wave Enable (BBSQW). This bit, when set to logic 1, enables the square-wave output when V_{CC} is absent and when the DS1374 is being powered by the V_{BACKUP} pin. When BBSQW is logic 0, the SQW pin goes high impedance when V_{CC} falls below the power-fail trip point. This bit is disabled (logic 0) when power is first applied.

Bit 3/Watchdog Reset Steering Bit (WDSTR). This bit selects which output pin the watchdog-reset signal occurs on. When the WDSTR bit is set to logic 0, a 250ms pulse occurs on the $\overline{RST}$ pin if WD/$\overline{ALM}$ = 1 and the WD/$\overline{ALM}$ counter reaches zero. The 250ms reset pulse occurs on the $\overline{INT}$ pin when the WDSTR bit is set to logic 1. This bit is logic 0 when power is first applied.

Bits 2, 1/Rate Select (RS2 and RS1). These bits control the frequency of the square-wave output when the square wave has been enabled. Table 4 shows the square-wave frequencies that can be selected with the RS bits. These bits are both set (logic 1) when power is first applied.

Bit 0/Alarm Interrupt Enable (AIE). When set to logic 1, this bit permits the alarm flag (AF) bit in the status register to assert $\overline{INT}$ (when WDSTR = 1). When set to logic 0 or WDSTR is set to logic 0, the AF bit does not initiate the $\overline{INT}$ signal. If the WD/$\overline{ALM}$ bit is set to logic 1 and the AF flag is set, writing AIE to zero does not truncate the 250ms pulse on the $\overline{INT}$ pin. The AIE bit is at logic 0 when power is first applied. The $\overline{INT}$ output is available while the device is powered by either supply.

Table 4. Square-Wave Output Frequency

RS2	RS1	SQUARE-WAVE OUTPUT FREQUENCY
0	0	1Hz
0	1	4.096kHz
1	0	8.192kHz
1	1	32.768kHz

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OSF	0	0	0	0	0	0	AF

Status Register (08h)

Bit 7/Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period of time and can be used to judge the validity of the timekeeping data. This bit is set to logic 1 any time the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltage present on both V_{CC} and V_{BACKUP} are insufficient to support oscillation.
3) The $\overline{EOSC}$ bit is turned off.
4) External influences on the crystal (i.e., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0.

Bit 0/Alarm Flag (AF). A logic 1 in the alarm flag bit indicates that the WD/$\overline{ALM}$ counter reached zero. If WD/$\overline{ALM}$ is set to zero and the AIE bit = 1, the $\overline{INT}$ pin goes low and stays low until AF is cleared. AF is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write logic 1 leaves the value unchanged. If WD/$\overline{ALM}$ is set to 1 and the AIE bit = 1, the $\overline{INT}$ pin pulses low for 250ms when the WD/$\overline{ALM}$ counter reaches zero and sets AF = 1. At the pulse completion, the DS1374 clears the AF bit to zero. If the 250ms pulse is active, writing AF to zero does not truncate the pulse.

Trickle-Charge Register (10h)

The simplified schematic in Figure 7 shows the basic components of the trickle charger. The trickle-charge select (TCS) bits (bits 4–7) control the selection of the trickle charger. To prevent accidental enabling, only a pattern of 1010 enables the trickle charger. All other patterns disable the trickle charger. The trickle charger is disabled when power is first applied. The diode select (DS) bits (bits 2, 3) select whether or not a diode is connected between V_{CC} and V_{BACKUP}. If DS is 01, no diode is selected; if DS is 10, a diode is selected. The ROUT bits (bits 0, 1) select the value of the resistor connected between V_{CC} and V_{BACKUP}. Table 5 shows the resistor selected by the resistor select (ROUT) bits and the diode selected by the diode select (DS) bits.

Warning: The ROUT value of 250Ω must not be selected whenever V_{CC} is greater than 3.63V.

The user determines diode and resistor selection according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example.

Assume that a system power supply of 3.3V is applied to V_{CC} and a super cap is connected to V_{BACKUP}. Also assume the trickle charger has been enabled with a diode and resistor R2 between V_{CC} and V_{BACKUP}. The maximum current I_{MAX} would therefore be calculated as follows:

$$I_{MAX} = (3.3V - \text{diode drop}) / R2 \approx (3.3V - 0.7V) / 2k\Omega \approx 1.3mA$$

As the super cap changes, the voltage drop between V_{CC} and V_{BACKUP} decreases and therefore the charge current decreases.

Table 5. Trickle Charge Register

TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	FUNCTION
X	X	X	X	0	0	X	X	Disabled
X	X	X	X	1	1	X	X	Disabled
X	X	X	X	X	X	0	0	Disabled
1	0	1	0	0	1	0	1	No diode, 250Ω resistor
1	0	1	0	1	0	0	1	One diode, 250Ω resistor
1	0	1	0	0	1	1	0	No diode, 2kΩ resistor
1	0	1	0	1	0	1	0	One diode, 2kΩ resistor
1	0	1	0	0	1	1	1	No diode, 4kΩ resistor
1	0	1	0	1	0	1	1	One diode, 4kΩ resistor
0	0	0	0	0	0	0	0	Power-on reset value

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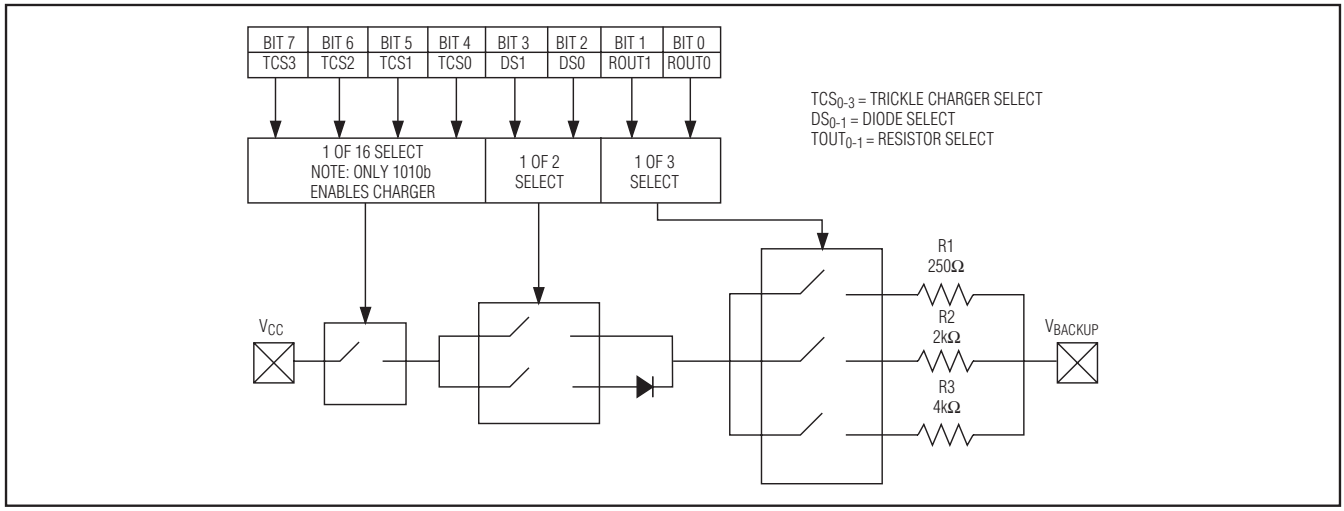

Figure 7. Programmable Trickle Charger

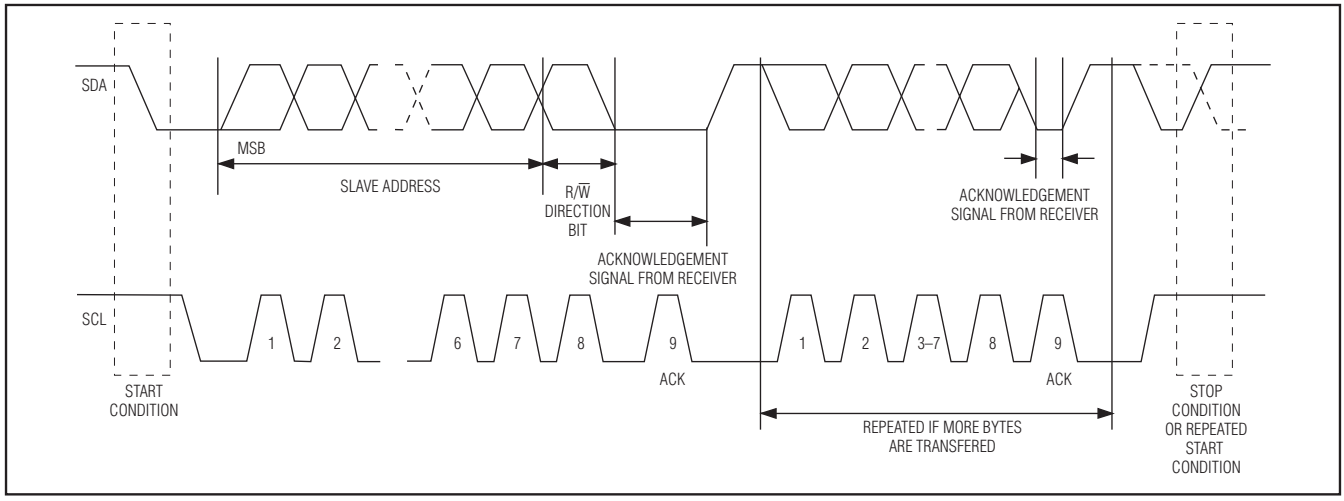

Figure 8. I²C Data Transfer Overview

I²C Serial Data Bus

The DS1374 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data is a receiver. The device that controls the message is called a master. The devices that are controlled by the master are slaves. A master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions must control the bus. The DS1374 operates as a slave on the I²C bus. Connections to the bus are made through the open-drain I/O lines SDA and SCL. A standard mode (100kHz max clock rate) and a fast mode (400kHz max clock rate) are defined within the bus specifications. The DS1374 works in both modes.

The following bus protocol has been defined (Figure 8):

- Data transfer can be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high can be interpreted as control signals.

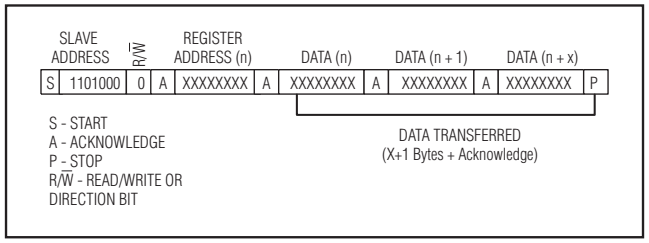

Figure 9. I²C Write Protocol

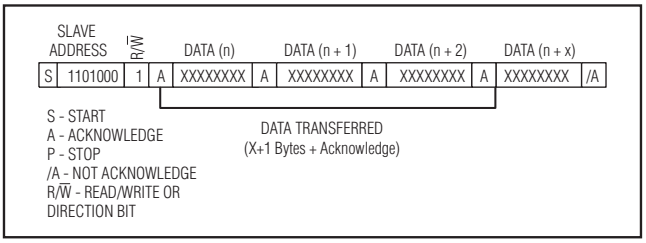

Figure 10. I²C Read Protocol

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain high.

Start data transfer: A change in the state of the data line from high to low, while the clock line is high, defines a START condition.

Stop data transfer: A change in the state of the data line from low to high, while the clock line is high, defines a STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and the STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit. A standard mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined within the I²C bus specifications.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse. Setup and hold times must be considered. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the STOP condition.

Figures 9 and 10 detail how data transfer is accomplished on the 2-wire bus. Depending on the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.

Data transfer from a slave transmitter to a master receiver. The master transmits the first byte (the slave address). The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned.

The master device generates the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released.

The DS1374 can operate in the following two modes:

Slave Receiver Mode (Write Mode): Serial data and clock data are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit. The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit DS1374 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which is zero for a write. After receiving and decoding the slave address byte, the DS1374 outputs an acknowledge on SDA.

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After the DS1374 acknowledges the slave address + write bit, the master transmits a register address to the DS1374. This sets the register pointer on the DS1374, with the DS1374 acknowledging the transfer. The master can then transmit zero or more bytes of data, with the DS1374 acknowledging each byte received. The register pointer increments after each data byte is transferred. The master generates a STOP condition to terminate the data write.

Slave Transmitter Mode (Read Mode): The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1374, while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit. The slave address byte is the first byte received after the START condition is generated by the master. The slave address byte contains the 7-bit DS1374 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which is 1 for a read. After receiving and decoding the slave address byte, the DS1374 outputs an acknowledge on SDA. The DS1374 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode, the first address that is read is the last one stored in the register pointer. The DS1374 must receive a not acknowledge to end a read.

Handling, PC Board Layout, and Assembly

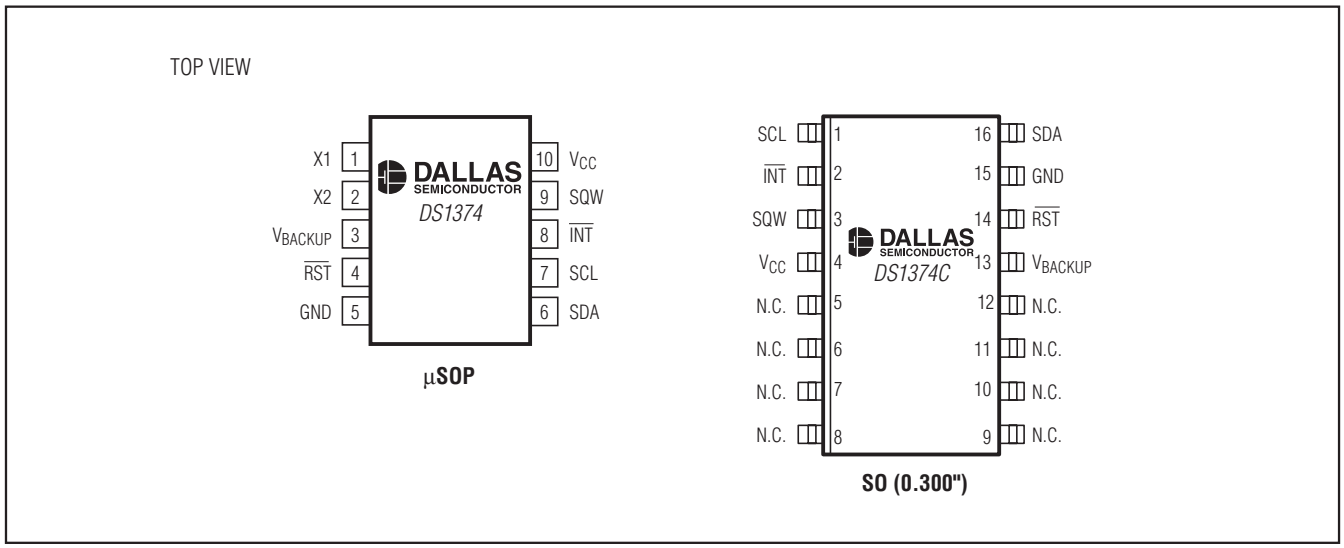
The DS1374C package contains a quartz tuning-fork crystal. Pick-and-place equipment can be used, but precautions should be taken to ensure that excessive shocks are avoided. Ultrasonic cleaning should be avoided to prevent damage to the crystal.

Avoid running signal traces under the package, unless a ground plane is placed between the package and the signal line. All no connect (N.C.) pins must be connected to ground.

Moisture-sensitive packages are shipped from the factory dry-packed. Handling instructions listed on the package label must be followed to prevent damage during reflow. Refer to the IPC/JEDEC J-STD-020 standard for moisture-sensitive device (MSD) classifications.

I²C, 32-Bit Binary Counter Watchdog RTC with Trickle Charger and Reset Input/Output

Pin Configurations



Chip Information

PROCESS: CMOS

SUBSTRATE CONNECTED TO GROUND

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 SO (0.300")	W16#H2	21-0042	90-0107
10 µSOP (3.0mm)	U10+2	21-0061	90-0330

I²C, 32-Bit Binary Counter Watchdog RTC with Trickle Charger and Reset Input/Output

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
3	8/10	Removed leaded parts from the *Ordering Information* table; in the *Absolute Maximum Ratings* section, added the thermal information, lead information, and new Note 1, and updated the soldering information; in the *Control Register (07h)* section, corrected the references of INTCN to WDSTR in the AIE bit description; removed the section about the SO package reflow in the *Handling, PC Board Layout, and Assembly* section; added the land pattern no. to the *Package Information* table	1–5, 12, 16, 17

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