



**THE DATASHEET OF  
DMC2710UDW-7**



## Product Summary

Device	BV <sub>DSS</sub>	R <sub>DS(on)</sub> MAX	I <sub>D</sub> MAX @T <sub>A</sub> = +25°C
Q1	20V	0.45Ω @ V <sub>GS</sub> = 4.5V	0.75A
		0.6Ω @ V <sub>GS</sub> = 2.5V	0.65A
Q2	-20V	0.75Ω @ V <sub>GS</sub> = -4.5V	-0.6A
		1.05Ω @ V <sub>GS</sub> = -2.5V	-0.5A

## Description

This new generation MOSFET is designed to minimize on-state resistance (R<sub>DS(on)</sub>), yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

## Applications

- Battery-Operated Systems and Solid-State Relays
- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories, Transistors, etc.
- Power Supply Converter Circuits

## Features and Benefits

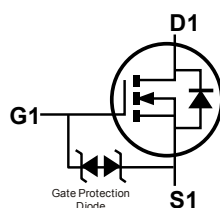
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Complementary Pair MOSFET
- Ultra-Small Surface Mount Package
- ESD-Protected
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3)**
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](mailto:contact@diodes.com) or your local Diodes representative. <https://www.diodes.com/quality/product-definitions/>**

## Mechanical Data

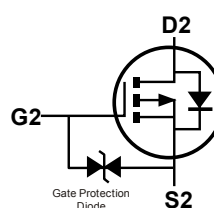
- Case: SOT363
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish Annealed over Alloy 42 Leadframe (Lead Free Plating). Solderable per MIL-STD-202, Method 208 <sup>(e3)</sup>
- Terminal Connections: See Diagram
- Weight: 0.006 grams (Approximate)



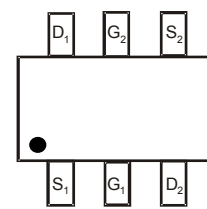
Top View



Q1 N-Channel



Q2 P-Channel



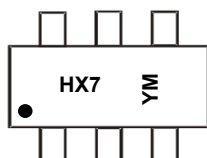
Top View Pin-Out

## Ordering Information (Note 4)

Part Number	Case	Packaging
DMC2710UDW-7	SOT363	3000/Tape & Reel
DMC2710UDW-13	SOT363	10000/Tape & Reel

- Notes:
- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
  - See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  - Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  - For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

## Marking Information



HX7 = Product Type Marking Code  
 YM or YM = Date Code Marking  
 Y or Y = Year (ex: I = 2021)  
 M = Month (ex: 9 = September)

### Date Code Key

Year	2018	.....	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Code	F	.....	I	J	K	L	M	N	O	P	R	S
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

**Maximum Ratings** (@  $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic		Symbol	Q1 Value	Q2 Value	Unit
Drain-Source Voltage		$V_{DS}$	20	-20	V
Gate-Source Voltage		$V_{GS}$	$\pm 6$	$\pm 6$	V
Continuous Drain Current (Note 6) N-Channel: $V_{GS} = 4.5\text{V}$ P-Channel: $V_{GS} = -4.5\text{V}$	Steady State	$I_D$	0.75 0.6	-0.6 -0.47	A
Maximum Continuous Body Diode Forward Current (Note 6)		$I_S$	0.5	-0.4	A
Pulsed Drain Current (10 $\mu\text{s}$ Pulse, Duty Cycle = 1%)		$I_{DM}$	5	-2.5	A

**Thermal Characteristics** (@  $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	$T_A = +25^\circ\text{C}$	$P_D$	0.29	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	433	$^\circ\text{C/W}$
Total Power Dissipation (Note 6)	$T_A = +25^\circ\text{C}$	$P_D$	0.38	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	325	$^\circ\text{C/W}$
Operating and Storage Temperature Range		$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$

**Electrical Characteristics N-CHANNEL – Q1** (@  $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	20	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current	$I_{DSS}$	—	—	100	nA	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	$I_{GSS}$	—	—	$\pm 1.0$	$\mu\text{A}$	$V_{GS} = \pm 4.5\text{V}, V_{DS} = 0\text{V}$
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	$V_{GS(th)}$	0.5	—	1.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	0.18	0.45	$\Omega$	$V_{GS} = 4.5\text{V}, I_D = 600\text{mA}$
			0.21	0.6		$V_{GS} = 2.5\text{V}, I_D = 500\text{mA}$
			0.26	0.75		$V_{GS} = 1.8\text{V}, I_D = 350\text{mA}$
Diode Forward Voltage (Note 7)	$V_{SD}$	—	0.7	1.2	V	$V_{GS} = 0\text{V}, I_S = 150\text{mA}$
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	$C_{iss}$	—	42	—	pF	$V_{DS} = 16\text{V}, V_{GS} = 0\text{V}$ $f = 1.0\text{MHz}$
Output Capacitance	$C_{oss}$	—	13	—	pF	
Reverse Transfer Capacitance	$C_{rss}$	—	6.5	—	pF	
Total Gate Charge	$Q_g$	—	0.6	—	nC	$V_{GS} = 4.5\text{V}, V_{DS} = 10\text{V},$ $I_D = 250\text{mA}$
Gate-Source Charge	$Q_{gs}$	—	0.1	—	nC	
Gate-Drain Charge	$Q_{gd}$	—	0.1	—	nC	
Turn-On Delay Time	$t_{D(on)}$	—	4.9	—	ns	$V_{DD} = 10\text{V}, V_{GS} = 4.5\text{V},$ $R_L = 47\Omega, R_g = 10\Omega$ $I_D = 200\text{mA}$
Turn-On Rise Time	$t_R$	—	3.1	—	ns	
Turn-Off Delay Time	$t_{D(off)}$	—	386	—	ns	
Turn-Off Fall Time	$t_F$	—	174	—	ns	
Reverse Recovery Time	$t_{RR}$	—	88	—	ns	$I_F = 1\text{A}, di/dt = 100\text{A}/\mu\text{s}$
Reverse Recovery Charge	$Q_{RR}$	—	29	—	nC	

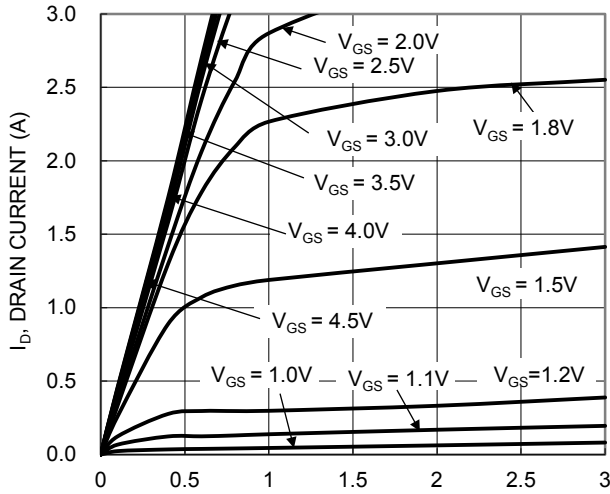
- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
  - Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
  - Short duration pulse test used to minimize self-heating effect.
  - Guaranteed by design. Not subject to production testing.

**Electrical Characteristics P-CHANNEL – Q2** (@ T<sub>A</sub> = +25°C, unless otherwise specified.)

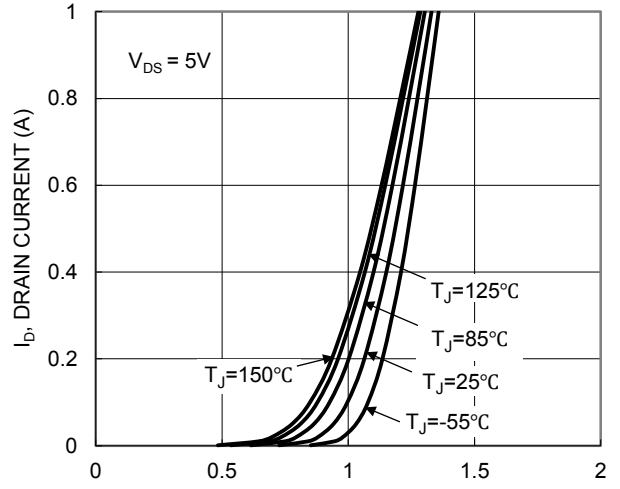
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-20	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	-100	nA	V <sub>DS</sub> = -20V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±2.0	μA	V <sub>GS</sub> = ±4.5V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	-0.5	—	-1.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	—	0.48	0.75	Ω	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -430mA
			0.6	1.05		V <sub>GS</sub> = -2.5V, I <sub>D</sub> = -300mA
			0.76	1.5		V <sub>GS</sub> = -1.8V, I <sub>D</sub> = -150mA
Diode Forward Voltage (Note 7)	V <sub>SD</sub>	—	-0.7	-1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -150mA
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	C <sub>iss</sub>	—	49	—	pF	V <sub>DS</sub> = -16V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>oss</sub>	—	12	—	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	—	3.4	—	pF	
Total Gate Charge	Q <sub>g</sub>	—	0.7	—	nC	V <sub>GS</sub> = -4.5V, V <sub>DS</sub> = -10V, I <sub>D</sub> = -250mA
Gate-Source Charge	Q <sub>gs</sub>	—	0.1	—	nC	
Gate-Drain Charge	Q <sub>gd</sub>	—	0.1	—	nC	
Turn-On Delay Time	t <sub>D(on)</sub>	—	16	—	ns	V <sub>DS</sub> = -10V, V <sub>GS</sub> = -4.5V, R <sub>g</sub> = 10Ω, R <sub>L</sub> = 47Ω I <sub>D</sub> = -200mA
Turn-On Rise Time	t <sub>r</sub>	—	15	—	ns	
Turn-Off Delay Time	t <sub>D(off)</sub>	—	213	—	ns	
Turn-Off Fall Time	t <sub>f</sub>	—	89	—	ns	
Reverse Recovery Time	t <sub>RR</sub>	—	10.5	—	ns	I <sub>F</sub> = 1A, di/dt = 100A/μs
Reverse Recovery Charge	Q <sub>RR</sub>	—	1.8	—	nC	

Notes: 7. Short duration pulse test used to minimize self-heating effect.  
8. Guaranteed by design. Not subject to production testing.

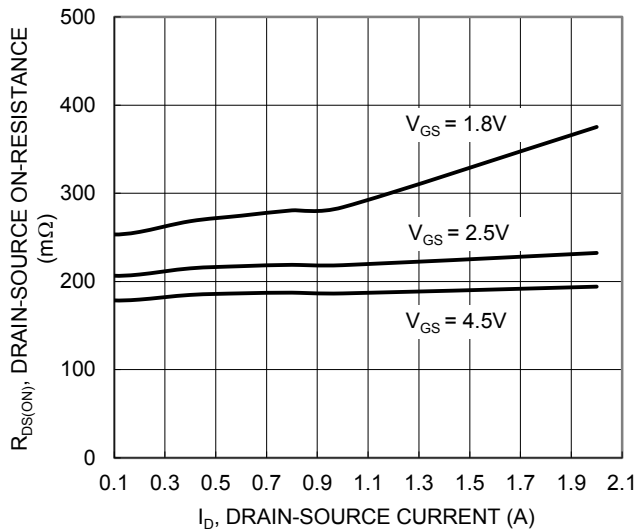
**Typical Characteristics - N-CHANNEL**



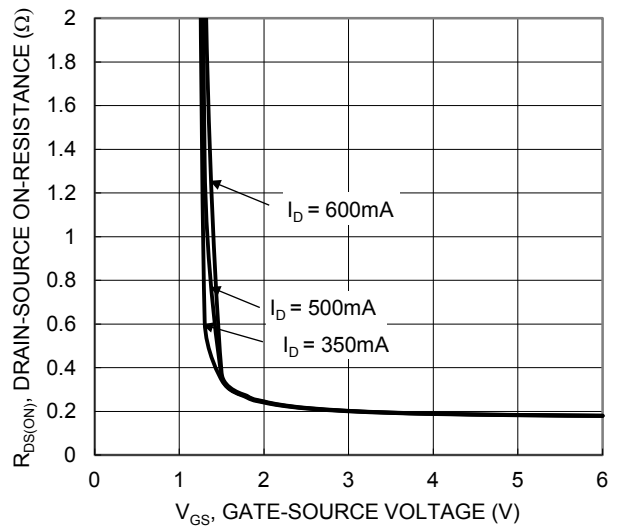
$V_{DS}$ , DRAIN-SOURCE VOLTAGE (V)  
Figure 1. Typical Output Characteristic



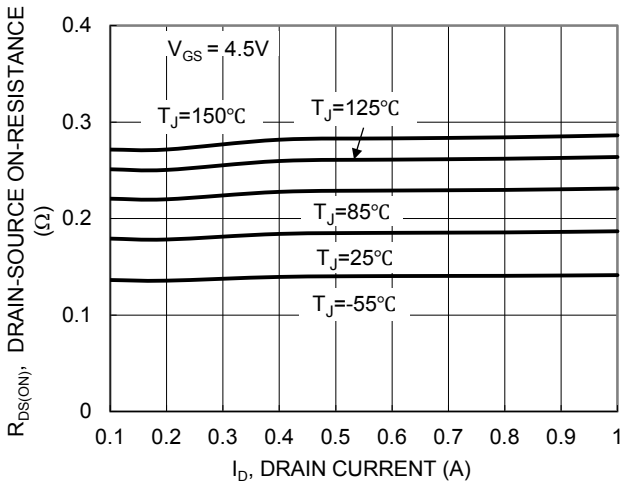
$V_{GS}$ , GATE-SOURCE VOLTAGE (V)  
Figure 2. Typical Transfer Characteristic



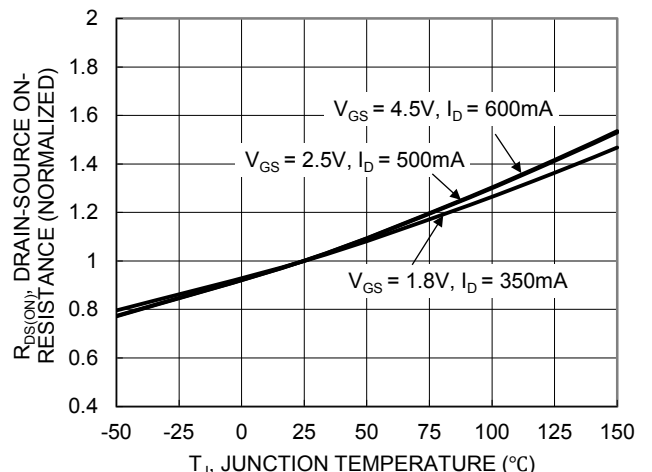
$I_D$ , DRAIN-SOURCE CURRENT (A)  
Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage



$V_{GS}$ , GATE-SOURCE VOLTAGE (V)  
Figure 4. Typical Transfer Characteristic



$I_D$ , DRAIN CURRENT (A)  
Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature



$T_J$ , JUNCTION TEMPERATURE ( $^\circ C$ )  
Figure 6. On-Resistance Variation with Junction Temperature

**Typical Characteristics - N-CHANNEL** (continued)

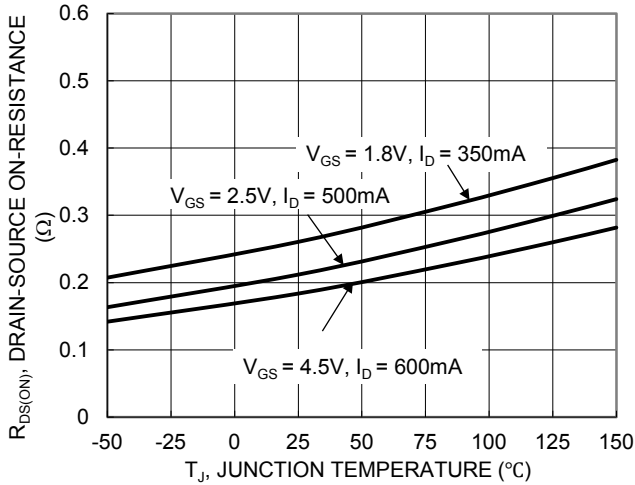


Figure 7. On-Resistance Variation with Junction Temperature

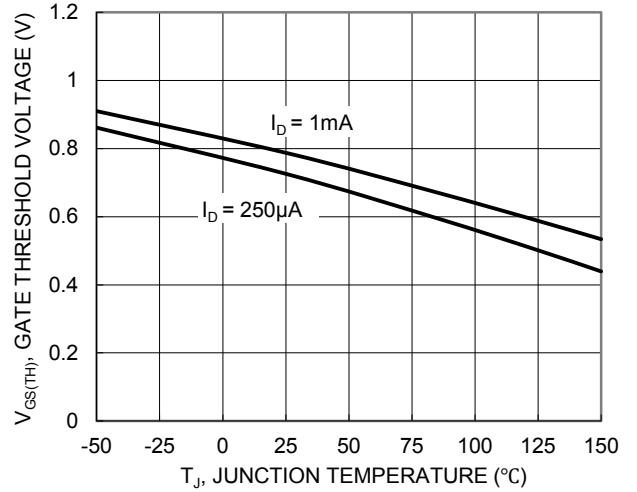


Figure 8. Gate Threshold Variation vs. Junction Temperature

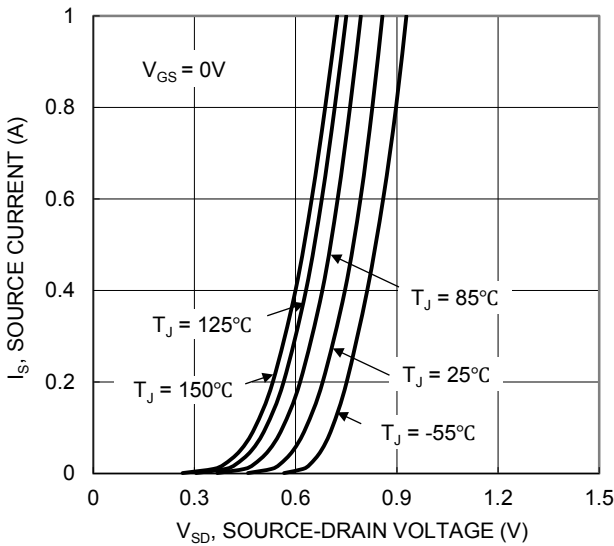


Figure 9. Diode Forward Voltage vs. Current

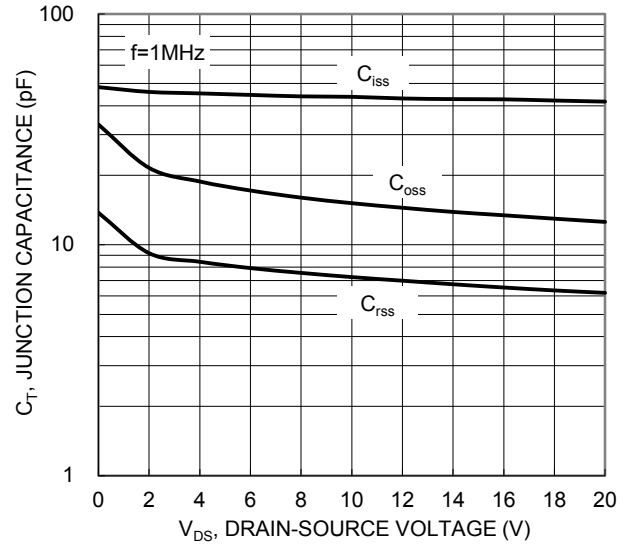


Figure 10. Typical Junction Capacitance

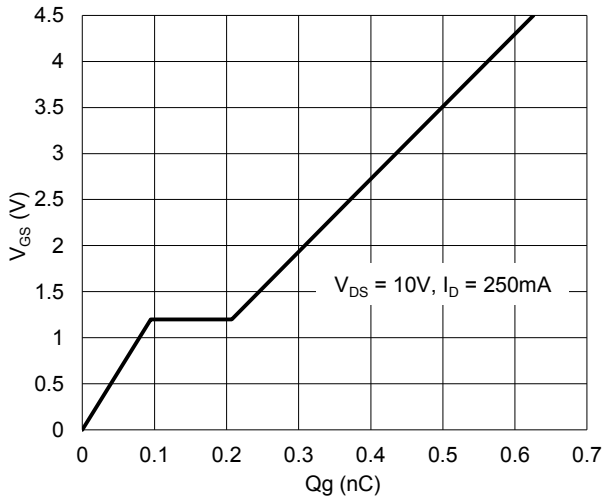


Figure 11. Gate Charge

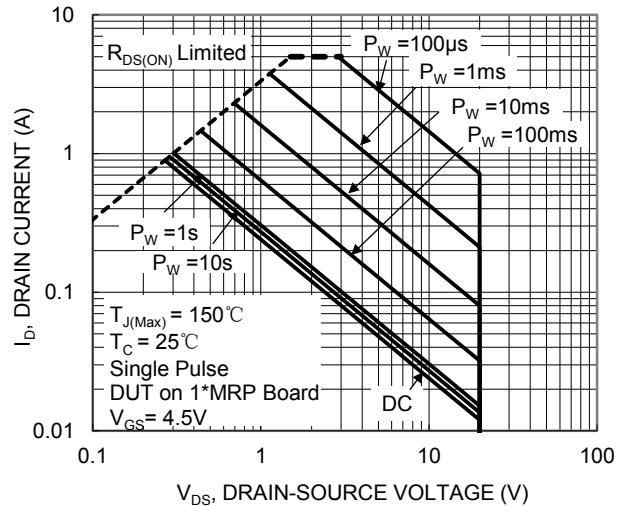


Figure 12. SOA, Safe Operation Area

**Typical Characteristics - P-CHANNEL**

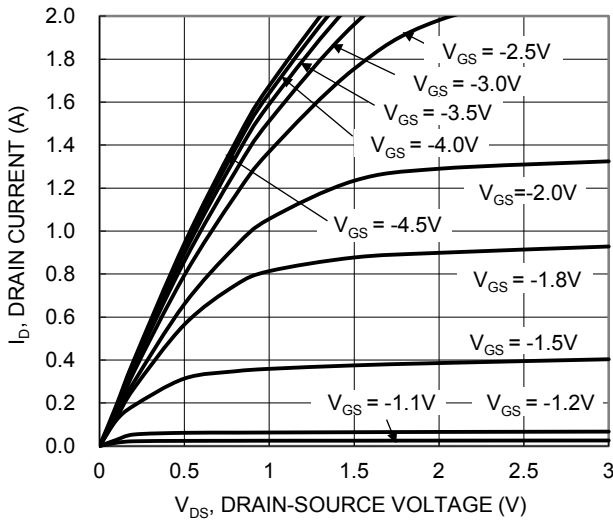


Figure 13. Typical Output Characteristic

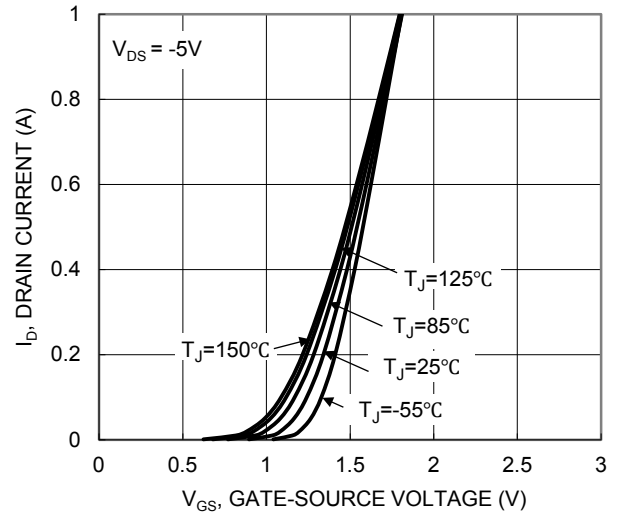


Figure 14. Typical Transfer Characteristic

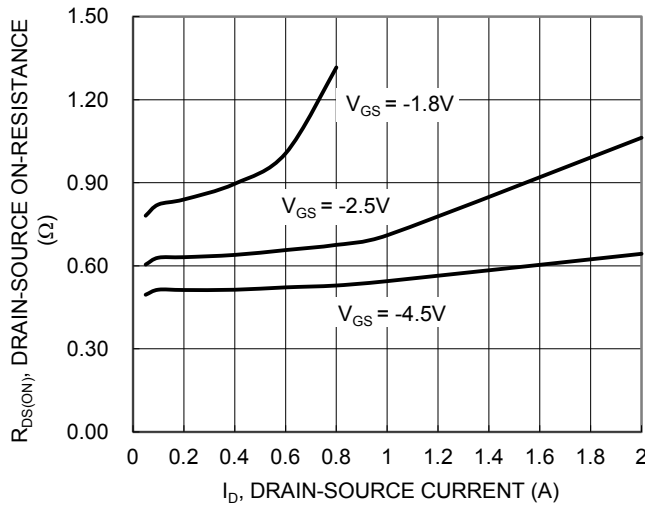


Figure 15. Typical On-Resistance vs. Drain Current and Gate Voltage

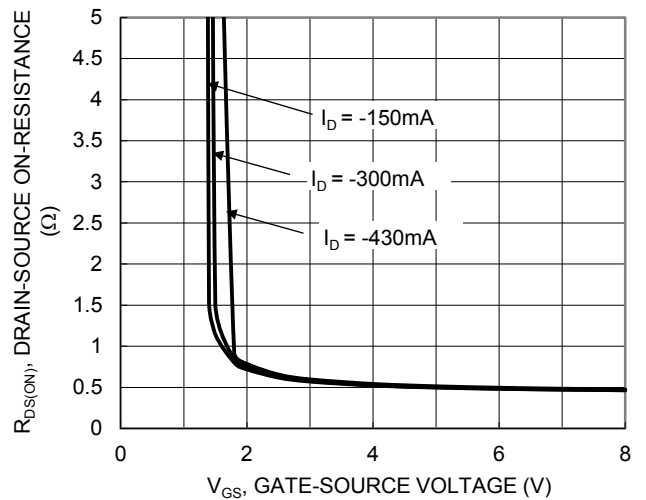


Figure 16. Typical Transfer Characteristic

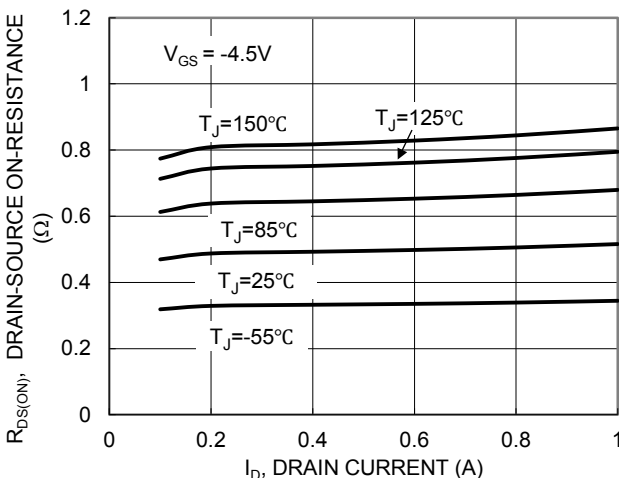


Figure 17. Typical On-Resistance vs. Drain Current and Temperature

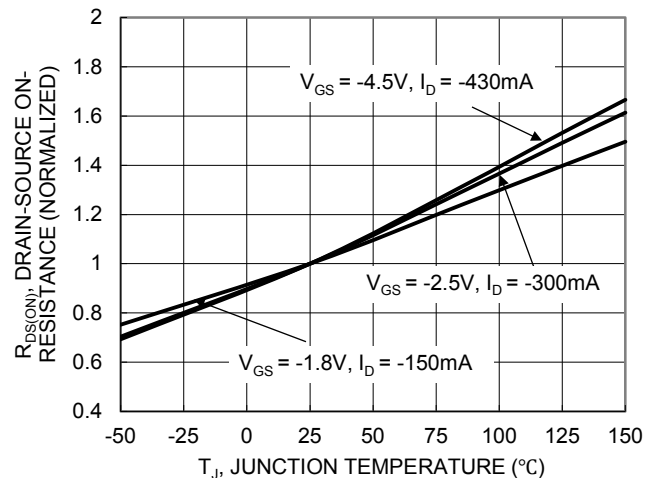


Figure 18. On-Resistance Variation with Temperature

**Typical Characteristics - P-CHANNEL** (continued)

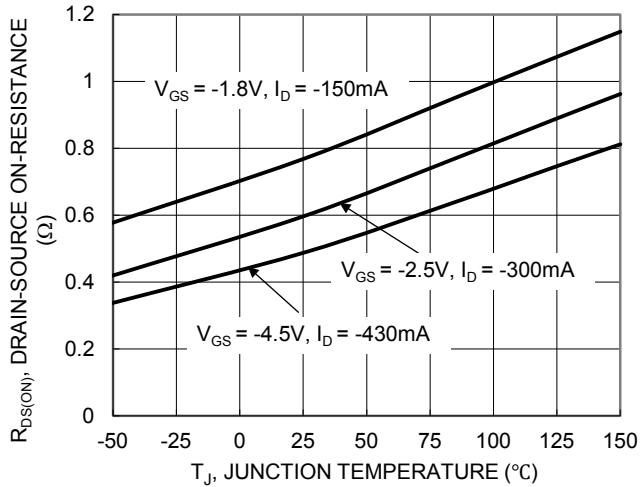


Figure 19. On-Resistance Variation with Temperature

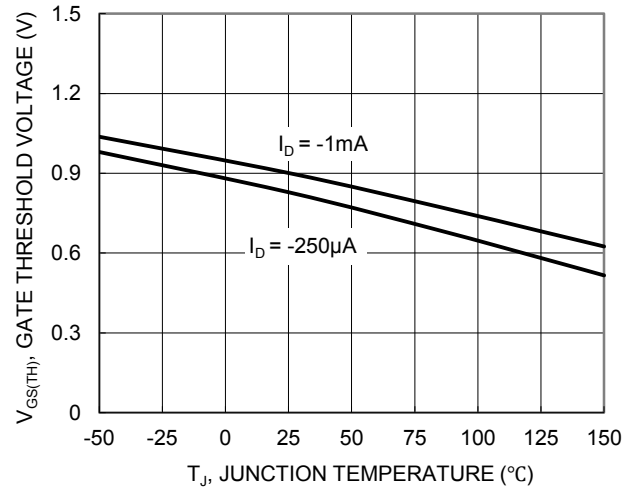


Figure 20. Gate Threshold Variation vs. Junction Temperature

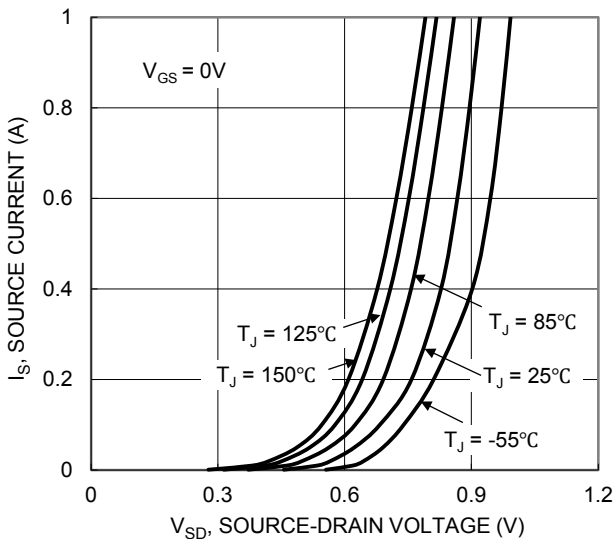


Figure 21. Diode Forward Voltage vs. Current

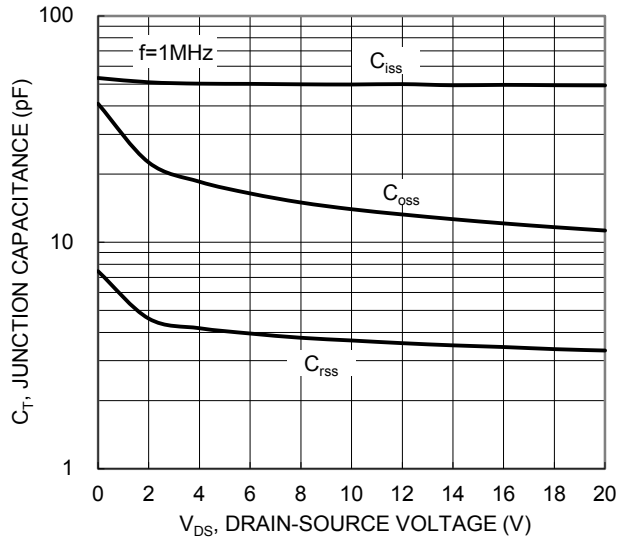


Figure 22. Typical Junction Capacitance

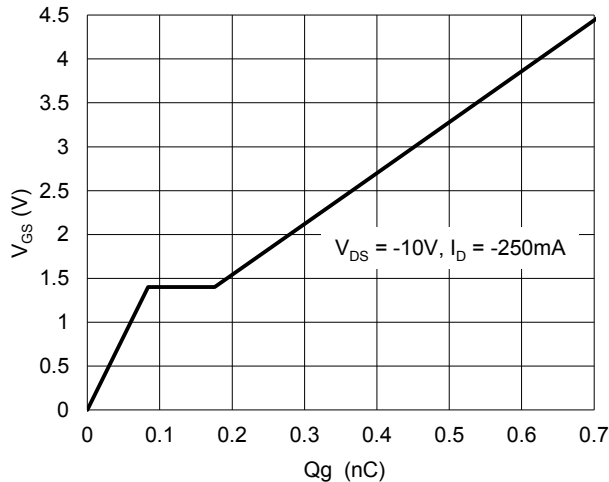


Figure 23. Gate Charge

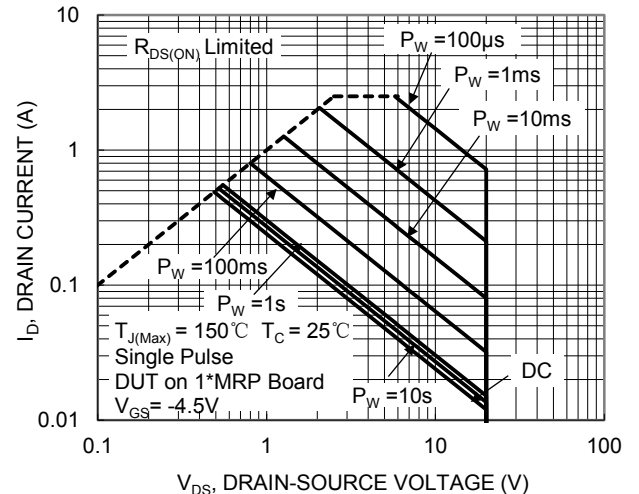


Figure 24. SOA, Safe Operation Area

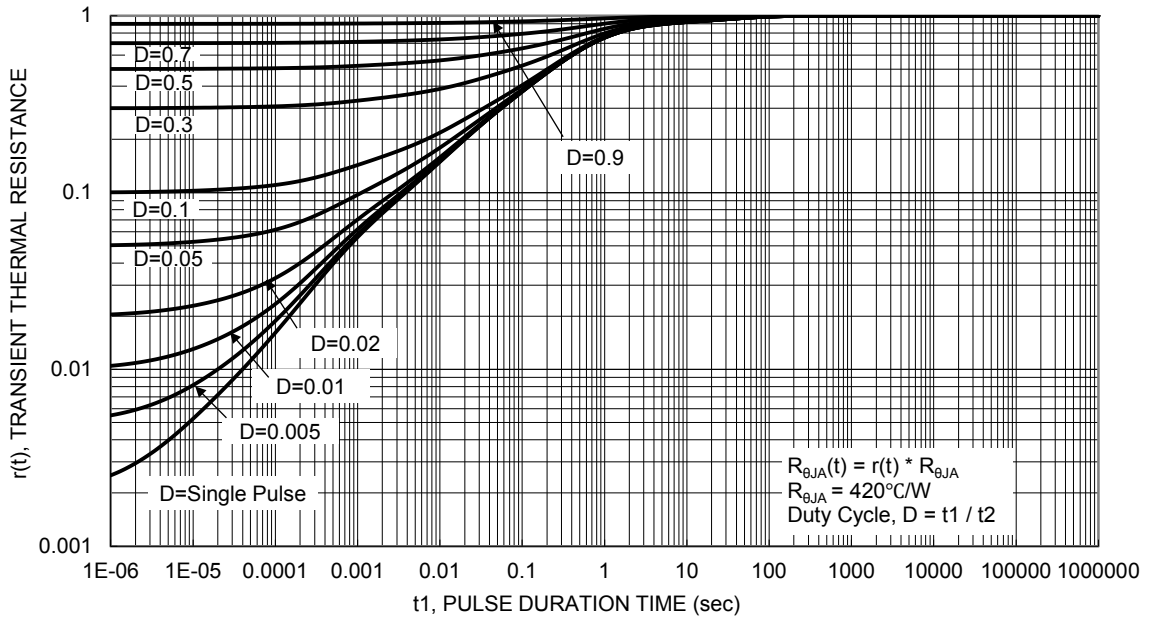
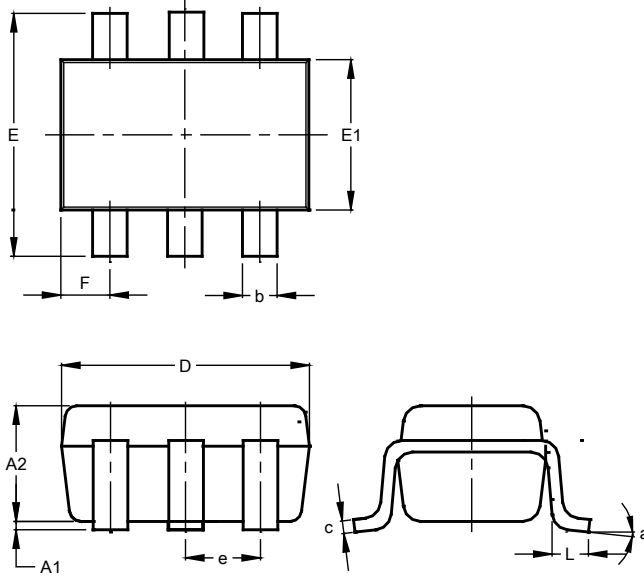


Figure 25. Transient Thermal Resistance

**Package Outline Dimensions**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**SOT363**

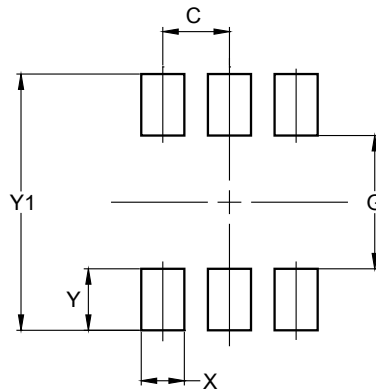


SOT363			
Dim	Min	Max	Typ
A1	0.00	0.10	0.05
A2	0.90	1.00	0.95
b	0.10	0.30	0.25
c	0.10	0.22	0.11
D	1.80	2.20	2.15
E	2.00	2.20	2.10
E1	1.15	1.35	1.30
e	0.650 BSC		
F	0.40	0.45	0.425
L	0.25	0.40	0.30
a	0°	8°	--
All Dimensions in mm			

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**SOT363**



Dimensions	Value (in mm)
C	0.650
G	1.300
X	0.420
Y	0.600
Y1	2.500

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-  Alternative Solution
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