THE DATASHEET OF

CY9BF114NPMC-G-JNE2

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Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

CY9B110R Series

32-bit Arm® Cortex®-M3 FM3 Microcontroller

The CY9B110R Series are a highly integrated 32-bit microcontrollers dedicated for embedded controllers with high-performance and competitive cost. These series are based on the Arm Cortex-M3 Processor with on-chip Flash memory and SRAM, and has peripheral functions such as Motor Control Timers, ADCs and Communication Interfaces (UART, CSIO, I²C, LIN). The products which are described in this data sheet are placed into TYPE4 product categories in FM3 Family Peripheral Manual.

Features

32-bit Arm Cortex-M3 Core

- Processor version: r2p1
- Up to 144 MHz Frequency Operation
- Memory Protection Unit (MPU): improves the reliability of an embedded system
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 48 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

On-chip Memories

[Flash memory]

These series are based on two independent on-chip Flash memories.

- MainFlash
  - Up to 512 Kbyte
  - Built-in Flash Accelerator System with 16 Kbyte trace buffer memory
  - The read access to Flash memory can be achieved without wait cycle up to operation frequency of 72 MHz. Even at the operation frequency more than 72 MHz, an equivalent access to Flash memory can be obtained by Flash Accelerator System.
  - Security function for code protection
- WorkFlash
  - 32 Kbyte
  - Read cycle
  - 4 wait-cycle: the operation frequency more than 72 MHz
  - 2 wait-cycle: the operation frequency more than 40 MHz, and to 72 MHz
  - 0wait-cycle: the operation frequency to 40 MHz
  - Security function is shared with code protection

[SRAM]

This Series contain a total of up to 64 Kbyte on-chip SRAM. This is composed of two independent SRAM (SRAM0, SRAM1). SRAM0 is connected to I-code bus and D-code bus of Cortex-M3 core. SRAM1 is connected to System bus.

- SRAM0: Up to 32 Kbyte
- SRAM1: Up to 32 Kbyte

External Bus Interface

- Supports SRAM, NOR and NAND Flash device
- Up to 8 chip selects
- 8-/16-bit Data width
- Up to 25-bit Address bit
- Maximum area size: Up to 256 Mbytes
- Supports Address/Data multiplex
- Supports external RDY input

Multi-function Serial Interface (Max eight channels)

- 4 channels with 16 steps×9-bit FIFO (ch.4-ch.7), 4 channels without FIFO (ch.0-ch.3)
- Operation mode is selectable from the followings for each channel.
  - UART
  - CSIO
  - LIN
  - I²C
- UART
  - Full-duplex double buffer
  - Selection with or without parity supported
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Hardware Flow control: Automatically control the transmission by CTS/RTS (only ch.4)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- CSIO
  - Full-duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detect function available
- LIN
  - LIN protocol Rev.2.1 supported
  - Full-duplex double buffer
  - Master/Slave mode supported
  - LIN break field generate (can be changed 13 to 16-bit length)
  - LIN break delimiter generate (can be changed 1 to 4-bit length)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- I²C
  - Standard-mode (Max 100 kbps) / Fast-mode (Max 400 kbps) supported

DMA Controller (Eight channels)

DMA Controller has an independent bus for CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32 bit (4 Gbyte)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: byte/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

A/D Converter (Max 16 channels)

- 12-bit A/D Converter
  - Successive Approximation Register type
  - Built-in 3 unit
  - Conversion time: 1.0 µs @ 5 V
  - Priority conversion available (priority at 2 levels)
  - Scanning conversion mode
  - Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for Priority conversion: 4 steps)

Base Timer (Max eight channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General Purpose I/O Port

This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up 103 fast general purpose I/O Ports@120 pin Package
- Some pin is 5 V tolerant I/O.
  See4. List of Pin Functions to confirm the corresponding pins.

Multi-function Timer (Max three units)

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3 ch./unit
- Input capture × 4 ch./unit
- Output compare × 6 ch./unit
- A/D activating compare × 3 ch./unit
- Waveform generator × 3 ch./unit
- 16-bit PPG timer × 3 ch./unit

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

Real-time clock (RTC)

The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 00 to 99.

- Interrupt function with specifying date and time (Year/Month/Day/Hour/Minute) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

Quadrature Position/Revolution Counter (QPRC) (Max three channels)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

Watch Counter

The Watch counter is used for wake up from power consumption mode.

- Interval timer: up to 64 s (Max) @ Sub Clock: 32.768 kHz

External Interrupt Controller Unit

- Up to 16 external interrupt input pin
- Include one non-maskable interrupt (NMI)

Watchdog Timer (Two channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.
This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.
"Hardware" watchdog timer is clocked by low-speed internal CR oscillator. Therefore, "Hardware" watchdog is active in any power consumption mode except Stop mode.

CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator helps a verify data transmission or storage integrity.
CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

Clock and Reset

- Clocks

Five clock sources (2 external oscillators, 2 internal CR oscillator, and Main PLL) that are dynamically selectable.

- Main Clock: 4 MHz to 48 MHz
- Sub Clock: 32.768 kHz
- High-speed internal CR Clock: 4 MHz
- Low-speed internal CR Clock: 100 kHz
- Main PLL Clock

- Resets
  - Reset requests from INITX pin
  - Power on reset
  - Software reset
  - Watchdog timers reset
  - Low-voltage detector reset
  - Clock supervisor reset

Clock Super Visor (CSV)

Clocks generated by internal CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)

This Series include 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-Power Consumption Mode

Three power consumption modes supported.

- Sleep
- Timer
- Stop

Debug

- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocells (ETM) provide comprehensive debug and trace facilities.

Power Supply

- Wide range voltage:
  VCC = 2.7 V to 5.5 V

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1. Product Lineup

Memory Size

Product name		CY9BF112N/R	CY9BF114N/R	CY9BF115N/R	CY9BF116N/R
MainFlash		128 Kbyte	256 Kbyte	384 Kbyte	512 Kbyte
WorkFlash		32 Kbyte	32 Kbyte	32 Kbyte	32 Kbyte
On-chip RAM		16 Kbyte	32 Kbyte	48 Kbyte	64 Kbyte
	SRAM0	8 Kbyte	16 Kbyte	24 Kbyte	32 Kbyte
	SRAM1	8 Kbyte	16 Kbyte	24 Kbyte	32 Kbyte

Function

Product name			CY9BF112N CY9BF114N CY9BF115N CY9BF116N	CY9BF112R CY9BF114R CY9BF115R CY9BF116R
Pin count			100/112	120
CPU			Cortex-M3	
	Freq.		144 MHz	
Power supply voltage range			VCC: 2.7 V to 5.5 V	
DMAC			8 ch.	
External Bus Interface			Addr: 25-bit (Max) R/Wdata: 8-/16-bit (Max) CS: 8 (Max) Support: SRAM, NOR Flash	Addr: 25-bit (Max) R/Wdata: 8-/16-bit (Max) CS: 8 (Max) Support: SRAM, NOR & NAND Flash
MF Serial Interface (UART/CSIO/LIN/I^{2}C)			8 ch. (Max) ch.4 to ch.7: FIFO (16steps × 9-bit) ch.0 to ch.3: No FIFO	
Base Timer (PWC/Reload timer/PWM/PPG)			8 ch. (Max)	
MF-Timer	A/D activation compare	3 ch.	3 units (Max)	
	Input capture	4 ch.		
	Free-run timer	3 ch.		
	Output compare	6 ch.		
	Waveform generator	3 ch.		
	PPG	3 ch.		
QPRC			3 ch. (Max)	
Dual Timer			1 unit	
Real-Time Clock			1 unit	
Watch Counter			1 unit	
CRC Accelerator			Yes	
Watchdog timer			1 ch. (SW) + 1 ch. (HW)	
External Interrupts			16 pins (Max) + NMI × 1	
I/O ports			83 pins (Max)	103 pins (Max)
12-bit A/D converter			16 ch. (3 units)	
CSV (Clock Super Visor)			Yes	
LVD (Low-Voltage Detector)			2 ch.	
Internal OSC	High-speed		4 MHz	
	Low-speed		100 kHz	
Debug Function			SWJ-DP/ETM	

Note:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the General I/O port according to your function use. See 12.4.3 Internal CR Oscillation Characteristics for accuracy of built-in CR.*

2. Packages

Package \ Product name	CY9BF112N CY9BF114N CY9BF115N CY9BF116N	CY9BF112R CY9BF114R CY9BF115R CY9BF116R
QFP: PQH100 (0.65 mm pitch)	❍	-
LQFP: LQI100 (0.5 mm pitch)	❍	-
LQFP: LQM120 (0.5 mm pitch)	-	❍
FBGA: LBC112 (0.8 mm pitch)	❍	-

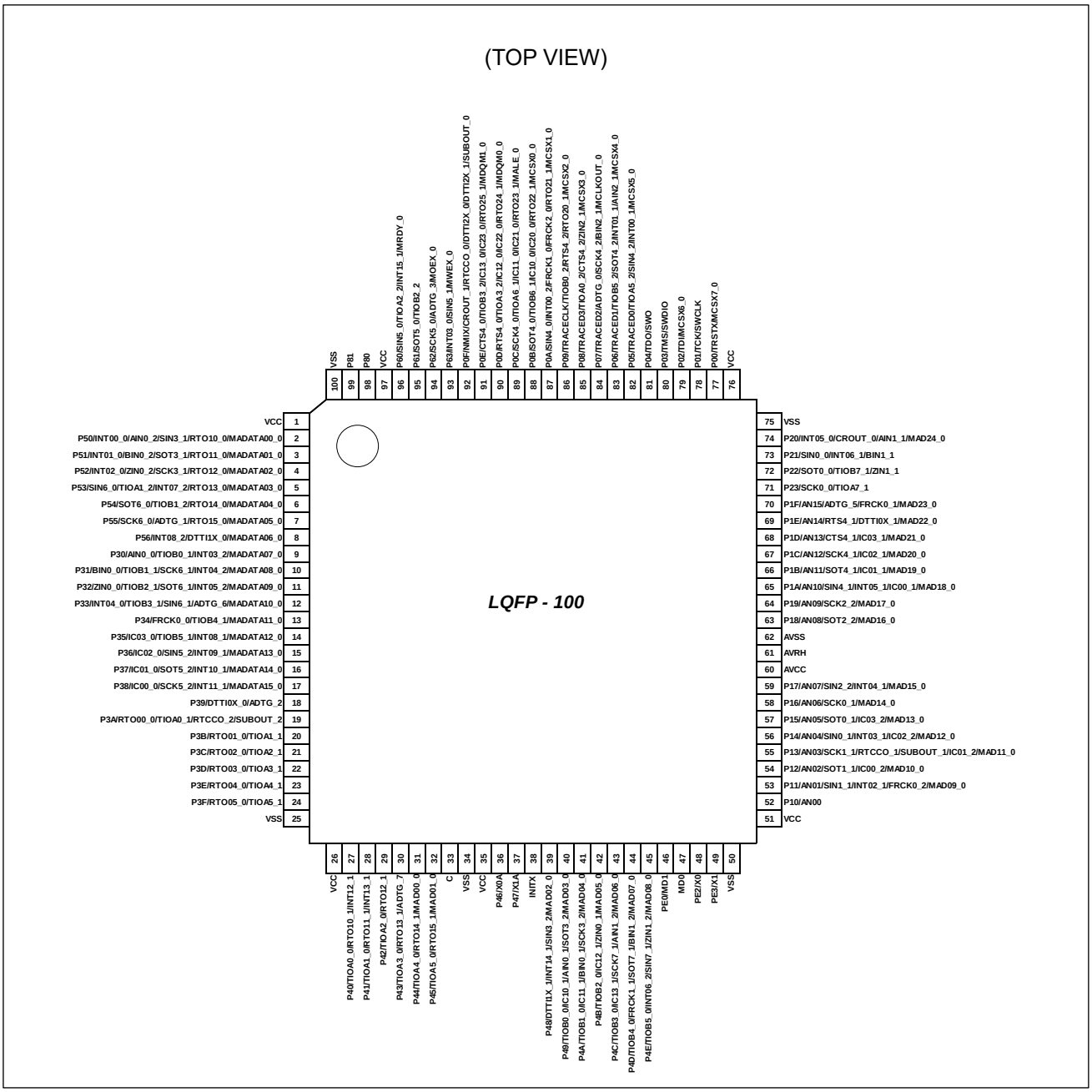
❍: Supported

Note:

- *See 14. Package Dimensions for detailed information on each package.*

3. Pin Assignment

LQI100

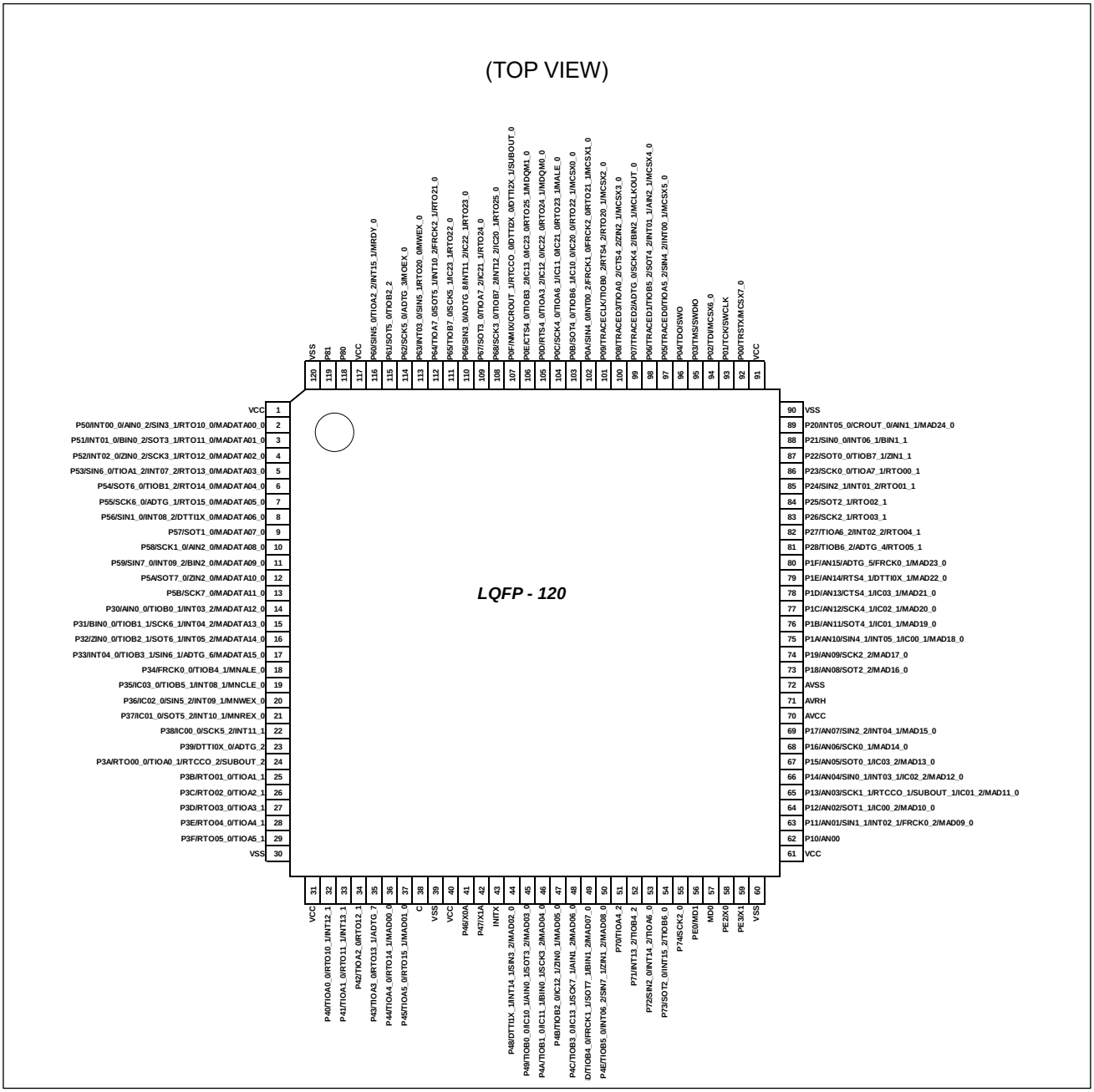


Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.*

  Use the extended port function register (EPFR) to select the pin.

LQM120

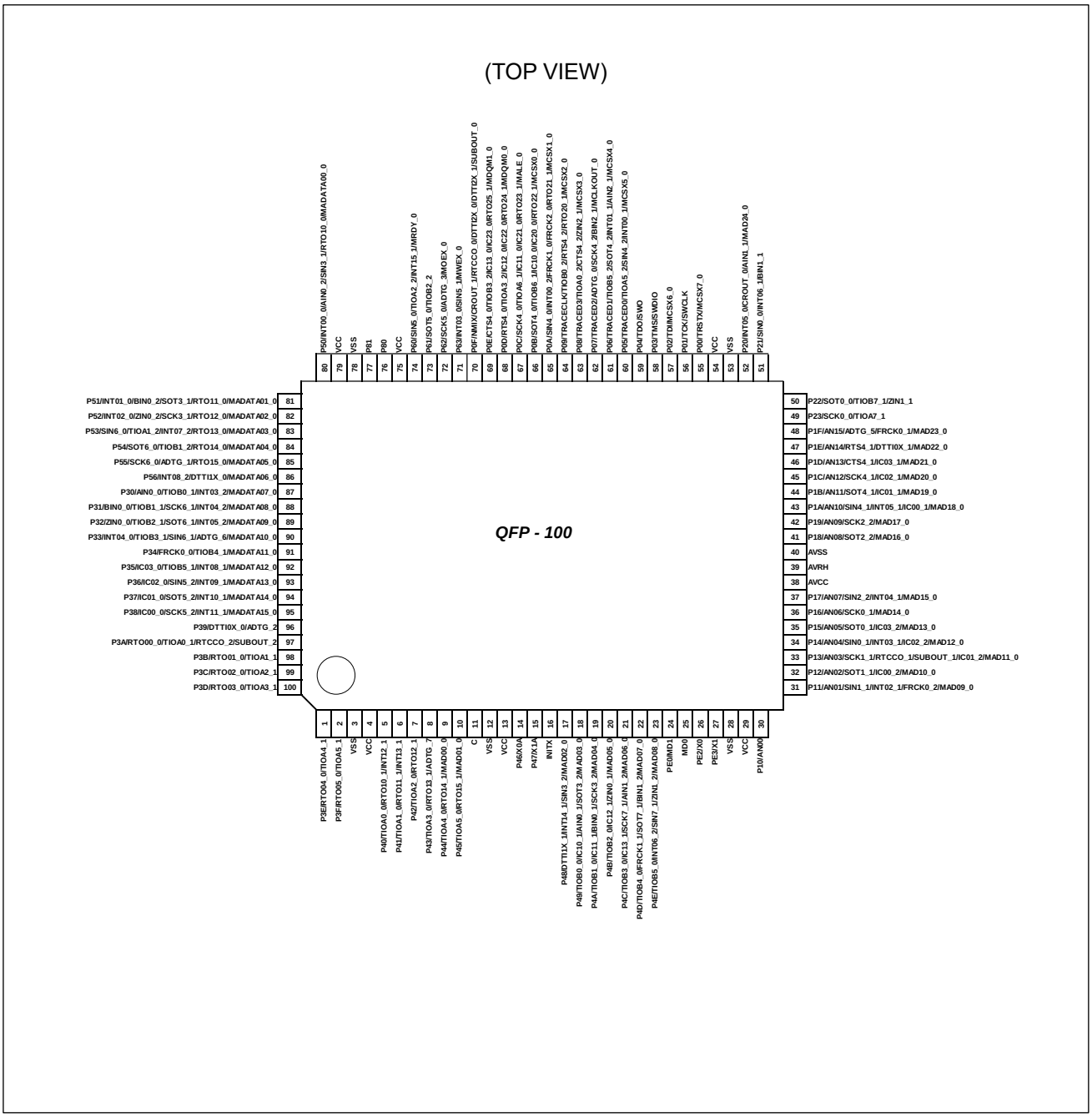


Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.*

  Use the extended port function register (EPFR) to select the pin.

PQH100

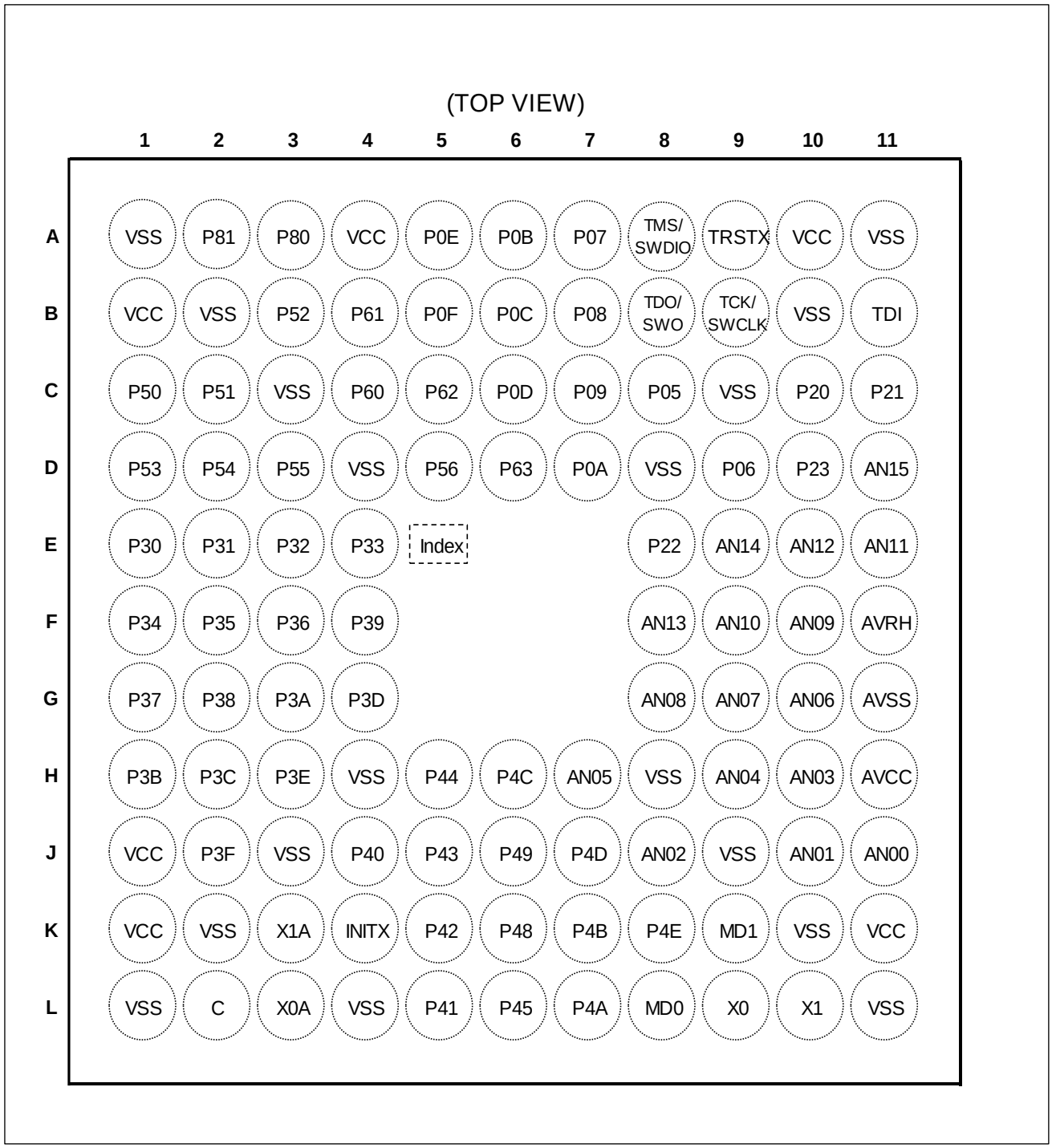


Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.*

  Use the extended port function register (EPFR) to select the pin.

LBC112



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.*

  Use the extended port function register (EPFR) to select the pin.

4. List of Pin Functions

List of pin numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.
Use the extended port function register (EPFR) to select the pin.

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
1	B1	1	79	VCC	-	
2	C1	2	80	P50	E	H
				INT00_0		
				AIN0_2		
				SIN3_1		
				RTO10_0 (PPG10_0)		
				MADATA00_0		
3	C2	3	81	P51	E	H
				INT01_0		
				BIN0_2		
				SOT3_1 (SDA3_1)		
				RTO11_0 (PPG10_0)		
				MADATA01_0		
4	B3	4	82	P52	E	H
				INT02_0		
				ZIN0_2		
				SCK3_1 (SCL3_1)		
				RTO12_0 (PPG12_0)		
				MADATA02_0		
5	D1	5	83	P53	E	H
				SIN6_0		
				TIOA1_2		
				INT07_2		
				RTO13_0 (PPG12_0)		
				MADATA03_0		
6	D2	6	84	P54	E	I
				SOT6_0 (SDA6_0)		
				TIOB1_2		
				RTO14_0 (PPG14_0)		
				MADATA04_0		

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
7	D3	7	85	P55 SCK6_0 (SCL6_0) ADTG_1 RTO15_0 (PPG14_0) MADATA05_0	E	I
8	D5	8	86	P56 INT08_2 DTTI1X_0 MADATA06_0	E	H
-	-		-	SIN1_0 (120pin only)		
-	-	9	-	P57 SOT1_0 (SDA1_0) MADATA07_0	E	I
-	-	10	-	P58 SCK1_0 (SCL1_0) AIN2_0 MADATA08_0	E	I
-	-	11	-	P59 SIN7_0 INT09_2 BIN2_0 MADATA09_0	E	H
-	-	12	-	P5A SOT7_0 (SDA7_0) ZIN2_0 MADATA10_0	E	I
-	-	13	-	P5B SCK7_0 (SCL7_0) MADATA11_0	E	I

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
9	E1	14	87	P30 AIN0_0 TIOB0_1 INT03_2	E	H
		-		MADATA07_0 (100pin only)		
-	-	14	-	MADATA12_0 (120pin only)		
10	E2	15	88	P31 BIN0_0 TIOB1_1 SCK6_1 (SCL6_1) INT04_2	E	H
		-		MADATA08_0 (100pin only)		
-	-	15	-	MADATA13_0 (120pin only)		
11	E3	16	89	P32 ZIN0_0 TIOB2_1 SOT6_1 (SDA6_1) INT05_2	E	H
		-		MADATA09_0 (100pin only)		
-	-	16	-	MADATA14_0 (120pin only)		
12	E4	17	90	P33 INT04_0 TIOB3_1 SIN6_1 ADTG_6	E	H
		-		MADATA10_0 (100pin only)		
-	-	17	-	MADATA15_0 (120pin only)		
13	F1	18	91	P34 FRCK0_0 TIOB4_1	E	I
		-		MADATA11_0 (100pin only)		
-	-	18	-	MNALE_0 (120pin only)		

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
14	F2	19	92	P35 IC03_0 TIOB5_1 INT08_1	E	H
		-		MADATA12_0 (100pin only)		
-	-	19	-	MNCLE_0 (120pin only)		
15	F3	20	93	P36 IC02_0 SIN5_2 INT09_1	E	H
		-		MADATA13_0 (100pin only)		
-	-	20	-	MNWEX_0 (120pin only)		
16	G1	21	94	P37 IC01_0 SOT5_2 (SDA5_2) INT10_1	E	H
		-		MADATA14_0 (100pin only)		
-	-	21	-	MNREX_0 (120pin only)		
17	G2	22	95	P38 IC00_0 SCK5_2 (SCL5_2) INT11_1	E	H
		-		MADATA15_0 (100pin only)		
18	F4	23	96	P39 DTTI0X_0 ADTG_2	E	I
19	G3	24	97	P3A RTO00_0 (PPG00_0) TIOA0_1 RTCCO_2 SUBOUT_2	G	I
-	B2	-	-	VSS	-	

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
20	H1	25	98	P3B RTO01_0 (PPG00_0) TIOA1_1	G	I
21	H2	26	99	P3C RTO02_0 (PPG02_0) TIOA2_1	G	I
22	G4	27	100	P3D RTO03_0 (PPG02_0) TIOA3_1	G	I
23	H3	28	1	P3E RTO04_0 (PPG04_0) TIOA4_1	G	I
24	J2	29	2	P3F RTO05_0 (PPG04_0) TIOA5_1	G	I
25	L1	30	3	VSS	-	
26	J1	31	4	VCC	-	
27	J4	32	5	P40 TIOA0_0 RTO10_1 (PPG10_1) INT12_1	G	H
28	L5	33	6	P41 TIOA1_0 RTO11_1 (PPG10_1) INT13_1	G	H
29	K5	34	7	P42 TIOA2_0 RTO12_1 (PPG12_1)	G	I
30	J5	35	8	P43 TIOA3_0 RTO13_1 (PPG12_1) ADTG_7	G	I
-	K2	-	-	VSS	-	
-	J3	-	-	VSS	-	
-	H4	-	-	VSS	-	

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
31	H5	36	9	P44 TIOA4_0 RTO14_1 (PPG14_1) MAD00_0	G	I
32	L6	37	10	P45 TIOA5_0 RTO15_1 (PPG14_1) MAD01_0	G	I
33	L2	38	11	C	-	
34	L4	39	12	VSS	-	
35	K1	40	13	VCC	-	
36	L3	41	14	P46 X0A	D	M
37	K3	42	15	P47 X1A	D	N
38	K4	43	16	INITX	B	C
39	K6	44	17	P48 DTTI1X_1 INT14_1 SIN3_2 MAD02_0	E	H
40	J6	45	18	P49 TIOB0_0 IC10_1 AIN0_1 SOT3_2 (SDA3_2) MAD03_0	E	I
41	L7	46	19	P4A TIOB1_0 IC11_1 BIN0_1 SCK3_2 (SCL3_2) MAD04_0	E	I
42	K7	47	20	P4B TIOB2_0 IC12_1 ZIN0_1 MAD05_0	E	I

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
43	H6	48	21	P4C TIOB3_0 IC13_1 SCK7_1 (SCL7_1) AIN1_2 MAD06_0	I*	I
44	J7	49	22	P4D TIOB4_0 FRCK1_1 SOT7_1 (SDA7_1) BIN1_2 MAD07_0	I*	I
45	K8	50	23	P4E TIOB5_0 INT06_2 SIN7_1 ZIN1_2 MAD08_0	I*	H
-	-	51	-	P70 TIOA4_2	E	I
-	-	52	-	P71 INT13_2 TIOB4_2	E	H
-	-	53	-	P72 SIN2_0 INT14_2 TIOA6_0	E	H
-	-	54	-	P73 SOT2_0 (SDA2_0) INT15_2 TIOB6_0	E	H
-	-	55	-	P74 SCK2_0 (SCL2_0)	E	I
46	K9	56	24	PE0 MD1	C	P
47	L8	57	25	MD0	J	D

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
48	L9	58	26	PE2	A	A
				X0		
49	L10	59	27	PE3	A	B
				X1		
50	L11	60	28	VSS	-	
51	K11	61	29	VCC	-	
52	J11	62	30	P10	F	K
				AN00		
53	J10	63	31	P11	F	L
				AN01		
				SIN1_1		
				INT02_1		
				FRCK0_2		
				MAD09_0		
-	K10	-	-	VSS	-	
-	J9	-	-	VSS	-	
54	J8	64	32	P12	F	K
				AN02		
				SOT1_1 (SDA1_1)		
				IC00_2		
				MAD10_0		
55	H10	65	33	P13	F	K
				AN03		
				SCK1_1 (SCL1_1)		
				RTCCO_1		
				SUBOUT_1		
				IC01_2		
				MAD11_0		

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
56	H9	66	34	P14 AN04 SIN0_1 INT03_1 IC02_2 MAD12_0	F	L
57	H7	67	35	P15 AN05 SOT0_1 (SDA0_1) IC03_2 MAD13_0	F	K
58	G10	68	36	P16 AN06 SCK0_1 (SCL0_1) MAD14_0	F	K
59	G9	69	37	P17 AN07 SIN2_2 INT04_1 MAD15_0	F	L
60	H11	70	38	AVCC	-	
61	F11	71	39	AVRH	-	
62	G11	72	40	AVSS	-	
63	G8	73	41	P18 AN08 SOT2_2 (SDA2_2) MAD16_0	F	K
64	F10	74	42	P19 AN09 SCK2_2 (SCL2_2) MAD17_0	F	K
65	F9	75	43	P1A AN10 SIN4_1 INT05_1 IC00_1 MAD18_0	F	L
-	H8	-	-	VSS	-	

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
66	E11	76	44	P1B AN11 SOT4_1 (SDA4_1) IC01_1 MAD19_0	F	K
67	E10	77	45	P1C AN12 SCK4_1 (SCL4_1) IC02_1 MAD20_0	F	K
68	F8	78	46	P1D AN13 CTS4_1 IC03_1 MAD21_0	F	K
69	E9	79	47	P1E AN14 RTS4_1 DTTI0X_1 MAD22_0	F	K
70	D11	80	48	P1F AN15 ADTG_5 FRCK0_1 MAD23_0	F	K
-	-	81	-	P28 TIOB6_2 ADTG_4 RTO05_1 (PPG04_1)	E	I
-	-	82	-	P27 TIOA6_2 INT02_2 RTO04_1 (PPG04_1)	E	H
-	-	83	-	P26 SCK2_1 (SCL2_1) RTO03_1 (PPG02_1)	E	I

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
-	-	84	-	P25 SOT2_1 (SDA2_1) RTO02_1 (PPG02_1)	E	I
-	B10	-	-	VSS	-	
-	C9	-	-	VSS	-	
-	-	85	-	P24 SIN2_1 INT01_2 RTO01_1 (PPG00_1)	E	H
71	D10	86	49	P23 SCK0_0 (SCL0_0) TIOA7_1	E	I
-	-		-	RTO00_1 (PPG00_1)		
72	E8	87	50	P22 SOT0_0 (SDA0_0) TIOB7_1 ZIN1_1	E	I
73	C11	88	51	P21 SIN0_0 INT06_1 BIN1_1	E	H
74	C10	89	52	P20 INT05_0 CROUT_0 AIN1_1 MAD24_0	E	H
75	A11	90	53	VSS	-	
76	A10	91	54	VCC	-	
77	A9	92	55	P00 TRSTX MCSX7_0	E	E
78	B9	93	56	P01 TCK SWCLK	E	E

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
79	B11	94	57	P02 TDI MCSX6_0	E	E
80	A8	95	58	P03 TMS SWDIO	E	E
81	B8	96	59	P04 TDO SWO	E	E
82	C8	97	60	P05 TRACED0 TIOA5_2 SIN4_2 INT00_1 MCSX5_0	E	F
-	D8	-	-	VSS	-	
83	D9	98	61	P06 TRACED1 TIOB5_2 SOT4_2 (SDA4_2) INT01_1 AIN2_1 MCSX4_0	E	F
84	A7	99	62	P07 TRACED2 ADTG_0 SCK4_2 (SCL4_2) BIN2_1 MCLKOUT_0	E	G
85	B7	100	63	P08 TRACED3 TIOA0_2 CTS4_2 ZIN2_1 MCSX3_0	E	G
86	C7	101	64	P09 TRACECLK TIOB0_2 RTS4_2 RTO20_1 (PPG20_1) MCSX2_0	E	G

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
87	D7	102	65	P0A SIN4_0 INT00_2 FRCK1_0 FRCK2_0 RTO21_1 (PPG20_1) MCSX1_0	I*	H
88	A6	103	66	P0B SOT4_0 (SDA4_0) TIOB6_1 IC10_0 IC20_0 RTO22_1 (PPG22_1) MCSX0_0	I*	I
89	B6	104	67	P0C SCK4_0 (SCL4_0) TIOA6_1 IC11_0 IC21_0 RTO23_1 MALE_0	I*	I
90	C6	105	68	P0D RTS4_0 TIOA3_2 IC12_0 IC22_0 RTO24_1 (PPG24_1) MDQM0_0	E	I
91	A5	106	69	P0E CTS4_0 TIOB3_2 IC13_0 IC23_0 RTO25_1 (PPG24_1) MDQM1_0	E	I
-	D4	-	-	VSS	-	
-	C3	-	-	VSS	-	

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
92	B5	107	70	P0F NMIX CROUT_1 RTCCO_0 SUBOUT_0 DTTI2X_0 DTTI2X_1	E	J
-	-	108	-	P68 SCK3_0 (SCL3_0) TIOB7_2 INT12_2 IC20_1 RTO25_0 (PPG24_0)	G	H
-	-	109	-	P67 SOT3_0 (SDA3_0) TIOA7_2 IC21_1 RTO24_0 (PPG24_0)	G	I
-	-	110	-	P66 SIN3_0 ADTG_8 INT11_2 IC22_1 RTO23_0 (PPG22_0)	G	H
-	-	111	-	P65 TIOB7_0 SCK5_1 (SCL5_1) IC23_1 RTO22_0 (PPG22_0)	G	I
-	-	112	-	P64 TIOA7_0 SOT5_1 (SDA5_1) INT10_2 FRCK2_1 RTO21_0 (PPG20_0)	G	H

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
93	D6	113	71	P63 INT03_0 SIN5_1 MWEX_0	G	H
-	-		-	RTO20_0 (PPG20_0)		
94	C5	114	72	P62 SCK5_0 (SCL5_0) ADTG_3 MOEX_0	E	I
95	B4	115	73	P61 SOT5_0 (SDA5_0) TIOB2_2	E	I
96	C4	116	74	P60 SIN5_0 TIOA2_2 INT15_1 MRDY_0	I*	H
97	A4	117	75	VCC	-	
98	A3	118	76	P80	H	O
99	A2	119	77	P81	H	O
100	A1	120	78	VSS	-	

*: 5 V tolerant I/O

List of pin functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.
Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No			
			LQFP-100	FBGA-112	LQFP-120	QFP-100
ADC	ADTG_0	A/D converter external trigger input pin	84	A7	99	62
	ADTG_1		7	D3	7	85
	ADTG_2		18	F4	23	96
	ADTG_3		94	C5	114	72
	ADTG_4		-	-	81	-
	ADTG_5		70	D11	80	48
	ADTG_6		12	E4	17	90
	ADTG_7		30	J5	35	8
	ADTG_8		-	-	110	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	52	J11	62	30
	AN01		53	J10	63	31
	AN02		54	J8	64	32
	AN03		55	H10	65	33
	AN04		56	H9	66	34
	AN05		57	H7	67	35
	AN06		58	G10	68	36
	AN07		59	G9	69	37
	AN08		63	G8	73	41
	AN09		64	F10	74	42
	AN10		65	F9	75	43
	AN11		66	E11	76	44
	AN12		67	E10	77	45
	AN13		68	F8	78	46
	AN14		69	E9	79	47
	AN15		70	D11	80	48
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	27	J4	32	5
	TIOA0_1		19	G3	24	97
	TIOA0_2		85	B7	100	63
	TIOB0_0	Base timer ch.0 TIOB pin	40	J6	45	18
	TIOB0_1		9	E1	14	87
	TIOB0_2		86	C7	101	64
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	28	L5	33	6
	TIOA1_1		20	H1	25	98
	TIOA1_2		5	D1	5	83
	TIOB1_0	Base timer ch.1 TIOB pin	41	L7	46	19
	TIOB1_1		10	E2	15	88
	TIOB1_2		6	D2	6	84
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	29	K5	34	7
	TIOA2_1		21	H2	26	99
	TIOA2_2		96	C4	116	74
	TIOB2_0	Base timer ch.2 TIOB pin	42	K7	47	20
	TIOB2_1		11	E3	16	89
	TIOB2_2		95	B4	115	73

Module	Pin name	Function	Pin No			
			LQFP-100	FBGA-112	LQFP-120	QFP-100
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	30	J5	35	8
	TIOA3_1		22	G4	27	100
	TIOA3_2		90	C6	105	68
	TIOB3_0	Base timer ch.3 TIOB pin	43	H6	48	21
	TIOB3_1		12	E4	17	90
	TIOB3_2		91	A5	106	69
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	31	H5	36	9
	TIOA4_1		23	H3	28	1
	TIOA4_2		-	-	51	-
	TIOB4_0	Base timer ch.4 TIOB pin	44	J7	49	22
	TIOB4_1		13	F1	18	91
	TIOB4_2		-	-	52	-
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	32	L6	37	10
	TIOA5_1		24	J2	29	2
	TIOA5_2		82	C8	97	60
	TIOB5_0	Base timer ch.5 TIOB pin	45	K8	50	23
	TIOB5_1		14	F2	19	92
	TIOB5_2		83	D9	98	61
Base Timer 6	TIOA6_0	Base timer ch.6 TIOA pin	-	-	53	-
	TIOA6_1		89	B6	104	67
	TIOA6_2		-	-	82	-
	TIOB6_0	Base timer ch.6 TIOB pin	-	-	54	-
	TIOB6_1		88	A6	103	66
	TIOB6_2		-	-	81	-
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin	-	-	112	-
	TIOA7_1		71	D10	86	49
	TIOA7_2		-	-	109	-
	TIOB7_0	Base timer ch.7 TIOB pin	-	-	111	-
	TIOB7_1		72	E8	87	50
	TIOB7_2		-	-	108	-

Module	Pin name	Function	Pin No			
			LQFP-100	FBGA-112	LQFP-120	QFP-100
Debugger	SWCLK	Serial wire debug interface clock input pin	78	B9	93	56
	SWDIO	Serial wire debug interface data input / output pin	80	A8	95	58
	SWO	Serial wire viewer output pin	81	B8	96	59
	TCK	JTAG test clock input pin	78	B9	93	56
	TDI	JTAG test data input pin	79	B11	94	57
	TDO	JTAG debug data output pin	81	B8	96	59
	TMS	JTAG test mode state input/output pin	80	A8	95	58
	TRACECLK	Trace CLK output pin of ETM	86	C7	101	64
	TRACED0	Trace data output pin of ETM	82	C8	97	60
	TRACED1		83	D9	98	61
	TRACED2		84	A7	99	62
	TRACED3		85	B7	100	63
	TRSTX	JTAG test reset input pin	77	A9	92	55
External Bus	MAD00_0	External bus interface address bus	31	H5	36	9
	MAD01_0		32	L6	37	10
	MAD02_0		39	K6	44	17
	MAD03_0		40	J6	45	18
	MAD04_0		41	L7	46	19
	MAD05_0		42	K7	47	20
	MAD06_0		43	H6	48	21
	MAD07_0		44	J7	49	22
	MAD08_0		45	K8	50	23
	MAD09_0		53	J10	63	31
	MAD10_0		54	J8	64	32
	MAD11_0		55	H10	65	33
	MAD12_0		56	H9	66	34
	MAD13_0		57	H7	67	35
	MAD14_0		58	G10	68	36
	MAD15_0		59	G9	69	37
	MAD16_0		63	G8	73	41
	MAD17_0		64	F10	74	42
	MAD18_0		65	F9	75	43
	MAD19_0		66	E11	76	44
	MAD20_0		67	E10	77	45
	MAD21_0		68	F8	78	46
	MAD22_0		69	E9	79	47
	MAD23_0		70	D11	80	48
	MAD24_0		74	C10	89	52
	MCSX0_0	External bus interface chip select output pin	88	A6	103	66
	MCSX1_0		87	D7	102	65
	MCSX2_0		86	C7	101	64
	MCSX3_0		85	B7	100	63
	MCSX4_0		83	D9	98	61
	MCSX5_0		82	C8	97	60
	MCSX6_0		79	B11	94	57
	MCSX7_0		77	A9	92	55

Module	Pin name	Function	Pin No			
			LQFP-100	FBGA-112	LQFP-120	QFP-100
External Bus	MADATA0_0	External bus interface data bus (Address / data multiplex bus)	2	C1	2	80
	MADATA1_0		3	C2	3	81
	MADATA2_0		4	B3	4	82
	MADATA3_0		5	D1	5	83
	MADATA4_0		6	D2	6	84
	MADATA5_0		7	D3	7	85
	MADATA6_0		8	D5	8	86
	MADATA7_0		9	E1	9	87
	MADATA8_0		10	E2	10	88
	MADATA9_0		11	E3	11	89
	MADATA10_0		12	E4	12	90
	MADATA11_0		13	F1	13	91
	MADATA12_0		14	F2	14	92
	MADATA13_0		15	F3	15	93
	MADATA14_0		16	G1	16	94
	MADATA15_0		17	G2	17	95
	MDQM0_0	External bus interface byte mask signal output pin	90	C6	105	68
	MDQM1_0		91	A5	106	69
	MALE_0	External bus interface Address Latch enable output signal for multiplex	89	B6	104	67
	MRDY_0	External bus interface external RDY input signal	96	C4	116	74
	MCLKOUT_0	External bus interface external clock output pin	84	A7	99	62
	MNALE_0	External bus interface ALE signal to control NAND Flash output pin	-	-	18	-
	MNCLE_0	External bus interface CLE signal to control NAND Flash output pin	-	-	19	-
	MNREX_0	External bus interface read enable signal to control NAND Flash	-	-	21	-
	MNWEX_0	External bus interface write enable signal to control NAND Flash	-	-	20	-
	MOEX_0	External bus interface read enable signal for SRAM	94	C5	114	72
	MWEX_0	External bus interface write enable signal for SRAM	93	D6	113	71

Module	Pin name	Function	Pin No			
			LQFP-100	FBGA-112	LQFP-120	QFP-100
External Interrupt	INT00_0	External interrupt request 00 input pin	2	C1	2	80
	INT00_1		82	C8	97	60
	INT00_2		87	D7	102	65
	INT01_0	External interrupt request 01 input pin	3	C2	3	81
	INT01_1		83	D9	98	61
	INT01_2		-	-	85	-
	INT02_0	External interrupt request 02 input pin	4	B3	4	82
	INT02_1		53	J10	63	31
	INT02_2		-	-	82	-
	INT03_0	External interrupt request 03 input pin	93	D6	113	71
	INT03_1		56	H9	66	34
	INT03_2		9	E1	14	87
	INT04_0	External interrupt request 04 input pin	12	E4	17	90
	INT04_1		59	G9	69	37
	INT04_2		10	E2	15	88
	INT05_0	External interrupt request 05 input pin	74	C10	89	52
	INT05_1		65	F9	75	43
	INT05_2		11	E3	16	89
	INT06_1	External interrupt request 06 input pin	73	C11	88	51
	INT06_2		45	K8	50	23
	INT07_2	External interrupt request 07 input pin	5	D1	5	83
	INT08_1	External interrupt request 08 input pin	14	F2	19	92
	INT08_2		8	D5	8	86
	INT09_1	External interrupt request 09 input pin	15	F3	20	93
	INT09_2		-	-	11	-
	INT10_1	External interrupt request 10 input pin	16	G1	21	94
	INT10_2		-	-	112	-
	INT11_1	External interrupt request 11 input pin	17	G2	22	95
	INT11_2		-	-	110	-
	INT12_1	External interrupt request 12 input pin	27	J4	32	5
	INT12_2		-	-	108	-
	INT13_1	External interrupt request 13 input pin	28	L5	33	6
	INT13_2		-	-	52	-
	INT14_1	External interrupt request 14 input pin	39	K6	44	17
	INT14_2		-	-	53	-
	INT15_1	External interrupt request 15 input pin	96	C4	116	74
	INT15_2		-	-	54	-
	NMIX	Non-Maskable Interrupt input pin	92	B5	107	70

Module	Pin name	Function	Pin No			
			LQFP-100	FBGA-112	LQFP-120	QFP-100
GPIO	P00	General-purpose I/O port 0	77	A9	92	55
	P01		78	B9	93	56
	P02		79	B11	94	57
	P03		80	A8	95	58
	P04		81	B8	96	59
	P05		82	C8	97	60
	P06		83	D9	98	61
	P07		84	A7	99	62
	P08		85	B7	100	63
	P09		86	C7	101	64
	P0A		87	D7	102	65
	P0B		88	A6	103	66
	P0C		89	B6	104	67
	P0D		90	C6	105	68
	P0E		91	A5	106	69
	P0F		92	B5	107	70
	P10	General-purpose I/O port 1	52	J11	62	30
	P11		53	J10	63	31
	P12		54	J8	64	32
	P13		55	H10	65	33
	P14		56	H9	66	34
	P15		57	H7	67	35
	P16		58	G10	68	36
	P17		59	G9	69	37
	P18		63	G8	73	41
	P19		64	F10	74	42
	P1A		65	F9	75	43
	P1B		66	E11	76	44
	P1C		67	E10	77	45
	P1D		68	F8	78	46
	P1E		69	E9	79	47
	P1F		70	D11	80	48
	P20	General-purpose I/O port 2	74	C10	89	52
	P21		73	C11	88	51
	P22		72	E8	87	50
	P23		71	D10	86	49
	P24		-	-	85	-
	P25		-	-	84	-
	P26		-	-	83	-
	P27		-	-	82	-
	P28		-	-	81	-

Module	Pin name	Function	Pin No			
			LQFP-100	FBGA-112	LQFP-120	QFP-100
GPIO	P30	General-purpose I/O port 3	9	E1	14	87
	P31		10	E2	15	88
	P32		11	E3	16	89
	P33		12	E4	17	90
	P34		13	F1	18	91
	P35		14	F2	19	92
	P36		15	F3	20	93
	P37		16	G1	21	94
	P38		17	G2	22	95
	P39		18	F4	23	96
	P3A		19	G3	24	97
	P3B		20	H1	25	98
	P3C		21	H2	26	99
	P3D		22	G4	27	100
	P3E		23	H3	28	1
	P3F		24	J2	29	2
	P40	General-purpose I/O port 4	27	J4	32	5
	P41		28	L5	33	6
	P42		29	K5	34	7
	P43		30	J5	35	8
	P44		31	H5	36	9
	P45		32	L6	37	10
	P46		36	L3	41	14
	P47		37	K3	42	15
	P48		39	K6	44	17
	P49		40	J6	45	18
	P4A		41	L7	46	19
	P4B		42	K7	47	20
	P4C		43	H6	48	21
	P4D		44	J7	49	22
	P4E		45	K8	50	23
	P50	General-purpose I/O port 5	2	C1	2	80
	P51		3	C2	3	81
	P52		4	B3	4	82
	P53		5	D1	5	83
	P54		6	D2	6	84
	P55		7	D3	7	85
	P56		8	D5	8	86
	P57		-	-	9	-
	P58		-	-	10	-
	P59		-	-	11	-
	P5A		-	-	12	-
	P5B		-	-	13	-

Module	Pin name	Function	Pin No			
			LQFP-100	FBGA-112	LQFP-120	QFP-100
GPIO	P60	General-purpose I/O port 6	96	C4	116	74
	P61		95	B4	115	73
	P62		94	C5	114	72
	P63		93	D6	113	71
	P64		-	-	112	-
	P65		-	-	111	-
	P66		-	-	110	-
	P67		-	-	109	-
	P68		-	-	108	-
	P70	General-purpose I/O port 7	-	-	51	-
	P71		-	-	52	-
	P72		-	-	53	-
	P73		-	-	54	-
	P74		-	-	55	-
	P80	General-purpose I/O port 8	98	A3	118	76
	P81		99	A2	119	77
	PE0	General-purpose I/O port E	46	K9	56	24
	PE2		48	L9	58	26
	PE3		49	L10	59	27
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	73	C11	88	51
	SIN0_1		56	H9	66	34
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I^2C (operation mode 4).	72	E8	87	50
	SOT0_1 (SDA0_1)		57	H7	67	35
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SCL0 when it is used in an I^2C (operation mode 4).	71	D10	86	49
	SCK0_1 (SCL0_1)		58	G10	68	36
Multi-function Serial 1	SIN1_0	Multi-function serial interface ch.1 input pin	-	-	8	-
	SIN1_1		53	J10	63	31
	SOT1_0 (SDA1_0)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I^2C (operation mode 4).	-	-	9	-
	SOT1_1 (SDA1_1)		54	J8	64	32
	SCK1_0 (SCL1_0)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a CSIO (operation modes 4) and as SCL1 when it is used in an I^2C (operation mode 4).	-	-	10	-
	SCK1_1 (SCL1_1)		55	H10	65	33

Module	Pin name	Function	Pin No.			
			LQFP-100	FBGA-112	LQFP-120	QFP-100
Multi-function Serial 2	SIN2_0	Multi-function serial interface ch.2 input pin	-	-	53	-
	SIN2_1		-	-	85	-
	SIN2_2		59	G9	69	37
	SOT2_0 (SDA2_0)	Multi-function serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I^2C (operation mode 4).	-	-	54	-
	SOT2_1 (SDA2_1)		-	-	84	-
	SOT2_2 (SDA2_2)		63	G8	73	41
	SCK2_0 (SCL2_0)	Multi-function serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a CSIO (operation modes 2) and as SCL2 when it is used in an I^2C (operation mode 4).	-	-	55	-
	SCK2_1 (SCL2_1)		-	-	83	-
	SCK2_2 (SCL2_2)		64	F10	74	42
Multi-function Serial 3	SIN3_0	Multi-function serial interface ch.3 input pin	-	-	110	-
	SIN3_1		2	C1	2	80
	SIN3_2		39	K6	44	17
	SOT3_0 (SDA3_0)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I^2C (operation mode 4).	-	-	109	-
	SOT3_1 (SDA3_1)		3	C2	3	81
	SOT3_2 (SDA3_2)		40	J6	45	18
	SCK3_0 (SCL3_0)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a CSIO (operation modes 2) and as SCL3 when it is used in an I^2C (operation mode 4).	-	-	108	-
	SCK3_1 (SCL3_1)		4	B3	4	82
	SCK3_2 (SCL3_2)		41	L7	46	19

Module	Pin name	Function	Pin No			
			LQFP-100	FBGA-112	LQFP-120	QFP-100
Multi-function Serial 4	SIN4_0	Multi-function serial interface ch.4 input pin	87	D7	102	65
	SIN4_1		65	F9	75	43
	SIN4_2		82	C8	97	60
	SOT4_0 (SDA4_0)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I^2C (operation mode 4).	88	A6	103	66
	SOT4_1 (SDA4_1)		66	E11	76	44
	SOT4_2 (SDA4_2)		83	D9	98	61
	SCK4_0 (SCL4_0)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a CSIO (operation modes 2) and as SCL4 when it is used in an I^2C (operation mode 4).	89	B6	104	67
	SCK4_1 (SCL4_1)		67	E10	77	45
	SCK4_2 (SCL4_2)		84	A7	99	62
	RTS4_0	Multi-function serial interface ch.4 RTS output pin	90	C6	105	68
	RTS4_1		69	E9	79	47
	RTS4_2		86	C7	101	64
	CTS4_0	Multi-function serial interface ch.4 CTS input pin	91	A5	106	69
	CTS4_1		68	F8	78	46
	CTS4_2		85	B7	100	63
Multi-function Serial 5	SIN5_0	Multi-function serial interface ch.5 input pin	96	C4	116	74
	SIN5_1		93	D6	113	93
	SIN5_2		15	F3	20	93
	SOT5_0 (SDA5_0)	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I^2C (operation mode 4).	95	B4	115	73
	SOT5_1 (SDA5_1)		-	-	112	-
	SOT5_2 (SDA5_2)		16	G1	21	94
	SCK5_0 (SCL5_0)	Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a CSIO (operation modes 2) and as SCL5 when it is used in an I^2C (operation mode 4).	94	C5	114	72
	SCK5_1 (SCL5_1)		-	-	111	-
	SCK5_2 (SCL5_2)		17	G2	22	95

Module	Pin name	Function	Pin No			
			LQFP-100	FBGA-112	LQFP-120	QFP-100
Multi-function Serial 6	SIN6_0	Multi-function serial interface ch.6 input pin	5	D1	5	83
	SIN6_1		12	E4	17	90
	SOT6_0 (SDA6_0)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I^2C (operation mode 4).	6	D2	6	84
	SOT6_1 (SDA6_1)		11	E3	16	89
	SCK6_0 (SCL6_0)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a CSIO (operation modes 2) and as SCL6 when it is used in an I^2C (operation mode 4).	7	D3	7	85
	SCK6_1 (SCL6_1)		10	E2	15	88
Multi-function Serial 7	SIN7_0	Multi-function serial interface ch.7 input pin	-	-	11	-
	SIN7_1		45	K8	50	23
	SOT7_0 (SDA7_0)	Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I^2C (operation mode 4).	-	-	12	-
	SOT7_1 (SDA7_1)		44	J7	49	22
	SCK7_0 (SCL7_0)	Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a CSIO (operation modes 2) and as SCL7 when it is used in an I^2C (operation mode 4).	-	-	13	-
	SCK7_1 (SCL7_1)		43	H6	48	21

Module	Pin name	Function	Pin No			
			LQFP-100	FBGA-112	LQFP-120	QFP-100
Multi-function Timer 0	DTTI0X_0	Input signal controlling wave form generator outputs RTO00 to RTO05 of Multi-function timer 0.	18	F4	23	96
	DTTI0X_1		69	E9	79	47
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin	13	F1	18	91
	FRCK0_1		70	D11	80	48
	FRCK0_2		53	J10	63	31
	IC00_0	16-bit input capture ch.0 input pin of Multi-function timer 0. ICxx describes channel number.	17	G2	22	95
	IC00_1		65	F9	75	43
	IC00_2		54	J8	64	32
	IC01_0		16	G1	21	94
	IC01_1		66	E11	76	44
	IC01_2		55	H10	65	33
	IC02_0		15	F3	20	93
	IC02_1		67	E10	77	45
	IC02_2		56	H9	66	34
	IC03_0		14	F2	19	92
	IC03_1		68	F8	78	46
	IC03_2		57	H7	67	35
	RTO00_0 (PPG00_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	19	G3	24	97
	RTO00_1 (PPG00_1)		-	-	86	-
	RTO01_0 (PPG00_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	20	H1	25	98
	RTO01_1 (PPG00_1)		-	-	85	-
	RTO02_0 (PPG02_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	21	H2	26	99
	RTO02_1 (PPG02_1)		-	-	84	-
	RTO03_0 (PPG02_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	22	G4	27	100
	RTO03_1 (PPG02_1)		-	-	83	-
	RTO04_0 (PPG04_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	23	H3	28	1
	RTO04_1 (PPG04_1)		-	-	82	-
	RTO05_0 (PPG04_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	24	J2	29	2
	RTO05_1 (PPG04_1)		-	-	81	-

Module	Pin name	Function	Pin No			
			LQFP-100	FBGA-112	LQFP-120	QFP-100
Multi-function Timer 1	DTTI1X_0	Input signal controlling wave form generator outputs RTO10 to RTO15 of Multi-function timer 1.	8	D5	8	86
	DTTI1X_1		39	K6	44	17
	FRCK1_0	16-bit free-run timer ch.1 external clock input pin	87	D7	102	65
	FRCK1_1		44	J7	49	22
	IC10_0	16-bit input capture ch.1 input pin of Multi-function timer 1. ICxx describes channel number.	88	A6	103	66
	IC10_1		40	J6	45	18
	IC11_0		89	B6	104	67
	IC11_1		41	L7	46	19
	IC12_0		90	C6	105	68
	IC12_1		42	K7	47	20
	IC13_0		91	A5	106	69
	IC13_1		43	H6	48	21
	RTO10_0 (PPG10_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	2	C1	2	80
	RTO10_1 (PPG10_1)		27	J4	32	5
	RTO11_0 (PPG10_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	3	C2	3	81
	RTO11_1 (PPG10_1)		28	L5	33	6
	RTO12_0 (PPG12_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	4	B3	4	82
	RTO12_1 (PPG12_1)		29	K5	34	7
	RTO13_0 (PPG12_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	5	D1	5	83
	RTO13_1 (PPG12_1)		30	J5	35	8
	RTO14_0 (PPG14_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	6	D2	6	84
	RTO14_1 (PPG14_1)		31	H5	36	9
	RTO15_0 (PPG14_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	7	D3	7	85
	RTO15_1 (PPG14_1)		32	L6	37	10

Module	Pin name	Function	Pin No			
			LQFP-100	FBGA-112	LQFP-120	QFP-100
Multi-function Timer 2	DTTI2X_0	Input signal controlling wave form generator outputs RTO20 to RTO25 of Multi-function timer 2.	92	B5	107	70
	DTTI2X_1		92	B5	107	70
	FRCK2_0	16-bit free-run timer ch.2 external clock input pin	87	D7	102	65
	FRCK2_1		-	-	112	-
	IC20_0	16-bit input capture ch.2 input pin of Multi-function timer 2. ICxx describes channel number.	88	A6	103	66
	IC20_1		-	-	108	-
	IC21_0		89	B6	104	67
	IC21_1		-	-	109	-
	IC22_0		90	C6	105	68
	IC22_1		-	-	110	-
	IC23_0		91	A5	106	69
	IC23_1		-	-	111	-
	RTO20_0 (PPG20_0)	Wave form generator output pin of Multi-function timer 2. This pin operates as PPG20 when it is used in PPG2 output modes.	-	-	113	-
	RTO20_1 (PPG20_1)		86	C7	101	64
	RTO21_0 (PPG20_0)	Wave form generator output pin of Multi-function timer 2. This pin operates as PPG20 when it is used in PPG2 output modes.	-	-	112	-
	RTO21_1 (PPG20_1)		87	D7	102	65
	RTO22_0 (PPG22_0)	Wave form generator output pin of Multi-function timer 2. This pin operates as PPG22 when it is used in PPG2 output modes.	-	-	111	-
	RTO22_1 (PPG22_1)		88	A6	103	66
	RTO23_0 (PPG22_0)	Wave form generator output pin of Multi-function timer 2. This pin operates as PPG22 when it is used in PPG2 output modes.	-	-	110	-
	RTO23_1 (PPG22_1)		89	B6	104	67
	RTO24_0 (PPG24_0)	Wave form generator output pin of Multi-function timer 2. This pin operates as PPG24 when it is used in PPG2 output modes.	-	-	109	-
	RTO24_1 (PPG24_1)		90	C6	105	68
	RTO25_0 (PPG24_0)	Wave form generator output pin of Multi-function timer 2. This pin operates as PPG24 when it is used in PPG2 output modes.	-	-	108	-
	RTO25_1 (PPG24_1)		91	A5	106	69

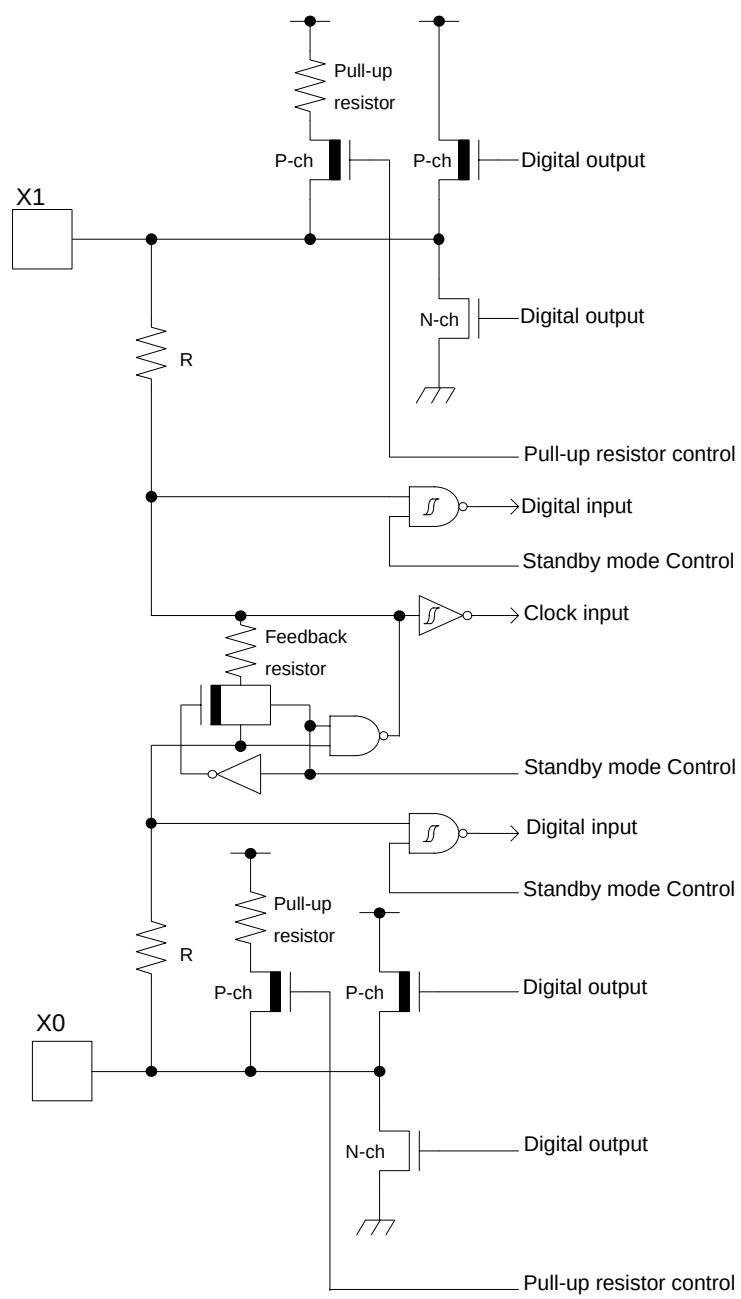
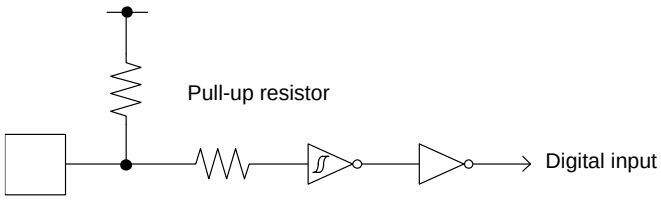
Module	Pin name	Function	Pin No			
			LQFP-100	FBGA-112	LQFP-120	QFP-100
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch.0 AIN input pin	9	E1	14	87
	AIN0_1		40	J6	45	18
	AIN0_2		2	C1	2	80
	BIN0_0	QPRC ch.0 BIN input pin	10	E2	15	88
	BIN0_1		41	L7	46	19
	BIN0_2		3	C2	3	81
	ZIN0_0	QPRC ch.0 ZIN input pin	11	E3	16	89
	ZIN0_1		42	K7	47	20
	ZIN0_2		4	B3	4	82
Quadrature Position/ Revolution Counter 1	AIN1_1	QPRC ch.1 AIN input pin	74	C10	89	52
	AIN1_2		43	H6	48	21
	BIN1_1	QPRC ch.1 BIN input pin	73	C11	88	51
	BIN1_2		44	J7	49	22
	ZIN1_1	QPRC ch.1 ZIN input pin	72	E8	87	50
	ZIN1_2		45	K8	50	23
Quadrature Position/ Revolution Counter 2	AIN2_0	QPRC ch.2 AIN input pin	-	-	10	-
	AIN2_1		83	D9	98	61
	BIN2_0	QPRC ch.2 BIN input pin	-	-	11	-
	BIN2_1		84	A7	99	62
	ZIN2_0	QPRC ch.2 ZIN input pin	-	-	12	-
	ZIN2_1		85	B7	100	63
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of Real-time clock	92	B5	107	70
	RTCCO_1		55	H10	65	33
	RTCCO_2		19	G3	24	97
	SUBOUT_0	Sub clock output pin	92	B5	107	70
	SUBOUT_1		55	H10	65	33
	SUBOUT_2		19	G3	24	97

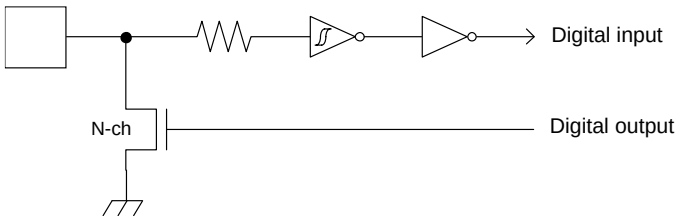
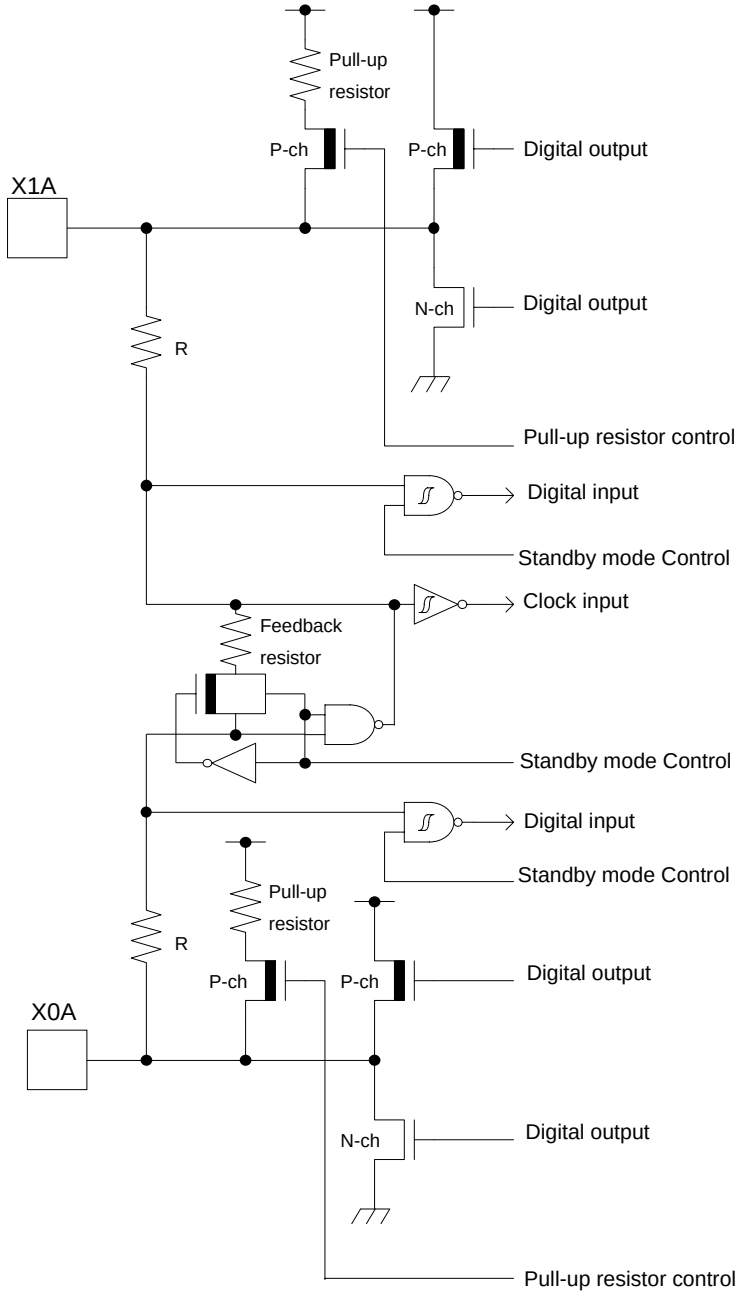
Module	Pin name	Function	Pin No			
			LQFP-100	FBGA-112	LQFP-120	QFP-100
Reset	INITX	External Reset Input pin. A reset is valid when INITX="L".	38	K4	43	16
Mode	MD0	Mode 0 pin. During normal operation, MD0="L" must be input. During serial programming to Flash memory, MD0="H" must be input.	47	L8	57	25
	MD1	Mode 1 pin. During serial programming to Flash memory, MD1="L" must be input.	46	K9	56	24
Power	VCC	Power supply Pin	1	B1	1	79
	VCC	Power supply Pin	26	J1	31	4
	VCC	Power supply Pin	35	K1	40	13
	VCC	Power supply Pin	51	K11	61	29
	VCC	Power supply Pin	76	A10	91	54
	VCC	Power supply Pin	97	A4	117	75
GND	VSS	GND Pin	-	B2	-	
	VSS	GND Pin	25	L1	30	3
	VSS	GND Pin	-	K2	-	
	VSS	GND Pin	-	J3	-	
	VSS	GND Pin	-	H4	-	
	VSS	GND Pin	34	L4	39	12
	VSS	GND Pin	50	L11	60	28
	VSS	GND Pin	-	K10	-	
	VSS	GND Pin	-	J9	-	
	VSS	GND Pin	-	H8	-	
	VSS	GND Pin	-	B10	-	
	VSS	GND Pin	-	C9	-	
	VSS	GND Pin	75	A11	90	53
	VSS	GND Pin	-	D8	-	
	VSS	GND Pin	-	D4	-	
	VSS	GND Pin	-	C3	-	
	VSS	GND Pin	100	A1	120	78
Clock	X0	Main clock (oscillation) input pin	48	L9	58	26
	X0A	Sub clock (oscillation) input pin	36	L3	41	14
	X1	Main clock (oscillation) I/O pin	49	L10	59	27
	X1A	Sub clock (oscillation) I/O pin	37	K3	42	15
	CROUT_0	Built-in high-speed CR-osc clock output port	74	C10	89	52
	CROUT_1		92	B5	107	70
Analog Power	AVCC	A/D converter analog power pin	60	H11	70	38
	AVRH	A/D converter analog reference voltage input pin	61	F11	71	39
Analog GND	AVSS	A/D converter GND pin	62	G11	72	40
C pin	C	Power stabilization capacity pin	33	L2	38	11

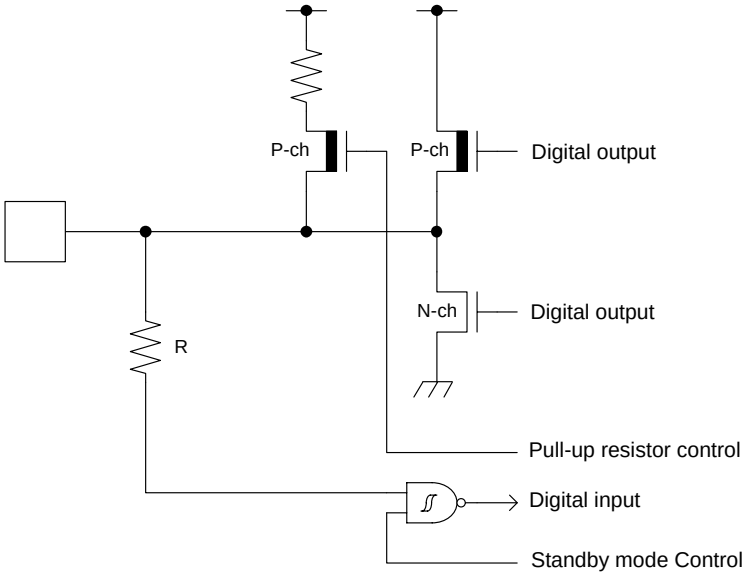
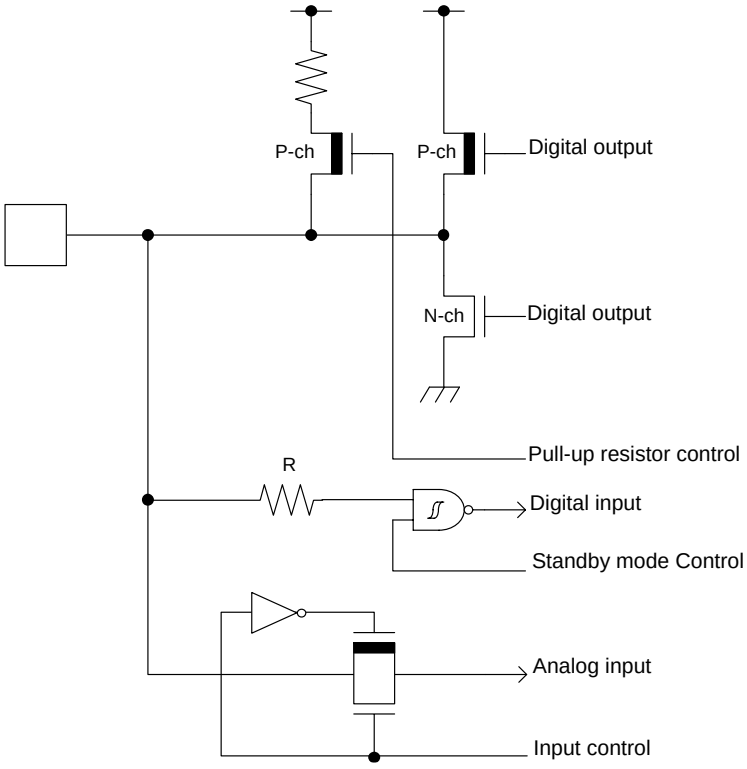
Note:

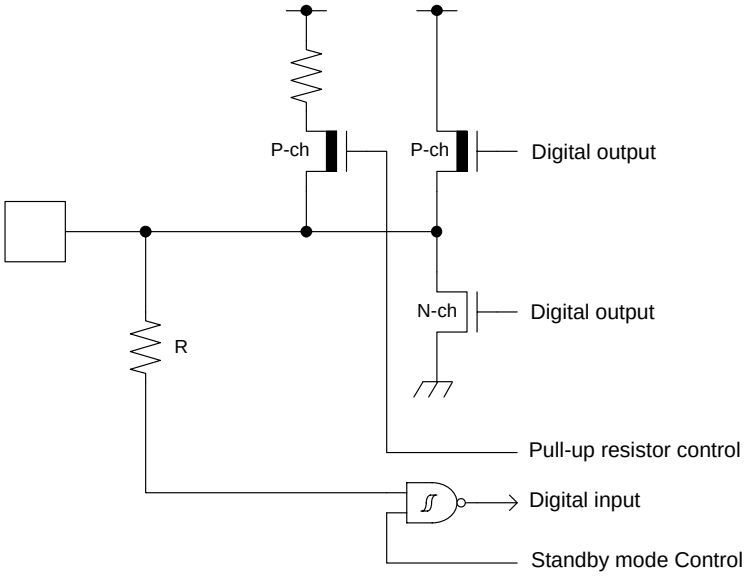
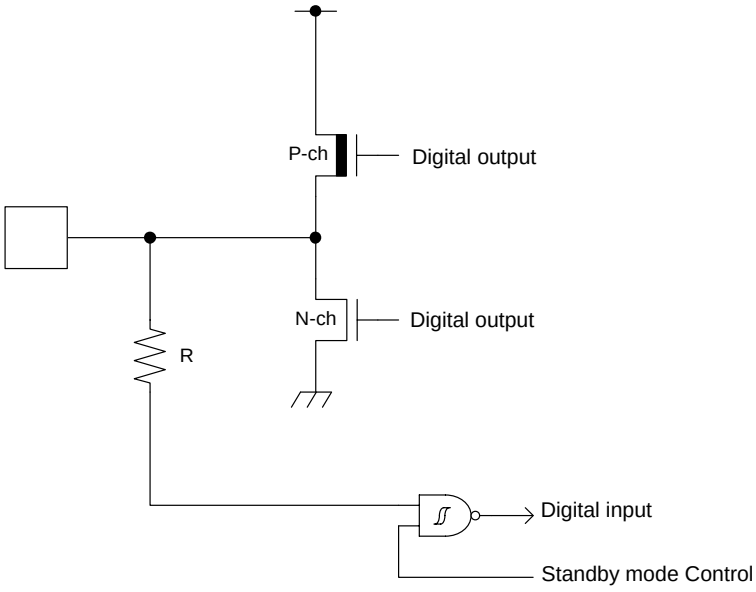
- *While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.*

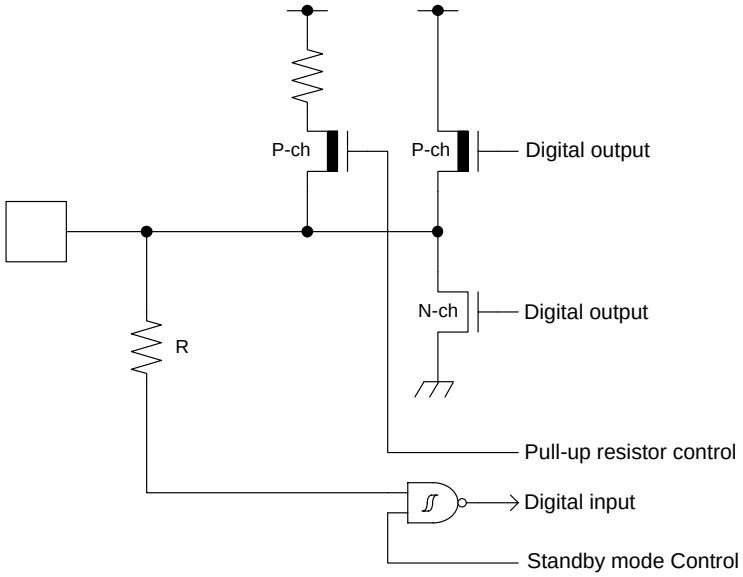
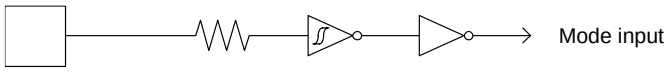
5. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. – Oscillation feedback resistor: Approximately 1 MΩ – With Standby mode control When the GPIO is selected. – CMOS level output. – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor: Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA
B		– CMOS level hysteresis input – Pull-up resistor: Approximately 50 kΩ

Type	Circuit	Remarks
C		– Open drain output – CMOS level hysteresis input
D		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. – Oscillation feedback resistor: Approximately 5 MΩ – With Standby mode control When the GPIO is selected. – CMOS level output. – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor: Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA

Type	Circuit	Remarks
E		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor: Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off – +B input is available
F		– CMOS level output – CMOS level hysteresis input – With input control – Analog input – With pull-up resistor control – With standby mode control – Pull-up resistor: Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off – +B input is available

Type	Circuit	Remarks
G		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor: Approximately 50 kΩ – I_{OH}= -12 mA, I_{OL}= 12 mA – +B input is available
H		– CMOS level output – CMOS level hysteresis input – With standby mode control – I_{OH}= -20.5 mA, I_{OL}= 18.5 mA

Type	Circuit	Remarks
I		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – 5 V tolerant – With standby mode control – I_{OH} = -4 mA, I_{OL} = 4 mA – Available to control of PZR registers. – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
J		CMOS level hysteresis input

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

   Therefore, avoid this type of connection.

3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress' recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (FBGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.

   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).

   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

7. Handling Devices

Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each POWER pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between each Power supply pin and GND pin, between AVCC pin and AVSS pin near this device.

Stabilizing power supply voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/µs when there is a momentary fluctuation on switching the power supply.

Crystal oscillator circuit

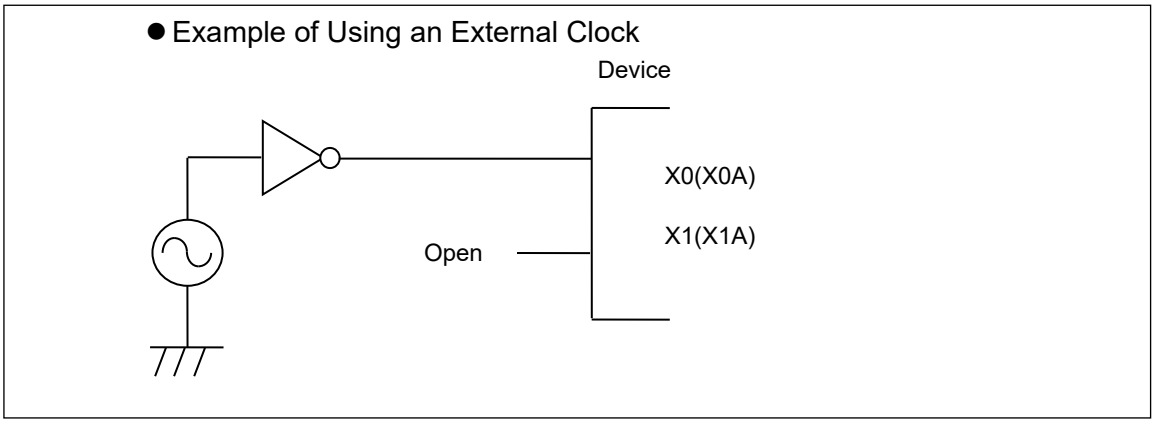
Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

Using an external clock

When using an external clock, the clock signal should be input to the X0, X0A pin only and the X1, X1A pin should be kept open.



Handling when using Multi function serial pin as I²C pin

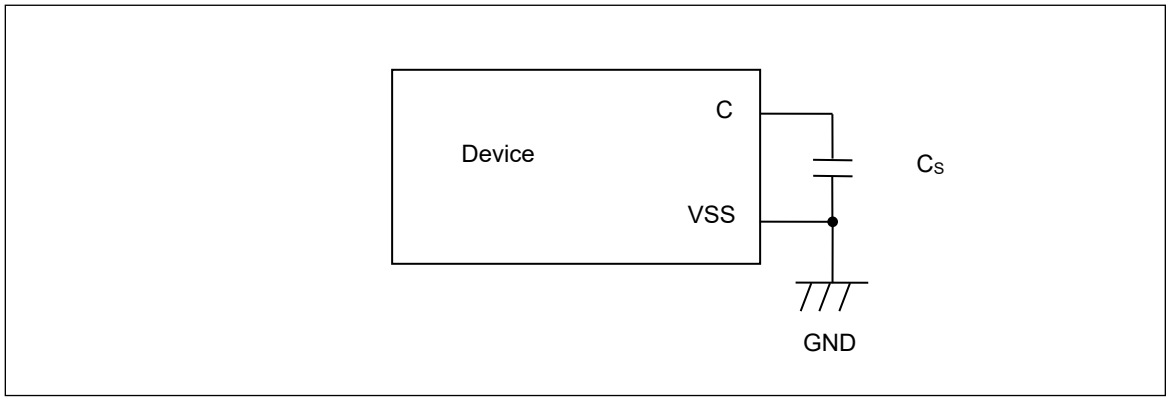
If it is using multi function serial pin as I²C pins, P-ch transistor of digital output is always disable. However, I²C pins need to keep the electrical characteristic like other pins and not to connect to external I²C bus system with power OFF.

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (CS) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.

However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.

A smoothing capacitor of about 4.7 µF would be recommended for this series.



Mode pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

Notes on power-on

Turn power on/off in the following order or at the same time.

If not using the A/D converter, connect AVCC = VCC and AVSS = VSS.

Turning on: VCC → AVCC → AVRH
Turning off: AVRH → AVCC → VCC

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

Differences in features among the products with different memory sizes and between Flash products and MASK products

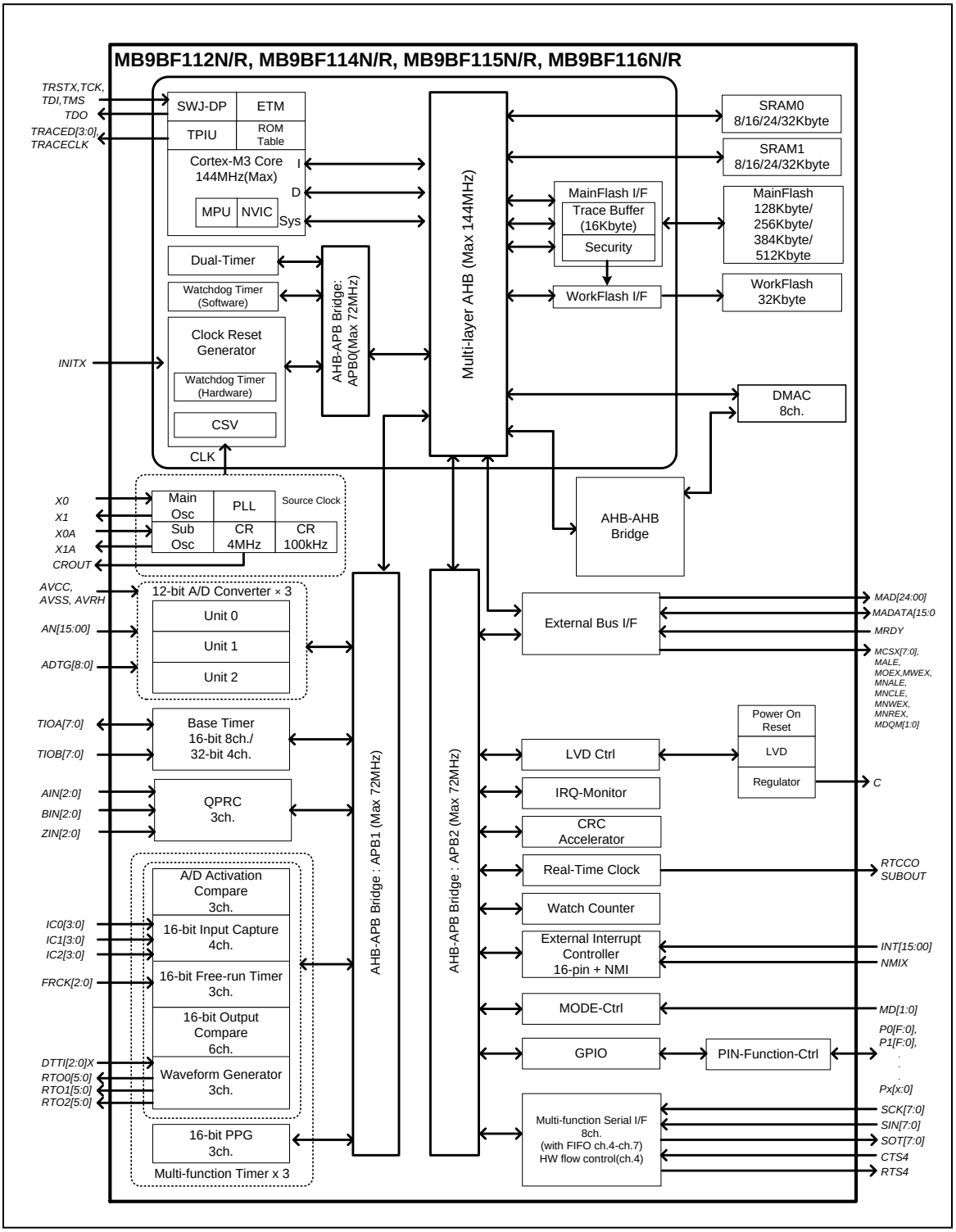
The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

Pull-Up function of 5 V tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

8. Block Diagram

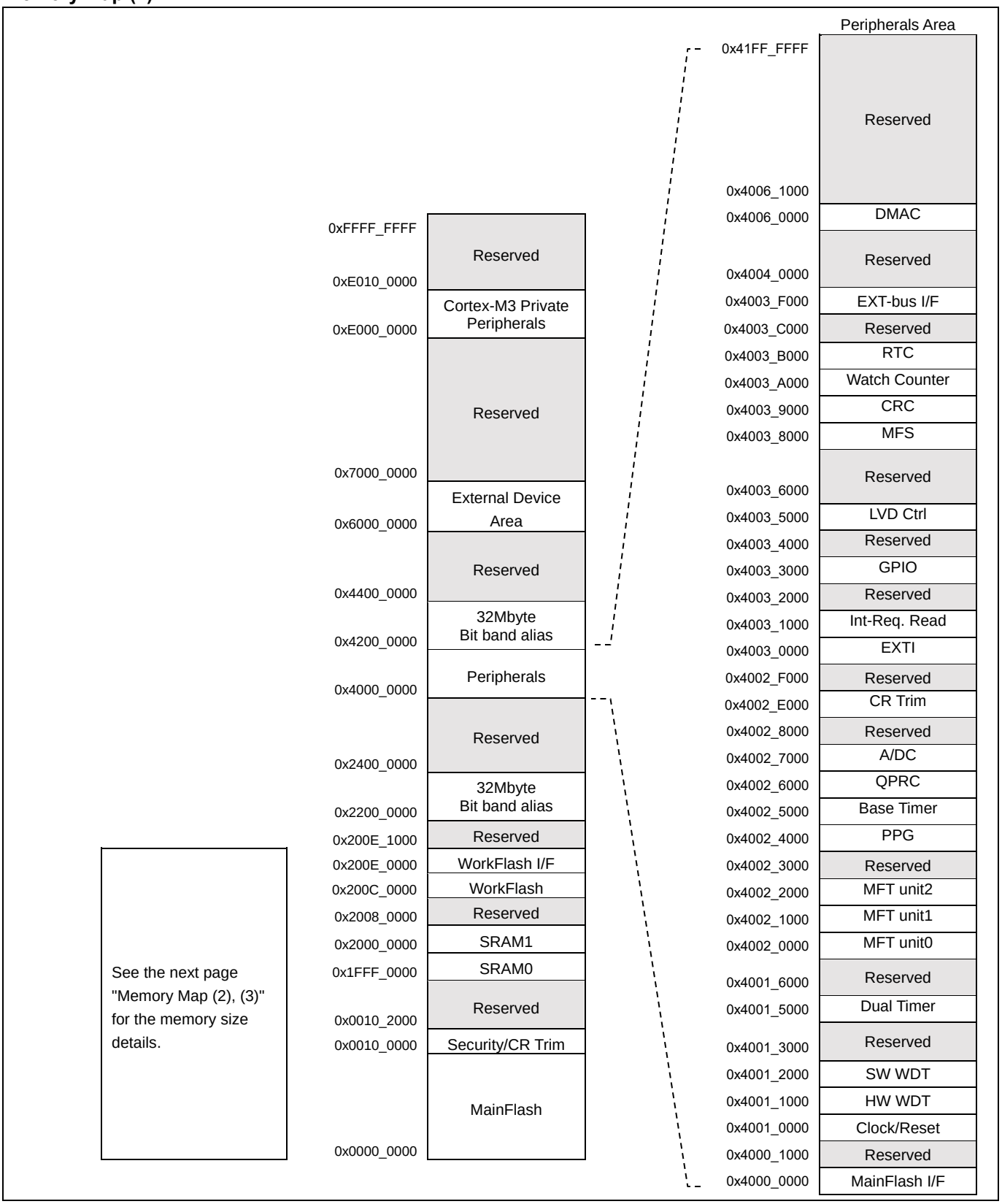


9. Memory Size

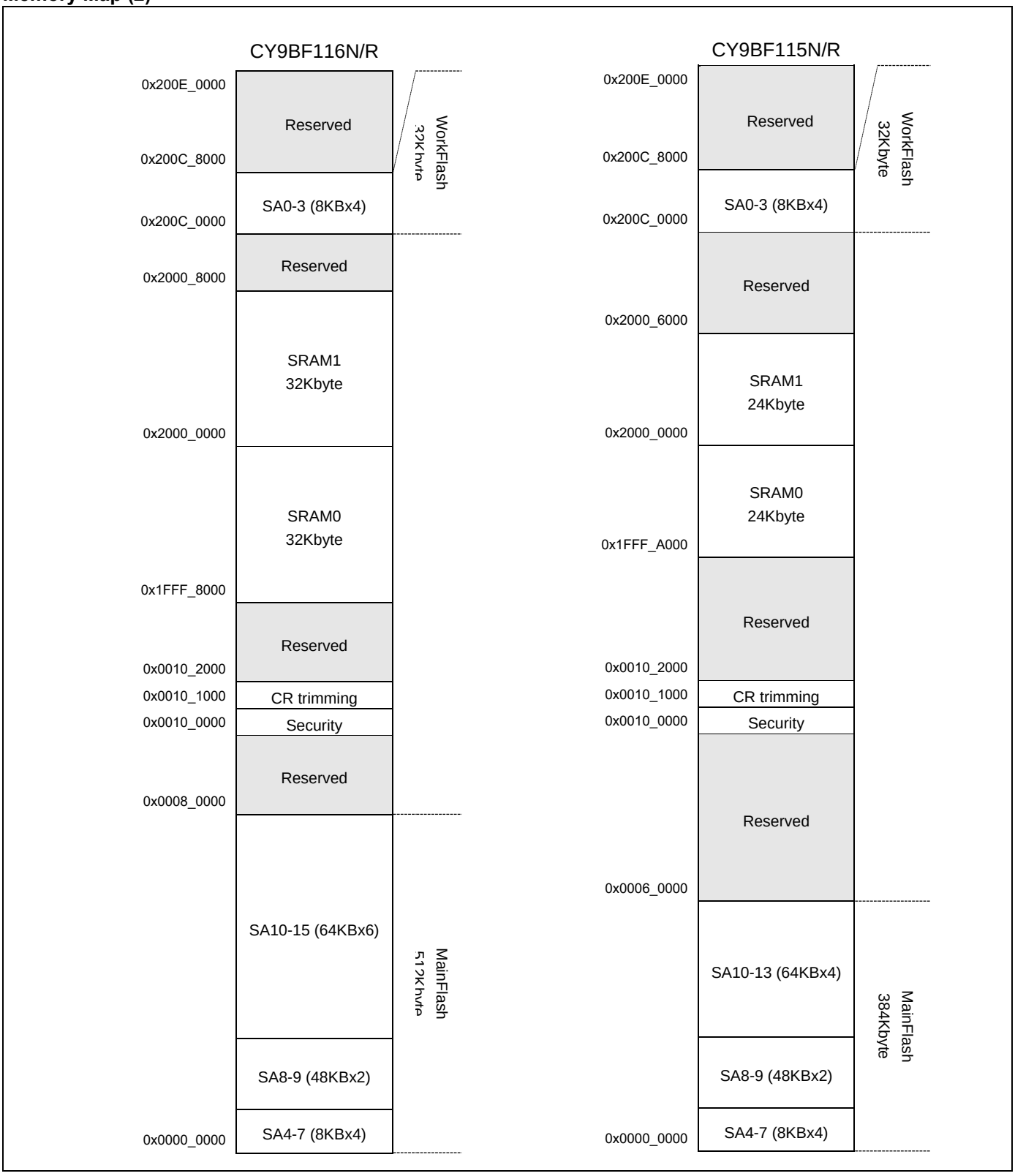
See 1. Product Lineup of "Memory size" to confirm the memory size.

10. Memory Map

Memory Map (1)

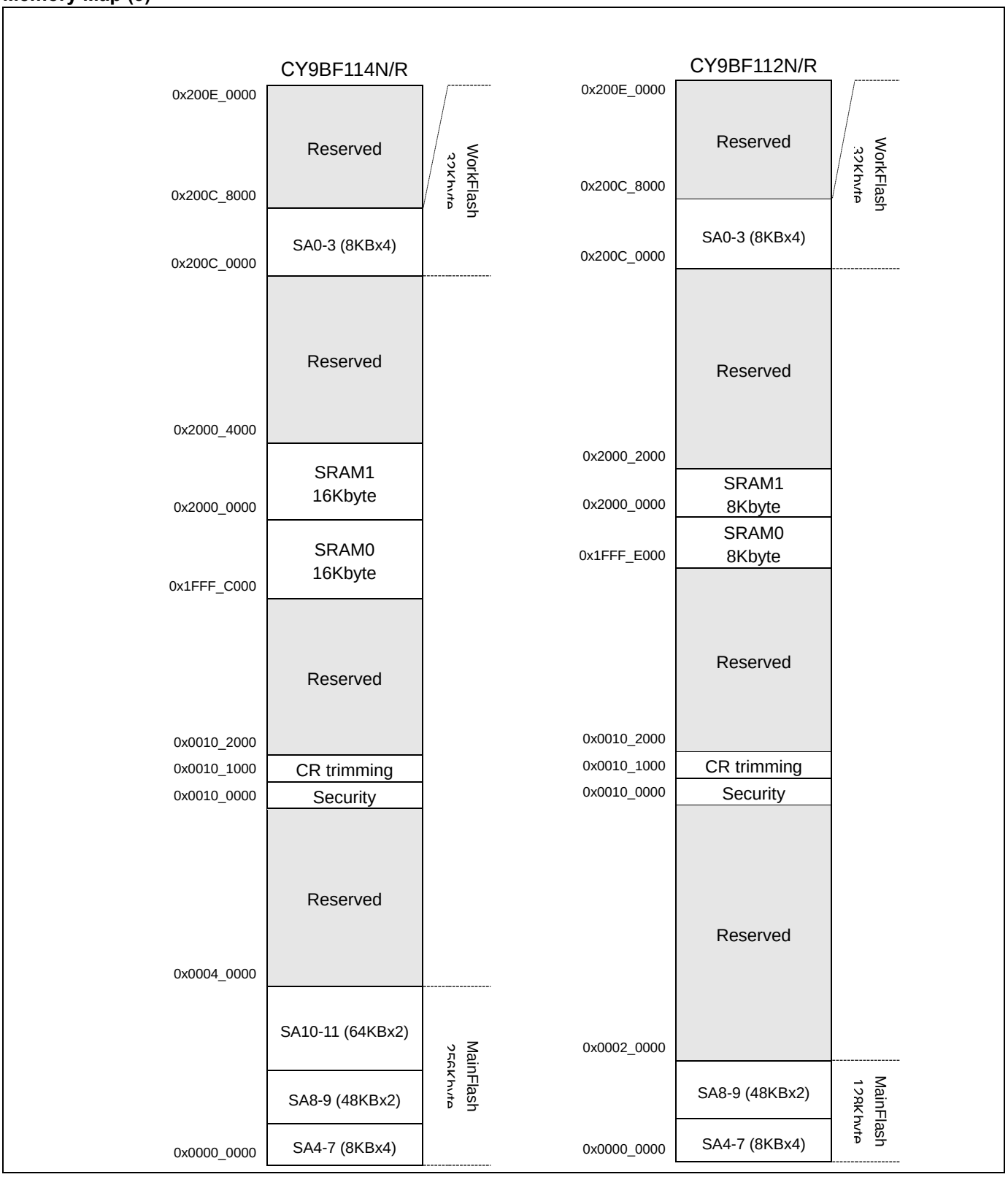


Memory Map (2)



See "CY9B510R/410R/310R/110R Series Flash programming Manual" for sector structure of Flash.

Memory Map (3)



See "CY9B510R/410R/310R/110R Series Flash programming Manual" for sector structure of Flash.

Peripheral Address Map

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	MainFlash I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function timer unit0
0x4002_1000	0x4002_1FFF		Multi-function timer unit1
0x4002_2000	0x4002_3FFF		Multi-function timer unit2
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Quadrature Position/Revolution Counter
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_5FFF		Low-Voltage Detector
0x4003_6000	0x4003_6FFF		Reserved
0x4003_7000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function serial Interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_BFFF		Real-time clock
0x4003_C000	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External Memory interface
0x4004_0000	0x4005_FFFF	AHB	Reserved
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x41FF_FFFF		Reserved
0x200E_0000	0x200E_FFFF		WorkFlash I/F register

11. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

■ INITX = 0

This is the period when the INITX pin is the "L" level.

■ INITX = 1

This is the period when the INITX pin is the "H" level.

■ SPL = 0

This is the status that standby pin level setting bit (SPL) in standby mode control register (STB_CTL) is set to "0".

■ SPL = 1

This is the status that standby pin level setting bit (SPL) in standby mode control register (STB_CTL) is set to "1".

■ Input enabled

Indicates that the input function can be used.

■ Internal input fixed at "0"

This is the status that the input function cannot be used. Internal input is fixed at "L".

■ Hi-Z

Indicates that the output drive transistor is disabled and the pin is put in the Hi-Z state.

■ Setting disabled

Indicates that the setting is disabled.

■ Maintain previous state

Maintains the state that was immediately prior to entering the current mode.

If a built-in peripheral function is operating, the output follows the peripheral function.

If the pin is being used as a port, that output is maintained.

■ Analog input is enabled

Indicates that the analog input is enabled.

■ Trace output

Indicates that the trace function can be used.

List of Pin Status

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or sleep mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Main crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Main crystal oscillator output pin	Hi-Z/ Internal input fixed at "0"/ or Input enable	Hi-Z/ Internal input fixed at "0"	Hi-Z/ Internal input fixed at "0"	Maintain previous state	Maintain previous state/ Hi-Z at oscillation stop*1/ Internal input fixed at "0"	Maintain previous state/ Hi-Z at oscillation stop*1/ Internal input fixed at "0"
C	INITX input pin	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	JTAG selected	Hi-Z	Pull-up/ Input enabled	Pull-up/ Input enabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z/ Internal input fixed at "0"
F	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output
	External interrupt enabled selected						Maintain previous state
	GPIO selected, or other than above resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or sleep mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
G	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output
	GPIO selected, or other than above resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
H	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected, or other than above resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
I	GPIO selected, resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
J	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected, or other than above resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or sleep mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
K	Analog input selected	Hi-Z	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled
	GPIO selected, or other than above resource selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
L	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Analog input selected	Hi-Z	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled
	GPIO selected, or other than above resource selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
M	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Sub crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or sleep mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
N	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Sub crystal oscillator output pin	Hi-Z/ Internal input fixed at "0"/ or Input enable	Hi-Z/ Internal input fixed at "0"	Hi-Z/ Internal input fixed at "0"	Maintain previous state	Maintain previous state/ Hi-Z at oscillation stop*2/ Internal input fixed at "0"	Maintain previous state/ Hi-Z at oscillation stop*2/ Internal input fixed at "0"
O	GPIO selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
P	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Input enabled

*1: Oscillation is stopped at Sub Timer mode, Low-speed CR Timer mode, and Stop mode.

*2: Oscillation is stopped at Stop mode.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage*1, *3	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage*1, *3	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage*1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5 V tolerant
Analog pin input voltage*1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5 V)	V	
Output voltage*1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
Clamp maximum current	I_{CLAMP}	-2	+2	mA	*7
Clamp total maximum current	$\Sigma [I_{CLAMP}]$		+20	mA	*7
L level maximum output current*4	I_{OL}	-	10	mA	4 mA type
			20	mA	12 mA type
			39	mA	P80, P81
L level average output current*6	I_{OLAV}	-	4	mA	4 mA type
			12	mA	12 mA type
			18.5	mA	P80, P81
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total average output current*6	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current*4	I_{OH}	-	- 10	mA	4 mA type
			- 20	mA	12 mA type
			- 39	mA	P80, P81
H level average output current*5	I_{OHAV}	-	- 4	mA	4 mA type
			- 12	mA	12 mA type
			- 20.5	mA	P80, P81
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current*6	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	1000	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0.0$ V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: Ensure that the voltage does not exceed V_{CC} + 0.5 V, for example, when the power is turned on.

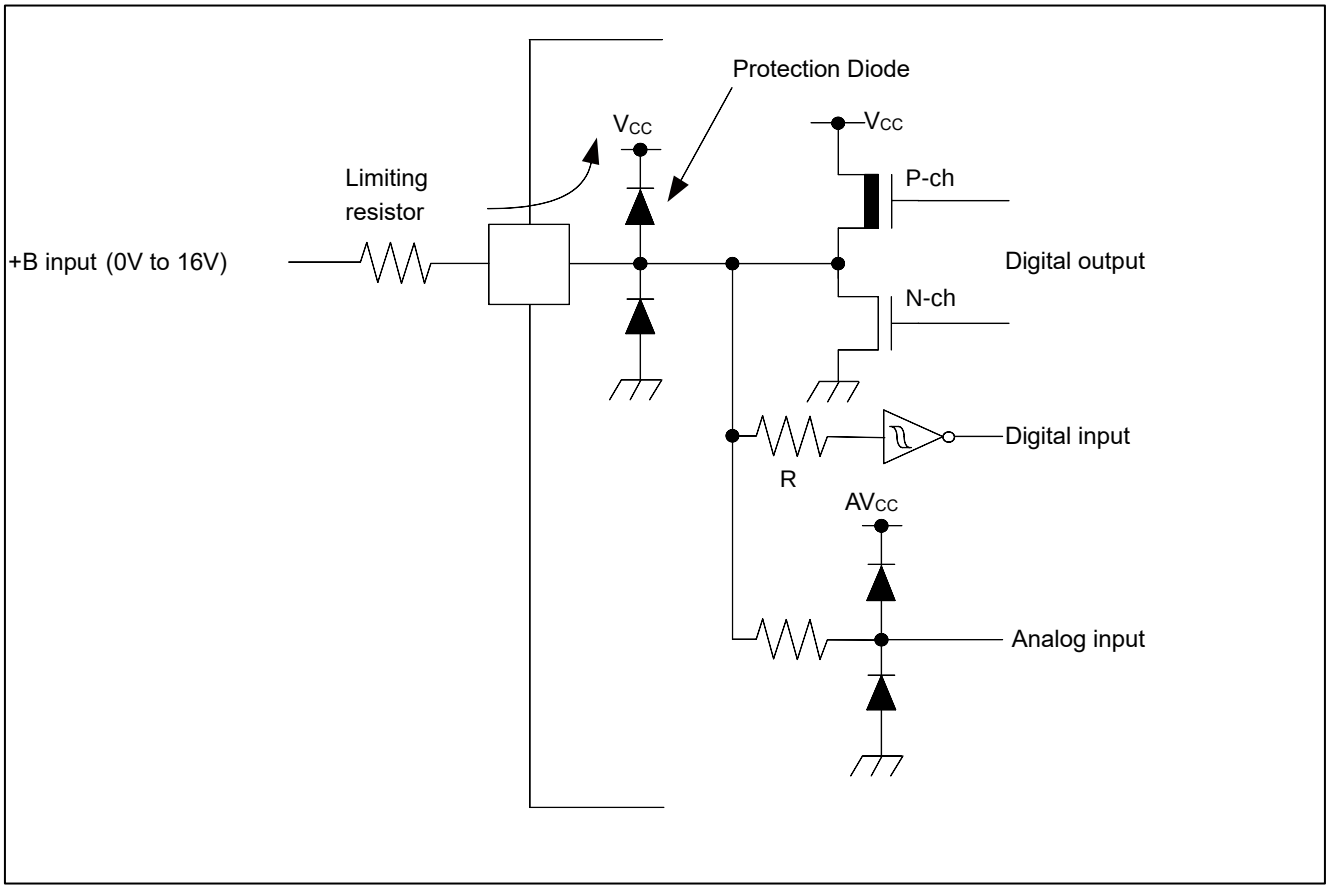
*4: The maximum output current is the peak value for a single pin.

*5: The average output is the average current for a single pin over a period of 100 ms.

*6: The total average output current is the average current for all pins over a period of 100 ms.

*7:

- See "4 List of Pin Functions" and "5 I/O Circuit Type" about +B input available pin.
- Use within recommended operating conditions.
- Use at DC voltage (current) the +B input.
- The +B signal should always be applied a limiting resistance placed between the +B signal and the device.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the device pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the device drive current is low, such as in the low-power consumption modes, the +B input potential may pass through the protective diode and increase the potential at the VCC and AVCC pin, and this may affect other devices.
- Note that if a +B signal is input when the device power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- The following is a recommended circuit example (I/O equivalent circuit).



WARNING:

- *Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.*

12.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0V)

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply voltage		V_{CC}	-	2.7*2	5.5	V	
Analog power supply voltage		AV_{CC}	-	2.7	5.5	V	AV_{CC} = V_{CC}
Analog reference voltage		AVRH	-	2.7	AV_{CC}	V	
Smoothing capacitor		C_S	-	1	10	µF	For built-in 1.2 V regulator*1
Operating temperature	LQI100 LQM120	T_A	When mounted on four-layer PCB	- 40	+ 85	°C	
	PQH100 LBC112	T_A	-	- 40	+ 85	°C	

*1: See "C Pin" in "7 Handling Devices" for the connection of the smoothing capacitor.

*2: In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR(including Main PLL is used) or built-in Low-speed CR is possible to operate only.

WARNING:

- *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
- *Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.*

12.3 DC Characteristics

12.3.1 Current Rating

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ*3	Max*4		
Run mode current	I_{CC}	VCC	PLL Run mode	CPU: 144 MHz, Peripheral: 72 MHz, Main Flash 2 Wait TraceBuffer: ON FRWTR.RWT = 10 FSYNDN.SD = 000 FBFCR.BE = 1	85	117	mA	*1, *5
				CPU: 72 MHz, Peripheral: 72 MHz, Main Flash 0 Wait TraceBuffer: OFF FRWTR.RWT = 00 FSYNDN.SD = 000 FBFCR.BE = 0	52	70	mA	*1, *5
			High-speed CR Run mode	CPU/ Peripheral: 4 MHz*2 Main Flash 0 Wait FRWTR.RWT = 00 FSYNDN.SD = 000	5	17	mA	*1
			Sub Run mode	CPU/ Peripheral: 32 kHz Main Flash 0 Wait FRWTR.RWT = 00 FSYNDN.SD = 000	1.3	14	mA	*1, *6
			Low-speed CR Run mode	CPU/ Peripheral: 100 kHz Main Flash 0 Wait FRWTR.RWT = 00 FSYNDN.SD = 000	1.3	14	mA	*1
Sleep mode current	I_{CCS}		PLL Sleep mode	Peripheral: 72 MHz	28	43	mA	*1, *5
			High-speed CR Sleep mode	Peripheral: 4 MHz*2	3	16	mA	*1
			Sub Sleep mode	Peripheral: 32 kHz	1	14	mA	*1, *6
			Low-speed CR Sleep mode	Peripheral: 100 kHz	1	14	mA	*1

*1: When all ports are fixed.

*2: When setting it to 4 MHz by trimming.

*3: T_A=+25°C, V_{CC}=5.5 V

*4: T_A=+85°C, V_{CC}=5.5 V

*5: When using the crystal oscillator of 4 MHz(Including the current consumption of the oscillation circuit)

*6: When using the crystal oscillator of 32 kHz(Including the current consumption of the oscillation circuit)

Parameter	Symbol	Pin name	Conditions		Value Typ*2	Value Max*2	Unit	Remarks
Timer mode current	I_{CCT}	VCC	Main Timer mode	T_A = + 25°C, When LVD is off	3.2	6	mA	*1, *3
				T_A = + 85°C, When LVD is off	-	15	mA	*1, *3
			Sub Timer mode	T_A = + 25°C, When LVD is off	0.9	3	mA	*1, *4
				T_A = + 85°C, When LVD is off	-	12	mA	*1, *4
Stop mode current	I_{CCH}		Stop mode	T_A = + 25°C, When LVD is off	0.8	3	mA	*1
				T_A = + 85°C, When LVD is off	-	12	mA	*1

*1: When all ports are fixed

*2: V_{CC} = 5.5 V

*3: When using the crystal oscillator of 4 MHz(Including the current consumption of the oscillation circuit)

*4: When using the crystal oscillator of 32 kHz(Including the current consumption of the oscillation circuit)

Low-Voltage Detection Current

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, TA = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value Typ	Value Max	Unit	Remarks
Low voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation for interrupt V_{CC} = 5.5 V	4	7	µA	At not detect

Flash Memory Current

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, TA = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value Typ	Value Max	Unit	Remarks
Flash memory write/erase current	$I_{CCFLASH}$	VCC	MainFlash At Write/Erase	11.4	13.1	mA	*
			WorkFlash At Write/Erase	11.4	13.1	mA	

*: The current at which to write or erase Flash memory, $I_{CCFLASH}$ is added to I_{CC}.

A/D Converter Current

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value Typ	Value Max	Unit	Remarks
Power supply current	I_{CCAD}	AVCC	At 1unit operation	0.47	0.62	mA	
			At stop	0.06	25	µA	
Reference power supply current	I_{CCAVRH}	AVRH	At 1unit operation AVRH=5.5 V	1.1	1.96	mA	
			At stop	0.06	4	µA	

12.3.2 Pin Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	-	V_{CC} × 0.8	-	V_{CC} + 0.3	V	
		5 V tolerant input pin	-	V_{CC} × 0.8	-	V_{SS} + 5.5	V	
L level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	-	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
		5 V tolerant input pin	-	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
H level output voltage	V_{OH}	4 mA type	V_{CC} ≥ 4.5 V I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V I_{OH} = - 2 mA					
		12 mA type	V_{CC} ≥ 4.5 V I_{OH} = - 12 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V I_{OH} = - 8 mA					
		P80, P81	V_{CC} ≥ 4.5 V I_{OH} = - 20.5 mA	V_{CC} - 0.4	-	V_{CC}	V	
			V_{CC} < 4.5 V I_{OH} = - 13.0 mA					

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
L level output voltage	V_{OL}	4 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 2 mA					
		12 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 12 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 8 mA					
		P80, P81	$V_{CC} \geq 4.5$ V, I_{OL} = 18.5 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 10.5 mA					
Input leak current	I_{IL}	-	-	- 5	-	+5	µA	
Pull-up resistance value	R_{PU}	Pull-up pin	$V_{CC} \geq 4.5$ V	25	50	100	kΩ	
			$V_{CC} < 4.5$ V	30	80	200		
Input capacitance	C_{IN}	Other than VCC, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

12.4 AC Characteristics

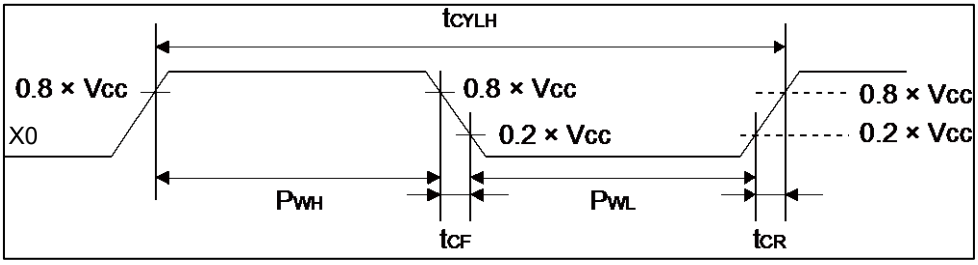
12.4.1 Main Clock Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0 X1	$V_{CC} \geq 4.5$ V	4	48	MHz	When crystal oscillator is connected
			$V_{CC} < 4.5$ V	4	20		
			$V_{CC} \geq 4.5$ V	4	48	MHz	When using external clock
			$V_{CC} < 4.5$ V	4	20		
Input clock cycle	t_{CYLH}		$V_{CC} \geq 4.5$ V	20.83	250	ns	When using external clock
			$V_{CC} < 4.5$ V	50	250		
Input clock pulse width	-		P_{WH}/t_{CYLH} P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CF}, t_{CR}		-	-	5	ns	When using external clock
Internal operating clock*1 frequency	f_{CM}	-	-	-	144	MHz	Master clock
	f_{CC}	-	-	-	144	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	72	MHz	APB0 bus clock*2
	f_{CP1}	-	-	-	72	MHz	APB1 bus clock*2
	f_{CP2}	-	-	-	72	MHz	APB2 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	6.94	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	13.8	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	13.8	-	ns	APB1 bus clock*2
	t_{CYCP2}	-	-	13.8	-	ns	APB2 bus clock*2

*1: For more information about each internal operating clock, see "CHAPTER 2-1: Clock" in "FM3 Family PERIPHERAL MANUAL".

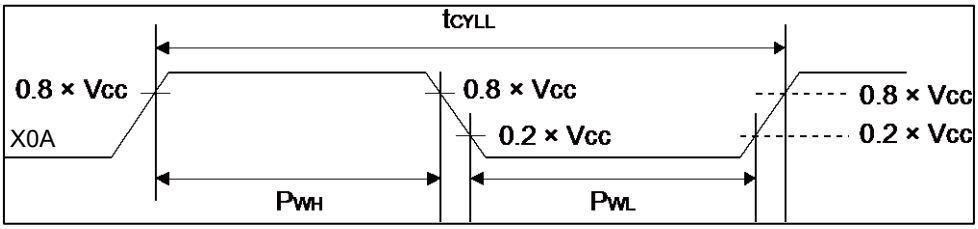
*2: For about each APB bus which each peripheral is connected to, see "8. Block Diagram" in this data sheet.



12.4.2 Sub Clock Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	1/ t_{CYLL}	X0A X1A	-	-	32.768	-	kHz	When crystal oscillator is connected
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL} P_{WL}/t_{CYLL}	45	-	55	%	When using external clock



12.4.3 Internal CR Oscillation Characteristics

High-speed Internal CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRH}	T_A = + 25°C	3.96	4	4.04	MHz	When trimming*1
		T_A = 0°C to + 70°C	3.84	4	4.16		
		T_A = - 40°C to + 85°C	3.8	4	4.2		
		T_A = - 40°C to + 85°C	3	4	5		When not trimming
Frequency stability time	t_{CRWT}	-	-	-	90	µs	*2

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming.

*2: Frequency stable time is time to stable of the frequency of the High-speed CR clock after the trim value is set.
After setting the trim value, the period when the frequency stability time passes can use the High-speed CR clock as a source clock.

Low-speed Internal CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	

12.4.4 Operating Conditions of Main PLL (In the case of using main clock for input of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiple rate	-	13	-	75	multiple	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	300	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	144	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see "CHAPTER 2-1: Clock" in "FM3 Family PERIPHERAL MANUAL".

12.4.5 Operating Conditions of Main PLL (In the case of using high-speed internal CR)

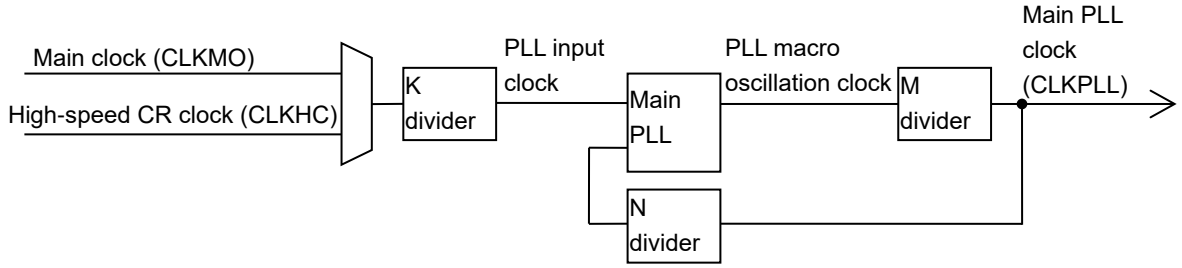
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiple rate	-	13	-	75	multiple	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	300	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	144	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see "CHAPTER 2-1: Clock" in "FM3 Family PERIPHERAL MANUAL".

Main PLL connection



12.4.6 Reset Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	

12.4.7 Power-on Reset Timing

(V_{SS} = 0V, T_A = - 40°C to + 85°C)

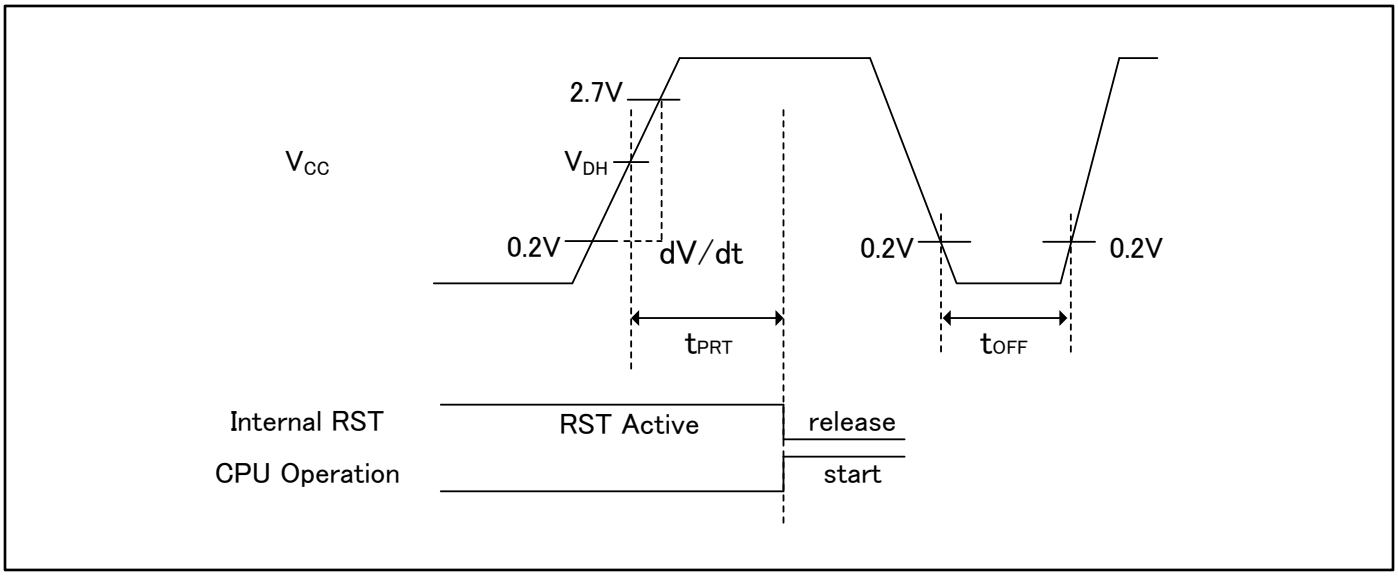
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply shut down time	t_{OFF}	VCC	-	50	-	-	ms	*1
Power ramp rate	dV/dt		Vcc: 0.2 V to 2.70 V	0.8	-	1000	mV/µs	*2
Time until releasing Power-on reset	t_{PRT}		-	0.57	-	0.76	ms	

*1: V_{CC} must be held below 0.2 V for minimum period of t_{OFF}. Improper initialization may occur if this condition is not met.

*2: This dV/dt characteristic is applied at the power-on of cold start (t_{OFF}>50 ms).

Note:

- *If t_{OFF} cannot be satisfied designs must assert external reset(INITX) at power-up and at any brownout event per "12. 4. 6.Reset Input Characteristics".*



Glossary

VDH: detection voltage of Low Voltage detection reset. See "12.6.Low-voltage Detection Characteristics"

12.4.8 External Bus Timing

External bus clock output characteristics

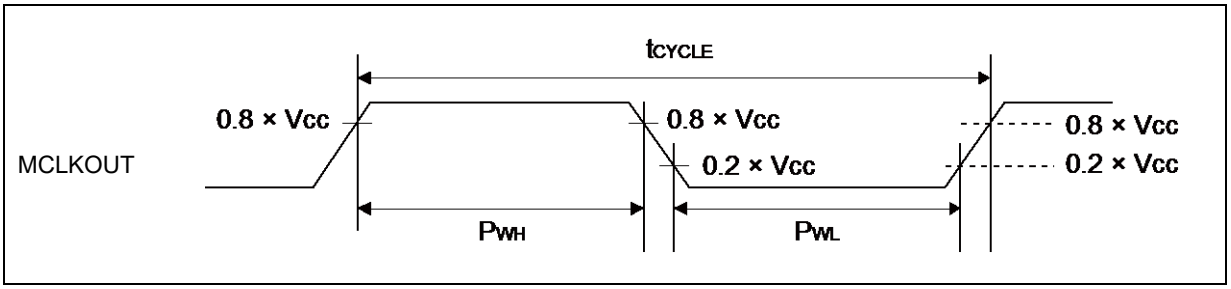
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{CYCLE}	MCLKOUT*1	$V_{CC} \geq 4.5$ V	-	50*2	MHz
			$V_{CC} < 4.5$ V	-	32*3	MHz

*1: External bus clock (MCLKOUT) is divided clock of HCLK.
For more information about setting of clock divider, see "CHPATER 12: External Bus Interface" in "FM3 Family PERIPHERAL MANUAL".
When external bus clock is not output, this characteristic does not give any effect on external bus operation.

*2: When AHB bus clock frequency is more than 100 MHz, the divider setting for MCLKOUT must be more than 4.

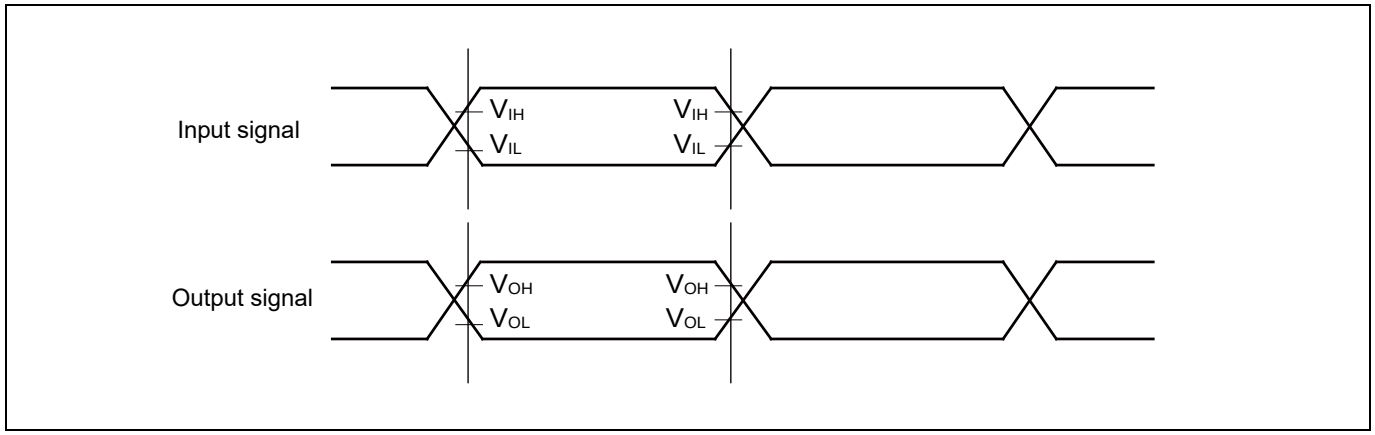
*3: When AHB bus clock frequency is more than 64 MHz, the divider setting for MCLKOUT must be more than 4.



External bus signal input/output characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V_{IH}	-	0.8 × V_{CC}	V	
	V_{IL}		0.2 × V_{CC}	V	
Signal output characteristics	V_{OH}		0.8 × V_{CC}	V	
	V_{OL}		0.2 × V_{CC}	V	



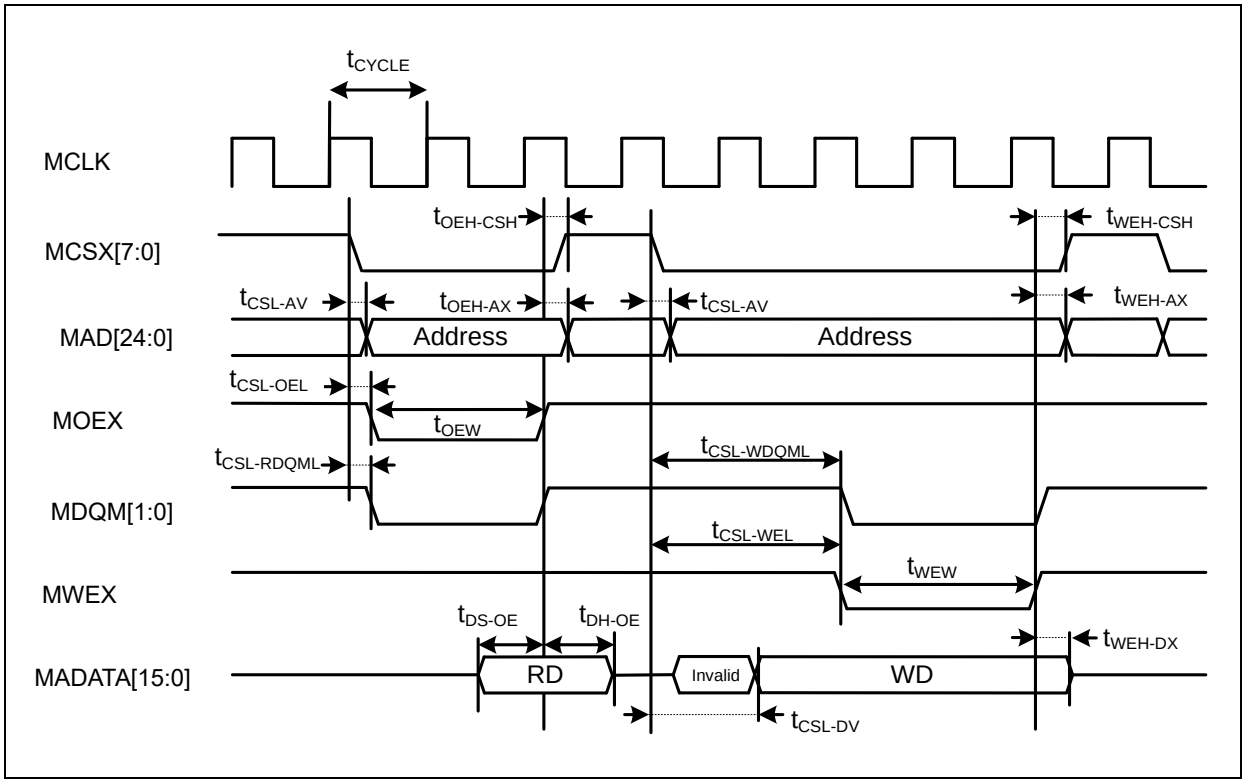
Separate Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
MOEX Min pulse width	t_{OEW}	MOEX	$V_{CC} \geq 4.5$ V	MCLK×n-3	-	ns
			$V_{CC} < 4.5$ V			
MCSX ↓ → Address output delay time	$t_{CSL - AV}$	MCSX[7:0] MAD[24:0]	$V_{CC} \geq 4.5$ V	-9	+9	ns
			$V_{CC} < 4.5$ V	-12	+12	
MOEX ↑ → Address hold time	$t_{OEH - AX}$	MOEX MAD[24:0]	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MCSX ↓ → MOEX ↓ delay time	$t_{CSL - OEL}$	MOEX MCSX[7:0]	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MOEX ↑ → MCSX ↑ time	$t_{OEH - CSH}$		$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MCSX ↓ → MDQM ↓ delay time	$t_{CSL - RDQML}$	MCSX MDQM[1:0]	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
Data set up → MOEX ↑ time	$t_{DS - OE}$	MOEX MADATA[15:0]	$V_{CC} \geq 4.5$ V	20	-	ns
			$V_{CC} < 4.5$ V	38	-	
MOEX ↑ → Data hold time	$t_{DH - OE}$	MOEX MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	-	ns
			$V_{CC} < 4.5$ V			
MWEX Min pulse width	t_{WEW}	MWEX	$V_{CC} \geq 4.5$ V	MCLK×n-3	-	ns
			$V_{CC} < 4.5$ V			
MWEX ↑ → Address output delay time	$t_{WEH - AX}$	MWEX MAD[24:0]	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MCSX ↓ → MWEX ↓ delay time	$t_{CSL - WEL}$	MWEX MCSX[7:0]	$V_{CC} \geq 4.5$ V	MCLK×n-9	MCLK×n+9	ns
			$V_{CC} < 4.5$ V	MCLK×n-12	MCLK×n+12	
MWEX ↑ → MCSX ↑ delay time	$t_{WEH - CSH}$		$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MCSX ↓→ MDQM ↓ delay time	$t_{CSL-WDQML}$	MCSX MDQM[1:0]	$V_{CC} \geq 4.5$ V	MCLK×n-9	MCLK×n+9	ns
			$V_{CC} < 4.5$ V	MCLK×n-12	MCLK×n+12	
MCSX ↓→ Data output time	$t_{CSL - DV}$	MCSX MADATA[15:0]	$V_{CC} \geq 4.5$ V	MCLK-9	MCLK+9	ns
			$V_{CC} < 4.5$ V	MCLK-12	MCLK+12	
MWEX ↑ → Data hold time	$t_{WEH - DX}$	MWEX MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	

Note:

− *When the external load capacitance = 30 pF. (m = 0 to 15, n = 1 to 16)*


tCYCLE
MCLK
MCSX[7:0]
MAD[24:0]
MOEX
MDQM[1:0]
MWEX
MADATA[15:0]
tOEH-CSH
tWEH-CSH
tCSL-AV
tOEH-AX
tCSL-AV
tWEH-AX
Address
Address
tCSL-OEL
tOEW
tCSL-RDQML
tCSL-WDQML
tCSL-WEL
tWEW
tDS-OE
tDH-OE
tWEH-DX
RD
Invalid
WD
tCSL-DV

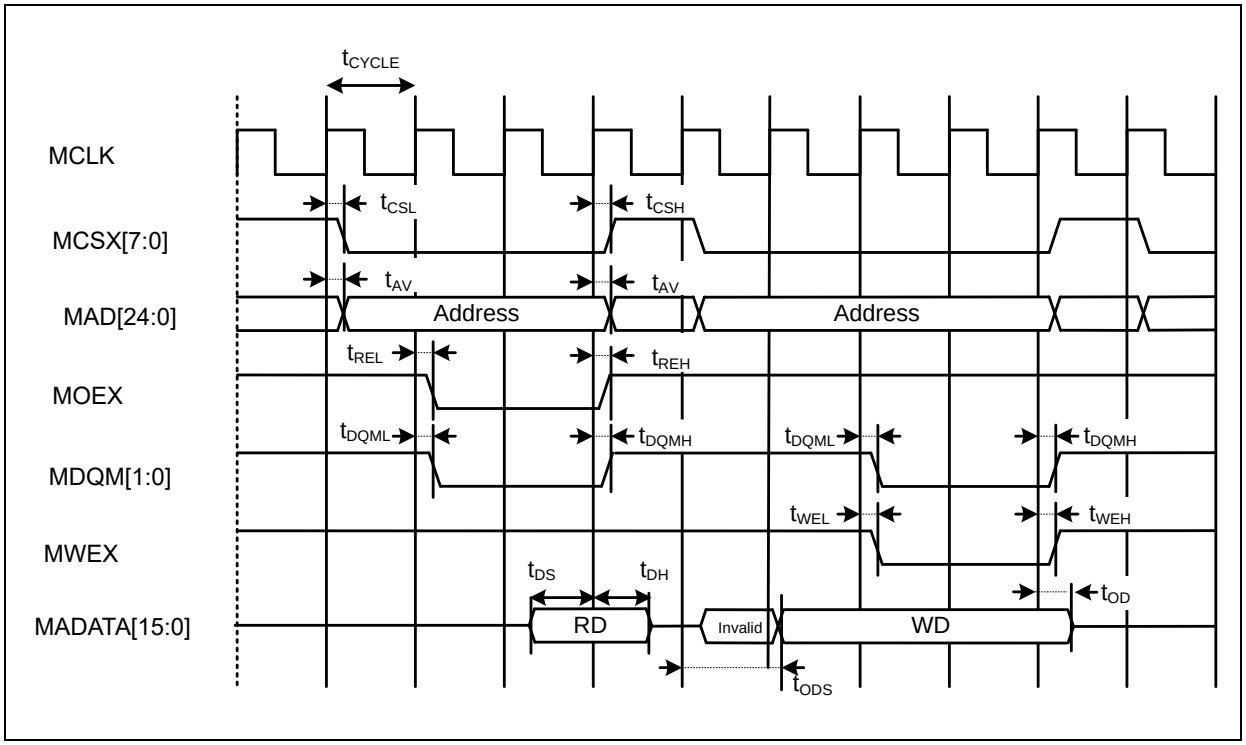
Separate Bus Access Synchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Address delay time	t_{AV}	MCLK MAD[24:0]	$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
MCSX delay time	t_{CSL}	MCLK MCSX[7:0]	$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
	t_{CSH}		$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
MOEX delay time	t_{REL}	MCLK MOEX	$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
	t_{REH}		$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
Data set up → MCLK ↑ time	t_{DS}	MCLK MADATA[15:0]	$V_{CC} \geq 4.5$ V	19	-	ns
			$V_{CC} < 4.5$ V	37		
MCLK ↑ → Data hold time	t_{DH}	MCLK MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	-	ns
			$V_{CC} < 4.5$ V			
MWEX delay time	t_{WEL}	MCLK MWEX	$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
	t_{WEH}		$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
MDQM[1:0] delay time	t_{DQML}	MCLK MDQM[1:0]	$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
	t_{DQMH}		$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
MCLK ↑ → Data output time	t_{ODS}	MCLK, MADATA[15:0]	$V_{CC} \geq 4.5$ V	MCLK+1	MCLK+18	ns
			$V_{CC} < 4.5$ V		MCLK+24	
MCLK ↑ → Data hold time	t_{OD}	MCLK MADATA[15:0]	$V_{CC} \geq 4.5$ V	1	18	ns
			$V_{CC} < 4.5$ V		24	

Note:

- *When the external load capacitance = 30 pF.*



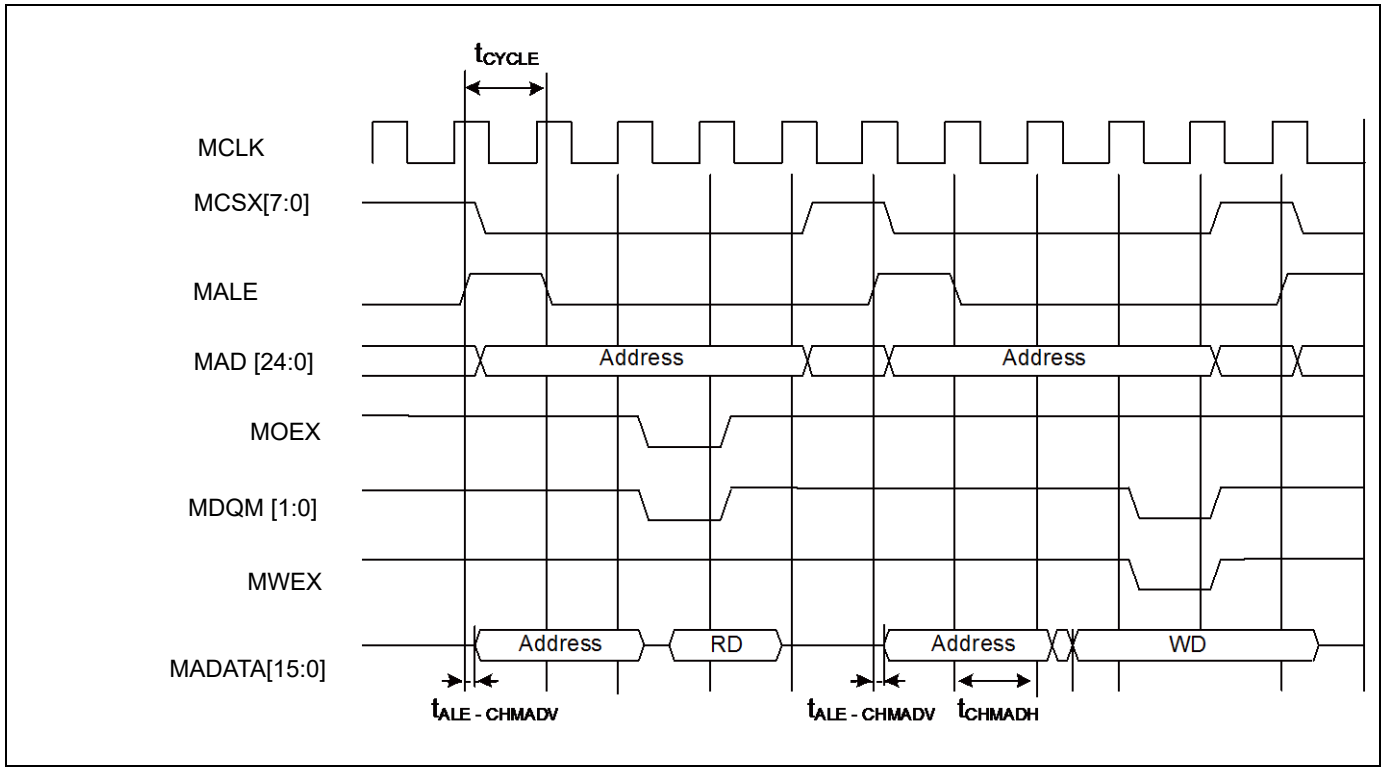
Multiplexed Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Multiplexed address delay time	$t_{ALE-CHMADV}$	MALE MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	10	ns
			$V_{CC} < 4.5$ V		20	
Multiplexed address hold time	t_{CHMADH}		$V_{CC} \geq 4.5$ V	MCLK×n+0	MCLK×n+10	ns
			$V_{CC} < 4.5$ V	MCLK×n+0	MCLK×n+20	

Note:

- *When the external load capacitance = 30 pF. (m = 0 to 15, n = 1 to 16)*



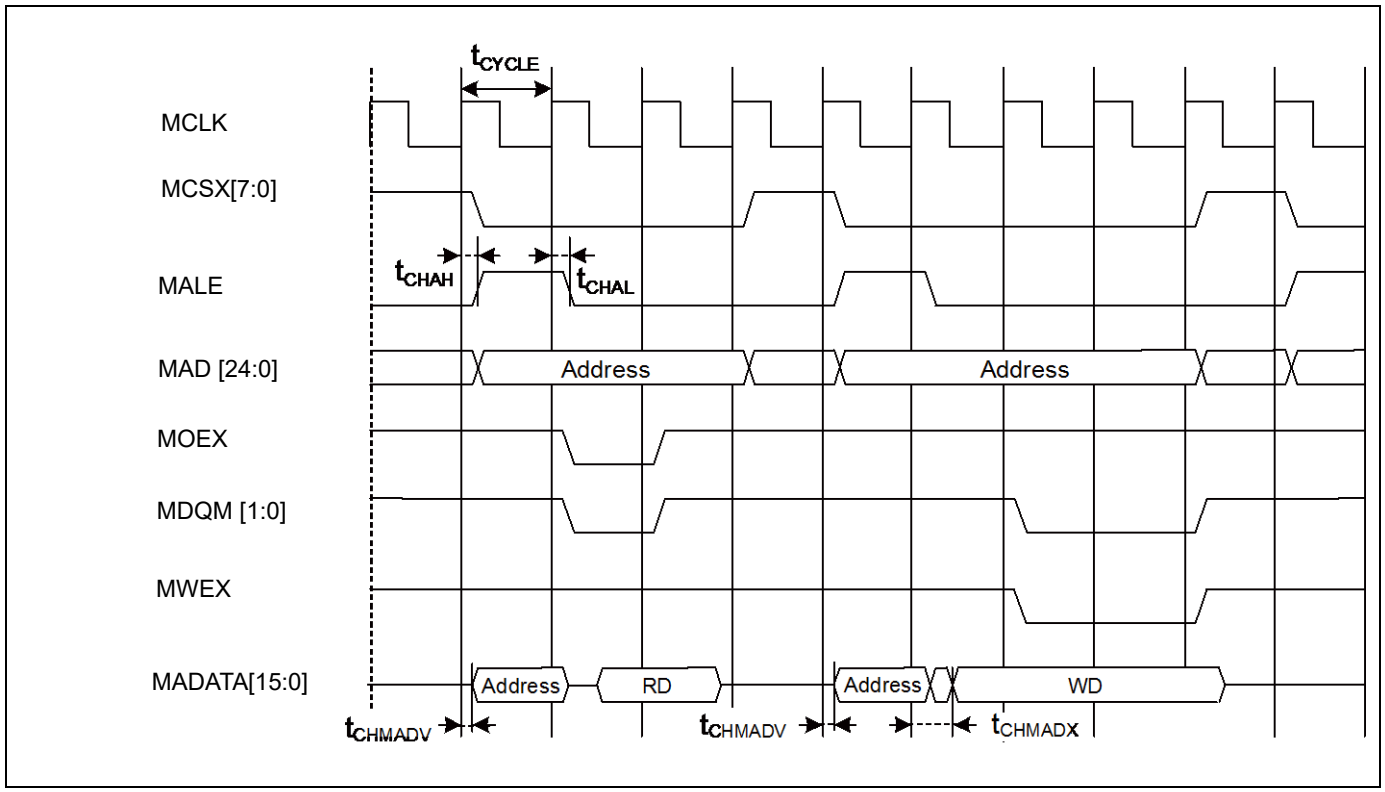
Multiplexed Bus Access Synchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MALE delay time	t_{CHAL}	MCLK ALE	$V_{CC} \geq 4.5$ V	1	9	ns	
			$V_{CC} < 4.5$ V		12	ns	
	t_{CHAH}		$V_{CC} \geq 4.5$ V	1	9	ns	
			$V_{CC} < 4.5$ V		12	ns	
MCLK ↑ → Multiplexed Address delay time	t_{CHMADV}	MCLK MADATA[15:0]	$V_{CC} \geq 4.5$ V	1	t_{OD}	ns	
			$V_{CC} < 4.5$ V				
MCLK ↑ → Multiplexed Data output time	t_{CHMADX}		$V_{CC} \geq 4.5$ V	1	t_{OD}	ns	
			$V_{CC} < 4.5$ V				

Note:

- *When the external load capacitance = 30 pF*



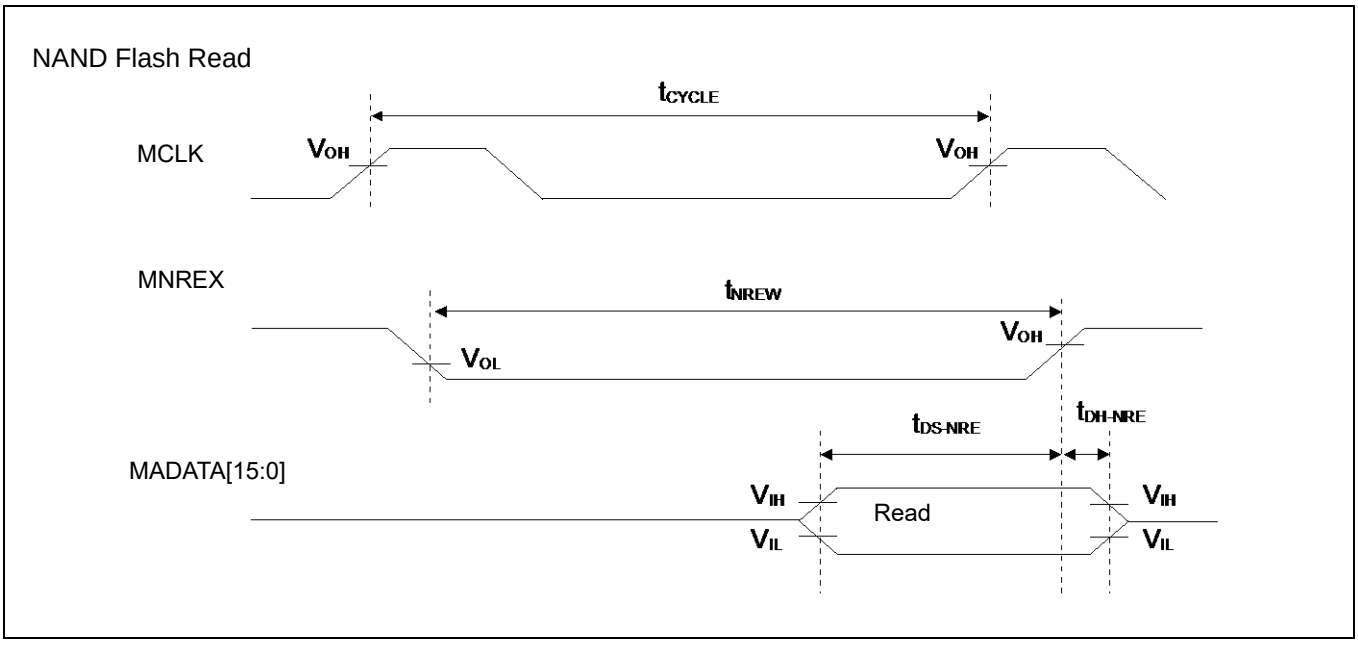
NAND Flash Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = -40°C to +85°C)

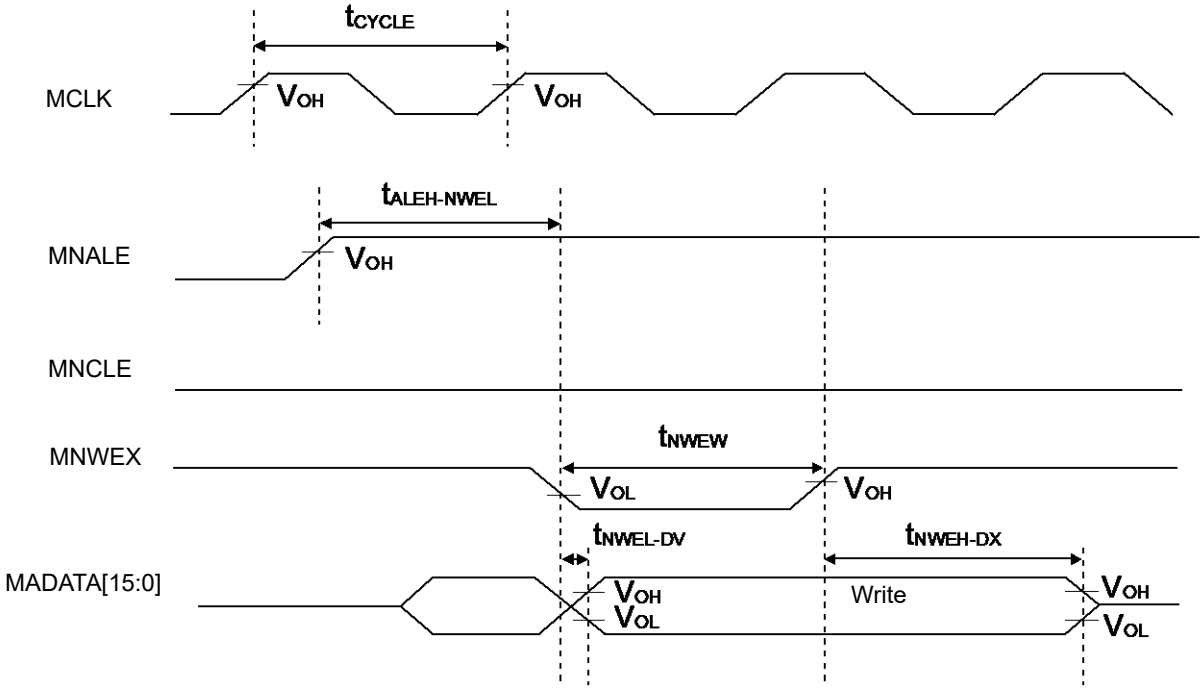
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
MNREX Min pulse width	t_{NREW}	MNREX	$V_{CC} \geq 4.5$ V	MCLK×n-3	-	ns
			$V_{CC} < 4.5$ V			
Data setup → MNREX ↑ time	t_{DS-NRE}	MNREX MADATA[15:0]	$V_{CC} \geq 4.5$ V	20	-	ns
			$V_{CC} < 4.5$ V	38	-	
MNREX ↑ → Data hold time	t_{DH-NRE}	MNREX MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	-	ns
			$V_{CC} < 4.5$ V			
MNALE ↑ → MNWEX delay time	$t_{ALEH-NWEL}$	MNALE MNWEX	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MNALE ↓ → MNWEX delay time	$t_{ALEL-NWEL}$	MNALE MNWEX	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MNCLE ↑ → MNWEX delay time	$t_{CLEH-NWEL}$	MNCLE MNWEX	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MNWEX ↑ → MNCLE delay time	$t_{NWEH-CLEL}$	MNCLE MNWEX	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MNWEX Min pulse width	t_{NWEW}	MNWEX	$V_{CC} \geq 4.5$ V	MCLK×n-3	-	ns
			$V_{CC} < 4.5$ V			
MNWEX ↓ → Data delay time	$t_{NWEL-DV}$	MNWEX MADATA[15:0]	$V_{CC} \geq 4.5$ V	- 9	+ 9	ns
			$V_{CC} < 4.5$ V	-12	+12	
MNWEX ↑ → Data hold time	$t_{NWEH-DX}$	MNWEX MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	

Note:

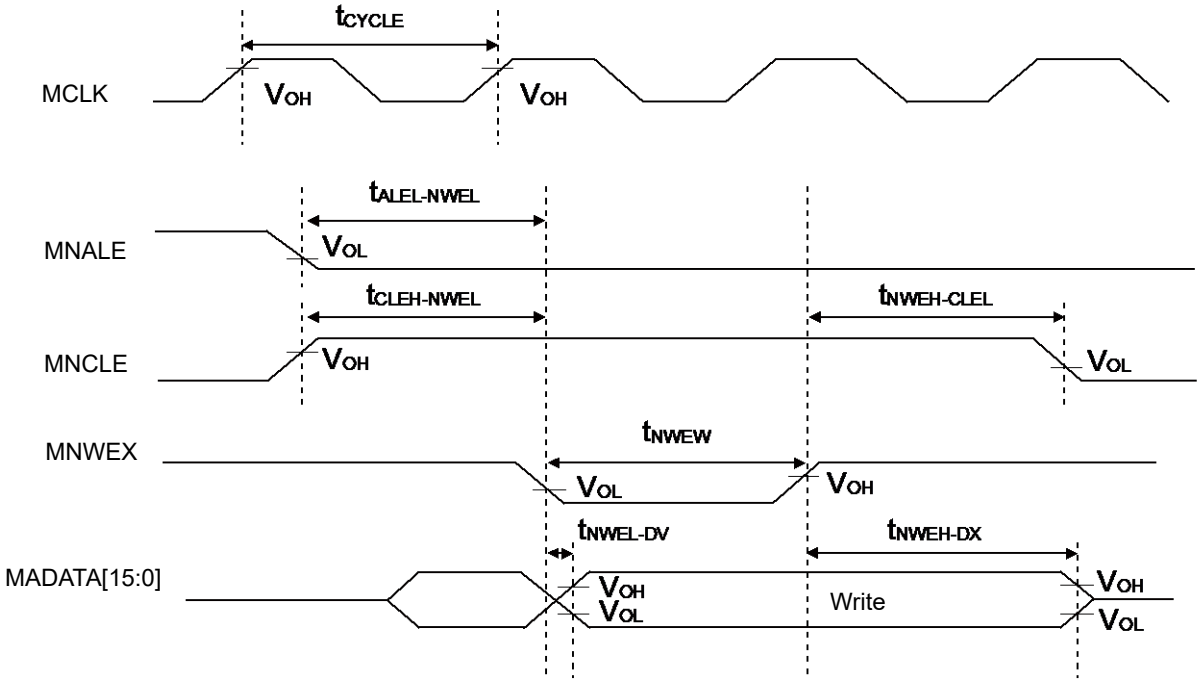
- *When the external load capacitance = 30 pF. (m=0 to 15, n=1 to 16)*



NAND Flash Address Write



NAND Flash Command Write

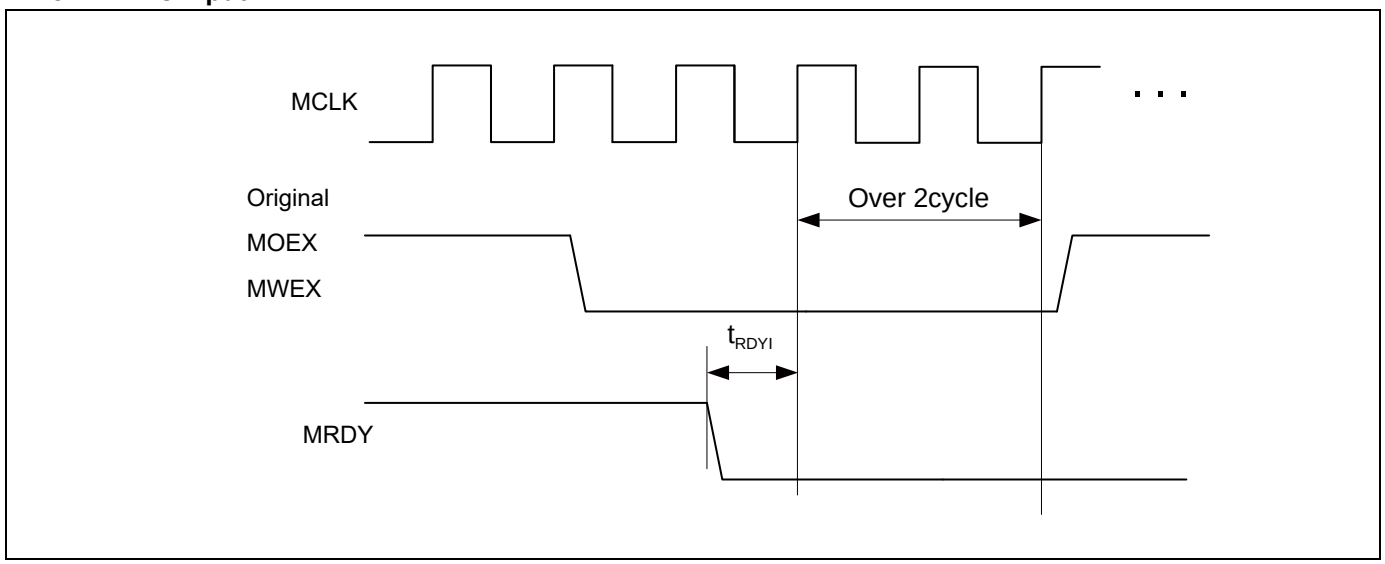


External Ready Input Timing

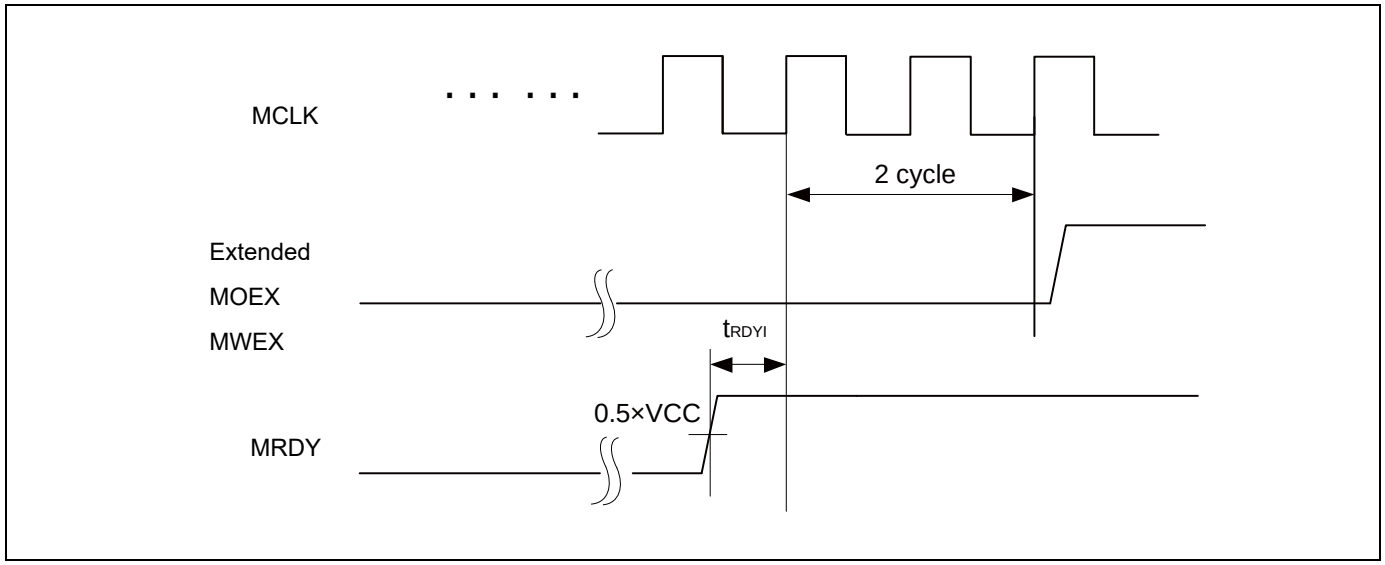
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK ↑ MRDY input setup time	t_{RDYI}	MCLK MRDY	$V_{CC} \geq 4.5$ V	19	-	ns	
			$V_{CC} < 4.5$ V	37			

When RDY is input



When RDY is released

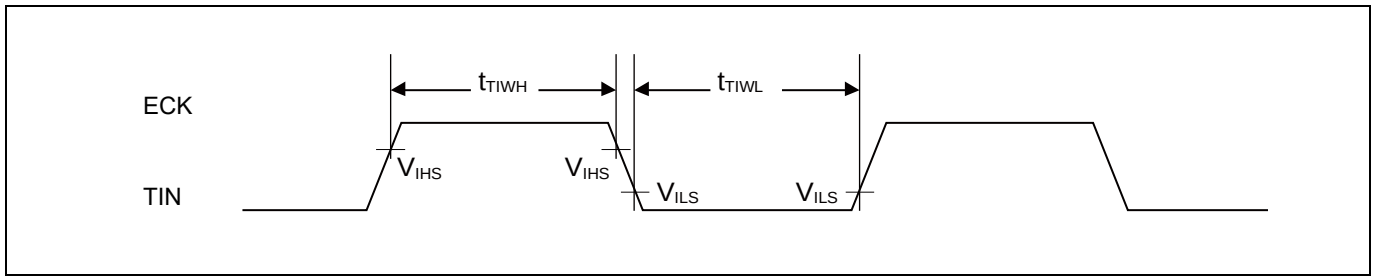


12.4.9 Base Timer Input Timing

Timer input timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

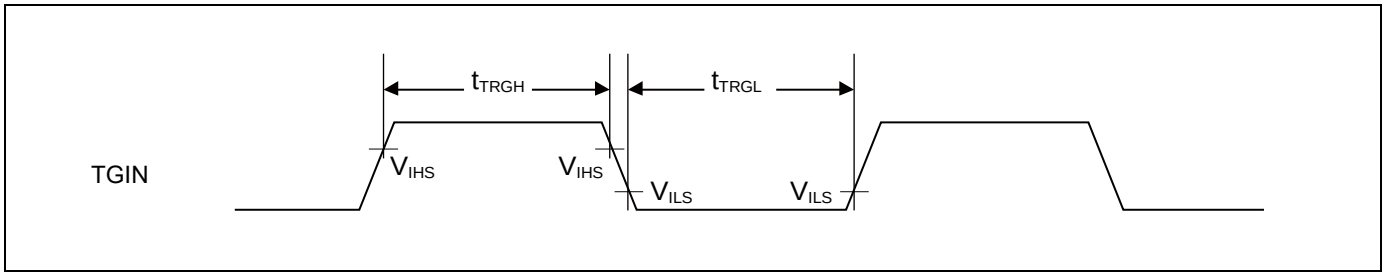
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



Trigger input timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



Note:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Base Timer is connected to, see "8 Block Diagram" in this data sheet.

12.4.10 CSIO/UART Timing

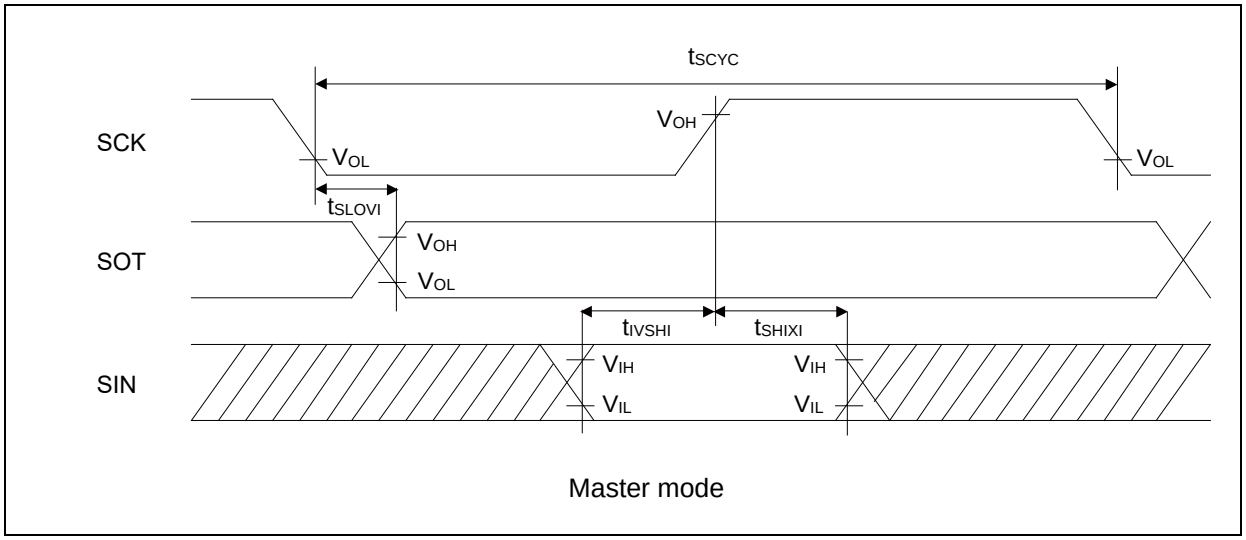
CSIO (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

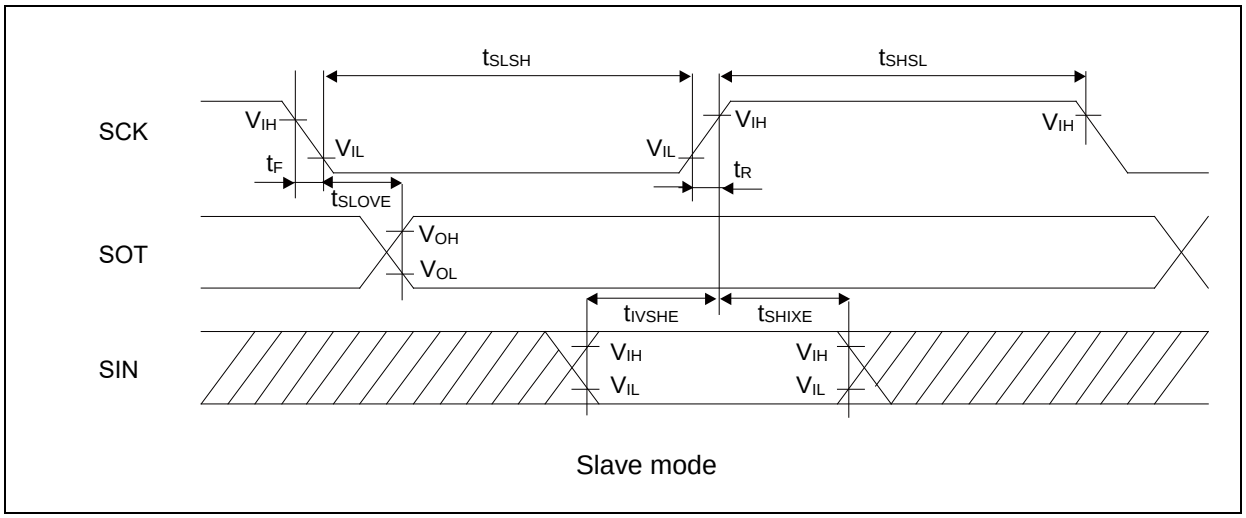
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx SOTx		-30	+30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx SINx		20	-	20	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Multi-function Serial is connected to, see "8 Block Diagram" in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance = 30 pF.*



Master mode



Slave mode

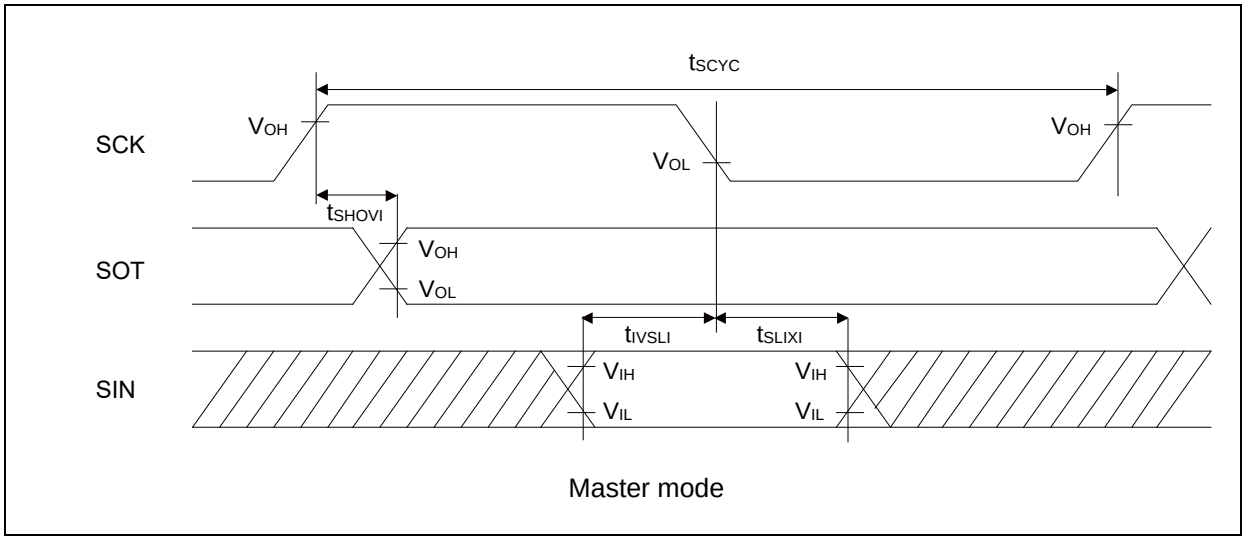
CSIO (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

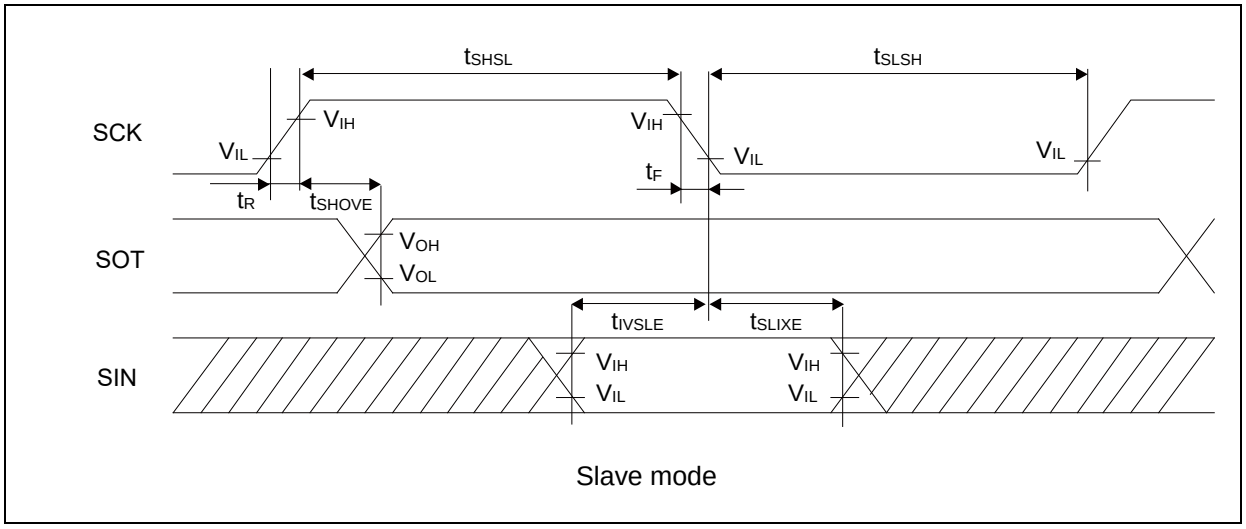
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx SOTx		-30	+30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx SINx		50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx SINx		20	-	20	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Multi-function Serial is connected to, see "8 Block Diagram" in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance = 30 pF.*



Master mode



Slave mode

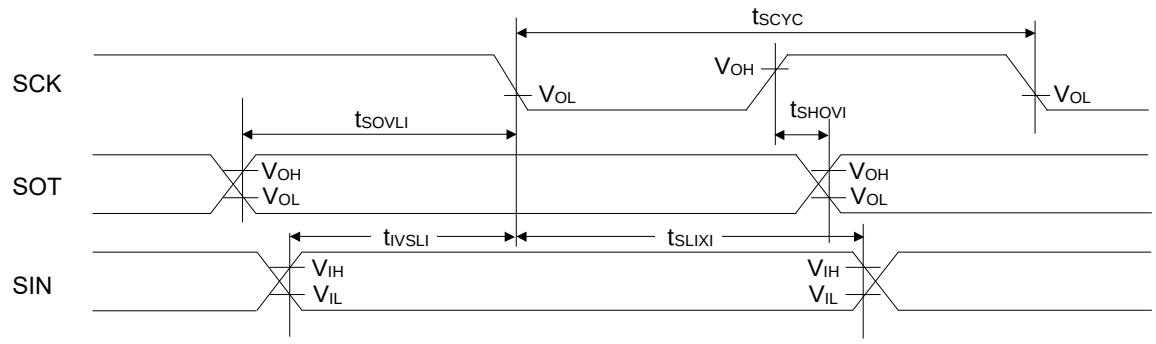
CSIO (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

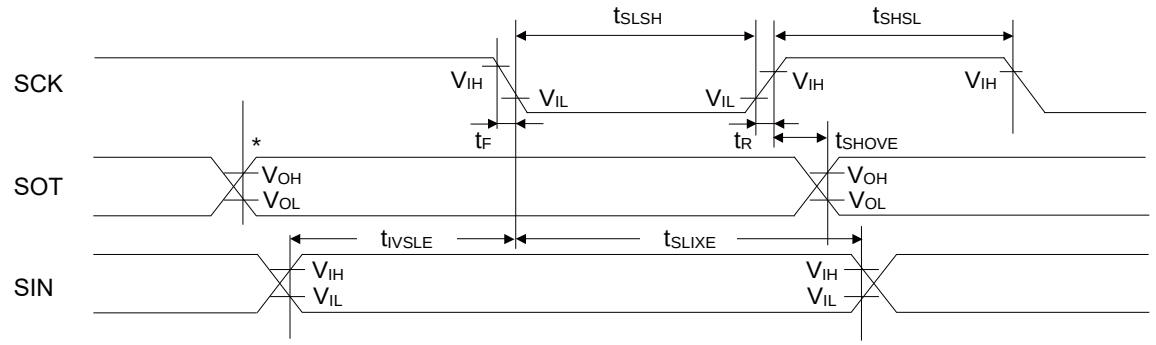
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx SOTx		-30	+30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx SINx		50	-	30	-	ns
SCK ↓→ SIN hold time	t_{SLIXI}	SCKx SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx SINx		10	-	10	-	ns
SCK ↓→ SIN hold time	t_{SLIXE}	SCKx SINx		20	-	20	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Multi-function Serial is connected to, see "8 Block Diagram" in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance = 30 pF.*



Master mode



Slave mode

*: Changes when writing to TDR register

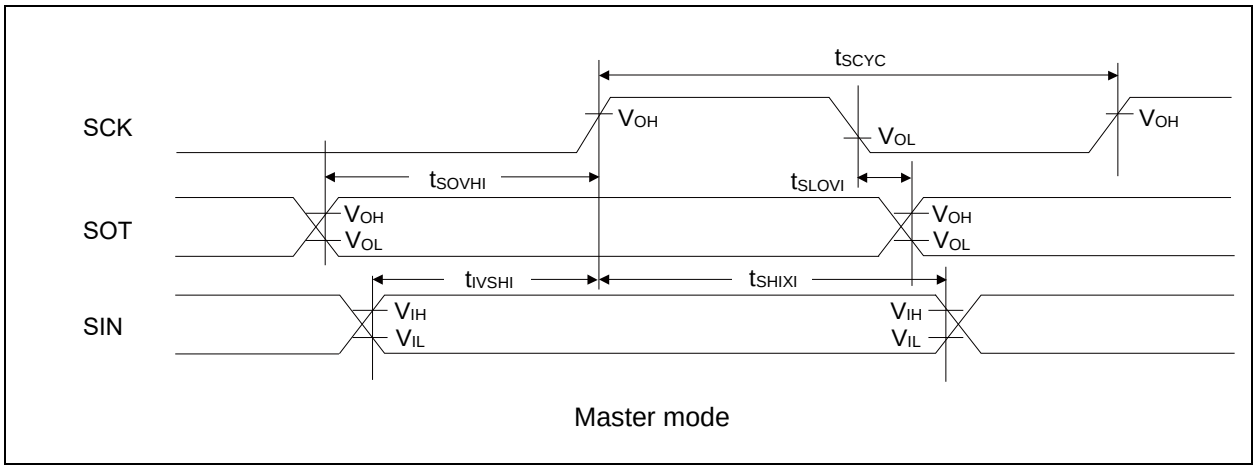
CSIO (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

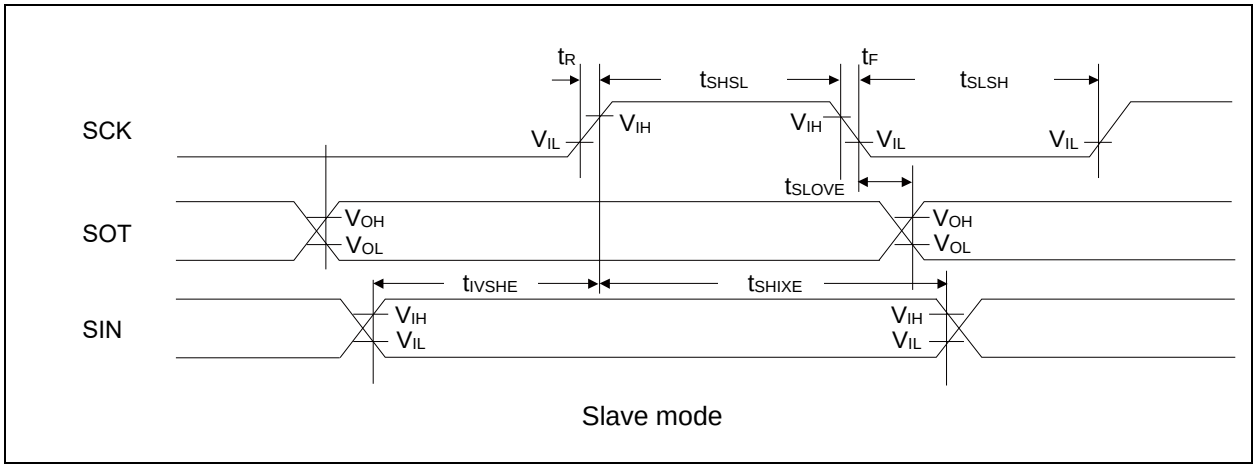
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx SOTx		-30	+30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx SINx		20	-	20	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Multi-function Serial is connected to, see "8 Block Diagram" in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance = 30 pF.*



Master mode

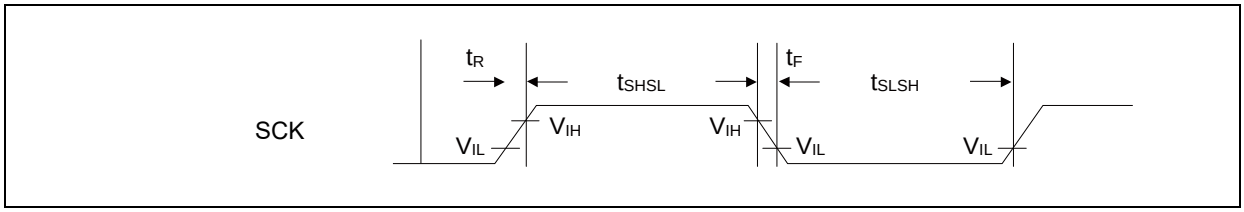


Slave mode

UART external clock input (EXT = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock H pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK fall time	t_F		-	5	ns	
SCK rise time	t_R		-	5	ns	



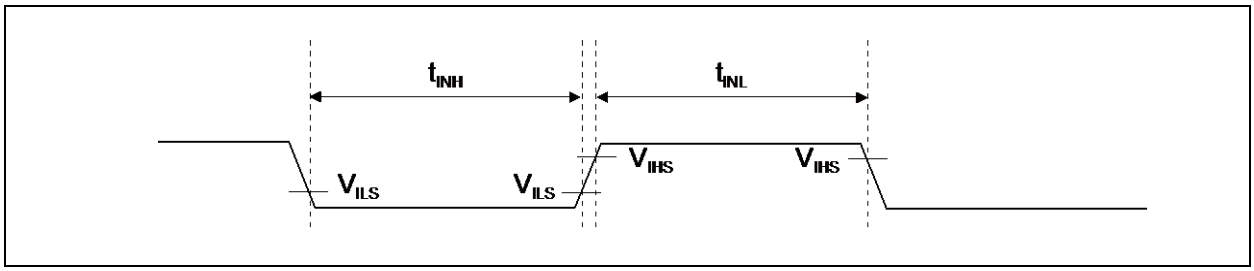
12.4.11 External Input Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTG	-	$2t_{CYCP}$*	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$*	-	ns	Wave form generator
		INTxx, NMIX	Except Timer mode, Stop mode	$2t_{CYCP}$ + 100*	-	ns	External interrupt NMI
			Timer mode, Stop mode	500	-	ns	

*: t_{CYCP} indicates the APB bus clock cycle time.

About the APB bus number which A/D converter, Multi-function Timer, External interrupt is connected to, see "8.Block Diagram" in this data sheet.



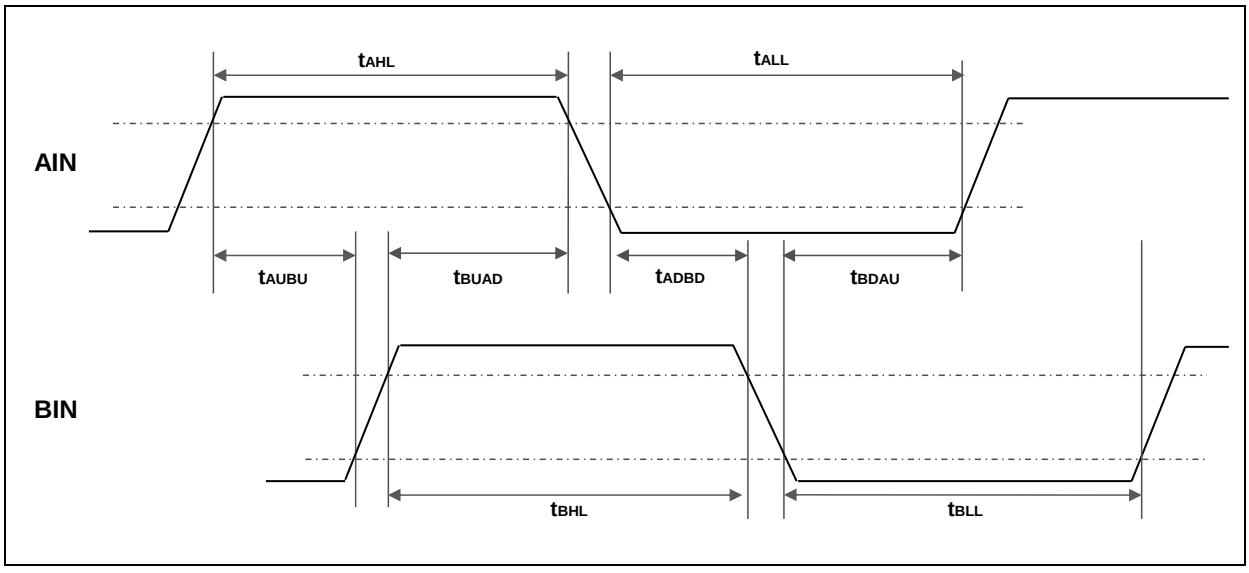
12.4.12 Quadrature Position/Revolution Counter timing

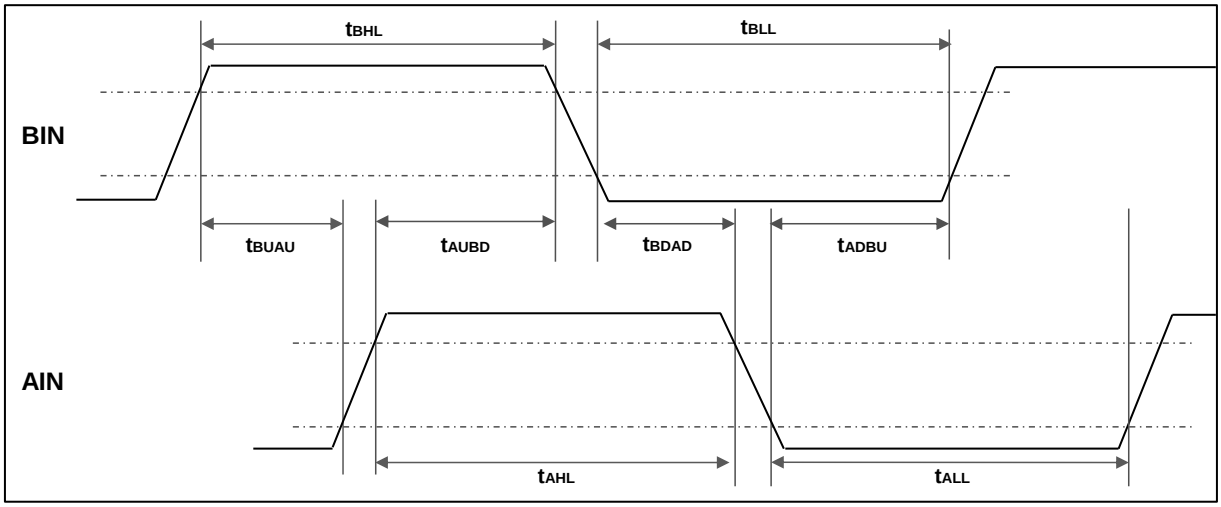
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

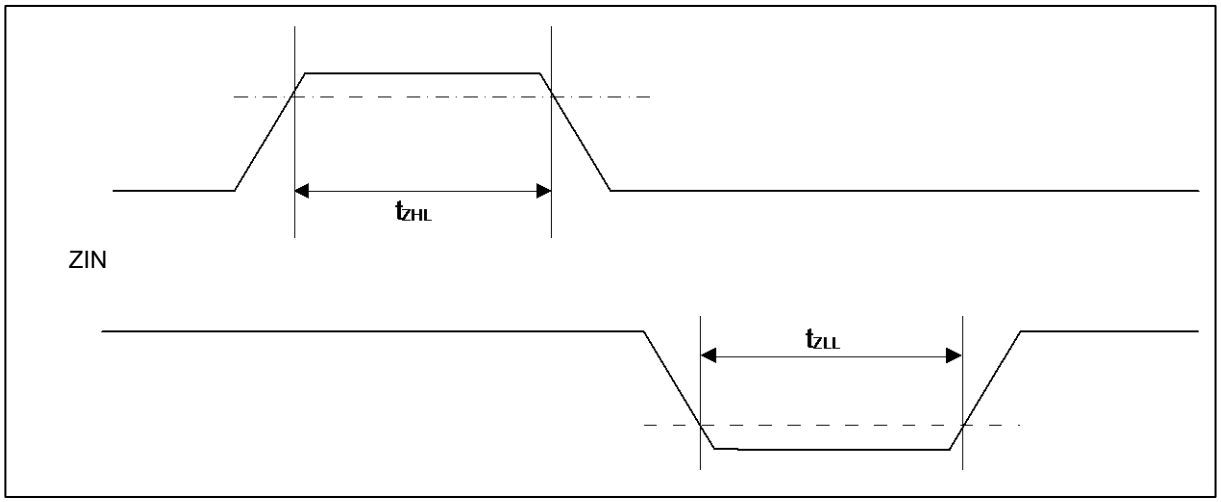
Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin H width	t_{AHL}	-	$2t_{CYCP}$*	-	ns
AIN pin L width	t_{ALL}	-			
BIN pin H width	t_{BHL}	-			
BIN pin L width	t_{BLL}	-			
BIN rise time from AIN pin H level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin H level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin L level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin L level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin H level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin H level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin L level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rise time from AIN pin L level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin H width	t_{ZHL}	QCR:CGSC=0			
ZIN pin L width	t_{ZLL}	QCR:CGSC=0			
AIN/BIN rise and fall time from determined ZIN level	t_{ZABE}	QCR:CGSC=1			
Determined ZIN level from AIN/BIN rise and fall time	t_{ABEZ}	QCR:CGSC=1			

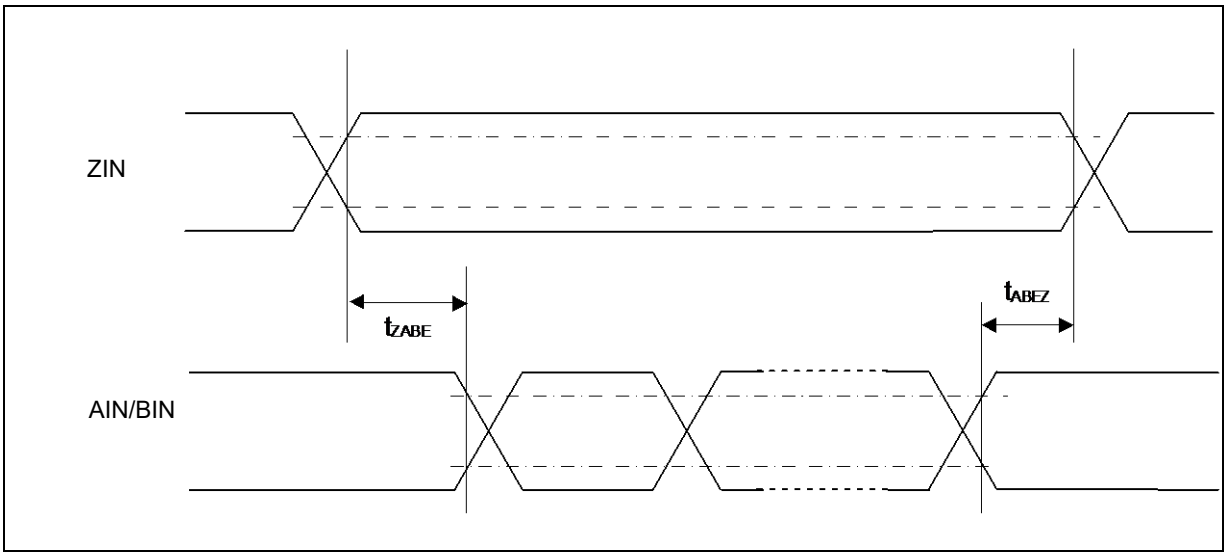
*: t_{CYCP} indicates the APB bus clock cycle time.

About the APB bus number which Quadrature Position/Revolution Counter is connected to, see "8.Block Diagram" in this data sheet.




tBHL
tBLL
BIN
tBUAU
tAUBD
tBDAD
tADBU
AIN
tAHL
tALL


tZHL
ZIN
tZLL


ZIN
tZABE
tABEZ
AIN/BIN

12.4.13 I²C Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCLclock L width	t_{LOW}		4.7	-	1.3	-	µs	
SCLclock H width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between STOP condition and START condition	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	8 MHz ≤ t_{CYCP} ≤ 40 MHz	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	*5
		40 MHz < t_{CYCP} ≤ 60 MHz	3 t_{CYCP}*4	-	3 t_{CYCP}*4	-	ns	*5
		60 MHz < t_{CYCP} ≤ 72 MHz	4 t_{CYCP}*4	-	4 t_{CYCP}*4	-	ns	*5

*1: R and C represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively.

Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy that it doesn't extend at least L period (t_{LOW}) of device's SCL signal.

*3: Fast-mode I²C bus device can be used on Standard-mode I²C bus system as long as the device satisfies the requirement of t_{SUDAT} ≥ 250 ns.

*4: t_{CYCP} is the APB bus clock cycle time.

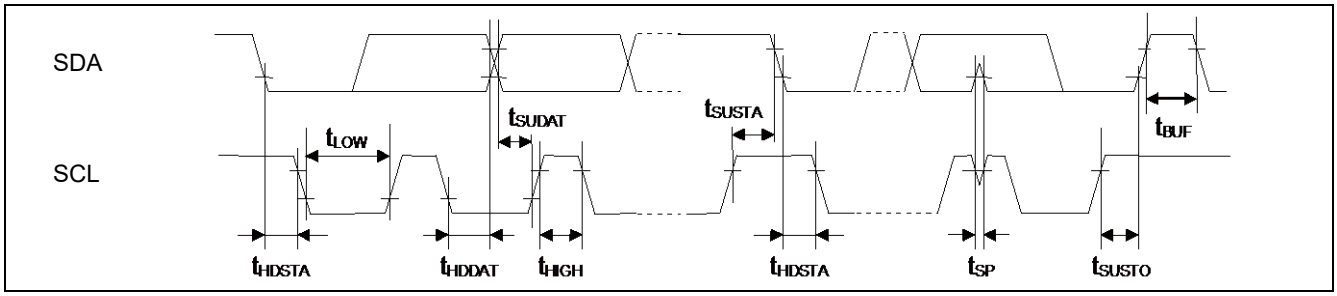
About the APB bus number that I2C is connected to, see "8 Block Diagram" in this data sheet.

To use Standard-mode, set the APB bus clock at 2 MHz or more.

To use Fast-mode, set the APB bus clock at 8 MHz or more.

*5: The number of the steps of the noise filter can be changed by register settings.

Change the number of the noise filter steps according to APB2 bus clock frequency.



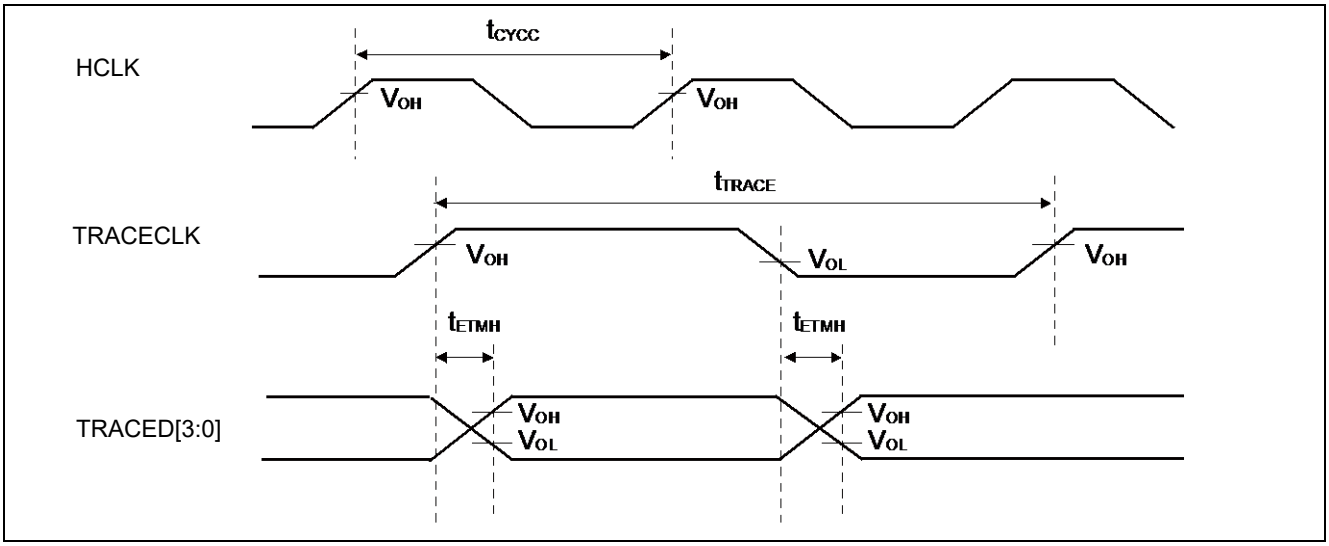
12.4.14 ETM Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK TRACED[3:0]	$V_{CC} \geq 4.5$ V	2	9	ns	
			$V_{CC} < 4.5$ V	2	15		
TRACECLK frequency	1/ t_{TRACE}	TRACECLK	$V_{CC} \geq 4.5$ V	-	50	MHz	
			$V_{CC} < 4.5$ V	-	32	MHz	
TRACECLK cycle time	t_{TRACE}		$V_{CC} \geq 4.5$ V	20	-	ns	
			$V_{CC} < 4.5$ V	31.25	-	ns	

Note:

- *When the external load capacitance = 30 pF.*



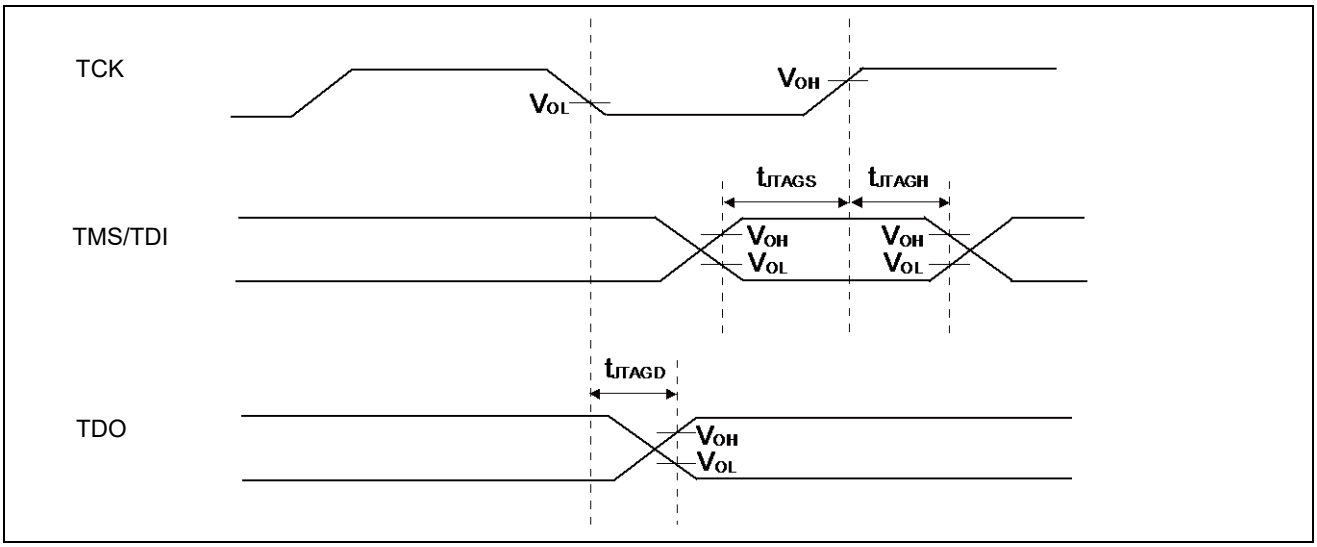
12.4.15 JTAG Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TMS, TDI hold time	t_{JTAGH}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TDO delay time	t_{JTAGD}	TCK, TDO	$V_{CC} \geq 4.5$ V	-	25	ns	
			$V_{CC} < 4.5$ V	-	45		

Note:

- *When the external load capacitance = 30 pF.*



12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-	± 4.0	± 4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential Nonlinearity	-	-	-	± 2.3	± 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	-	± 10	± 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	-	AVRH ± 10	AVRH ± 15	mV	
Conversion time	-	-	1.0*1	-	-	µs	AV_{CC} ≥ 4.5 V
			1.2*1	-	-		AV_{CC} < 4.5 V
Sampling time	t_S	-	*2	-	-	ns	AV_{CC} ≥ 4.5 V
			*2	-	-		AV_{CC} < 4.5 V
Compare clock cycle*3	t_{CCK}	-	50	-	2000	ns	AV_{CC} ≥ 4.5 V
							AV_{CC} < 4.5 V
State transition time to operation permission	t_{STT}	-	-	-	1.0	µs	
Analog input capacity	C_{AIN}	-	-	-	12.9	pF	
Analog input resistance	R_{AIN}	-	-	-	2	kΩ	AV_{CC} ≥ 4.5 V
					3.8		AV_{CC} < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	AV_{CC}	V	

*1: Conversion time is the value of sampling time (t_S) + compare time (t_C).

The condition of the minimum conversion time is the following.

AV_{CC} ≥ 4.5 V, HCLK=120 Hz sampling time: 300 ns, compare time: 700 ns

AV_{CC} < 4.5 V, HCLK=120 Hz sampling time: 500 ns, compare time: 700 ns

Ensure that it satisfies the value of sampling time (t_S) and compare clock cycle (t_{CCK}).

For setting*4 of sampling time and compare clock cycle, see "CHAPTER 1-1: 12-bit A/D Converter" in "FM3 Family PERIPHERAL MANUAL Analog Macro Part".

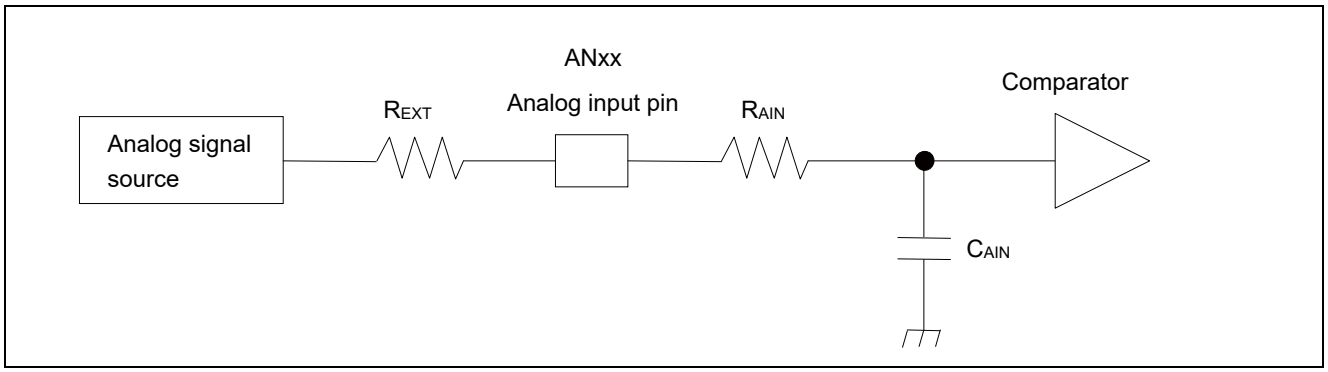
A/D Converter register is set at APB bus clock timing. Sampling and compare clock is set at Base clock (HCLK).

About the APB bus number which the A/D Converter is connected to, see "8 Block Diagram" in this data sheet.

*2: A necessary sampling time changes by external impedance.

Ensure that it set the sampling time to satisfy (Equation 1).

*3: Compare time (t_C) is the value of (Equation 2).



(Equation 1) $t_S \geq (R_{AIN} + R_{EXT}) \times C_{AIN} \times 9$

t_S: Sampling time

R_{AIN}: Input resistance of A/D = 2 kΩ at 4.5 V < AV_{CC} < 5.5 V
Input resistance of A/D = 3.8 kΩ at 2.7 V < AV_{CC} < 4.5 V

C_{AIN}: Input capacity of A/D = 12.9 pF at 2.7 V < AV_{CC} < 5.5 V

R_{EXT}: Output impedance of external circuit

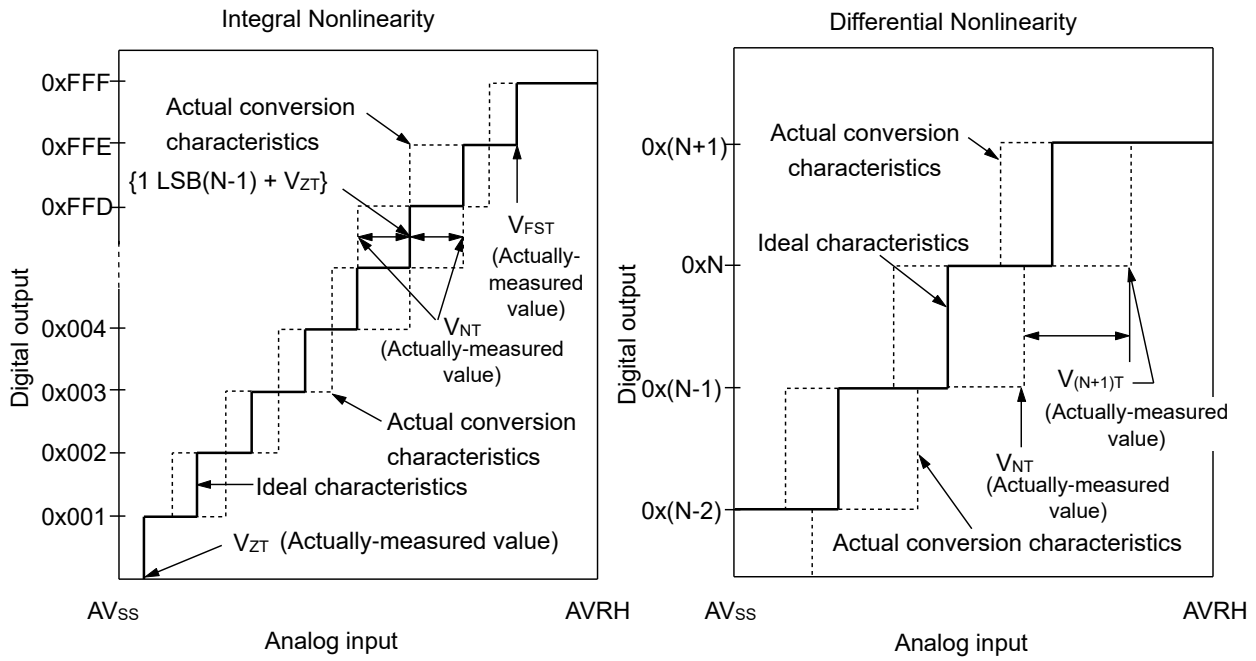
(Equation 2) $t_C = t_{CCK} \times 14$

t_C: Compare time

t_{CCK}: Compare clock cycle

Definition of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.
V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

12.6 Low-Voltage Detection Characteristics

12.6.1 Low-Voltage Detection Reset

(T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH	-	2.30	2.50	2.70	V	When voltage rises

12.6.2 Interrupt of Low-Voltage Detection

(T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 0000	2.58	2.8	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.9	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 0001	2.76	3.0	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.1	3.34	V	When voltage rises
Detected voltage	VDL	SVHI = 0010	2.94	3.2	3.45	V	When voltage drops
Released voltage	VDH		3.04	3.3	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 0011	3.31	3.6	3.88	V	When voltage drops
Released voltage	VDH		3.40	3.7	3.99	V	When voltage rises
Detected voltage	VDL	SVHI = 0100	3.40	3.7	3.99	V	When voltage drops
Released voltage	VDH		3.50	3.8	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 0111	3.68	4.0	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.1	4.42	V	When voltage rises
Detected voltage	VDL	SVHI = 1000	3.77	4.1	4.42	V	When voltage drops
Released voltage	VDH		3.86	4.2	4.53	V	When voltage rises
Detected voltage	VDL	SVHI = 1001	3.86	4.2	4.53	V	When voltage drops
Released voltage	VDH		3.96	4.3	4.64	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	4032 × t_{CYCP}*	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

12.7 MainFlash Memory Write/Erase Characteristics

12.7.1 Write / Erase time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 85°C)

Parameter		Value		Unit	Remarks
		Typ*	Max*		
Sector erase time	Large Sector	0.7	3.7	s	Includes write time prior to internal erase
	Small Sector	0.3	1.1		
Half word (16-bit) write time		12	384	µs	Not including system-level overhead time
Chip erase time		8	38.4	s	Includes write time prior to internal erase

*: The typical value is immediately after shipment, the maximum value is guarantee value under 100,000 cycle of erase/write.

12.7.2 Erase/write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20*	
10,000	10*	
100,000	5*	

*: At average + 85°C

12.8 WorkFlash Memory Write/Erase Characteristics

12.8.1 Write / Erase time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 85°C)

Parameter	Value		Unit	Remarks
	Typ*	Max*		
Sector erase time	0.3	1.5	s	Includes write time prior to internal erase
Half word (16-bit) write time	20	384	µs	Not including system-level overhead time
Chip erase time	1.2	6	s	Includes write time prior to internal erase

*: The typical value is immediately after shipment, the maximum value is guarantee value under 10,000 cycle of erase/write.

12.8.2 Erase/write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20*	
10,000	10*	

*: At average + 85°C

12.9 Return Time from Low-Power Consumption Mode

12.9.1 Return Factor: Interrupt

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

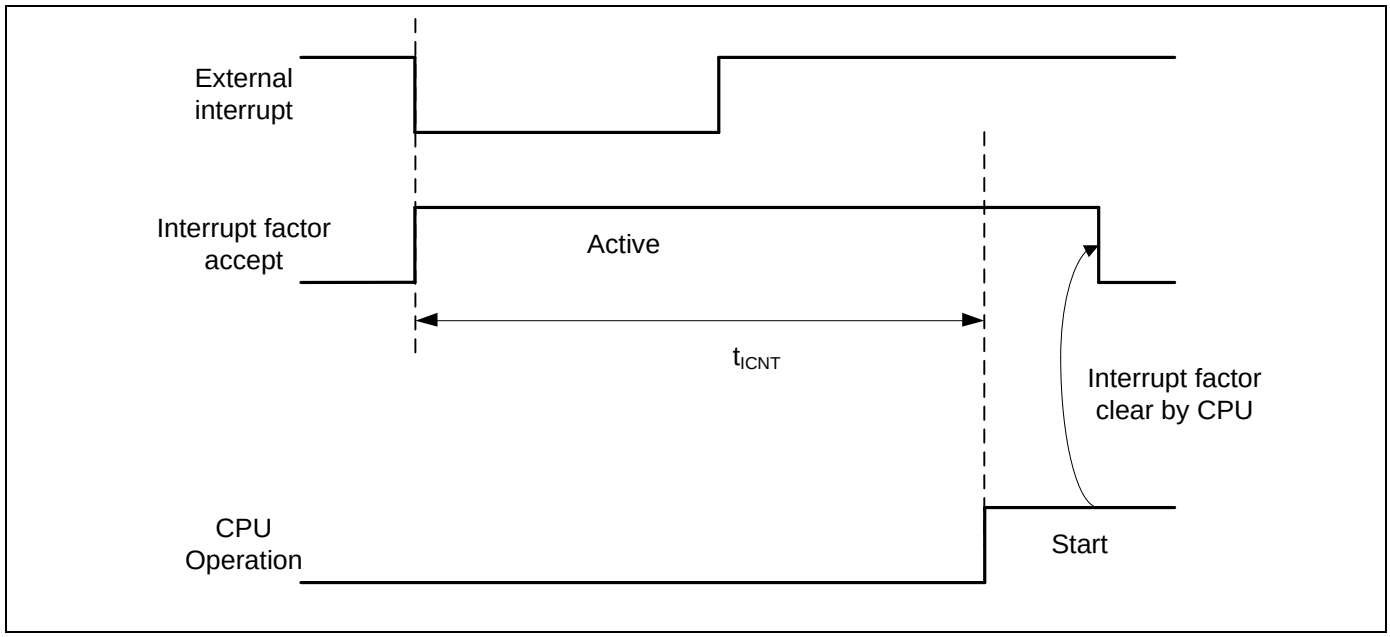
Return Count Time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 85°C

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{ICNT}	t_{CYCC}		ns	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		40	80	µs	
Low-speed CR Timer mode		453	737	µs	
Sub Timer mode		453	737	µs	
Stop mode		453	737	µs	

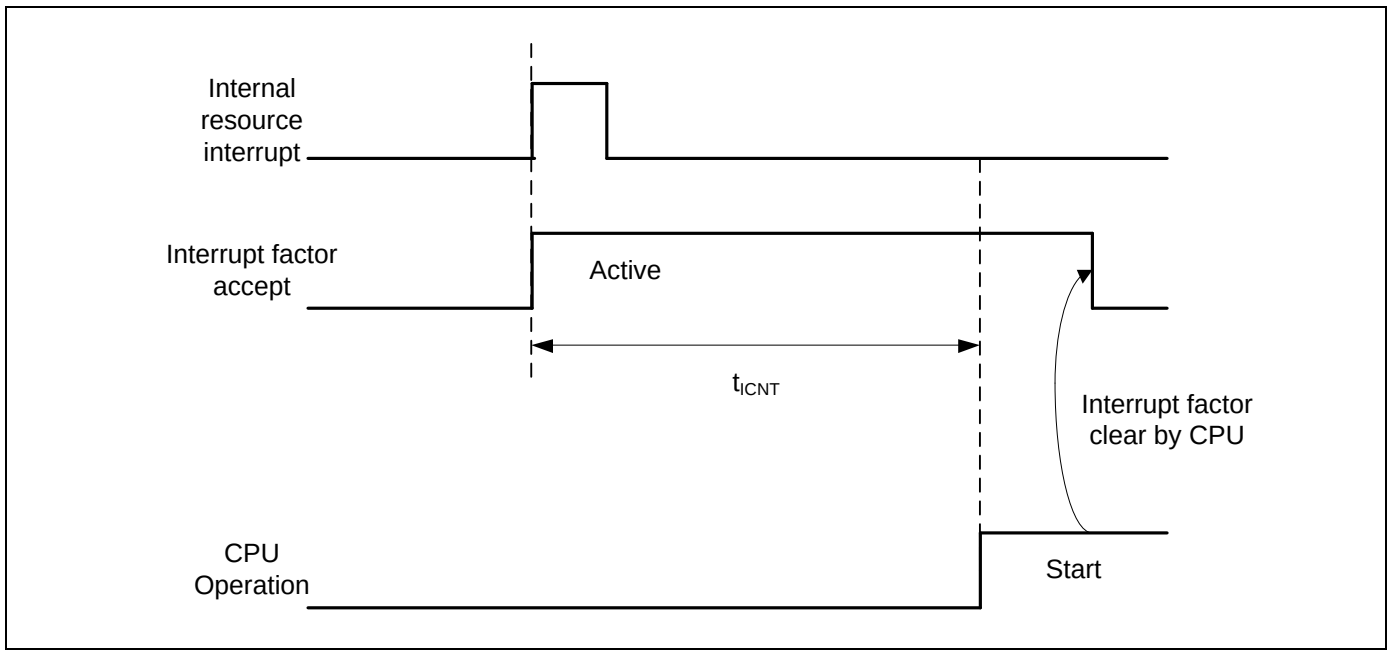
*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by external interrupt*)



*: External interrupt is set to detecting fall edge.

Operation example of return from Low-Power consumption mode (by internal resource interrupt*)



*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- *The return factor is different in each Low-Power consumption modes.*

  See "CHAPTER 6: Low Power Consumption Mode and Operations of Standby Modes" in "FM3 Family PERIPHERAL MANUAL" about the return factor from Low-Power consumption mode.

- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "CHAPTER 6: Low Power Consumption Mode" in "FM3 Family PERIPHERAL MANUAL".*

12.9.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

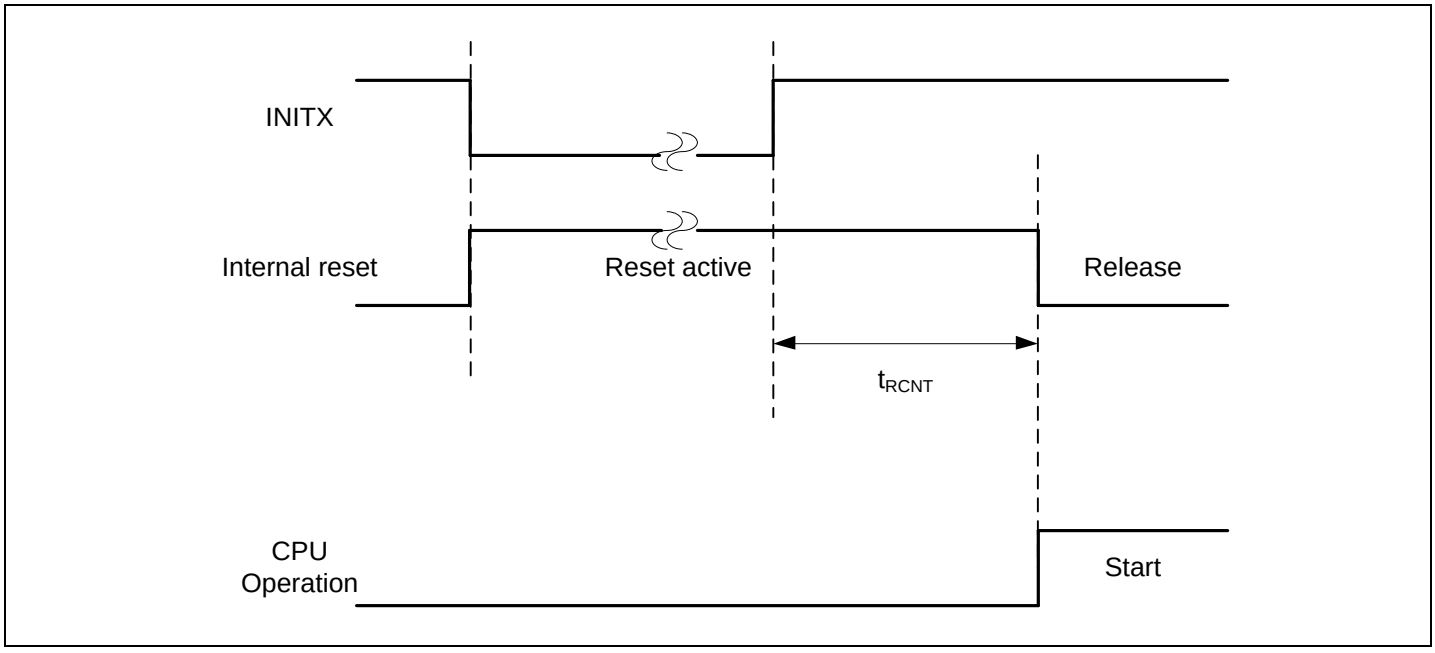
Return Count Time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 85°C)

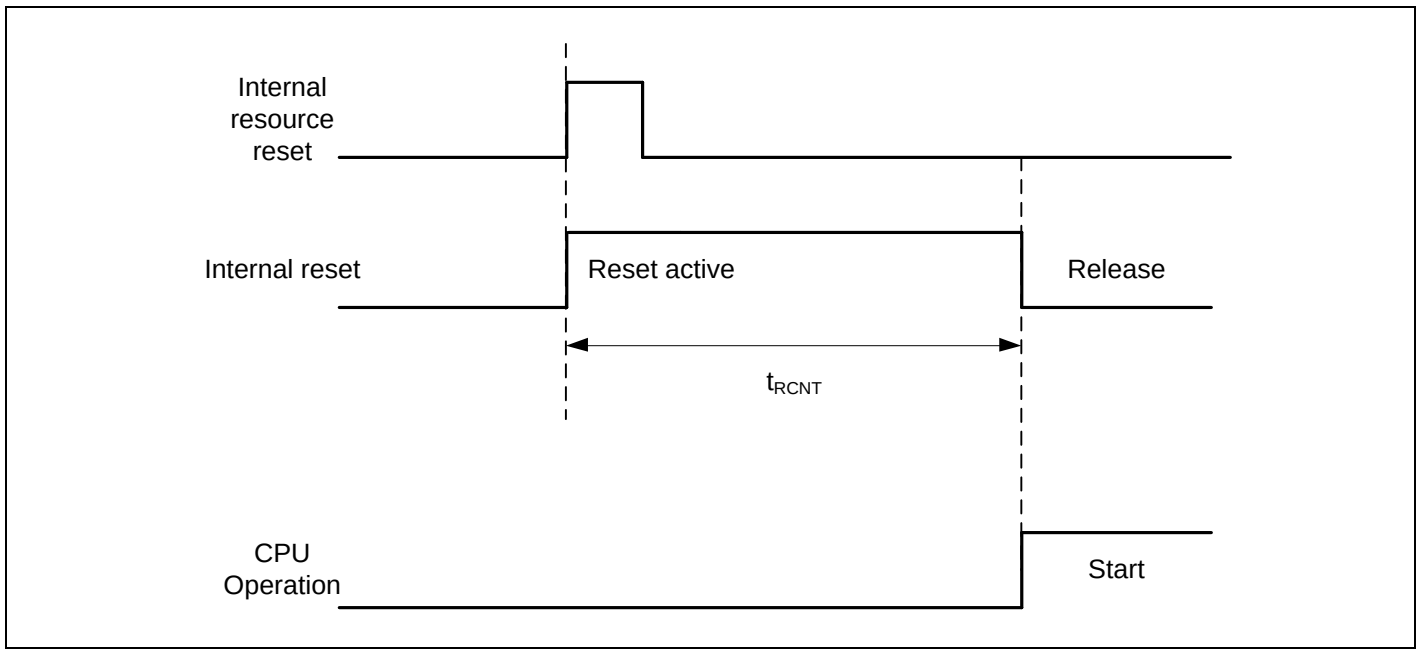
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{RCNT}	321	461	µs	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		321	461	µs	
Low-speed CR Timer mode		441	701	µs	
Sub Timer mode		441	701	µs	
Stop mode		441	701	µs	

*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by INITX)



Operation example of return from low power consumption mode (by internal resource reset*)



*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- *The return factor is different in each Low-Power consumption modes.*

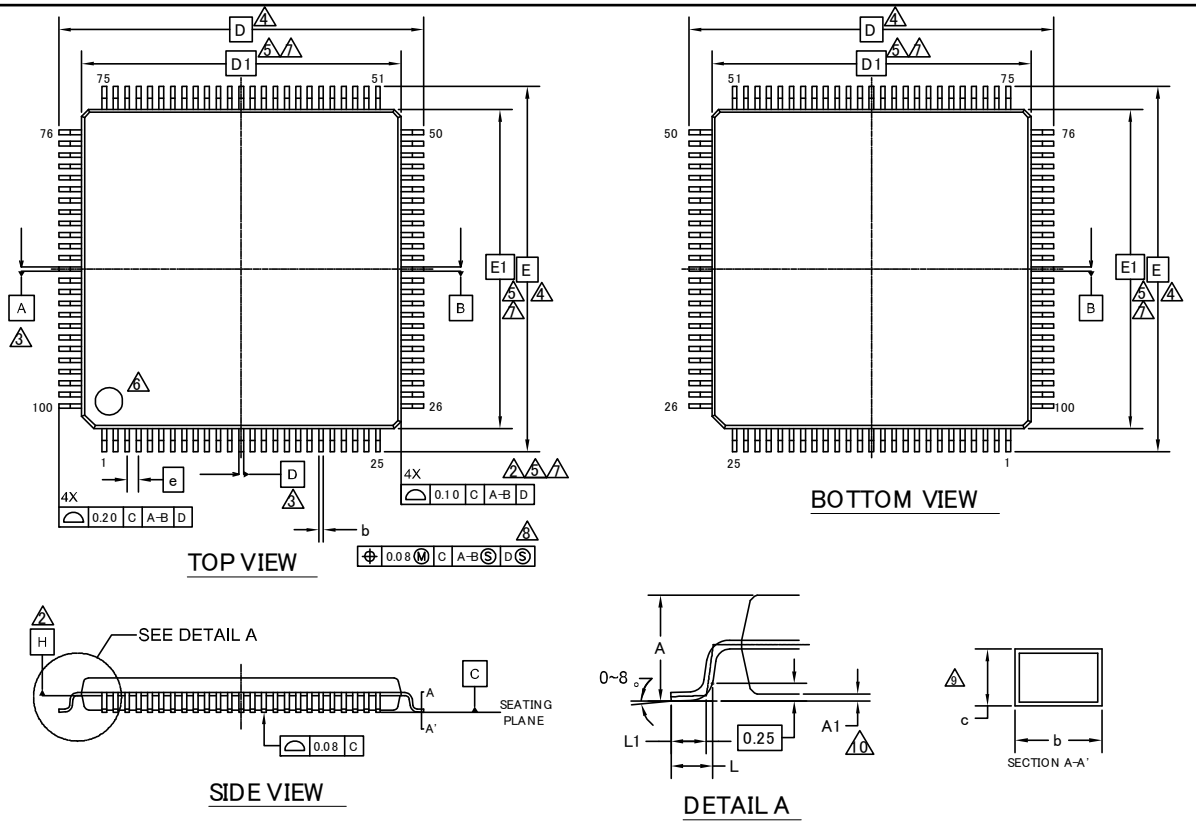
  See "CHAPTER 6: Low Power Consumption Mode and Operations of Standby Modes" in "FM3 Family PERIPHERAL MANUAL".
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "CHAPTER 6: Low Power Consumption Mode" in "FM3 Family PERIPHERAL MANUAL".*
- *The time during the power-on reset/low-voltage detection reset is excluded. See "(6) Power-on Reset Timing" in "4. AC Characteristics" in "12 Electrical Characteristics" for the detail on the time during the power-on reset/low -voltage detection reset.*
- *When in recovery from reset, CPU changes to the High-speed CR Run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the Main PLL clock stabilization wait time.*
- *The internal resource reset means the watchdog reset and the CSV reset.*

13. Ordering Information

Part number	On-chip Flash memory	On-chip SRAM	Package	Packing
CY9BF112NPQC-G-JNE2	Main: 128 Kbyte Work: 32 Kbyte	16 Kbyte	Plastic・QFP 100-pin (0.65 mm pitch), (PQH100)	Tray
CY9BF114NPQC-G-JNE2	Main: 256 Kbyte Work: 32 Kbyte	32 Kbyte		
CY9BF115NPQC-G-JNE2	Main: 384 Kbyte Work: 32 Kbyte	48 Kbyte		
CY9BF116NPQC-G-JNE2	Main: 512 Kbyte Work: 32 Kbyte	64 Kbyte		
CY9BF112NPMC-G-JNE2	Main: 128 Kbyte Work: 32 Kbyte	16 Kbyte	Plastic・LQFP 100-pin (0.5 mm pitch), (LQI100)	
CY9BF114NPMC-G-JNE2	Main: 256 Kbyte Work: 32 Kbyte	32 Kbyte		
CY9BF115NPMC-G-JNE2	Main: 384 Kbyte Work: 32 Kbyte	48 Kbyte		
CY9BF116NPMC-G-JNE2	Main: 512 Kbyte Work: 32 Kbyte	64 Kbyte		
CY9BF112RPMC-G-JNE2	Main: 128 Kbyte Work: 32 Kbyte	16 Kbyte	Plastic・LQFP 120-pin (0.5 mm pitch), (LQM120)	
CY9BF114RPMC-G-JNE2	Main: 256 Kbyte Work: 32 Kbyte	32 Kbyte		
CY9BF115RPMC-G-JNE2	Main: 384 Kbyte Work: 32 Kbyte	48 Kbyte		
CY9BF116RPMC-G-JNE2	Main: 512 Kbyte Work: 32 Kbyte	64 Kbyte		
CY9BF112NBGL-GE1	Main: 128 Kbyte Work: 32 Kbyte	16 Kbyte	Plastic・FBGA 112-pin (0.8 mm pitch), (LBC112)	
CY9BF114NBGL-GE1	Main: 256 Kbyte Work: 32 Kbyte	32 Kbyte		
CY9BF115NBGL-GE1	Main: 384 Kbyte Work: 32 Kbyte	48 Kbyte		
CY9BF116NBGL-GE1	Main: 512 Kbyte Work: 32 Kbyte	64 Kbyte		

14. Package Dimensions

Package Type	Package Code
LQFP 100	LQI100



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.15	—	0.27
c	0.09	—	0.20
D	16.00 BSC		
D1	14.00 BSC		
e	0.50 BSC		
E	16.00 BSC		
E1	14.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

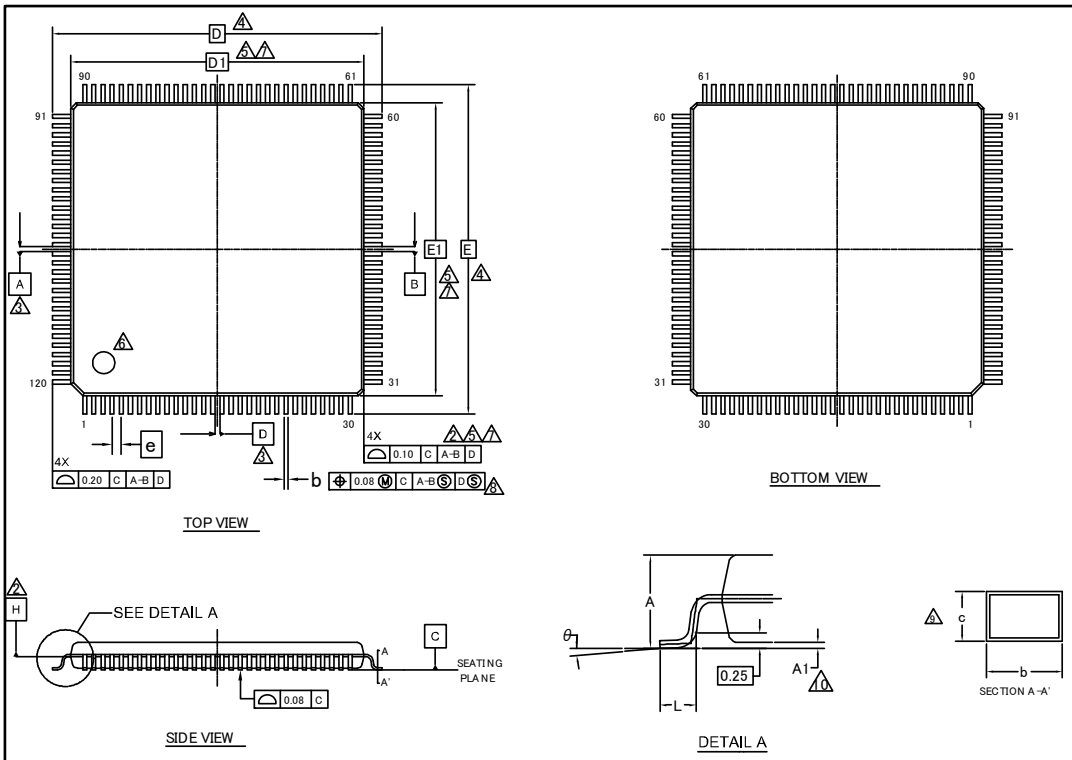
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 100 LEAD LQFP
14.0X14.0X1.7 MM LQI100 REV*A

002-11500 *A

Package Type	Package Code
LQFP 120	LQM120



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.115	—	0.195
D		18.00 BSC	
D1		16.00 BSC	
e		0.50 BSC	
E		18.00 BSC	
E1		16.00 BSC	
L	0.45	0.60	0.75
θ	0°	—	8°

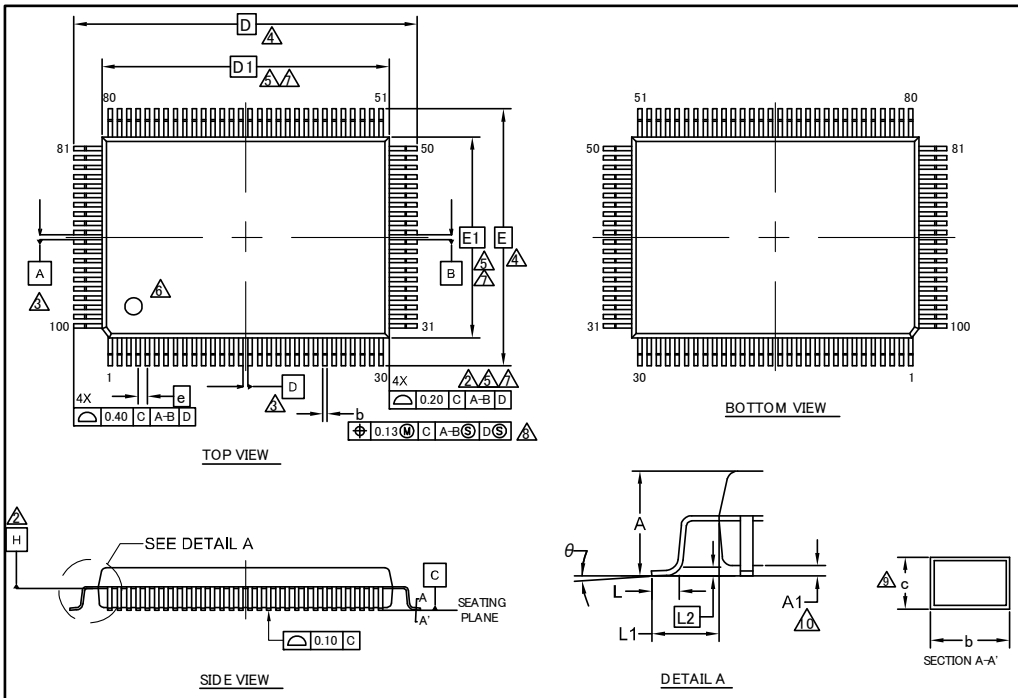
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
11. JEDEC SPECIFICATION NO. REF: N/A.

PACKAGE OUTLINE, 120 LEAD LQFP
18.0X18.0X1.7 MM LQM120 REV**

002-16172 **

Package Type	Package Code
QFP 100	PQH100



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	3.35
A1	0.05	—	0.45
b	0.27	0.32	0.37
c	0.11	—	0.23
D		23.90 BSC	
D1		20.00 BSC	
e		0.65 BSC	
E		17.90 BSC	
E1		14.00 BSC	
θ	0°	—	8°
L	0.73	0.88	1.03
L1		1.95 REF	
L2		0.25 BSC	

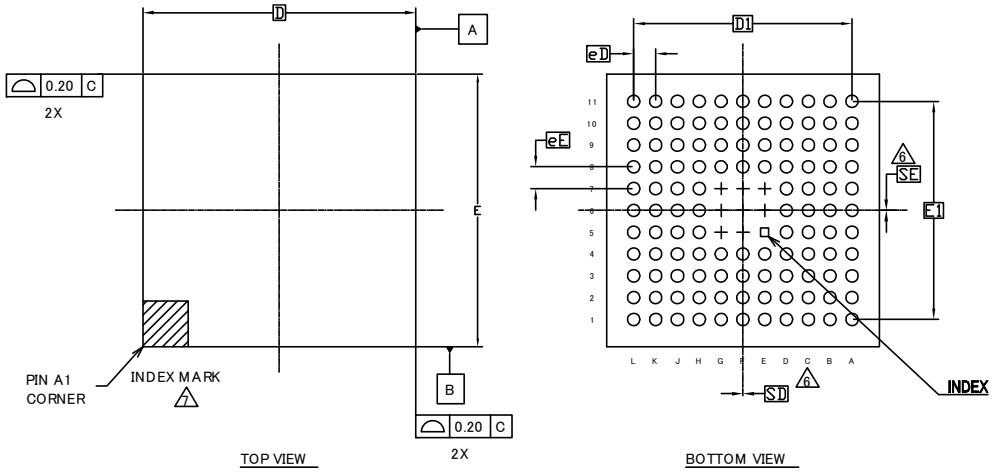
NOTES

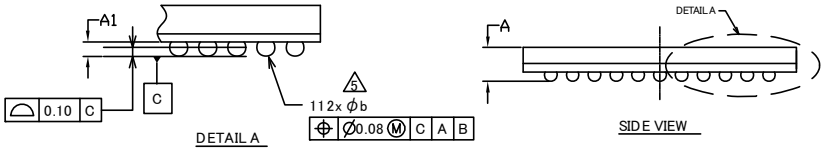
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 100 LEAD QFP
20.00X14.00X3.35 MM PQH100 REV**

002-15156 **

Package Type	Package Code
FBGA 112	LBC112





SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	–	–	1.45
A1	0.25	0.35	0.45
D		10.00 BSC	
E		10.00 BSC	
D1		8.00 BSC	
E1		8.00 BSC	
MD		11	
ME		11	
N		112	
Ø b	0.35	0.45	0.55
eD		0.80 BSC	
eE		0.80 BSC	
SD		0.00	
SE		0.00	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATIO N PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

PACKAGE OUTLINE, 112 BALL FBGA
10.00X10.00X1.45 MM LBC112 REV**

002-13225 **

15. Major Changes

Spansion Publication Number: DS706-00028

Page	Section	Change Results
Revision 2.0		
5	■ FEATURES ● External Interrupt Controller Unit	Corrected the external interrupt input pin.
101	■ ELECTRICAL CHARACTERISTICS 5. 12-bit A/D Converter ● Electrical Characteristics for the A/D Converter	Corrected the value of "Compare clock cycle". Max: 10000 → 2000
106	■ ORDERING INFORMATION	Corrected the part number.
Revision 2.1		
-	-	Company name and layout design change
Revision 3.0		
2	■Features ●External Bus Interface	Added the description of Maximum area size
9	■Packages	Deleted the description of ES
27, 28	■List of Pin Functions · List of pin numbers	Modified I/O circuit type of P63 to P68
47, 49	■I/O Circuit Type	Added the description of I2C to the type of E, F and I
47, 48	■I/O Circuit Type	Added about +B input
54	■Handling Devices	Added "□Stabilizing power supply voltage"
54	■Handling Devices ●Crystal oscillator circuit	Added the following description "Evaluate oscillation of your using crystal oscillator by your mount board."
55	■Handling Devices ●C Pin	Changed the description
56	■Block Diagram	Modified the block diagram
57	■Memory Map · Memory map(1)	Modified the area of "External Device Area"
58, 59	■Memory Map · Memory map(2)(3)	Added the summary of Flash memory sector and the note
66, 67	■Electrical Characteristics 1. Absolute Maximum Ratings	· Added the Clamp maximum current · Added the output current of P80 and P81 · Added about +B input
68	■Electrical Characteristics 2. Recommended Operation Conditions	· Modified the minimum value of Analog reference voltage · Added Smoothing capacitor · Added the note about less than the minimum power supply voltage
69, 70	■Electrical Characteristics 3. DC Characteristics (1) Current rating	· Changed the table format · Added Main TIMER mode current · Added Flash Memory Current · Moved A/D Converter Current · Modified the unit of low voltage detection circuit (LVD) power supply current
73	■Electrical Characteristics 4. AC Characteristics (1) Main Clock Input Characteristics	Added Master clock at Internal operating clock frequency
74	■Electrical Characteristics 4. AC Characteristics (3) Built-in CR Oscillation Characteristics	Added Frequency stability time at Built-in high-speed CR

Page	Section	Change Results
75	■Electrical Characteristics 4. AC Characteristics (4-1) Operating Conditions of Main PLL (4-2) Operating Conditions of Main PLL	· Added Main PLL clock frequency · Added the figure of Main PLL connection
76	■Electrical Characteristics 4. AC Characteristics (6) Power-on Reset Timing	· Added Time until releasing Power-on reset · Changed the figure of timing
78-80	■Electrical Characteristics 4. AC Characteristics (7) External Bus Timing	Modified Data output time
88-95	■Electrical Characteristics 4. AC Characteristics (8) CSIO/UART Timing	· Modified from UART Timing to CSIO/UART Timing · Changed from Internal shift clock operation to Master mode · Changed from External shift clock operation to Slave mode
102	■Electrical Characteristics 5. 12bit A/D Converter	· Added the typical value of Integral Nonlinearity, Differential Nonlinearity, Zero transition voltage and Full-scale transition voltage · Modified Stage transition time to operation permission · Modified the minimum value of Reference voltage
105	■Electrical Characteristics 7. Low-voltage Detection Characteristics (2) Interrupt of Low-voltage Detection	Modified LVD stabilization wait time
106	■Electrical Characteristics 8. WorkFlash Memory Write/Erase Characteristics (1) Write / Erase time	· Modified sector erase time · Modified half word(16-bit) write time
107-110	■Electrical Characteristics 9. Return Time from Low-Power Consumption Mode	Added Return Time from Low-Power Consumption Mode
111	■Ordering Information	Change to full part number
112-115	■Package Dimensions	Deleted FPT-100P-M20 and FPT-120P-M21

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: CY9B110R Series 32-bit Arm® Cortex®-M3 FM3 Microcontroller
Document Number: 002-05622

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	TOYO	03/13/2015	Migrated to Cypress and assigned document number 002-05622. No change to document contents.
*A	5175344	TOYO	03/17/2016	Changed package code as below. FPT-100P-M23 to LQI100-02 FPT-120P-M37 to LQM120-02 FPT-100P-M36 to PQH100 BGA-112P-M04 to LBC112. P.19 - Modified I/O circuit type of MD0. P.43 - Added the note of JTAG pins. P.56 - Modified X1A of block diagram. P.75 - Modified max value of PLL macro oscillation clock frequency to 144 MHz. P.111-114 - Changed package Dimensions.
*B	5314949	TOYO	06/21/2016	P.110 - Modified part number.
*C	5666809	YSKA	03/21/2017	“Modified RTC description in “Features, Real-Time Clock(RTC)” Changed starting count value from 01 to 00. Deleted “second, or day of the week” in the Interrupt function (Page 2). Updated “12.4.7 Power-On Reset Timing”: Changed parameter from “Power Supply rising time(t_{VCCR})[ms]” to “Power ramp rate(dV/dt)[mV/us]” and added some comments (Page 75). Updated Package code as follows (Page 8-12, 67, 109) LQI100-02 -> LQI100, LQM120-02 -> LQM120. Updated “14. Package dimensions” (Page 110-113). Modified typo in “13. Ordering Information” (Page 109). Added the Baud rate spec in “12.4.10 CSIO/UART Timing” (Page 86, 88, 90, 92).
*D	6064714	HUAL	02/09/2018	Updated to new template. Completing Sunset Review.
*E	6517762	HUAL	05/07/2019	Updated Document Title to read as “CY9B110R Series 32-bit Arm® Cortex®-M3 FM3 Microcontroller”. Replaced “MB9B110R Series” with “CY9B110R Series” in all instances across the document. Updated Ordering Information: Updated part numbers. Updated to new template.

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