



**THE DATASHEET OF  
BD18347EFV-ME2**



# For Automotive, 40 V 150 mA 4ch Constant Current LED Driver

**BD18337EFV-M BD18347EFV-M**

## General Description

BD18337EFV-M / BD18347EFV-M are 40 V-withstanding constant current LED driver for automotive applications. It is a 4 channel LED driver with the built-in energy sharing control which can realize to make the board size small. High reliability can be realized with LED Open Detection, the OUTx (all later x=1 to 4) pin Short Circuit Protection, Over Voltage Mute and Thermal Shutdown Function. In case the output OUTx pin has 3 LEDs in series, BD18337EFV-M has to be used, in case of 2 LEDs in series, BD18347EFV-M has to be used.

## Key Specifications

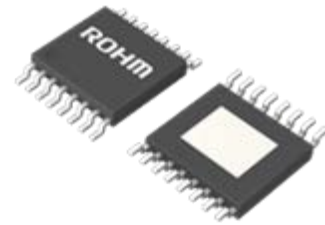
- Input Voltage Range: 5.5 V to 20.0 V
- Maximum Output Current: 150 mA/ch
- Output Current Accuracy:  $\pm 5\%$
- Relative Channel Accuracy:  $\pm 5\%$
- Operating Temperature Range:  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

## Package

HTSSOP-B16

**W (Typ) x D (Typ) x H (Max)**

5.00 mm x 6.40 mm x 1.00 mm



## Features

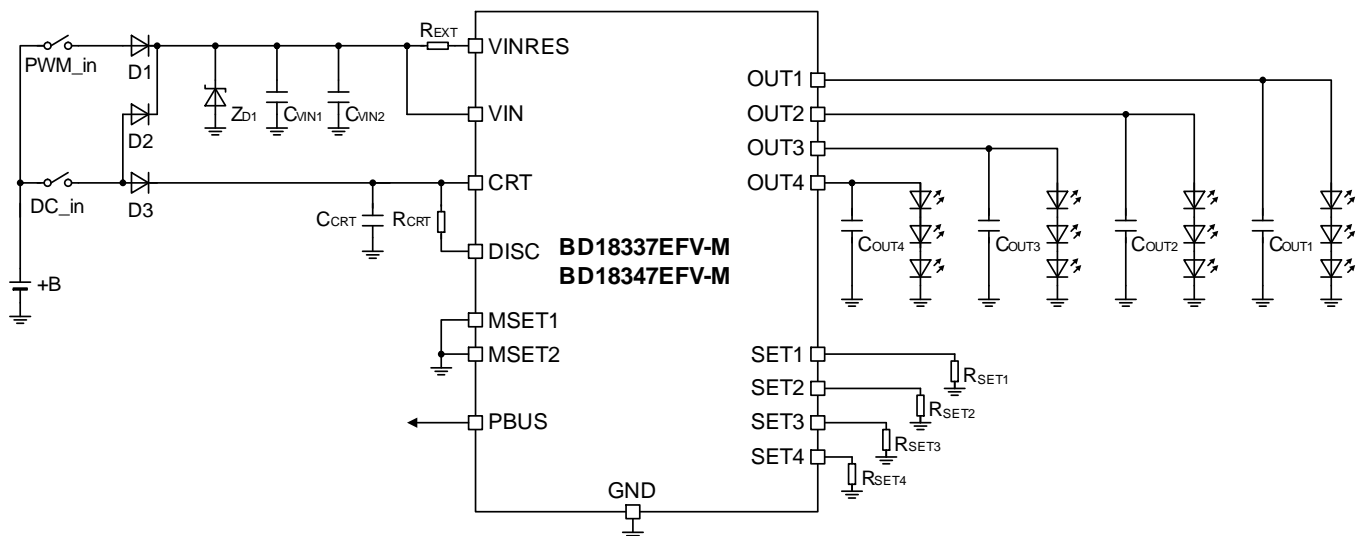
- AEC-Q100 Qualified<sup>(Note 1)</sup>
- Energy Sharing Control
- PWM Dimming Function
- License Lamp Mode
- LED Open Detection
- OUTx pin Short Circuit Protection (SCP)
- Over Voltage Mute Function (OVM)
- Disable LED Open Detection Function at Reduced-Voltage
- LED Failure Input / Output Functions (PBUS)

(Note 1) Grade1

## Applications

- Automotive LED Exterior Lamp (Rear Lamp, License Lamp, DRL / Position Lamp, Fog Lamp etc.)
- Automotive LED Interior Lamp (Air Conditioner Lamp, Interior Lamp, Cluster Light etc.)

## Typical Application Circuit



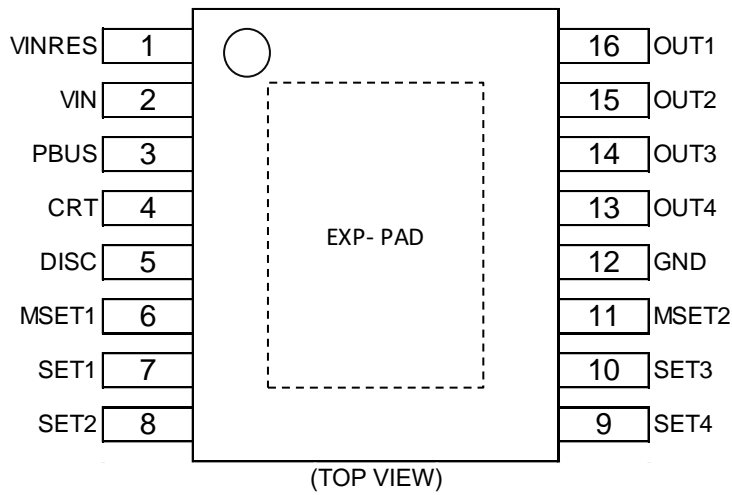
○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays

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TSZ22111 • 14 • 001

Pin Configuration



Pin Description

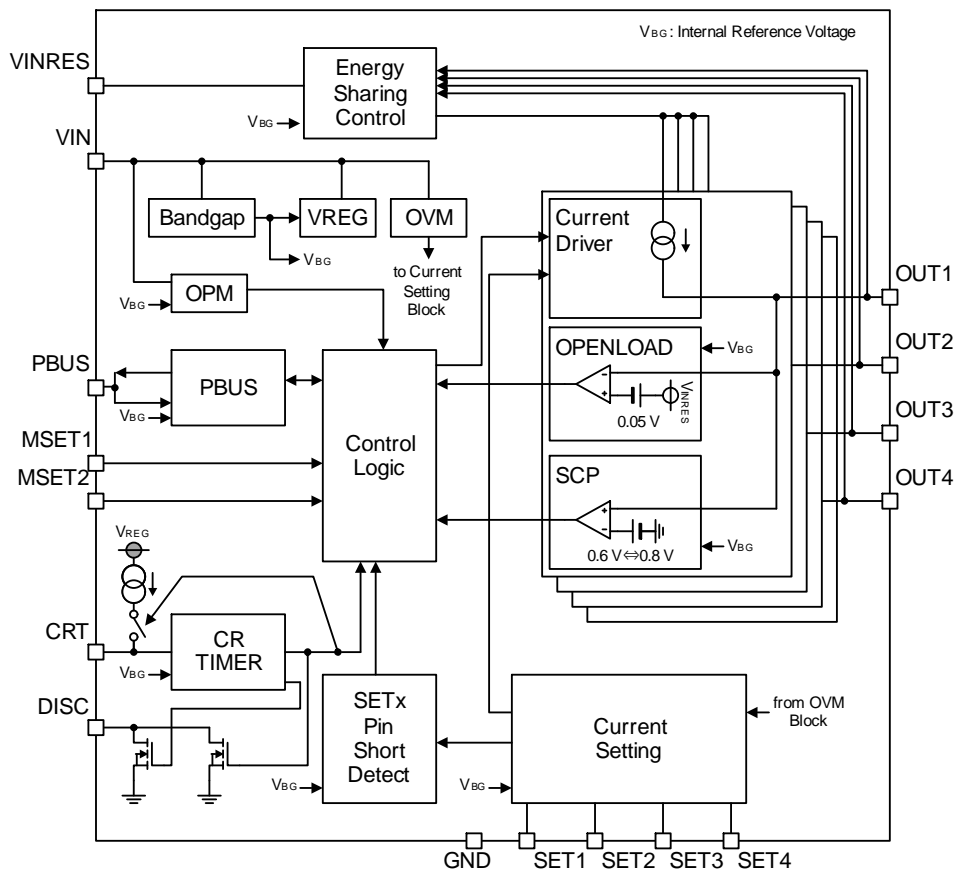
Pin No.	Pin Name	Function
1	VINRES	Energy sharing external resistor connection <sup>(Note 1)</sup>
2	VIN	Supply voltage input
3	PBUS	Output for fault flag / Input to disable output current
4	CRT	CR TIMER setting <sup>1</sup> <sup>(Note 2)</sup>
5	DISC	CR TIMER setting <sup>2</sup> <sup>(Note 3)</sup>
6	MSET1	Mode setting pin 1
7	SET1	Output current setting pin 1
8	SET2	Output current setting pin 2
9	SET4	Output current setting pin 4
10	SET3	Output current setting pin 3
11	MSET2	Mode setting pin 2
12	GND	GND
13	OUT4	Current output pin 4
14	OUT3	Current output pin 3
15	OUT2	Current output pin 2
16	OUT1	Current output pin 1
-	EXP-PAD	The EXP-PAD connect to GND.

<sup>(Note 1)</sup> Short the VINRES pin to the VIN pin when not in use.

<sup>(Note 2)</sup> Short the CRT pin to the VIN pin when not in use.

<sup>(Note 3)</sup> Open the DISC pin or connect it to GND when not in use.

Block Diagram



**Absolute Maximum Ratings (Ta=25 °C)**

Parameter	Symbol	Rating	Unit
Supply Voltage (VIN)	V <sub>IN</sub>	-0.3 to +40.0	V
Supply Voltage (VINRES)	V <sub>VINRES</sub>	-0.3 to +40.0 < V <sub>IN</sub>	V
VIN to VINRES Pin Voltage	V <sub>VIN_VINRES</sub>	-0.3 to +10.0	V
CRT, DISC Pin Voltage	V <sub>CRT</sub> , V <sub>DISC</sub>	-0.3 to +40.0	V
MSET1, MSET2 Pin Voltage	V <sub>MSET1</sub> , V <sub>MSET2</sub>	-0.3 to +20.0	V
OUT1,OUT2,OUT3,OUT4 Pin Voltage	V <sub>OUT1</sub> , V <sub>OUT2</sub> , V <sub>OUT3</sub> , V <sub>OUT4</sub>	-0.3 to V <sub>IN</sub> +0.3V	V
PBUS Pin Voltage	V <sub>PBUS</sub>	-0.3 to +20.0	V
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C
Maximum Junction Temperature	T <sub>jmax</sub>	150	°C

**Caution 1:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Caution 2:** Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

**Thermal Resistance**(Note 1)

Parameter	Symbol	Thermal Resistance(Typ)		Unit
		1s <sup>(Note 3)</sup>	2s2p <sup>(Note 4)</sup>	
HTSSOP-B16				
Junction to Ambient	θ <sub>JA</sub>	113	36	°C/W
Junction to Top Characterization Parameter <sup>(Note 2)</sup>	Ψ <sub>JT</sub>	13	9	°C/W

(Note 1) Based on JESD51-2A(Still-Air), using a BD18347EFV-M Chip.

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size	Thermal Via <sup>(Note 5)</sup>	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

(Note 5) This thermal via connects with the copper pattern of all layers.

**Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (VIN) <sup>(Note 1)</sup>	V <sub>IN</sub>	5.5	13.0	20.0	V
Output Current (each channel)	I <sub>OUTx</sub>	-	-	150	mA
CR Timer Frequency	f <sub>PWM</sub>	-	-	750	Hz
PWM Minimum Pulse Width	t <sub>MIN</sub>	100	-	-	μs
Operating Temperature	T <sub>opr</sub>	-40	-	+125	°C

(Note 1) ASO should not be exceeded.

**Operating Conditions**

Parameter	Symbol	Min	Max	Unit
Capacitor Connecting VIN Pin 1	C <sub>VIN1</sub> <sup>(Note 2)</sup>	1.0	-	μF
Capacitor Connecting VIN Pin 2	C <sub>VIN2</sub> <sup>(Note 2)</sup>	0.047	-	μF
Capacitor Connecting LED Anode	C <sub>OUT1</sub> , C <sub>OUT2</sub> , C <sub>OUT3</sub> , C <sub>OUT4</sub> <sup>(Note 2)</sup>	0.01	0.47	μF
Capacitor for Setting CR Timer	C <sub>CRT</sub> <sup>(Note 2)</sup>	0.01	0.22	μF
Resistor for Setting CR Timer	R <sub>CRT</sub>	0.1	50	kΩ
Resistor for Setting Output Current	R <sub>SET1</sub> , R <sub>SET2</sub> , R <sub>SET3</sub> , R <sub>SET4</sub>	12	36	kΩ

(Note 2) Recommended ceramic capacitor.

**Electrical Characteristics** (Unless otherwise specified, Ta=-40 °C to +125 °C, V<sub>IN</sub>=13 V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
<b>[Circuit Current I<sub>VIN</sub>]</b>						
Circuit Current in Normal Mode	I <sub>VIN1</sub>	-	3.0	7.0	mA	
Circuit Current when LED Open is Detected	I <sub>VIN2</sub>	-	3.0	7.0	mA	at LED Open Detection
Circuit Current when PBUS is Low	I <sub>VIN3</sub>	-	3.0	7.0	mA	V <sub>PBUS</sub> =0 V
<b>[Output Current I<sub>OUTx</sub>]</b>						
OUTx OFF Current	I <sub>OUTx_OFF</sub>	-	-	1	μA	V <sub>OUTx</sub> =2 V, V <sub>CRT</sub> =0 V, Ta=25 °C
VINRES-OUTx Pin Drop Voltage	V <sub>DR</sub>	-	-	1.0	V	I <sub>OUTx</sub> =100 mA
LED Open Detection Output Current	I <sub>OUTx_OPEN</sub>	-	-	10	mA	V <sub>OUTx</sub> =V <sub>VINRES</sub> -100 mV
<b>[Energy Sharing Control]</b>						
Energy Sharing Control Voltage	V <sub>ES</sub>	1.3	2.0	3.0	V	V <sub>VINRES</sub> -V <sub>OUTx_MAX</sub> , V <sub>VIN</sub> =13 V, V <sub>OUTx</sub> =9 V
ON Resistance Between the VIN Pin and the VINRES Pin	R <sub>VIN_VINRES</sub>	-	0.5	1.0	Ω	I <sub>VIN</sub> =100 mA
<b>[LED Open Detection]</b>						
OUTx Pin LED Open Detection Voltage	V <sub>OPD</sub>	20	50	100	mV	V <sub>VINRES</sub> -V <sub>OUTx</sub>
<b>[Disable LED Open Detection Function at Reduced-Voltage]</b>						
VIN Pin Voltage	V <sub>VIN_OPM</sub>	10.5	11.0	11.5	V	BD18337EFV-M
VIN Pin Voltage	V <sub>VIN_OPM</sub>	7.30	7.65	8.00	V	BD18347EFV-M
<b>[OUTx pin Short Circuit Protection (SCP)]</b>						
OUTx Pin Short Circuit Current	I <sub>OUTx_SCP</sub>	0.1	0.3	1.0	mA	V <sub>OUTx</sub> =0.9 V
OUTx Pin Short Circuit Protection Voltage	V <sub>SCP</sub>	0.5	0.6	0.7	V	
OUTx Pin Short Circuit Protection Release Voltage	V <sub>SCPR</sub>	0.7	0.8	0.9	V	
SCP Detect Delay Time 1	t <sub>SCPD1</sub>	10	60	150	μs	Refer to <a href="#">Figure 17</a>
SCP Detect Delay Time 2	t <sub>SCPD2</sub>	-	20	-	μs	Refer to <a href="#">Figure 17</a>
SCP Release Delay Time	t <sub>SCPR</sub>	-	40	-	μs	Refer to <a href="#">Figure 17</a>
SCP Protection Disable Time at Power On	t <sub>SCPPON</sub>	-	140	-	μs	Refer to <a href="#">Figure 17</a>
<b>[Output Current Setting]</b>						
Output Current Setting Coefficient	K <sub>SET</sub>	1710	1800	1890	-	R <sub>SETx</sub> =12 kΩ to 18 kΩ, I <sub>OUTx</sub> =K <sub>SET</sub> / R <sub>SETx</sub> [A]
		1620	1800	1980	-	R <sub>SETx</sub> =18 kΩ to 36 kΩ, I <sub>OUTx</sub> =K <sub>SET</sub> / R <sub>SETx</sub> [A]
SETx Pin Voltage	V <sub>SETx</sub>	1.08	1.20	1.32	V	
SETx Pin Short Detection Resistance	R <sub>SETx_SHORT</sub>	1.0	2.4	5.0	kΩ	

## Electrical Characteristics – continued (Unless otherwise specified, Ta=-40 °C to +125 °C, VIN=13 V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
<b>[CR TIMER]</b>						
CRT Pin Charge Current	ICRT	36	40	44	μA	
CRT Pin Charge Voltage	VCRT_CHA	0.72	0.80	0.88	V	
CRT Pin Discharge Voltage 1	VCRT_DIS1	1.80	2.00	2.20	V	
CRT Pin Discharge Voltage 2	VCRT_DIS2	2.10	2.40	3.00	V	VCRT > VCRT_DIS2 RDISC1 → RDISC2
CRT Pin Charge Resistance	RCHA	28.5	30.0	31.5	kΩ	
CRT Discharge Constant	VCRT_CHA / VCRT_DIS1	0.38	0.4	0.42	V / V	
DISC Pin ON Resistance 1	RDISC1	20	50	100	Ω	IDISC=10 mA
DISC Pin ON Resistance 2	RDISC2	2.5	5	10	kΩ	IDISC=100 μA
CRT Pin Leakage Current	ICRT_LEAK	-	-	10	μA	VCRT=VIN
<b>[Over Voltage Mute Function (OVM)]</b>						
Over Voltage Mute Start Voltage	VOVMS	20.0	22.0	24.0	V	$\Delta I_{OUTx} = -3\%$ $\Delta I_{OUTx} = \frac{I_{OUTx} (@V_{IN}=V_{OVM})}{I_{OUTx} (@V_{IN}=13V)} - 1$
Over Voltage Mute Gain	IOVMG	-	-20	-	%/V	$\Delta I_{OUTx} / \Delta V_{IN}$
<b>[PBUS]</b>						
Input High Voltage	VPBUSH	2.4	-	-	V	
Input Low Voltage	VPBUSL	-	-	0.6	V	
PBUS Pin Source Current	IPBUS	75	150	300	μA	
PBUS Pin Output Low Voltage	VPBUS_OL	-	-	0.6	V	Source 3 mA to the PBUS pin
PBUS Pin Output High Voltage	VPBUS_OH	3.5	4.5	5.5	V	Sink 10 μA from the PBUS pin
PBUS Pin Leakage Current	IPBUS_LEAK	-	-	10	μA	VPBUS=7 V
<b>[UVLO VIN]</b>						
UVLO VIN Detection Voltage	VUVLO_VIND	4.50	4.75	5.00	V	VIN: Sweep down
UVLO VIN Release Voltage	VUVLO_VINR	5.00	5.25	5.50	V	VIN: Sweep up
<b>[UVLO VINRES]</b>						
UVLO VINRES Detection Voltage	VUVLO_VINRESD	4.25	4.50	4.75	V	VINRES: Sweep down
UVLO VINRES Release Voltage	VUVLO_VINRESR	4.75	5.00	5.25	V	VINRES: Sweep up
<b>[MSET1, MSET2]</b>						
MSET1, MSET2 Input H Voltage	VMSETH	2.4	-	-	V	
MSET1, MSET2 Input L Voltage	VMSETL	-	-	0.6	V	
MSET1, MSET2 Pin Outflow Current	IMSET	25	50	100	μA	VMSET1=0 V, VMSET2=0 V

**Typical Performance Curves (Reference Data)**  
 (Unless otherwise specified,  $T_a=25\text{ }^\circ\text{C}$ ,  $V_{IN}=13\text{ V}$ )

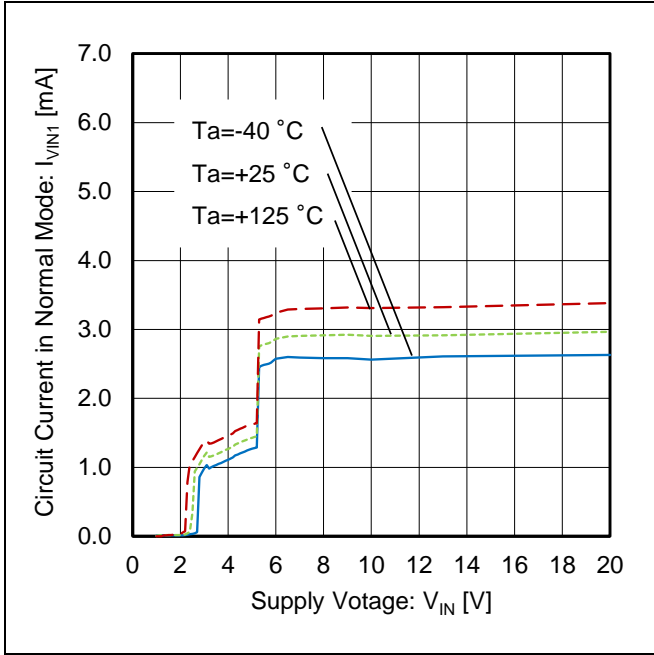


Figure 1. Circuit Current in Normal Mode vs Supply Voltage

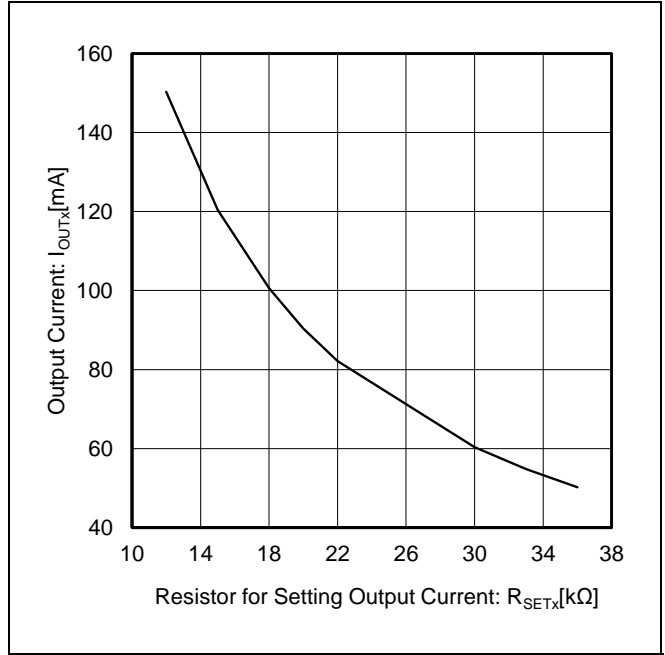


Figure 2. Output Current vs Resistor for Setting Output Current

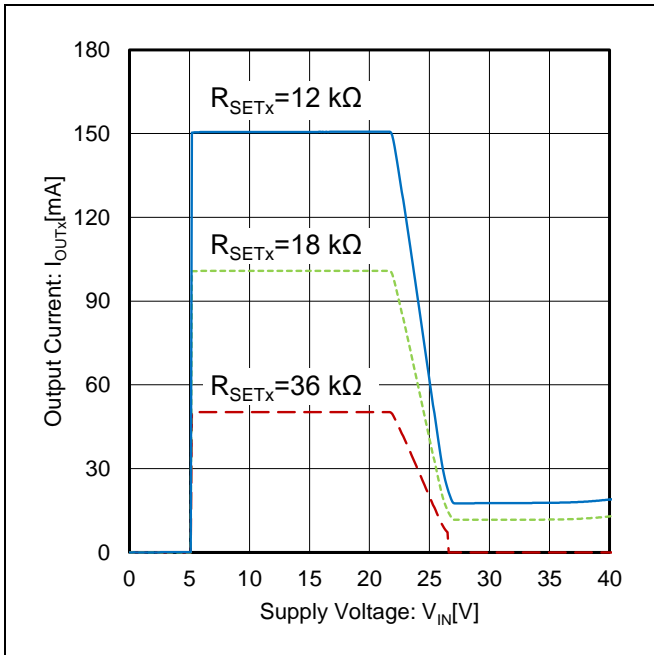


Figure 3. Output Current vs Supply Voltage

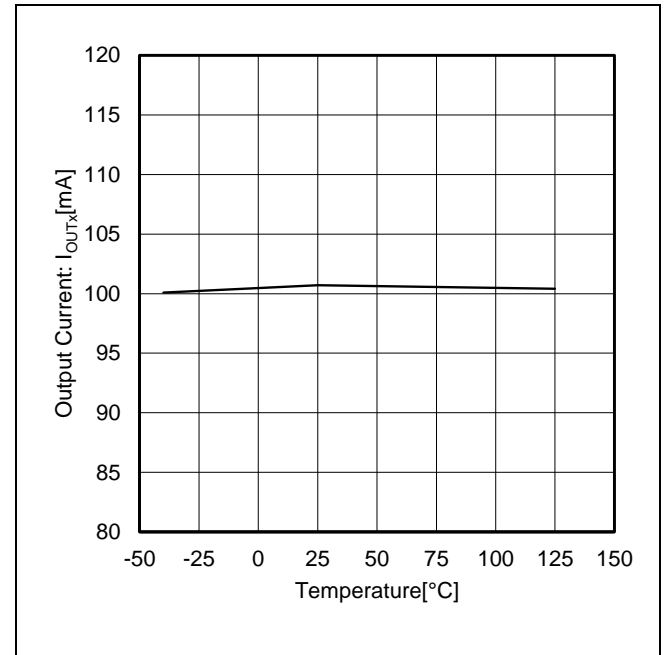


Figure 4. Output Current vs Temperature

Typical Performance Curves (Reference Data) – continued

(Unless otherwise specified,  $T_a=25\text{ }^\circ\text{C}$ ,  $V_{IN}=13\text{ V}$ )

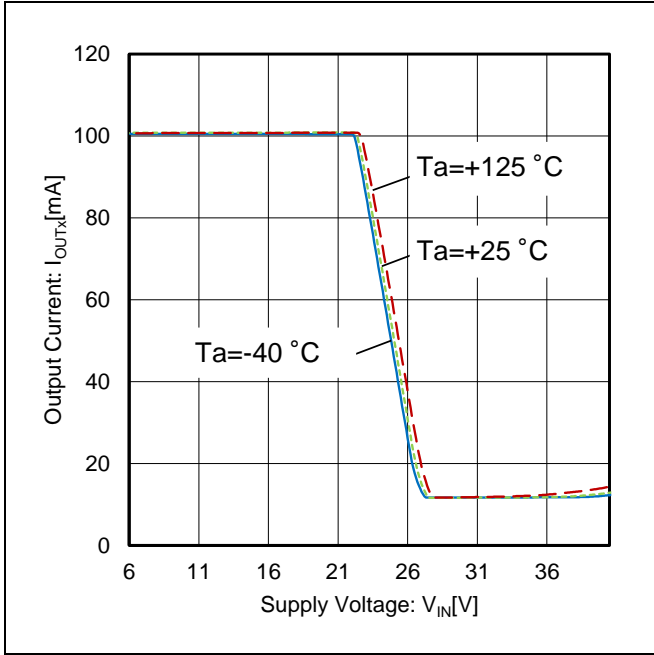


Figure 5. Output Current vs Supply Voltage

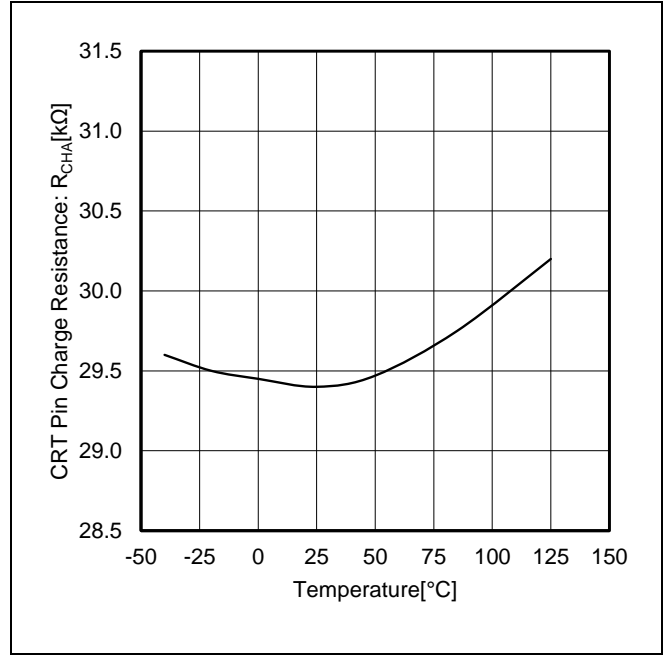


Figure 6. CRT Pin Charge Resistance vs Temperature

**Description of Function**

(Unless otherwise specified, Ta=25 °C, VIN=13 V)

**1. Output Current Setting and Power Control**

Output current IOUTx can be set by the value of the output current setting resistor RSETx.

$$I_{OUTx} = \frac{K_{SET}}{R_{SETx}} \quad [A]$$

where:

KSET is the output current setting coefficient 1800 (Typ).

RSETx is the output current setting resistor.

When not to use the OUTx pin, open the SETx pin.

**•Required VIN for set current to flow**

Output Current IOUTx and minimum VIN should be set to satisfy the following relationship.

$$V_{IN} \geq V_{f\_LED} \times N + V_{DR} + R_{VIN\_VINRES} \times I_{OUTx\_TOTAL} \quad [V]$$

where:

VIN is the VIN pin voltage.

Vf\_LED is the LED forward voltage.

N is the number of LED.

VDR is the VINRES - OUTx drop voltage.

RVIN\_VINRES is the ON resistance between the VIN pin and the VINRES pin.

IOUTx\_TOTAL is the total output current.

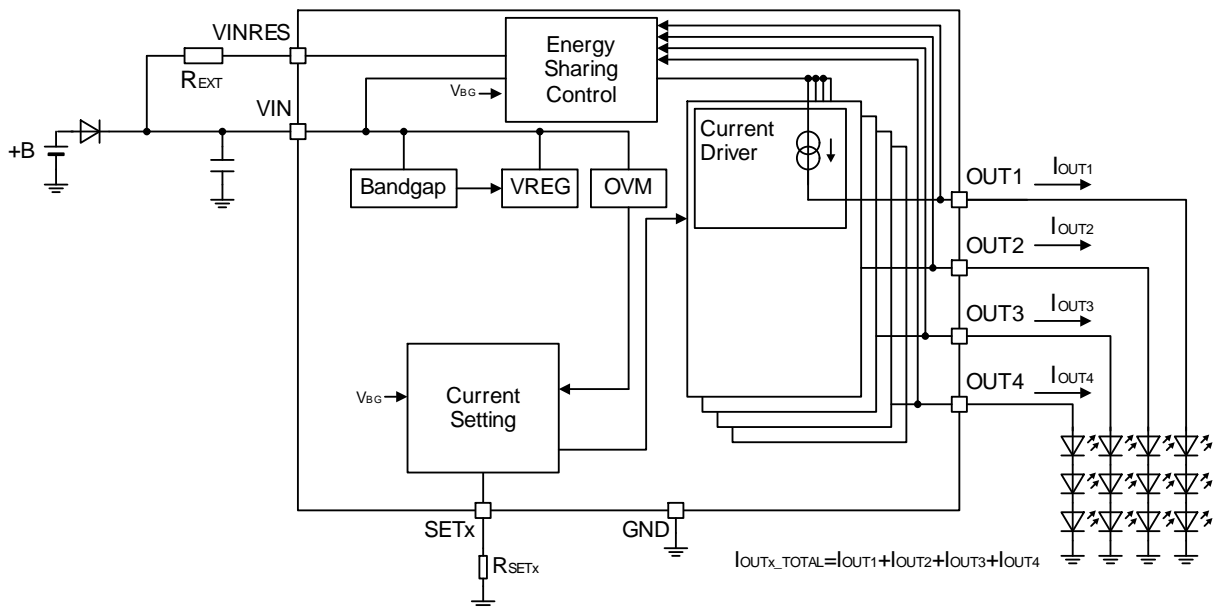


Figure 7. Output Current Setting

Description of Function – continued

2. Energy Sharing Control

Energy sharing is performed by connecting external resistor  $R_{EXT}$  between the VIN and VINRES pins. It makes possible to distribute the heat generated by the IC to  $R_{EXT}$ . (When not in use, short the VINRES pin with the VIN pin.)

The IC controls the difference voltage to  $V_{ES}$  (2.0 V(Typ)) which is between the VINRES pin and the pin that has maximum voltage among OUT1 to OUT4 pins.

Insert resistor in the anode of the LED, when the following expression is not satisfied.

$$V_{UVLO\_VINRESR} \leq V_{OUTx\_MAX}$$

$$V_{OUTx} = I_{OUTx} \times R_{OUTx} + V_{f\_LED} \times N$$

where:

- $V_{UVLO\_VINRESR}$  is the VINRES pin UVLO release voltage, 5.00 V (Typ).
- $V_{OUTx\_MAX}$  is the maximum voltage among the OUT1 to OUT4 pins
- $V_{ES}$  is the Energy Sharing control voltage, 2.0 V (Typ).
- $V_{OUTx}$  is the OUTx pin voltage.
- $I_{OUTx}$  is the OUTx pin current.
- $R_{OUTx}$  is the resistor inserted in the anode of LED.
- $V_{f\_LED}$  is the LED forward voltage.
- $N$  is the number of LED.

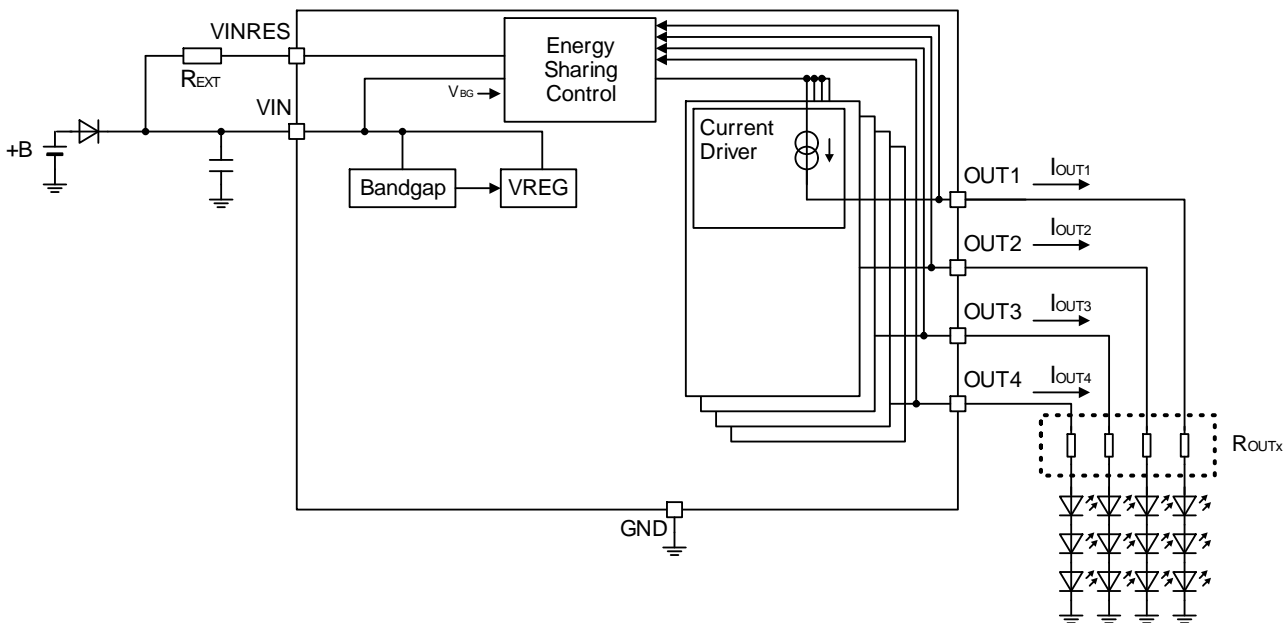


Figure 8. Energy Sharing Control

2. Energy Sharing Control – continued

The power consumption( $P_c$ ) across the IC and  $R_{EXT}$  when  $I_{OUT\_TOTAL}=200\text{ mA}$ ,  $V_{OUTx}=6\text{ V}$  ( $x=1\text{ to }4$ ),  $R_{EXT}=30\ \Omega$ ,  $40\ \Omega$  or  $50\ \Omega$  are shown below. (Reference data)

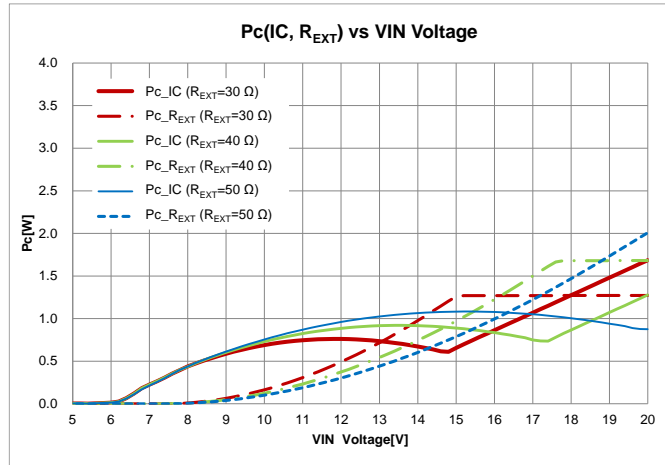


Figure 9. Energy Sharing Control Operation Example 1

The power consumption( $P_c$ ) across the IC and  $R_{EXT}$  when  $I_{OUT\_TOTAL}=300\text{ mA}$ ,  $V_{OUTx}=6\text{ V}$  ( $x=1\text{ to }4$ ),  $R_{EXT}=20\ \Omega$ ,  $30\ \Omega$  or  $40\ \Omega$  are shown below. (Reference data)

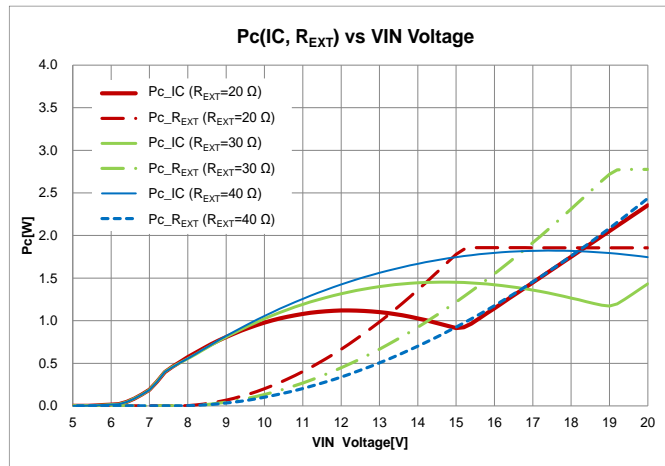


Figure 10. Energy Sharing Control Operation Example 2

The power consumption( $P_c$ ) across the IC and  $R_{EXT}$  when  $I_{OUT\_TOTAL}=400\text{ mA}$ ,  $V_{OUTx}=6\text{ V}$  ( $x=1\text{ to }4$ ),  $R_{EXT}=15\ \Omega$ ,  $20\ \Omega$  or  $25\ \Omega$  are shown below. (Reference data)

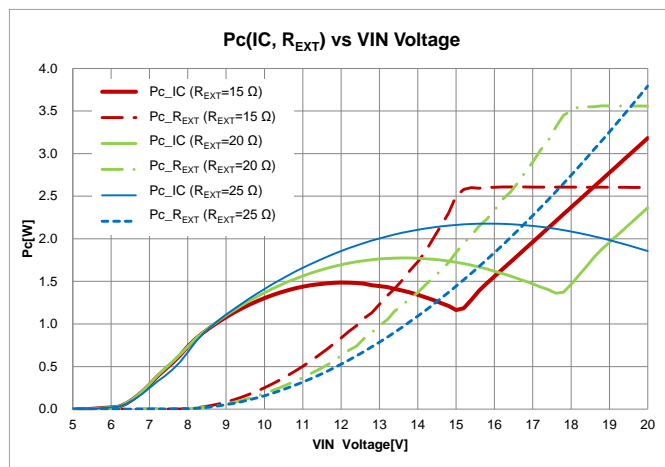


Figure 11. Energy Sharing Control Operation Example 3

## Description of Function – continued

## 3. Table of Operations

Depending on the CRT pin voltage, the IC switches between DC mode and PWM mode. Switching conditions are shown in the table below. When  $V_{IN} > 22.0\text{ V}$ , output current is limited to reduce power dissipation across the IC. Detect LED open and the OUTx pin short circuit then output current is turned OFF. When the PBUS pin is pulled low, all drivers are turned OFF. This IC also has inbuilt Under Voltage Lockout (UVLO) and Thermal Shutdown function (TSD). The correspondence table is given below. For details, refer to functional description of each block.

Operation Mode	CRT Pin	Detecting Condition		Output Current ( $I_{OUTx}$ )	PBUS Pin
		[Detect]	[Release]		
DC	$V_{CRT} \geq 2.0\text{ V (Typ)}$	-	-	50 mA to 150 mA	-
PWM Dimming	See Description of Function 4	-	-	See Description of Function 4	-
Over Voltage Mute (OVM)	-	$V_{IN} > 22.0\text{ V (Typ)}$	$V_{IN} \leq 22.0\text{ V (Typ)}$	See Description of Function 13	-
LED Open Detection	-	$V_{OUTx} \geq V_{INRES} - 0.05\text{ V (Typ)}$ and $V_{IN} \geq V_{IN\_OPM} \text{ (Typ)}$	$V_{OUTx} < V_{INRES} - 0.05\text{ V (Typ)}$ or $V_{IN} < V_{IN\_OPM} \text{ (Typ)}$	See Description of Function 11	Low
OUTx Pin Short Circuit Protection (SCP)	-	$V_{OUTx} \leq 0.6\text{ V (Typ)}$	$V_{OUTx} \geq 0.8\text{ V (Typ)}$	See Description of Function 11	Low
SETx Pin Short Detection	-	$R_{SET} \leq 2.4\text{ k}\Omega \text{ (Typ)}$	$R_{SET} > 2.4\text{ k}\Omega \text{ (Typ)}$	OFF	Low
PBUS Control OFF	-	$V_{PBUS} \leq 0.6\text{ V}$	$V_{PBUS} \geq 2.4\text{ V}$	OFF	$V_{PBUS} \leq 0.6\text{ V input}$
Under Voltage Lockout (VIN UVLO)	-	$V_{IN} \leq 4.75\text{ V (Typ)}$	$V_{IN} \geq 5.25\text{ V (Typ)}$	OFF	High
Under Voltage Lockout (VINRES UVLO)	-	$V_{INRES} \leq 4.50\text{ V (Typ)}$	$V_{INRES} \geq 5.00\text{ V (Typ)}$	Power Control OFF	High
TSD	-	$T_j \geq 175\text{ }^\circ\text{C (Typ)}$	$T_j \leq 150\text{ }^\circ\text{C (Typ)}$	OFF	High

Description of Function – continued

4. PWM Dimming Operation

PWM Dimming is performed with the following circuit. The dimming cycle and ON Duty Width can be set by values of the external components ( $C_{CRT}$ ,  $R_{CRT}$ ). Connect the CRT pin to the VIN pin when not in use. Connect the DISC pin to GND or open when not in use.

The CR timer function is activated if DC SW is OPEN. To perform PWM dimming of output current, a triangular waveform is generated at the CRT pin. The output current ( $I_{OUTx}$ ) is turned OFF while CRT voltage is ramp up, and output current ( $I_{OUTx}$ ) is turned ON while CRT voltage is ramp down.

When  $V_{CRT} \geq V_{CRT\_DIS1}$  (2.0 V (Typ)), dimming mode turns to DC Control. When  $V_{CRT} > V_{CRT\_DIS2}$  (2.4 V (Typ)), the DISC pin ON resistor changes from  $R_{DISC1}$  (50  $\Omega$  (Typ)) to  $R_{DISC2}$  (5 k $\Omega$  (Typ)), and the power consumption of the IC is reduced by reducing the inflow current of the DISC pin.

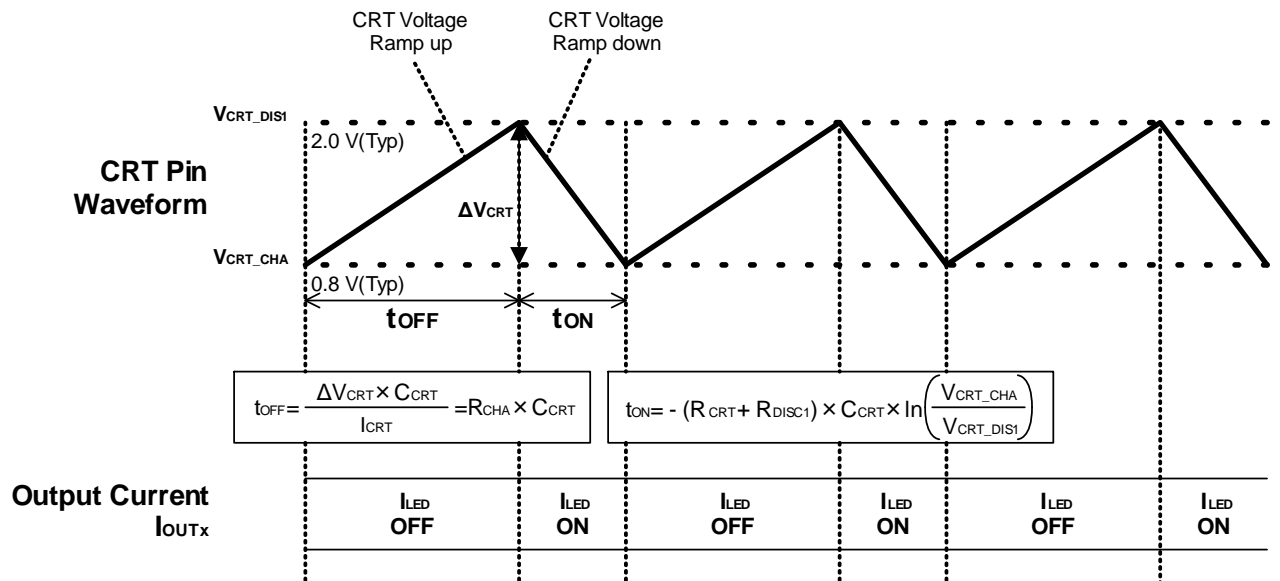
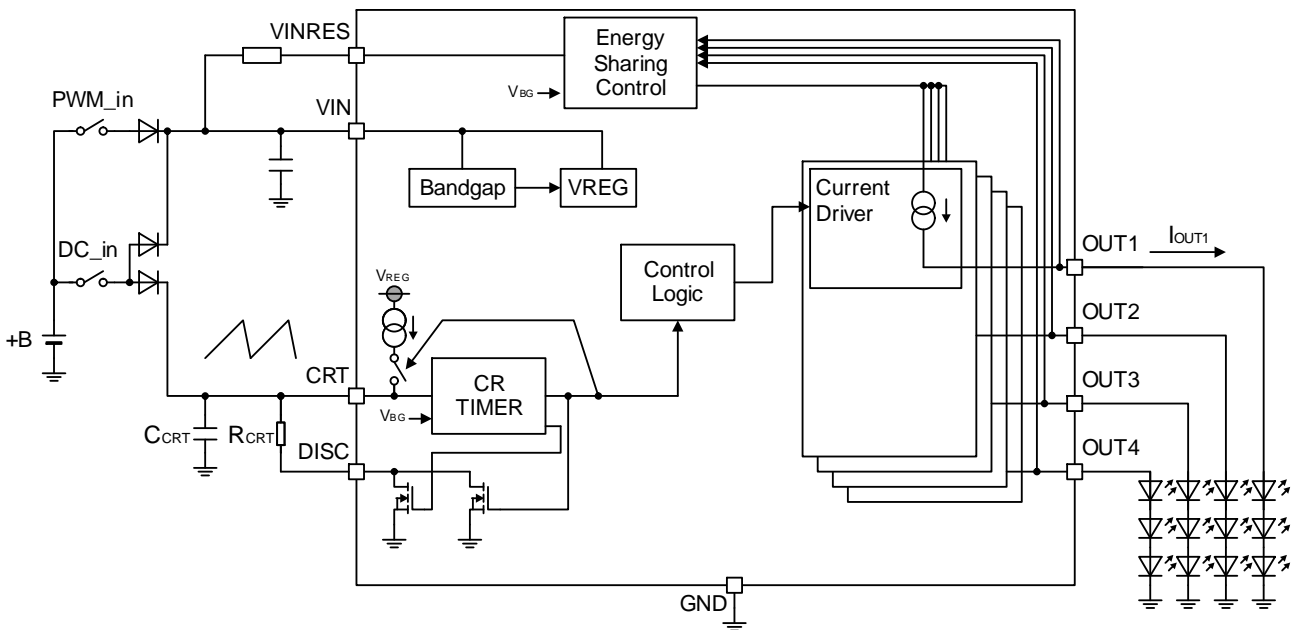


Figure 12. PWM Dimming Operation

4. PWM Dimming Operation – continued

- (1) CRT ramp up time  $t_{OFF}$  and CRT ramp down time  $t_{ON}$   
 CRT ramp up time  $t_{OFF}$  and CRT ramp down time  $t_{ON}$  can be defined from the following equations.  
 Make sure that  $t_{ON}$  is set PWM Minimum Pulse Width  $t_{MIN}$  100  $\mu$ s or more.

$$t_{OFF} = \frac{\Delta V_{C_{CRT}} \times C_{CRT}}{I_{C_{CRT}}} = R_{CHA} \times C_{CRT} \quad [s]$$

$$t_{ON} = -(R_{C_{CRT}} + R_{DISC1}) \times C_{CRT} \times \ln\left(\frac{V_{C_{CRT\_CHA}}}{V_{C_{CRT\_DIS1}}}\right) \quad [s]$$

where:

- $I_{C_{CRT}}$  is the CRT pin charge current, 40  $\mu$ A (Typ).
- $R_{CHA}$  is the CRT pin charge resistor, 30 k $\Omega$  (Typ).
- $R_{DISC1}$  is the DISC pin ON resistor1, 50  $\Omega$  (Typ).
- $V_{C_{CRT\_CHA}}$  is the CRT pin charge voltage, 0.8 V (Typ).
- $V_{C_{CRT\_DIS1}}$  is the CRT pin discharge voltage1, 2.0 V (Typ).

- (2) PWM Dimming Frequency ( $f_{PWM}$ )  
 PWM Dimming Frequency is defined by  $t_{ON}$  and  $t_{OFF}$ .

$$f_{PWM} = \frac{1}{t_{ON} + t_{OFF}} \quad [Hz]$$

- (3) ON Duty ( $D_{ON}$ )  
 PWM ON duty is defined by  $t_{ON}$  and  $t_{OFF}$ .

$$D_{ON} = \frac{t_{ON}}{t_{ON} + t_{OFF}} \quad [\%]$$

(Example) In case of  $R_{C_{CRT}}=3.6$  k $\Omega$ ,  $C_{C_{CRT}}=0.1$   $\mu$ F

$$t_{OFF} = R_{CHA} \times C_{C_{CRT}} = 30 \text{ k}\Omega \times 0.1 \mu\text{F} = 3.0 \quad [ms]$$

$$t_{ON} = -(R_{C_{CRT}} + R_{DISC1}) \times C_{C_{CRT}} \times \ln(V_{C_{CRT\_CHA}}/V_{C_{CRT\_DIS1}}) \\ = -(3.6 \text{ k}\Omega + 50 \Omega) \times 0.1 \mu\text{F} \times \ln(0.8 \text{ V}/2.0 \text{ V}) = 0.334 \quad [ms]$$

$$f_{PWM} = 1/(t_{ON} + t_{OFF}) = 1/(3.0 \text{ ms} + 0.334 \text{ ms}) = 300 \quad [Hz]$$

$$D_{ON} = t_{ON}/(t_{ON} + t_{OFF}) = 0.334 \text{ ms}/(3.0 \text{ ms} + 0.334 \text{ ms}) = 10.0 \quad [\%]$$

•PWM Dimming Operation Using External Signal

In case external PWM input to the CRT pin, make sure that input pulse high voltage  $\geq$  2.2 V and pulse low voltage  $\leq$  0.6 V. Also open the DISC pin or connect to GND.

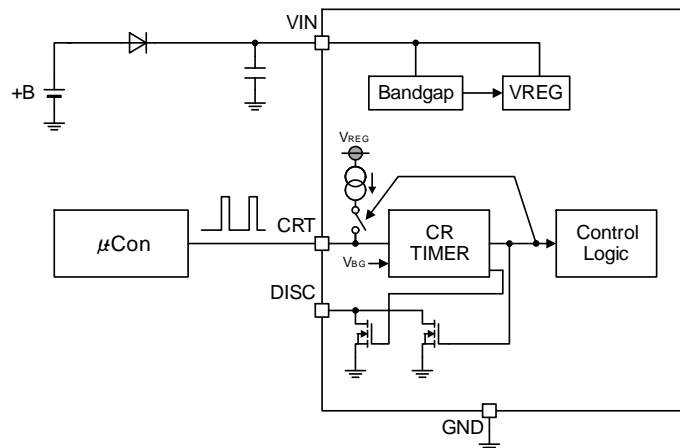


Figure 13. PWM Dimming Operation Using External Signal

4. PWM Dimming Operation – continued

●About deviation of CRT ramp up/down time with a reverse connection protection diode

If this LSI is used to drive LED like below schematic, it is possible to occur CRT ramp up/down time deviation due to characteristics of reverse current  $I_r$  diode (D2, D3).

Consider to choose a diode (D2, D3) which is recommended by Rohm or  $I_r$  value  $1 \mu\text{A}$  (Max) or less.

Since reverse current flows even with the recommended diodes, connect a resistor  $R_{DCIN}$  of  $10 \text{ k}\Omega$  or less between point A and GND so that the voltage at point A does not rise.

Mechanism of deviation of CRT ramp up/down time from set values.

- (1) During the PWM dimming operation mode, Point A on [Figure 14](#) is Hi-Z.
- ↓
- (2) Reverse current  $I_r$  of D2 and D3 goes to Point A.  
 (Power supply voltage is being input into the cathode of D2, so mainly reverse current of D2 goes into C1.)  
 →Reverse current  $I_r$  of D3 is added to the CRT pin charge current and discharge current, so CRT ramp up/down time deviates from the settings.
- ↓
- (3) C1 gets charged, voltage at Point A rises.
- ↓
- (4) Point A voltage  $\geq$  the CRT pin voltage of each IC.
- ↓
- (5)  $V_f$  occurs in the diodes D3.
- ↓
- (6) D3 circulate forward current  $I_F$   
 →Forward current  $I_F$  of D3 is added to the CRT pin charge current and discharge current, so CRT ramp up/down time deviates from the settings.
- ↓
- (7) Repetition of (2) to (6).

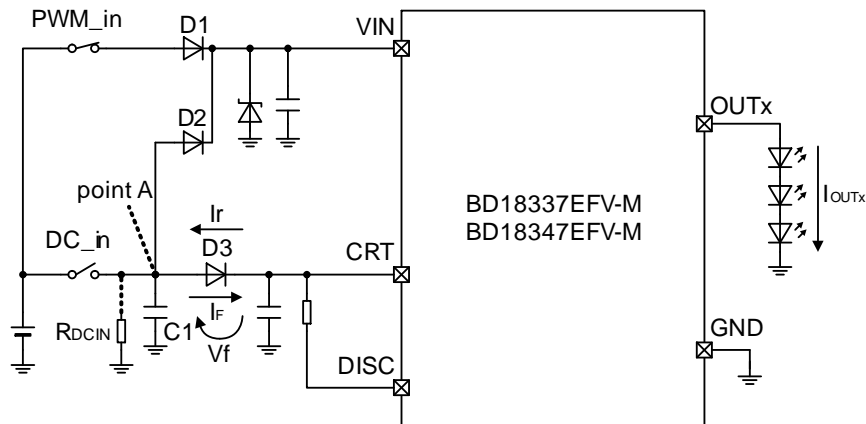


Figure 14. How Reverse Protection Diode Affects the CRT pin Ramp Up / Down Time

Description of Function – continued

5. The SETx pin Short Detection Function

When the SETx pin is shorted to GND, the IC detects that the SETx pin current has increased and turns off the output current. The maximum resistance on the SETx pin short detection is  $R_{SETx} \leq 5.0 \text{ k}\Omega$  (Max). Fault is indicated by pulling the PBUS pin low.

Note that the SETx pin short detection resistance value  $R_{SETx}$  is 5 kΩ or less when the over voltage mute function is active.

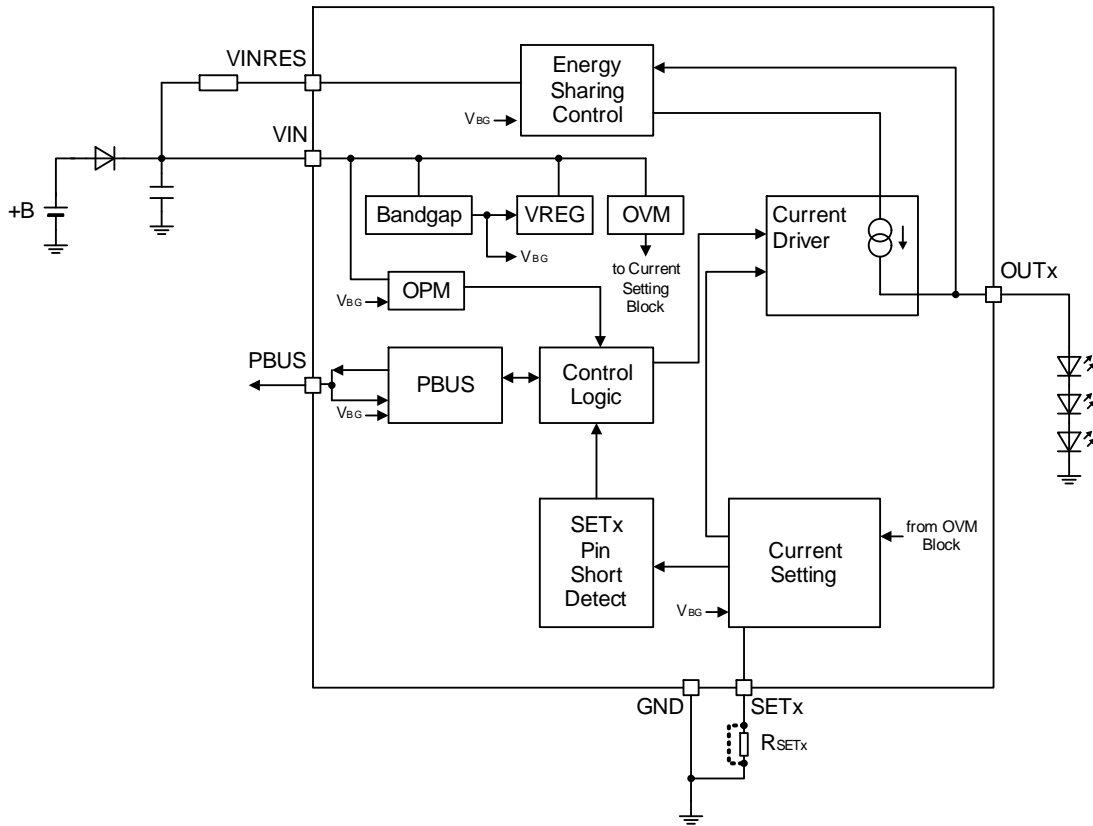


Figure 15. SETx pin Short Detection

Description of Function – continued

6. LED Open Detection Function

When one of the LEDs is in the open state, the OUTx pin voltage rises. At  $V_{OUTx} \geq V_{INRES} - 0.05\text{ V}$  (Typ), LED Open Detection operation is performed. In case of LED Open Detection, fault is indicated by pulling the PBUS pin low.

7. Disable LED Open Detection Function at Reduced-Voltage

Built-in disable LED Open Detection function prevents erroneous detection of LED Open during voltage ramp up or ramp down at the VIN pin. Open Detection is not performed until the VIN pin voltage is internal OPM threshold voltage ( $V_{IN\_OPM}$ ) or more. LED Open Detection remains disabled during power supply ramp up and ramp down, when  $V_{IN} < V_{IN\_OPM}$ .

For disable LED Open Detection function to work properly, LEDs must be selected according to the following formula:

$$V_{f\_LED\_OPD} \times N + 100\text{ mV} + R_{VIN\_VINRES} \times 40\text{ mA} < V_{IN\_OPM} \quad [V]$$

where:

- $V_{f\_LED\_OPD}$  is the LED Vf when  $I_f = I_{OUT\_OPEN}$  ( $I_{OUT\_OPEN} = 10\text{ mA}$  (Max))
- $R_{VIN\_VINRES}$  is the ON resistance between the VIN pin and the VINRES pin.
- $N$  is the number of LED.

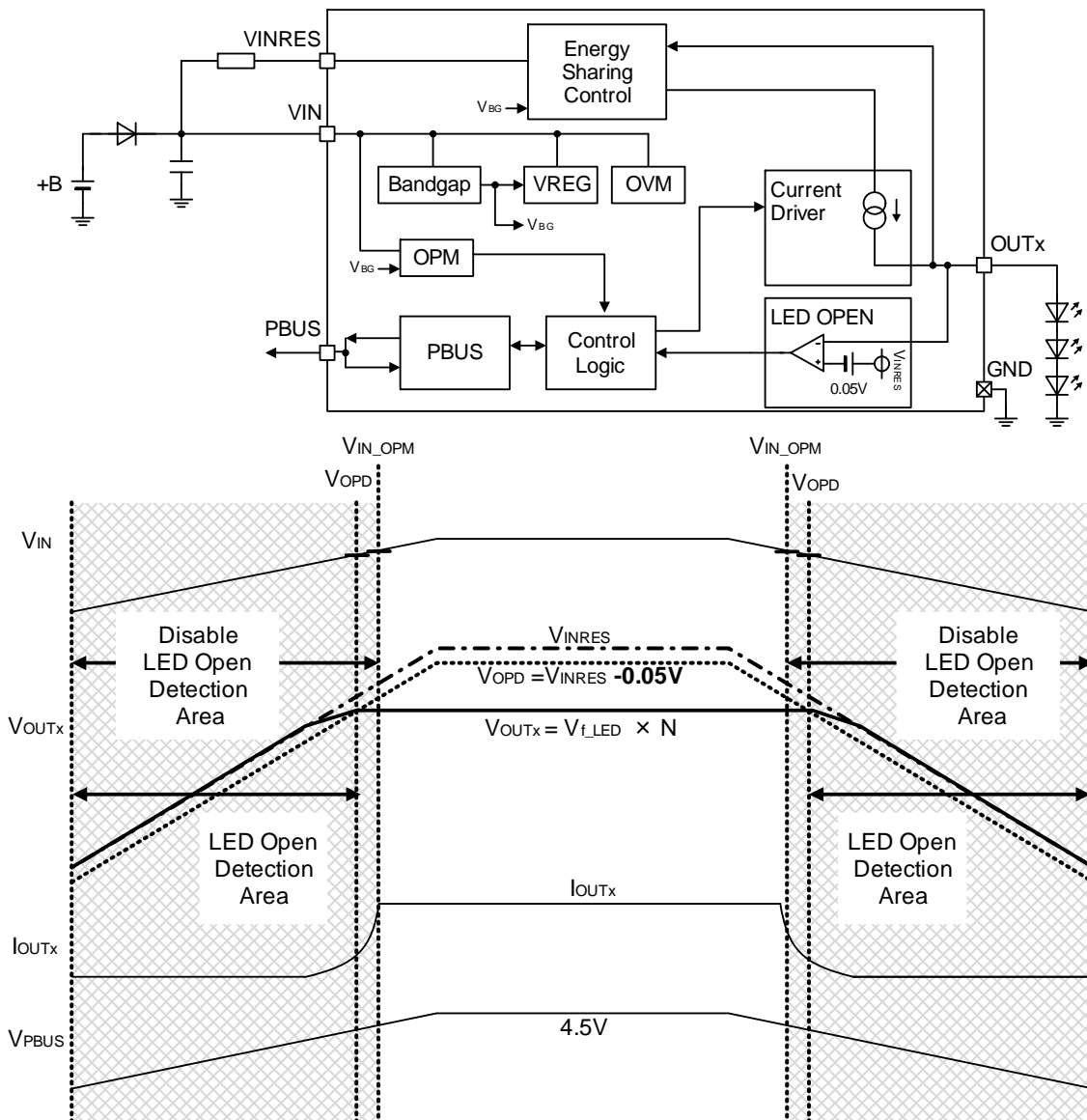


Figure 16. Disable LED Open Detection Voltage at Reduced-Voltage

Description of Function – continued

8. OUTx pin Short Circuit Protection (SCP)

If the OUTx pin is shorted to GND, the OUTx voltage goes low. When the OUTx pin voltage  $V_{OUTx} \leq 0.6\text{ V}$  (Typ), then SCP mechanism is enabled after a delay of  $t_{SCPD2}$  ( $20\ \mu\text{s}$  (Typ)). In case of SCP, output current  $I_{OUT}$  is turned off to prevent thermal damage of the IC. Fault is indicated by pulling the PBUS pin low after a delay open  $t_{SCPD1}$  ( $60\ \mu\text{s}$  (Typ)). To prevent false SCP at power supply startup, the output SCP is disabled until  $V_{CRT} > 2.0\text{ V}$  (Typ) once UVLO is released. In case of power supply ramping up with the OUTx pin short circuit condition ( $V_{OUTx} < 0.6\text{ V}$  (Typ)), SCP mechanism is enabled after  $t_{SCPPON}$  ( $140\ \mu\text{s}$  (Typ)), only if UVLO is released and  $V_{CRT} > 2.0\text{ V}$  (Typ).

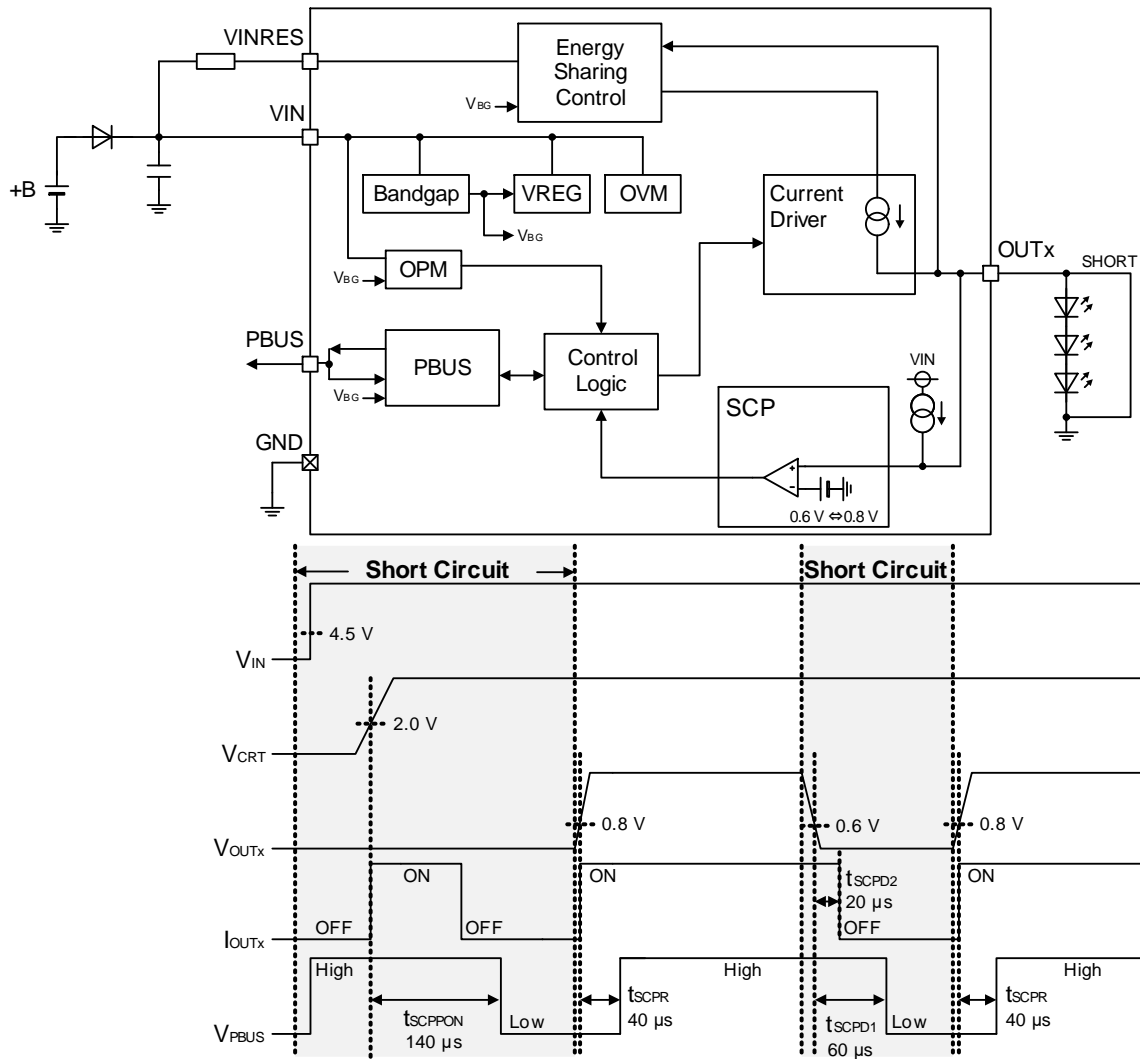


Figure 17. OUTx pin Short Circuit Protection (SCP)

•OUTx pin short circuit current

When  $V_{OUTx} < 1.3\text{ V}$ , the OUTx pin short circuit current  $I_{OUTx\_SCP}$  flows to prevent malfunction of the OUTx pin short circuit protection mechanism.

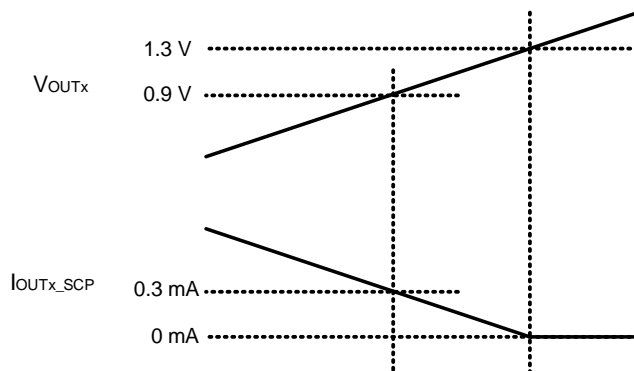


Figure 18. OUTx pin Short Circuit Current

Description of Function – continued

9. Connection Method of LEDs to Output pins – Effect on Protection Functions

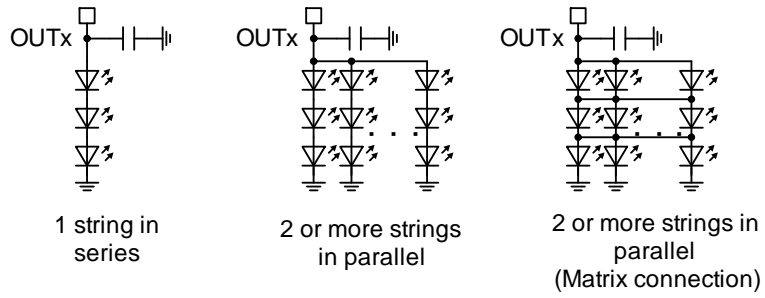


Figure 19. About the Capacitor of Connecting LED Anode

Connection method	Output SCP	LED Open Detection
1 string in Series	Detectable	Detectable
2 or more strings in parallel	Detectable	Not detectable <sup>(Note 1)</sup>
2 or more strings in parallel (Matrix connection)	Detectable	Not detectable <sup>(Note 2)</sup>

(Note 1) Detectable only when one or more LEDs are open in all columns.  
 (Note 2) Detectable only when all LEDs from any row are open.

Description of Function – continued

10. LED Open Detection, SCP and OUTx pin Hi-Z in DC/PWM Dimming Modes

Operation of LED Open Detection and SCP sections differ in DC mode and PWM dimming mode.

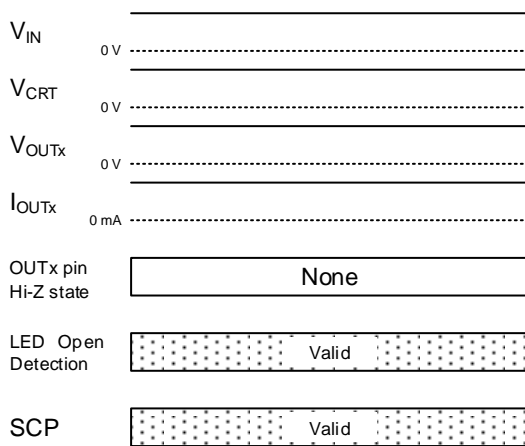
In DC mode, LED Open Detection and SCP are enabled at all times.

In PWM dimming mode, the LED Open Detection function is valid only during the falling edge of CRT signal, whereas SCP is valid at all times. There is a possibility of the OUTx pin becoming Hi-Z. False SCP may occur if the OUTx pin voltage drops due to external noise<sup>(Note 1)</sup>. Connect a capacitor (0.1 μF or more<sup>(Note 2)</sup>) to GND, close to the OUTx pin to avoid erroneous output.

(Note 1) Propagation noise, radiation noise, interference between wires, interference between connectors, etc.

(Note 2) When connecting 0.1 μF or more, evaluate the delay time from the start of VIN until the IOUTx current flows. Also, evaluate the IOUTx pulse width in the PWM dimming mode.

In DC mode



In PWM dimming mode

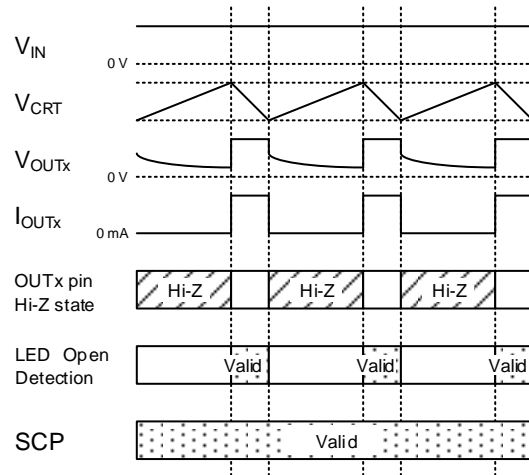


Figure 20. LED Open Detection, SCP and the OUTx pin Hi-Z

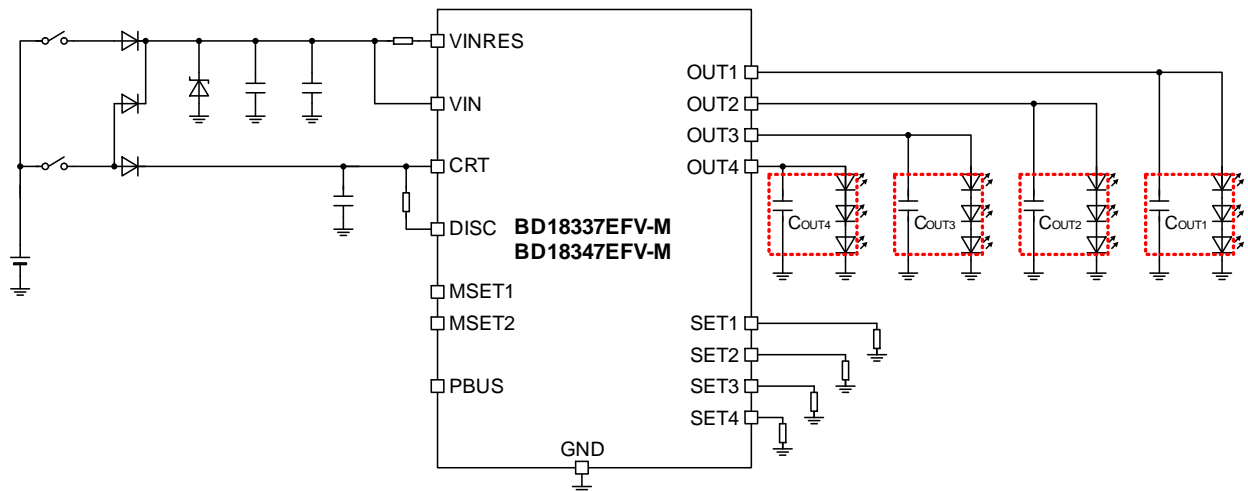


Figure 21. Capacitor Connected to the OUTx pin

10. LED Open Detection, SCP and OUTx pin Hi-Z in DC/PWM Dimming Modes – continued

Evaluation example (ILED pulse width at PWM Dimming operation)

- Condition: +B=13 V
- Ta=25 °C
- LED=1 Strings
- C<sub>CRT</sub>=0.01 μF
- R<sub>CRT</sub>=1.0 kΩ
- PWM Dimming Mode

	50 mA / ch		150 mA / ch	
C <sub>OUTx</sub> =0.01 μF		Rise Time		Rise Time
		3.5 μs		2.5 μs
		Fall Time		Fall Time
		0.8 μs		0.8 μs
C <sub>OUTx</sub> =0.22 μF		Rise Time		Rise Time
		7.7 μs		4.9 μs
		Fall Time		Fall Time
		12 μs		9.9 μs

Description of Function – continued

11. Lamp Control Modes (MSET1, MSET2)

By connecting the MSET1 pin to ground or open, it is possible to change output channel operation mode on detecting an LED error. The MSET2 pin can also be used to control CH4 operation.

MSET1=L (GND short): If SCP or LED Open is detected in any one of 4 channels, all the channels are OFF.

MSET1=H (Pin open) : Remaining channels continue to operate even if one channel detects SCP or LED Open.

MSET2=L (GND short): CH4 operates in the same way as CH1 to CH3

MSET2=H (Pin open) : CH4 ignores the PWM signal generated by CRTIMER and are always in DC mode. When CH4 detects SCP or LED Open, PBUS : H is maintained and CH1 to CH3 continue to operate (License Lamp Mode).

Normal Mode (MSET2=L)

MSET1	MSET2	OUT1 to OUT3 OPEN Detect	OUT1 to OUT3 SCP	OUT4 OPEN Detect	OUT4 SCP	LED Error CH Output	Remaining CH1 to CH3 Output	CH4 Output	PBUS
L All CH OFF	L Normal Mode	Detect	-	-	-	ON	OFF	OFF	L
		-	Detect	-	-	OFF	OFF	OFF	
		-	-	Detect	-	ON	OFF	ON	
		-	-	-	Detect	OFF	OFF	OFF	
H IndividualCH OFF		Detect	-	-	-	ON	ON	ON	L
		-	Detect	-	-	OFF	ON	ON	
		-	-	Detect	-	ON	ON	ON	
		-	-	-	Detect	OFF	ON	OFF	

License Mode (MSET2=H)

MSET1	MSET2	OUT1 to OUT3 OPEN Detect	OUT1 to OUT3 SCP	OUT4 OPEN Detect	OUT4 SCP	LED Error CH Output	Remaining CH1 to CH3 Output	CH4 Output	PBUS	
L All CH OFF	H License Mode	Detect	-	-	-	ON	OFF	ON	L	
		-	Detect	-	-	OFF	OFF	ON		
		-	-	Detect	-	ON	ON	ON	H	
		-	-	-	Detect	OFF	ON	OFF		
H IndividualCH OFF		Detect	-	-	-	-	ON	ON	ON	L
		-	Detect	-	-	OFF	ON	ON		
		-	-	Detect	-	ON	ON	ON	H	
		-	-	-	Detect	OFF	ON	OFF		

Figure 22. Lamp Control Modes (MSET1, MSET2)

Description of Function – continued

12. PBUS Function

The PBUS pin is the pin to input and output an error signal.

When abnormality such as LED Open or the OUTx pin short circuit occurs, it can notify the abnormality to the outside by changing the PBUS pin output from high to low. In addition, by externally controlling the PBUS pin from high to low, the output current is turned off. When using multiple LSIs to drive multiple LEDs, it is possible to turn off all LED lines at once by connecting the PBUS pins of each CH as shown in the figure below, even if LED Open or the OUTx pin short circuit occurs.

**Caution of using the PBUS Pin**

Do not connect to the PBUS pins other than below list items due to the difference of ratings, internal threshold voltages, and so on. (BD18340FV-M, BD18341FV-M, BD18342FV-M, BD18343FV-M, BD18345EFV-M, BD18337EFV-M, BD18347EFV-M)

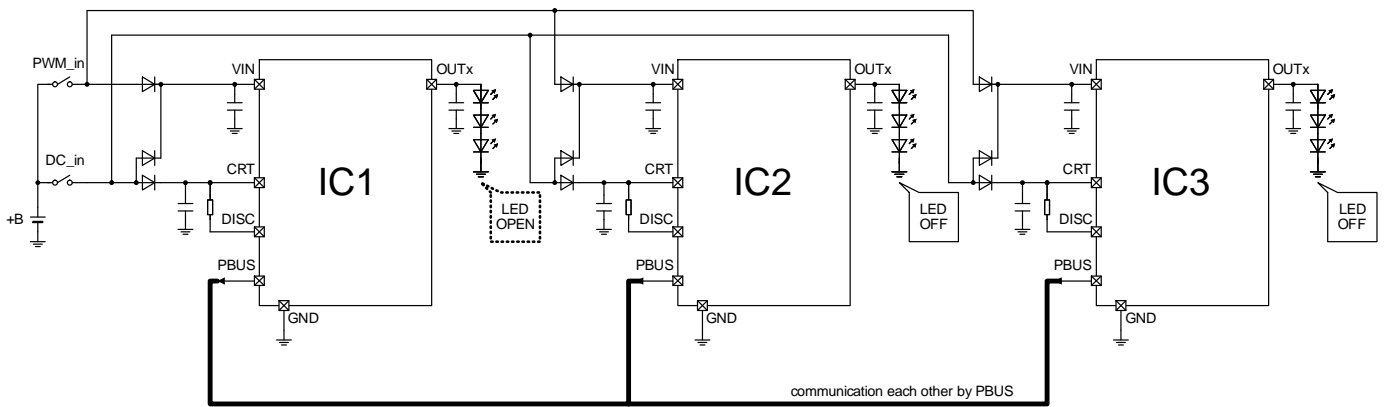


Figure 23. PBUS Function

▼ Example of Protective Operation due to LED Open Circuit

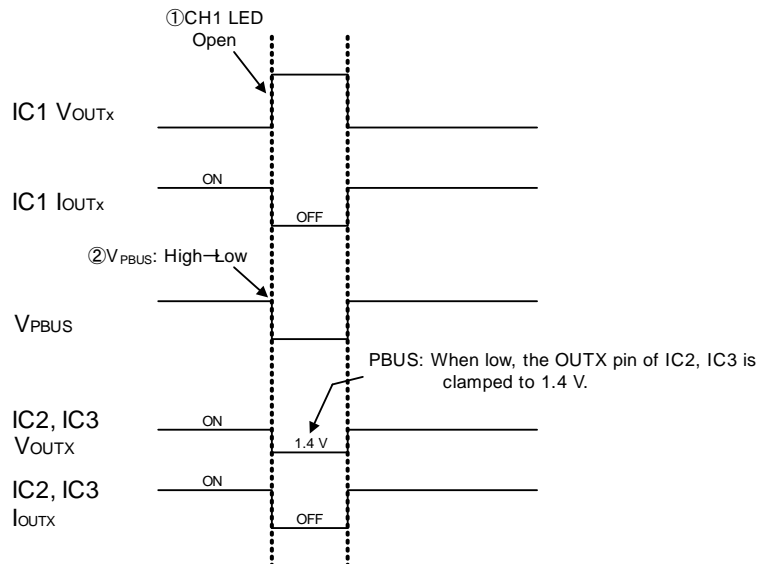


Figure 24. Example of Protective Operation

In case of LED Open,  $V_{PBUS}$  of IC1 goes from High to Low. As  $V_{PBUS}$  goes low, IC2 and IC3 LED drivers turn off their LEDs. When  $V_{PBUS}$  goes low, the OUTx pins are clamped to 1.4 V (Typ), in order to prevent output ground protection operation.

Description of Function – continued

13. Over Voltage Mute Function (OVM)

When the VIN pin voltage exceeds 22.0 V (Typ), Over Voltage Mute function is activated to prevent thermal deterioration to the IC. This is done by attenuating the output current ( $I_{OUTx}$ ). The output current ( $I_{OUTx}$ ) is attenuated at -20 %/V (Typ). If the output current is attenuated less than 10 mA (Typ), output current is turned OFF.

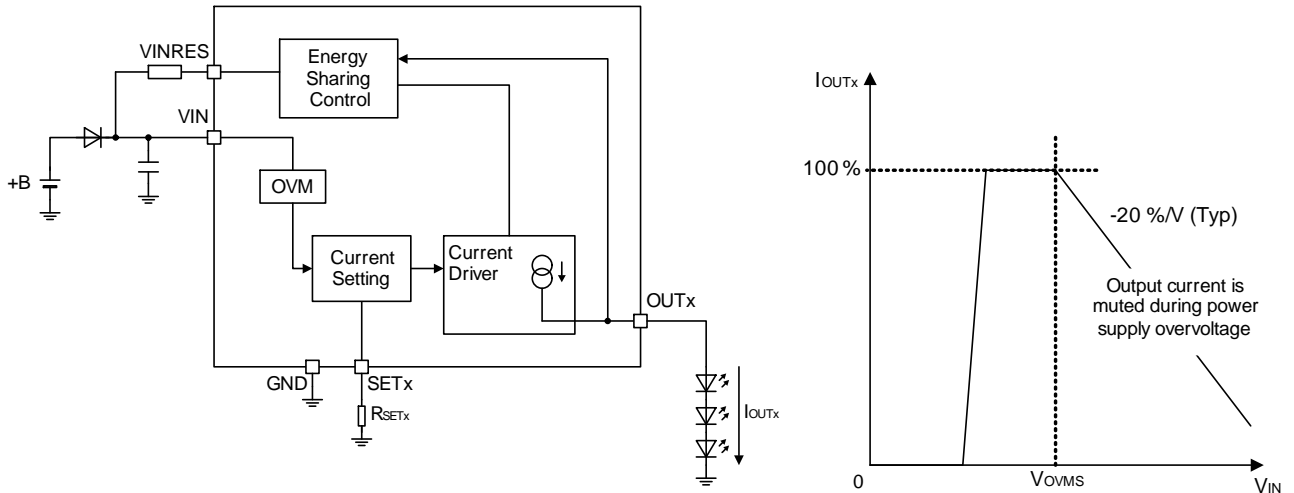


Figure 25. Over Voltage Mute Function (OVM)

14. Under Voltage Lockout (UVLO)

UVLO circuit prevents the IC malfunction during times of power supply ramp up, ramp down or instantaneous power interruptions. When the VIN pin voltage is 4.75 V (Typ) or less, VIN UVLO is activated and output current ( $I_{OUTx}$ ) is turned OFF, and when the VIN pin voltage increases to 5.25 V (Typ) or more, VIN UVLO is deactivated and normal operation resumes. The VINRES pin voltage is 4.50 V (Typ) or less, VINRES UVLO is activated and power control function is turned OFF, and when The VINRES pin voltage increases to 5.00V (Typ) or more, VINRES UVLO is deactivated and power control function is turned ON.

Application Examples

1.  $I_{OUTx}=75\text{ mA/ch License MODE}$ ,  
**PWM ON Duty:10 %**, **Pulse Width=0.334 ms**, **PWM Frequency=300 Hz**

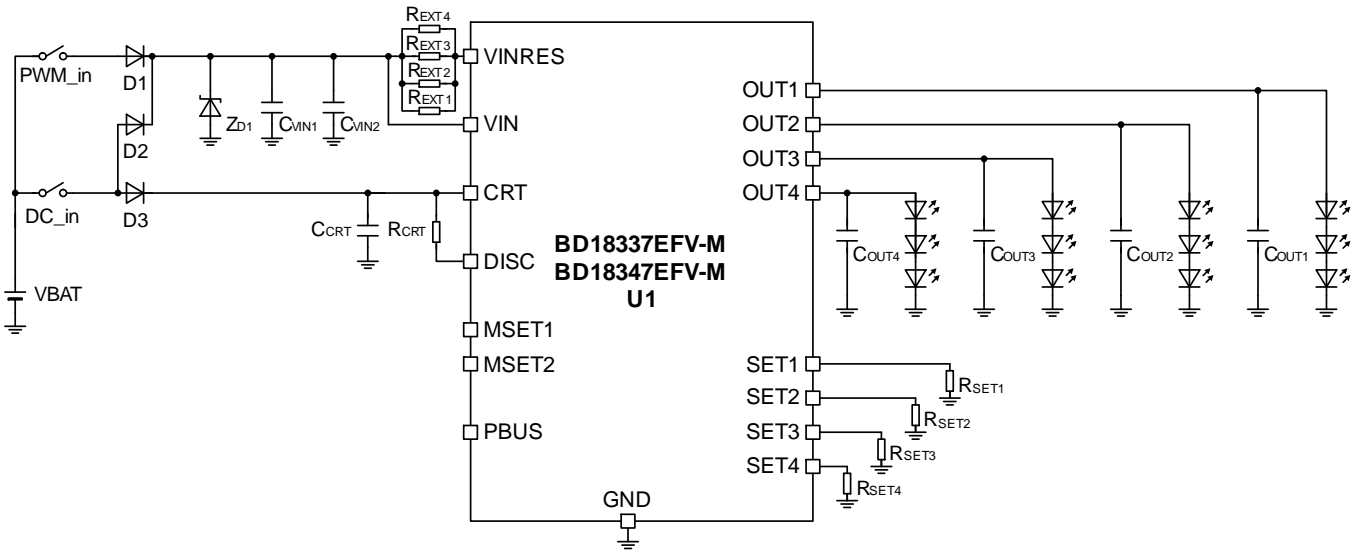


Figure 26. Application Example 1

Recommended Parts List 1

Parts	No.	Parts Name	Value	Unit	Product Maker
IC	U1	BD18337EFV-M BD18347EFV-M	-	-	ROHM
Diode	D1, D2	RFN2LAM6STF	-	-	ROHM
	D3	RFN1LAM6STF	-	-	ROHM
	Z <sub>D1</sub>	TND12H-220KB00AAA0	-	-	NIPPON CHEMICON
Resistor	R <sub>SET1</sub> , R <sub>SET2</sub> , R <sub>SET3</sub> , R <sub>SET4</sub>	MCR03EZPFX2402	24	kΩ	ROHM
	R <sub>EXT1</sub> , R <sub>EXT2</sub> , R <sub>EXT3</sub> , R <sub>EXT4</sub>	LTR100JZPJ101	100	Ω	ROHM
	R <sub>CRT</sub>	MCR03EZPFX3601	3.6	kΩ	ROHM
Capacitor	C <sub>VIN1</sub>	GCM32ER71H475KA40	4.7	μF	murata
	C <sub>VIN2</sub>	GCM155R71H104KE37	0.1	μF	murata
	C <sub>CRT</sub>	GCM155R71H104KE37	0.1	μF	murata
	C <sub>OUT1</sub> , C <sub>OUT2</sub> , C <sub>OUT3</sub> , C <sub>OUT4</sub>	GCM155R71H104KE37	0.1	μF	murata

About Z<sub>D1</sub>, place according to test standard of battery line.

Application Examples – continued

- 2.  $I_{OUTx}=100\text{ mA/ch}$ , Tail / Stop application with MSET1=L  
 PWM ON Duty=10 %, Pulse Width=0.334 ms, PWM Frequency=300 Hz

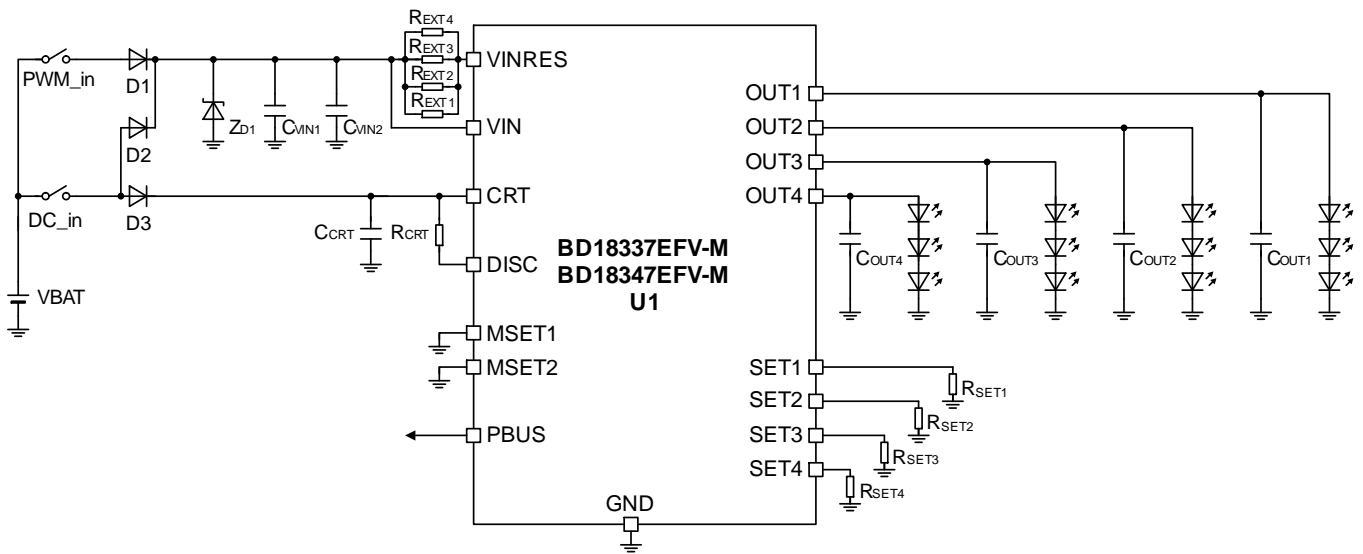


Figure 27. Application Example 2

Recommended Parts List 2

Parts	No.	Parts Name	Value	Unit	Product Maker
IC	U1	BD18337EFV-M BD18347EFV-M	-	-	ROHM
Diode	D1, D2	RFN2LAM6STF	-	-	ROHM
	D3	RFN1LAM6STF	-	-	ROHM
	Z <sub>D1</sub>	TND12H-220KB00AAA0	-	-	NIPPON CHEMICON
Resistor	R <sub>SET1</sub> , R <sub>SET2</sub> , R <sub>SET3</sub> , R <sub>SET4</sub>	MCR03EZPFX2402	18	kΩ	ROHM
	R <sub>EXT1</sub> , R <sub>EXT2</sub> , R <sub>EXT3</sub> , R <sub>EXT4</sub>	LTR100JZPJ101	100	Ω	ROHM
	R <sub>CRT</sub>	MCR03EZPFX3601	3.6	kΩ	ROHM
Capacitor	C <sub>VIN1</sub>	GCM32ER71H475KA40	4.7	μF	murata
	C <sub>VIN2</sub>	GCM155R71H104KE37	0.1	μF	murata
	C <sub>CRT</sub>	GCM155R71H104KE37	0.1	μF	murata
	C <sub>OUT1</sub> , C <sub>OUT2</sub> , C <sub>OUT3</sub> , C <sub>OUT4</sub>	GCM155R71H104KE37	0.1	μF	murata

About Z<sub>D1</sub>, place according to test standard of battery line.

Application Examples – continued

3. I<sub>OUTx</sub>=100 mA/ch, PWM Control Each Channel from External Signal

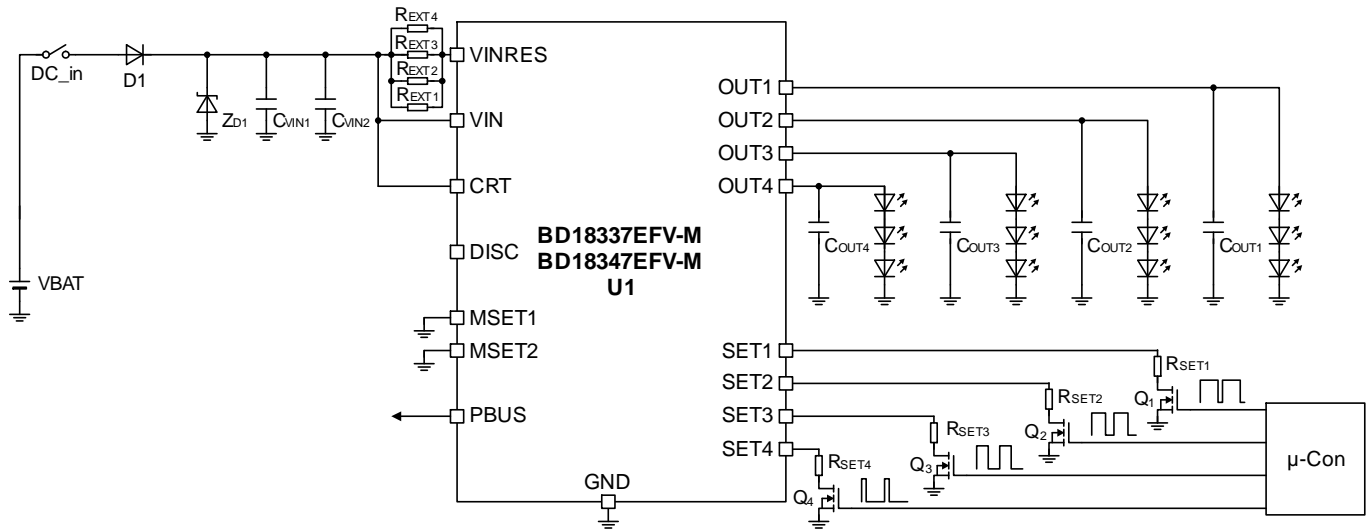


Figure 28. Application Example 3

Recommended Parts List 3

Parts	No.	Parts Name	Value	Unit	Product Maker
IC	U1	BD18337EFV-M BD18347EFV-M	-	-	ROHM
MOSFET	Q1 to Q4	RJU003N03FRAT106	-	-	ROHM
Diode	D1	RFN2LAM6STF	-	-	ROHM
	ZD1	TND12H-220KB00AAA0	-	-	NIPPON CHEMICON
Resistor	RSET1, RSET2, RSET3, RSET4	MCR03EZPFX2402	18	kΩ	ROHM
	REXT1, REXT2, REXT3, REXT4	LTR100JZPJ101	100	Ω	ROHM
Capacitor	CVIN1	GCM32ER71H475KA40	4.7	μF	murata
	CVIN2	GCM155R71H104KE37	0.1	μF	murata
	COUT1, COUT2, COUT3, COUT4	GCM155R71H104KE37	0.1	μF	murata

About Z<sub>D1</sub>, place according to test standard of battery line.

## Power Dissipation

Thermal design should meet the following equation.

$$P_d > P_C$$

$$P_d = (1/\theta_{JA}) \times (T_{jmax} - T_a) \text{ or } (1/\Psi_{JT}) \times (T_{jmax} - T_T)$$

When don't use Energy Sharing Control, refer to below equation.

$$P_C = (V_{IN} \times (I_{VIN1} + I_{DISC}) + (V_{IN} - V_{OUT1}) \times I_{OUT1} + (V_{IN} - V_{OUT2}) \times I_{OUT2} + (V_{IN} - V_{OUT3}) \times I_{OUT3} + (V_{IN} - V_{OUT4}) \times I_{OUT4}$$

When use Energy Sharing Control, refer to page 11 and 12.

where:

$P_d$	is the power dissipation.
$P_C$	is the power consumption.
$V_{IN}$	is the VIN pin voltage.
$I_{VIN1}$	is the circuit current at normal mode.
$I_{DISC}$	is the DISC pin input current.
$I_{OUT1}$ to $I_{OUT4}$	is the output current through each channel.
$V_{OUT1}$ to $V_{OUT4}$	is the OUTx pin voltage each channel.
$\theta_{JA}$	is the thermal resistance of junction to ambient.
$\Psi_{JT}$	is the thermal characterization parameter of junction to center case surface.
$T_{jmax}$	is the maximum junction temperature (150 °C).
$T_a$	is the ambient temperature.
$T_T$	is the case surface temperature.

I/O Equivalence Circuits

No.	Pin Name	I/O Equivalence Circuit	No.	Pin Name	I/O Equivalence Circuit
1	VINRES		6,11	MSET1 MSET2	
3	PBUS		7 to 10	SET1 SET2 SET3 SET4	
4	CRT		13 to 16	OUT1 OUT2 OUT3 OUT4	
5	DISC				

## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

### 6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

### 9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When  $GND > Pin A$  and  $GND > Pin B$ , the P-N junction operates as a parasitic diode.  
 When  $GND > Pin B$ , the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

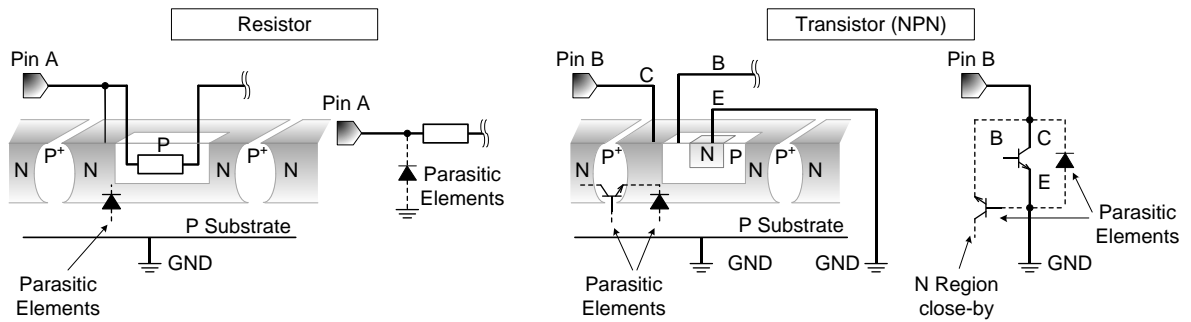


Figure 29. Example of Monolithic IC Structure

11. Ceramic Capacitor

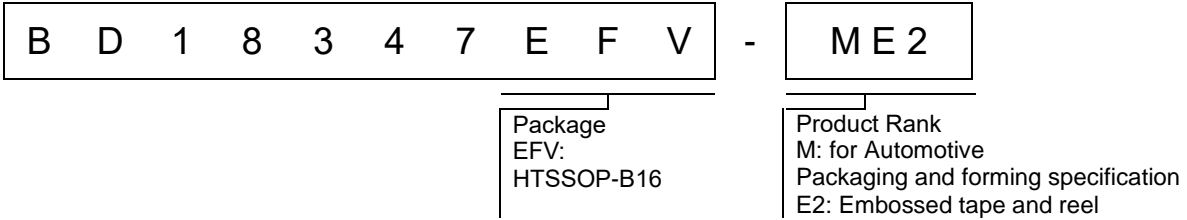
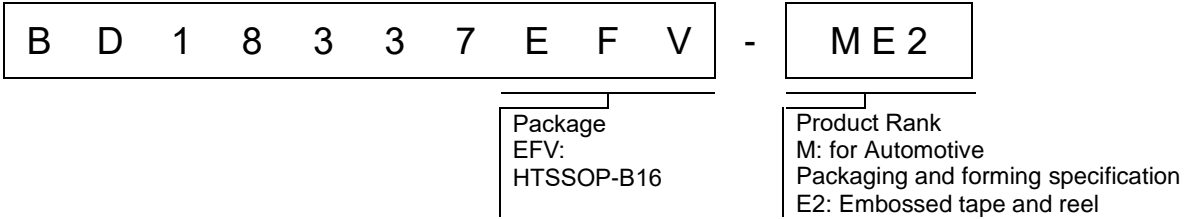
When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

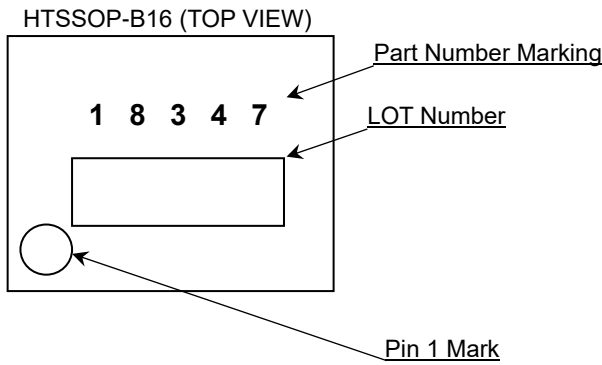
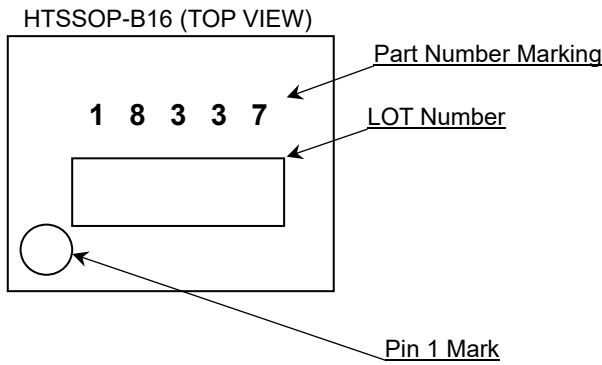
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature ( $T_j$ ) will rise which will activate the TSD circuit that will turn OFF power output pins. When the  $T_j$  falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

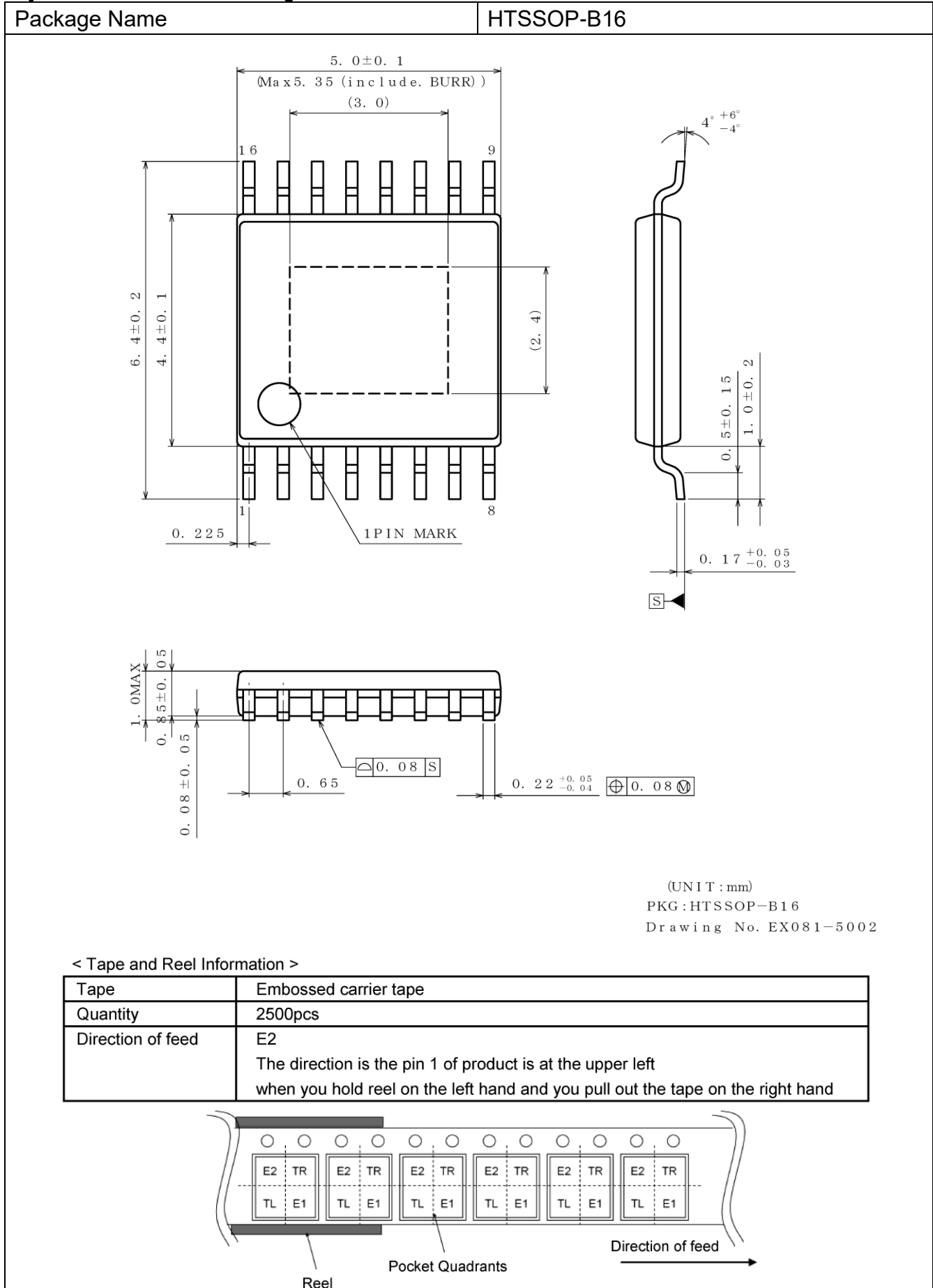
Ordering Information



Marking Diagram



Physical Dimension and Packing Information



Revision History

Date	Revision	Changes
21.Jan.2019	001	New Release
25.Jul.2019	002	<p>Page.6 Electrical Characteristics Circuit current <math>I_{VIN1}</math>, <math>I_{VIN2}</math>, <math>I_{VIN3}</math> Typ 4 mA → Typ 3 mA</p> <p>Page.10 L-9 Sentence Revise Page.11 L-1 Sentence L2-3 Sentence Revise</p> <p>Page.15 PWN dimming function Revise Make sure that <math>t_{ON}</math> is set PWM Minimum Pulse Width <math>t_{MIN}</math> 10 <math>\mu</math>s or more. ↓ Make sure that <math>t_{ON}</math> is set PWM Minimum Pulse Width <math>t_{MIN}</math> 100 <math>\mu</math>s or more.</p> <p>Page.15 (Example) In case of <math>R_{CRT}=3.6</math> k<math>\Omega</math>, <math>C_{CRT}=0.1</math> <math>\mu</math>F Insert unit each formula.</p> <p>Page.19 OUTx pin Short Circuit Protection(SCP) Revise the PBUS pin low after a delay open <math>t_{SCPR}</math> (40 <math>\mu</math>s (Typ)) ↓ the PBUS pin low after a delay open <math>t_{SCPD1}</math> (60 <math>\mu</math>s (Typ))</p>
8.Apr.2022	003	<p>Page.11 <math>V_{UVLO\_VINRESR} \leq V_{OUTx\_MAX} + V_{ES}</math> ↓ <math>V_{UVLO\_VINRESR} \leq V_{OUTx\_MAX}</math></p> <p>Page.23 Figure 22 CH4 Output=OFF→ON  <ul style="list-style-type: none"> <li>• MSET1=L, MSET2=H, OUT1 to OUT3 OPEN Detect=Detect.</li> <li>• MSET1=L, MSET2=H, OUT1 to OUT3 SCP=Detect.</li> </ul> </p>

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CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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  - [h] Use of the Products in places subject to dew condensation
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7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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