



**THE DATASHEET OF  
PI3DPX1203BZHIEX**



## DisplayPort 1.4 HBR3 Linear Redriver with Latency-Free, DP Transparent Link Training support

### Description

PI3DPX1203B is the DisplayPort 1.4 compliant, up to 4 channel, 8.1 Gbps HBR3 Linear Redriver with Link Training transparency support. Displayport source-side and sink-side devices communicate through the AUX transaction between the source and the sink-side devices.

Input Equalization, Voltage Swing and Flat Gain control can be configured with pin-strapping or I2C programming to optimized Main Link high speed signals over a variety of physical medium by reducing inter-symbol interference. Pericom's Linear Redriver technology can deliver 2 times better additive jitters performance than traditional Redrivers.

Linear Equalizer always provide very flexible component placement, cascade connection and easy adjustment after the Redriver location changes during the product development events.

### Features

- Compliant with VESA DisplayPort 1.4 specification up to 8.1 Gbps Link Rate
- Latency-free for the variable video frame rate support
- Dual mode DisplayPort support
- Linear Redriver allows flexible placement with DP Main Link boost setting
- Ideal for DP Alt Type-C Source and Sink-side application with PD Controllers with Aux Link Training Transparent Mode support
- Linear Equalizer increases Link Margin with Sink-side DFE (Decision Feedback Equalizer)
- Independent Main Link channel configuration for 4-bit Equalization, 2-bit Voltage Output swing and 2-bit Flat Gain control
- Pin strap or I2C programmable for device configuration setting
- Intra- and Inter-Channel Polarity Swap support
- I2C Address selectable for configuration register access
- Low Stand-by power consumption
- Power supply voltage: 3.3V
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)

### Applications

- Notebook, Desktop, AIO PC
- Display Monitors
- Active Adaptors, Dongles, Docking

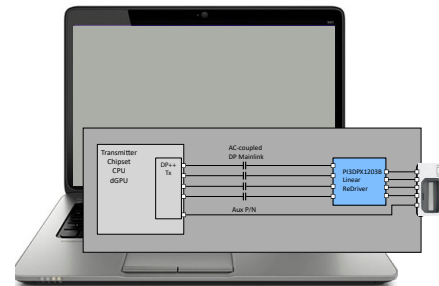


Figure 1-1 DP1.4 HBR3 Redriver in the NB PC

### Ordering Information

Ordering Number	Package Code	Package Description
PI3DPX1203BZLEX	ZL	32-pin, Very Thin Quad Flat No-Lead (TQFN) (3X6mm)
PI3DPX1203BZHDX	ZH	42-pin, Very Thin Quad Flat No-Lead (TQFN) (3.5x9mm)
PI3DPX1203BZHIEX	ZH	Industrial Temperature, 42-pin, Very Thin Quad Flat No-Lead (TQFN) (3.5x9mm)

#### Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

## 2. General Information

### 2.1 Revision History

Revision	Description of Changes
Oct 2016	Ch2. 32-pin TQFN package added. Improve EQ , Stand-by power consumption from PI3DPX1203 DP1.4 Linear Redriver. Support I2C slave programming mode.
Feb 2017	Ch5. DP1.4 CTS compliance test report added
Mar 2017	Ch2. ZH42 pin-out typo fixed. Pin6, 12, 30 changed to NC. Ch4. No index Byte support Ch5. Gp, GF-gain, V1dB_4G typical value updated
May 2017	Ch5. power consumption; IDDQ = typ 0.2uA, max 1mA; IDD = typ 243mA, max =290mA. Ch5. Power-up timing diagram, PRSNT# application schematics added
Jun 2017	In 42-pin package, clarified NC and DNC pins
Jul 2017	Application reference schematic updated to support HPD IRQ
Dec 2017	Package marking added (p42).
Jul 2018	Ordering Information Deleted Section 2.3 Related Products Features Section 4.4 Output -14dB Compressing Setting Section 4.5 EQ Setting Section 6.4 AX/DC Characteristics Figure 6-6 Peaking Gain Definition
Sept 2019	Part Marking

### 2.2 Similar Products Comparison

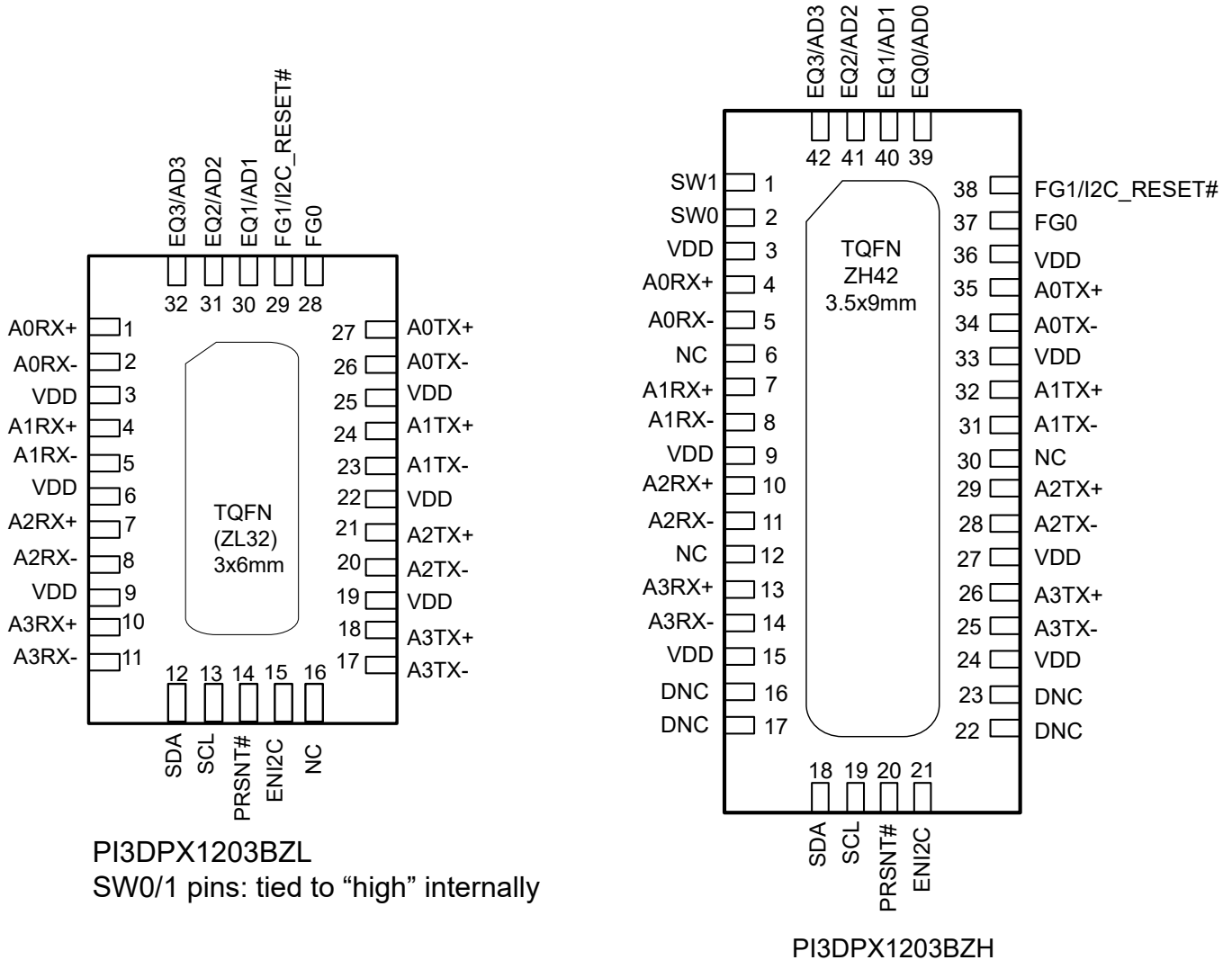
	PI3DPX1203B	PI3DPX1203
Key Features	New silicon. Improved IDDQ = 0.2mA and IDD together. Optimized setting for the DP 1.4 speed.	Old version. IDDQ = 2mA typ
Package Pin-out	Drop in compatible with PI3DPX1203 version	

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### 3. Pin Configuration

#### 3.1 Package Pin-out (Top View)



**Figure 3-1 32/42-pin package pin-out**

**Note:** The polarity (+/-) of each high speed pairs can use interchangeably. Output pins of polarity and data channel will always follow the input polarity and data channel assignment changes.

## 3.2 Pin Description

### 32-pin package

Pin #	Pin Name	Type	Description
<b>Data Signals</b>			
1 2	A0RX+ A0RX-	I	CML differential positive/negative input for Channel A0, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
27 26	A0TX+ A0TX-	O	CML differential positive/negative outputs for Channel A0, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
4 5	A1RX+ A1RX-	I	CML differential positive/negative inputs for Channel A1, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
24 23	A1TX+ A1TX-	O	CML differential positive/negative outputs for Channel A1, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
7 8	A2RX+ A2RX-	I	CML differential positive/negative inputs for Channel A2, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
21 20	A2TX+ A2TX-	O	CML differential positive/negative outputs for Channel A2, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
10 11	A3RX+ A3RX-	I	CML differential positive/negative inputs for Channel A3, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
18 17	A3TX+ A3TX-	O	CML differential positive/negative outputs for Channel A3, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
<b>Control Signals</b>			
12	SDA	I/O	I <sup>2</sup> C Serial Data line
13	SCL	I/O	I <sup>2</sup> C Serial Clock line
14	PRSNT#	I	Cable Present Detect input. This pin has internal 100kΩ pull-up. When High, a cable is not present, and the device is put in lower power mode. When Low, the device is enabled and in normal operation.
15	ENI2C	I	I2C Enable pin. Tied to VDD = Register access I2C Slave mode Tied to GND = Pin mode
32,31,30	EQ[3:1]	I	EQ Control pin. Inputs with internal 100kΩ pull-up. This pins set the amount of Equalizer Boost in all channels when ENI2C is low.
	AD[3:1]	I	Address bits control pins for I2C programming with internal 100kΩ pull-up.
29	FG1/I2C_RESET#	I	Shared pin for Gain Control bit-1 and I2C Reset pin. Inputs with internal 100kΩ pull up resistor. (1) Sets the output flat gain level bit-1 on all channels when ENI2C is Low. (2) I2C Reset pin. Active Low to reset the registers to default state.
28	FG0	I	Flat Gain control bit-0 pin. Inputs with internal 100kΩ pull up resistor. Sets the output flat gain level on all channels when ENI2C is low.
16	NC	NC	Not connect
<b>Power Pins</b>			
3,6,9,19,22,25	VDD	PWR	3.3V Power supply pins
Center Pad	GND	GND	Exposed Ground pad.

**42-pin package**

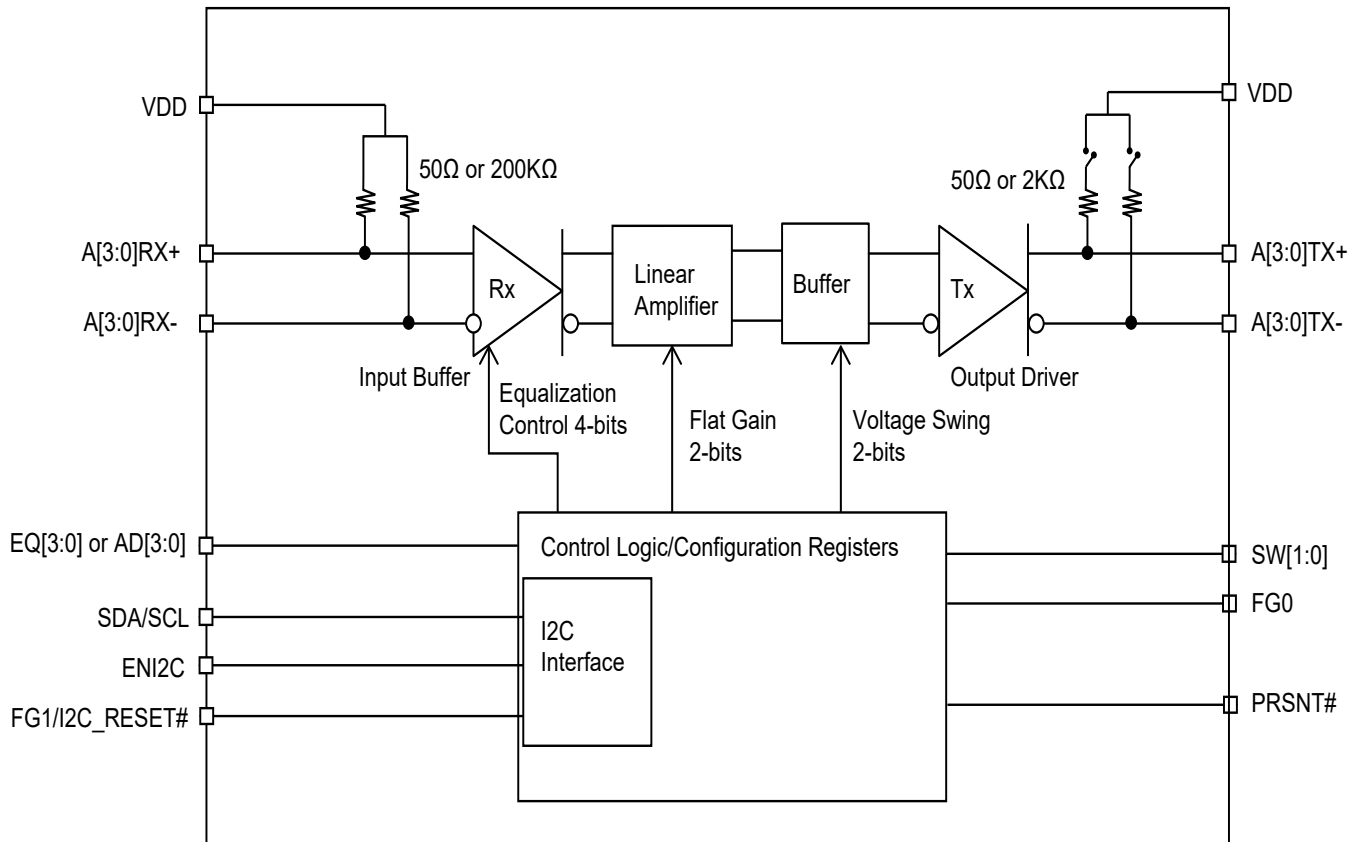
Pin #	Pin Name	Type	Description
<b>Data Signals</b>			
4 5	A0RX+ A0RX-	I	CML differential positive/negative input for Channel A0, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
35 34	A0TX+ A0TX-	O	CML differential positive/negative outputs for Channel A0, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
7 8	A1RX+ A1RX-	I	CML differential positive/negative inputs for Channel A1, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
32 31	A1TX+ A1TX-	O	CML differential positive/negative outputs for Channel A1, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
10 11	A2RX+ A2RX-	I	CML differential positive/negative inputs for Channel A2, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
29 28	A2TX+ A2TX-	O	CML differential positive/negative outputs for Channel A2, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
13 14	A3RX+ A3RX-	I	CML differential positive/negative inputs for Channel A3, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
26 25	A3TX+ A3TX-	O	CML differential positive/negative outputs for Channel A3, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
<b>Control Signals</b>			
19	SCL	I/O	I2C Serial Clock line
18	SDA	I/O	I2C Serial Data line
20	PRSNT#	I	Cable Present Detect input. This pin has internal 100kΩ pull-up. When High, a cable is not present, and the device is put in lower power mode. When Low, the device is enabled and in normal operation.
21	ENI2C	I	I2C Enable pin. Tie to VDD = Register access I2C Slave mode Tie to GND = Pin mode
39,40,41,42	EQ[3:0]	I	EQ Control pin. Inputs with internal 100kΩ pull-up. This pins set the amount of Equalizer Boost in all channel when ENI2C is LOW.
	AD[3:0]	I	I2C address bits control pins for programming with internal 100kΩ pull-up.
1,2	SW[1:0]	I	Output Swing control pins. Inputs with internal 100kΩ pull-up. This pin sets the output Voltage Level in all channel when ENI2C is LOW.
37	FG0	I	Gain Control pin bit 0 Inputs with internal 100kΩ pull up resistor. Sets the output flat gain level on all channels when ENI2C is low.
38	FG1/I2C_RESET#	I	Shared pin for Flat Gain control bit-1 or I2C Reset pin. Inputs with internal 100kΩ pull up resistor. (1) Sets the output flat gain level bit-1 on all channels when ENI2C is Low. (2) I2C Reset pin. Active Low to reset the registers to default state.

**42-pin package cont.**

Pin #	Pin Name	Type	Description
6,12,30	NC		No Connect ( Don't care) pin
16, 17, 22, 23	DNC		Do Not Connect pin
<b>Power Pins</b>			
3, 9, 15, 24, 27, 33, 36	VDD	PWR	3.3V Power Supply pins
Center Pad	GND	GND	Exposed Ground pad.

## 4. Functional Description

### 4.1 Functional Block Diagram



**Figure 4-1 PI3DPX1203B Block Diagram**

## 4.2 Power-Down Mode

Power Enable function: One pin control or I2C control, when PRSNT# is set to high, the IC goes into power down mode, both input and output termination set to 200K and high impedance respectively. Individual channel enabling is done through the I2C register programming.

PRSNT#	Description	Input Termination Resistor	Output Termination Resistor
H	Power-down mode. PRSNT# is internally pull-up 100 kΩ	200 kΩ pull-up	Hi-Z (2 kΩ pull-up)
L	Active Low for normal operation	50 Ω pull-up	50 Ω pull-up

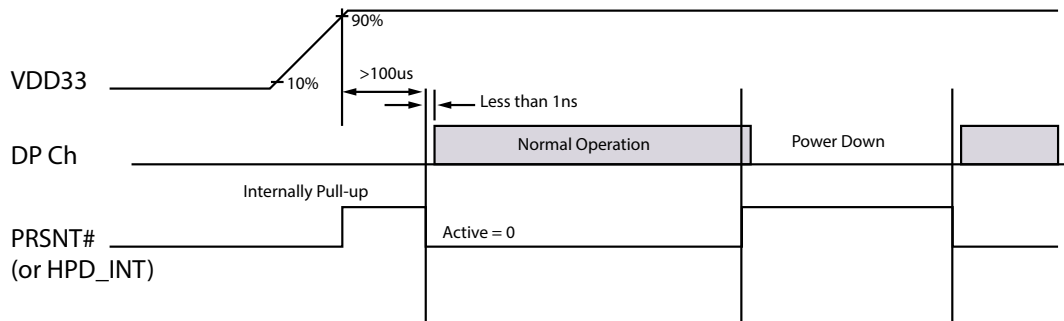


Figure 4-2 Power-up sequence recommendation

## 4.3 Flat Gain Setting

Flat Gain Control 2 bits FG[1:0] are the selection bits for the DC value.

Table 4-1. Flat Gain 2 bits Control Setting

FG1	FG0	Gain (dB)	Notes
0	0	-3.5	
0	1	-1.5	
1	0	0.5	Keep 0.5dB Gain setting for most application cases. Try other setting for the long cable/ transmission line when 0.5dB does not work.
1	1	2.5	

#### 4.4 Output -1 dB Compression Setting

Swing Control 2 bits SW[1:0] control the linearity of the output voltage

Table 4-2. Output Swing -1dB Compression 2 bits Setting

SW1	SW0	mVppd @ 8.1 Gbps (Internally 100KΩ Pull-up)	Notes
0	0	920mV	Recommend setting for fixed DP swing like embedded DP
0	1	1040mV	
1	0	1280mV	DP spec max swing = 1.2Vdiff
1	1	1370mV	Reserved for the non-standard DP application

#### 4.5 EQ Setting

Input EQ control 4 bits EQ[3:0] are the selection pins for the equalization selection for each Main Link channel.

Table 4-3. Input Equalizer 4 bits Setting

EQ3	EQ2	EQ1	EQ0	2.7 Gbps Input EQ(dB)	5.4 Gbps Input EQ(dB)	8.1 Gbps Input EQ(dB)
0	0	0	0	2.3	3.2	3.9
0	0	0	1	2.4	3.5	4.4
0	0	1	0	2.5	3.8	4.9
0	0	1	1	2.6	4.1	5.5
0	1	0	0	2.7	4.5	6.0
0	1	0	1	2.9	4.8	6.5
0	1	1	0	3.0	5.1	6.9
0	1	1	1	3.1	5.5	7.4
1	0	0	0	3.2	5.8	7.8
1	0	0	1	3.4	6.1	8.3
1	0	1	0	3.5	6.4	8.7
1	0	1	1	3.7	6.7	9.0
1	1	0	0	3.8	7.0	9.4
1	1	0	1	4.0	7.4	9.8
1	1	1	0	4.1	7.6	10.1
1	1	1	1	4.3	7.9	10.4

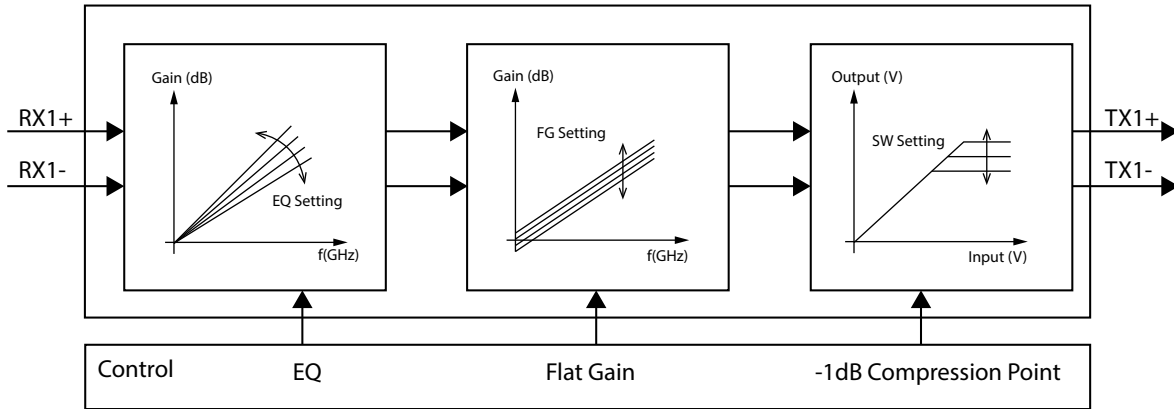


Figure 4-3 Illustration of EQ, Gain and -1dB Compression Point setting

## 5. I2C Programming

### 5.1 I2C Registers

Table 5-1. I2C Address assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	1	AD3	AD2	AD1	1 for ZL32 package AD0 for ZH42 package	1=R, 0=W

Table 5-2. I2C Programming Register definition

#### BYTE 0

Bit	Type	Power up condition	Description	Control affected	Comment
7:0	Reserved				

#### BYTE 1

Bit	Type	Power up condition	Description	Control affected	Comment
7:0	Reserved				

#### BYTE 2

Bit	Type	Power up condition	Description	Control affected	Comment
7	R/W	0		A3 Power down	1 = Power down
6	R/W	0		A2 Power down	
5	R/W	0		A1 Power down	
4	R/W	0		A0 Power down	
3	R/W	0	Reserved		
2	R/W	0			
1	R/W	0			
0	R/W	0			

**BYTE 3**

Bit	Type	Power up condition	Description	Control affected	Comment
7	R/W	0	Channel A0 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	

**BYTE 4**

Bit	Type	Power up condition	Description	Control affected	Comment
7	R/W	0	Channel A1 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	

**BYTE 5**

Bit	Type	Power up condition	Description	Control affected	Comment
7	R/W	0	Channel A2 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	

**BYTE 6**

Bit	Type	Power up condition	Description	Control affected	Comment
7	R/W	0	Channel A3 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	

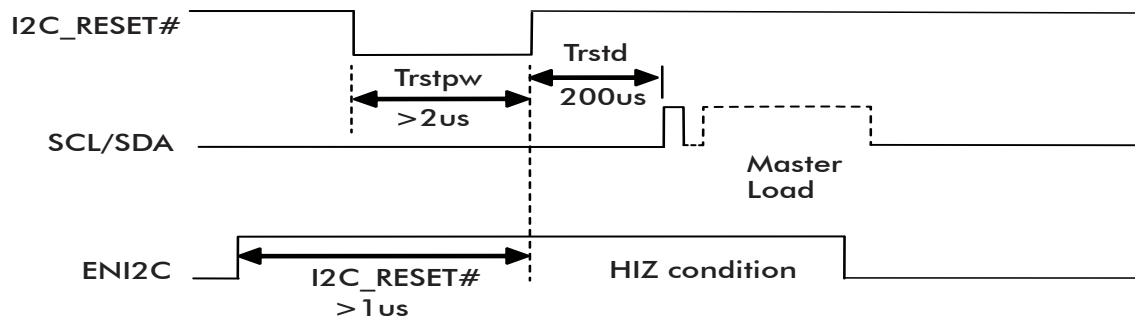
**BYTE 7**

Bit	Type	Power up condition	Description	Control affected	Comment
7:0	Reserved				

## 5.2 I2C Operation

The integrated I2C interface operates as a slave device mode. Standard I2C mode (100 Kbps) is supported with 7-bit addressing and data byte format 8-bit.

The device supports Read/Write. The bytes must be accessed in sequential order from the lowest to the highest byte with the ability to stop after any complete byte has been transferred. Address bits A3 to A0 are programmable to support multiple chips environment. The Data is loaded until a Stop sequence is issued.



**Figure 5-1 I2C Reset, Enable and SCL/SDA Timing Diagram**

### Transferring Data

Every byte put on the SDA line must be 8-bit long. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (see the I2C Data Transfer diagram). It will never hold the clock line SCL LOW to force the master into a wait state.

### Acknowledge

Data transfer with acknowledge is required from the master. When the master releases the SDA line (HIGH) during the acknowledge clock pulse, it will pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse as indicated in the I2C Data Transfer diagram. It will generate an acknowledge after each byte has been received.

### Data Transfer

A data transfer cycle begins with the master issuing a start bit. After recognizing a start bit, it will watch the next byte of information for a match with its address setting. When a match is found it will respond with a read or write of data on the following clocks. Each byte must be followed by an acknowledge bit, except for the last byte of a read cycle which ends with a stop bit. Data is transferred with the most significant bit (MSB) first.

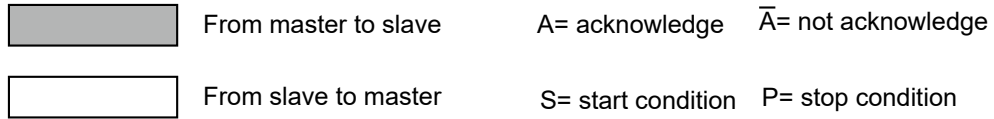
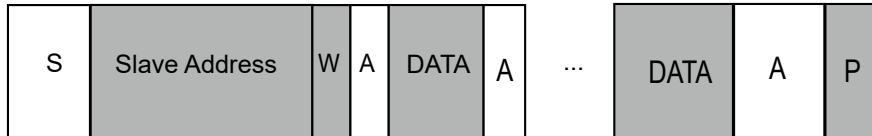
### Start & Stop Conditions

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

Read Sequence



Write Sequence



**Figure 5-2 I2C Read / Write Timing Sequence**

## 6. Electrical Specification

### 6.1 Absolute Maximum Ratings

Supply Voltage to Ground Potential.....	-0.5 V to +4.6 V
DC SIG Voltage.....	-0.5 V to +4.6 V
Output Current.....	-25 mA to +25 mA
Power Dissipation Continuous.....	1.63 W
ESD, HBM.....	-2 kV to +2 kV
Storage Temperature.....	-65 °C to +150 °C
Maximum Junction temperature.....	125 °C

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### 6.2 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

Parameter	Min.	Typ.	Max	Units
Power supply voltage (VDD to GND)	3.0	3.3	3.6	V
Supply Noise Tolerance (from 100KHz to 10MHz)		100		mVp-p
Operating free-air temperature (TA)	Commercial Temperature		70	°C
	Industrial Temperature		-40 <sup>(1)</sup>	85 °C

Note:

(1) I-temp is design guarantee, not production tested.

### 6.3 Power Consumption

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V <sub>DD</sub>	Power supply voltage		3.0	3.3	3.6	V
I <sub>DD</sub>	Operation power supply current	SW[1:0]=10 ( 1.2V <sub>DIFF</sub> swing @8Gbps, 0dB pre-emphasis)		243	290	mA
I <sub>DDQ</sub>	Standby power supply current	All other control pins are open. Disabled I2C master mode & I2C internal clock		0.2	1	mA

Note: Power consumption varies with the different Gain / Output Swing (-1dB Compression Point) setting.

Control Setting	Gain (dB)	Voltage Swing Limit (mV)	IDD(mA)
FG/SW=0000	-3.5	920	211
FG/SW=0001	-3.5	1040	228
FG/SW=0010	-3.5	1280	245
FG/SW=0100	-2.5	920	263
FG/SW=0101	-2.5	1040	228
FG/SW=0110	-2.5	1280	245
FG/SW=1000	+0.5	920	211

Control Setting	Gain (dB)	Voltage Swing limit (mV)	IDD(mA)
FG/SW=1000	+0.5	920	211
FG/SW=1001	+0.5	1040	223
FG/SW=1010	+0.5	1280	244
FG/SW=1100	+2.5	920	210
FG/SW=1101	+2.5	1040	226
FG/SW=1110	+2.5	1280	243

## 6.4 AC/DC Characteristics

### 6.4.1 LVCMOS I/O DC Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V <sub>IH</sub>	DC input logic HIGH		VDD/2+0.7		VDD+0.3	V
V <sub>IL</sub>	DC input logic LOW		-0.3		VDD/2-0.7	V
V <sub>OH</sub>	At IOH = -200 μA		VDD+0.2			V
V <sub>OL</sub>	At IOL = -200 μA				0.2	V
V <sub>HYS</sub>	Hysteresis of Schmitt trigger input		0.8			V

### 6.4.2 Main Link Differential

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C <sub>RX</sub>	RX AC coupling capacitance			220		nF
S11	Input return loss <sup>(2)</sup>	10 MHz to 4.1 GHz differential		-13.0		dB
		1 GHz to 4.1 GHz common mode		-5.0		
S22	Output return loss <sup>(2)</sup>	10 MHz to 4.1 GHz differential		-15		dB
		1 GHz to 4.1 GHz common mode		-6.0		
R <sub>IN</sub>	DC single-ended input impedance			50		Ω
	DC Differential Input Impedance			100		
R <sub>OUT</sub>	DC single-ended output impedance			50		Ω
	DC Differential output Impedance			100		
Z <sub>RX-HIZ</sub>	DC input impedance during reset or power down			200		kΩ
V <sub>RX-DIFFp-p</sub>	Peak to peak differential input voltage	For HBR3		0.2 <sup>(1)</sup>	1.2	Vppd
	Input Source common-mode noise	DC - 200MHz			150	mVpp
t <sub>PD</sub>	Latency	From input to output		0.5		ns
G <sub>p</sub>	Peaking gain: Compensation at 4 GHz, relative to 100 MHz, 100 mVp-p sine wave input	EQ[3:0] = 1111		10.4		dB
		EQ[3:0] = 1000		7.8		
		EQ[3:0] = 0000		3.9		
		Variation around typical	-3		+3	dB
G <sub>F-gain</sub>	Flat gain: 100 MHz, EQ[3:0] = 1000, SW[1:0] = 10	FG[1:0] = 11		+2.5		dB
		FG[1:0] = 10		0.5		
		FG[1:0] = 01		-1.5		
		FG[1:0] = 00		-3.5		
		Variation around typical	-3		+3	dB
	Frequency Response Gain curve 1-5GHz with 18-inch FR4, FG=10		Pls refer the Freq/Gain curve below			dB

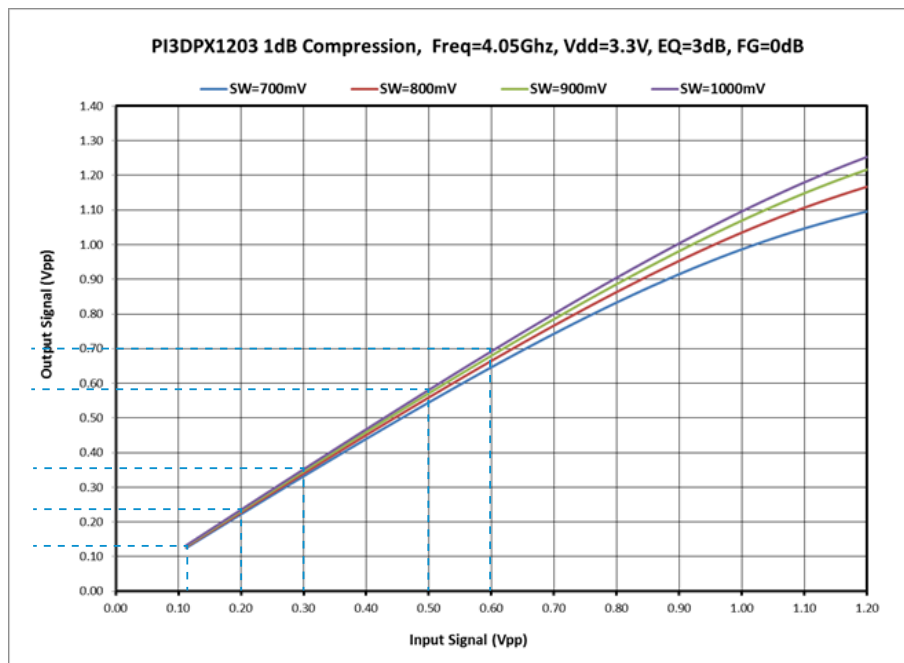
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{1dB\_100M}$	-1 dB compression point of output swing (at 100 MHz)	SW[1:0] = 11 SW[1:0] = 10 SW[1:0] = 01 SW[1:0] = 00		1370 1280 1040 920		mVppd
$V_{Coup}$	Channel isolation (Note 1)	100MHz to 4GHz		25		dB
$V_{noise\_input}$	Input-referred noise	100MHz to 4GHz, FG<1:0> = 11, EQ<3:0> = 0000		0.5		$mV_{RMS}$
		100MHz to 4GHz, FG<1:0> = 11, EQ<3:0> = 1010		0.4		
$V_{noise\_out-put}$	Output-referred noise (Note 2)	100MHz to 4GHz, FG<1:0> = 11, EQ<3:0> = 0000		0.7		$mV_{RMS}$
		100MHz to 4GHz, FG<1:0> = 11, EQ<3:0> = 1010		0.8	1.6	
	Deterministic Jitter	Data Rate = 8Gbps FGx[1:0] = 10		EQ = 0000 EQ = 1010 EQ = 1111		UIp-p

Note:

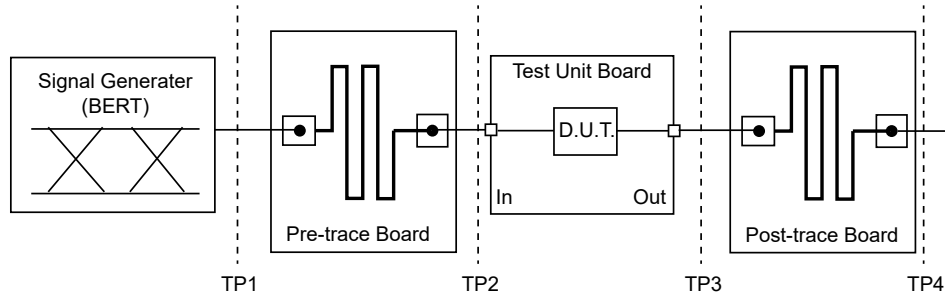
(1) Channel Isolation measured using a vector-network analyzer (VNA) with -15dBm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.

(2) Guaranteed by design and characterization.

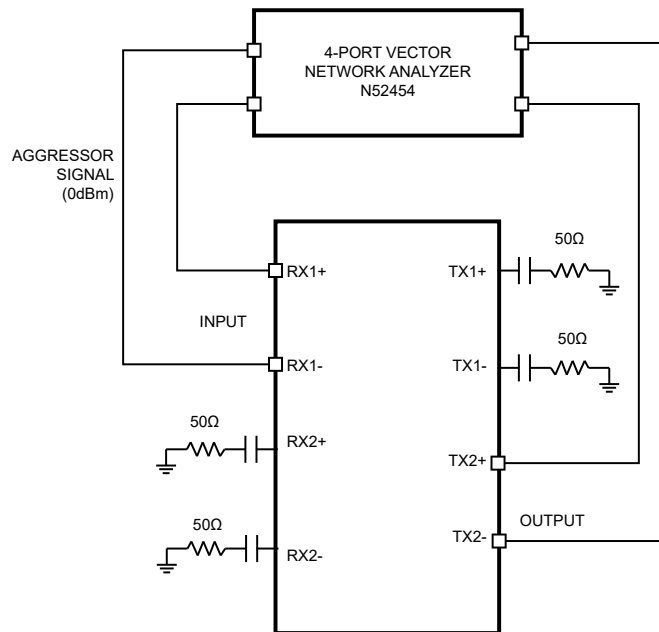
(3) Please refer more data in the VIN / VOUT plot. VOUT changes with the EQ and FG setting. Both the ReDriver and the Sink device system should be carefully designed to ensure sink-device compliance.



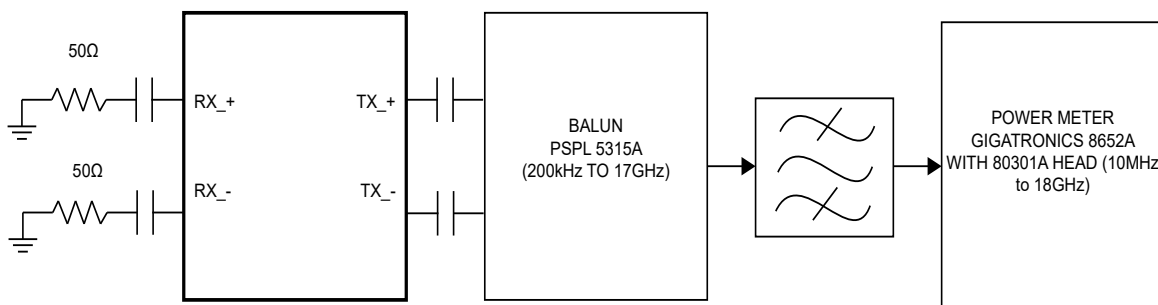
**Figure 6-1 1dB Compression(Voltage Sweep) between 0 to 600mV Inputs @ 8Gbps**



**Figure 6-2 AC Electrical Measurement Test Setup**



**Figure 6-3 Channel-Isolation Test Configuration**

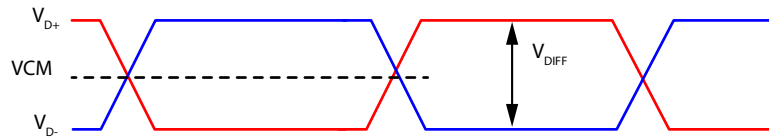


**Figure 6-4 Noise Test Configuration**

Common Mode Voltage

$$V_{CM} = (|V_{D+} + V_{D-}| / 2)$$

$$V_{CMP} = (\max |V_{D+} + V_{D-}| / 2)$$



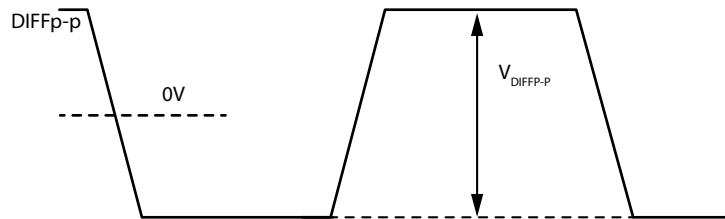
$V_{D+} - V_{D-}$

Symmetric Differential Swing

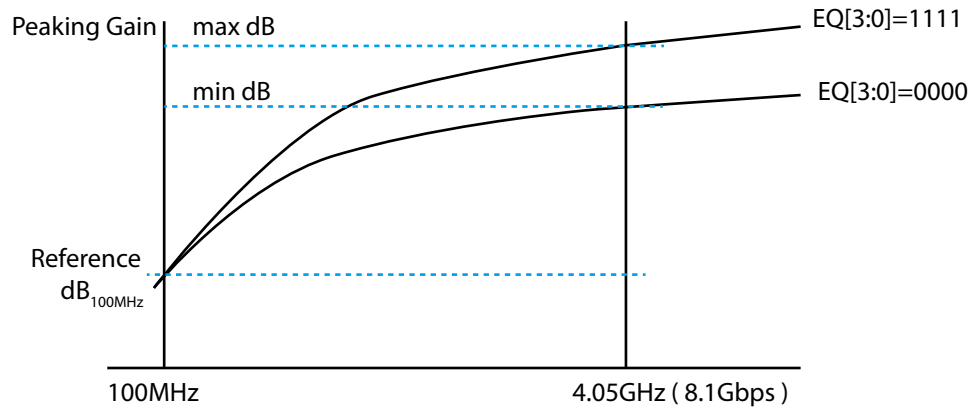
$$V_{DIFFP-P} = (2 * \max |V_{D+} - V_{D-}|)$$

Asymmetric Differential Swing

$$V_{DIFFP-P} = (\max |V_{D+} - V_{D-}| \{V_{D+} > V_{D-}\} + \max |V_{D+} - V_{D-}| \{V_{D+} < V_{D-}\})$$



**Figure 6-5 Definition of Differential Voltage and Differential Voltage Peak-to-Peak**



**Figure 6-6 Definition of Peaking Gain relative to 100 MHz, 100 mVp-p sine wave input**

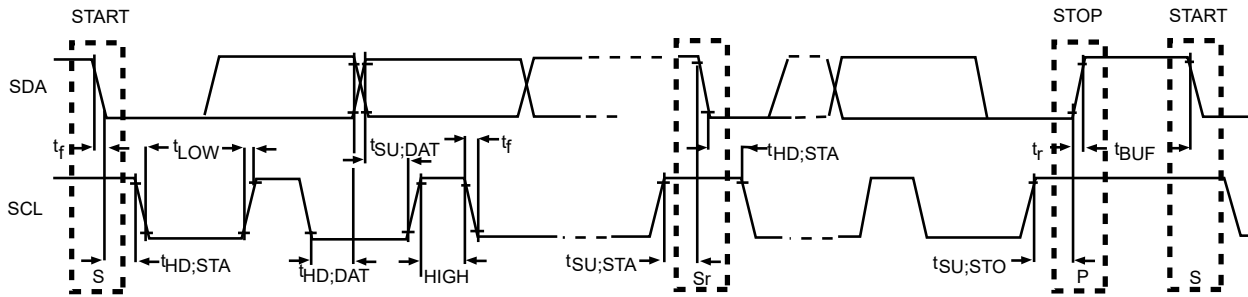
### 6.4.3 SCL/SDA Specification for I2C BUS

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
SDA and SCL I/O for I2C-bus						
$V_{DD}$	Nominal Bus Voltage		3.0		3.6	V
$V_{IH}$	DC input logic HIGH		$V_{DD}/2 + 0.7$		$V_{DD} + 0.3$	V
$V_{IL}$	DC input logic LOW		-0.3		$V_{DD}/2 - 0.7$	V
$V_{OL}$	DC output logic LOW	$I_{OL} = 3mA$			0.4	V
$t_{OF}$	Output fall time from $V_{IHmin}$ to $V_{ILmax}$ with bus cap. 10-400pF				250	ns
AC/DC Specifications - SCL/SDA for I2C BUS						
$I_{PU}$	Current Through Pull-Up Resistor or Current Source	High Power specification	3.0		3.6	mA
$I_{leak-bus}$	Input leakage per bus segment		-200		200	uA
$I_{leak-pin}$	Input leakage per device pin			-15		uA
CI	Capacitance for SDA/SCL				10	pF
$f_{SCLK}$	Bus Operation Frequency			100		KHz
$t_{BUF}$	"Bus Free Time Between Stop and Start condition"		1.3			us
$t_{HD:STA}$	Hold time after (Repeated) Start condition. After this period, the first clock is generated.	At $I_{pull-up}$ , Max	0.6			us
$t_{SU:STA}$	Repeated start condition setup time		0.6			us
$t_{SU:STO}$	Stop condition setup time		0.6			us
$t_{HD:DAT}$	Data hold time		0			ns
$t_{SU:DAT}$	Data setup time		100			ns
$t_{LOW}$	Clock Low period		1.3			us
$t_{HIGH}$	Clock High period		0.6		50	us
$t_F$	Clock/Data fall time				300	ns
$t_R$	Clock/Data rise time				300	ns
$t_{POR}$	"Time in which a device must be operation after power-on reset"				500	ms

Note:

- (1) Recommended value.
- (2) Recommended maximum capacitance load per bus segment is 400pF.
- (3) Compliant to I2C physical layer specification.
- (4) Ensured by Design. Parameter not tested in production.

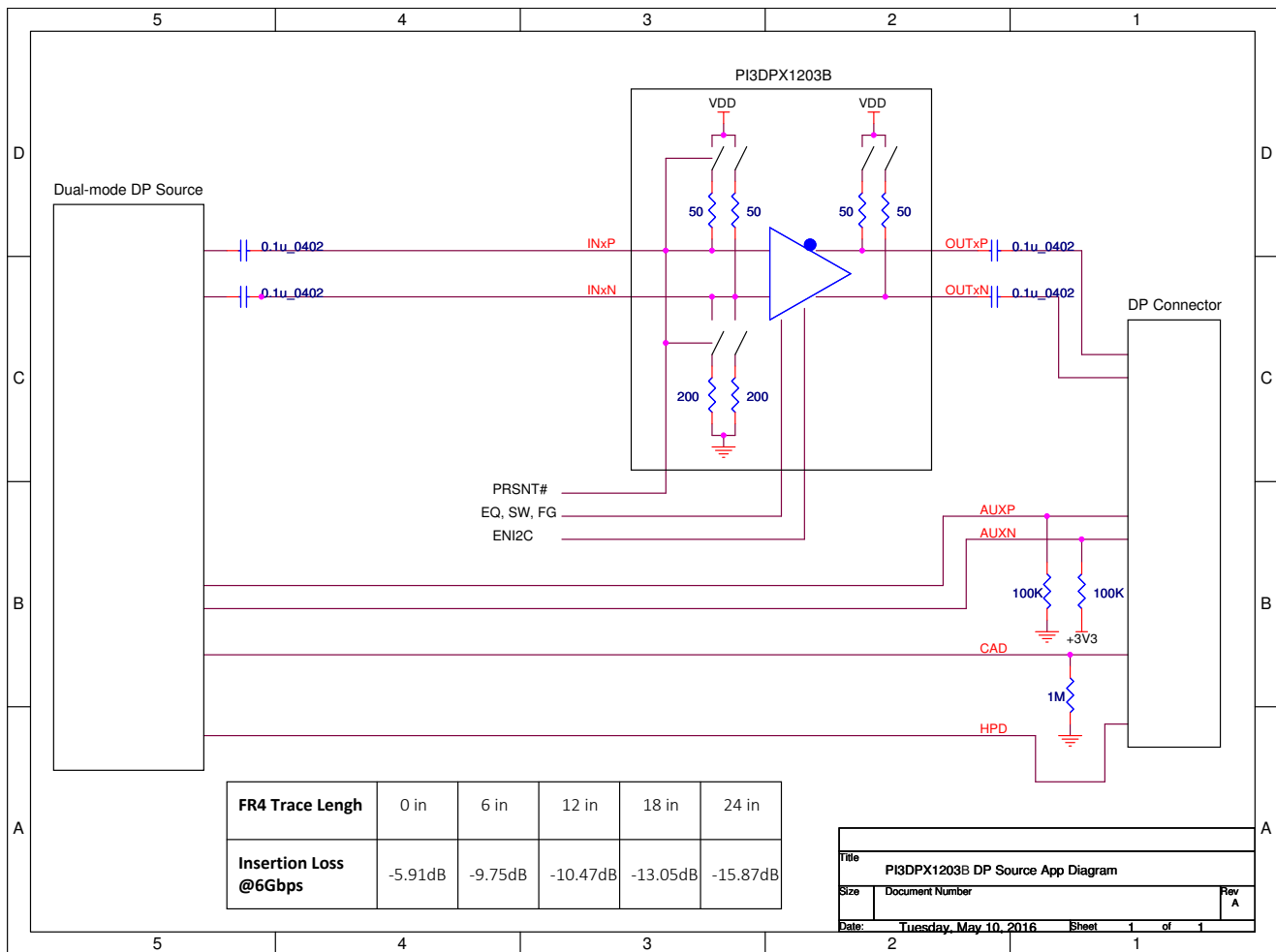


**Figure 6-7 I<sup>2</sup>C Timing Diagram**

## 7. Applications

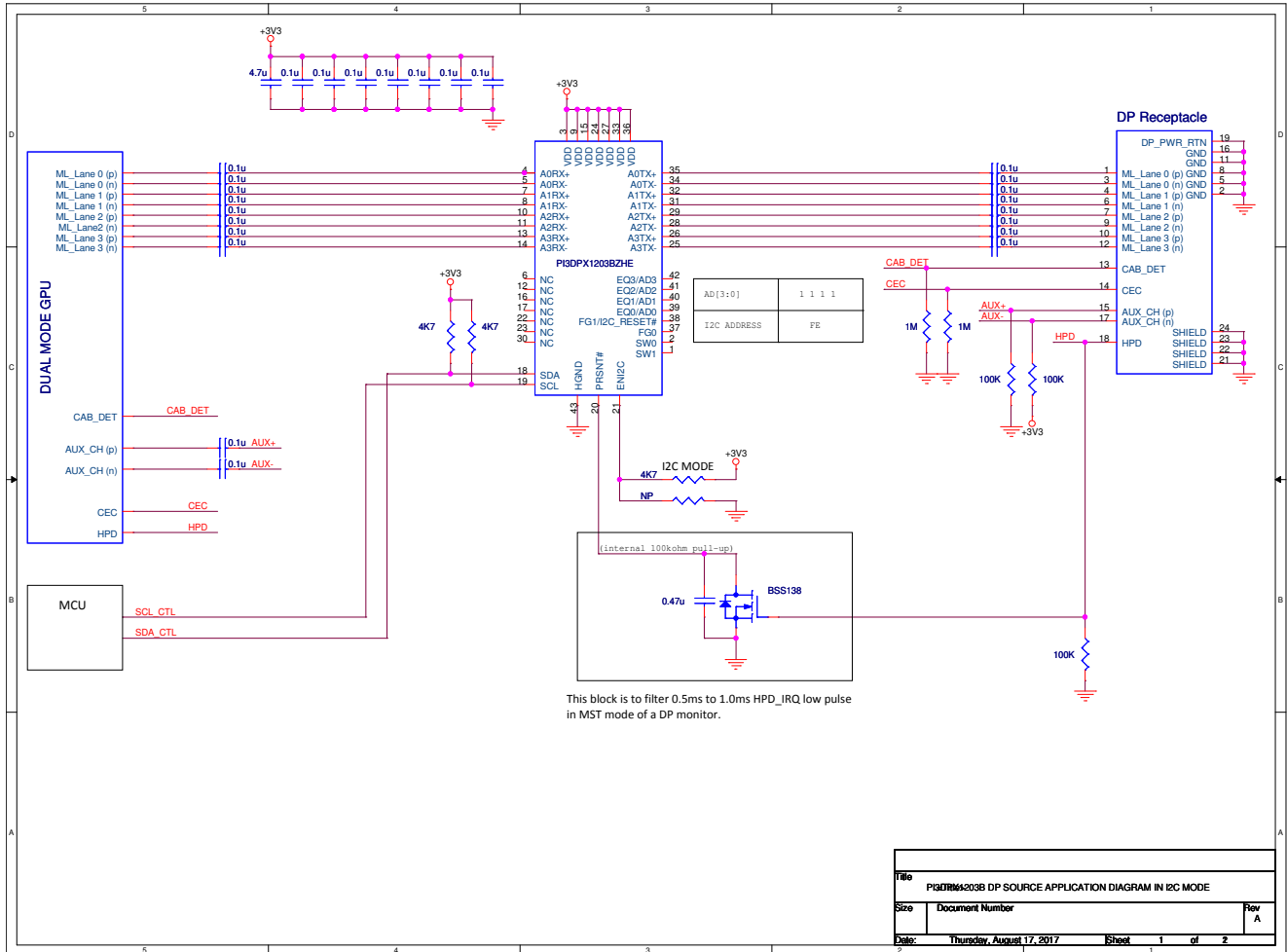
### 7.1 Reference Schematic

- Determine the loss profile between transmitter and receiver.
- Based upon the loss profile and signal swing, determine the optimal equalization settings.
- Select appropriate voltage output swing.
- If required, select the correct differential pair polarity.
- To set voltage logic levels on configuration pins, use a 5-kΩ pull-up for high level, tie pin to GND for low level, and place a 5-kΩ pull-up and 5-kΩ pull-down for HiZ.



**Figure 7-1 Source side DP Redriver Connection Diagram**

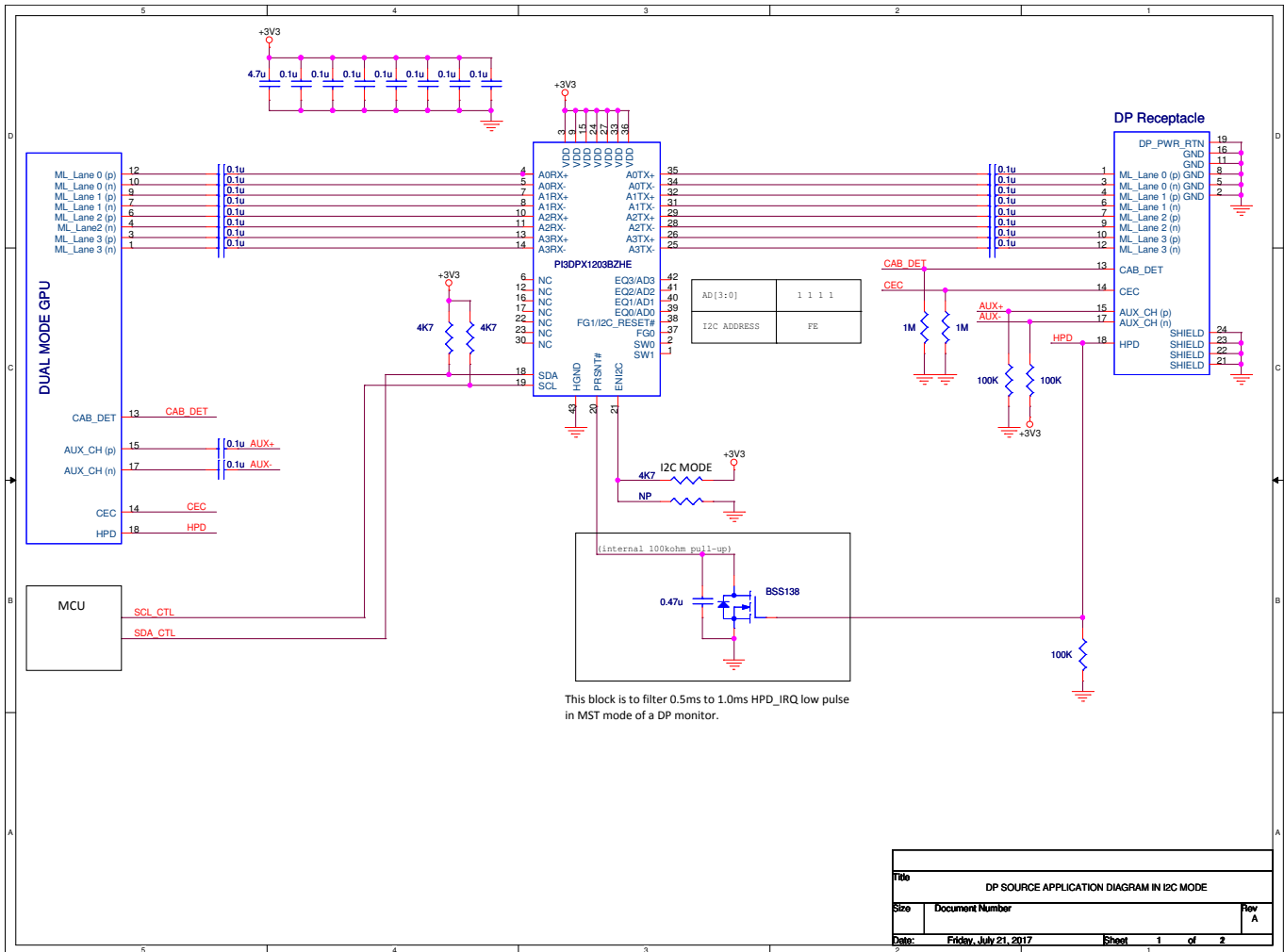
**7.2 Reference Schematic for HPD\_IRQ MST Mode**



**Figure 7-2 DP Source Application in Pin Mode**

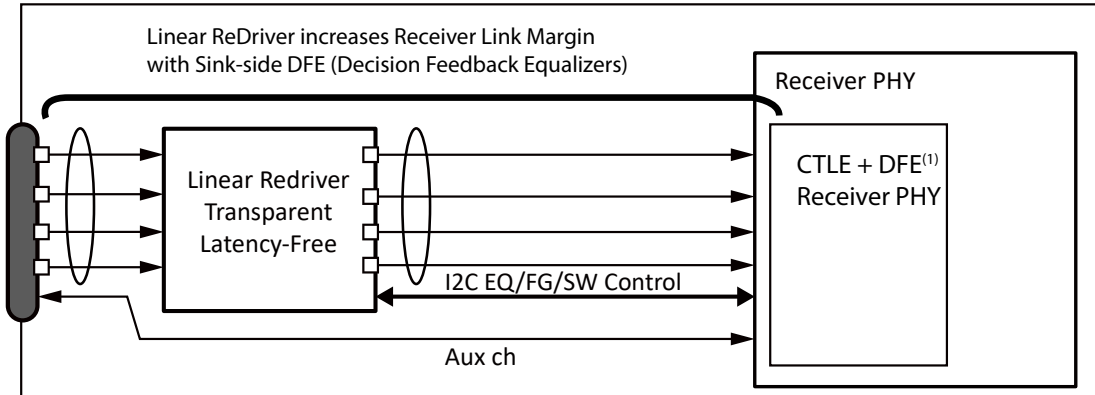
File		
PI3DPX1203B DP SOURCE APPLICATION DIAGRAM IN I2C MODE		
Size	Document Number	Rev A
Date:	Thursday, August 17, 2017	Sheet 1 of 2

**PI3DPX1203B**



**Figure 7-3 DP Source Application in I2C Mode**

### 7.3 Sink-side Application



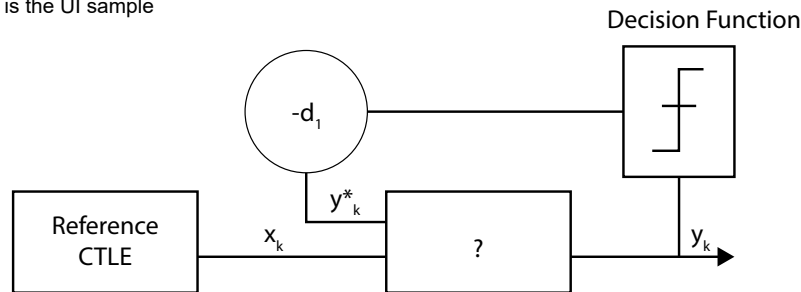
Note

(1) The HBR3 receiver equalizer includes a CTLE cascaded with a one-tap adaptive DFE with a feedback coefficient limited to < 50mV. The DFE behavior is described below.

$$y_k = x_k - d_1 * \text{sgn}(y_k - 1)$$

where:

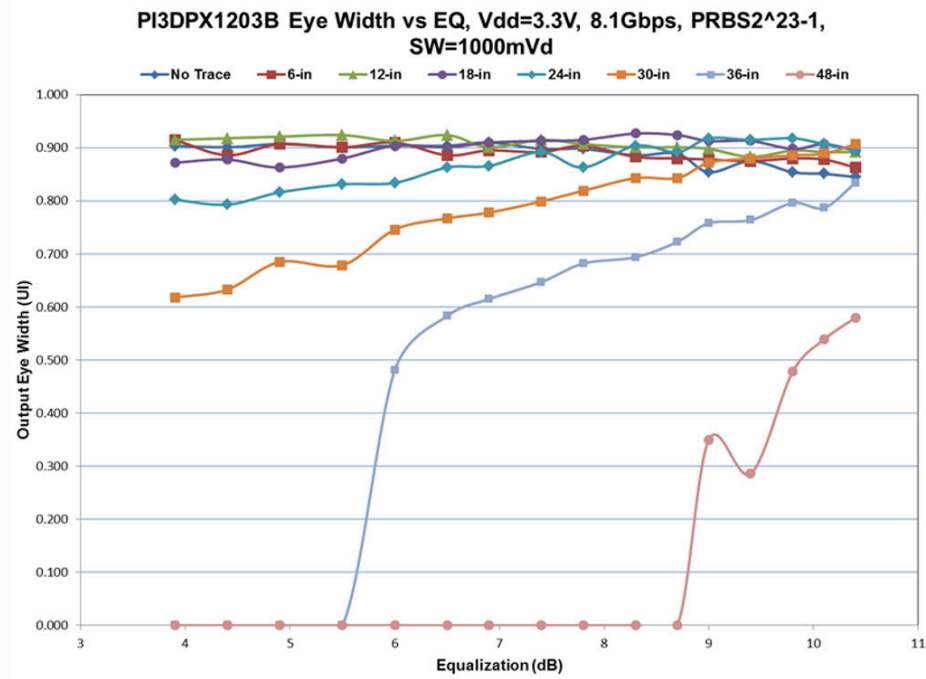
- $y_k$  is the DFE differential output voltage
- $y_k^*$  is the decision function output voltage
- $x_k$  is the differential input voltage after CTLE
- $d_1$  is the feedback coefficient
- $k$  is the UI sample



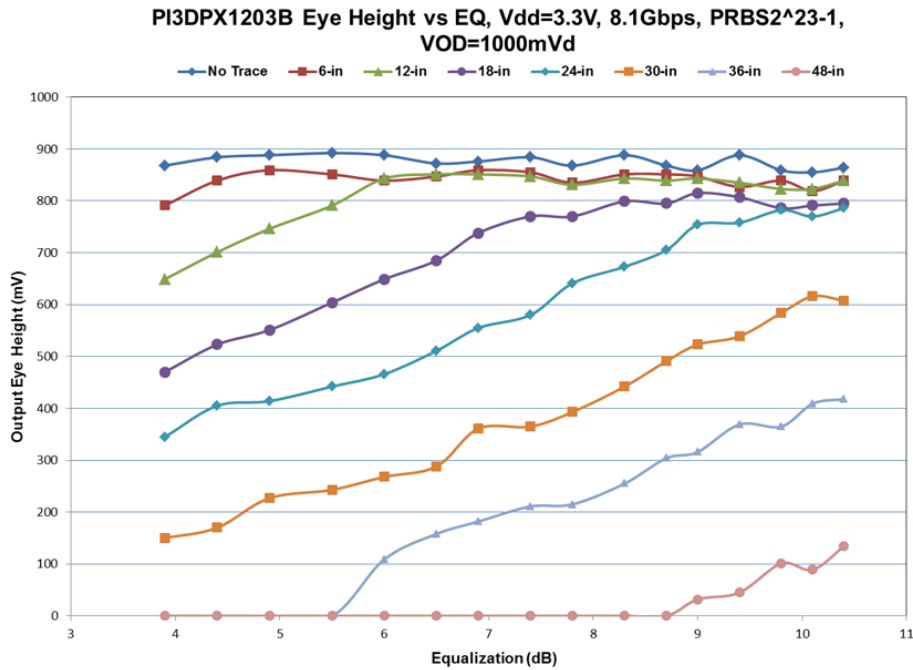
Reference HBR3 Receiver Equalizer DFE

**Figure 7-4 Linear Redriver Linking with Sink-side Receiver CTLE+DFE**

**7.4 Output Swing and Gain Information**



**Figure 7-5 Eye Width vs EQ, Output\_Swing =1000mV, Gain=+0.5dB (Input Swing=1000mVd)**

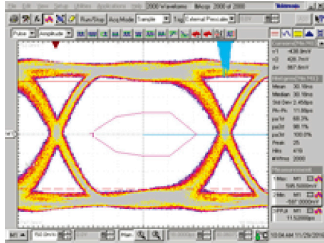


**Figure 7-6 Eye Height vs EQ, Output Swing =1000mV, Gain=+2.5dB (Vin =800mVdiff)**

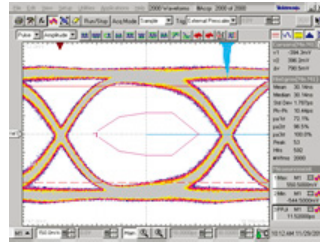
### 7.5 Output Eye diagram, Trace length and EQ

Condition: Output Eye Opening with Input Equalization, 8.1 Gbps, Vdd=3.3V, 25C, Using PRBS 2<sup>23</sup>-1 pattern, Input Swing=800mVd, Output Swing= 1000mV

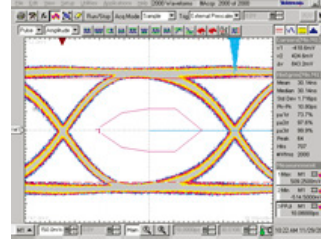
No Trace, EQ=3.9dB



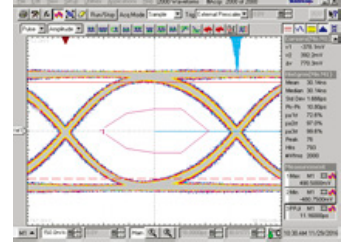
6-in, EQ=3.9dB



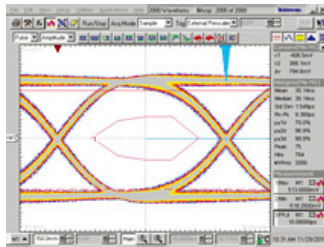
12-in, EQ = 6.0dB



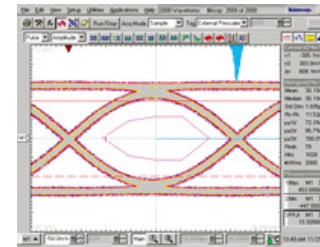
18-in, EQ=7.4dB



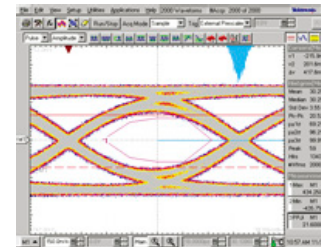
24-in, EQ=8.7dB



30-in, EQ = 10.4dB



36-in, EQ= 10.4dB

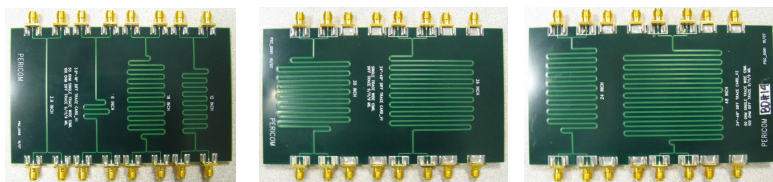


**Figure 7-7 Output Eye Diagram at FG 0.5dB**

Note:

Table 7-1. Trace card insertion loss profile is shown below.

Frequency	3 GHz	6GHz	Units
6 inch Input Trace	-1.43	-4	dB
12 inch Input Trace	-6.1	-11	dB
18 inch Input Trace	-8.34	-15	dB
30 inch Input Trace	-10.14	-18	dB
36 inch Input Trace	-12.13	-22	dB
48 inch Input Trace	-16.42	-29	dB



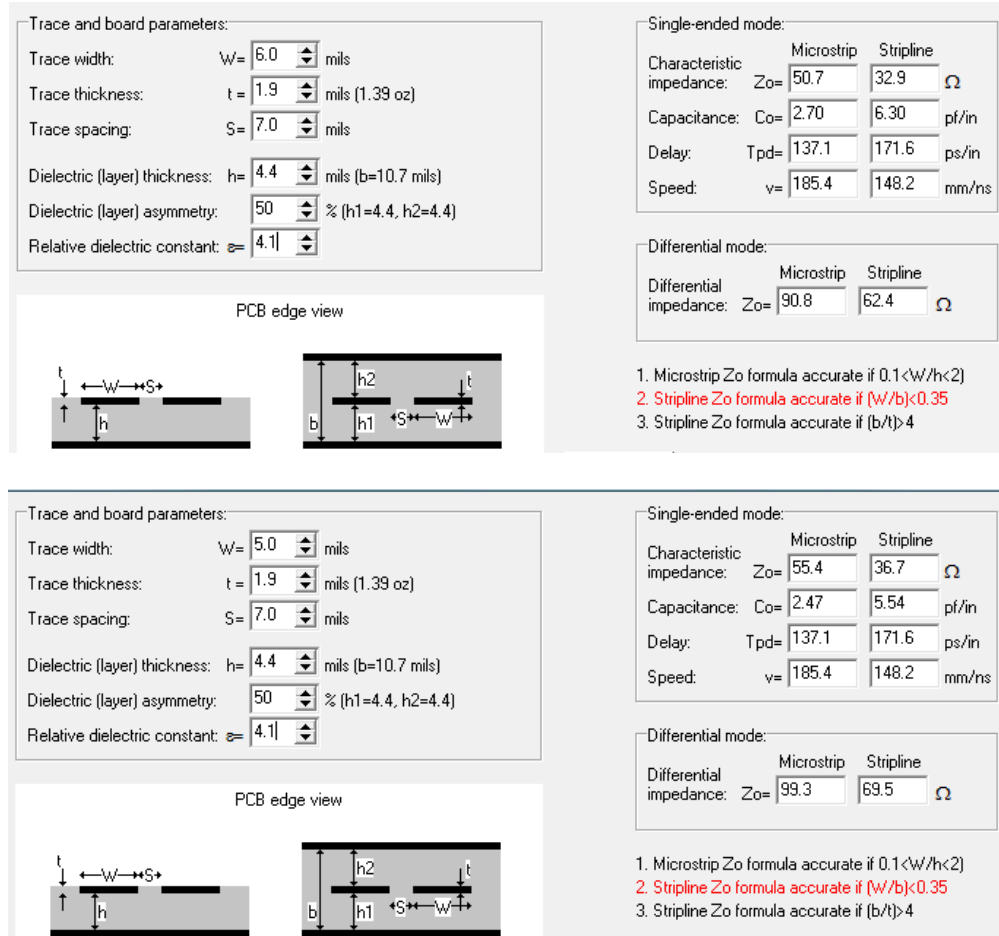
**Figure 7-8 Trace Board Photo**



### 7.7 High-speed signal Routing

Well-designed layout is essential to prevent signal reflection:

- For 90Ω differential impedance, width-spacing-width micro-strip of 6-7-6 mils is recommended; for 100Ω differential impedance, width-spacing-width micro-strip of 5-7-5 mils is recommended.
- Differential impedance tolerance is targeted at ±15%.



**Figure 7-10 Trace Width and Clearance of Micro-strip and Strip-line**

- For micro-strip, using 1/2oz Cu is fine. For strip-line in 6+ PCB layers, 1oz Cu is more preferable.

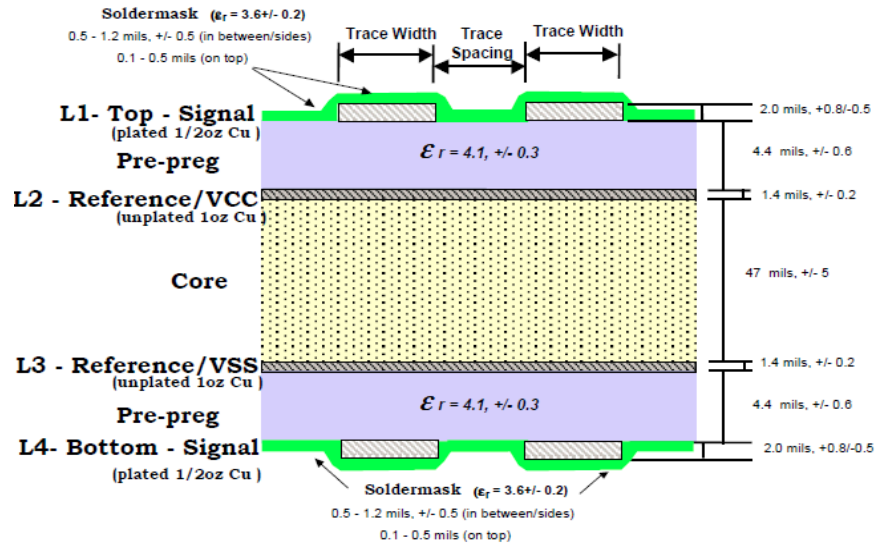


Figure 7-11 4-Layer PCB Stack-up Example

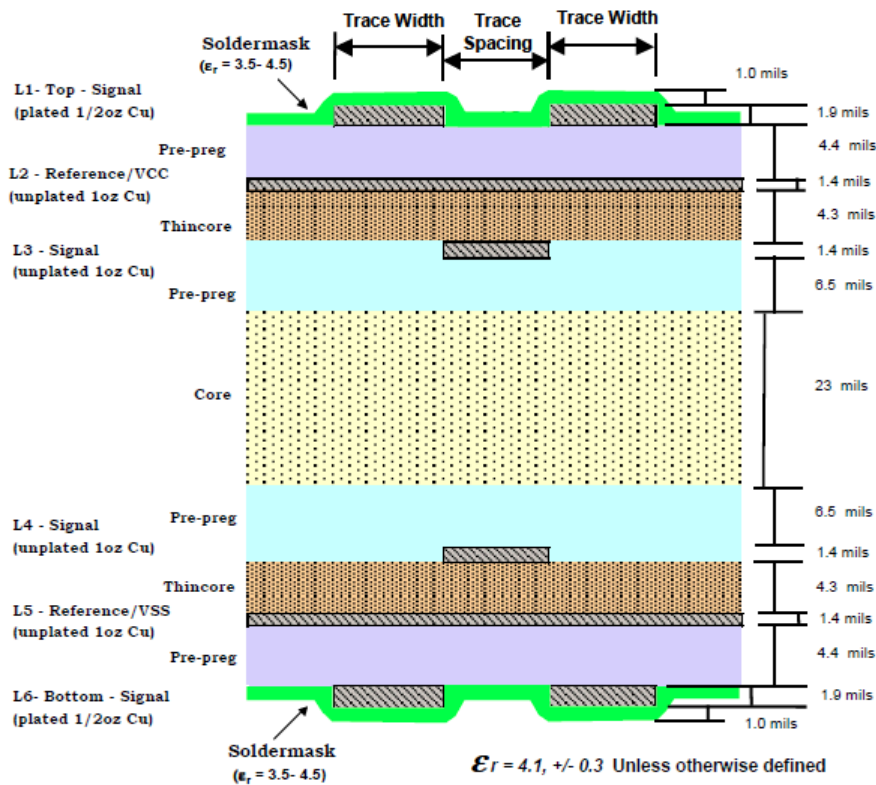
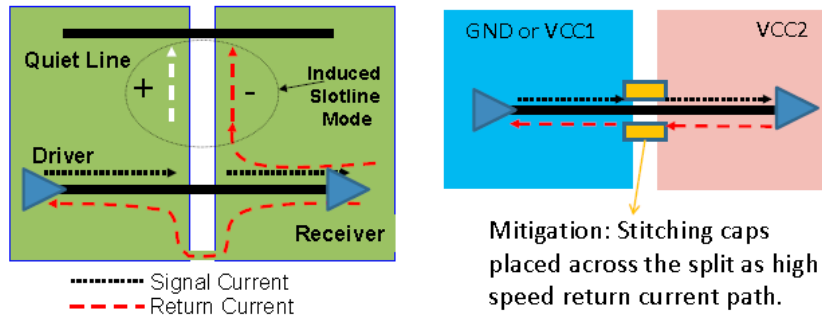


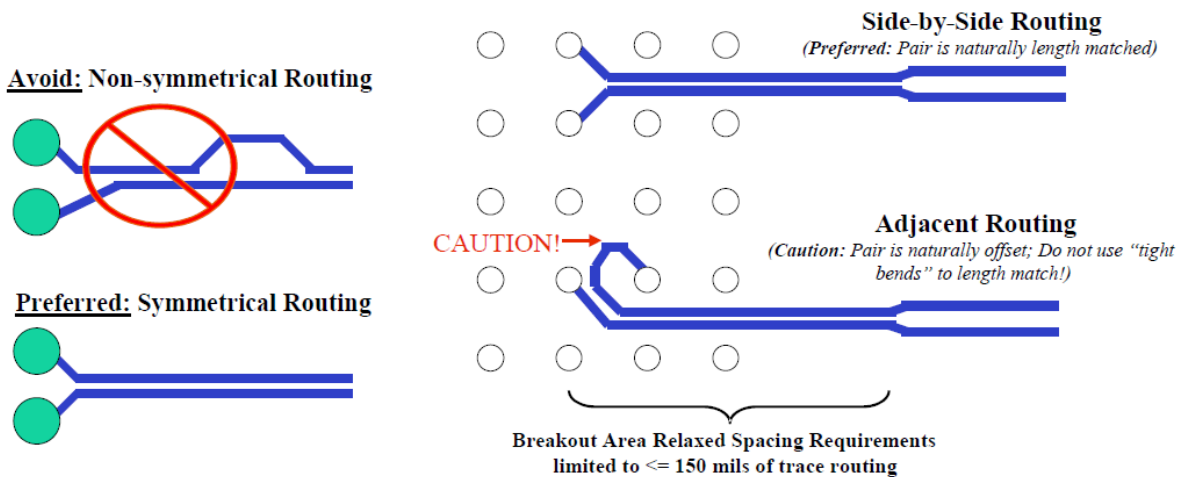
Figure 7-12 6-Layer PCB Stack-up Example

- Ground referencing is highly recommended. If unavoidable, stitching capacitors of 0.1uF should be placed when reference plane is changed.



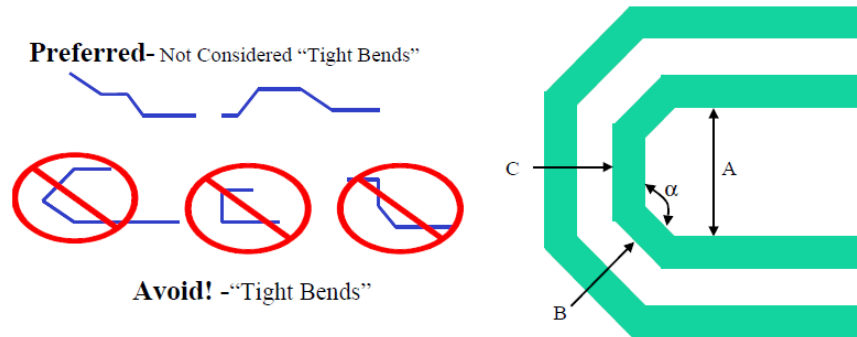
**Figure 7-13** Stitching Capacitor Placement

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.
- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.



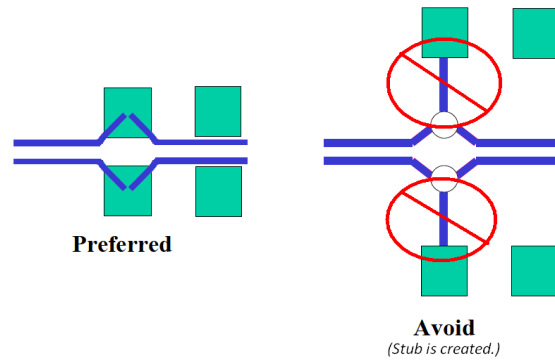
**Figure 7-14** Layout Guidance of Matched Differential Pair

- For minimal crosstalk, inter-pair spacing between two differential micro-strip pairs should be at least 20 mils or 4 times the dielectric thickness of the PCB.
- Wider trace width of each differential pair is recommended in order to minimize the loss, especially for long routing. More consistent PCB impedance can be achieved by a PCB vendor if trace is wider.
- Differential signals should be routed away from noise sources and other switching signals on the printed circuit board.
- To minimize signal loss and jitter, tight bend is not recommended. All angles  $\alpha$  should be at least 135 degrees. The inner air gap A should be at least 4 times the dielectric thickness of the PCB.



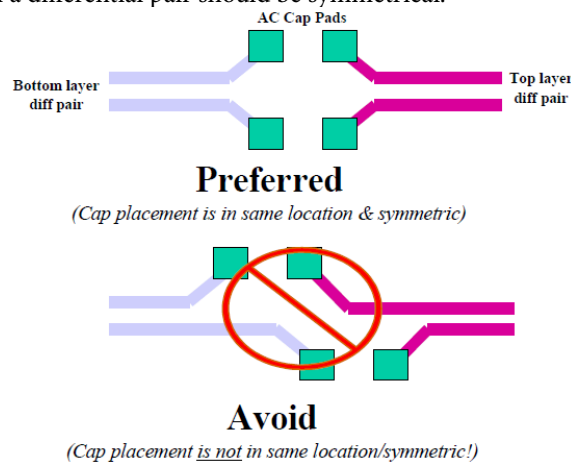
**Figure 7-15 Layout Guidance of Bends**

- Stub creation should be avoided when placing shunt components on a differential pair.



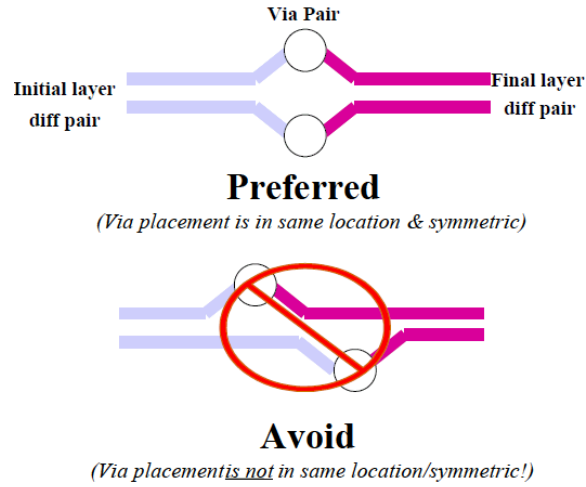
**Figure 7-16 Layout Guidance of Shunt Component**

- Placement of series components on a differential pair should be symmetrical.



**Figure 7-17 Layout Guidance of Series Component**

- Stitching vias or test points must be used sparingly and placed symmetrically on a differential pair.

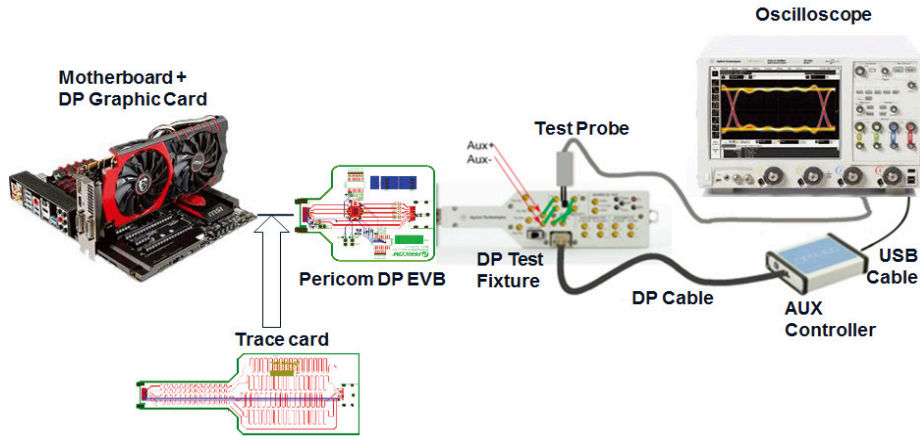


**Figure 7-18 Layout Guidance of Stitching Via**

## 7.8 CTS Compliant Test Report

### 7.8.1 Test setup Information

Internal DisplayPort test setup is shown below for the reference.



**Figure 7-19 Displayport test set-up**

**Table 7-2. CTS Trace card insertion loss information**

DP FR4 trace	0 in	6 in	12 in	18 in	24 in	30 in	36 in
Insertion loss @ 8.1Gbps	-8.15 dB	-11.52 dB	-14.88 dB	-17.60 dB	-19.94 dB	-22.92 dB	-28.62 dB

7.8.2 Compliance Test Report

# Test Report

Overall Result: **PASS**

Test Configuration Details	
Device Description	
Test Specification	1.4
Lane	4 Lanes
SSC	Disabled
Test Session Details	
DisplayPort Test Controller	UnigrafDPTC
Fixture Type	Other
Infiniium SW Version	05.70.00901
Infiniium Model Number	DSOX92504A
Infiniium Serial Number	MY54410104
Application SW Version	3.52.0001
Debug Mode Used	No
Compliance Limits (official)	DisplayPort Compliance Test Specification Version 1.4 Official Test Limit
Probe (Channel 1)	Model: N2801A Serial: US54094067 Head: N5444A Atten: Calibrated (5 JUN 2017 09:48:34), Using Cal Atten (5.6383E+000) Skew: Calibrated (5 JUN 2017 09:48:45), Using Cal Skew
Probe (Channel 2)	Model: N2801A Serial: US54094054 Head: N5444A Atten: Calibrated (5 JUN 2017 09:50:19), Using Cal Atten (5.4968E+000) Skew: Calibrated (5 JUN 2017 09:50:31), Using Cal Skew
Probe (Channel 3)	Model: N2801A Serial: US54094059 Head: N5444A Atten: Calibrated (5 JUN 2017 09:51:30), Using Cal Atten (5.6826E+000) Skew: Calibrated (5 JUN 2017 09:51:40), Using Cal Skew
Probe (Channel 4)	Model: N2801A Serial: US54094057 Head: N5444A Atten: Calibrated (5 JUN 2017 09:52:22), Using Cal Atten (5.5321E+000) Skew: Calibrated (5 JUN 2017 09:52:33), Using Cal Skew
Last Test Date	2017-06-09 15:08:51 UTC +08:00

Figure 7-20 DP1.4 Compliance Test Report

### Summary of Results

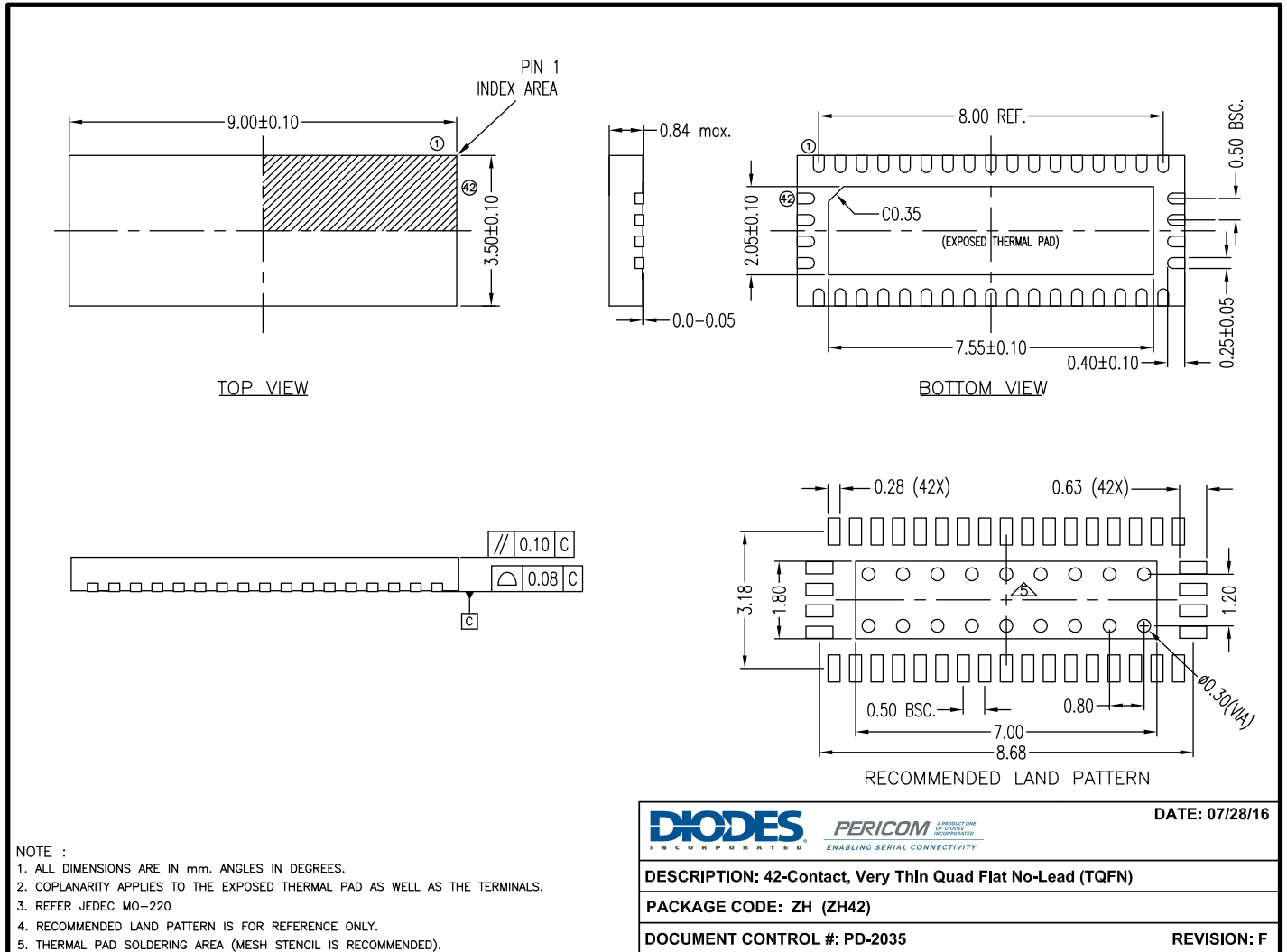
Test Statistics	
Failed	0
Passed	15
Total	15

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Worst Actual	Worst Margin	Pass Limits
✓	0	2	3.1 Lane 3 - Eye Diagram Test (TP3_EQ) (HBR2 and HBR3) - HBR2CPAT	0.000	50.0 %	-500 m <= VALUE <
✓	0	1	3.1 Lane 3 - Eye Diagram Test with No Cable Model (TP3_EQ) (HBR2 and HBR3) - HBR2CPAT	0.000	50.0 %	-500 m <= VALUE <
✓	0	2	3.12 Lane 3 - Total Jitter Test (TP3_EQ) (High Bit Rate 3) - HBR2CPAT	566.000 mUI	12.9 %	VALUE <= 650.000 mUI
✓	0	1	3.12 Lane 3 - Total Jitter Test with No Cable Model (TP3_EQ) (High Bit Rate 3) - HBR2CPAT	626.600 mUI	3.6 %	VALUE <= 650.000 mUI
✓	0	10	3.3 Lane 3 - Peak to Peak Voltage Test - PLTPAT	874 mV	36.7 %	VALUE <= 1.380 V
✓	0	1	3.2 Lane 3 - Non Pre-Emphasis Level Test (Swing 2/Swing 0) - PLTPAT	5.3748 dB	10.3 %	5.2000 dB <= VALUE <= 5.5496 dB
✓	0	1	3.2 Lane 3 - Non Pre-Emphasis Level Test (Swing 2/Swing 1) - PLTPAT	3.0294 dB	24.8 %	1.6000 dB <= VALUE <= 4.6488 dB
✓	0	4	3.3 Lane 3 - Pre-Emphasis Level Test (Pre-emphasis 0) - PLTPAT	-3.536 dB	151E+01 %	VALUE <= 250 mdB
✓	0	3	3.3 Lane 3 - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 0) - PLTPAT	2.021 dB	1.1 %	VALUE >= 2.000 dB
✓	0	1	3.3 Lane 3 - Non-Transition Voltage Range Measurement (Swing 2) - PLTPAT	1.007	42.2 %	VALUE >= 708 mV
✓	0	2	3.3 Lane 3 - Pre-Emphasis Level Delta Test (Pre-emphasis 2 to Pre-emphasis 1) - PLTPAT	2.304 dB	44.0 %	VALUE >= 1.600 dB
✓	0	1	3.3 Lane 3 - Non-Transition Voltage Range Measurement (Swing 1) - PLTPAT	1.037	46.5 %	VALUE >= 708 mV
✓	0	1	3.3 Lane 3 - Pre-Emphasis Level Delta Test (Pre-emphasis 3 to Pre-emphasis 2) - PLTPAT	1.874 dB	17.1 %	VALUE >= 1.600 dB

## 8. Mechanical/Packaging Information

### 8.1 Mechanical Outline

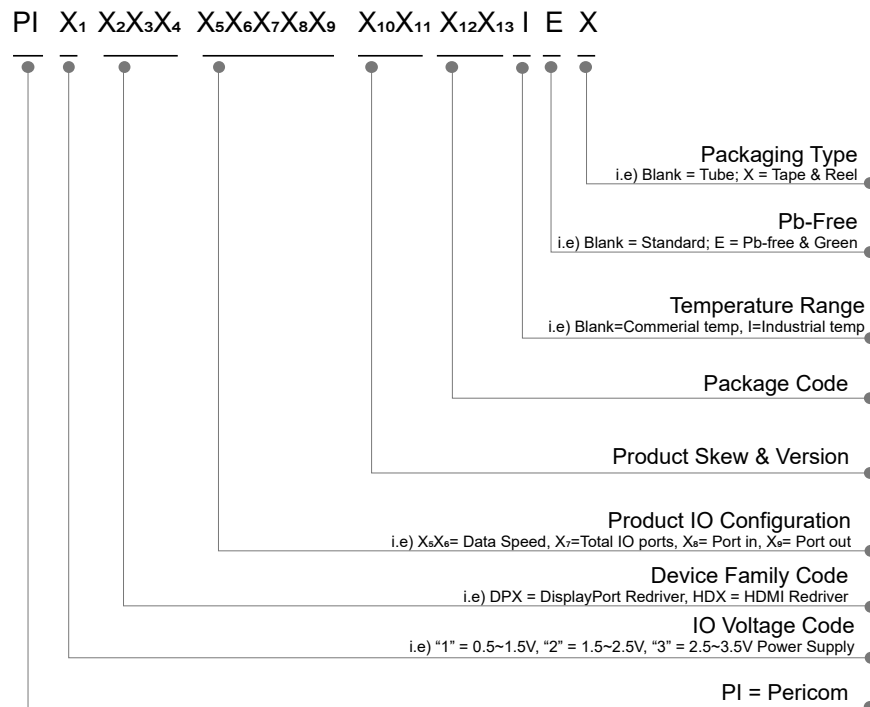


**Figure 8-1 42-contact TQFN (ZH42) Package Mechanical Drawing**

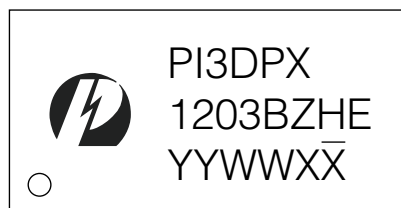


## 8.2 Part Marking Information

Product marking follows our standard part number ordering information.



**Figure 8-3 Part Number Information**



YY: Year  
 WW: Workweek  
 1st X: Assembly Code  
 2nd X: Fab Code

**Figure 8-4 Package Marketing Information**

### 8.3 Tape & Reel Materials and Design

#### 8.3.1 Carrier Tape

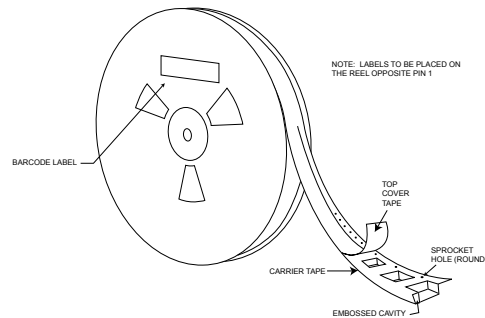
The Pocketed Carrier Tape is made of Conductive Polystyrene plus Carbon material (or equivalent). The surface resistivity is  $10^6 \Omega/\text{sq}$ . maximum. Pocket tapes are designed so that the component remains in position for automatic handling after cover tape is removed. Each pocket has a hole in the center for automated sensing if the pocket is occupied or not, thus facilitating device removal. Sprocket holes along the edge of the center tape enable direct feeding into automated board assembly equipment. See Figures 3 and 4 for carrier tape dimensions.

#### 8.3.2 Cover Tape

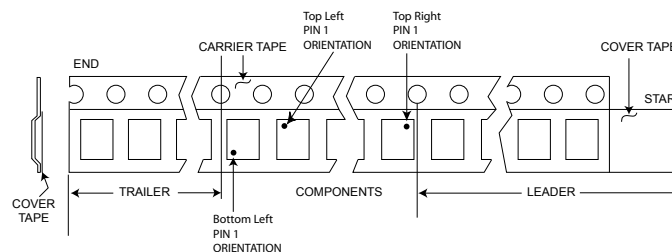
Cover tape is made of Anti-static Transparent Polyester film. The surface resistivity is  $10^7 \Omega/\text{sq}$ . Minimum to  $10^{11} \Omega/\text{sq}$ . maximum. The cover tape is heat-sealed to the edges of the carrier tape to encase the devices in the pockets. The force to peel back the cover tape from the carrier tape shall be a MEAN value of 20 to 80gm (2N to 0.8N).

#### 8.3.3 Reel

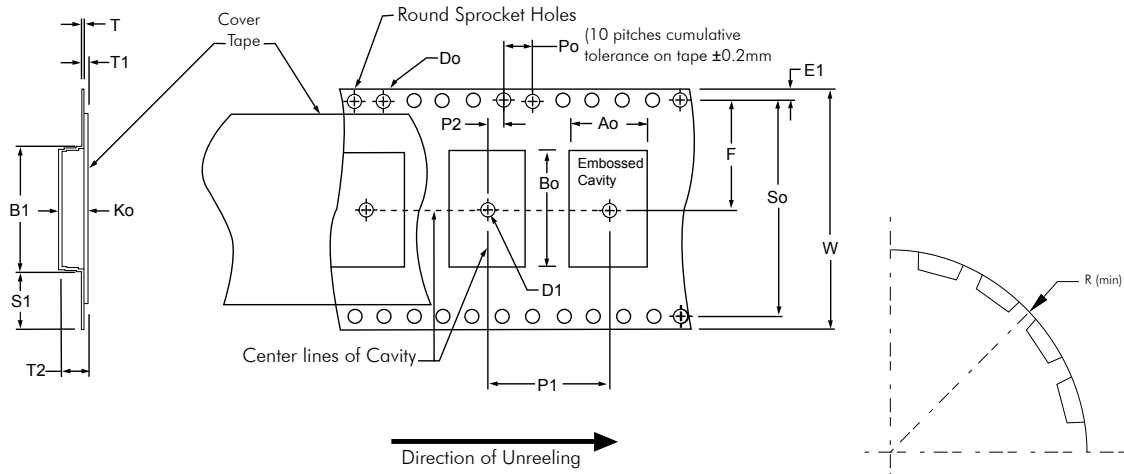
The device loading orientation is in compliance with EIA-481, current version (Figure 2). The loaded carrier tape is wound onto either a 13-inch reel, (Figure 4) or 7-inch reel. The reel is made of Anti-static High-Impact Polystyrene. The surface resistivity  $10^7 \Omega/\text{sq}$ . minimum to  $10^{11} \Omega/\text{sq}$ . max.



**Figure 8-5 Tape & Reel Label Information**



**Figure 8-6 Tape Leader and Trailer pin 1 Orientations**



**Figure 8-7 Standard Embossed Carrier Tape Dimensions**

**Table 8-1. Constant Dimensions**

Tape Size	D0	D1 (Min)	E1	P0	P2	R (See Note 2)	S1 (Min)	T (Max)	T1 (Max)
8mm	1.5 +0.1 -0.0	1.0	1.75 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	25	0.6	0.6	0.1
12mm		1.5				2.0 ± 0.1			
16mm					2.0				
24mm		2.0				2.0 ± 0.15			
32mm					2.0		2.0 ± 0.15		
44mm		2.0				2.0 ± 0.15			

**Table 8-2. Variable Dimensions**

Tape Size	P1	B1 (Max)	E2 (Min)	F	So	T2 (Max.)	W (Max)	A0, B0, & K0
8mm	Specific per package type. Refer to FR-0221 (Tape and Reel Packing Information)	4.35	6.25	3.5 ± 0.05	N/A (see note 4)	2.5	8.3	See Note 1
12mm		8.2	10.25	5.5 ± 0.05		6.5	12.3	
16mm		12.1	14.25	7.5 ± 0.1		8.0	16.3	
24mm		20.1	22.25	11.5 ± 0.1	12.0	24.3		
32mm		23.0	N/A	14.2 ± 0.1		28.4 ± 0.1	32.3	
44mm		35.0	N/A	20.2 ± 0.15	40.4 ± 0.1	16.0	44.3	

**NOTES:**

- A0, B0, and K0 are determined by component size. The cavity must restrict lateral movement of component to 0.5mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16,24,32, and 44mm wide carrier. The maximum component rotation within the cavity must be limited to 20° maximum for 8 and 12 mm carrier tapes and 10° maximum for 16 through 44mm.
- Tape and components will pass around reel with radius "R" without damage.
- S1 does not apply to carrier width ≥32mm because carrier has sprocket holes on both sides of carrier where Do ≥ S1.
- So does not exist for carrier ≤32mm because carrier does not have sprocket hole on both side of carrier.

Table 8-3. Reel Dimensions by Tape Size

Tape Size	A	N (Min) See Note A	W1	W2 (Max)	W3	B (Min)	C	D (Min)
8mm	178 ±2.0mm or 330±2.0mm	60 ±2.0mm or 100±2.0mm	8.4 +1.5/-0.0 mm	14.4 mm	Shall Ac- commo- date Tape Width Without Interfer- ence	1.5mm	13.0 +0.5/- 0.2 mm	20.2mm
12mm			12.4 +2.0/-0.0 mm	18.4 mm				
16mm	330 ±2.0mm	100 ±2.0mm	16.4 +2.0/-0.0 mm	22.4 mm				
24mm			24.4 +2.0/-0.0 mm	30.4 mm				
32mm			32.4 +2.0/-0.0 mm	38.4 mm				
44mm			44.4 +2.0/-0.0 mm	50.4 mm				

NOTE:

A. If reel diameter A=178 ±2.0mm, then the corresponding hub diameter (N(min)) will by 60 ±2.0mm. If reel diameter A=330±2.0mm, then the corresponding hub diameter (N(min)) will by 100±2.0mm.

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