



**THE DATASHEET OF
NLV SX4014MUTAG**



NLSX4014

4-Bit 100 Mb/s Configurable Dual-Supply Level Translator

The NLSX4014 is a 4-bit configurable dual-supply bidirectional level translator without a direction control pin. The I/O V_{CC} - and I/O V_L -ports are designed to track two different power supply rails, V_{CC} and V_L respectively. The V_{CC} supply rail is configurable from 1.3 V to 4.5 V while the V_L supply rail is configurable from 0.9 V to ($V_{CC} - 0.4$) V. This allows lower voltage logic signals on the V_L side to be translated into higher voltage logic signals on the V_{CC} side, and vice-versa. Both I/O ports are auto-sensing; thus, no direction pin is required.

The Output Enable (EN) input, when Low, disables both I/O ports by putting them in 3-state. This significantly reduces the supply currents from both V_{CC} and V_L . The EN signal is designed to track V_L .

Features

- Wide High-Side V_{CC} Operating Range: 1.3 V to 4.5 V
Wide Low-Side V_L Operating Range: 0.9 V to ($V_{CC} - 0.4$) V
- Power Supply Isolation
 - ◆ All Outputs are in the High Impedance State if Either V_L or V_{CC} is at Ground
- High-Speed with 100 Mb/s Guaranteed Data Rate for $V_L > 1.6$ V
- Low Bit-to-Bit Skew
- Overvoltage Tolerant Enable and I/O Pins
- Non-preferential Powerup Sequencing
- Small packaging: 1.7 mm x 2.0 mm UQFN12
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free Devices

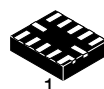
Typical Applications

- Mobile Phones, PDAs, Other Portable Devices



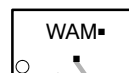
ON Semiconductor®

www.onsemi.com

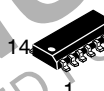


UQFN12
MU SUFFIX
CASE 523AE

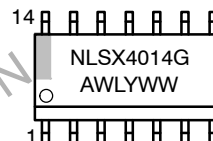
MARKING DIAGRAMS



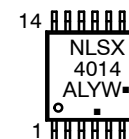
WA = Specific Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)



SOIC-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ▪ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------|-------------------|------------------|
| NLSX4014MUTAG | UQFN12 (Pb-Free) | 3000/Tape & Reel |
| NLVSX4014MUTAG | UQFN12 (Pb-Free) | 3000/Tape & Reel |
| NLSX4014DR2G | SO-14 (Pb-Free) | 2500/Tape & Reel |
| NLSX4014DTR2G | TSSOP14 (Pb-Free) | 2500/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NLSX4014

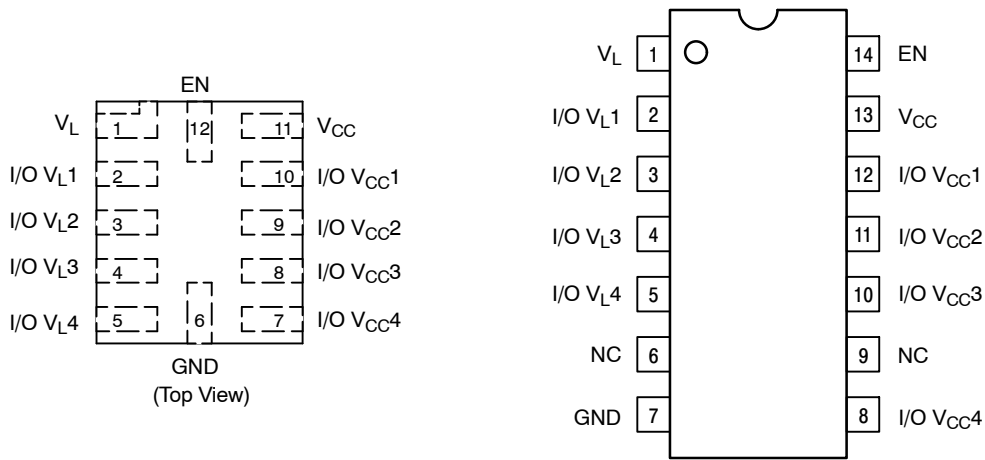


Figure 1. Pin Assignments

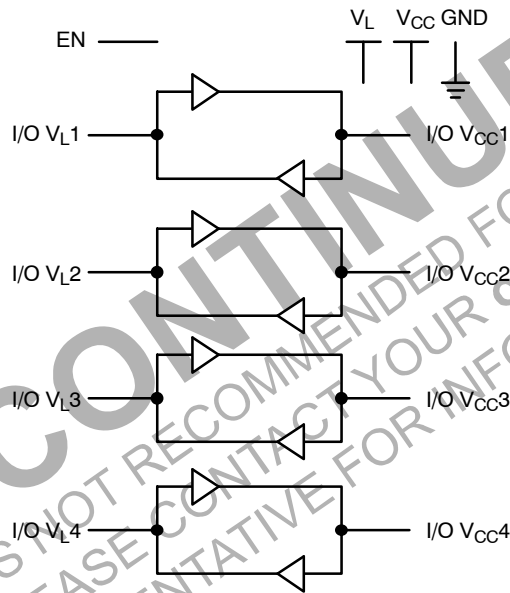


Figure 2. Logic Diagram

PIN ASSIGNMENT

| Pins | Description |
|----------------------------------|-----------------------------------------|
| V _{CC} | V _{CC} Input Voltage |
| V _L | V _L Input Voltage |
| GND | Ground |
| EN | Output Enable |
| I/O V _{CC} ⁿ | I/O Port, Referenced to V _{CC} |
| I/O V _L ⁿ | I/O Port, Referenced to V _L |

FUNCTION TABLE

| EN | Operating Mode |
|----|---------------------|
| L | Hi-Z |
| H | I/O Buses Connected |

NLSX4014

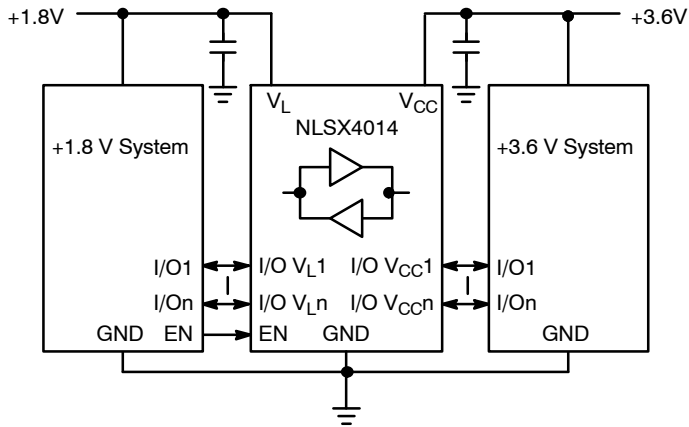


Figure 3. Typical Application Circuit

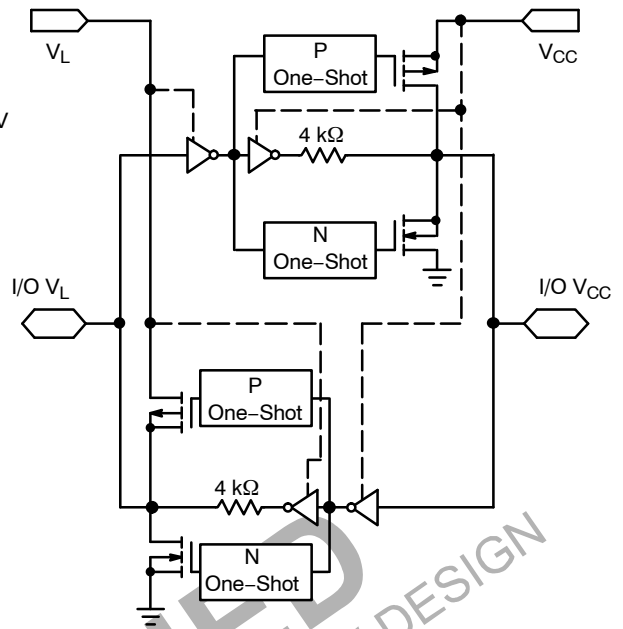


Figure 4. Simplified Functional Diagram (1 I/O Line)
(EN = 1)

DISCONTINUED

THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi
REPRESENTATIVE FOR INFORMATION

NLSX4014

MAXIMUM RATINGS

| Symbol | Parameter | Value | Condition | Unit |
|--------------|----------------------------------------------|----------------------------|-------------|-------------|
| V_{CC} | V_{CC} Supply Voltage | -0.5 to +5.5 | | V |
| V_L | V_L Supply Voltage | -0.5 to +5.5 | | V |
| I/O V_{CC} | V_{CC} -Referenced DC Input/Output Voltage | -0.5 to ($V_{CC} + 0.3$) | | V |
| I/O V_L | V_L -Referenced DC Input/Output Voltage | -0.5 to ($V_L + 0.3$) | | V |
| V_{EN} | Enable Control Pin DC Input Voltage | -0.5 to +5.5 | | V |
| I_{IK} | Input Diode Clamp Current | -50 | $V_I < GND$ | mA |
| I_{OK} | Output Diode Clamp Current | -50 | $V_O < GND$ | mA |
| I_{CC} | DC Supply Current Through V_{CC} | ± 100 | | mA |
| I_L | DC Supply Current Through V_L | ± 100 | | mA |
| I_{GND} | DC Ground Current Through Ground Pin | ± 100 | | mA |
| T_{STG} | Storage Temperature | -65 to +150 | | $^{\circ}C$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---------------------|---------------------------------------------------------------------------------------------------------|-----------------------------------------|----------------|-------------|
| V_{CC} | V_{CC} Supply Voltage | 1.3 | 4.5 | V |
| V_L | V_L Supply Voltage | 0.9 | $V_{CC} - 0.4$ | V |
| V_{EN} | Enable Control Pin Voltage | GND | 4.5 | V |
| V_{IO} | Bus Input/Output Voltage | I/O V_{CC} GND I/O V_L GND | 4.5 4.5 | V |
| T_A | Operating Temperature Range | -40 | +85 | $^{\circ}C$ |
| $\Delta I/\Delta V$ | Input Transition Rise or Rate V_I, V_{IO} from 30% to 70% of V_{CC} ; $V_{CC} = 3.3 V \pm 0.3 V$ | 0 | 10 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

NLSX4014

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions (Note 1) | V _{CC} (V) (Note 2) | V _L (V) (Note 3) | -40°C to +85°C | | | Unit |
|------------------|-----------------------------------------|--------------------------------------------|---------------------------------|--------------------------------|-----------------------|-----------------|-----------------------|------|
| | | | | | Min | Typ (Note 4) | Max | |
| V _{IHC} | I/O V _{CC} Input HIGH Voltage | | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | 0.8 * V _{CC} | - | - | V |
| V _{ILC} | I/O V _{CC} Input LOW Voltage | | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | - | - | 0.2 * V _{CC} | V |
| V _{IHL} | I/O V _L Input HIGH Voltage | | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | 0.8 * V _L | - | - | V |
| V _{ILL} | I/O V _L Input LOW Voltage | | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | - | - | 0.2 * V _L | V |
| V _{IH} | Control Pin Input HIGH Voltage | T _A = +25°C | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | 0.8 * V _L | - | - | V |
| V _{IL} | Control Pin Input LOW Voltage | T _A = +25°C | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | - | - | 0.2 * V _L | V |
| V _{OHC} | I/O V _{CC} Output HIGH Voltage | I/O V _{CC} Source Current = 20 μA | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | 0.8 * V _{CC} | - | - | V |
| V _{OLC} | I/O V _{CC} Output LOW Voltage | I/O V _{CC} Sink Current = 20 μA | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | - | - | 0.2 * V _{CC} | V |
| V _{OHL} | I/O V _L Output HIGH Voltage | I/O V _L Source Current = 20 μA | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | 0.8 * V _L | - | - | V |
| V _{OLL} | I/O V _L Output LOW Voltage | I/O V _L Sink Current = 20 μA | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | - | - | 0.2 * V _L | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Normal test conditions are V_{EN} = 0 V, C_{IOVCC} = 15 pF and C_{IOVL} = 15 pF, unless otherwise specified.
2. V_{CC} is the supply voltage associated with the high voltage port, and V_{CC} ranges from +1.3 V to 4.5 V under normal operating conditions.
3. V_L is the supply voltage associated with the low voltage port. V_L must be less than or equal to (V_{CC} - 0.4) V during normal operation. However, during startup and shutdown conditions, V_L can be greater than (V_{CC} - 0.4) V.
4. Typical values are for V_{CC} = +2.8 V, V_L = +1.8 V and T_A = +25°C. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

NLSX4014

POWER CONSUMPTION

| Symbol | Parameter | Test Conditions (Note 5) | V _{CC} (V) (Note 6) | V _L (V) (Note 7) | -40°C to +85°C | | | Unit |
|---------------------|-----------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------|--------------------------------|----------------|-----|------|------|
| | | | | | Min | Typ | Max | |
| I _{Q-VCC} | Supply Current from V _{CC} | EN = V _L ; I/O V _{CCn} = 0 V, I/O V _{Ln} = 0 V, I/O V _{CCn} = V _{CC} or I/O V _{Ln} = V _L and I _o = 0 | 1.3 to 3.6 | 0.9 to (V _{CC} - 0.4) | - | - | 1.0 | μA |
| | | | 0 | 4.1 | - | - | 2.0 | |
| | | | 4.5 | 0 | - | - | 2.0 | |
| I _{Q-VL} | Supply Current from V _L | EN = V _L ; I/O V _{CCn} = 0 V, I/O V _{Ln} = 0 V, I/O V _{CCn} = V _{CC} or I/O V _{Ln} = V _L and I _o = 0 | 1.3 to 3.6 | 0.9 to (V _{CC} - 0.4) | - | - | 1.0 | μA |
| | | | | < (V _{CC} - 0.2) | | | | |
| | | | 0 | 4.1 | - | - | 2.0 | |
| | | EN = V _L ; I/O V _{CCn} = 0 V, I/O V _{Ln} = 0 V, I/O V _{CCn} = V _{CC} or I/O V _{Ln} = (V _{CC} - 0.2 V) and I _o = 0 | 4.5 | 0 | | | | |
| I _{TS-VCC} | V _{CC} Tristate Output Mode Supply Current | EN = 0 V | 1.3 to 3.6 | 0.9 to (V _{CC} - 0.4) | - | - | 1.0 | μA |
| I _{TS-VL} | V _L Tristate Output Mode Supply Current | EN = 0 V | 1.3 to 3.6 | 0.9 to (V _{CC} - 0.4) | - | - | 0.2 | μA |
| | | EN = 0 V | | V _{CC} - 0.2 | - | - | 2.0 | |
| I _{OZ} | I/O Tristate Output Mode Leakage Current | EN = 0 V | 1.3 to 3.6 | 0.9 to (V _{CC} - 0.4) | - | - | 0.15 | μA |
| | | EN = 0 V | | V _{CC} - 0.2 | - | - | 2.0 | |
| I _{EN} | Output Enable Pin Input Current | - | 1.3 to 3.6 | 0.9 to (V _{CC} - 0.4) | - | - | 1.0 | μA |
| I _{OFF} | V _L Port | I/O V _{Ln} = 0 to 4.1 V | 0 to 4.5 | 0 | - | - | 2.0 | μA |
| | V _{CC} Port | I/O V _{CCn} = 0 to 4.5 V | 0 | 0 to 4.1 | - | - | 2.0 | |

5. Normal test conditions are V_{EN} = 0 V, C_{I0VCC} = 15 pF and C_{I0VL} = 15 pF, unless otherwise specified.

6. V_{CC} is the supply voltage associated with the high voltage port, and V_{CC} ranges from +1.3 V to 3.6 V.

7. V_L is the supply voltage associated with the low voltage port. V_L must be less than or equal to (V_{CC} - 0.4) V during normal operation. However, during startup and shutdown conditions, V_L can be greater than (V_{CC} - 0.4) V.

DISCONTINUED FOR NEW DESIGN

THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT SALES FOR MORE INFORMATION
REPRESENTATIVE FOR INFORMATION

NLSX4014

TIMING CHARACTERISTICS

| Symbol | Parameter | Test Conditions (Note 8) | V _{CC} (V) (Note 9) | V _L (V) (Note 10) | -40°C to +85°C | | | Unit |
|------------------------|-----------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------|---------------------------------|----------------|------------------|-----|------|
| | | | | | Min | Typ (Note 11) | Max | |
| t _{R-VCC} | I/O V _{CC} Rise Time (Output = I/O_V _{CC}) | C _{I_OV_{CC}} = 15 pF | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | | 0.7 | 2.4 | ns |
| t _{F-VCC} | I/O V _{CC} Falltime (Output = I/O_V _{CC}) | C _{I_OV_{CC}} = 15 pF | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | | 0.5 | 1.0 | ns |
| t _{R-VL} | I/O V _L Risetime (Output = I/O_V _L) | C _{I_OV_L} = 15 pF | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | | 1.0 | 3.8 | ns |
| t _{F-VL} | I/O V _L Falltime (Output = I/O_V _L) | C _{I_OV_L} = 15 pF | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | | 0.6 | 1.2 | ns |
| Z _{O-VCC} | I/O V _{CC} One-Shot Output Impedance | | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | | 30 | | Ω |
| Z _{O-VL} | I/O V _L One-Shot Output Impedance | | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | | 30 | | Ω |
| t _{PD_VL-VCC} | Propagation Delay (Output = I/O_V _{CC} , t _{PHL} , t _{PLH}) | C _{I_OV_{CC}} = 15 pF | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | | 4.5 | 9.3 | ns |
| t _{PD_VCC-VL} | Propagation Delay (Output = I/O_V _L , t _{PHL} , t _{PLH}) | C _{I_OV_L} = 15 pF | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | | 3.0 | 6.5 | ns |
| t _{SK_VL-VCC} | Channel-to-Channel Skew (Output = I/O_V _{CC}) | C _{I_OV_{CC}} = 15 pF | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | | 0.2 | 0.3 | nS |
| t _{SK_VCC-VL} | Channel-to-Channel Skew (Output = I/O_V _L) | C _{I_OV_{CC}} = 15 pF | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | | 0.2 | 0.3 | nS |
| MDR | Maximum Data Rate | (Output = I/O_V _{CC} , C _{I_OV_{CC}} = 15 pF) (Output = I/O_V _L , C _{I_OV_L} = 15 pF) | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | 110 | | | Mb/s |
| | | | > 2.2 | > 1.8 | 140 | | | |

8. Normal test conditions are V_{EN} = 0 V, C_{I_OV_{CC}} = 15 pF and C_{I_OV_L} = 15 pF, unless otherwise specified.

9. V_{CC} is the supply voltage associated with the high voltage port, and V_{CC} ranges from +1.3 V to 4.5 V under normal operating conditions.

10. V_L is the supply voltage associated with the low voltage port. V_L must be less than or equal to (V_{CC} - 0.4) V during normal operation. However, during startup and shutdown conditions, V_L can be greater than (V_{CC} - 0.4) V.

11. Typical values are for V_{CC} = +2.8 V, V_L = +1.8 V and T_A = +25°C. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

ENABLE / DISABLE TIME MEASUREMENTS

| Symbol | Parameter | Test Conditions (Note 12) | V _{CC} (V) (Note 13) | V _L (V) (Note 14) | -40°C to +85°C | | | Unit |
|----------------------|--------------------------------------------------------------------------|--------------------------------------------------|----------------------------------|---------------------------------|----------------|------------------|-----|------|
| | | | | | Min | Typ (Note 15) | Max | |
| t _{EN-VCC} | Turn-On Enable Time (Output = I/O_V _{CC} , t _{pZH}) | C _{I_OV_{CC}} = 15 pF | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | | 130 | 180 | ns |
| | Turn-On Enable Time (Output = I/O_V _{CC} , t _{pZL}) | C _{I_OV_L} = 15 pF | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | | 100 | 150 | ns |
| t _{EN-VL} | Turn-On Enable Time (Output = I/O_V _L , t _{pZH}) | C _{I_OV_{CC}} = 15 pF | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | | 95 | 185 | ns |
| | Turn-On Enable Time (Output = I/O_V _L , t _{pZL}) | C _{I_OV_L} = 15 pF | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | | 70 | 110 | ns |
| t _{DIS-VCC} | Turn-Off Disable Time (Output = I/O_V _{CC} , t _{pZH}) | C _{I_OV_{CC}} = 15 pF | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | | 175 | 250 | ns |
| | Propagation Delay (Output = I/O_V _{CC} , t _{pLZ}) | C _{I_OV_L} = 15 pF | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | | 150 | 190 | ns |
| t _{DIS-VL} | Turn-Off Disable Time (Output = I/O_V _L , t _{pZH}) | C _{I_OV_{CC}} = 15 pF | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | | 180 | 250 | ns |
| | Propagation Delay (Output = I/O_V _L , t _{pLZ}) | C _{I_OV_L} = 15 pF | 1.3 to 4.5 | 0.9 to (V _{CC} - 0.4) | | 160 | 220 | ns |

- 12. Normal test conditions are V_{EN} = 0 V, C_{I_OV_{CC}} = 15 pF and C_{I_OV_L} = 15 pF, unless otherwise specified.
- 13. V_{CC} is the supply voltage associated with the high voltage port, and V_{CC} ranges from +1.3 V to 4.5 V under normal operating conditions.
- 14. V_L is the supply voltage associated with the low voltage port. V_L must be less than or equal to (V_{CC} - 0.4) V during normal operation. However, during startup and shutdown conditions, V_L can be greater than (V_{CC} - 0.4) V.
- 15. Typical values are for V_{CC} = +2.8 V, V_L = +1.8 V and T_A = +25 °C. All units are production tested at T_A = +25 °C. Limits over the operating temperature range are guaranteed by design.

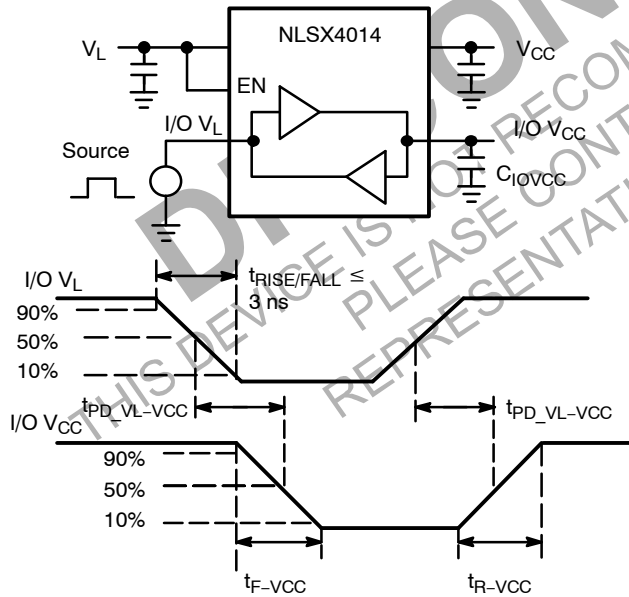


Figure 5. Driving I/O V_L Test Circuit and Timing

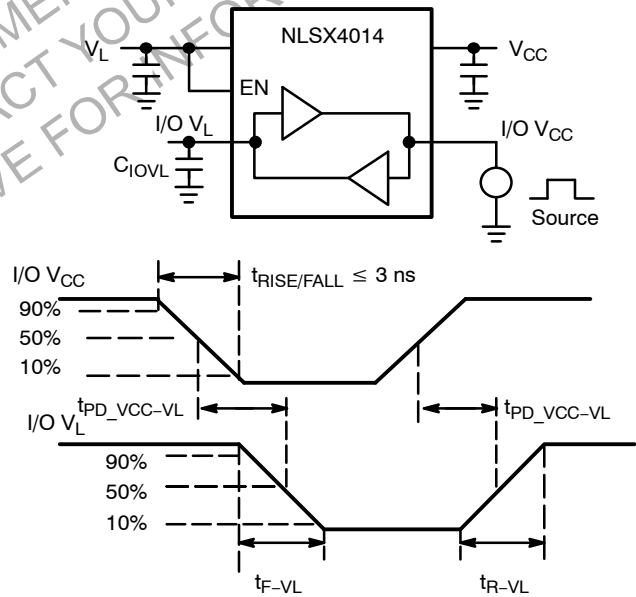
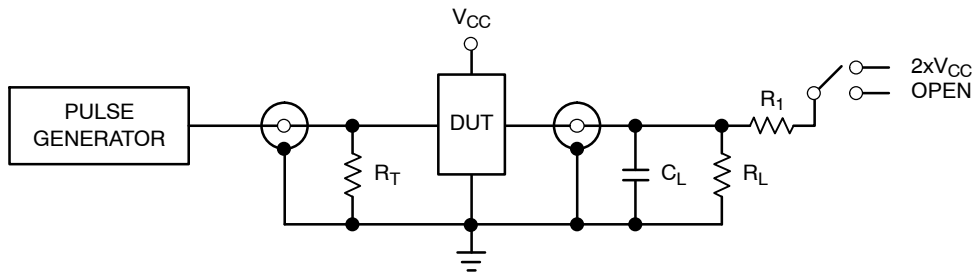


Figure 6. Driving I/O V_{CC} Test Circuit and Timing

NLSX4014



| Test | Switch |
|-----------------------|-------------------|
| t_{PZH} , t_{PHZ} | Open |
| t_{PZL} , t_{PLZ} | $2 \times V_{CC}$ |

$C_L = 15 \text{ pF}$ or equivalent (Includes jig and probe capacitance)
 $R_L = R_1 = 50 \text{ k}\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 7. Test Circuit for Enable/Disable Time Measurement

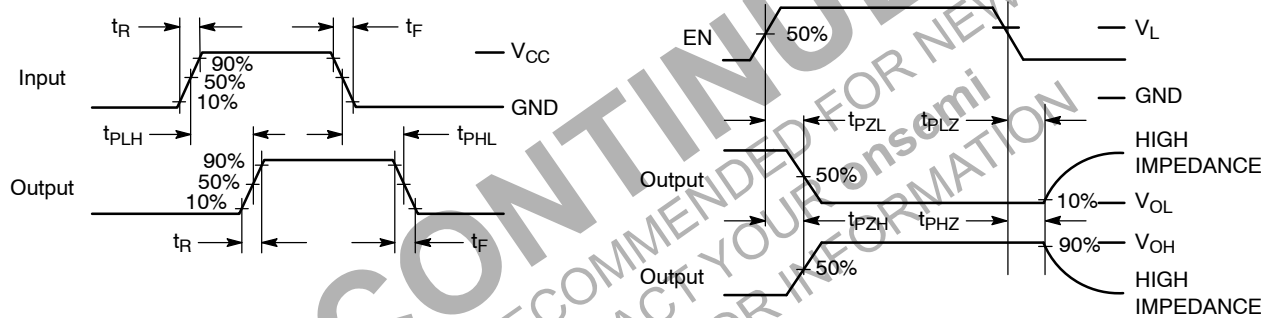


Figure 8. Timing Definitions for Propagation Delays and Enable/Disable Measurement

IMPORTANT APPLICATIONS INFORMATION

Level Translator Architecture

The NLSX4014 auto sense translator provides bi-directional voltage level shifting to transfer data in multiple supply voltage systems. This device has two supply voltages, V_L and V_{CC} , which set the logic levels on the input and output sides of the translator. When used to transfer data from the V_L to the V_{CC} ports, input signals referenced to the V_L supply are translated to output signals with a logic level matched to V_{CC} . In a similar manner, the V_{CC} to V_L translation shifts input signals with a logic level compatible to V_{CC} to an output signal matched to V_L .

The NLSX4014 consists of four bi-directional channels that independently determine the direction of the data flow without requiring a directional pin. The one-shot circuits are used to detect the rising or falling input signals. In addition, the one shots decrease the rise and fall time of the output signal for high-to-low and low-to-high transitions.

Input Driver Requirements

For proper operation, the input driver to the auto sense translator should be capable of driving 2.0 mA of peak output current.

Output Load Requirements

The NLSX4014 is designed to drive CMOS inputs. Resistive pullup or pulldown loads of less than 50 k Ω should not be used with this device. The NLSX3373 or NLSX3378 open-drain auto sense translators are alternate translator options for an application such as the I²C bus that requires pullup resistors.

Enable Input (EN)

The NLSX4014 has an Enable pin (EN) that provides tri-state operation at the I/O pins. Driving the Enable pin to a low logic level minimizes the power consumption of the device and drives the I/O V_{CC} and I/O V_L pins to a high impedance state. Normal translation operation occurs when the EN pin is equal to a logic high signal. The EN pin is referenced to the V_L supply and has Over-Voltage Tolerant (OVT) protection.

Uni-Directional versus Bi-Directional Translation

The NLSX4014 can function as a non-inverting uni-directional translator. One advantage of using the translator as a uni-directional device is that each I/O pin can be configured as either an input or output. The configurable input or output feature is especially useful in applications such as SPI that use multiple uni-directional I/O lines to send data to and from a device. The flexible I/O port of the auto sense translator simplifies the trace connections on the PCB.

Power Supply Guidelines

It is recommended that the V_L supply should be less than or equal to the value of the V_{CC} minus 0.4 V. The sequencing of the power supplies will not damage the device during the power up operation; however, the current consumption of the device will increase if V_L exceeds V_{CC} minus 0.4 V. In addition, the I/O V_{CC} and I/O V_L pins are in the high impedance state if either supply voltage is equal to 0 V.

For optimal performance, 0.01 to 0.1 μ F decoupling capacitors should be used on the V_L and V_{CC} power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the power supply voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

The NLSX4014 provides power supply isolation if either supply voltage V_L or V_{CC} is equal to 0 V. The isolation occurs because the I/O pins are in the high impedance state. It is recommended that pulldown resistors should be used if the V_L or V_{CC} are floated or in a high impedance state. A pulldown resistor connected from the supply voltage to ground ensures that the translator's supply voltage is equal to 0 V.

MECHANICAL CASE OUTLINE

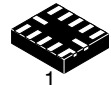
PACKAGE DIMENSIONS

ON Semiconductor®

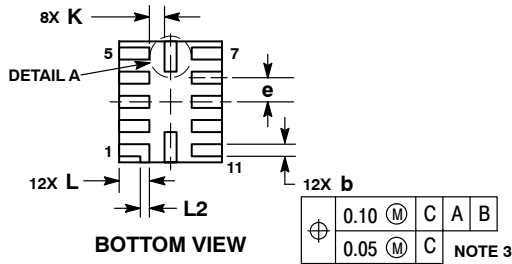
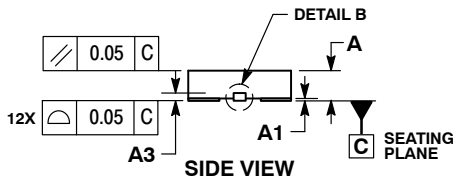
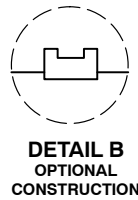
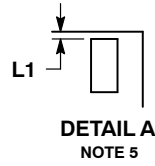
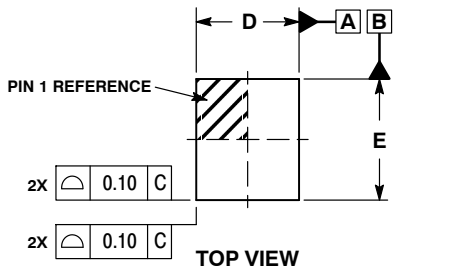


UQFN12 1.7x2.0, 0.4P CASE 523AE-01 ISSUE A

DATE 11 JUN 2007



SCALE 4:1

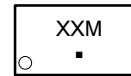


NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS
- DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
- MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH 0.03 MAX ON BOTTOM SURFACE OF TERMINALS.
- DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.45 | 0.55 |
| A1 | 0.00 | 0.05 |
| A3 | 0.127 REF | |
| b | 0.15 | 0.25 |
| D | 1.70 BSC | |
| E | 2.00 BSC | |
| e | 0.40 BSC | |
| K | 0.20 | --- |
| L | 0.45 | 0.55 |
| L1 | 0.00 | 0.03 |
| L2 | 0.15 REF | |

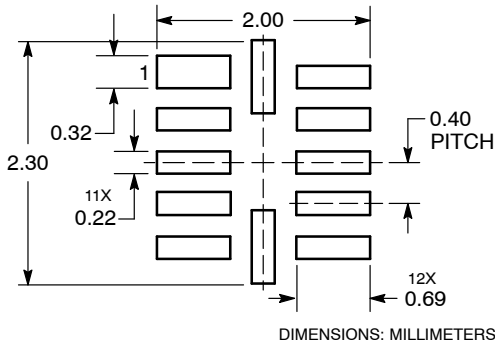
GENERIC MARKING DIAGRAM*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

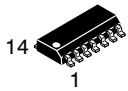
MOUNTING FOOTPRINT SOLDERMASK DEFINED



| | | |
|-------------------------|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98AON23418D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | UQFN12 1.7 X 2.0, 0.4P | PAGE 1 OF 1 |

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

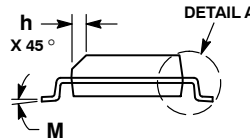
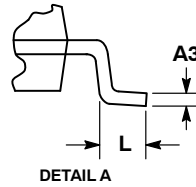
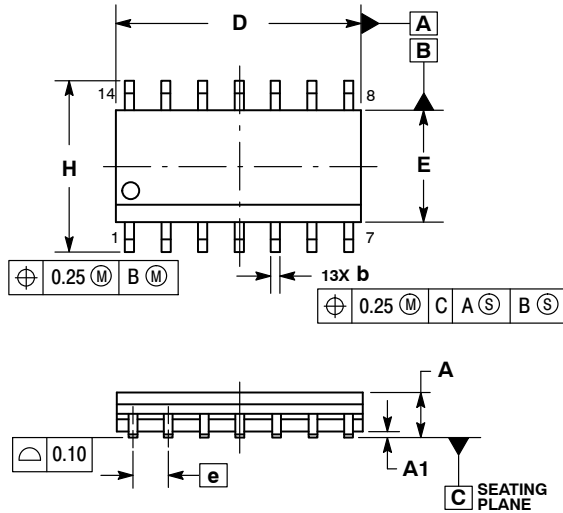
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB
CASE 751A-03
ISSUE L

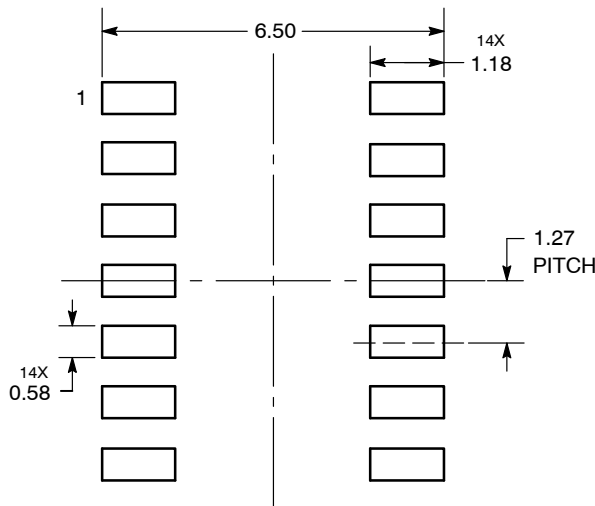
DATE 03 FEB 2016



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0° | 7° | 0° | 7° |

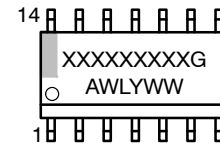
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

| | | |
|------------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98ASB42565B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | SOIC-14 NB | PAGE 1 OF 2 |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 2:
 CANCELLED

STYLE 3:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON CATHODE

STYLE 4:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 5:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 6:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

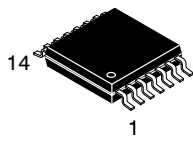
STYLE 7:
 PIN 1. ANODE/CATHODE
 2. COMMON ANODE
 3. COMMON CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. COMMON CATHODE
 12. COMMON ANODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

STYLE 8:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

| | | |
|-------------------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98ASB42565B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | SOIC-14 NB | PAGE 2 OF 2 |

onsemi and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

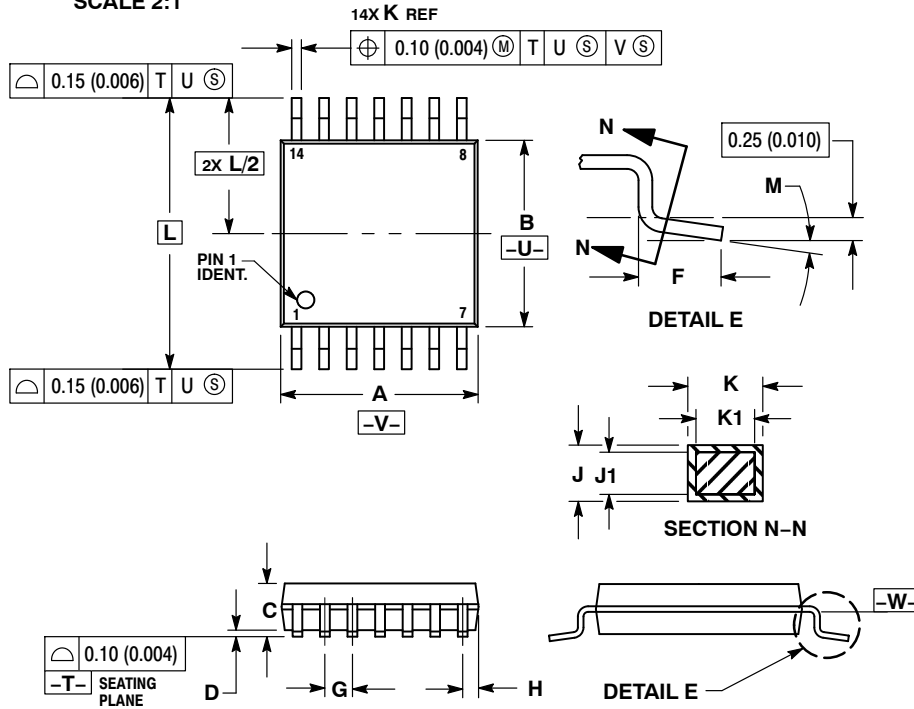
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TSSOP-14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

SCALE 2:1

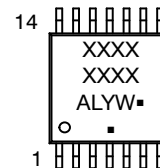


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

GENERIC MARKING DIAGRAM*

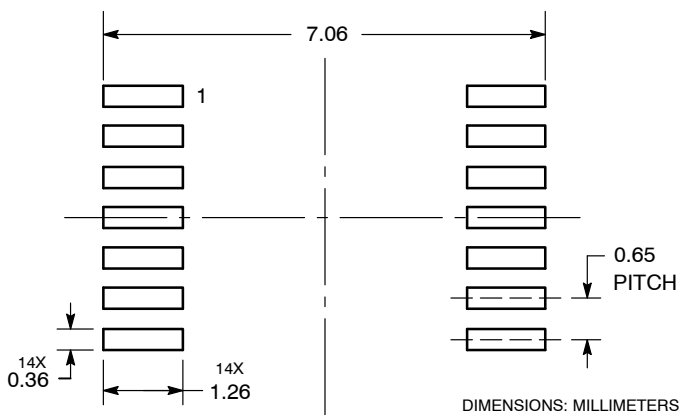


- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT



| | | |
|-------------------------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98ASH70246A | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | TSSOP-14 WB | PAGE 1 OF 1 |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View NLVSX4014MUTAG on WIN SOURCE](#)

 [ON Semiconductor](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management