



**THE DATASHEET OF
XMC4500E144X1024ACXQSA1**



XMC4500

Microcontroller Series
for Industrial Applications

XMC4000 Family

ARM[®] Cortex[®]-M4
32-bit processor core

Data Sheet

V1.6 2023-04

Microcontrollers

Edition 2023-04

**Published by
Infineon Technologies AG
81726 Munich, Germany**

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Revision History: V1.6 2023-04

Previous Versions:

V1.5, 2017-12
 V1.4, 2016-01
 V1.3, 2014-03
 V1.2, 2013-07
 V1.1, 2013-07
 V1.0, 2013-01
 V0.9, 2012-12
 V0.8, 2012-11

| Page | Subjects |
|-----------------|---|
| V1.6, 2023-04 | |
| 118 | Table 64: Added package details: PG-LQFP-100-29 and PG-LQFP-144-26. Deleted package details: PG-LQFP-100-11 and PG-LQFP-144-18. |
| 121, 123 | Added package diagrams: PG-LQFP-100-29 and PG-LQFP-144-26. |
| 118 | Deleted package diagrams: PG-LQFP-100-11 and PG-LQFP-144-18. |

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Table of Contents

| | | |
|----------|---|----|
| | Table of Contents | 5 |
| | About this Document | 7 |
| 1 | Summary of Features | 8 |
| 1.1 | Ordering Information | 10 |
| 1.2 | Device Types | 11 |
| 1.3 | Device Type Features | 12 |
| 1.4 | Definition of Feature Variants | 14 |
| 1.5 | Identification Registers | 15 |
| 2 | General Device Information | 16 |
| 2.1 | Logic Symbols | 16 |
| 2.2 | Pin Configuration and Definition | 19 |
| 2.2.1 | Package Pin Summary | 22 |
| 2.2.2 | Port I/O Functions | 29 |
| 2.2.2.1 | Port I/O Function Table | 30 |
| 2.3 | Power Connection Scheme | 36 |
| 3 | Electrical Parameters | 38 |
| 3.1 | General Parameters | 38 |
| 3.1.1 | Parameter Interpretation | 38 |
| 3.1.2 | Absolute Maximum Ratings | 39 |
| 3.1.3 | Pin Reliability in Overload | 40 |
| 3.1.4 | Pad Driver and Pad Classes Summary | 43 |
| 3.1.5 | Operating Conditions | 44 |
| 3.2 | DC Parameters | 45 |
| 3.2.1 | Input/Output Pins | 45 |
| 3.2.2 | Analog to Digital Converters (VADC) | 51 |
| 3.2.3 | Digital to Analog Converters (DAC) | 55 |
| 3.2.4 | Out-of-Range Comparator (ORC) | 59 |
| 3.2.5 | Die Temperature Sensor | 61 |
| 3.2.6 | USB OTG Interface DC Characteristics | 62 |
| 3.2.7 | Oscillator Pins | 64 |
| 3.2.8 | Power Supply Current | 68 |
| 3.2.9 | Flash Memory Parameters | 71 |
| 3.3 | AC Parameters | 72 |
| 3.3.1 | Testing Waveforms | 72 |
| 3.3.2 | Power-Up and Supply Monitoring | 73 |
| 3.3.3 | Power Sequencing | 74 |
| 3.3.4 | Phase Locked Loop (PLL) Characteristics | 76 |
| 3.3.5 | Internal Clock Source Characteristics | 77 |

Table of Contents

| | | |
|----------|--|------------|
| 3.3.6 | JTAG Interface Timing | 79 |
| 3.3.7 | Serial Wire Debug Port (SW-DP) Timing | 81 |
| 3.3.8 | Embedded Trace Macro Cell (ETM) Timing | 82 |
| 3.3.9 | Peripheral Timing | 83 |
| 3.3.9.1 | Delta-Sigma Demodulator Digital Interface Timing | 83 |
| 3.3.9.2 | Synchronous Serial Interface (USIC SSC) Timing | 84 |
| 3.3.9.3 | Inter-IC (IIC) Interface Timing | 87 |
| 3.3.9.4 | Inter-IC Sound (IIS) Interface Timing | 89 |
| 3.3.9.5 | SDMMC Interface Timing | 91 |
| 3.3.10 | EBU Timing | 99 |
| 3.3.10.1 | EBU Asynchronous Timing | 99 |
| 3.3.10.2 | EBU Burst Mode Access Timing | 106 |
| 3.3.10.3 | EBU Arbitration Signal Timing | 108 |
| 3.3.10.4 | EBU SDRAM Access Timing | 109 |
| 3.3.11 | USB Interface Characteristics | 113 |
| 3.3.12 | Ethernet Interface (ETH) Characteristics | 114 |
| 3.3.12.1 | ETH Measurement Reference Points | 114 |
| 3.3.12.2 | ETH Management Signal Parameters (ETH_MDC, ETH_MDIO) . . | 115 |
| 3.3.12.3 | ETH MII Parameters | 116 |
| 3.3.12.4 | ETH RMII Parameters | 117 |
| 4 | Package and Reliability | 118 |
| 4.1 | Package Parameters | 118 |
| 4.1.1 | Thermal Considerations | 119 |
| 4.2 | Package Outlines | 120 |
| 4.3 | Quality Declarations | 124 |

About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC4[12]00 series devices.

The document describes the characteristics of a superset of the XMC4[12]00 series devices. For simplicity, the various device types are referred to by the collective term XMC4[12]00 throughout this manual.

XMC4000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
 - describes the functionality of the superset of devices.
- **Data Sheets**
 - list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
 - list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to <http://www.infineon.com/xmc4000> to get access to the latest versions of those documents.

1 Summary of Features

The XMC4500 devices are members of the XMC4000 Family of microcontrollers based on the ARM Cortex-M4 processor core. The XMC4000 is a family of high performance and energy efficient microcontrollers optimized for Industrial Connectivity, Industrial Control, Power Conversion, Sense & Control.

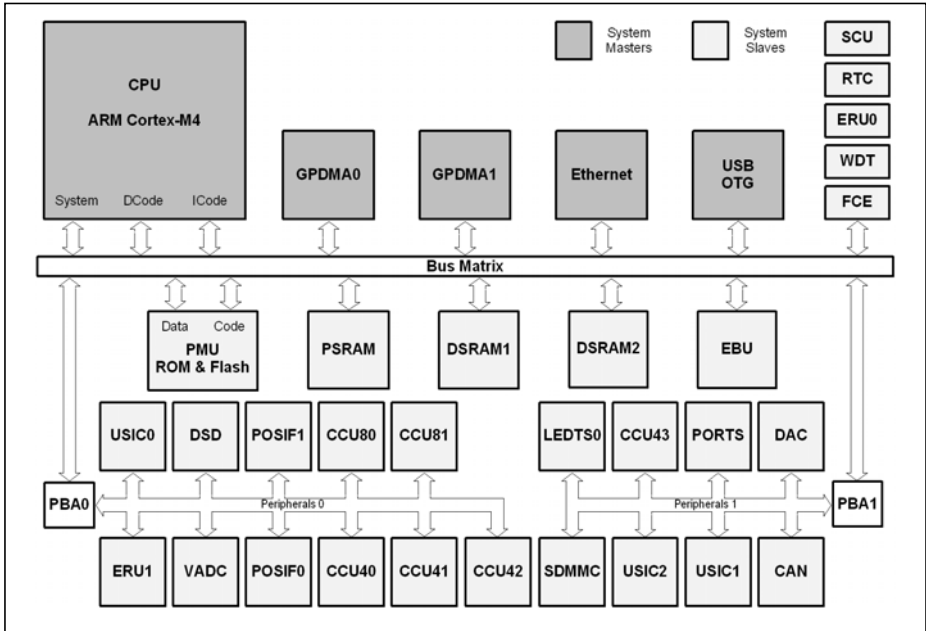


Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
 - High Performance 32-bit ARM Cortex-M4 CPU
 - 16-bit and 32-bit Thumb2 instruction set
 - DSP/MAC instructions
 - System timer (SysTick) for Operating System support
- Floating Point Unit
- Memory Protection Unit
- Nested Vectored Interrupt Controller
- Two General Purpose DMA with up-to 12 channels
- Event Request Unit (ERU) for programmable processing of external and internal service requests
- Flexible CRC Engine (FCE) for multiple bit error detection

On-Chip Memories

- 16 KB on-chip boot ROM
- 64 KB on-chip high-speed program memory
- 64 KB on-chip high speed data memory
- 32 KB on-chip high-speed communication
- 1024 KB on-chip Flash Memory with 4 KB instruction cache

Communication Peripherals

- Ethernet MAC module capable of 10/100 Mbit/s transfer rates
- Universal Serial Bus, USB 2.0 host, Full-Speed OTG, with integrated PHY
- Controller Area Network interface (MultiCAN), Full-CAN/Basic-CAN with 3 nodes, 64 message objects (MO), data rate up to 1MBit/s
- Six Universal Serial Interface Channels (USIC), providing 6 serial channels, usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- LED and Touch-Sense Controller (LEDTS) for Human-Machine interface
- SD and Multi-Media Card interface (SDMMC) for data storage memory cards
- External Bus Interface Unit (EBU) enabling communication with external memories and off-chip peripherals

Analog Frontend Peripherals

- Four Analog-Digital Converters (VADC) of 12-bit resolution, 8 channels each, with input out-of-range comparators
- Delta Sigma Demodulator with four channels, digital input stage for A/D signal conversion
- Digital-Analogue Converter (DAC) with two channels of 12-bit resolution

Industrial Control Peripherals

- Two Capture/Compare Units 8 (CCU8) for motor control and power conversion
- Four Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Two Position Interfaces (POSIF) for servo motor positioning
- Window Watchdog Timer (WDT) for safety sensitive applications
- Die Temperature Sensor (DTS)
- Real Time Clock module with alarm support
- System Control Unit (SCU) for system configuration and control

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability
- Tri-stated in input mode
- Push/pull or open drain output mode
- Boundary scan test support over JTAG interface

On-Chip Debug Support

- Full support for debug features: 8 breakpoints, CoreSight, trace
- Various interfaces: ARM-JTAG, SWD, single wire trace

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC4<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set
- <Z> the package variant
 - E: LFBGA
 - F: LQFP
 - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
 - F: -40°C to 85°C
 - X: -40°C to 105°C
 - K: -40°C to 125°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC4500 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC4500 series, some descriptions may not apply to a specific product.

For simplicity the term **XMC4500** is used for all derivatives throughout this document.

1.2 Device Types

These device types are available and can be ordered through Infineon's direct and/or distribution channels.

Table 1 Synopsis of XMC4500 Device Types

| Derivative¹⁾ | Package | Flash Kbytes | SRAM Kbytes |
|--------------------------------|----------------|---------------------|--------------------|
| XMC4500-E144x1024 | PG-LFBGA-144 | 1024 | 160 |
| XMC4500-F144x1024 | PG-LQFP-144 | 1024 | 160 |
| XMC4500-F100x1024 | PG-LQFP-100 | 1024 | 160 |
| XMC4500-F144x768 | PG-LQFP-144 | 768 | 160 |
| XMC4500-F100x768 | PG-LQFP-100 | 768 | 160 |
| XMC4502-F100x768 | PG-LQFP-100 | 768 | 160 |
| XMC4504-F144x512 | PG-LQFP-144 | 512 | 128 |
| XMC4504-F100x512 | PG-LQFP-100 | 512 | 128 |

1) x is a placeholder for the supported temperature range.

1.3 Device Type Features

The following table lists the available features per device type.

Table 2 Features of XMC4500 Device Types

| Derivative ¹⁾ | LEDTS Intf. | SDMMC Intf. | EBU Intf. ²⁾ | ETH Intf. ³⁾ | USB Intf. | USIC Chan. | MultiCAN Nodes, MO |
|--------------------------|-------------|-------------|-------------------------|-------------------------|-----------|------------|-------------------------|
| XMC4500-E144x1024 | 1 | 1 | SDM | MR | 1 | 3 x 2 | N0, N1, N2 MO[0..63] |
| XMC4500-F144x1024 | 1 | 1 | SDM | MR | 1 | 3 x 2 | N0, N1, N2 MO[0..63] |
| XMC4500-F100x1024 | 1 | 1 | M16 | R | 1 | 3 x 2 | N0, N1, N2 MO[0..63] |
| XMC4500-F144x768 | 1 | 1 | SDM | MR | 1 | 3 x 2 | N0, N1, N2 MO[0..63] |
| XMC4500-F100x768 | 1 | 1 | M16 | R | 1 | 3 x 2 | N0, N1, N2 MO[0..63] |
| XMC4502-F100x768 | 1 | 1 | M16 | - | 1 | 3 x 2 | N0, N1, N2 MO[0..63] |
| XMC4504-F144x512 | 1 | 1 | SDM | - | - | 3 x 2 | - |
| XMC4504-F100x512 | 1 | 1 | M16 | - | - | 3 x 2 | - |

1) x is a placeholder for the supported temperature range.

2) Memory types supported S=SDRAM, D=DEMUX, M=MUX 16-bit and 32-bit, M16=MUX 16-bit

3) Supported interfaces, M=MII, R=RMII.

Table 3 Features of XMC4500 Device Types

| Derivative¹⁾ | ADC Chan. | DSD Chan. | DAC Chan. | CCU4 Slice | CCU8 Slice | POSIF Intf. |
|--------------------------------|------------------|------------------|------------------|-------------------|-------------------|--------------------|
| XMC4500-E144x1024 | 32 | 4 | 2 | 4 x 4 | 2 x 4 | 2 |
| XMC4500-F144x1024 | 32 | 4 | 2 | 4 x 4 | 2 x 4 | 2 |
| XMC4500-F100x1024 | 24 | 4 | 2 | 4 x 4 | 2 x 4 | 2 |
| XMC4500-F144x768 | 32 | 4 | 2 | 4 x 4 | 2 x 4 | 2 |
| XMC4500-F100x768 | 24 | 4 | 2 | 4 x 4 | 2 x 4 | 2 |
| XMC4502-F100x768 | 24 | 4 | 2 | 4 x 4 | 2 x 4 | 2 |
| XMC4504-F144x512 | 32 | 4 | 2 | 4 x 4 | 2 x 4 | 2 |
| XMC4504-F100x512 | 24 | 4 | 2 | 4 x 4 | 2 x 4 | 2 |

1) x is a placeholder for the supported temperature range.

1.4 Definition of Feature Variants

The XMC4500 types are offered with several memory sizes and number of available VADC channels. **Table 4** describes the location of the available Flash memory, **Table 5** describes the location of the available SRAMs, **Table 6** the available VADC channels.

Table 4 Flash Memory Ranges

| Total Flash Size | Cached Range | Uncached Range |
|------------------|--|--|
| 512 Kbytes | 0800 0000 _H – 0807 FFFF _H | 0C00 0000 _H – 0C07 FFFF _H |
| 768 Kbytes | 0800 0000 _H – 080B FFFF _H | 0C00 0000 _H – 0C0B FFFF _H |
| 1,024 Kbytes | 0800 0000 _H – 080F FFFF _H | 0C00 0000 _H – 0C0F FFFF _H |

Table 5 SRAM Memory Ranges

| Total SRAM Size | Program SRAM | System Data SRAM | Communication Data SRAM |
|-----------------|--|--|--|
| 128 Kbytes | 1000 0000 _H – 1000 FFFF _H | 2000 0000 _H – 2000 FFFF _H | – |
| 160 Kbytes | 1000 0000 _H – 1000 FFFF _H | 2000 0000 _H – 2000 FFFF _H | 3000 0000 _H – 3000 7FFF _H |

Table 6 ADC Channels¹⁾

| Package | VADC G0 | VADC G1 | VADC G2 | VADC G3 |
|-----------------------------|----------|----------|----------|----------|
| PG-LQFP-144 PG-LFBGA-144 | CH0..CH7 | CH0..CH7 | CH0..CH7 | CH0..CH7 |
| PG-LQFP-100 | CH0..CH7 | CH0..CH7 | CH0..CH3 | CH0..CH3 |

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

1.5 Identification Registers

The identification registers allow software to identify the marking.

Table 7 XMC4500 Identification Registers

| Register Name | Value | Marking |
|----------------------|------------------------|----------------|
| SCU_IDCHIP | 0004 5002 _H | EES-AA, ES-AA |
| SCU_IDCHIP | 0004 5003 _H | ES-AB, AB |
| SCU_IDCHIP | 0004 5004 _H | AC |
| JTAG IDCODE | 101D B083 _H | EES-AA, ES-AA |
| JTAG IDCODE | 101D B083 _H | ES-AB, AB |
| JTAG IDCODE | 401D B083 _H | AC |

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

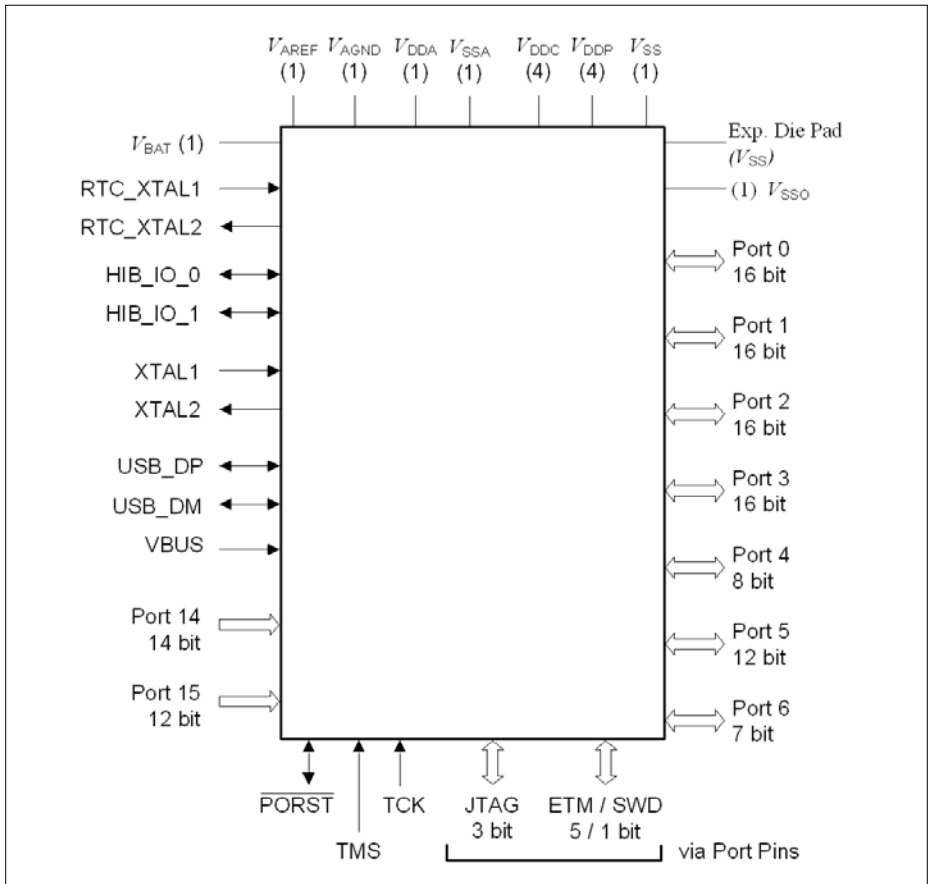


Figure 2 XMC4500 Logic Symbol PG-LQFP-144

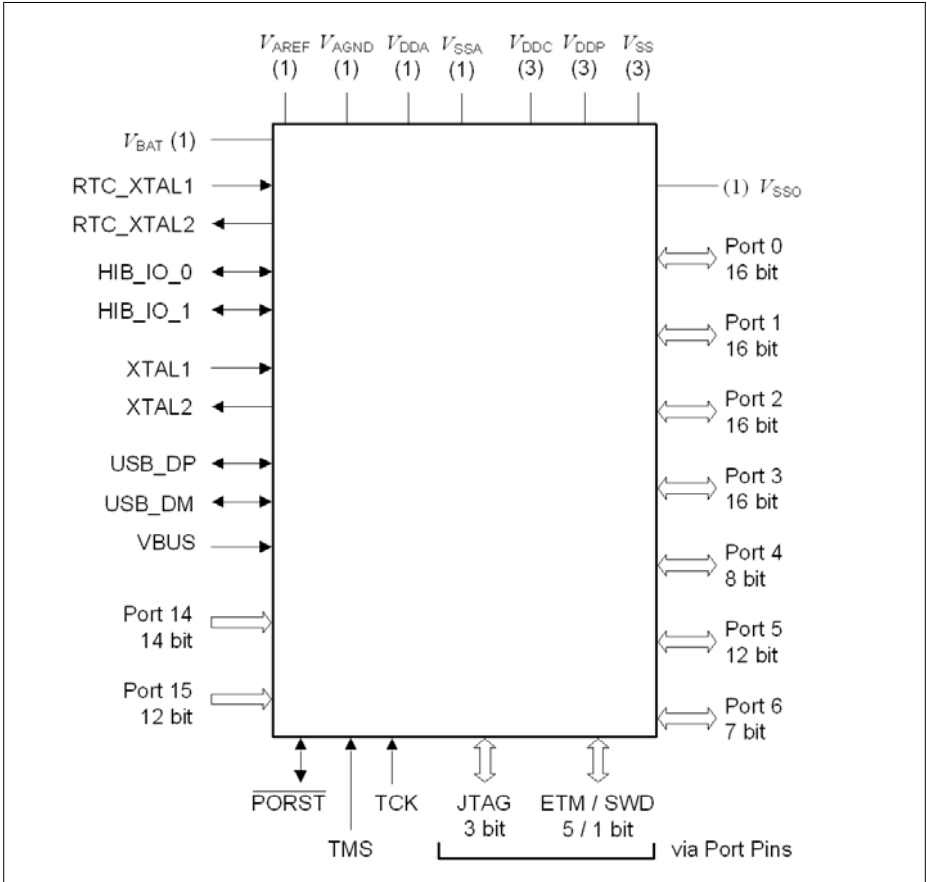


Figure 3 XMC4500 Logic Symbol PG-LFBGA-144

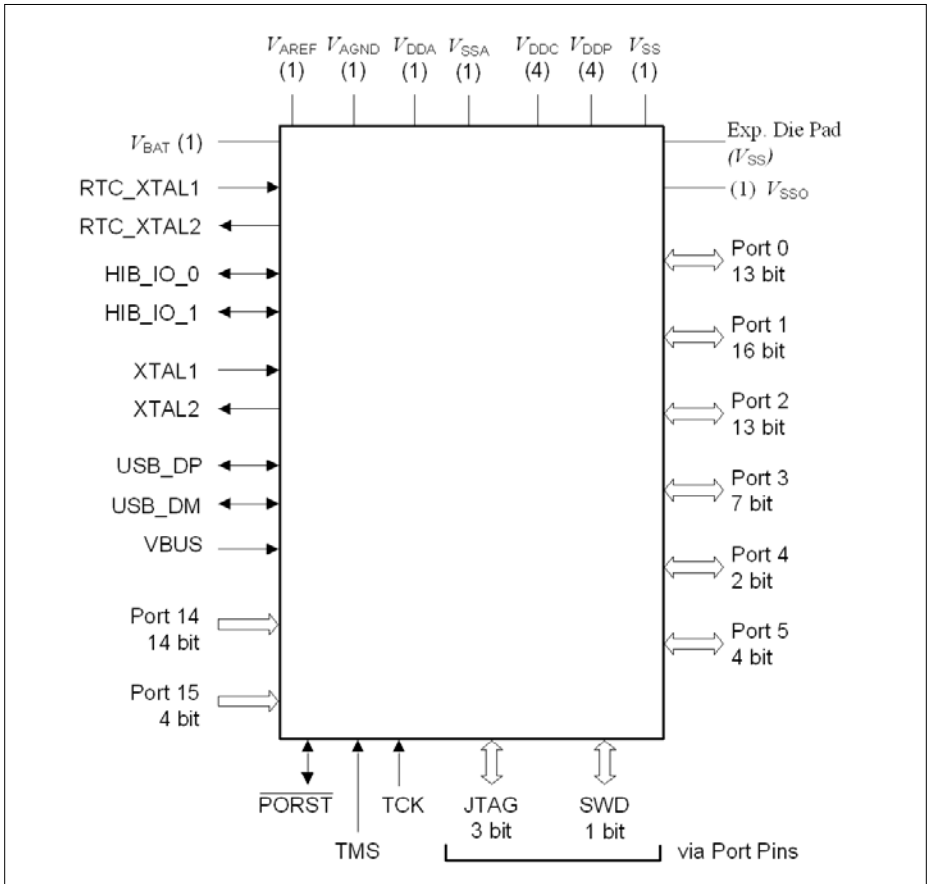


Figure 4 XMC4500 Logic Symbol PG-LQFP-100

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the four sides of the different packages.

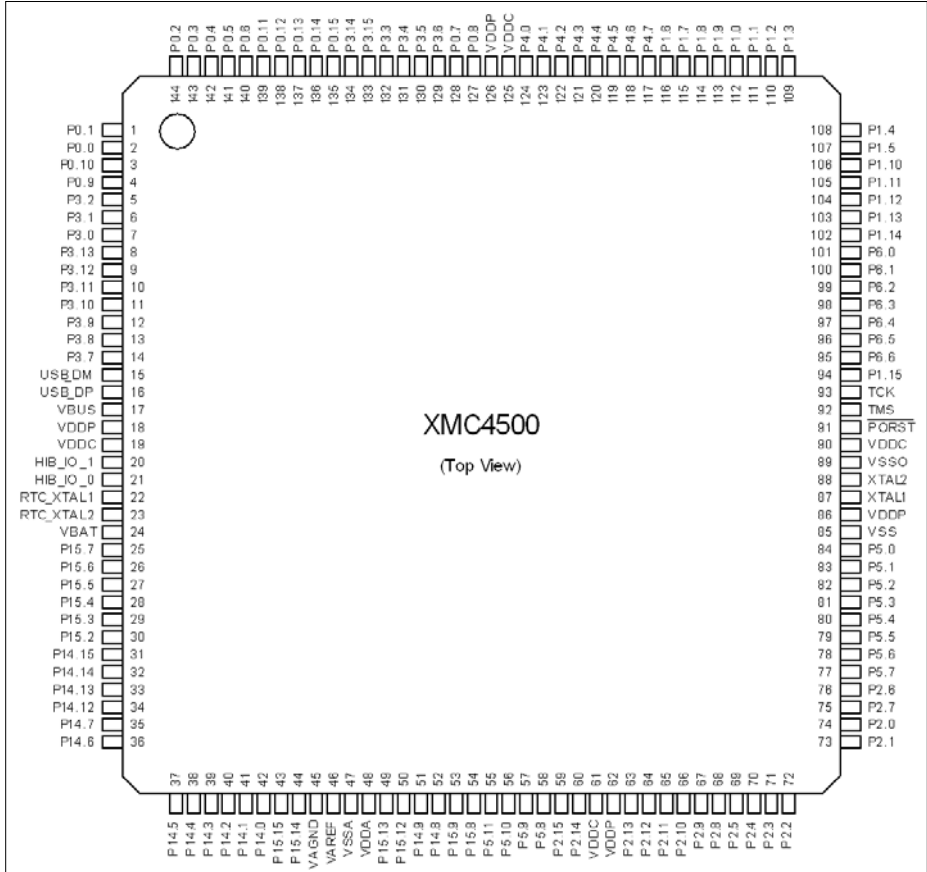


Figure 5 XMC4500 PG-LQFP-144 Pin Configuration (top view)

General Device Information

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | |
|---|---------------|---------------|-------------|-------------|--------|-------|-------|-------|------|-------|---------------------------|-------|---|
| A | VSS | VDDC | P0.2 | P0.3 | P0.5 | P0.6 | P3.6 | P0.8 | P4.1 | P1.8 | VDDP | VSS | A |
| B | VDDP | P3.1 | P3.2 | P0.10 | P0.4 | P3.5 | P0.7 | P4.0 | P1.6 | P1.7 | P1.9 | VDDC | B |
| C | P3.0 | P3.13 | P0.1 | P0.0 | P0.13 | P0.15 | P4.4 | P4.6 | P4.7 | P1.4 | P1.2 | P1.3 | C |
| D | USB_D M | P3.12 | P3.11 | P0.9 | P0.12 | P3.14 | P3.15 | P4.5 | P1.0 | P1.5 | P1.11 | P1.10 | D |
| E | USB_D P | VBUS | P3.8 | P3.7 | P0.11 | P0.14 | P3.4 | P4.2 | P1.1 | P1.14 | P1.12 | P1.13 | E |
| F | RTC_X TAL2 | RTC_X TAL1 | HB_I O_1 | HB_I O_0 | P3.9 | P3.10 | P3.3 | P4.3 | P6.1 | P6.4 | P6.5 | P6.6 | F |
| G | VBAT | P15.3 | P15.5 | P15.4 | P15.6 | P15.7 | TMS | TCK | P6.3 | P6.0 | $\overline{\text{PORST}}$ | P1.15 | G |
| H | P15.2 | P14.15 | P14.14 | P14.13 | P5.10 | P5.8 | P5.2 | P5.1 | P5.0 | P6.2 | XTAL1 | XTAL2 | H |
| J | P14.12 | P14.7 | P14.6 | P14.3 | P5.11 | P2.15 | P5.7 | P5.5 | P2.6 | P5.3 | P2.0 | VSSO | J |
| K | P14.4 | P14.5 | P14.2 | P15.15 | P15.12 | P5.9 | P2.14 | P5.6 | P2.7 | P5.4 | P2.2 | P2.1 | K |
| L | VDDA | P14.1 | P14.0 | P15.14 | P14.9 | P15.9 | P2.12 | P2.10 | P2.8 | P2.4 | P2.3 | VDDP | L |
| M | VSSA | VAGND | VAREF | P15.13 | P14.8 | P15.8 | P2.13 | P2.11 | P2.9 | P2.5 | VDDC | VSS | M |

1 2 3 4 5 6 7 8 9 10 11 12
XMC4500- (top view)

Figure 6 XMC4500 PG-LFBGA-144 Pin Configuration (top view)

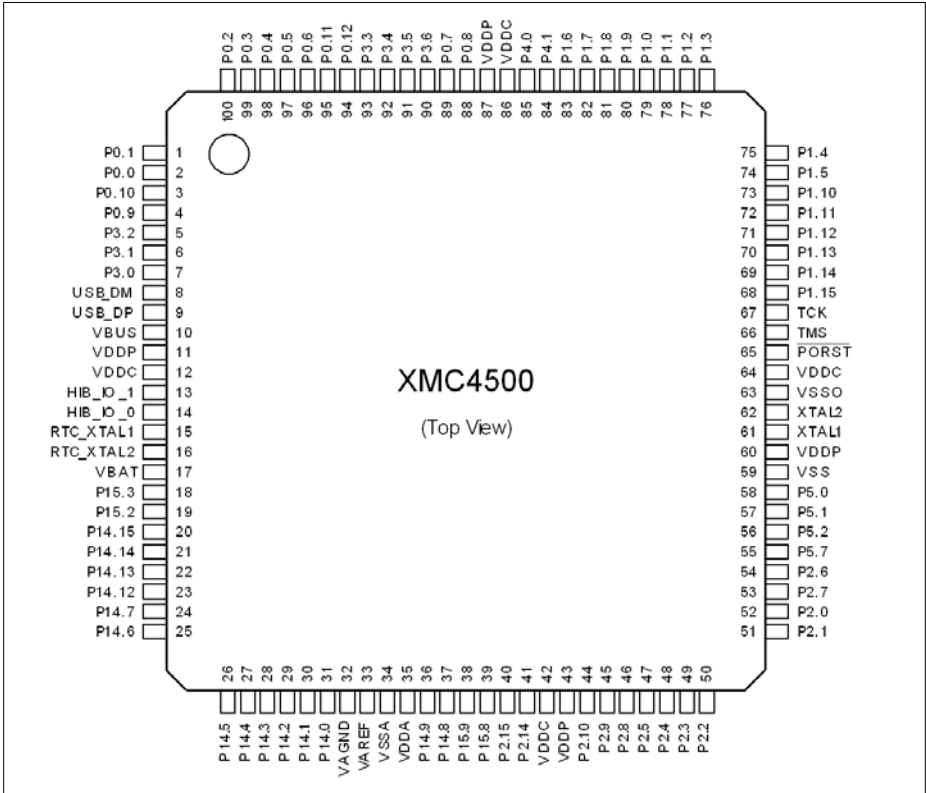


Figure 7 XMC4500 PG-LQFP-100 Pin Configuration (top view)

2.2.1 Package Pin Summary

The following general scheme is used to describe each pin:

Table 8 Package Pin Mapping Description

| Function | Package A | Package B | ... | Pad Type | Notes |
|----------|-----------|-----------|-----|----------|-------|
| Name | N | Ax | ... | A2 | |

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the dedicated pins (i.e. $\overline{\text{PORST}}$) and supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type (A1, A1+, A2, special=special pad, In=input pad, AN/DIG_IN=analog and digital input, Power=power supply). Details about the pad properties are defined in the Electrical Parameters.

In the “Notes”, special information to the respective pin/function is given, i.e. deviations from the default configuration after reset. Per default the regular Port pins are configured as direct input with no internal pull device active.

Table 9 Package Pin Mapping

| Function | LQFP-144 | LFBGA-144 | LQFP-100 | Pad Type | Notes |
|----------|----------|-----------|----------|----------|--|
| P0.0 | 2 | C4 | 2 | A1+ | |
| P0.1 | 1 | C3 | 1 | A1+ | |
| P0.2 | 144 | A3 | 100 | A2 | |
| P0.3 | 143 | A4 | 99 | A2 | |
| P0.4 | 142 | B5 | 98 | A2 | |
| P0.5 | 141 | A5 | 97 | A2 | |
| P0.6 | 140 | A6 | 96 | A2 | |
| P0.7 | 128 | B7 | 89 | A2 | After a system reset, via HWSEL this pin selects the DB.TDI function. |
| P0.8 | 127 | A8 | 88 | A2 | After a system reset, via HWSEL this pin selects the $\overline{\text{DB.TRST}}$ function, with a weak pull-down active. |
| P0.9 | 4 | D4 | 4 | A2 | |
| P0.10 | 3 | B4 | 3 | A1+ | |

General Device Information
Table 9 Package Pin Mapping (cont'd)

| Function | LQFP-144 | LFBGA-144 | LQFP-100 | Pad Type | Notes |
|----------|----------|-----------|----------|----------|---|
| P0.11 | 139 | E5 | 95 | A1+ | |
| P0.12 | 138 | D5 | 94 | A1+ | |
| P0.13 | 137 | C5 | - | A1+ | |
| P0.14 | 136 | E6 | - | A1+ | |
| P0.15 | 135 | C6 | - | A1+ | |
| P1.0 | 112 | D9 | 79 | A1+ | |
| P1.1 | 111 | E9 | 78 | A1+ | |
| P1.2 | 110 | C11 | 77 | A2 | |
| P1.3 | 109 | C12 | 76 | A2 | |
| P1.4 | 108 | C10 | 75 | A1+ | |
| P1.5 | 107 | D10 | 74 | A1+ | |
| P1.6 | 116 | B9 | 83 | A2 | |
| P1.7 | 115 | B10 | 82 | A2 | |
| P1.8 | 114 | A10 | 81 | A2 | |
| P1.9 | 113 | B11 | 80 | A2 | |
| P1.10 | 106 | D12 | 73 | A1+ | |
| P1.11 | 105 | D11 | 72 | A1+ | |
| P1.12 | 104 | E11 | 71 | A2 | |
| P1.13 | 103 | E12 | 70 | A2 | |
| P1.14 | 102 | E10 | 69 | A2 | |
| P1.15 | 94 | G12 | 68 | A2 | |
| P2.0 | 74 | J11 | 52 | A2 | |
| P2.1 | 73 | K12 | 51 | A2 | After a system reset, via HWSEL this pin selects the DB.TDO function. |
| P2.2 | 72 | K11 | 50 | A2 | |
| P2.3 | 71 | L11 | 49 | A2 | |
| P2.4 | 70 | L10 | 48 | A2 | |
| P2.5 | 69 | M10 | 47 | A2 | |
| P2.6 | 76 | J9 | 54 | A1+ | |
| P2.7 | 75 | K9 | 53 | A1+ | |
| P2.8 | 68 | L9 | 46 | A2 | |
| P2.9 | 67 | M9 | 45 | A2 | |

General Device Information

Table 9 Package Pin Mapping (cont'd)

| Function | LQFP-144 | LFBGA-144 | LQFP-100 | Pad Type | Notes |
|----------|----------|-----------|----------|----------|-------|
| P2.10 | 66 | L8 | 44 | A2 | |
| P2.11 | 65 | M8 | - | A2 | |
| P2.12 | 64 | L7 | - | A2 | |
| P2.13 | 63 | M7 | - | A2 | |
| P2.14 | 60 | K7 | 41 | A2 | |
| P2.15 | 59 | J6 | 40 | A2 | |
| P3.0 | 7 | C1 | 7 | A2 | |
| P3.1 | 6 | B2 | 6 | A2 | |
| P3.2 | 5 | B3 | 5 | A2 | |
| P3.3 | 132 | F7 | 93 | A1+ | |
| P3.4 | 131 | E7 | 92 | A1+ | |
| P3.5 | 130 | B6 | 91 | A2 | |
| P3.6 | 129 | A7 | 90 | A2 | |
| P3.7 | 14 | E4 | - | A1+ | |
| P3.8 | 13 | E3 | - | A1+ | |
| P3.9 | 12 | F5 | - | A1+ | |
| P3.10 | 11 | F6 | - | A1+ | |
| P3.11 | 10 | D3 | - | A1+ | |
| P3.12 | 9 | D2 | - | A2 | |
| P3.13 | 8 | C2 | - | A2 | |
| P3.14 | 134 | D6 | - | A1+ | |
| P3.15 | 133 | D7 | - | A1+ | |
| P4.0 | 124 | B8 | 85 | A2 | |
| P4.1 | 123 | A9 | 84 | A2 | |
| P4.2 | 122 | E8 | - | A1+ | |
| P4.3 | 121 | F8 | - | A1+ | |
| P4.4 | 120 | C7 | - | A1+ | |
| P4.5 | 119 | D8 | - | A1+ | |
| P4.6 | 118 | C8 | - | A1+ | |
| P4.7 | 117 | C9 | - | A1+ | |
| P5.0 | 84 | H9 | 58 | A1+ | |
| P5.1 | 83 | H8 | 57 | A1+ | |
| P5.2 | 82 | H7 | 56 | A1+ | |

General Device Information

Table 9 Package Pin Mapping (cont'd)

| Function | LQFP-144 | LFBGA-144 | LQFP-100 | Pad Type | Notes |
|----------|----------|-----------|----------|-------------------|-------|
| P5.3 | 81 | J10 | - | A2 | |
| P5.4 | 80 | K10 | - | A2 | |
| P5.5 | 79 | J8 | - | A2 | |
| P5.6 | 78 | K8 | - | A2 | |
| P5.7 | 77 | J7 | 55 | A1+ | |
| P5.8 | 58 | H6 | - | A2 | |
| P5.9 | 57 | K6 | - | A2 | |
| P5.10 | 56 | H5 | - | A1+ | |
| P5.11 | 55 | J5 | - | A1+ | |
| P6.0 | 101 | G10 | - | A2 | |
| P6.1 | 100 | F9 | - | A2 | |
| P6.2 | 99 | H10 | - | A2 | |
| P6.3 | 98 | G9 | - | A1+ | |
| P6.4 | 97 | F10 | - | A2 | |
| P6.5 | 96 | F11 | - | A2 | |
| P6.6 | 95 | F12 | - | A2 | |
| P14.0 | 42 | L3 | 31 | AN/DIG_IN | |
| P14.1 | 41 | L2 | 30 | AN/DIG_IN | |
| P14.2 | 40 | K3 | 29 | AN/DIG_IN | |
| P14.3 | 39 | J4 | 28 | AN/DIG_IN | |
| P14.4 | 38 | K1 | 27 | AN/DIG_IN | |
| P14.5 | 37 | K2 | 26 | AN/DIG_IN | |
| P14.6 | 36 | J3 | 25 | AN/DIG_IN | |
| P14.7 | 35 | J2 | 24 | AN/DIG_IN | |
| P14.8 | 52 | M5 | 37 | AN/DAC/DI G_IN | |
| P14.9 | 51 | L5 | 36 | AN/DAC/DI G_IN | |
| P14.12 | 34 | J1 | 23 | AN/DIG_IN | |
| P14.13 | 33 | H4 | 22 | AN/DIG_IN | |
| P14.14 | 32 | H3 | 21 | AN/DIG_IN | |
| P14.15 | 31 | H2 | 20 | AN/DIG_IN | |
| P15.2 | 30 | H1 | 19 | AN/DIG_IN | |

General Device Information
Table 9 Package Pin Mapping (cont'd)

| Function | LQFP-144 | LFBGA-144 | LQFP-100 | Pad Type | Notes |
|----------|----------|-----------|----------|------------|---|
| P15.3 | 29 | G2 | 18 | AN/DIG_IN | |
| P15.4 | 28 | G4 | - | AN/DIG_IN | |
| P15.5 | 27 | G3 | - | AN/DIG_IN | |
| P15.6 | 26 | G5 | - | AN/DIG_IN | |
| P15.7 | 25 | G6 | - | AN/DIG_IN | |
| P15.8 | 54 | M6 | 39 | AN/DIG_IN | |
| P15.9 | 53 | L6 | 38 | AN/DIG_IN | |
| P15.12 | 50 | K5 | - | AN/DIG_IN | |
| P15.13 | 49 | M4 | - | AN/DIG_IN | |
| P15.14 | 44 | L4 | - | AN/DIG_IN | |
| P15.15 | 43 | K4 | - | AN/DIG_IN | |
| USB_DP | 16 | E1 | 9 | special | |
| USB_DM | 15 | D1 | 8 | special | |
| HIB_IO_0 | 21 | F4 | 14 | A1 special | At the first power-up and with every reset of the hibernate domain this pin is configured as open-drain output and drives "0". As output the medium driver mode is active. |
| HIB_IO_1 | 20 | F3 | 13 | A1 special | At the first power-up and with every reset of the hibernate domain this pin is configured as input with no pull device active. As output the medium driver mode is active. |
| TCK | 93 | G8 | 67 | A1 | Weak pull-down active. |
| TMS | 92 | G7 | 66 | A1+ | Weak pull-up active. As output the strong-soft driver mode is active. |
| PORST | 91 | G11 | 65 | special | Weak pull-up permanently active, strong pull-down controlled by EVR. |
| XTAL1 | 87 | H11 | 61 | clock_IN | |
| XTAL2 | 88 | H12 | 62 | clock_O | |

General Device Information

Table 9 Package Pin Mapping (cont'd)

| Function | LQFP-144 | LFBGA-144 | LQFP-100 | Pad Type | Notes |
|-----------|----------|-----------|----------|----------|--|
| RTC_XTAL1 | 22 | F2 | 15 | clock_IN | |
| RTC_XTAL2 | 23 | F1 | 16 | clock_O | |
| VBAT | 24 | G1 | 17 | Power | When VDDP is supplied VBAT has to be supplied as well. |
| VBUS | 17 | E2 | 10 | special | |
| VAREF | 46 | M3 | 33 | AN_Ref | |
| VAGND | 45 | M2 | 32 | AN_Ref | |
| VDDA | 48 | L1 | 35 | AN_Power | |
| VSSA | 47 | M1 | 34 | AN_Power | |
| VDDC | 19 | - | 12 | Power | |
| VDDC | 61 | - | 42 | Power | |
| VDDC | 90 | - | 64 | Power | |
| VDDC | 125 | - | 86 | Power | |
| VDDC | - | A2 | - | Power | |
| VDDC | - | B12 | - | Power | |
| VDDC | - | M11 | - | Power | |
| VDDP | 18 | - | 11 | Power | |
| VDDP | 62 | - | 43 | Power | |
| VDDP | 86 | - | 60 | Power | |
| VDDP | 126 | - | 87 | Power | |
| VDDP | - | A11 | - | Power | |
| VDDP | - | B1 | - | Power | |
| VDDP | - | L12 | - | Power | |
| VSS | 85 | - | 59 | Power | |
| VSS | - | A1 | - | Power | |
| VSS | - | A12 | - | Power | |
| VSS | - | M12 | - | Power | |

General Device Information

Table 9 Package Pin Mapping (cont'd)

| Function | LQFP-144 | LFBGA-144 | LQFP-100 | Pad Type | Notes |
|----------|----------|-----------|----------|----------|---|
| VSSO | 89 | J12 | 63 | Power | |
| VSS | Exp. Pad | - | Exp. Pad | Power | <p>Exposed Die Pad The exposed die pad is connected internally to VSS. For proper operation, it is mandatory to connect the exposed pad directly to the common ground on the board. For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.</p> |

2.2.2 Port I/O Functions

The following general scheme is used to describe each Port pin:

Table 10 Port I/O Function Description

| Function | Outputs | | | Inputs | | |
|----------|----------|----------|----------|----------|----------|----------|
| | ALT1 | ALTn | HWO0 | HWI0 | Input | Input |
| P0.0 | | MODA.OUT | MODB.OUT | MODB.INA | MODC.INA | |
| Pn.y | MODA.OUT | | | | MODA.INA | MODC.INB |

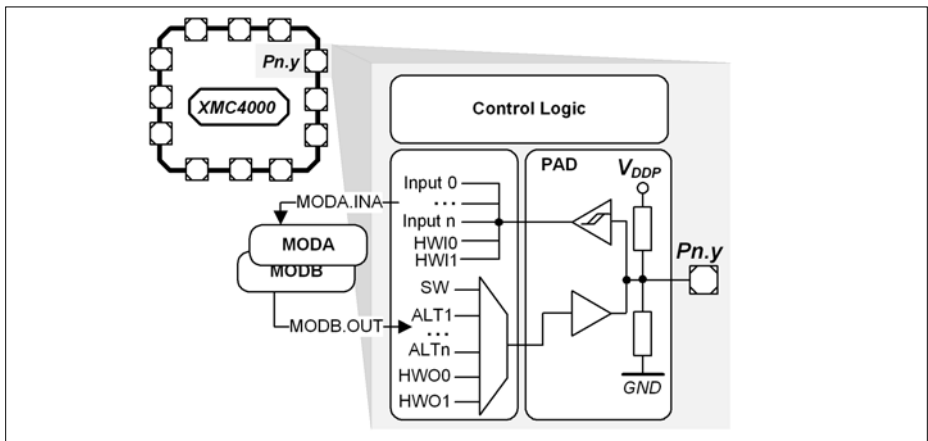


Figure 8 Simplified Port Structure

$Pn.y$ is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via $Pn_IN.y$, Pn_OUT defines the output value.

Up to four alternate output functions (ALT1/2/3/4) can be mapped to a single port pin, selected by $Pn_IOCR.PC$. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL it is possible to select between different hardware “masters” ($HWO0/HWI0$, $HWO1/HWI1$). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

2.2.2.1 Port I/O Function Table

Table 11 Port I/O Functions

| Function | Outputs | | | | | | Inputs | | | | | | | |
|----------|------------------|--------------|-------|-------------|------------|----------|------------|----------|--------------|---------------|-----------|-----------|-----------|---------------|
| | ALT1 | ALT2 | ALT3 | ALT4 | HWC00 | HWC01 | HWC10 | HW11 | Input | Input | Input | Input | Input | Input |
| P0.0 | | CAN_ML7XD | CC180 | LED7S0_C0L2 | | | | | U1C1_DVDD | ETH0_CK1_RMIB | ERL0_0B0 | | | ETH0_CK1_RMIB |
| P0.1 | USB_DRV6V/BUS | U1C1_DOU70 | CC180 | LED7S0_C0L3 | | | | | ETH0_CRSD_VB | ERL0_0A0 | ERL0_0A0 | | | ETH0_RXD0VB |
| P0.2 | | U1C1_SEL01 | CC180 | DOU71 | U1C0_DOU73 | ERL1_A09 | U1C0_HWN3 | ERL1_D0 | ETH0_RXD0B | ERL1_3B3 | ERL1_3B3 | | | |
| P0.3 | | CC180 | DOU72 | U1C0 | U1C0 | ERL1_A09 | U1C0_HWN2 | ERL1_D1 | ETH0_RXD1B | ERL1_3B0 | ERL1_3B0 | | | |
| P0.4 | ETH0_TALEN | | CC180 | DOU70 | U1C0 | ERL1_A09 | U1C0_HWN1 | ERL1_D2 | U1C0_D0A0 | ERL0_2B5 | ERL0_2B5 | | | |
| P0.5 | ETH0_T0D0 | U1C0_DOU70 | CC180 | DOU70 | U1C0 | ERL1_A09 | U1C0_HWN0 | ERL1_D3 | U1C0_DX0B | ERL1_3A0 | ERL1_3A0 | | | |
| P0.6 | ETH0_T0D1 | U1C0_SEL00 | CC180 | DOU70 | ER1_A07 | ERL1_A09 | | | U1C0_DX2A | ERL0_3B2 | ERL0_3B2 | CC180_NZB | | CC180_NZB |
| P0.7 | WWDV_SERVICE_OUT | U1C0_SEL00 | CC180 | DOU70 | ERL1_A09 | ERL1_A09 | U1C0_D8 | ERL1_D6 | U1C0_DS0 | ERL0_2B1 | ERL0_2B1 | CC180_NGA | CC180_NGA | CC180_IN3A |
| P0.8 | SQU_EXCLK | U1C0_SCLKOUT | CC180 | DOU70 | ERL1_A09 | ERL1_A09 | U1C0_T0D1 | ERL1_D7 | U1C0_DIN0A | ERL0_2A1 | ERL0_2A1 | CC180_N1B | | |
| P0.9 | | U1C1_SEL00 | CC180 | DOU72 | ERL1_A09 | ERL1_A09 | U1C0_D0A0 | | U1C1_D0A0 | ERL0_0B1 | ERL0_0B1 | | | |
| P0.10 | ETH0_MDC | U1C1_SCLKOUT | CC180 | DOU72 | | | U1C1_D0A1 | | U1C1_D0A1 | ERL0_1A0 | ERL0_1A0 | | | |
| P0.11 | | U1C0_SCLKOUT | CC180 | DOU73 | SWMVC_RST | ERL1_B09 | U1C0_DX1A | | ETH0_RX0RB | ERL0_3A2 | ERL0_3A2 | | | |
| P0.12 | | U1C1_SEL00 | CC180 | DOU73 | ERL1_A09 | ERL1_A09 | U1C1_HELDA | | U1C1_DX2B | ERL0_2B2 | ERL0_2B2 | | | |
| P0.13 | | U1C1_SCLKOUT | CC180 | DOU72 | | | U1C1 | | U1C1_DX1B | ERL0_2A2 | ERL0_2A2 | | | |
| P0.14 | | U1C0_SEL00 | CC180 | DOU71 | U1C1_DOU73 | ERL1_A09 | U1C1_HWN3 | | | CC180_NZC | CC180_NZC | | | |
| P0.15 | | U1C0_SEL00 | CC180 | DOU70 | U1C1_DOU72 | ERL1_A09 | U1C1_HWN2 | | | CC180_N1C | CC180_N1C | | | |
| P1.0 | DSD_CSPWMM | U1C0_SEL00 | CC180 | DOU73 | ERL1_A09 | ERL1_A09 | U1C0_D0A0 | | U1C0_D0A0 | ERL0_3B0 | ERL0_3B0 | CC180_N3A | | CC180_N3A |
| P1.1 | DSD_CSPWMP | U1C0_SCLKOUT | CC180 | DOU72 | SDMVC_SWVC | ERL1_A09 | U1C0_DX1A | | U1C0_PO3F0 | ERL0_N2A | ERL0_N2A | CC180_N2A | | CC180_N2A |
| P1.2 | | U1C0_SEL00 | CC180 | DOU71 | ERL1_A09 | ERL1_A09 | U1C0_HWN3 | ERL1_D14 | U1C0_PO3F0 | ERL1_2B0 | ERL1_2B0 | CC180_N1A | | CC180_N1A |
| P1.3 | | U1C0_MCLKOUT | CC180 | DOU70 | ERL1_A09 | ERL1_A09 | U1C0_HWN2 | ERL1_D15 | U1C0_PO3F0 | ERL1_2A0 | ERL1_2A0 | CC180_N0A | | CC180_N0A |
| P1.4 | WWDV_SERVICE_OUT | CAN_ML7XD | CC180 | DOU71 | U1C0_DOU73 | ERL1_A09 | U1C0_HWN1 | | U1C0_PO3F0 | ERL0_2B5 | ERL0_2B5 | CC180_N1C | | CC180_N1C |

Table 11 Port I/O Functions (cont'd)

| Function | Outputs | | | | | Inputs | | | | | | | | | | |
|----------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| | ALT1 | ALT2 | ALT3 | ALT4 | HW00 | HW01 | HW10 | HW11 | Input | Input | Input | Input | Input | Input | Input | Input |
| P1.5 | CAN_NL_TXD | UC03_DOUT9 | CC181_OUT10 | UC03_DOUT0 | UC03_DOUT0 | UC03_DOUT0 | UC03_HW10 | UC03_DOUT0 | UC03_DOUT0 | CAN_NL_RXDA | ERU0_ZAD | ERU1_GAO | CC141_NVIC | DS0_DIN2B | | |
| P1.6 | UC03_SCKOUT | UC03_SCKOUT | DS0_MCLK2 | DS0_MCLK2 | DS0_MCLK2 | DS0_MCLK2 | DS0_MCLK2 | DS0_MCLK2 | DS0_MCLK2 | DS0_MCLK2 | | | | | | |
| P1.7 | UC03_SCKOUT | UC03_SCKOUT | DS0_MCLK2 | DS0_MCLK2 | DS0_MCLK2 | DS0_MCLK2 | DS0_MCLK2 | DS0_MCLK2 | DS0_MCLK2 | DS0_MCLK2 | | | | | | |
| P1.8 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | CAN_NL_RXDA | DS0_MCLK2 | | | | | |
| P1.9 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | CAN_NL_RXDA | DS0_MCLK2 | | | | | |
| P1.10 | ETH0_MDC | UC03_SCKOUT | CC181_OUT11 | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT |
| P1.11 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 |
| P1.12 | ETH0_TX_EN | CAN_NL_TXD | CC181_OUT11 | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT |
| P1.13 | ETH0_TXD0 | UC03_SEL0 | CC181_OUT11 | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT |
| P1.14 | ETH0_TXD1 | UC03_SEL0 | CC181_OUT11 | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT |
| P1.15 | SCU_EXCLK | UC03_SEL0 | CC181_OUT11 | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT |
| P2.0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 |
| P2.1 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 |
| P2.2 | VADC_EMU00D | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 |
| P2.3 | VADC_EMU00R | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 |
| P2.4 | VADC_EMU00Z | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 |
| P2.5 | ETH0_TX_EN | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 |
| P2.6 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 |
| P2.7 | ETH0_MDC | CAN_NL_TXD | CC181_OUT11 | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT |
| P2.8 | ETH0_TXD0 | UC03_SEL0 | CC181_OUT11 | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT |
| P2.9 | ETH0_TXD1 | UC03_SEL0 | CC181_OUT11 | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT |
| P2.10 | VADC_EMU00D | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 | UC03_SEL0 |
| P2.11 | ETH0_TXR | UC03_SEL0 | CC181_OUT11 | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT | UC03_SCKOUT |

Table 11 Port I/O Functions (cont'd)

| Function | Outputs | | | | | | Inputs | | | | | | | |
|----------|---------------|--------------|-------------|-------------------------------------|-------------------------|----------|---------------|----------|----------|----------|------------|------------|------------|------------|
| | ALT1 | ALT2 | ALT3 | ALT4 | HW00 | HW01 | HWI0 | HWI1 | Input | Input | Input | Input | Input | Input |
| P2.12 | ETH0_TMD2 | ETH0_TMD3 | COH41_OUT33 | ETH0_TXD0 ETH0_TXD1 ETH0_TXD2 | DB_ETM_TRACE_DA TA1 | ERU_AD30 | ERU_D30 | ERU_D31 | UIC0_D30 | UIC0_D31 | COH43_IN3C | COH43_IN3C | | |
| P2.13 | ETH0_TMD3 | ETH0_TMD4 | COH41_OUT34 | ETH0_TXD1 ETH0_TXD2 | DB_ETM_TRACE_DA TA0 | ERU_AD31 | ERU_D31 | ERU_D32 | UIC0_D31 | UIC0_D32 | COH43_IN3C | COH43_IN3C | | |
| P2.14 | VADC_EMU_A11 | UIC0_DOUT0 | COH40_OUT21 | LEDTS0_LINE9 | DB_ETM_TRACE_CLK B02 | ERIT_B02 | LEDTS0_TSINA | ERU_D32 | UIC0_D32 | UIC0_D33 | COH43_IN3B | COH43_IN3B | COH43_IN3B | COH43_IN3B |
| P2.15 | VADC_EMU_A12 | UIC0_DOUT1 | COH40_OUT22 | LEDTS0_LINE8 | EXTENDE06 BCT | ERIT_BCT | LEDTS0_TSINB | ERU_D33 | UIC0_D33 | UIC0_D34 | COH42_IN3B | COH42_IN3B | COH42_IN3B | COH42_IN3B |
| P3.0 | UIC1_SELO0 | UIC1_SCLKOUT | COH42_OUT0 | UIC1_SEL0 | ERIT_B03 | ERIT_B03 | UIC1_D34 | UIC1_D35 | UIC1_D34 | UIC1_D35 | COH40_IN3C | COH40_IN3C | COH40_IN3C | COH40_IN3C |
| P3.1 | USB_DRIVE/USB | CAN_M0_TX0 | LEDTS0_COA | LEDTS0_COA | ERIT_H03/WR | ERIT_C50 | | | ERU_D35 | ERU_D36 | COH40_IN3C | COH40_IN3C | COH40_IN3C | COH40_IN3C |
| P3.2 | UIC1_SELO1 | UIC1_SCLKOUT | COH42_OUT1 | UIC1_SEL1 | SWMMC_CPL_OUT | ERIT_C50 | | | ERU_D36 | ERU_D37 | COH40_IN3C | COH40_IN3C | COH40_IN3C | COH40_IN3C |
| P3.3 | UIC1_SELO2 | UIC1_SCLKOUT | COH42_OUT2 | UIC1_SEL2 | SWMMC_LED | ERIT_C50 | | | ERU_D37 | ERU_D38 | COH42_IN3A | COH42_IN3A | COH42_IN3A | COH42_IN3A |
| P3.4 | UIC1_SELO3 | UIC1_SCLKOUT | COH42_OUT3 | UIC1_SEL3 | SWMMC_BIS_POWER | ERIT_C50 | | | ERU_D38 | ERU_D39 | COH42_IN3A | COH42_IN3A | COH42_IN3A | COH42_IN3A |
| P3.5 | UIC1_SELO4 | UIC1_SCLKOUT | COH42_OUT4 | UIC1_SEL4 | SWMMC_CMD_OUT | ERU_A54 | SWMMC_CMD_IN | ERU_D39 | UIC1_D39 | UIC1_D40 | COH42_IN3A | COH42_IN3A | COH42_IN3A | COH42_IN3A |
| P3.6 | UIC1_SELO5 | UIC1_SCLKOUT | COH42_OUT5 | UIC1_SEL5 | SWMMC_CPL_OUT | ERU_A55 | SWMMC_CMD_IN | ERU_D40 | UIC1_D40 | UIC1_D41 | COH42_IN3A | COH42_IN3A | COH42_IN3A | COH42_IN3A |
| P3.7 | UIC1_SELO6 | UIC1_SCLKOUT | COH41_OUT6 | LEDTS0_LINE0 | SWMMC_CPL_OUT | ERU_A55 | | | UIC0_D41 | UIC0_D42 | COH42_IN3A | COH42_IN3A | COH42_IN3A | COH42_IN3A |
| P3.8 | UIC0_SELO | UIC0_SCLKOUT | COH41_OUT7 | LEDTS0_LINE1 | | | | | UIC0_D42 | UIC0_D43 | COH42_IN3A | COH42_IN3A | COH42_IN3A | COH42_IN3A |
| P3.9 | UIC0_SELO1 | UIC0_SCLKOUT | COH41_OUT8 | LEDTS0_LINE2 | | | | | UIC0_D43 | UIC0_D44 | COH42_IN3A | COH42_IN3A | COH42_IN3A | COH42_IN3A |
| P3.10 | UIC0_SELO2 | UIC0_SCLKOUT | COH41_OUT9 | LEDTS0_LINE3 | | | | | UIC0_D44 | UIC0_D45 | COH42_IN3A | COH42_IN3A | COH42_IN3A | COH42_IN3A |
| P3.11 | UIC0_SELO3 | UIC0_SCLKOUT | COH42_OUT0 | LEDTS0_LINE4 | | | | | UIC0_D45 | UIC0_D46 | COH42_IN3A | COH42_IN3A | COH42_IN3A | COH42_IN3A |
| P3.12 | UIC0_SELO4 | UIC0_SCLKOUT | COH42_OUT1 | LEDTS0_LINE5 | | | | | UIC0_D46 | UIC0_D47 | COH42_IN3A | COH42_IN3A | COH42_IN3A | COH42_IN3A |
| P3.13 | UIC0_SELO5 | UIC0_SCLKOUT | COH42_OUT2 | LEDTS0_LINE6 | | | | | UIC0_D47 | UIC0_D48 | COH42_IN3A | COH42_IN3A | COH42_IN3A | COH42_IN3A |
| P3.14 | UIC0_SELO6 | UIC0_SCLKOUT | COH42_OUT3 | LEDTS0_LINE7 | | | | | UIC0_D48 | UIC0_D49 | COH42_IN3A | COH42_IN3A | COH42_IN3A | COH42_IN3A |
| P3.15 | UIC0_SELO7 | UIC0_SCLKOUT | COH41_OUT4 | LEDTS0_LINE8 | | | | | UIC0_D49 | UIC0_D50 | COH42_IN3A | COH42_IN3A | COH42_IN3A | COH42_IN3A |
| P4.0 | UIC1_SELO | UIC1_SCLKOUT | COH41_OUT5 | LEDTS0_LINE9 | SWMMC_DATA_OUT | ERU_A59 | SWMMC_DATA_IN | ERU_D50 | UIC1_D50 | UIC1_D51 | COH42_IN3C | COH42_IN3C | COH42_IN3C | COH42_IN3C |
| P4.1 | UIC1_SELO1 | UIC1_SCLKOUT | COH41_OUT6 | LEDTS0_LINE0 | SWMMC_DATA_OUT | ERU_A59 | SWMMC_DATA_IN | ERU_D51 | UIC1_D51 | UIC1_D52 | COH42_IN3C | COH42_IN3C | COH42_IN3C | COH42_IN3C |
| P4.2 | UIC1_SELO2 | UIC1_SCLKOUT | COH41_OUT7 | LEDTS0_LINE1 | SWMMC_DATA_OUT | ERU_A59 | SWMMC_DATA_IN | ERU_D52 | UIC1_D52 | UIC1_D53 | COH42_IN3C | COH42_IN3C | COH42_IN3C | COH42_IN3C |

Table 11 Port I/O Functions (cont'd)

| Function | Outputs | | | | | Inputs | | | | | | | | | | |
|----------|-----------------|------------------|-----------------|---------------------|------|--------|------------------|-------------------|--------------------|-------|-------|-------|-------|-------|---------------|----------------|
| | ALT1 | ALT2 | ALT3 | ALT4 | HW00 | HW01 | HW10 | HW11 | Input | Input | Input | Input | Input | Input | Input | Input |
| P4.3 | UC11 SELO2 | UC00 SELO5 | CC143 OUT3 | | | | | | | | | | | | CC143 IN5A | |
| P4.4 | | UC01 SELO4 | CC143 OUT2 | UC11 DOU13 | | | UC11 HW10 | | | | | | | | CC143 IN5A | |
| P4.5 | | UC00 SELO3 | CC143 OUT1 | UC11 DOU12 | | | UC11 HW10 | | | | | | | | CC143 IN5A | |
| P4.6 | | UC00 SELO2 | CC143 OUT0 | UC11 DOU11 | | | UC11 HW11 | CAN, NZ_PWD | | | | | | | CC143 IN5A | |
| P4.7 | | CAN, NZ_TXD | | UC11 DOU10 | | | UC11 HW10 | UC11 DX5C | | | | | | | CC143 IN5C | |
| P5.0 | UC00 DOU10 | PSD, COP_PWIN | CC181 OUT3 | UC00 DOU10 | | | UC00 HW10 | UC00 DX0B | ETH0, RXD0D | | | | | | CC181 IN5A | CC181 IN5A |
| P5.1 | UC01 DOU10 | PSD, COP_PWP | CC181 OUT2 | UC00 DOU11 | | | UC00 HW11 | UC00 DX0A | ETH0, RXD1D | | | | | | CC181 IN5B | |
| P5.2 | UC00 SCK/OUT | | CC181 OUT1 | | | | | UC00 DX1A | ETH0, CARE_DV1D | | | | | | CC181 IN1B | ETH0, RXD1D |
| P5.3 | UC00 SELO0 | | CC181 OUT2 | ERU ONE | | | | UC00 DX0A | ETH0, RXERD | | | | | | CC181 IN2B | |
| P5.4 | UC00 SELO1 | | CC181 OUT13 | ER1T RCS | | | | | ETH0, CRSD | | | | | | CC181 IN3B | |
| P5.5 | UC00 SELO2 | | CC181 OUT12 | ER1T CRS | | | | | ETH0, COLD | | | | | | | |
| P5.6 | UC00 SELO3 | | CC181 OUT103 | ERU BFCL1D | | | | ERU BFCL1I | | | | | | | | |
| P5.7 | | | CC181 OUT102 | UC00 DOU12 | | | UC00 HW10 | | | | | | | | | |
| P5.8 | UC00 SCK/OUT | | CC180 OUT01 | ERU SCK1MD | | | | ETH0, RXD1A | UI10, DX1B | | | | | | | |
| P5.9 | UC00 SELO0 | | CC180 OUT120 | ERU BFCL1D | | | | ETH0, RXD1A | UI10, DX2B | | | | | | | |
| P5.10 | UC00 MCK/OUT | | CC180 OUT10 | LED1S0, LINE7 | | | LED1S0, TS17A | ETH0, CLK_T1A | | | | | | | | |
| P5.11 | UC00 SELO1 | | CC180 OUT100 | | | | | ETH0, CR5A | | | | | | | | |
| P6.0 | ETH0, TXD0 | UC11 SELO1 | CC181 OUT131 | ERU ETM_TRACECLK | | | | | | | | | | | | |
| P6.1 | ETH0, TAG3 | UC11 SELO0 | CC181 OUT130 | ERU ETM_TRACECLK | | | | UC11 DX5C | | | | | | | | |
| P6.2 | ETH0, T1EN | UC11 SCK/OUT | CC143 OUT15 | ERU ETM_TRACECLK | | | | UC11 DX1C | | | | | | | | |
| P6.3 | | | CC143 OUT12 | ERU T1A2 | | | | UC11 DX5C | ETH0, RXD0B | | | | | | | |
| P6.4 | | UC11 DOU10 | CC143 OUT11 | ERU SCK1MD | | | | ERU SCK1MI | ETH0, RXD2B | | | | | | | |
| P6.5 | | UC11 MCK/OUT | CC143 OUT10 | ERU ETM_TRACECLK | | | | ETH0, CLK_RM1D | ETH0, CLK_RM1D | | | | | | | ETH0, CURV0 |

Table 11 Port I/O Functions (cont'd)

| Function | Outputs | | | | Inputs | | | | | | | | | | | |
|----------|---------|------|-----------|-----------|----------------------|----------|------|------------|------------|--------------|------------|-------|-------|---------------|-------------|--------|
| | ALT1 | ALT2 | ALT3 | ALT4 | HW00 | HW01 | HWI0 | HWI1 | Input | Input | Input | Input | Input | Input | Input | Input |
| P16.6 | | | RSD_MCLK3 | RSD_MCLK3 | RE_ETM_TRACE/EDA_TAO | BRIT_BCS | | | RSD_MCLK3A | ETH0_CLK_TXB | | | | | | |
| P14.0 | | | | | | | | VADC_G0CH0 | | | | | | | | |
| P14.1 | | | | | | | | VADC_G0CH1 | | | | | | | | |
| P14.2 | | | | | | | | VADC_G0CH2 | | | | | | | | |
| P14.3 | | | | | | | | VADC_G0CH3 | | | | | | | CAN_NO_RX0B | |
| P14.4 | | | | | | | | VADC_G0CH4 | | VADC_G2CH0 | | | | | | |
| P14.5 | | | | | | | | VADC_G0CH5 | | VADC_G2CH1 | | | | | POSF0_INZB | |
| P14.6 | | | | | | | | VADC_G0CH6 | | VADC_G2CH1 | | | | | POSF0_INB | GIORC6 |
| P14.7 | | | | | | | | VADC_G0CH7 | | | | | | | POSF0_INB | GIORC7 |
| P14.8 | | | | | DAC_OUT_0 | | | VADC_G1CH0 | | | VADC_G3CH2 | | | | ETH0_RX0DC | |
| P14.9 | | | | | DAC_OUT_1 | | | VADC_G1CH1 | | | VADC_G3CH3 | | | | ETH0_RX0DC | |
| P14.12 | | | | | | | | VADC_G1CH4 | | | | | | | | |
| P14.13 | | | | | | | | VADC_G1CH6 | | | | | | | | |
| P14.14 | | | | | | | | VADC_G1CH6 | | | | | | | | GIORC6 |
| P14.15 | | | | | | | | VADC_G1CH6 | | | | | | | | GIORC7 |
| P15.2 | | | | | | | | VADC_G2CH2 | | VADC_G2CH2 | | | | | | |
| P15.3 | | | | | | | | VADC_G2CH3 | | VADC_G2CH3 | | | | | | |
| P15.4 | | | | | | | | VADC_G2CH4 | | VADC_G2CH4 | | | | | | |
| P15.5 | | | | | | | | VADC_G2CH5 | | VADC_G2CH5 | | | | | | |
| P15.6 | | | | | | | | VADC_G2CH6 | | VADC_G2CH6 | | | | | | |
| P15.7 | | | | | | | | VADC_G2CH7 | | VADC_G2CH7 | | | | | | |
| P15.8 | | | | | | | | | | VADC_G3CH0 | | | | ETH0_CLK_RM1C | ETH0_CHRRVC | |
| P15.9 | | | | | | | | | | VADC_G3CH1 | | | | ETH0_CRS_DVC | ETH0_RX0VC | |

2.3 Power Connection Scheme

Figure 9 shows a reference power connection scheme for the XMC4500.

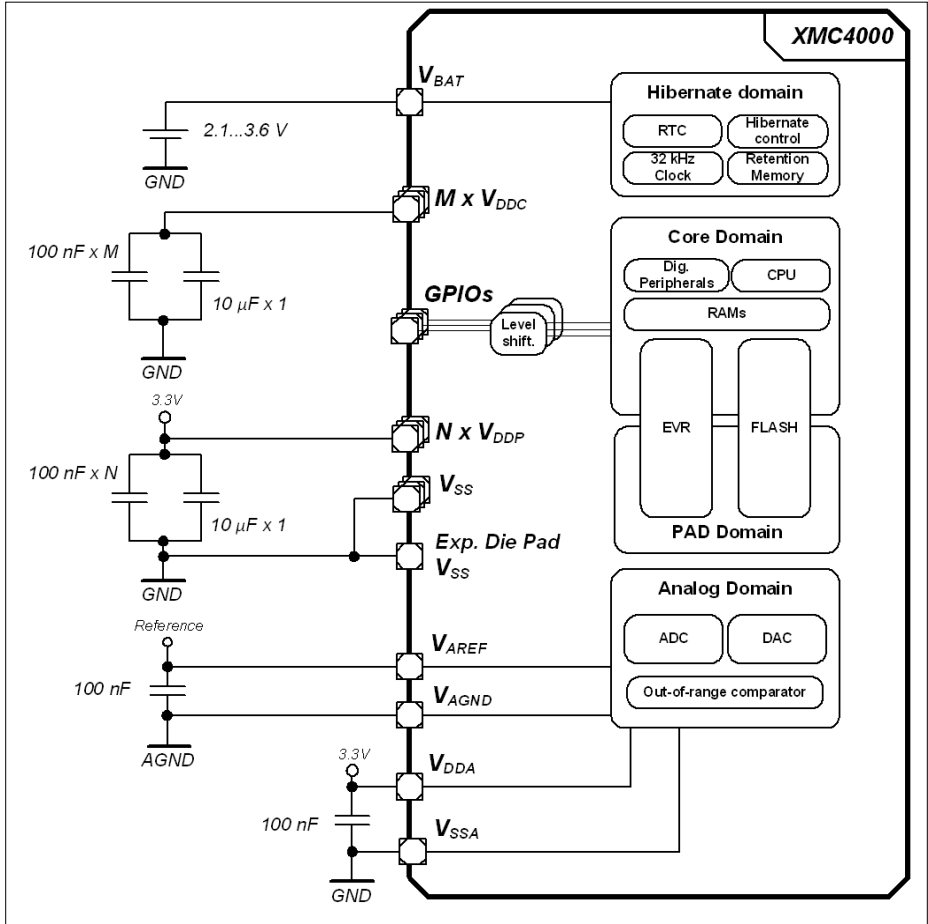


Figure 9 Power Connection Scheme

Every power supply pin needs to be connected. Different pins of the same supply need also to be externally connected. As example, all V_{DDP} pins must be connected externally to one V_{DDP} net. In this reference scheme one 100 nF capacitor is connected at each supply pin against V_{SS} . An additional 10 μ F capacitor is connected to the V_{DDP} nets and an additional 10 μ F capacitor to the V_{DDC} nets.

The XMC4500 has a common ground concept, all V_{SS} , V_{SSA} and V_{SSO} pins share the same ground potential. In packages with an exposed die pad it must be connected to the common ground as well.

V_{AGND} is the low potential to the analog reference V_{AREF} . Depending on the application it can share the common ground or have a different potential.

When V_{DDP} is supplied, V_{BAT} must be supplied as well. If no other supply source (e.g. battery) is connected to V_{BAT} , the V_{BAT} pin can also be connected directly to V_{DDP} .

3 Electrical Parameters

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the XMC4500 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with a two-letter abbreviation in column "Symbol":

- **CC**
Such parameters indicate **C**ontroller **C**haracteristics, which are a distinctive feature of the XMC4500 and must be regarded for system design.
- **SR**
Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC4500 is designed in.

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 12 Absolute Maximum Rating Parameters

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|-------------------------|----|--------|------|--------------------------------|------|-----------------------|
| | | | Min. | Typ. | Max. | | |
| Storage temperature | T_{ST} | SR | -65 | – | 150 | °C | – |
| Junction temperature | T_J | SR | -40 | – | 150 | °C | – |
| Voltage at 3.3 V power supply pins with respect to V_{SS} | V_{DDP} | SR | – | – | 4.3 | V | – |
| Voltage on any Class A and dedicated input pin with respect to V_{SS} | V_{IN} | SR | -1.0 | – | $V_{DDP} + 1.0$ or max. 4.3 | V | whichever is lower |
| Voltage on any analog input pin with respect to V_{AGND} | V_{AIN} V_{AREF} | SR | -1.0 | – | $V_{DDP} + 1.0$ or max. 4.3 | V | whichever is lower |
| Input current on any pin during overload condition | I_{IN} | SR | -10 | – | +10 | mA | |
| Absolute maximum sum of all input circuit currents for one port group during overload condition ¹⁾ | ΣI_{IN} | SR | -25 | – | +25 | mA | |
| Absolute maximum sum of all input circuit currents during overload condition | ΣI_{IN} | SR | -100 | – | +100 | mA | |

1) The port groups are defined in [Table 16](#).

Figure 10 explains the input voltage ranges of V_{IN} and V_{AIN} and its dependency to the supply level of V_{DDP} . The input voltage must not exceed 4.3 V, and it must not be more than 1.0 V above V_{DDP} . For the range up to $V_{DDP} + 1.0$ V also see the definition of the overload conditions in [Section 3.1.3](#).

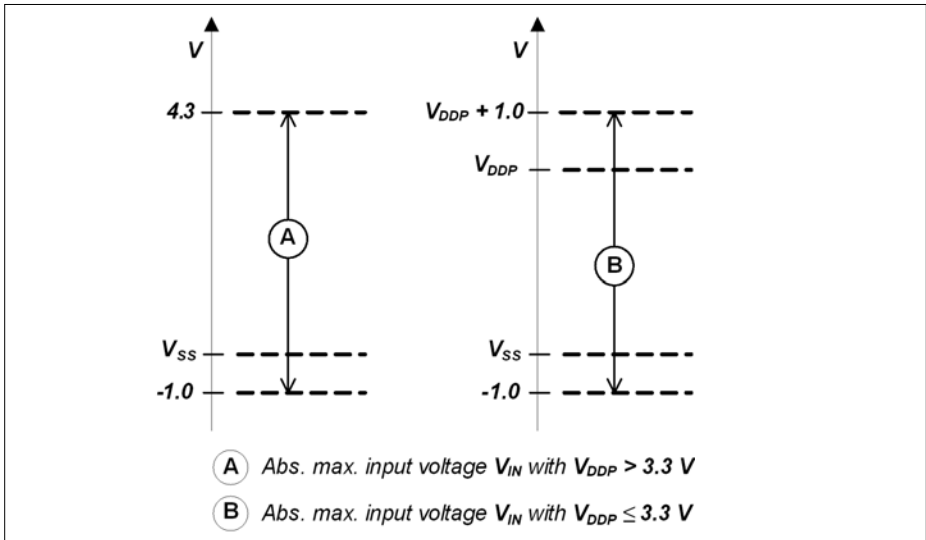


Figure 10 Absolute Maximum Input Voltage Ranges

3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 13 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **“Operating Conditions”** are met for
 - pad supply levels (V_{DDP} or V_{DDA})
 - temperature

If a pin current is outside of the **“Operating Conditions”** but within the overload conditions, then the parameters of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

Table 13 **Overload Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|-----------|----|--------|------|------|------|--|
| | | | Min. | Typ. | Max. | | |
| Input current on any port pin during overload condition | I_{OV} | SR | -5 | – | 5 | mA | |
| Absolute sum of all input circuit currents for one port group during overload condition ¹⁾ | I_{OVG} | SR | – | – | 20 | mA | $\Sigma I_{OVx} $, for all $I_{OVx} < 0$ mA |
| | | | – | – | 20 | mA | $\Sigma I_{OVx} $, for all $I_{OVx} > 0$ mA |
| Absolute sum of all input circuit currents during overload condition | I_{OVS} | SR | – | – | 80 | mA | ΣI_{OVG} |

1) The port groups are defined in [Table 16](#).

Figure 11 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

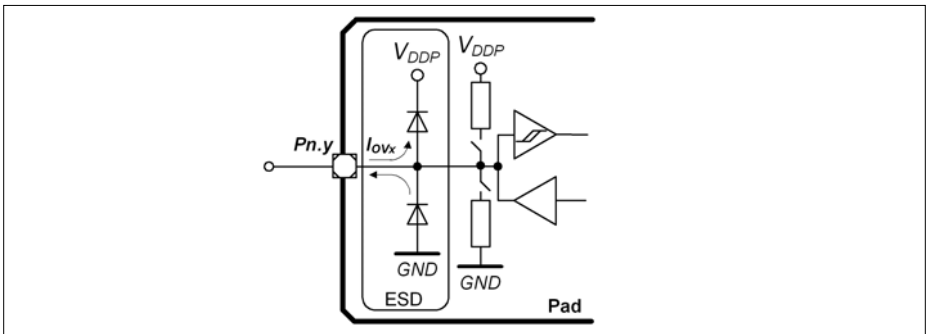


Figure 11 **Input Overload Current via ESD structures**

[Table 14](#) and [Table 15](#) list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the “**Absolute Maximum Ratings**” must not be exceeded during overload.

Table 14 PN-Junction Characteristics for positive Overload

| Pad Type | $I_{OV} = 5 \text{ mA}, T_J = -40 \text{ }^\circ\text{C}$ | $I_{OV} = 5 \text{ mA}, T_J = 150 \text{ }^\circ\text{C}$ |
|-----------|---|---|
| A1 / A1+ | $V_{IN} = V_{DDP} + 1.0 \text{ V}$ | $V_{IN} = V_{DDP} + 0.75 \text{ V}$ |
| A2 | $V_{IN} = V_{DDP} + 0.7 \text{ V}$ | $V_{IN} = V_{DDP} + 0.6 \text{ V}$ |
| AN/DIG_IN | $V_{IN} = V_{DDP} + 1.0 \text{ V}$ | $V_{IN} = V_{DDP} + 0.75 \text{ V}$ |

Table 15 PN-Junction Characteristics for negative Overload

| Pad Type | $I_{OV} = 5 \text{ mA}, T_J = -40 \text{ }^\circ\text{C}$ | $I_{OV} = 5 \text{ mA}, T_J = 150 \text{ }^\circ\text{C}$ |
|-----------|---|---|
| A1 / A1+ | $V_{IN} = V_{SS} - 1.0 \text{ V}$ | $V_{IN} = V_{SS} - 0.75 \text{ V}$ |
| A2 | $V_{IN} = V_{SS} - 0.7 \text{ V}$ | $V_{IN} = V_{SS} - 0.6 \text{ V}$ |
| AN/DIG_IN | $V_{IN} = V_{DDP} - 1.0 \text{ V}$ | $V_{IN} = V_{DDP} - 0.75 \text{ V}$ |

Table 16 Port Groups for Overload and Short-Circuit Current Sum Parameters

| Group | Pins |
|-------|-------------------------------|
| 1 | P0.[15:0], P3.[15:0] |
| 2 | P14.[15:0], P15.[15:0] |
| 3 | P2.[15:0], P5.[11:0] |
| 4 | P1.[15:0], P4.[7:0], P6.[6:0] |

3.1.4 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and their basic characteristics.

Table 17 Pad Driver and Pad Classes Overview

| Class | Power Supply | Type | Sub-Class | Speed Grade | Load | Termination |
|-------|--------------|------------|----------------------------------|-------------|--------|--------------------------------|
| A | 3.3 V | LVTTTL I/O | A1 (e.g. GPIO) | 6 MHz | 100 pF | No |
| | | | A1+ (e.g. serial I/Os) | 25 MHz | 50 pF | Series termination recommended |
| | | | A2 (e.g. ext. Bus) | 80 MHz | 15 pF | Series termination recommended |

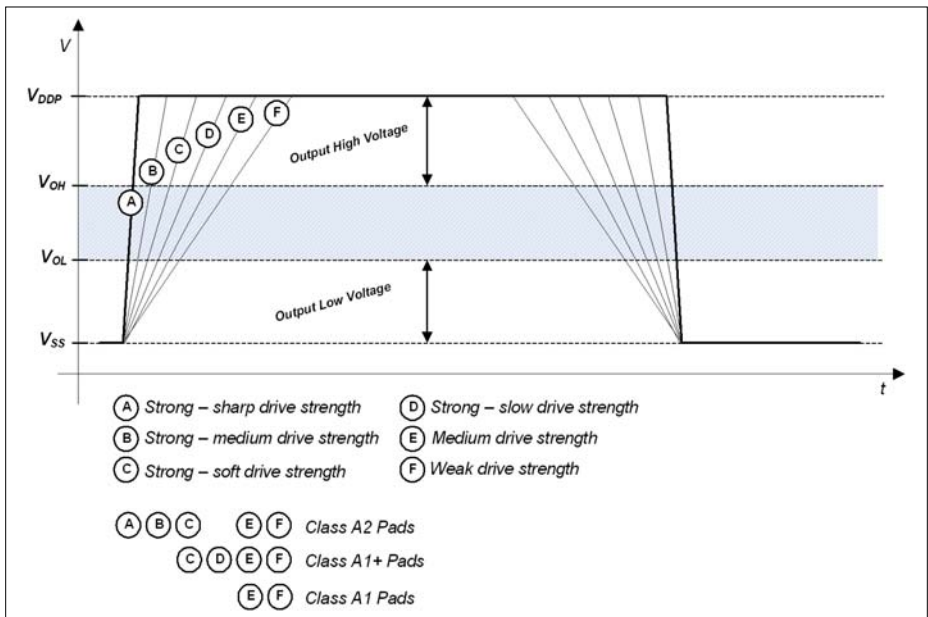


Figure 12 Output Slopes with different Pad Driver Modes

Figure 12 is a qualitative display of the resulting output slope performance with different output driver modes. The detailed input and output characteristics are listed in **Section 3.2.1**.

3.1.5 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC4500. All parameters specified in the following sections refer to these operating conditions, unless noted otherwise.

Table 18 Operating Conditions Parameters

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|------------------------|--------------------|------|--------------------|------|--|
| | | Min. | Typ. | Max. | | |
| Ambient Temperature | T_A SR | -40 | – | 85 | °C | Temp. Range F |
| | | -40 | – | 105 | °C | Temp. Range X |
| | | -40 | – | 125 | °C | Temp. Range K |
| Digital supply voltage | V_{DDP} SR | 3.13 ¹⁾ | 3.3 | 3.63 ²⁾ | V | |
| Core Supply Voltage | V_{DDC} CC | – ¹⁾ | 1.3 | – | V | Generated internally |
| Digital ground voltage | V_{SS} SR | 0 | – | – | V | |
| Analog supply voltage | V_{DDA} SR | 3.0 | 3.3 | 3.6 ²⁾ | V | |
| Analog ground voltage for V_{DDA} | V_{SSA} SR | -0.1 | 0 | 0.1 | V | |
| Battery Supply Voltage for Hibernate Domain | V_{BAT} SR | 1.95 ³⁾ | – | 3.63 | V | When V_{DDP} is supplied V_{BAT} has to be supplied as well. |
| System Frequency | f_{SYS} SR | – | – | 120 | MHz | |
| Short circuit current of digital outputs | I_{SC} SR | -5 | – | 5 | mA | |
| Absolute sum of short circuit currents per pin group ⁴⁾ | ΣI_{SC_PG} SR | – | – | 20 | mA | |
| Absolute sum of short circuit currents of the device | ΣI_{SC_D} SR | – | – | 100 | mA | |

1) See also the Supply Monitoring thresholds, [Section 3.3.2](#).

2) Voltage overshoot to 4.0 V is permissible at Power-Up and \overline{PORST} low, provided the pulse duration is less than 100 μ s and the cumulated sum of the pulses does not exceed 1 h over lifetime.

3) To start the hibernate domain it is required that $V_{BAT} \geq 2.1$ V, for a reliable start of the oscillation of RTC_XTAL in crystal mode it is required that $V_{BAT} \geq 3.0$ V.

4) The port groups are defined in [Table 16](#).

3.2 DC Parameters

3.2.1 Input/Output Pins

The digital input stage of the shared analog/digital input pins is identical to the input stage of the standard digital input/output pins.

The Pull-up on the $\overline{\text{PORST}}$ pin is identical to the Pull-up on the standard digital input/output pins.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 19 Standard Pad Parameters

| Parameter | Symbol | Values | | Unit | Note / Test Condition |
|--|----------------|----------------------|------|---------------|---|
| | | Min. | Max. | | |
| Pin capacitance (digital inputs/outputs) | C_{IO} CC | – | 10 | pF | |
| Pull-down current | $ I_{PDL} $ CC | 150 | – | μA | ¹⁾ $V_{IN} \geq 0.6 \times V_{DDP}$ |
| | | – | 10 | μA | ²⁾ $V_{IN} \leq 0.36 \times V_{DDP}$ |
| Pull-Up current | $ I_{PUH} $ CC | – | 10 | μA | ²⁾ $V_{IN} \geq 0.6 \times V_{DDP}$ |
| | | 100 | – | μA | ¹⁾ $V_{IN} \leq 0.36 \times V_{DDP}$ |
| Input Hysteresis for pads of all A classes ³⁾ | HYS_A CC | $0.1 \times V_{DDP}$ | – | V | |
| $\overline{\text{PORST}}$ spike filter always blocked pulse duration | t_{SF1} CC | – | 10 | ns | |
| $\overline{\text{PORST}}$ spike filter pass-through pulse duration | t_{SF2} CC | 100 | – | ns | |
| $\overline{\text{PORST}}$ pull-down current | $ I_{PPD} $ CC | 13 | – | mA | $V_{IN} = 1.0 \text{ V}$ |

1) Current required to override the pull device with the opposite logic level (“force current”).

With active pull device, at load currents between force and keep current the input state is undefined.

2) Load current at which the pull device still maintains the valid logic level (“keep current”).

With active pull device, at load currents between force and keep current the input state is undefined.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

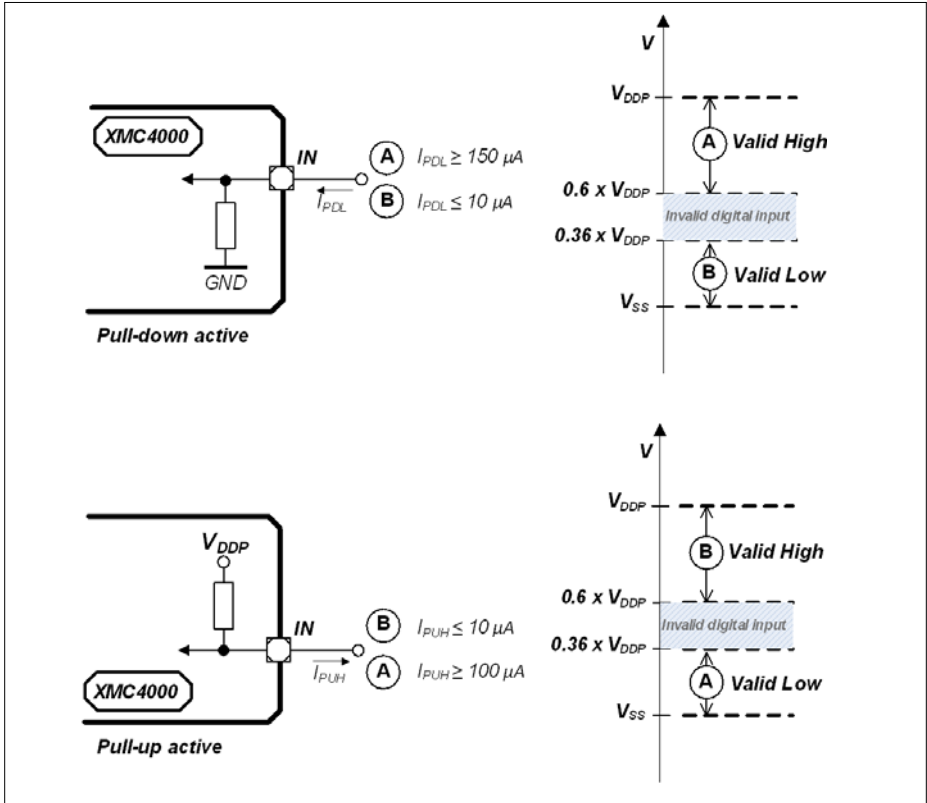


Figure 13 Pull Device Input Characteristics

Figure 13 visualizes the input characteristics with an active internal pull device:

- in the cases "A" the internal pull device is overridden by a strong external driver;
- in the cases "B" the internal pull device defines the input logical state against a weak external load.

Electrical Parameters
Table 20 Standard Pads Class_A1

| Parameter | Symbol | Values | | Unit | Note / Test Condition |
|---|---------------|----------------------|-----------------------|------|--|
| | | Min. | Max. | | |
| Input leakage current | I_{OZA1} CC | -500 | 500 | nA | $0\text{ V} \leq V_{IN} \leq V_{DDP}$ |
| Input high voltage | V_{IHA1} SR | $0.6 \times V_{DDP}$ | $V_{DDP} + 0.3$ | V | max. 3.6 V |
| Input low voltage | V_{ILA1} SR | -0.3 | $0.36 \times V_{DDP}$ | V | |
| Output high voltage, POD ¹⁾ = weak | V_{OHA1} CC | $V_{DDP} - 0.4$ | – | V | $I_{OH} \geq -400\ \mu\text{A}$ |
| | | 2.4 | – | V | $I_{OH} \geq -500\ \mu\text{A}$ |
| Output high voltage, POD ¹⁾ = medium | | $V_{DDP} - 0.4$ | – | V | $I_{OH} \geq -1.4\ \text{mA}$ |
| | | 2.4 | – | V | $I_{OH} \geq -2\ \text{mA}$ |
| Output low voltage | V_{OLA1} CC | – | 0.4 | V | $I_{OL} \leq 500\ \mu\text{A}$; POD ¹⁾ = weak |
| | | – | 0.4 | V | $I_{OL} \leq 2\ \text{mA}$; POD ¹⁾ = medium |
| Fall time | t_{FA1} CC | – | 150 | ns | $C_L = 20\ \text{pF}$; POD ¹⁾ = weak |
| | | – | 50 | ns | $C_L = 50\ \text{pF}$; POD ¹⁾ = medium |
| Rise time | t_{RA1} CC | – | 150 | ns | $C_L = 20\ \text{pF}$; POD ¹⁾ = weak |
| | | – | 50 | ns | $C_L = 50\ \text{pF}$; POD ¹⁾ = medium |

1) POD = Pin Out Driver

Table 21 Standard Pads Class_A1+

| Parameter | Symbol | Values | | Unit | Note / Test Condition |
|-----------------------|----------------|----------------------|-----------------------|---------------|---------------------------------------|
| | | Min. | Max. | | |
| Input leakage current | I_{OZA1+} CC | -1 | 1 | μA | $0\text{ V} \leq V_{IN} \leq V_{DDP}$ |
| Input high voltage | V_{IHA1+} SR | $0.6 \times V_{DDP}$ | $V_{DDP} + 0.3$ | V | max. 3.6 V |
| Input low voltage | V_{ILA1+} SR | -0.3 | $0.36 \times V_{DDP}$ | V | |

Electrical Parameters
Table 21 Standard Pads Class_A1+

| Parameter | Symbol | Values | | Unit | Note / Test Condition | |
|---|--------------------------|--------------------------|------|------|--|---|
| | | Min. | Max. | | | |
| Output high voltage, POD ¹⁾ = weak | V _{OHA1+} CC | V _{DDP} - 0.4 | – | V | I _{OH} ≥ -400 μA | |
| | | 2.4 | – | V | I _{OH} ≥ -500 μA | |
| Output high voltage, POD ¹⁾ = medium | | V _{DDP} - 0.4 | – | V | I _{OH} ≥ -1.4 mA | |
| | | 2.4 | – | V | I _{OH} ≥ -2 mA | |
| Output high voltage, POD ¹⁾ = strong | | V _{DDP} - 0.4 | – | V | I _{OH} ≥ -1.4 mA | |
| | | 2.4 | – | V | I _{OH} ≥ -2 mA | |
| Output low voltage | | V _{OLA1+} CC | – | 0.4 | V | I _{OL} ≤ 500 μA; POD ¹⁾ = weak |
| | | | – | 0.4 | V | I _{OL} ≤ 2 mA; POD ¹⁾ = medium |
| | – | | 0.4 | V | I _{OL} ≤ 2 mA; POD ¹⁾ = strong | |
| Fall time | t _{FA1+} CC | – | 150 | ns | C _L = 20 pF; POD ¹⁾ = weak | |
| | | – | 50 | ns | C _L = 50 pF; POD ¹⁾ = medium | |
| | | – | 28 | ns | C _L = 50 pF; POD ¹⁾ = strong; edge = slow | |
| | | – | 16 | ns | C _L = 50 pF; POD ¹⁾ = strong; edge = soft; | |
| Rise time | t _{RA1+} CC | – | 150 | ns | C _L = 20 pF; POD ¹⁾ = weak | |
| | | – | 50 | ns | C _L = 50 pF; POD ¹⁾ = medium | |
| | | – | 28 | ns | C _L = 50 pF; POD ¹⁾ = strong; edge = slow | |
| | | – | 16 | ns | C _L = 50 pF; POD ¹⁾ = strong; edge = soft | |

1) POD = Pin Out Driver

Table 22 Standard Pads Class_A2

| Parameter | Symbol | Values | | Unit | Note / Test Condition |
|--------------------------------------|------------------|----------------------|-----------------------|---------------|--|
| | | Min. | Max. | | |
| Input Leakage current | I_{OZA2} CC | -6 | 6 | μA | $0\text{ V} \leq V_{IN} < 0.5 \cdot V_{DDP} - 1\text{ V};$ $0.5 \cdot V_{DDP} + 1\text{ V} < V_{IN} \leq V_{DDP}$ |
| | | -3 | 3 | μA | $0.5 \cdot V_{DDP} - 1\text{ V} < V_{IN} < 0.5 \cdot V_{DDP} + 1\text{ V}$ |
| Input high voltage | V_{IHA2} SR | $0.6 \times V_{DDP}$ | $V_{DDP} + 0.3$ | V | max. 3.6 V |
| Input low voltage | V_{ILA2} SR | -0.3 | $0.36 \times V_{DDP}$ | V | |
| Output high voltage, POD = weak | V_{OHA2} CC | $V_{DDP} - 0.4$ | – | V | $I_{OH} \geq -400\ \mu\text{A}$ |
| | | 2.4 | – | V | $I_{OH} \geq -500\ \mu\text{A}$ |
| Output high voltage, POD = medium | | $V_{DDP} - 0.4$ | – | V | $I_{OH} \geq -1.4\ \text{mA}$ |
| | | 2.4 | – | V | $I_{OH} \geq -2\ \text{mA}$ |
| Output high voltage, POD = strong | | $V_{DDP} - 0.4$ | – | V | $I_{OH} \geq -1.4\ \text{mA}$ |
| | | 2.4 | – | V | $I_{OH} \geq -2\ \text{mA}$ |
| Output low voltage, POD = weak | V_{OLA2} CC | – | 0.4 | V | $I_{OL} \leq 500\ \mu\text{A}$ |
| Output low voltage, POD = medium | | – | 0.4 | V | $I_{OL} \leq 2\ \text{mA}$ |
| Output low voltage, POD = strong | | – | 0.4 | V | $I_{OL} \leq 2\ \text{mA}$ |

Electrical Parameters

Table 22 Standard Pads Class_A2

| Parameter | Symbol | Values | | Unit | Note / Test Condition |
|-----------|--------------|--------|------|------|--|
| | | Min. | Max. | | |
| Fall time | t_{FA2} CC | – | 150 | ns | $C_L = 20$ pF; POD = weak |
| | | – | 50 | ns | $C_L = 50$ pF; POD = medium |
| | | – | 3.7 | ns | $C_L = 50$ pF; POD = strong; edge = sharp |
| | | – | 7 | ns | $C_L = 50$ pF; POD = strong; edge = medium |
| | | – | 16 | ns | $C_L = 50$ pF; POD = strong; edge = soft |
| Rise time | t_{RA2} CC | – | 150 | ns | $C_L = 20$ pF; POD = weak |
| | | – | 50 | ns | $C_L = 50$ pF; POD = medium |
| | | – | 3.7 | ns | $C_L = 50$ pF; POD = strong; edge = sharp |
| | | – | 7.0 | ns | $C_L = 50$ pF; POD = strong; edge = medium |
| | | – | 16 | ns | $C_L = 50$ pF; POD = strong; edge = soft |

3.2.2 Analog to Digital Converters (VADC)

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 23 VADC Parameters (Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-----------------------------|------------------|------|-----------------------|---------|---|
| | | Min. | Typ. | Max. | | |
| Analog reference voltage ⁵⁾ | V_{AREF} SR | $V_{AGND} + 1$ | – | $V_{DDA} + 0.05^{1)}$ | V | |
| Analog reference ground ⁵⁾ | V_{AGND} SR | $V_{SSM} - 0.05$ | – | $V_{AREF} - 1$ | V | |
| Analog reference voltage range ²⁾⁵⁾ | $V_{AREF} - V_{AGND}$ SR | 1 | – | $V_{DDA} + 0.1$ | V | |
| Analog input voltage | V_{AIN} SR | V_{AGND} | – | V_{DDA} | V | |
| Input leakage at analog inputs ³⁾ | I_{OZ1} CC | -100 | – | 200 | nA | $0.03 \times V_{DDA} < V_{AIN} < 0.97 \times V_{DDA}$ |
| | | -500 | – | 100 | nA | $0 V \leq V_{AIN} \leq 0.03 \times V_{DDA}$ |
| | | -100 | – | 500 | nA | $0.97 \times V_{DDA} \leq V_{AIN} \leq V_{DDA}$ |
| Input leakage current at VAREF | I_{OZ2} CC | -1 | – | 1 | μA | $0 V \leq V_{AREF} \leq V_{DDA}$ |
| Input leakage current at VAGND | I_{OZ3} CC | -1 | – | 1 | μA | $0 V \leq V_{AGND} \leq V_{DDA}$ |
| Internal ADC clock | f_{ADCI} CC | 2 | – | 30 | MHz | $V_{DDA} = 3.3 V$ |
| Switched capacitance at the analog voltage inputs ⁴⁾ | C_{AINSW} CC | – | 7 | 20 | pF | |
| Total capacitance of an analog input | C_{AINTOT} CC | – | 25 | 30 | pF | |
| Switched capacitance at the positive reference voltage input ⁵⁾⁶⁾ | C_{AREFSW} CC | – | 15 | 30 | pF | |
| Total capacitance of the voltage reference inputs ⁵⁾ | $C_{AREFTOT}$ CC | – | 20 | 40 | pF | |

Electrical Parameters
Table 23 VADC Parameters (Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|------------------|--------|------|---------------------|------|--|
| | | Min. | Typ. | Max. | | |
| Total Unadjusted Error | TUE_{CC} | -4 | – | 4 | LSB | 12-bit resolution; $V_{DDA} = 3.3\text{ V}$; $V_{AREF} = V_{DDA}$ ⁷⁾ |
| Differential Non-Linearity Error ⁸⁾ | $EA_{DNL_{CC}}$ | -3 | – | 3 | LSB | |
| Gain Error ⁸⁾ | $EA_{GAIN_{CC}}$ | -4 | – | 4 | LSB | |
| Integral Non-Linearity ⁸⁾ | $EA_{INL_{CC}}$ | -3 | – | 3 | LSB | |
| Offset Error ⁸⁾ | $EA_{OFF_{CC}}$ | -4 | – | 4 | LSB | |
| RMS Noise ⁹⁾ | $EN_{RMS_{CC}}$ | – | 1 | 2 ¹⁰⁾¹¹⁾ | LSB | |
| Worst case ADC V_{DDA} power supply current per active converter | $I_{DDAA_{CC}}$ | – | 1.5 | 2 | mA | during conversion $V_{DDP} = 3.6\text{ V}$, $T_J = 150\text{ °C}$ |
| Charge consumption on V_{AREF} per conversion ⁵⁾ | $Q_{CONV_{CC}}$ | – | 30 | – | pC | $0\text{ V} \leq V_{AREF} \leq V_{DDA}$ ¹²⁾ |
| ON resistance of the analog input path | $R_{AIN_{CC}}$ | – | 700 | 1 700 | Ohm | |
| ON resistance for the ADC test (pull down for AIN7) | $R_{AIN7T_{CC}}$ | 180 | 550 | 900 | Ohm | |
| Resistance of the reference voltage input path | $R_{AREF_{CC}}$ | – | 700 | 1 700 | Ohm | |

- 1) A running conversion may become imprecise in case the normal conditions are violated (voltage overshoot).
- 2) If the analog reference voltage is below V_{DDA} , then the ADC converter errors increase. If the reference voltage is reduced by the factor k ($k < 1$), TUE, DNL, INL, Gain, and Offset errors increase also by the factor $1/k$.
- 3) The leakage current definition is a continuous function, as shown in figure ADCx Analog Inputs Leakage. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function (see [Figure 16](#)).
- 4) The sampling capacity of the conversion C-network is pre-charged to $V_{AREF}/2$ before the sampling moment. Because of the parasitic elements, the voltage measured at AINx can deviate from $V_{AREF}/2$.
- 5) Applies to AINx, when used as alternate reference input.
- 6) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead, smaller capacitances are successively switched to the reference voltage.
- 7) For 10-bit conversions, the errors are reduced to 1/4; for 8-bit conversions, the errors are reduced to 1/16. Never less than ± 1 LSB.
- 8) The sum of DNL/INL/GAIN/OFF errors does not exceed the related total unadjusted error TUE.

Electrical Parameters

- 9) This parameter is valid for soldered devices and requires careful analog board design.
- 10) Resulting worst case combined error is arithmetic combination of TUE and EN_{RMS} .
- 11) Value is defined for one sigma Gauss distribution.
- 12) The resulting current for a conversion can be calculated with $I_{AREF} = Q_{CONV} / t_c$.
The fastest 12-bit post-calibrated conversion of $t_c = 550$ ns results in a typical average current of $I_{AREF} = 54.5 \mu A$.

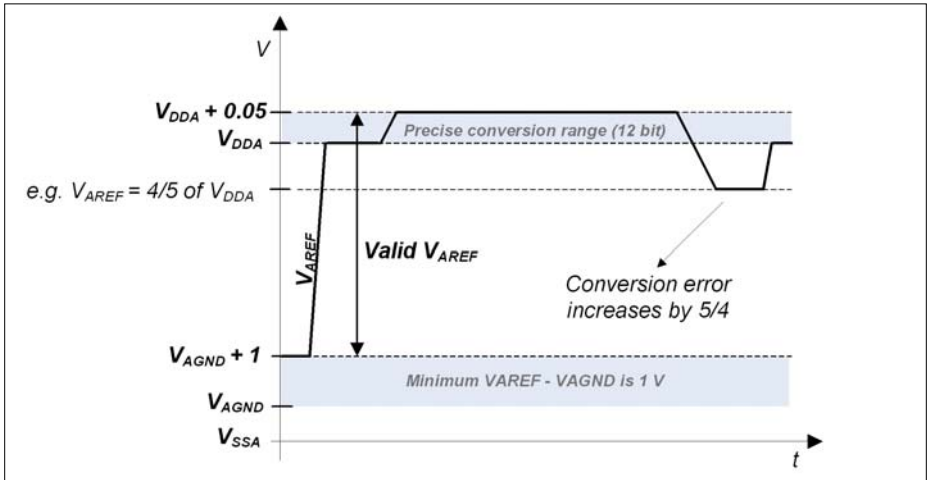


Figure 14 VADC Reference Voltage Range

The power-up calibration of the VADC requires a maximum number of $4 \cdot 352 \cdot f_{ADCI}$ cycles.

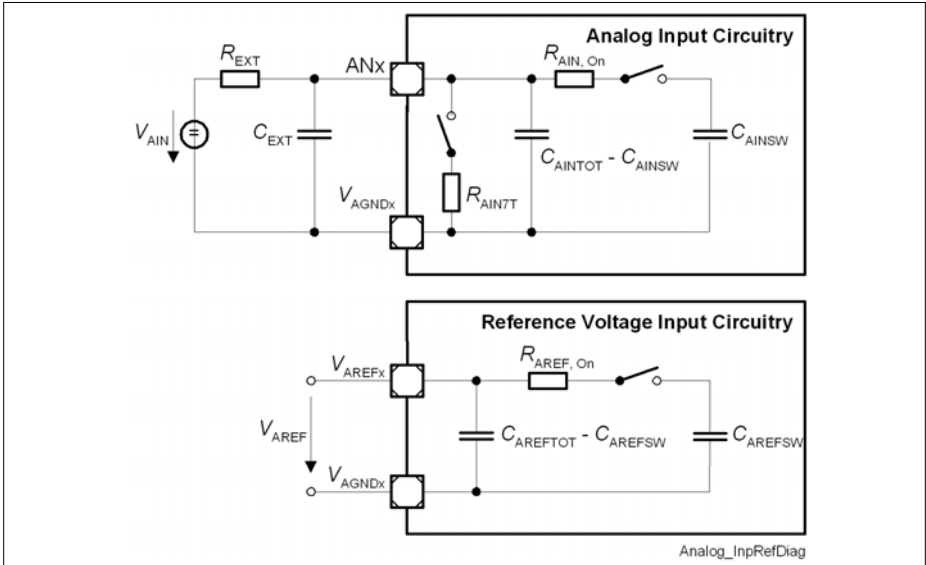


Figure 15 VADC Input Circuits

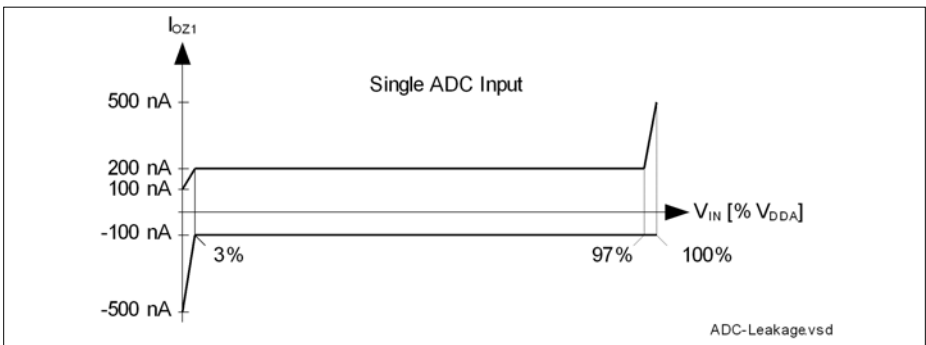


Figure 16 VADC Analog Input Leakage Current

Conversion Time

Table 24 Conversion Time (Operating Conditions apply)

| Parameter | Symbol | Values | Unit | Note |
|-----------------|----------|--|---------------|---|
| Conversion time | t_C CC | $2 \times T_{ADC} + (2 + N + STC + PC + DM) \times T_{ADCI}$ | μs | N = 8, 10, 12 for N-bit conversion $T_{ADC} = 1 / f_{PERIPH}$ $T_{ADCI} = 1 / f_{ADCI}$ |

- STC defines additional clock cycles to extend the sample time
- PC adds two cycles if post-calibration is enabled
- DM adds one cycle for an extended conversion time of the MSB

Conversion Time Examples

System assumptions:

$$f_{ADC} = 120 \text{ MHz i.e. } t_{ADC} = 8.33 \text{ ns, DIVA} = 3, f_{ADCI} = 30 \text{ MHz i.e. } t_{ADCI} = 33.3 \text{ ns}$$

According to the given formulas the following minimum conversion times can be achieved (STC = 0, DM = 0):

12-bit post-calibrated conversion (PC = 2):

$$t_{CN12C} = (2 + 12 + 2) \times t_{ADCI} + 2 \times t_{ADC} = 16 \times 33.3 \text{ ns} + 2 \times 8.33 \text{ ns} = 550 \text{ ns}$$

12-bit uncalibrated conversion:

$$t_{CN12} = (2 + 12) \times t_{ADCI} + 2 \times t_{ADC} = 14 \times 33.3 \text{ ns} + 2 \times 8.33 \text{ ns} = 483 \text{ ns}$$

10-bit uncalibrated conversion:

$$t_{CN10} = (2 + 10) \times t_{ADCI} + 2 \times t_{ADC} = 12 \times 33.3 \text{ ns} + 2 \times 8.33 \text{ ns} = 417 \text{ ns}$$

8-bit uncalibrated:

$$t_{CN8} = (2 + 8) \times t_{ADCI} + 2 \times t_{ADC} = 10 \times 33.3 \text{ ns} + 2 \times 8.33 \text{ ns} = 350 \text{ ns}$$

3.2.3 Digital to Analog Converters (DAC)

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Electrical Parameters
Table 25 DAC Parameters (Operating Conditions apply)

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|----------------------------|----------------|----|--------|-----------|------|------------|---|
| | | | Min. | Typ. | Max. | | |
| RMS supply current | I_{DD} | CC | – | 2.5 | 4 | mA | per active DAC channel, without load currents of DAC outputs |
| Resolution | RES | CC | – | 12 | – | Bit | |
| Update rate | f_{URATE_A} | CC | – | | 2 | Msample/s | data rate, where DAC can follow 64 LSB code jumps to ± 1 LSB accuracy |
| Update rate | f_{URATE_F} | CC | – | | 5 | Msample/s | data rate, where DAC can follow 64 LSB code jumps to ± 4 LSB accuracy |
| Settling time | t_{SETTLE} | CC | – | 1 | 2 | μ s | at full scale jump, output voltage reaches target value ± 20 LSB |
| Slew rate | SR | CC | 2 | 5 | – | V/ μ s | |
| Minimum output voltage | V_{OUT_MIN} | CC | – | 0.3 | – | V | code value unsigned: 000 _H ; signed: 800 _H |
| Maximum output voltage | V_{OUT_MAX} | CC | – | 2.5 | – | V | code value unsigned: FFF _H ; signed: 7FF _H |
| Integral non-linearity | INL | CC | -4 | ± 2.5 | 4 | LSB | $R_L \geq 5$ kOhm, $C_L \leq 50$ pF |
| Differential non-linearity | DNL | CC | -2 | ± 1 | 2 | LSB | $R_L \geq 5$ kOhm, $C_L \leq 50$ pF |
| Offset error | ED_{OFF} | CC | | ± 20 | | mV | |
| Gain error | ED_{G_IN} | CC | -6.5 | -1.5 | 3 | % | |
| Startup time | $t_{STARTUP}$ | CC | – | 15 | 30 | μ s | time from output enabling till code valid ± 16 LSB |

Electrical Parameters

Table 25 DAC Parameters (Operating Conditions apply) (cont'd)

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|--------------------------------|-------------------|----|--------|------|------|------|------------------------------------|
| | | | Min. | Typ. | Max. | | |
| 3dB Bandwidth of Output Buffer | f_{C1} | CC | 2.5 | 5 | – | MHz | verified by design |
| Output sourcing current | I_{OUT_SOURCE} | CC | – | -30 | – | mA | |
| Output sinking current | I_{OUT_SINK} | CC | – | 0.6 | – | mA | |
| Output resistance | R_{OUT} | CC | – | 50 | – | Ohm | |
| Load resistance | R_L | SR | 5 | – | – | kOhm | |
| Load capacitance | C_L | SR | – | – | 50 | pF | |
| Signal-to-Noise Ratio | SNR | CC | – | 70 | – | dB | examination bandwidth < 25 kHz |
| Total Harmonic Distortion | THD | CC | – | 70 | – | dB | examination bandwidth < 25 kHz |
| Power Supply Rejection Ratio | PSRR | CC | – | 56 | – | dB | to V_{DDA} verified by design |

Conversion Calculation

Unsigned:

$$DACxDATA = 4095 \times (V_{OUT} - V_{OUT_MIN}) / (V_{OUT_MAX} - V_{OUT_MIN})$$

Signed:

$$DACxDATA = 4095 \times (V_{OUT} - V_{OUT_MIN}) / (V_{OUT_MAX} - V_{OUT_MIN}) - 2048$$

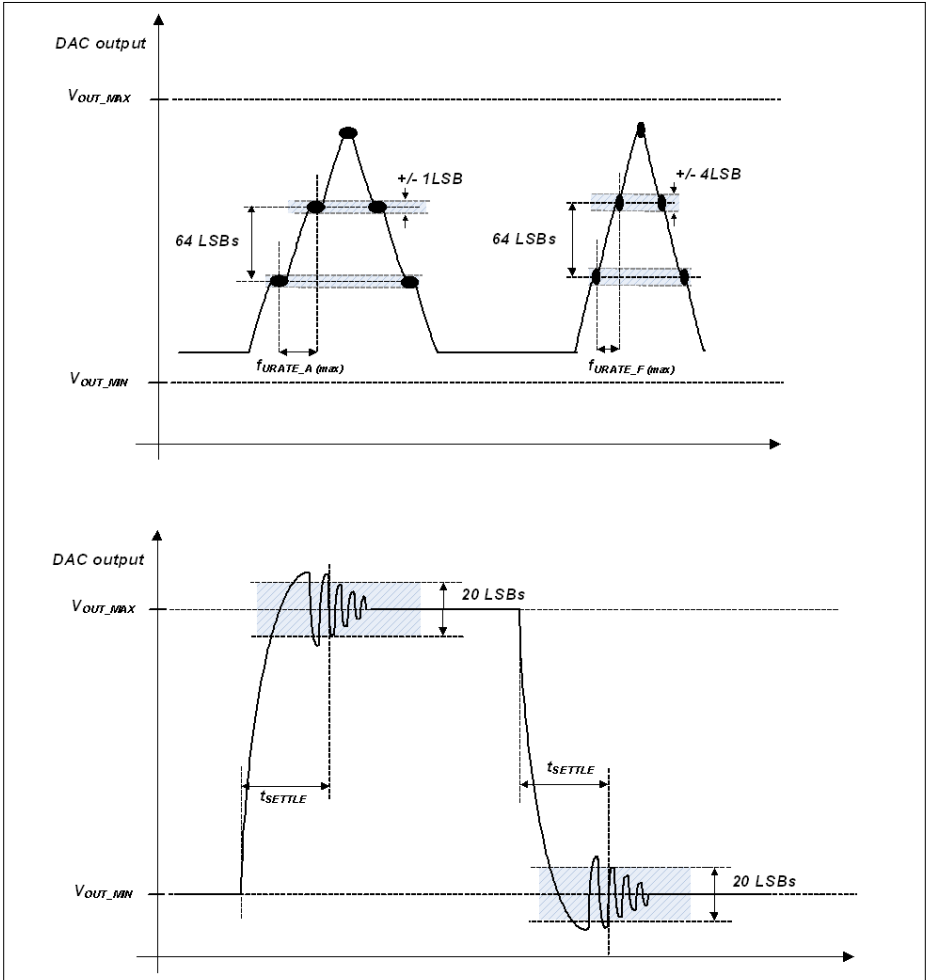


Figure 17 DAC Conversion Examples

3.2.4 Out-of-Range Comparator (ORC)

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above the analog reference¹⁾ (V_{AREF}) on selected input pins (GxORCy) and generates a service request trigger (GxORCOUTy).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The parameters in **Table 26** apply for the maximum reference voltage $V_{AREF} = V_{DDA} + 50 \text{ mV}$.

Table 26 ORC Parameters (Operating Conditions apply)

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|------------|----|--------|------|-----------|------|--|
| | | | Min. | Typ. | Max. | | |
| DC Switching Level | V_{ODC} | CC | 100 | 125 | 200 | mV | $V_{AIN} \geq V_{AREF} + V_{ODC}$ |
| Hysteresis | V_{OHYS} | CC | 50 | – | V_{ODC} | mV | |
| Detection Delay of a persistent Overvoltage | t_{ODD} | CC | 55 | – | 450 | ns | $V_{AIN} \geq V_{AREF} + 200 \text{ mV}$ |
| | | | 45 | – | 105 | ns | $V_{AIN} \geq V_{AREF} + 400 \text{ mV}$ |
| Always detected Overvoltage Pulse | t_{OPDD} | CC | 440 | – | – | ns | $V_{AIN} \geq V_{AREF} + 200 \text{ mV}$ |
| | | | 90 | – | – | ns | $V_{AIN} \geq V_{AREF} + 400 \text{ mV}$ |
| Never detected Overvoltage Pulse | t_{OPDN} | CC | – | – | 49 | ns | $V_{AIN} \geq V_{AREF} + 200 \text{ mV}$ |
| | | | – | – | 30 | ns | $V_{AIN} \geq V_{AREF} + 400 \text{ mV}$ |
| Release Delay | t_{ORD} | CC | 65 | – | 105 | ns | $V_{AIN} \leq V_{AREF}$ |
| Enable Delay | t_{OED} | CC | – | 100 | 200 | ns | |

1) Always the standard VADC reference, alternate references do not apply to the ORC.

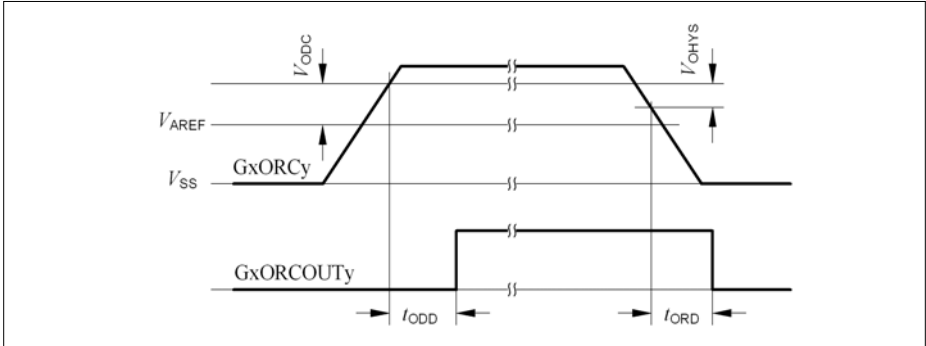


Figure 18 GxORCOUTy Trigger Generation

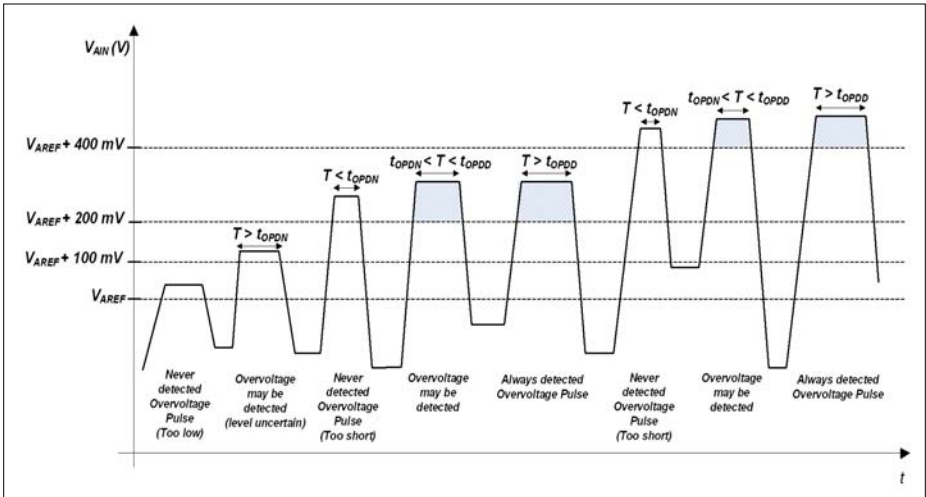


Figure 19 ORC Detection Ranges

3.2.5 Die Temperature Sensor

The Die Temperature Sensor (DTS) measures the junction temperature T_J .

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 27 Die Temperature Sensor Parameters

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|--------------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Temperature sensor range | T_{SR} SR | -40 | – | 150 | °C | |
| Linearity Error (to the below defined formula) | ΔT_{LE} CC | – | ±1 | – | °C | per $\Delta T_J \leq 30$ °C |
| Offset Error | ΔT_{OE} CC | – | ±6 | – | °C | $\Delta T_{OE} = T_J - T_{DTS}$ $V_{DDP} \leq 3.3$ V ¹⁾ |
| Measurement time | t_M CC | – | – | 100 | µs | |
| Start-up time after reset inactive | t_{TSST} SR | – | – | 10 | µs | |

1) At $V_{DDP_max} = 3.63$ V the typical offset error increases by an additional $\Delta T_{OE} = \pm 1$ °C.

The following formula calculates the temperature measured by the DTS in [°C] from the RESULT bit field of the DTSSTAT register.

$$\text{Temperature } T_{DTS} = (\text{RESULT} - 605) / 2.05 \text{ [°C]}$$

This formula and the values defined in **Table 27** apply with the following calibration values:

- DTSCON.BGTRIM = 8_H
- DTSCON.REFTRIM = 4_H

3.2.6 USB OTG Interface DC Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 28 USB OTG VBUS and ID Parameters (Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|----------------------------------|-------------------|--------|------|------|---------|--|
| | | Min. | Typ. | Max. | | |
| VBUS input voltage range | V_{IN} CC | 0.0 | – | 5.25 | V | |
| A-device VBUS valid threshold | V_{B1} CC | 4.4 | – | – | V | |
| A-device session valid threshold | V_{B2} CC | 0.8 | – | 2.0 | V | |
| B-device session valid threshold | V_{B3} CC | 0.8 | – | 4.0 | V | |
| B-device session end threshold | V_{B4} CC | 0.2 | – | 0.8 | V | |
| VBUS input resistance to ground | R_{VBUS_IN} CC | 40 | – | 100 | kOhm | |
| B-device VBUS pull-up resistor | R_{VBUS_PU} CC | 281 | – | – | Ohm | Pull-up voltage = 3.0 V |
| B-device VBUS pull-down resistor | R_{VBUS_PD} CC | 656 | – | – | Ohm | |
| USB.ID pull-up resistor | R_{UID_PU} CC | 14 | – | 25 | kOhm | |
| VBUS input current | I_{VBUS_IN} CC | – | – | 150 | μ A | $0\text{ V} \leq V_{IN} \leq 5.25\text{ V}$: $T_{AVG} = 1\text{ ms}$ |

Table 29 USB OTG Data Line (USB_DP, USB_DM) Parameters (Operating Conditions apply)

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|-----------|----|--------|------|-------|------|--------------------------------|
| | | | Min. | Typ. | Max. | | |
| Input low voltage | V_{IL} | SR | – | – | 0.8 | V | |
| Input high voltage (driven) | V_{IH} | SR | 2.0 | – | – | V | |
| Input high voltage (floating) ¹⁾ | V_{IHZ} | SR | 2.7 | – | 3.6 | V | |
| Differential input sensitivity | V_{DIS} | CC | 0.2 | – | – | V | |
| Differential common mode range | V_{CM} | CC | 0.8 | – | 2.5 | V | |
| Output low voltage | V_{OL} | CC | 0.0 | – | 0.3 | V | 1.5 kOhm pull-up to 3.6 V |
| Output high voltage | V_{OH} | CC | 2.8 | – | 3.6 | V | 15 kOhm pull-down to 0 V |
| DP pull-up resistor (idle bus) | R_{PUI} | CC | 900 | – | 1 575 | Ohm | |
| DP pull-up resistor (upstream port receiving) | R_{PUA} | CC | 1 425 | – | 3 090 | Ohm | |
| DP, DM pull-down resistor | R_{PD} | CC | 14.25 | – | 24.8 | kOhm | |
| Input impedance DP, DM | Z_{INP} | CC | 300 | – | – | kOhm | $0 V \leq V_{IN} \leq V_{DDP}$ |
| Driver output resistance DP, DM | Z_{DRV} | CC | 28 | – | 44 | Ohm | |

1) Measured at A-connector with 1.5 kOhm \pm 5% to 3.3 V \pm 0.3 V connected to USB_DP or USB_DM and at B-connector with 15 kOhm \pm 5% to ground connected to USB_DP and USB_DM.

3.2.7 Oscillator Pins

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The oscillator pins can be operated with an external crystal (see [Figure 20](#)) or in direct input mode (see [Figure 21](#)).

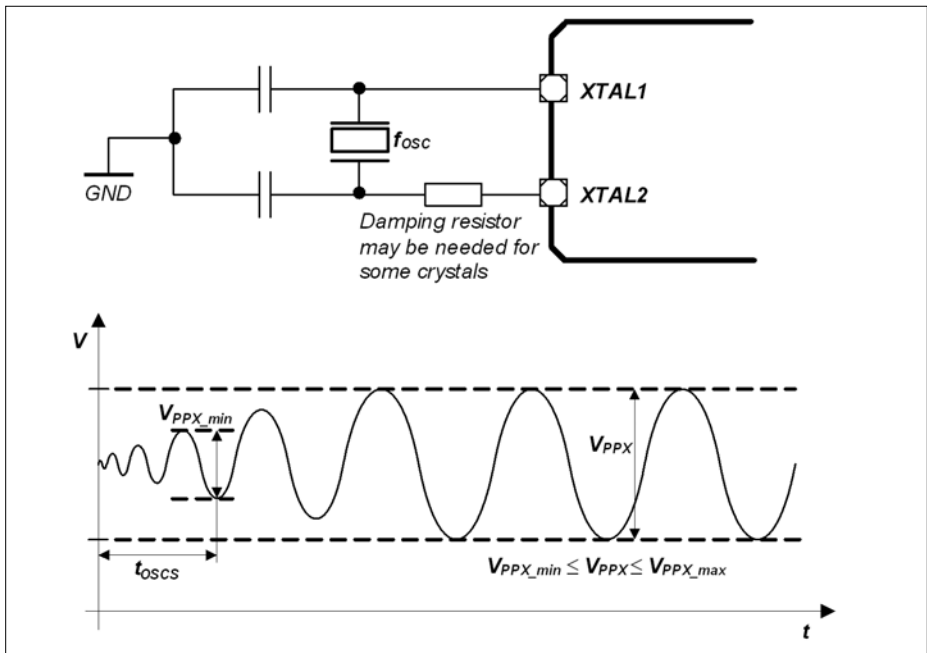


Figure 20 Oscillator in Crystal Mode

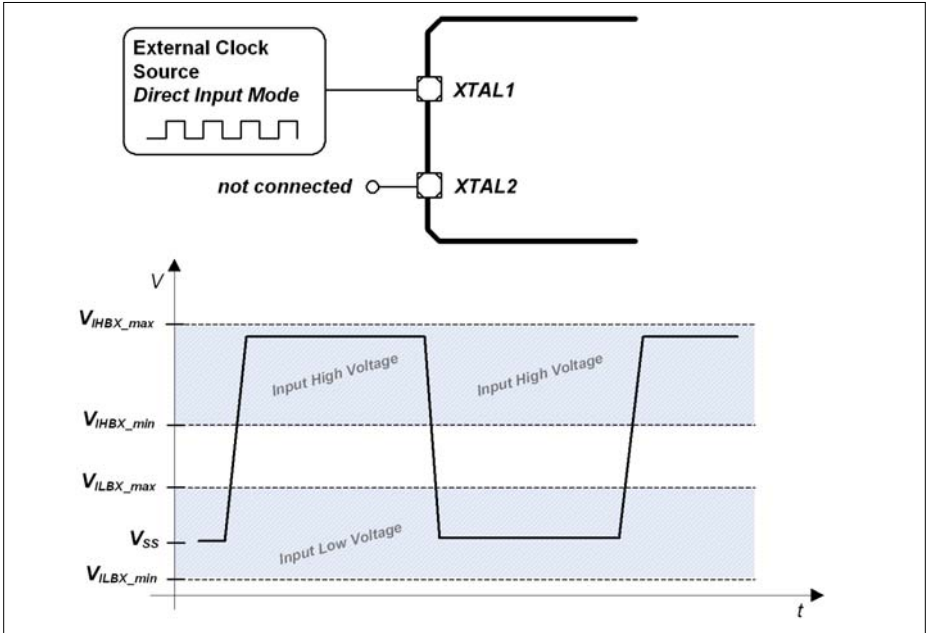


Figure 21 Oscillator in Direct Input Mode

Table 30 OSC_XTAL Parameters

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|----------------------|-----------------------------|------|------------------------|------|---|
| | | Min. | Typ. | Max. | | |
| Input frequency | f_{OSC} SR | 4 | – | 40 | MHz | Direct Input Mode selected |
| | | 4 | – | 25 | MHz | External Crystal Mode selected |
| Oscillator start-up time ¹⁾²⁾ | t_{OSCS} CC | – | – | 10 | ms | |
| Input voltage at XTAL1 | V_{IX} SR | -0.5 | – | $V_{\text{DDP}} + 0.5$ | V | |
| Input amplitude (peak-to-peak) at XTAL1 ²⁾³⁾ | V_{PPX} SR | $0.4 \times V_{\text{DDP}}$ | – | $V_{\text{DDP}} + 1.0$ | V | |
| Input high voltage at XTAL1 ⁴⁾ | V_{IHBX} SR | 1.0 | – | $V_{\text{DDP}} + 0.5$ | V | |
| Input low voltage at XTAL1 ⁴⁾ | V_{ILBX} SR | -0.5 | – | 0.4 | V | |
| Input leakage current at XTAL1 | I_{ILX1} CC | -100 | – | 100 | nA | Oscillator power down $0 \text{ V} \leq V_{\text{IX}} \leq V_{\text{DDP}}$ |

1) t_{OSCS} is defined from the moment the oscillator is enabled with SCU_OSCHPCTRL.MODE until the oscillations reach an amplitude at XTAL1 of $0.4 \times V_{\text{DDP}}$.

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

3) If the shaper unit is enabled and not bypassed.

4) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.

Table 31 RTC_XTAL Parameters

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---------------|-----------------------|--------|-----------------------|------|---|
| | | Min. | Typ. | Max. | | |
| Input frequency | f_{OSC} SR | – | 32.768 | – | kHz | |
| Oscillator start-up time ¹⁾²⁾³⁾ | t_{OSCS} CC | – | – | 5 | s | |
| Input voltage at RTC_XTAL1 | V_{IX} SR | -0.3 | – | $V_{BAT} + 0.3$ | V | |
| Input amplitude (peak-to-peak) at RTC_XTAL1 ²⁾⁴⁾ | V_{PPX} SR | 0.4 | – | – | V | |
| Input high voltage at RTC_XTAL1 ⁵⁾ | V_{IHBX} SR | $0.6 \times V_{BAT}$ | – | $V_{BAT} + 0.3$ | V | |
| Input low voltage at RTC_XTAL1 ⁵⁾ | V_{ILBX} SR | -0.3 | – | $0.36 \times V_{BAT}$ | V | |
| Input Hysteresis for RTC_XTAL1 ⁵⁾⁶⁾ | V_{HYSX} CC | $0.1 \times V_{BAT}$ | – | – | V | $3.0 \text{ V} \leq V_{BAT} < 3.6 \text{ V}$ |
| | | $0.03 \times V_{BAT}$ | – | – | V | $V_{BAT} < 3.0 \text{ V}$ |
| Input leakage current at RTC_XTAL1 | I_{ILX1} CC | -100 | – | 100 | nA | Oscillator power down $0 \text{ V} \leq V_{IX} \leq V_{BAT}$ |

- 1) t_{OSCS} is defined from the moment the oscillator is enabled by the user with SCU_OSCULCTRL.MODE until the oscillations reach an amplitude at RTC_XTAL1 of 400 mV.
- 2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.
- 3) For a reliable start of the oscillation in crystal mode it is required that $V_{BAT} \geq 3.0 \text{ V}$. A running oscillation is maintained across the full V_{BAT} voltage range.
- 4) If the shaper unit is enabled and not bypassed.
- 5) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.
- 6) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

3.2.8 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

If not stated otherwise, the operating conditions for the parameters in the following table are:

$$V_{DDP} = 3.3 \text{ V}, T_A = 25 \text{ }^\circ\text{C}$$

Table 32 Power Supply Parameters

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|---------------|---|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Active supply current ⁽¹⁾⁽¹⁰⁾ Peripherals enabled Frequency: $f_{CPU} / f_{PERIPH} / f_{CCU}$ in MHz | I_{DDPA} CC | – | 122 | – | mA | 120 / 120 / 120 |
| | | – | 110 | – | | 120 / 60 / 60 |
| | | – | 85 | – | | 60 / 60 / 120 |
| | | – | 65 | – | | 24 / 24 / 24 |
| | | – | 52 | – | | 1 / 1 / 1 |
| Active supply current Code execution from RAM Flash in Sleep mode | I_{DDPA} CC | – | 98 | – | mA | 120 / 120 / 120 |
| | | – | 80 | – | | 120 / 60 / 60 |
| Active supply current ⁽²⁾ Peripherals disabled Frequency: $f_{CPU} / f_{PERIPH} / f_{CCU}$ in MHz | I_{DDPA} CC | – | 115 | – | mA | 120 / 120 / 120 |
| | | – | 105 | – | | 120 / 60 / 60 |
| | | – | 80 | – | | 60 / 60 / 120 |
| | | – | 63 | – | | 24 / 24 / 24 |
| | | – | 50 | – | | 1 / 1 / 1 |
| Sleep supply current ⁽³⁾ Peripherals enabled Frequency: $f_{CPU} / f_{PERIPH} / f_{CCU}$ in MHz | I_{DDPS} CC | – | 115 | – | mA | 120 / 120 / 120 |
| | | – | 105 | – | | 120 / 60 / 60 |
| | | – | 83 | – | | 60 / 60 / 120 |
| | | – | 60 | – | | 24 / 24 / 24 |
| | | – | 48 | – | | 1 / 1 / 1 |
| | | $f_{CPU} / f_{PERIPH} / f_{CCU}$ in kHz | – | 46 | | – |

Electrical Parameters
Table 32 Power Supply Parameters

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---------------------|--------|------|--------------------|---------|--------------------------------------|
| | | Min. | Typ. | Max. | | |
| Sleep supply current ⁴⁾ Peripherals disabled Frequency: $f_{CPU} / f_{PERIPH} / f_{CCU}$ in MHz | I_{DDPS} CC | - | 110 | - | mA | 120 / 120 / 120 |
| | | - | 100 | - | | 120 / 60 / 60 |
| | | - | 77 | - | | 60 / 60 / 120 |
| | | - | 59 | - | | 24 / 24 / 24 |
| | | - | 48 | - | | 1 / 1 / 1 |
| | | - | 46 | - | | 100 / 100 / 100 |
| $f_{CPU} / f_{PERIPH} / f_{CCU}$ in kHz Deep Sleep supply current ⁵⁾ Flash in Sleep mode Frequency: $f_{CPU} / f_{PERIPH} / f_{CCU}$ in MHz $f_{CPU} / f_{PERIPH} / f_{CCU}$ in kHz | I_{DDPD} CC | - | 20 | - | mA | 24 / 24 / 24 |
| | | - | 12 | - | | 4 / 4 / 4 |
| | | - | 10 | - | | 1 / 1 / 1 |
| | | - | 6 | - | | 100 / 100 / 100 ⁶⁾ |
| Hibernate supply current RTC on ⁷⁾ | I_{DDPH} CC | - | 10 | - | μ A | $V_{BAT} = 3.3$ V |
| | | - | 7.5 | - | | $V_{BAT} = 2.4$ V |
| | | - | 6.2 | - | | $V_{BAT} = 2.0$ V |
| Hibernate supply current RTC off ⁸⁾ | I_{DDPH} CC | - | 9.2 | - | μ A | $V_{BAT} = 3.3$ V |
| | | - | 6.7 | - | | $V_{BAT} = 2.4$ V |
| | | - | 5.6 | - | | $V_{BAT} = 2.0$ V |
| Worst case active supply current ⁹⁾ | I_{DDPA} CC | - | - | 180 ¹⁰⁾ | mA | $V_{DDP} = 3.6$ V, $T_J = 150$ °C |
| V_{DDA} power supply current | I_{DDA} CC | - | - | - ¹¹⁾ | mA | |
| I_{DDP} current at \overline{PORST} Low | I_{DDP_PORST} CC | - | - | 16 | mA | $V_{DDP} = 3.6$ V, $T_J = 150$ °C |
| Power Dissipation | P_{DISS} CC | - | - | 1 | W | $V_{DDP} = 3.6$ V, $T_J = 150$ °C |
| Wake-up time from Sleep to Active mode | t_{SSA} CC | - | 6 | - | cycles | |

Table 32 Power Supply Parameters

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|--------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Wake-up time from Deep Sleep to Active mode | | – | – | – | ms | Defined by the wake-up of the Flash module, see Section 3.2.9 |
| Wake-up time from Hibernate mode | | – | – | – | ms | Wake-up via power-on reset event, see Section 3.3.2 |

- 1) CPU executing code from Flash, all peripherals idle.
- 2) CPU executing code from Flash.
- 3) CPU in sleep, all peripherals idle, Flash in Active mode.
- 4) CPU in sleep, Flash in Active mode.
- 5) CPU in sleep, peripherals disabled, after wake-up code execution from RAM.
- 6) To wake-up the Flash from its Sleep mode, $f_{CPU} \geq 1$ MHz is required.
- 7) OSC_ULP operating with external crystal on RTC_XTAL
- 8) OSC_ULP off, Hibernate domain operating with OSC_S1 clock
- 9) Test Power Loop: $f_{SYS} = 120$ MHz, CPU executing benchmark code from Flash, all CCUs in 100kHz timer mode, all ADC groups in continuous conversion mode, USICs as SPI in internal loop-back mode, CAN in 500kHz internal loop-back mode, interrupt triggered DMA block transfers to parity protected RAMs and FCE, DTS measurements and FPU calculations.
The power consumption of each customer application will most probably be lower than this value, but must be evaluated separately.
- 10) I_{DDP} decreases typically by approximately 6 mA when f_{SYS} decreases by 10 MHz, at constant T_J
- 11) Sum of currents of all active converters (ADC and DAC)

3.2.9 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 33 Flash Memory Parameters

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|------------------------|--------|------|------|-------|---|
| | | Min. | Typ. | Max. | | |
| Erase Time per 256 Kbyte Sector | t_{ERP} CC | – | 5 | 5.5 | s | |
| Erase Time per 64 Kbyte Sector | t_{ERP} CC | – | 1.2 | 1.4 | s | |
| Erase Time per 16 Kbyte Logical Sector | t_{ERP} CC | – | 0.3 | 0.4 | s | |
| Program time per page ¹⁾ | t_{PRP} CC | – | 5.5 | 11 | ms | |
| Erase suspend delay | t_{FL_ErSusp} CC | – | – | 15 | ms | |
| Wait time after margin change | $t_{FL_MarginDel}$ CC | 10 | – | – | μs | |
| Wake-up time | t_{WU} CC | – | – | 270 | μs | |
| Read access time | t_a CC | 22 | – | – | ns | For operation with $1/f_{CPU} < t_a$ wait states must be configured ²⁾ |
| Data Retention Time, Physical Sector ³⁾⁴⁾ | t_{RET} CC | 20 | – | – | years | Max. 1000 erase/program cycles |
| Data Retention Time, Logical Sector ³⁾⁴⁾ | t_{RETL} CC | 20 | – | – | years | Max. 100 erase/program cycles |
| Data Retention Time, User Configuration Block (UCB) ³⁾⁴⁾ | t_{RTU} CC | 20 | – | – | years | Max. 4 erase/program cycles per UCB |

1) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes an additional time of 5.5 ms.

2) The following formula applies to the wait state configuration: $FCON.WSPFLASH \times (1/f_{CPU}) \geq t_a$.

3) Storage and inactive time included.

4) Values given are valid for an average weighted junction temperature of $T_J = 110^\circ\text{C}$.

3.3 AC Parameters

3.3.1 Testing Waveforms

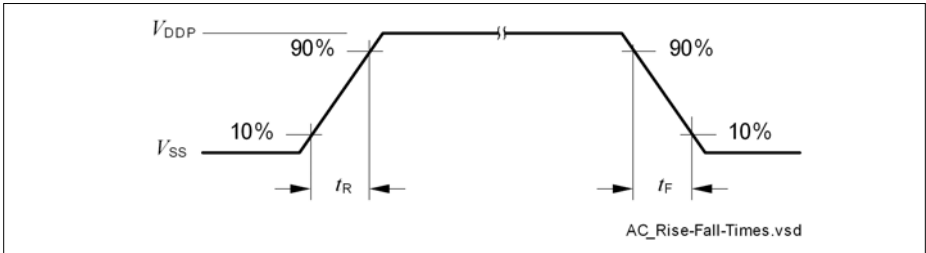


Figure 22 Rise/Fall Time Parameters

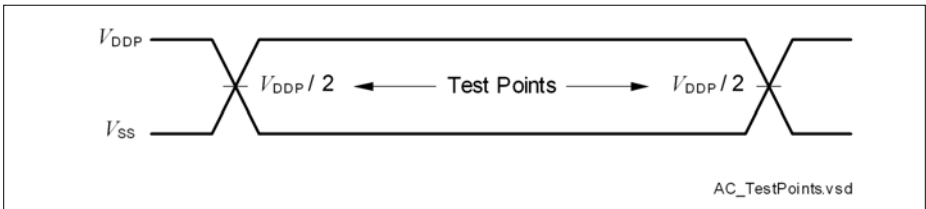


Figure 23 Testing Waveform, Output Delay

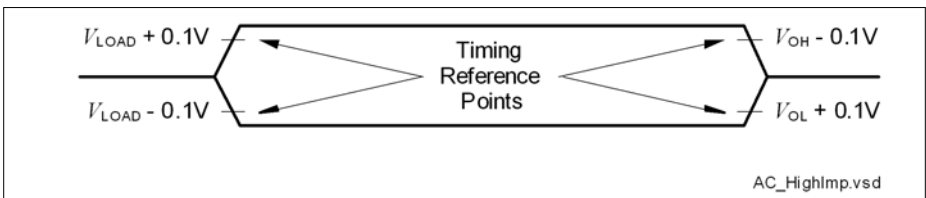


Figure 24 Testing Waveform, Output High Impedance

3.3.2 Power-Up and Supply Monitoring

$\overline{\text{PORST}}$ is always asserted when V_{DDP} and/or V_{DDC} violate the respective thresholds.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

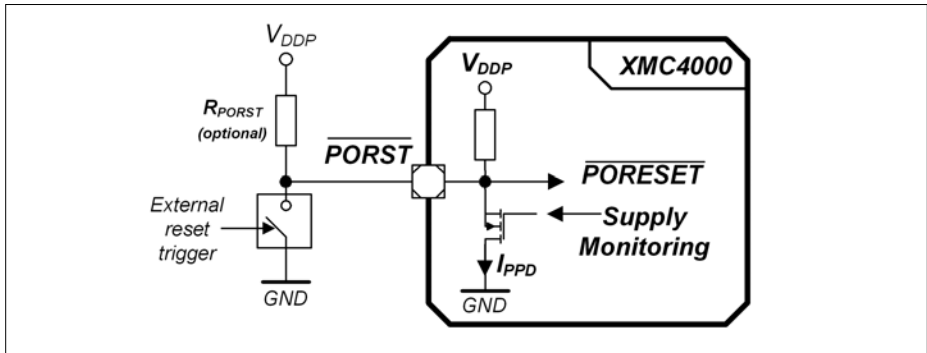


Figure 25 $\overline{\text{PORST}}$ Circuit

Table 34 Supply Monitoring Parameters

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|-----------------------|--------------------|------|--------------------|---------------|---|
| | | Min. | Typ. | Max. | | |
| Digital supply voltage reset threshold | V_{POR} CC | 2.79 ¹⁾ | – | 3.05 ²⁾ | V | 3) |
| Core supply voltage reset threshold | V_{PV} CC | – | – | 1.17 | V | |
| V_{DDP} voltage to ensure defined pad states | V_{DDPPA} CC | – | 1.0 | – | V | |
| $\overline{\text{PORST}}$ rise time | t_{PR} SR | – | – | 2 | μs | 4) |
| Startup time from power-on reset with code execution from Flash | t_{SSW} CC | – | 2.5 | 3.5 | ms | Time to the first user code instruction |
| V_{DDC} ramp up time | t_{VCR} CC | – | 550 | – | μs | Ramp up after power-on or after a reset triggered by a violation of V_{POR} or V_{PV} |

1) Minimum threshold for reset assertion.

- 2) Maximum threshold for reset deassertion.
- 3) The V_{DDP} monitoring has a typical hysteresis of $V_{PORHYS} = 180\text{ mV}$.
- 4) If t_{PR} is not met, low spikes on $\overline{\text{PORST}}$ may be seen during start up (e.g. reset pulses generated by the supply monitoring due to a slow ramping V_{DDP}).

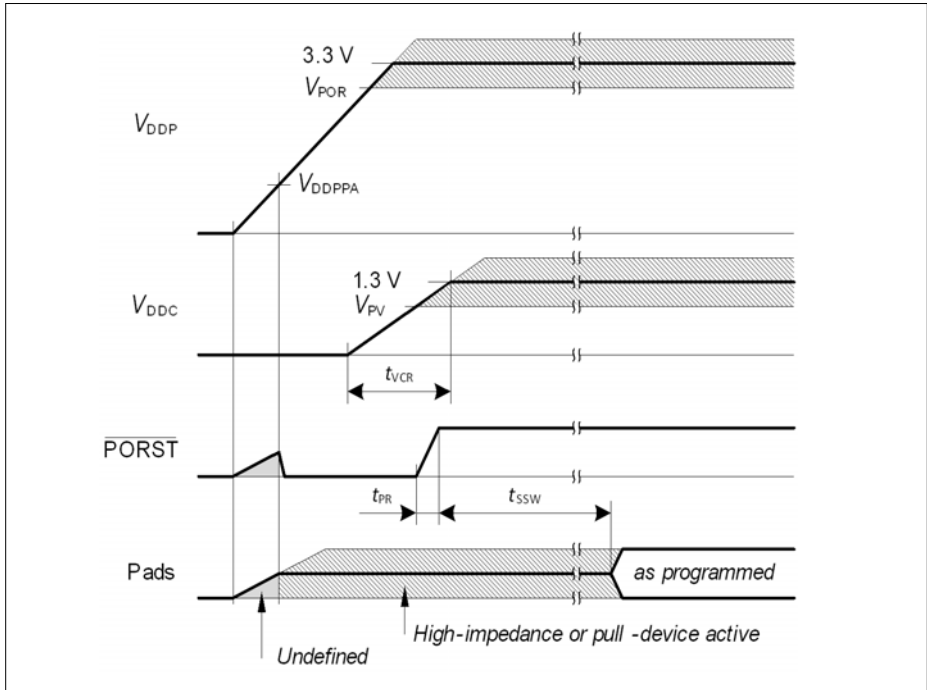


Figure 26 Power-Up Behavior

3.3.3 Power Sequencing

While starting up and shutting down as well as when switching power modes of the system it is important to limit the current load steps. A typical cause for such load steps is changing the CPU frequency f_{CPU} . Load steps exceeding the below defined values may cause a power on reset triggered by the supply monitor.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 35 Power Sequencing Parameters

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---------------------|--------|------|-----------|---------|--|
| | | Min. | Typ. | Max. | | |
| Positive Load Step Current | ΔI_{PLS} SR | - | - | 50 | mA | Load increase on V_{DDP} $\Delta t \leq 10$ ns |
| Negative Load Step Current | ΔI_{NLS} SR | - | - | 150 | mA | Load decrease on V_{DDP} $\Delta t \leq 10$ ns |
| V_{DDC} Voltage Over- / Undershoot from Load Step | ΔV_{LS} CC | - | - | ± 100 | mV | For maximum positive or negative load step |
| Positive Load Step Settling Time | t_{PLSS} SR | 50 | - | - | μ s | |
| Negative Load Step Settling Time | t_{NLSS} SR | 100 | - | - | μ s | |
| External Buffer Capacitor on V_{DDC} | C_{EXT} SR | - | 10 | - | μ F | In addition $C = 100$ nF capacitor on each V_{DDC} pin |

Positive Load Step Examples

System assumptions:

$f_{CPU} = f_{SYS}$, target frequency $f_{CPU} = 120$ MHz, main PLL $f_{VCO} = 480$ MHz, stepping done by K2 divider, t_{PLSS} between individual steps:

24 MHz - 48 MHz - 68 MHz - 96 MHz - 120 MHz (K2 steps 20 - 10 - 7 - 5 - 4)

24 MHz - 68 MHz - 96 MHz - 120 MHz (K2 steps 20 - 7 - 5 - 4)

24 MHz - 68 MHz - 120 MHz (K2 steps 20 - 7 - 4)

3.3.4 Phase Locked Loop (PLL) Characteristics

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Main and USB PLL

Table 36 PLL Parameters

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--------------------------|------------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Accumulated Jitter | D_p CC | – | – | ±5 | ns | accumulated over 300 cycles $f_{SYS} = 120$ MHz |
| Duty Cycle ¹⁾ | D_{DC} CC | 46 | 50 | 54 | % | Low pulse to total period, assuming an ideal input clock source |
| PLL base frequency | $f_{PLLBASE}$ CC | 30 | – | 140 | MHz | |
| VCO input frequency | f_{REF} CC | 4 | – | 16 | MHz | |
| VCO frequency range | f_{VCO} CC | 260 | – | 520 | MHz | |
| PLL lock-in time | t_L CC | – | – | 400 | μs | |

1) 50% for even K2 divider values, $50 \pm (10/K2)$ for odd K2 divider values.

3.3.5 Internal Clock Source Characteristics

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Fast Internal Clock Source

Table 37 Fast Internal Clock Parameters

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-------------------|-------------------------------|--------|------|------|---------------|--|
| | | Min. | Typ. | Max. | | |
| Nominal frequency | f_{OFINC} CC | – | 36.5 | – | MHz | not calibrated |
| | | – | 24 | – | MHz | calibrated |
| Accuracy | Δf_{OFI} CC | -0.5 | – | 0.5 | % | automatic calibration ¹⁾²⁾ |
| | | -15 | – | 15 | % | factory calibration, $V_{\text{DDP}} = 3.3 \text{ V}$ |
| | | -25 | – | 25 | % | no calibration, $V_{\text{DDP}} = 3.3 \text{ V}$ |
| | | -7 | – | 7 | % | Variation over voltage range ³⁾ $3.13 \text{ V} \leq V_{\text{DDP}} \leq 3.63 \text{ V}$ |
| Start-up time | t_{OFIS} CC | – | 50 | – | μs | |

1) Error in addition to the accuracy of the reference clock.

2) Automatic calibration compensates variations of the temperature and in the V_{DDP} supply voltage.

3) Deviations from the nominal V_{DDP} voltage induce an additional error to the uncalibrated and/or factory calibrated oscillator frequency.

Slow Internal Clock Source

Table 38 Slow Internal Clock Parameters

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-------------------|---------------------|--------|--------|------|---------------|---|
| | | Min. | Typ. | Max. | | |
| Nominal frequency | f_{OSI} CC | – | 32.768 | – | kHz | |
| Accuracy | Δf_{OSI} CC | -4 | – | 4 | % | $V_{BAT} = \text{const.}$ $0\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ |
| | | -5 | – | 5 | % | $V_{BAT} = \text{const.}$ $T_A < 0\text{ }^{\circ}\text{C}$ or $T_A > 85\text{ }^{\circ}\text{C}$ |
| | | -5 | – | 5 | % | $2.4\text{ V} \leq V_{BAT}$, $T_A = 25\text{ }^{\circ}\text{C}$ |
| | | -10 | – | 10 | % | $1.95\text{ V} \leq V_{BAT} < 2.4\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$ |
| Start-up time | t_{OSIS} CC | – | 50 | – | μs | |

3.3.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

Table 39 JTAG Interface Timing Parameters

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| TCK clock period | t_1 SR | 25 | – | – | ns | |
| TCK high time | t_2 SR | 10 | – | – | ns | |
| TCK low time | t_3 SR | 10 | – | – | ns | |
| TCK clock rise time | t_4 SR | – | – | 4 | ns | |
| TCK clock fall time | t_5 SR | – | – | 4 | ns | |
| TDI/TMS setup to TCK rising edge | t_6 SR | 6 | – | – | ns | |
| TDI/TMS hold after TCK rising edge | t_7 SR | 6 | – | – | ns | |
| TDO valid after TCK falling edge ¹⁾ (propagation delay) | t_8 CC | – | – | 13 | ns | $C_L = 50$ pF |
| | | 3 | – | – | ns | $C_L = 20$ pF |
| TDO hold after TCK falling edge ¹⁾ | t_{18} CC | 2 | – | – | ns | |
| TDO high imped. to valid from TCK falling edge ¹⁾²⁾ | t_9 CC | – | – | 14 | ns | $C_L = 50$ pF |
| TDO valid to high imped. from TCK falling edge ¹⁾ | t_{10} CC | – | – | 13.5 | ns | $C_L = 50$ pF |

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

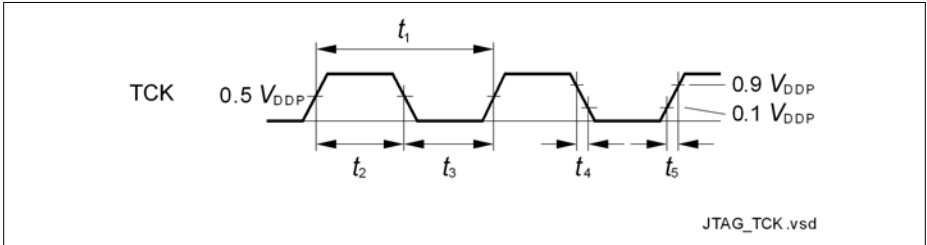


Figure 27 Test Clock Timing (TCK)

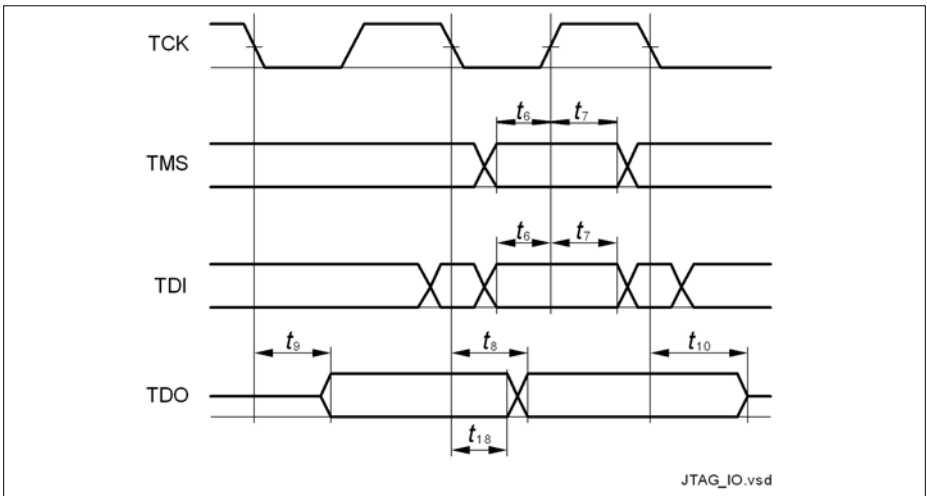


Figure 28 JTAG Timing

3.3.7 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

Table 40 SWD Interface Timing Parameters (Operating Conditions apply)

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|--|----------|----|--------|------|--------|------|-----------------------|
| | | | Min. | Typ. | Max. | | |
| SWDCLK clock period | t_{SC} | SR | 25 | – | – | ns | $C_L = 30$ pF |
| | | | 40 | – | – | ns | $C_L = 50$ pF |
| SWDCLK high time | t_1 | SR | 10 | – | 500000 | ns | |
| SWDCLK low time | t_2 | SR | 10 | – | 500000 | ns | |
| SWDIO input setup to SWDCLK rising edge | t_3 | SR | 6 | – | – | ns | |
| SWDIO input hold after SWDCLK rising edge | t_4 | SR | 6 | – | – | ns | |
| SWDIO output valid time after SWDCLK rising edge | t_5 | CC | – | – | 17 | ns | $C_L = 50$ pF |
| | | | – | – | 13 | ns | $C_L = 30$ pF |
| SWDIO output hold time from SWDCLK rising edge | t_6 | CC | 3 | – | – | ns | |

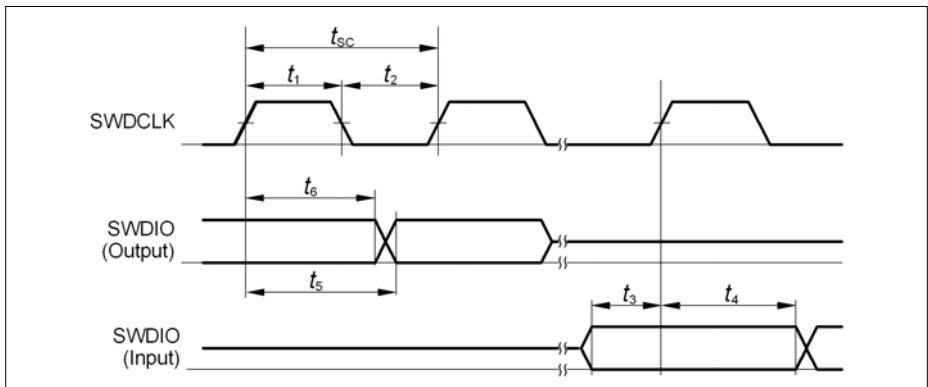


Figure 29 SWD Timing

3.3.8 Embedded Trace Macro Cell (ETM) Timing

The data timing refers to the active clock edge. The XMC4500 ETM uses the half-rate clocking mode. In this mode both, the rising and falling clock edges are active clock edges.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply, with $C_L \leq 15$ pF.

Table 41 ETM Interface Timing Parameters

| Parameter | Symbol | CC | Values | | | Unit | Note / Test Condition |
|----------------------------------|--------|----|--------|------|------|------|-----------------------|
| | | | Min. | Typ. | Max. | | |
| TRACECLK period | t_1 | CC | 16.7 | – | – | ns | – |
| TRACECLK high time | t_2 | CC | 2 | – | – | ns | – |
| TRACECLK low time | t_3 | CC | 2 | – | – | ns | – |
| TRACECLK and TRACEDATA rise time | t_4 | CC | – | – | 3 | ns | – |
| TRACECLK and TRACEDATA fall time | t_5 | CC | – | – | 3 | ns | – |
| TRACEDATA output valid time | t_6 | CC | -2 | – | 3 | ns | – |

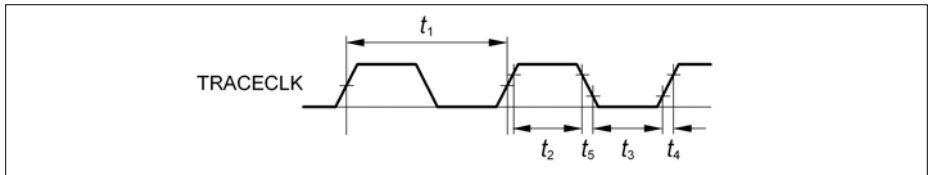


Figure 30 ETM Clock Timing

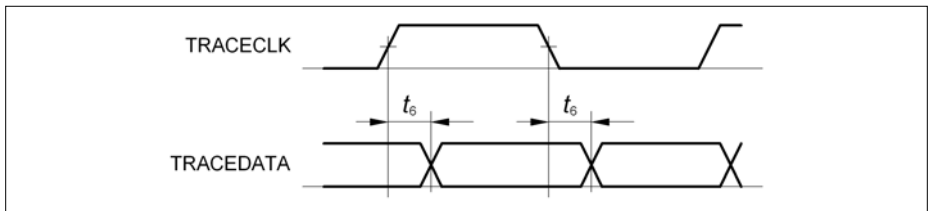


Figure 31 ETM Data Timing

3.3.9 Peripheral Timing

3.3.9.1 Delta-Sigma Demodulator Digital Interface Timing

The following parameters are applicable for the digital interface of the Delta-Sigma Demodulator (DSD).

The data timing is relative to the active clock edge. Depending on the operation mode of the connected modulator that can be the rising and falling clock edge.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 42 DSD Interface Timing Parameters

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|----------|-------------------------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| MCLK period in master mode | t_1 CC | 33.3 | – | – | ns | $t_1 \geq 4 \times t_{\text{PERIPH}}^{1)}$ |
| MCLK high time in master mode | t_2 CC | 9 | – | – | ns | $t_2 > t_{\text{PERIPH}}^{1)}$ |
| MCLK low time in master mode | t_3 CC | 9 | – | – | ns | $t_3 > t_{\text{PERIPH}}^{1)}$ |
| MCLK period in slave mode | t_1 SR | 33.3 | – | – | ns | $t_1 \geq 4 \times t_{\text{PERIPH}}^{1)}$ |
| MCLK high time in slave mode | t_2 SR | t_{PERIPH} | – | – | ns | ¹⁾ |
| MCLK low time in slave mode | t_3 SR | t_{PERIPH} | – | – | ns | ¹⁾ |
| DIN input setup time to the active clock edge | t_4 SR | $t_{\text{PERIPH}} + 4$ | – | – | ns | ¹⁾ |
| DIN input hold time from the active clock edge | t_5 SR | $t_{\text{PERIPH}} + 3$ | – | – | ns | ¹⁾ |

¹⁾ $t_{\text{PERIPH}} = 1 / f_{\text{PERIPH}}$

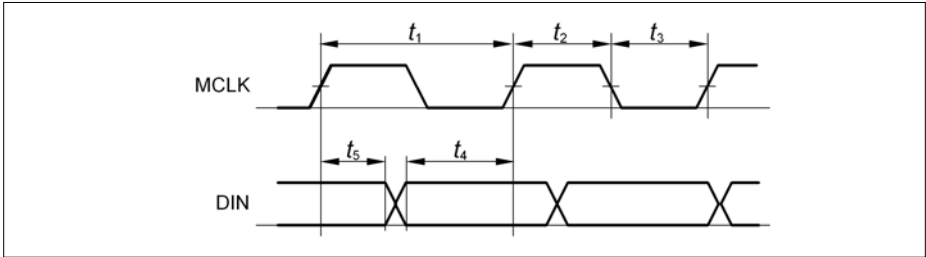


Figure 32 DSD Data Timing

3.3.9.2 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 43 USIC SSC Master Mode Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|--------------|---------------------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| SCLKOUT master clock period | t_{CLK} CC | 33.3 | – | – | ns | |
| Slave select output SELO active to first SCLKOUT transmit edge | t_1 CC | $t_{PB} - 6.5^{1)}$ | – | – | ns | |
| Slave select output SELO inactive after last SCLKOUT receive edge | t_2 CC | $t_{PB} - 8.5^{1)}$ | – | – | ns | |
| Data output DOUT[3:0] valid time | t_3 CC | -6 | – | 8 | ns | |
| Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge | t_4 SR | 23 | – | – | ns | |
| Data input DX0/DX[5:3] hold time from SCLKOUT receive edge | t_5 SR | 1 | – | – | ns | |

1) $t_{PB} = 1 / f_{PB}$

Table 44 USIC SSC Slave Mode Timing

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|-----------|----|--------|------|------|------|-----------------------|
| | | | Min. | Typ. | Max. | | |
| DX1 slave clock period | t_{CLK} | SR | 66.6 | – | – | ns | |
| Select input DX2 setup to first clock input DX1 transmit edge ¹⁾ | t_{10} | SR | 3 | – | – | ns | |
| Select input DX2 hold after last clock input DX1 receive edge ¹⁾ | t_{11} | SR | 4 | – | – | ns | |
| Receive data input DX0/DX[5:3] setup time to shift clock receive edge ¹⁾ | t_{12} | SR | 6 | – | – | ns | |
| Data input DX0/DX[5:3] hold time from clock input DX1 receive edge ¹⁾ | t_{13} | SR | 4 | – | – | ns | |
| Data output DOUT[3:0] valid time | t_{14} | CC | 0 | – | 24 | ns | |

1) This input timing is valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

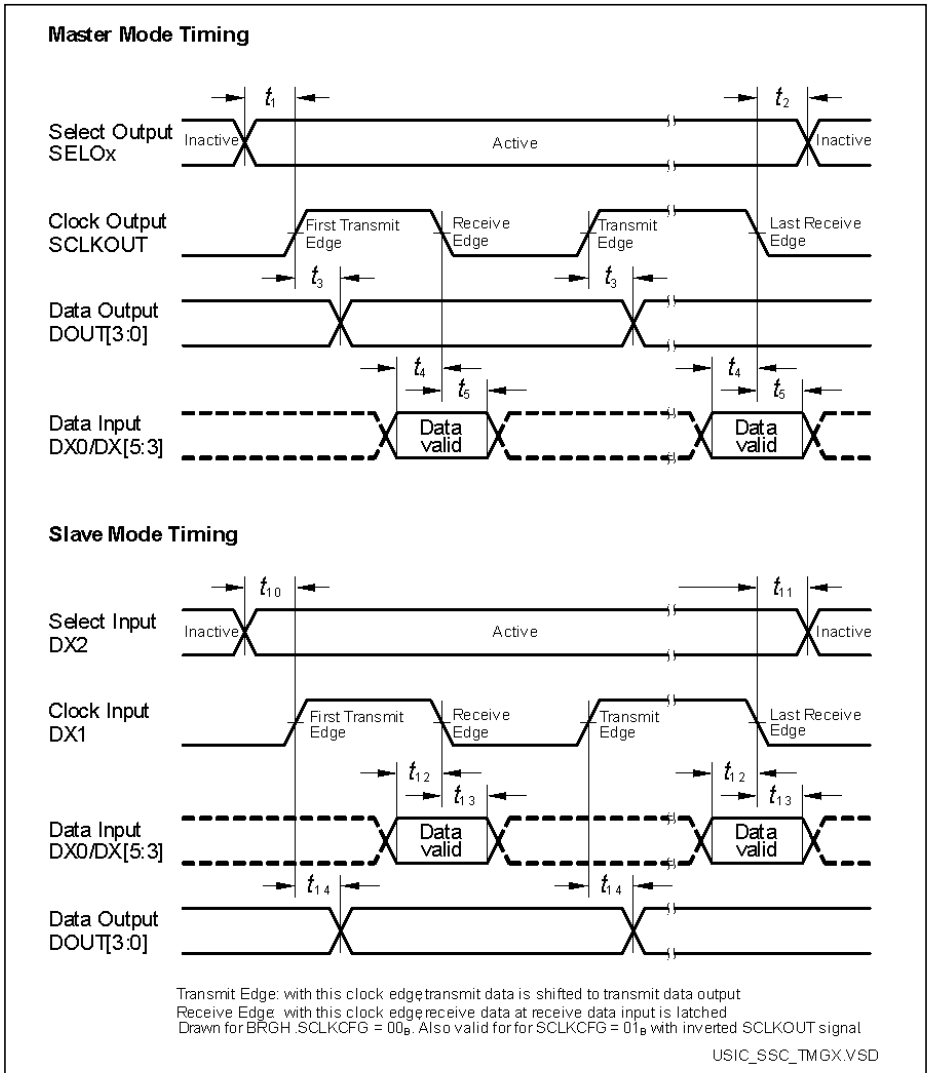


Figure 33 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.

3.3.9.3 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 45 USIC IIC Standard Mode Timing¹⁾

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-------------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Fall time of both SDA and SCL | t_1 CC/SR | - | - | 300 | ns | |
| Rise time of both SDA and SCL | t_2 CC/SR | - | - | 1000 | ns | |
| Data hold time | t_3 CC/SR | 0 | - | - | μs | |
| Data set-up time | t_4 CC/SR | 250 | - | - | ns | |
| LOW period of SCL clock | t_5 CC/SR | 4.7 | - | - | μs | |
| HIGH period of SCL clock | t_6 CC/SR | 4.0 | - | - | μs | |
| Hold time for (repeated) START condition | t_7 CC/SR | 4.0 | - | - | μs | |
| Set-up time for repeated START condition | t_8 CC/SR | 4.7 | - | - | μs | |
| Set-up time for STOP condition | t_9 CC/SR | 4.0 | - | - | μs | |
| Bus free time between a STOP and START condition | t_{10} CC/SR | 4.7 | - | - | μs | |
| Capacitive load for each bus line | C_b SR | - | - | 400 | pF | |

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

Table 46 USIC IIC Fast Mode Timing¹⁾

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-------------------|---------------------------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Fall time of both SDA and SCL | t_1 CC/SR | 20 + 0.1 * C_b 2) | - | 300 | ns | |
| Rise time of both SDA and SCL | t_2 CC/SR | 20 + 0.1 * C_b 2) | - | 300 | ns | |
| Data hold time | t_3 CC/SR | 0 | - | - | μs | |
| Data set-up time | t_4 CC/SR | 100 | - | - | ns | |
| LOW period of SCL clock | t_5 CC/SR | 1.3 | - | - | μs | |
| HIGH period of SCL clock | t_6 CC/SR | 0.6 | - | - | μs | |
| Hold time for (repeated) START condition | t_7 CC/SR | 0.6 | - | - | μs | |
| Set-up time for repeated START condition | t_8 CC/SR | 0.6 | - | - | μs | |
| Set-up time for STOP condition | t_9 CC/SR | 0.6 | - | - | μs | |
| Bus free time between a STOP and START condition | t_{10} CC/SR | 1.3 | - | - | μs | |
| Capacitive load for each bus line | C_b SR | - | - | 400 | pF | |

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.

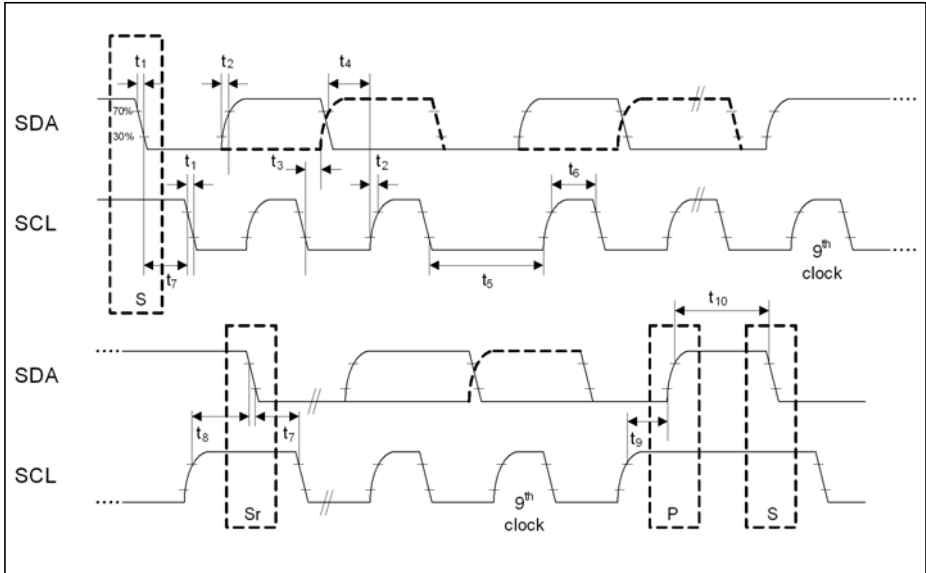


Figure 34 USIC IIC Stand and Fast Mode Timing

3.3.9.4 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 47 USIC IIS Master Transmitter Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-----------------|----------|------------------------|------|------------------------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Clock period | t_1 CC | 33.3 | – | – | ns | |
| Clock high time | t_2 CC | $0.35 \times t_{1min}$ | – | – | ns | |
| Clock low time | t_3 CC | $0.35 \times t_{1min}$ | – | – | ns | |
| Hold time | t_4 CC | 0 | – | – | ns | |
| Clock rise time | t_5 CC | – | – | $0.15 \times t_{1min}$ | ns | |

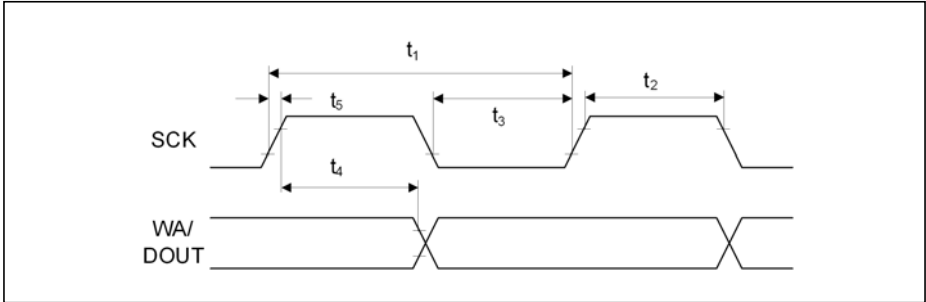


Figure 35 USIC IIS Master Transmitter Timing

Table 48 USIC IIS Slave Receiver Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-----------------|-------------|-------------------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Clock period | t_6 SR | 66.6 | – | – | ns | |
| Clock high time | t_7 SR | 0.35 x t_{6min} | – | – | ns | |
| Clock low time | t_8 SR | 0.35 x t_{6min} | – | – | ns | |
| Set-up time | t_9 SR | 0.2 x t_{6min} | – | – | ns | |
| Hold time | t_{10} SR | 0 | – | – | ns | |

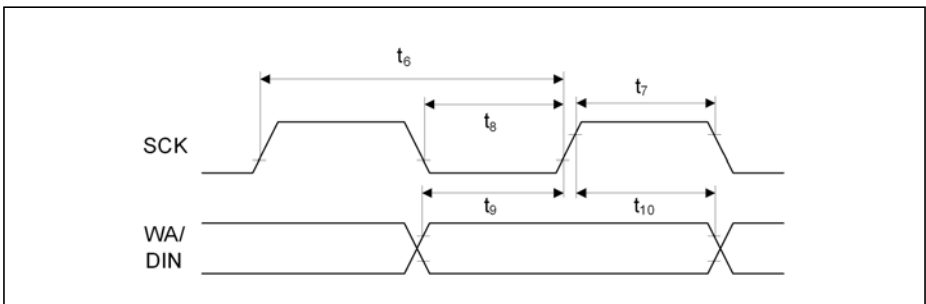


Figure 36 USIC IIS Slave Receiver Timing

3.3.9.5 SDMMC Interface Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply, total external capacitive load $C_L = 40$ pF.

AC Timing Specifications (Full-Speed Mode)

Table 49 SDMMC Timing for Full-Speed Mode

| Parameter | Symbol | Values | Unit | | Note/ Test Condition |
|--|------------------|--------|------|------|----------------------|
| | | | Min. | Max. | |
| Clock frequency in full speed transfer mode ($1/t_{pp}$) | f_{pp} CC | 0 | 24 | MHz | |
| Clock cycle in full speed transfer mode | t_{pp} CC | 40 | – | ns | |
| Clock low time | t_{WL} CC | 10 | – | ns | |
| Clock high time | t_{WH} CC | 10 | – | ns | |
| Clock rise time | t_{TLH} CC | – | 10 | ns | |
| Clock fall time | t_{THL} CC | – | 10 | ns | |
| Inputs setup to clock rising edge | t_{ISU_F} SR | 2 | – | ns | |
| Inputs hold after clock rising edge | t_{IH_F} SR | 2 | – | ns | |
| Outputs valid time in full speed mode | t_{ODLY_F} CC | – | 10 | ns | |
| Outputs hold time in full speed mode | t_{OH_F} CC | 0 | – | ns | |

Table 50 SD Card Bus Timing for Full-Speed Mode¹⁾

| Parameter | Symbol | Values | | Unit | Note/ Test Condition |
|--------------------------|-----------|--------|------|------|----------------------|
| | | Min. | Max. | | |
| SD card input setup time | t_{ISU} | 5 | – | ns | |
| SD card input hold time | t_{IH} | 5 | – | ns | |

Table 50 SD Card Bus Timing for Full-Speed Mode¹⁾ (cont'd)

| Parameter | Symbol | Values | | Unit | Note/ Test Condition |
|---------------------------|------------|--------|------|------|----------------------|
| | | Min. | Max. | | |
| SD card output valid time | t_{ODLY} | – | 14 | ns | |
| SD card output hold time | t_{OH} | 0 | – | ns | |

1) Reference card timing values for calculation examples. Not subject to production test and not characterized.

Full-Speed Output Path (Write)

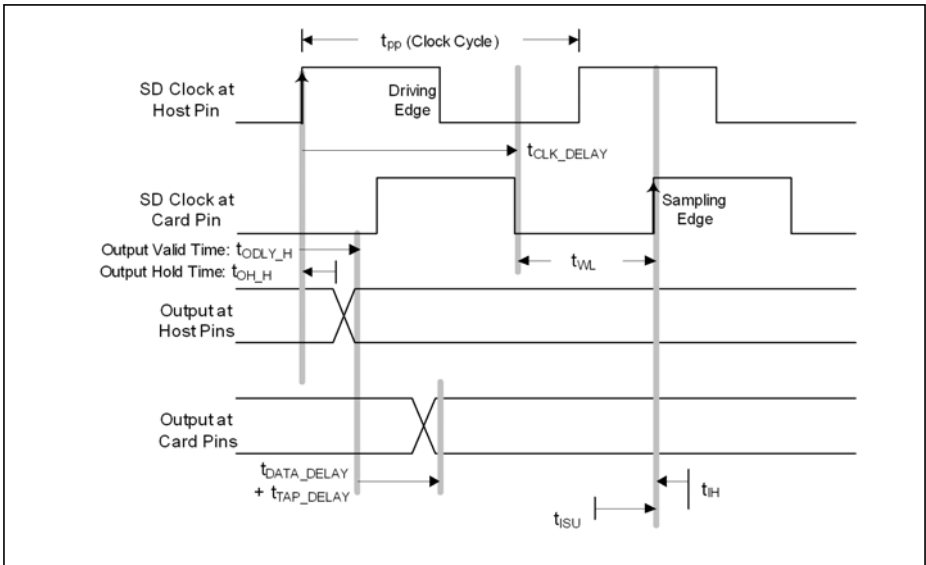


Figure 37 Full-Speed Output Path

Full-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

No clock delay:

(1)

$$t_{ODLY_F} + t_{DATA_DELAY} + t_{TAP_DELAY} + t_{ISU} < t_{WL}$$

With clock delay:

$$t_{ODLY_F} + t_{DATA_DELAY} + t_{TAP_DELAY} + t_{ISU} < t_{WL} + t_{CLK_DELAY} \quad (2)$$

$$t_{DATA_DELAY} + t_{TAP_DELAY} + t_{WL} < t_{PP} + t_{CLK_DELAY} - t_{ISU} - t_{ODLY_F} \quad (3)$$

$$t_{DATA_DELAY} + t_{TAP_DELAY} + 20 < 40 + t_{CLK_DELAY} - 5 - 10$$

$$t_{DATA_DELAY} < 5 + t_{CLK_DELAY} - t_{TAP_DELAY}$$

The data can be delayed versus clock up to 5 ns in ideal case of $t_{WL} = 20$ ns.

Full-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK_DELAY} < t_{WL} + t_{OH_F} + t_{DATA_DELAY} + t_{TAP_DELAY} - t_{IH} \quad (4)$$

$$t_{CLK_DELAY} < 20 + t_{DATA_DELAY} + t_{TAP_DELAY} - 5$$

$$t_{DATA_DELAY} < 15 + t_{CLK_DELAY} + t_{TAP_DELAY}$$

The clock can be delayed versus data up to 18.2 ns (external delay line) in ideal case of $t_{WL} = 20$ ns, with maximum $t_{TAP_DELAY} = 3.2$ ns programmed.

Full-Speed Input Path (Read)

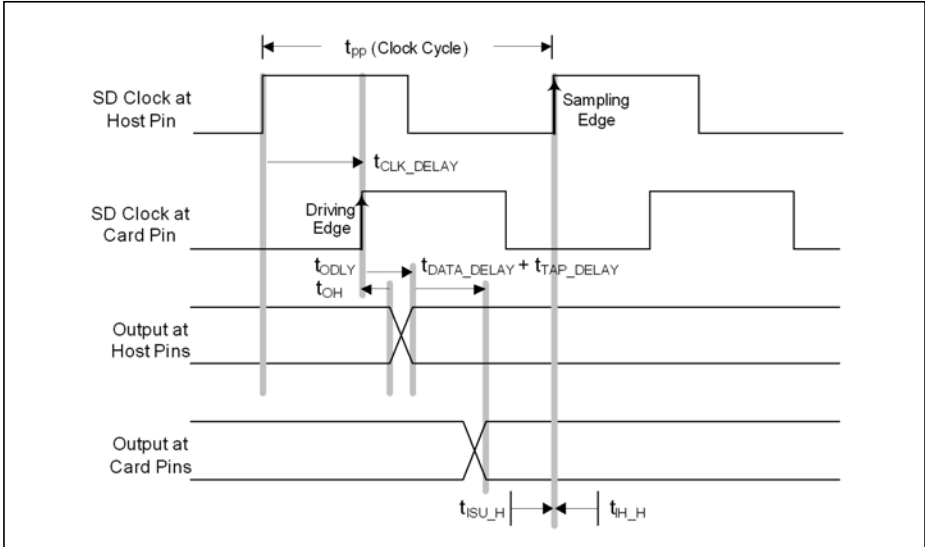


Figure 38 Full-Speed Input Path

Full-Speed Read Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(5)

$$t_{CLK_DELAY} + t_{DATA_DELAY} + t_{TAP_DELAY} + t_{ODLY} + t_{ISU_F} < 0.5 \times t_{pp}$$

$$t_{CLK_DELAY} + t_{DATA_DELAY} < 0.5 \times t_{pp} - t_{ODLY} - t_{ISU_F} - t_{TAP_DELAY}$$

$$t_{CLK_DELAY} + t_{DATA_DELAY} < 20 - 14 - 2 - t_{TAP_DELAY}$$

$$t_{CLK_DELAY} + t_{DATA_DELAY} < 4 - t_{TAP_DELAY}$$

The data + clock delay can be up to 4 ns for a 40 ns clock cycle.

Electrical Parameters

Full-Speed Read Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(6)

$$t_{\text{CLK_DELAY}} + t_{\text{OH}} + t_{\text{DATA_DELAY}} + t_{\text{TAP_DELAY}} > t_{\text{IH_F}}$$

$$t_{\text{CLK_DELAY}} + t_{\text{DATA_DELAY}} > t_{\text{IH_F}} - t_{\text{OH}} - t_{\text{TAP_DELAY}}$$

$$t_{\text{CLK_DELAY}} + t_{\text{DATA_DELAY}} > 2 - t_{\text{TAP_DELAY}}$$

The data + clock delay must be greater than 2 ns if $t_{\text{TAP_DELAY}}$ is not used.

If the $t_{\text{TAP_DELAY}}$ is programmed to at least 2 ns, the data + clock delay must be greater than 0 ns (or less). This is always fulfilled.

AC Timing Specifications (High-Speed Mode)

Table 51 SDMMC Timing for High-Speed Mode

| Parameter | Symbol | | Values | | Unit | Note/ Test Condition |
|---|----------------------|----|--------|------|------|----------------------|
| | | | Min. | Max. | | |
| Clock frequency in high speed transfer mode ($1/t_{\text{pp}}$) | f_{pp} | CC | 0 | 48 | MHz | |
| Clock cycle in high speed transfer mode | t_{pp} | CC | 20 | – | ns | |
| Clock low time | t_{WL} | CC | 7 | – | ns | |
| Clock high time | t_{WH} | CC | 7 | – | ns | |
| Clock rise time | t_{TLH} | CC | – | 3 | ns | |
| Clock fall time | t_{THL} | CC | – | 3 | ns | |
| Inputs setup to clock rising edge | $t_{\text{ISU_H}}$ | SR | 2 | – | ns | |
| Inputs hold after clock rising edge | $t_{\text{IH_H}}$ | SR | 2 | – | ns | |
| Outputs valid time in high speed mode | $t_{\text{ODLY_H}}$ | CC | – | 14 | ns | |
| Outputs hold time in high speed mode | $t_{\text{OH_H}}$ | CC | 2 | – | ns | |

Table 52 SD Card Bus Timing for High-Speed Mode¹⁾

| Parameter | Symbol | Values | | Unit | Note/ Test Condition |
|---------------------------|------------|--------|------|------|----------------------|
| | | Min. | Max. | | |
| SD card input setup time | t_{ISU} | 6 | – | ns | |
| SD card input hold time | t_{IH} | 2 | – | ns | |
| SD card output valid time | t_{ODLY} | – | 14 | ns | |
| SD card output hold time | t_{OH} | 2.5 | – | ns | |

1) Reference card timing values for calculation examples. Not subject to production test and not characterized.

High-Speed Output Path (Write)

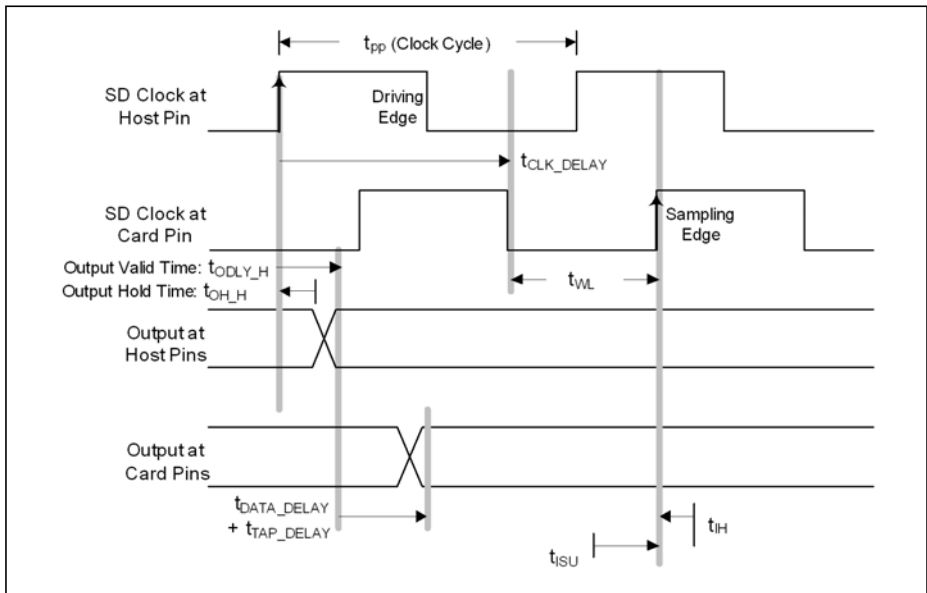


Figure 39 High-Speed Output Path

High-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew between the SD_CLK and SD_DAT/CMD signals on the PCB.

Electrical Parameters

No clock delay:

(7)

$$t_{ODLY_H} + t_{DATA_DELAY} + t_{TAP_DELAY} + t_{ISU} < t_{WL}$$

With clock delay:

(8)

$$t_{ODLY_H} + t_{DATA_DELAY} + t_{TAP_DELAY} + t_{ISU} < t_{WL} + t_{CLK_DELAY}$$

(9)

$$t_{DATA_DELAY} + t_{TAP_DELAY} - t_{CLK_DELAY} < t_{WL} - t_{ISU} - t_{ODLY_H}$$

$$t_{DATA_DELAY} - t_{CLK_DELAY} < t_{WL} - t_{ISU} - t_{ODLY_H} - t_{TAP_DELAY}$$

$$t_{DATA_DELAY} - t_{CLK_DELAY} < 10 - 6 - 14 - t_{TAP_DELAY}$$

$$t_{DATA_DELAY} - t_{CLK_DELAY} < -10 - t_{TAP_DELAY}$$

The data delay is less than the clock delay by at least 10 ns in the ideal case where $t_{WL} = 10$ ns.

High-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

(10)

$$t_{CLK_DELAY} < t_{WL} + t_{OH_H} + t_{DATA_DELAY} + t_{TAP_DELAY} - t_{IH}$$

$$t_{CLK_DELAY} - t_{DATA_DELAY} < t_{WL} + t_{OH_H} + t_{TAP_DELAY} - t_{IH}$$

$$t_{CLK_DELAY} - t_{DATA_DELAY} < 10 + 2 + t_{TAP_DELAY} - 2$$

$$t_{CLK_DELAY} - t_{DATA_DELAY} < 10 + t_{TAP_DELAY}$$

The clock can be delayed versus data up to 13.2 ns (external delay line) in ideal case of $t_{WL} = 10$ ns, with maximum $t_{TAP_DELAY} = 3.2$ ns programmed.

High-Speed Input Path (Read)

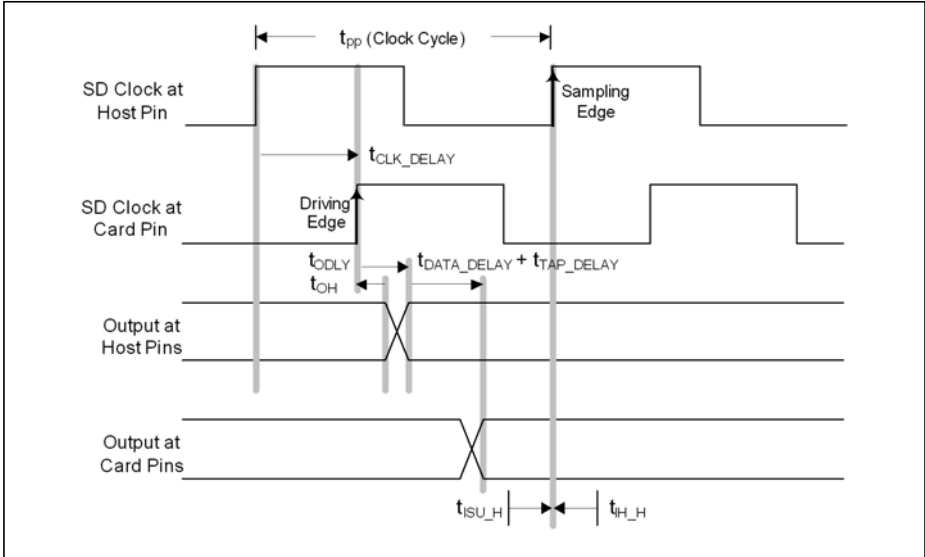


Figure 40 High-Speed Input Path

High-Speed Read Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(11)

$$t_{CLK_DELAY} + t_{DATA_DELAY} + t_{TAP_DELAY} + t_{ODLY} + t_{ISU_H} < t_{pp}$$

$$t_{CLK_DELAY} + t_{DATA_DELAY} < t_{pp} - t_{ODLY} - t_{ISU_H} - t_{TAP_DELAY}$$

$$t_{CLK_DELAY} + t_{DATA_DELAY} < 20 - 14 - 2 - t_{TAP_DELAY}$$

$$t_{CLK_DELAY} + t_{DATA_DELAY} < 4 - t_{TAP_DELAY}$$

The data + clock delay can be up to 4 ns for a 20 ns clock cycle.

High-Speed Read Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(12)

$$t_{\text{CLK_DELAY}} + t_{\text{OH}} + t_{\text{DATA_DELAY}} + t_{\text{TAP_DELAY}} > t_{\text{IH_H}}$$

$$t_{\text{CLK_DELAY}} + t_{\text{DATA_DELAY}} > t_{\text{IH_H}} - t_{\text{OH}} - t_{\text{TAP_DELAY}}$$

$$t_{\text{CLK_DELAY}} + t_{\text{DATA_DELAY}} > 2 - 2.5 - t_{\text{TAP_DELAY}}$$

$$t_{\text{CLK_DELAY}} + t_{\text{DATA_DELAY}} > -0.5 - t_{\text{TAP_DELAY}}$$

The data + clock delay must be greater than -0.5 ns for a 20 ns clock cycle. This is always fulfilled.

3.3.10 EBU Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply, with Class A2 pins and $C_L = 16$ pF.

3.3.10.1 EBU Asynchronous Timing

Note: For each timing, the accumulated PLL jitter must be added separately.

Table 53 Common Timing Parameters for all Asynchronous Timings

| Parameter | | Symbol | Limit Values | | Unit | Edge Setting |
|--|--|--------|--------------|------|------|--------------|
| | | | Min. | Max. | | |
| Pulse width deviation from the ideal programmed width due to the A2 pad asymmetry, strong driver mode, rise delay - fall delay. $C_L = 16$ pF. | CC | t_a | -1 | 1.5 | ns | sharp |
| | | | -2 | 1 | | medium |
| AD(24:16) output delay | to $\overline{\text{ADV}}$ rising edge, multiplexed read / write | CC | t_{13} | -5.5 | 2 | – |
| AD(24:16) output delay | | CC | t_{14} | -5.5 | 2 | – |

Read Timing

Table 54 Asynchronous Read Timing, Multiplexed and Demultiplexed

| Parameter | | Symbol | Limit Values | | Unit | |
|-----------------------------------|--|--------|--------------|------|------|----|
| | | | Min. | Max. | | |
| A(24:16) output delay | to \overline{RD} rising edge, deviation from the ideal programmed value. | CC | t_0 | -2.5 | 2.5 | ns |
| A(24:16) output delay | | CC | t_1 | -2.5 | 2.5 | |
| \overline{CS} rising edge | | CC | t_2 | -2 | 2.5 | |
| \overline{ADV} rising edge | | CC | t_3 | -1.5 | 4.5 | |
| \overline{BC} rising edge | | CC | t_4 | -2.5 | 2.5 | |
| \overline{WAIT} input setup | | SR | t_5 | 12 | – | |
| \overline{WAIT} input hold | | SR | t_6 | 0 | – | |
| Data input setup | | SR | t_7 | 12 | – | |
| Data input hold | | SR | t_8 | 0 | – | |
| RD / \overline{WR} output delay | | CC | t_9 | -2.5 | 1.5 | |

Multiplexed Read Timing

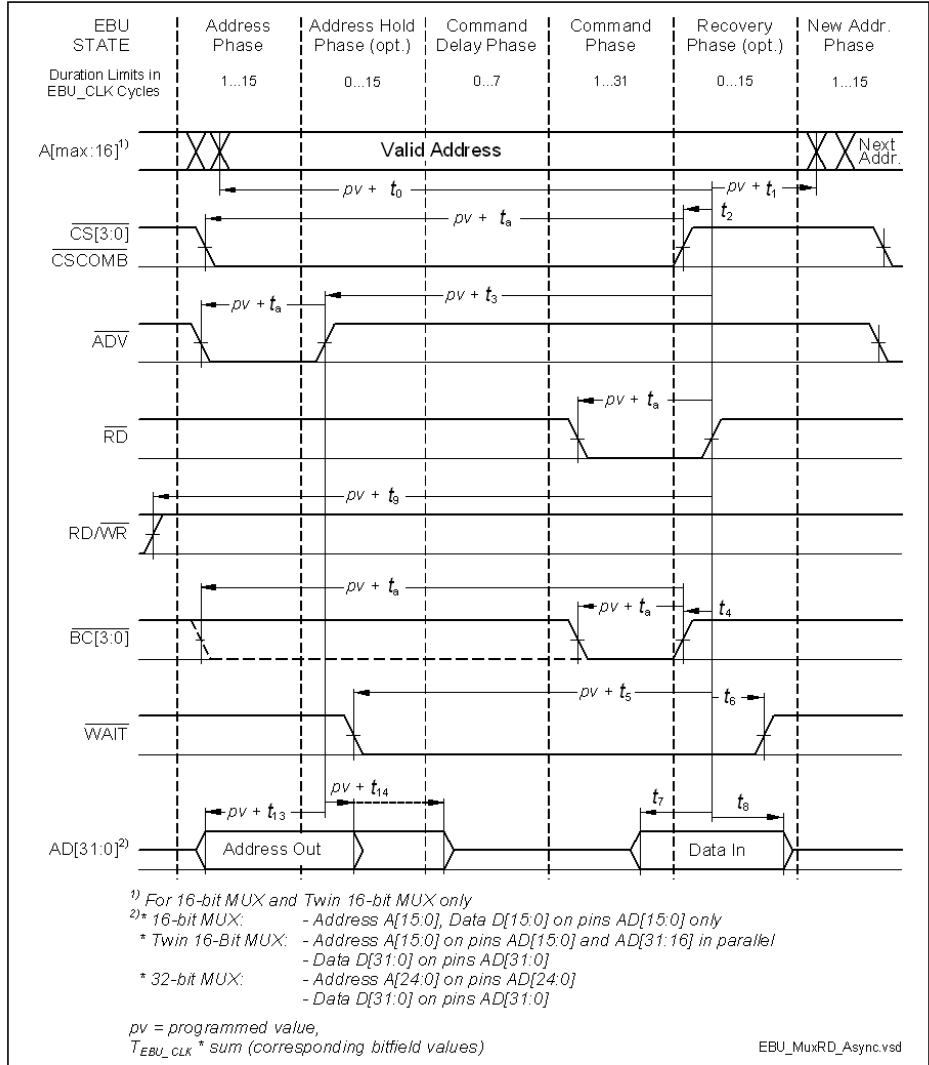


Figure 41 Multiplexed Read Access

Demultiplexed Read Timing

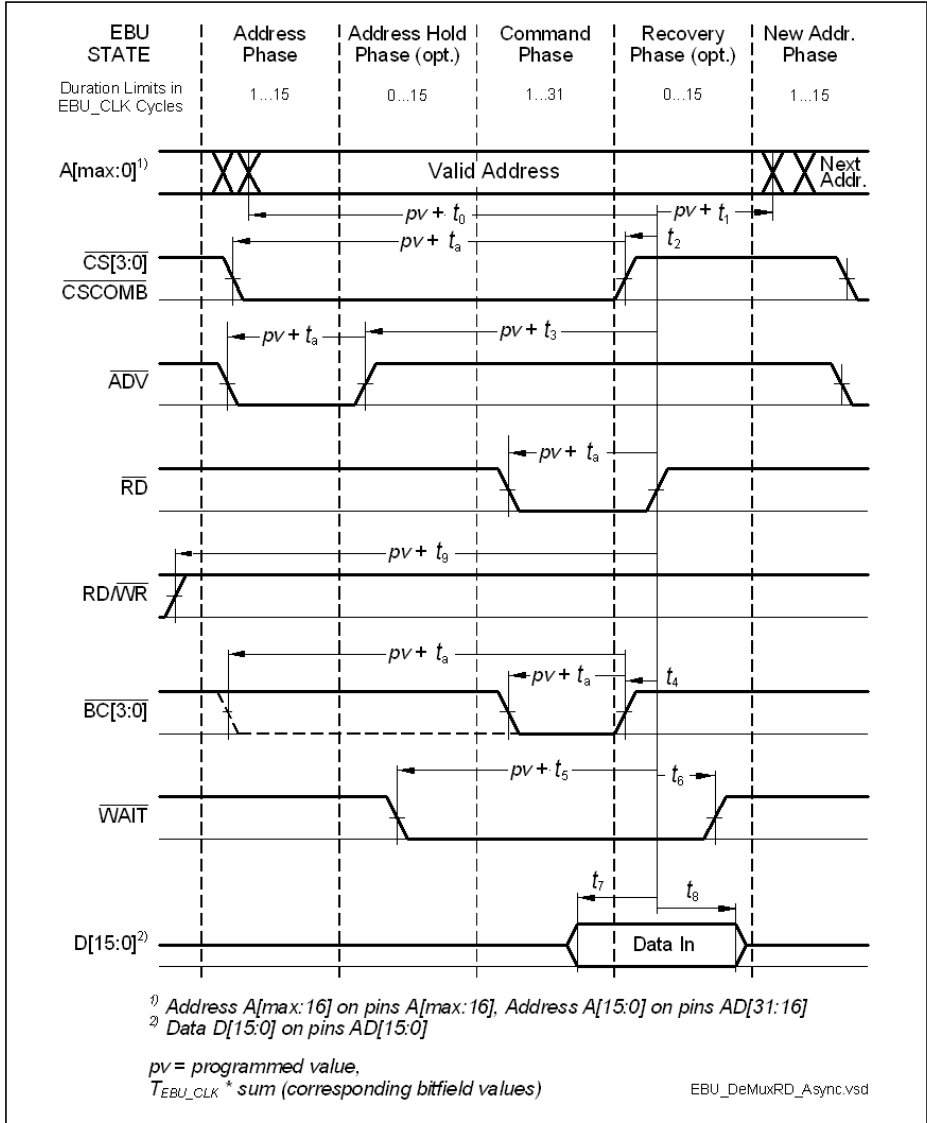


Figure 42 Demultiplexed Read Access

Write Timing

Table 55 Asynchronous Write Timing, Multiplexed and Demultiplexed

| Parameter | | Symbol | Limit Values | | Unit |
|--|---|-------------|--------------|------|------|
| | | | Min. | Max. | |
| A(24:0) output delay | to RD/ $\overline{\text{WR}}$ rising edge, deviation from the ideal programmed value. | CC t_{30} | -2.5 | 2.5 | ns |
| A(24:0) output delay | | CC t_{31} | -2.5 | 2.5 | |
| $\overline{\text{CS}}$ rising edge | | CC t_{32} | -2 | 2 | |
| $\overline{\text{ADV}}$ rising edge | | CC t_{33} | -2 | 4.5 | |
| $\overline{\text{BC}}$ rising edge | | CC t_{34} | -2.5 | 2 | |
| $\overline{\text{WAIT}}$ input setup | | SR t_{35} | 12 | – | |
| $\overline{\text{WAIT}}$ input hold | | SR t_{36} | 0 | – | |
| Data output delay | | CC t_{37} | -5.5 | 2 | |
| Data output delay | | CC t_{38} | -5.5 | 2 | |
| RD / $\overline{\text{WR}}$ output delay | | CC t_{39} | -2.5 | 1.5 | |

Multiplexed Write Timing

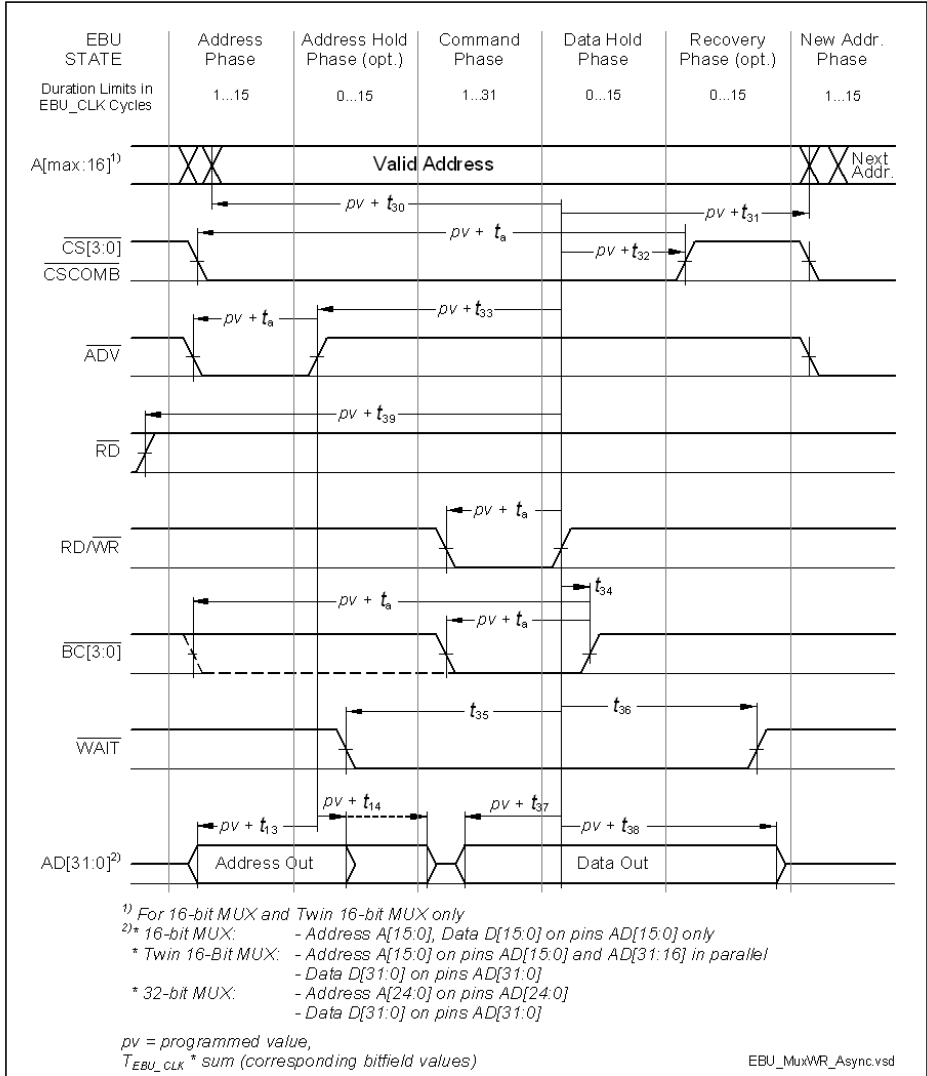


Figure 43 Multiplexed Write Access

Demultiplexed Write Timing

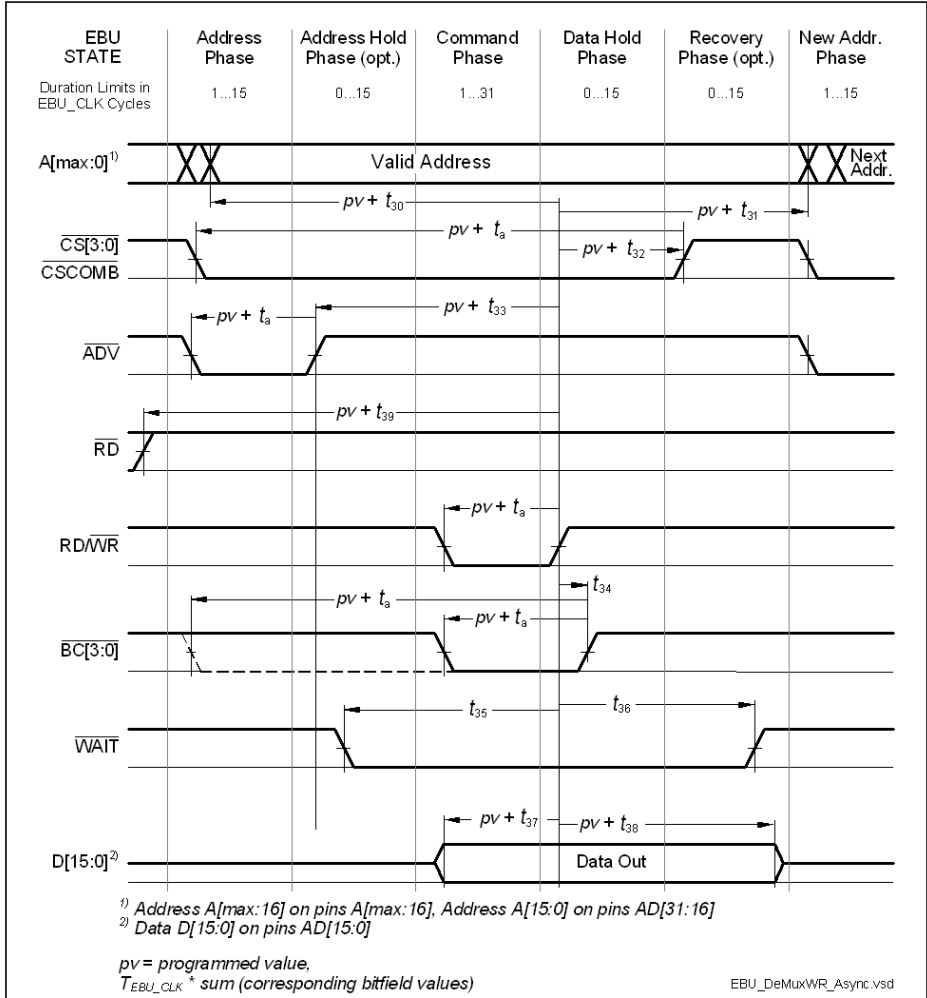


Figure 44 Demultiplexed Write Access

3.3.10.2 EBU Burst Mode Access Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply, with Class A2 pins and $C_L = 16$ pF.

Table 56 EBU Burst Mode Read / Write Access Timing Parameters

| Parameter | Symbol | CC | Values | | | Unit | Note / Test Condition |
|--|-----------|----|--------|------|------|------|-----------------------|
| | | | Min. | Typ. | Max. | | |
| Output delay from BFCLKO rising edge | t_{10} | CC | -2 | – | 2 | ns | – |
| \overline{RD} and $\overline{RD}/\overline{WR}$ active/inactive after BFCLKO active edge ¹⁾ | t_{12} | CC | -2 | – | 2 | ns | – |
| \overline{CSx} output delay from BFCLKO active edge ¹⁾ | t_{21} | CC | -2.5 | – | 1.5 | ns | – |
| \overline{ADV} active/inactive after BFCLKO active edge ²⁾ | t_{22} | CC | -2 | – | 2 | ns | – |
| \overline{BAA} active/inactive after BFCLKO active edge ²⁾ | t_{22a} | CC | -2.5 | – | 1.5 | ns | – |
| Data setup to BFCLKI rising edge ³⁾ | t_{23} | SR | 3 | – | – | ns | – |
| Data hold from BFCLKI rising edge ³⁾ | t_{24} | SR | 0 | – | – | ns | – |
| \overline{WAIT} setup (low or high) to BFCLKI rising edge ³⁾ | t_{25} | SR | 3 | – | – | ns | – |
| \overline{WAIT} hold (low or high) from BFCLKI rising edge ³⁾ | t_{26} | SR | 0 | – | – | ns | – |

1) An active edge can be a rising or falling edge, depending on the settings of bits BFCON.EBSE / ECSE and the clock divider ratio.

Negative minimum values for these parameters mean that the last data read during a burst may be corrupted. However, with clock feedback enabled, this value is an oversampling not required for the internal bus transaction, and will be discarded.

2) This parameter is valid for BUSCONx.EBSE = 1 and BUSAPx.EXTCLK = 0_B.

For BUSCONx.EBSE = 1 and other values of BUSAPx.EXTCLK, ADV and BAA will be delayed by 1/2 of the internal bus clock period $T_{CPU} = 1 / f_{CPU}$.

For BUSCONx. EBSE = 0 and BUSAPx.EXTCLK = 11_B, add 2 internal bus clock periods.

For BUSCONx. EBSE = 0 and other values of BUSAPx.EXTCLK, add 1 internal bus clock period.

Electrical Parameters

3) If the clock feedback is not enabled, the input signals are latched using the internal clock in the same way as for asynchronous access. Thus, t_5 , t_6 , t_7 and t_8 from the asynchronous timing apply.

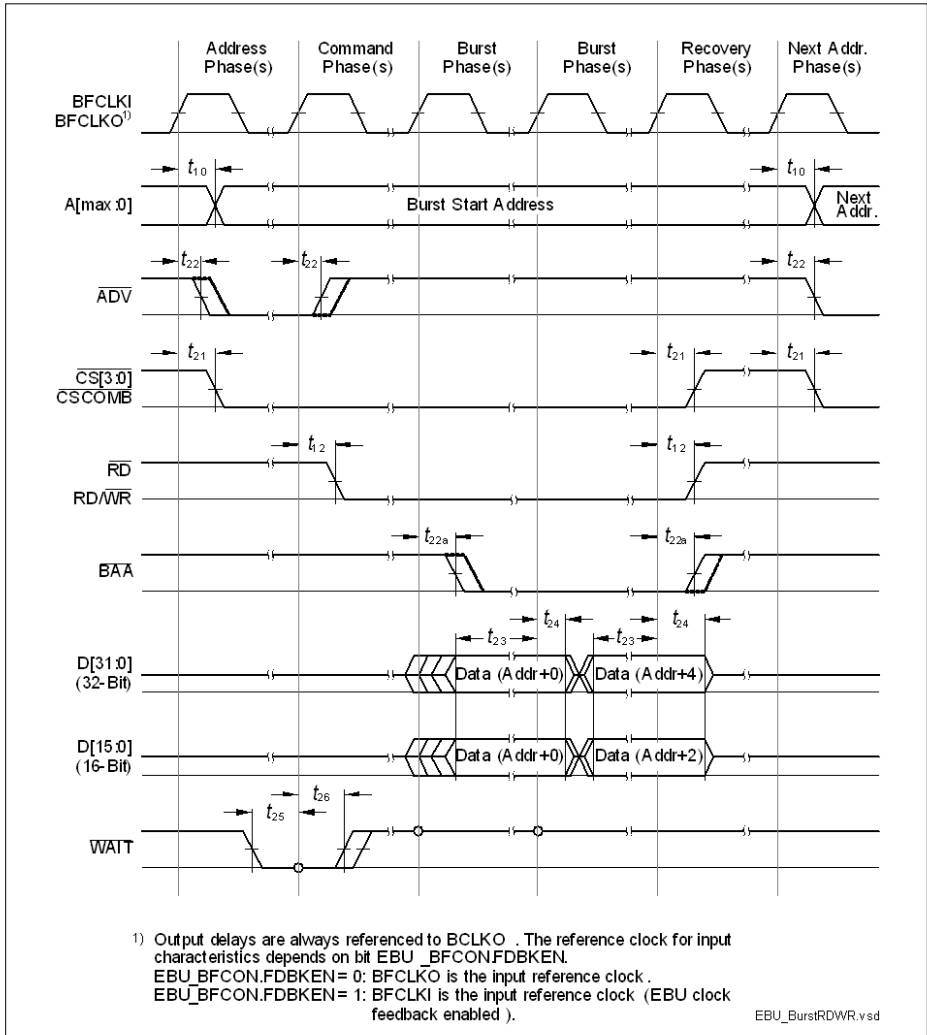


Figure 45 EBU Burst Mode Read / Write Access Timing

3.3.10.3 EBU Arbitration Signal Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 57 EBU Arbitration Signal Timing Parameters

| Parameter | Symbol | CC | Values | | | Unit | Note / Test Condition |
|--------------------------------------|--------|----|--------|------|------|------|-----------------------|
| | | | Min. | Typ. | Max. | | |
| Output delay from BFCLKO rising edge | t_1 | CC | – | – | 16 | ns | $C_L = 50 \text{ pF}$ |
| Data setup to BFCLKO falling edge | t_2 | SR | 11 | – | – | ns | – |
| Data hold from BFCLKO falling edge | t_3 | SR | 2 | – | – | ns | – |

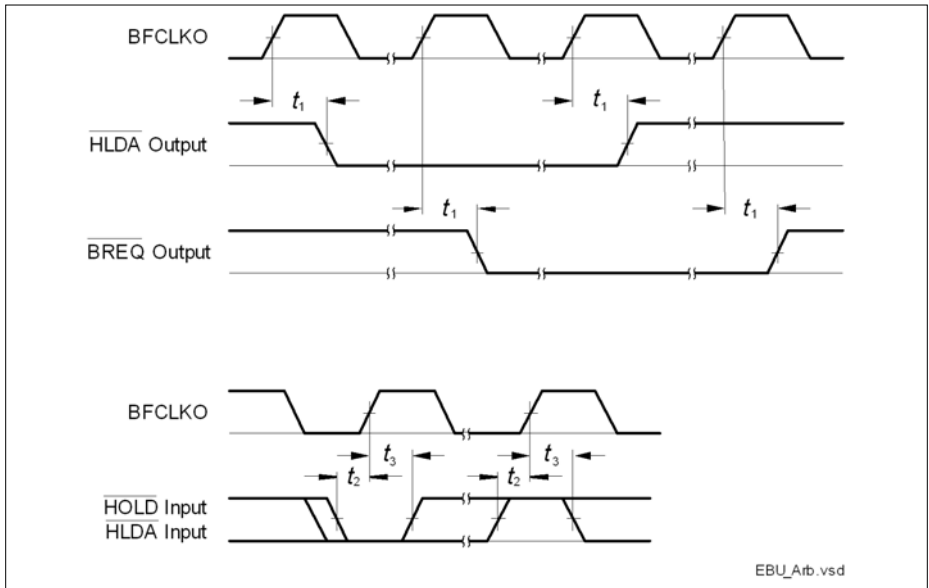


Figure 46 EBU Arbitration Signal Timing

3.3.10.4 EBU SDRAM Access Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply, with Class A2 pins and $C_L = 16$ pF.

Table 58 EBU SDRAM Access SDCLKO Signal Timing Parameters

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|------------------|--------|----|--------|------|------|------|-----------------------|
| | | | Min. | Typ. | Max. | | |
| SDCLKO period | t_1 | CC | 12.5 | – | – | ns | – |
| SDCLKO high time | t_2 | SR | 5.5 | – | – | ns | – |
| SDCLKO low time | t_3 | SR | 3.75 | – | – | ns | – |
| SDCLKO rise time | t_4 | SR | – | – | 3.0 | ns | – |
| SDCLKO fall time | t_5 | SR | – | – | 3.0 | ns | – |

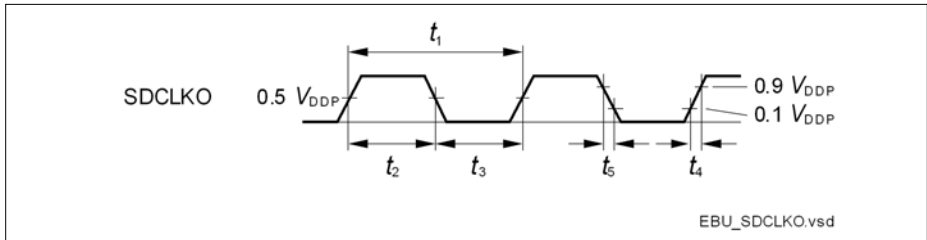


Figure 47 EBU SDRAM Access CLKOUT Timing

Table 59 EBU SDRAM Access Signal Timing Parameters

| Parameter | | Symbol | Limit Values | | Unit |
|--|--|-------------|--------------|------|------|
| | | | Min. | Max. | |
| A(15:0) output valid | from SDCLKO low-to-high transition | CC t_6 | – | 9 | ns |
| A(15:0) output hold | | CC t_7 | 3 | – | |
| $\overline{\text{CS}}(3:0)$ low | | CC t_8 | – | 9 | |
| $\overline{\text{CS}}(3:0)$ high | | CC t_9 | 3 | – | |
| $\overline{\text{RAS}}$ low | | CC t_{10} | – | 9 | |
| $\overline{\text{RAS}}$ high | | SR t_{11} | 3 | – | |
| $\overline{\text{CAS}}$ low | | SR t_{12} | – | 9 | |
| $\overline{\text{CAS}}$ high | | CC t_{13} | 3 | – | |
| $\overline{\text{RD}}/\overline{\text{WR}}$ low | | CC t_{14} | – | 9 | |
| $\overline{\text{RD}}/\overline{\text{WR}}$ high | | CC t_{15} | 3 | – | |
| $\overline{\text{BC}}(3:0)$ low | | CC t_{16} | – | 9 | |
| $\overline{\text{BC}}(3:0)$ high | | CC t_{17} | 3 | – | |
| D(15:0) output valid | | CC t_{18} | – | 9 | |
| D(15:0) output hold | | CC t_{19} | 3 | – | |
| CKE output valid ¹⁾ | | CC t_{22} | – | 7 | |
| CKE output hold ¹⁾ | | CC t_{23} | 2 | – | |
| D(15:0) input hold | | SR t_{21} | 3 | – | |
| D(15:0) input setup to SDCLKO low-to-high transition | SR t_{20} | 4 | – | | |

1) Not depicted in the read and write access timing figures below.

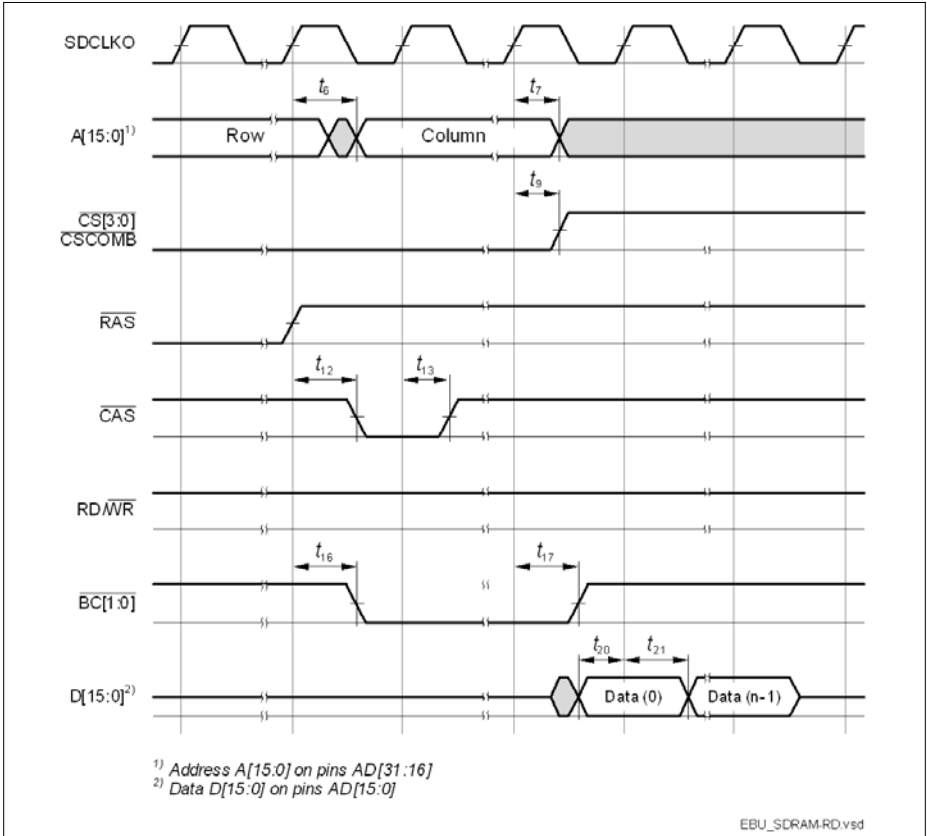


Figure 48 EBU SDRAM Read Access Timing

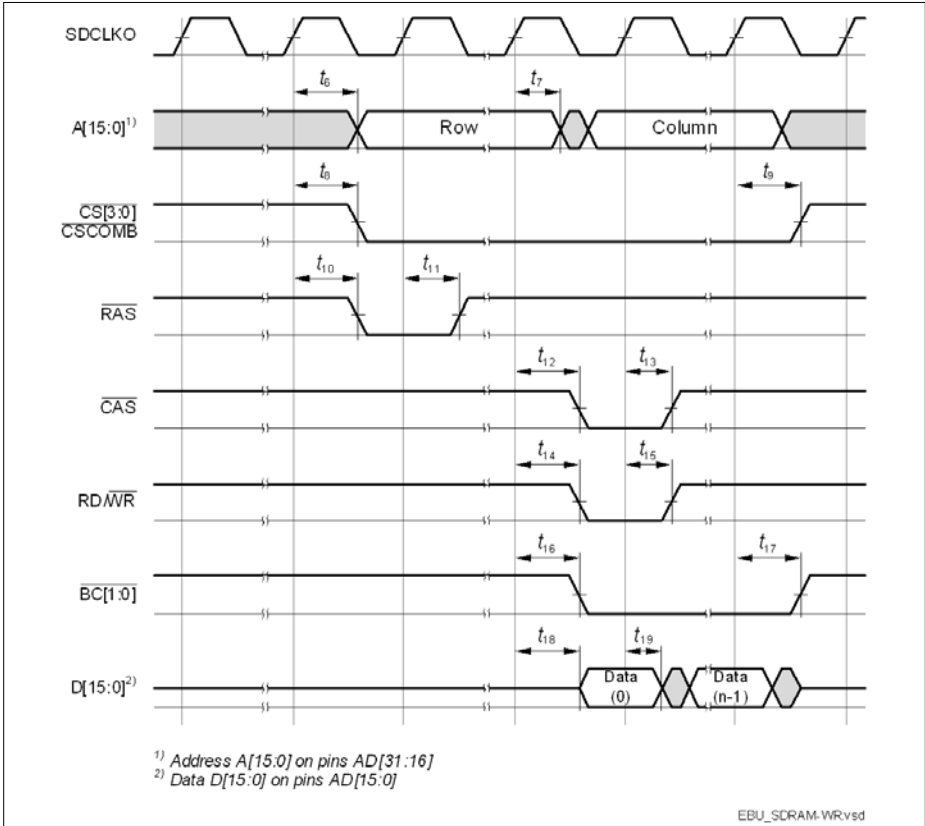


Figure 49 EBU SDRAM Write Access Timing

3.3.11 USB Interface Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 60 USB Timing Parameters (operating conditions apply)

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|-------------------------|-----------|----|--------|------|--------|------|-----------------------|
| | | | Min. | Typ. | Max. | | |
| Rise time | t_R | CC | 4 | – | 20 | ns | $C_L = 50 \text{ pF}$ |
| Fall time | t_F | CC | 4 | – | 20 | ns | $C_L = 50 \text{ pF}$ |
| Rise/Fall time matching | t_R/t_F | CC | 90 | – | 111.11 | % | $C_L = 50 \text{ pF}$ |
| Crossover voltage | V_{CRS} | CC | 1.3 | – | 2.0 | V | $C_L = 50 \text{ pF}$ |

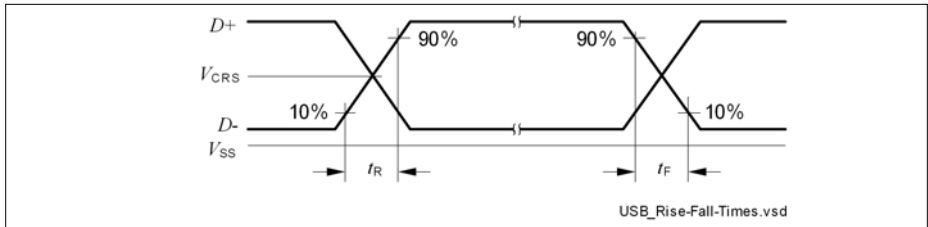


Figure 50 USB Signal Timing

3.3.12 Ethernet Interface (ETH) Characteristics

For proper operation of the Ethernet Interface it is required that $f_{SYS} \geq 100$ MHz.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.12.1 ETH Measurement Reference Points

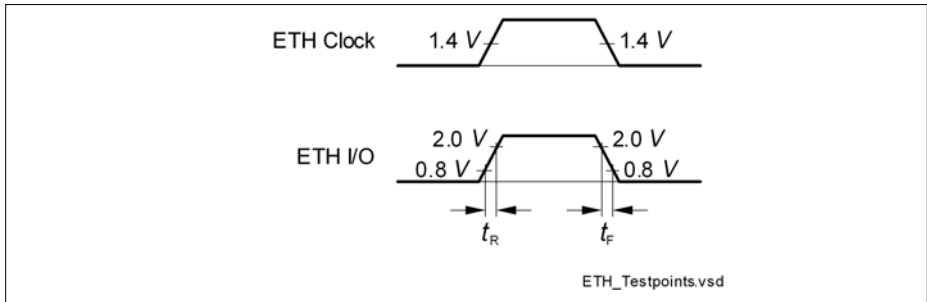


Figure 51 ETH Measurement Reference Points

3.3.12.2 ETH Management Signal Parameters (ETH_MDC, ETH_MDIO)

Table 61 ETH Management Signal Timing Parameters

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|------------------------------|--------|----|--------|------|------|------|-----------------------|
| | | | Min. | Typ. | Max. | | |
| ETH_MDC period | t_1 | CC | 400 | – | – | ns | $C_L = 25 \text{ pF}$ |
| ETH_MDC high time | t_2 | CC | 160 | – | – | ns | |
| ETH_MDC low time | t_3 | CC | 160 | – | – | ns | |
| ETH_MDIO setup time (output) | t_4 | CC | 10 | – | – | ns | |
| ETH_MDIO hold time (output) | t_5 | CC | 10 | – | – | ns | |
| ETH_MDIO data valid (input) | t_6 | SR | 0 | – | 300 | ns | |

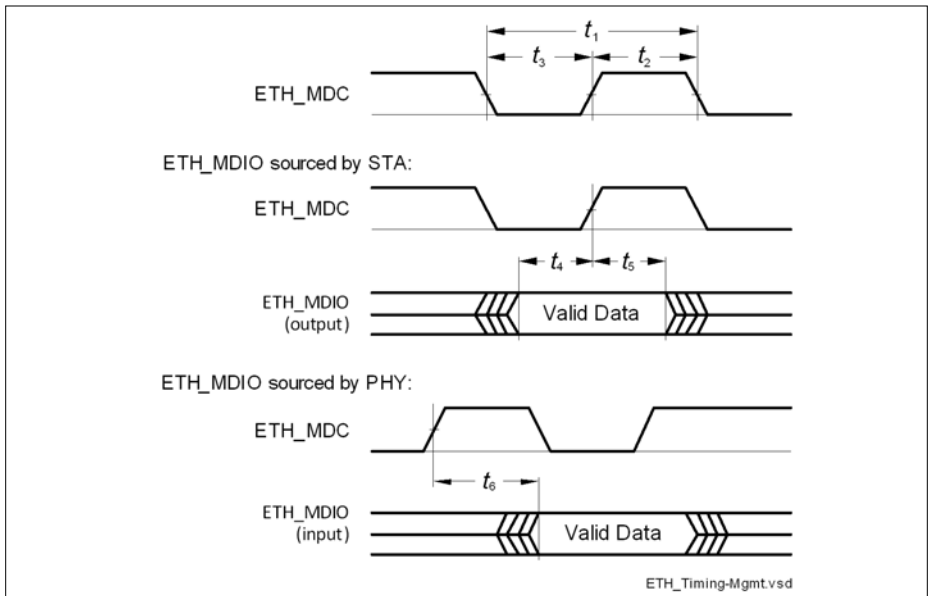


Figure 52 ETH Management Signal Timing

3.3.12.3 ETH MII Parameters

In the following, the parameters of the MII (Media Independent Interface) are described.

Table 62 ETH MII Signal Timing Parameters

| Parameter | Symbol | SR | Values | | | Unit | Note / Test Condition |
|---------------------------|----------|----|--------|------|------|------|-----------------------|
| | | | Min. | Typ. | Max. | | |
| Clock period, 10 Mbps | t_7 | SR | 400 | – | – | ns | $C_L = 25 \text{ pF}$ |
| Clock high time, 10 Mbps | t_8 | SR | 140 | – | 260 | ns | |
| Clock low time, 10 Mbps | t_9 | SR | 140 | – | 260 | ns | |
| Clock period, 100 Mbps | t_7 | SR | 40 | – | – | ns | |
| Clock high time, 100 Mbps | t_8 | SR | 14 | – | 26 | ns | |
| Clock low time, 100 Mbps | t_9 | SR | 14 | – | 26 | ns | |
| Input setup time | t_{10} | SR | 10 | – | – | ns | |
| Input hold time | t_{11} | SR | 10 | – | – | ns | |
| Output valid time | t_{12} | CC | 0 | – | 25 | ns | |

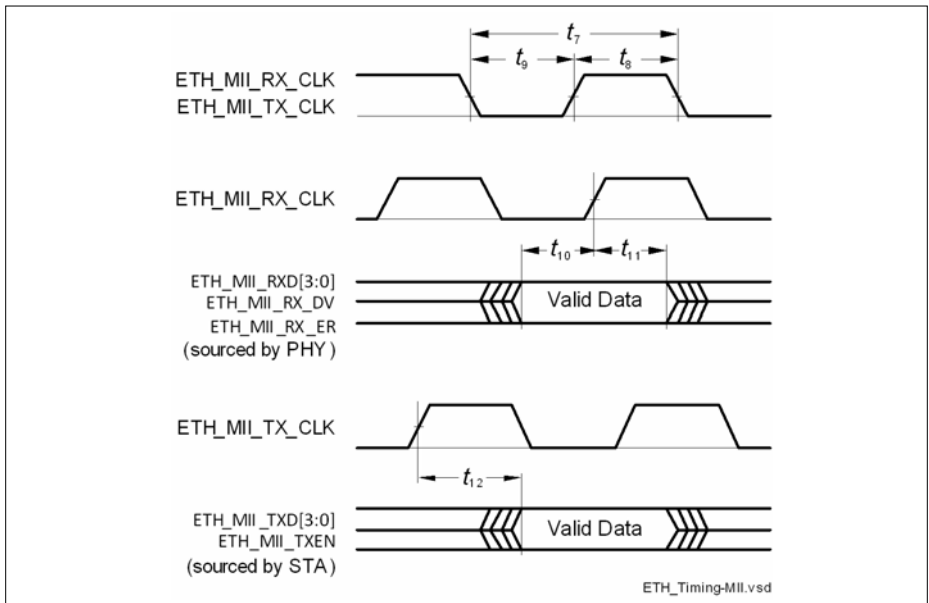


Figure 53 ETH MII Signal Timing

3.3.12.4 ETH RMII Parameters

In the following, the parameters of the RMII (Reduced Media Independent Interface) are described.

Table 63 ETH RMII Signal Timing Parameters

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|--|----------|----|--------|------|------|------|-----------------------------------|
| | | | Min. | Typ. | Max. | | |
| ETH_RMII_REF_CL clock period | t_{13} | SR | 20 | – | – | ns | $C_L = 25 \text{ pF}$; 50 ppm |
| ETH_RMII_REF_CL clock high time | t_{14} | SR | 7 | – | 13 | ns | $C_L = 25 \text{ pF}$ |
| ETH_RMII_REF_CL clock low time | t_{15} | SR | 7 | – | 13 | ns | |
| ETH_RMII_RXD[1:0], ETH_RMII_CRS setup time | t_{16} | SR | 4 | – | – | ns | |
| ETH_RMII_RXD[1:0], ETH_RMII_CRS hold time | t_{17} | SR | 2 | – | – | ns | |
| ETH_RMII_TXD[1:0], ETH_RMII_TXEN data valid | t_{18} | CC | 4 | – | 15 | ns | |

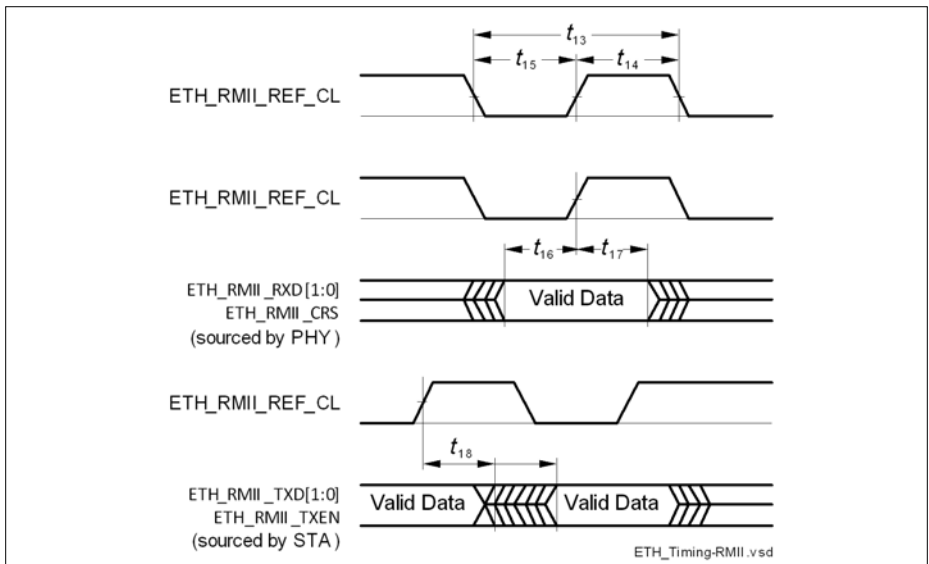


Figure 54 ETH RMII Signal Timing

4 Package and Reliability

The XMC4500 is a member of the XMC4000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the Exposed Die Pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 64 provides the thermal characteristics of the packages used in XMC4500.

Table 64 Thermal Characteristics of the Packages

| Parameter | Symbol | Limit Values | | Unit | Package Types |
|---|------------------------|--------------|------------------|------|------------------------------|
| | | Min. | Max. | | |
| Exposed Die Pad Dimensions (including U-Groove where applicable) | $E_x \times E_y$ CC | - | 6.5×6.5 | mm | PG-LQFP-144-24 |
| | | - | 7.0×7.0 | mm | PG-LQFP-100-25 |
| Exposed Die Pad Dimensions | - | - | 7.0×7.0 | mm | PG-LQFP-100-29 |
| | | - | 6.5×6.5 | mm | PG-LQFP-144-26 |
| Thermal resistance Junction-Ambient $T_j \leq 150 \text{ }^\circ\text{C}$ | $R_{\Theta JA}$ CC | - | 40.5 | K/W | PG-LFBGA-144-10 |
| | | - | 19.5 | K/W | PG-LQFP-144-24 ¹⁾ |
| | | - | 21.0 | K/W | PG-LQFP-100-25 ¹⁾ |
| | | - | 21.0 | K/W | PG-LQFP-100-29 ¹⁾ |
| | | - | 19.5 | K/W | PG-LQFP-144-26 ¹⁾ |

1) Device mounted on a 4-layer JEDEC board (JESD 51-7) with thermal vias; exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SS} , independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC4500 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$ ” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 150 °C.

The difference between junction temperature and ambient temperature is determined by $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as

$$P_{INT} = V_{DDP} \times I_{DDP} \text{ (switching current and leakage current).}$$

The static external power consumption caused by the output drivers is defined as

$$P_{IOSTAT} = \Sigma((V_{DDP} - V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP} , if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

4.2 Package Outlines

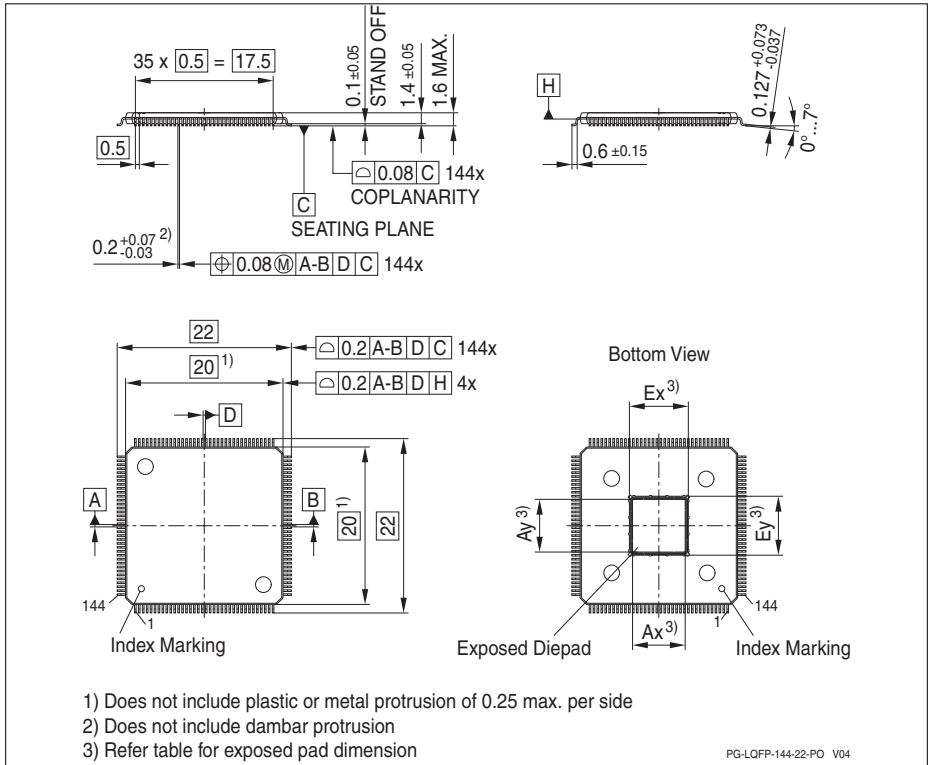


Figure 55 PG-LQFP-144-24 (Plastic Green Low Profile Quad Flat Package)

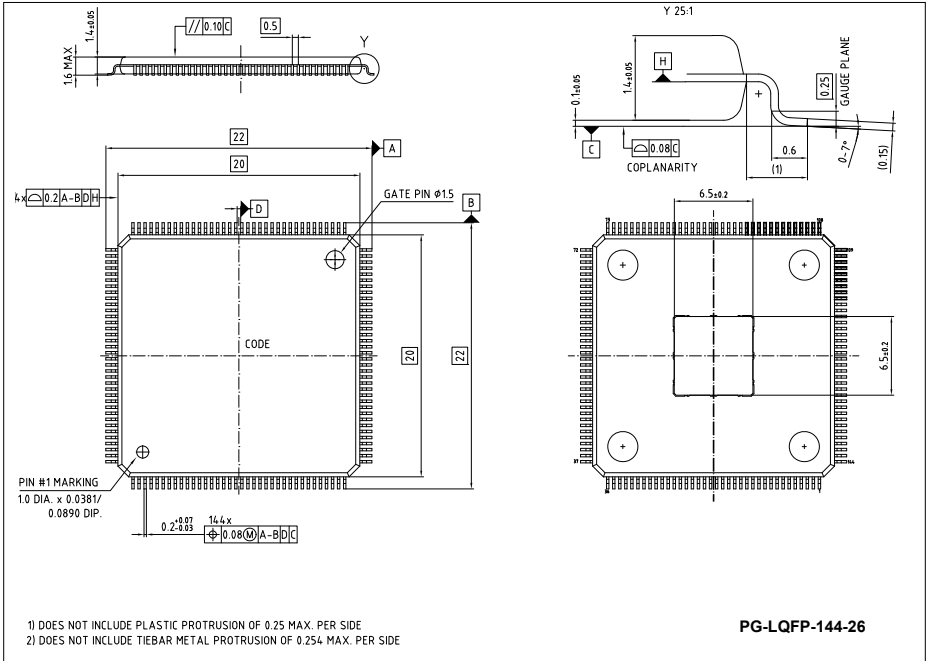


Figure 56 PG-LQFP-144-26 (Plastic Green Low Profile Quad Flat Package)

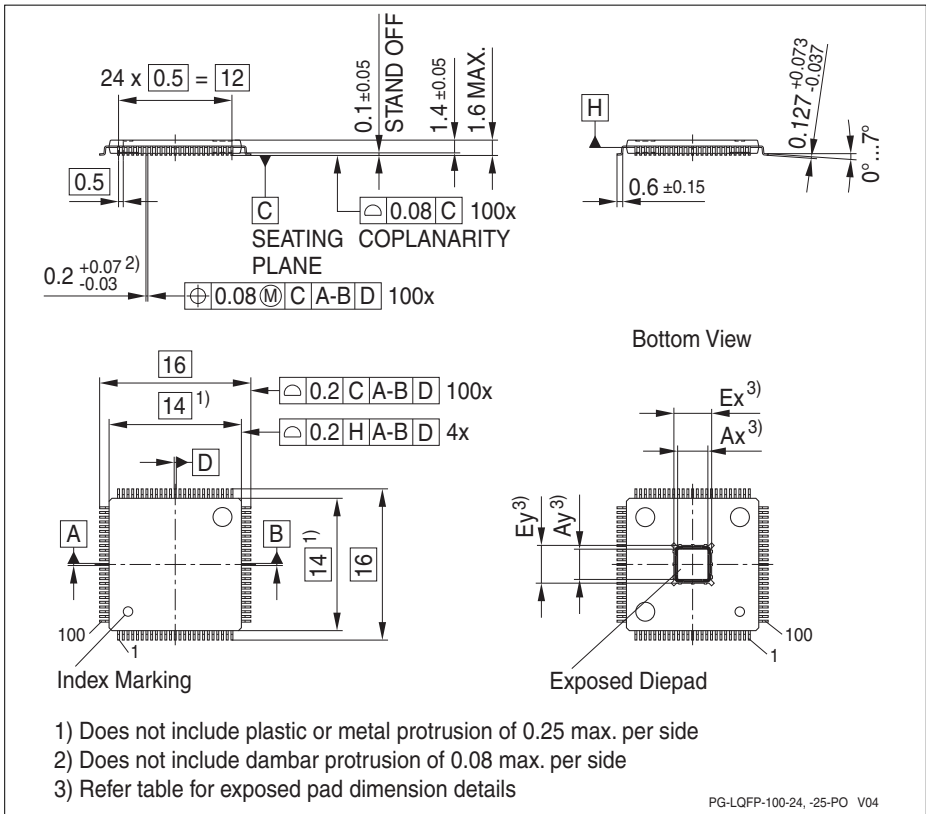


Figure 57 PG-LQFP-100-25 (Plastic Green Low Profile Quad Flat Package)

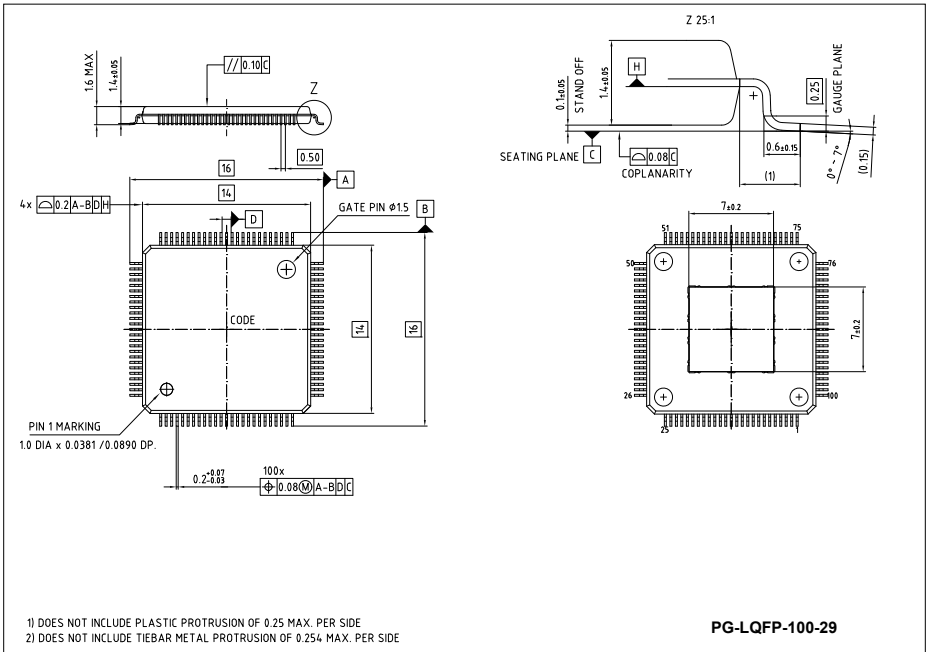


Figure 58 PG-LQFP-100-29 (Plastic Green Low Profile Quad Flat Package)

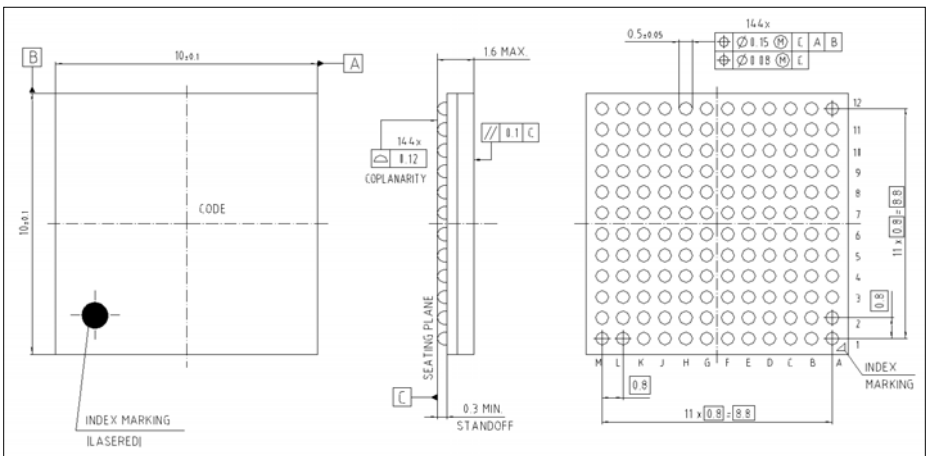


Figure 59 PG-LFBGA-144-10 (Plastic Green Low Profile Fine Pitch Ball Grid Array)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page “Packages”: <http://www.infineon.com/packages>.

4.3 Quality Declarations

The qualification of the XMC4500 is executed according to the JEDEC standard JESD47H.

Note: For automotive applications refer to the Infineon automotive microcontrollers.

Table 65 Quality Parameters

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|--------------|--------|------|-------|------------------|---|
| | | Min. | Typ. | Max. | | |
| Operation lifetime | t_{OP} CC | 20 | – | – | a | $T_J \leq 109^\circ\text{C}$, device permanent on |
| ESD susceptibility according to Human Body Model (HBM) | V_{HBM} SR | – | – | 2 000 | V | EIA/JESD22-A114-B |
| ESD susceptibility according to Charged Device Model (CDM) | V_{CDM} SR | – | – | 500 | V | Conforming to JESD22-C101-C |
| Moisture sensitivity level | MSL CC | – | – | 3 | – | JEDEC J-STD-020D |
| Soldering temperature | T_{SDR} SR | – | – | 260 | $^\circ\text{C}$ | Profile according to JEDEC J-STD-020D |

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