



**THE DATASHEET OF
ASFLMPLV-200.000MHZ-LR-T**



PERFORMANCE PLASTIC PACKAGE ULTRA MINIATURE PURE SILICON™ CLOCK OSCILLATORS

ASFLMP

Request Samples



Check Inventory



ESD Sensitive



5.0 x 3.2 x 0.85 mm

RoHS/RoHS II Compliant

MSL Level = 1

Features

- Low Power Consumption for high speed communication
- Exceptional Stability Over Temp. at -40 to +85°C, ±15ppm
- Extended Automotive Grade Temp. stability at -55 to +125°C, ±25ppm
- MIL-STD-883 shock and vibration compliant
- Durable QFN Plastic Compact Packaging
- Standby or Disable Tri-state function
- Low jitter (Period jitter RMS and Phase jitter RMS)
- High power supply noise reduction, -50dBc

Applications

- Storage Area Networks (SATA, SAS, Fiber Channel)
- Passive Optical Networks (EPON, 10G-EPON, GPON, 10G-PON)
- Ethernet (1G, 10GBASE-T, KR/LR/SR, FCoE)
- PCI Express
- Display port

Key Electrical Specifications CMOS, LVPECL, LVDS, and HCSL

Parameters		Min.	Typ.	Max.	Units	Notes
Frequency Range	CMOS	2.3000*		170.0000	MHz	-20 ~ +70°C -40 ~ +85°C
	CMOS	3.3000*		170.0000		-40 ~ +105°C -55 ~ +125°C
	LVPECL	2.3000*		460.0000		Commercial, Industrial temp. range
	LVDS	2.3000*		460.0000		Commercial, Industrial temp. range
	HCSL	2.3000*		460.0000		Commercial, Industrial temp. range
Operating Temperature		-20		+70	°C	See options
Storage Temperature		-55		+150	°C	
Overall Frequency Stability*:		-50		+50	ppm	See options
Supply Voltage (Vdd):		+2.25		+3.6	V	
Startup Time:				5	ms	
Enable Time				20	ns	STD (Tri-state)
				5	ms	PD option (Power Down)
Disable Time				5	ns	
Disable Current			20	22	mA	STD (Tri-state)
				0.095		PD option (Power Down)
Tri-state Function (Standby/Disable)		"1" (VIH≥0.75*Vdd) or Open: Oscillation "0" (VIL<0.25*Vdd) : Hi Z			V	40kΩ pull-up resistor embedded
Aging		-5.0		+5.0	ppm	First year



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Key Electrical Specifications– CMOS

Parameters	Min.	Typ.	Max.	Units	Notes
Supply Current (I _{dd})		31	35	mA	CL=15pF, 125MHz
Output Logic Level	V _{OH}	0.9*V _{dd}		V	I=±6mA
	V _{OL}		0.1*V _{dd}	V	
Rise Time		1.1	2.0	ns	CL=15pF 20% to 80%
Fall Time		1.3	2.0	ns	
Duty Cycle	45		55	%	
Integrated Phase Jitter (JPH)		0.30	2	ps	200kHz ~ 20MHz@125MHz
		0.38	2		100kHz ~ 20MHz@125MHz
		1.70	2		12kHz ~ 20MHz@125MHz
Period Jitter RMS (JPER)		3.0		ps	

Key Electrical Specifications– LVPECL

Parameters	Min.	Typ.	Max.	Units	Notes
Supply Current (I _{dd})		56.5	58	mA	RL=50Ω
Output Logic Level	V _{OH}	V _{dd} -1.08		V	RL=50Ω
	V _{OL}		V _{dd} -1.55	V	
Peak to Peak Output Swing (V _{pp})		800		mV	Single ended
Rise Time		250		ps	RL=50Ω , CL=0pF 20% to 80%
Fall Time		250			
Duty Cycle		48	52	%	Differential
Integrated Phase Jitter (J _{PH})		0.25	2	ps	200kHz ~ 20MHz @156.25MHz
		0.38	2		100kHz ~ 20MHz @156.25MHz
		1.70	2		12kHz ~ 20MHz @156.25MHz
Period Jitter RMS (J _{PER})		2.5		ps	



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Key Electrical Specifications– LVDS

Parameters	Min.	Typ.	Max.	Units	Notes
Supply Current (I_{dd})		29	32	mA	RL=100Ω
Output Offset Voltage (V_{OS})	1.125		1.4	V	RL=100Ω differential
Delta Offset Voltage (ΔV_{OS})			50	mV	
Peak to Peak Output Swing (V_{pp})		350		mV	Single ended
Rise Time		200		ps	RL=50Ω , CL=2pF 20% to 80%
Fall Time		200			
Duty Cycle	48		52	%	Differential
Integrated Phase Jitter (J_{PH})		0.28	2	ps	200kHz ~ 20MHz @156.25MHz
		0.40	2		100kHz ~ 20MHz @156.25MHz
		1.70	2		12kHz ~ 20MHz @156.25MHz
Period Jitter RMS (J_{PER})		2.5		ps	

Key Electrical Specifications– HCSL

Parameters	Min.	Typ.	Max.	Units	Notes
Supply Current (I_{dd})		40	42	mA	RL=50Ω
Output Logic Level	V_{OH}	0.725		V	RL=50Ω
	V_{OL}		0.1	V	
Peak to Peak Output Swing (V_{pp})		750		mV	Single ended
Rise Time		200	400	ps	RL=50Ω , CL=2pF 20% to 80%
Fall Time		200	400		
Duty Cycle	48		52	%	Differential
Integrated Phase Jitter (J_{PH})		0.28	2	ps	200kHz ~ 20MHz @156.25MHz
		0.40	2		100kHz ~ 20MHz @156.25MHz
		1.70	2		12kHz ~ 20MHz @156.25MHz
Period Jitter RMS (J_{PER})		2.5		ps	



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Absolute Maximum Ratings

Parameters	Min.	Max.	Units	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	V _{dd} +0.3	V	
Junction Temp.		+150	°C	
Storage Temp.	-55	+150	°C	
Soldering Temp.		+260	°C	40sec max
ESD			V	
HBM		4,000		
MM		400		
CDM		1,500		

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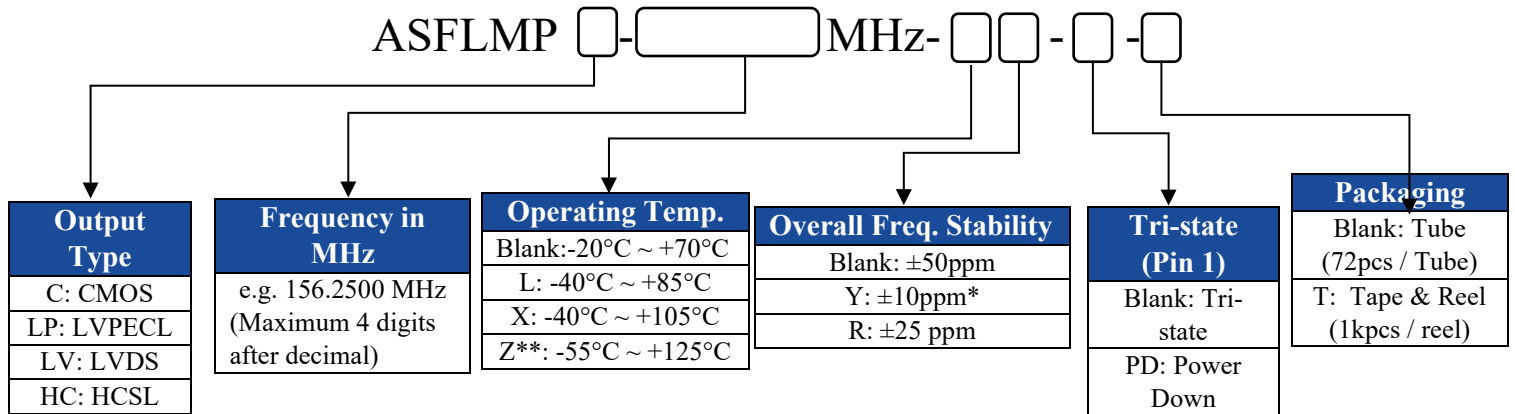


ESD Sensitive



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RoHS/RoHS II Compliant
MSL Level = 1

Options and Part Identification (left blank if standard)



* Temp option L, X or -20°C ~ +70°C, only

** CMOS output only

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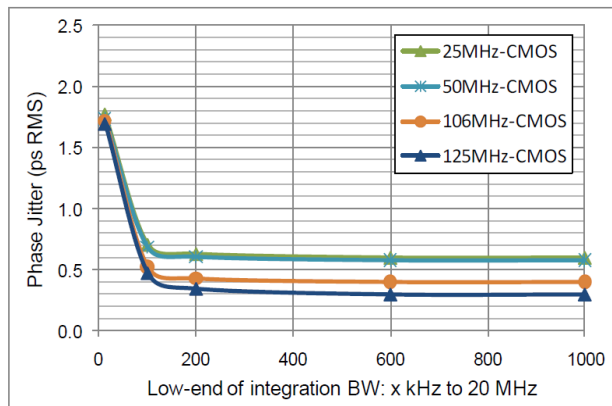
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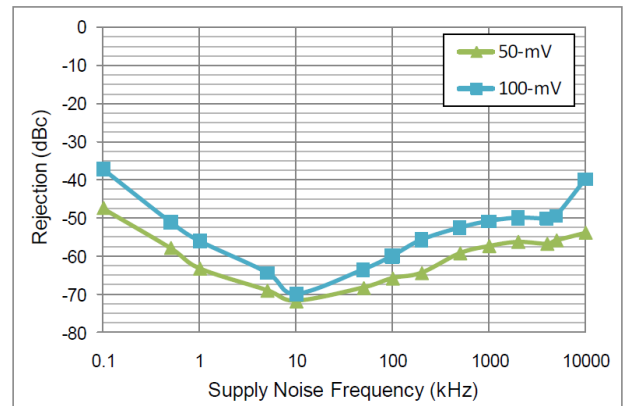
5.0 x 3.2 x 0.85 mm
RoHS/RoHS II Compliant
MSL Level = 1

Nominal Performance Parameters (Unless specified otherwise: T=25° C, VDD=3.3 V)

CMOS output

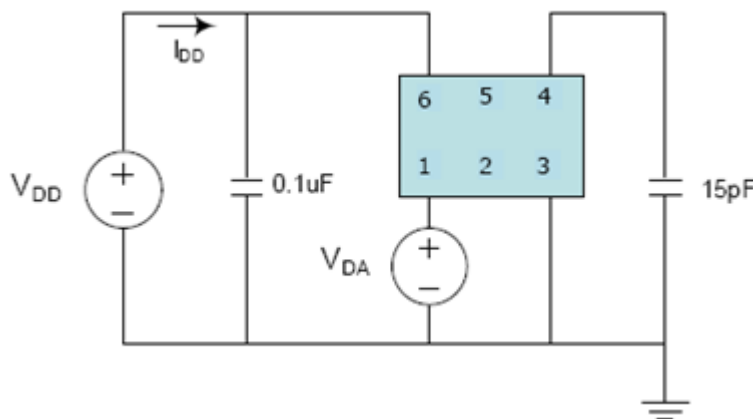


Phase jitter (integrated phase noise)



Power supply rejection ratio

Test Circuit



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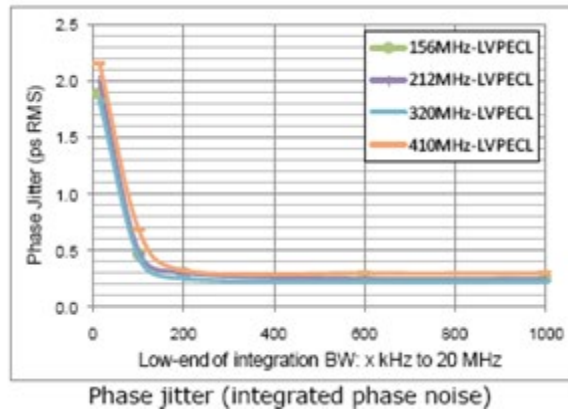
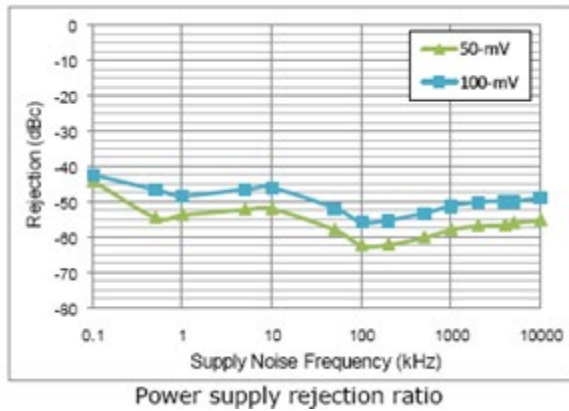


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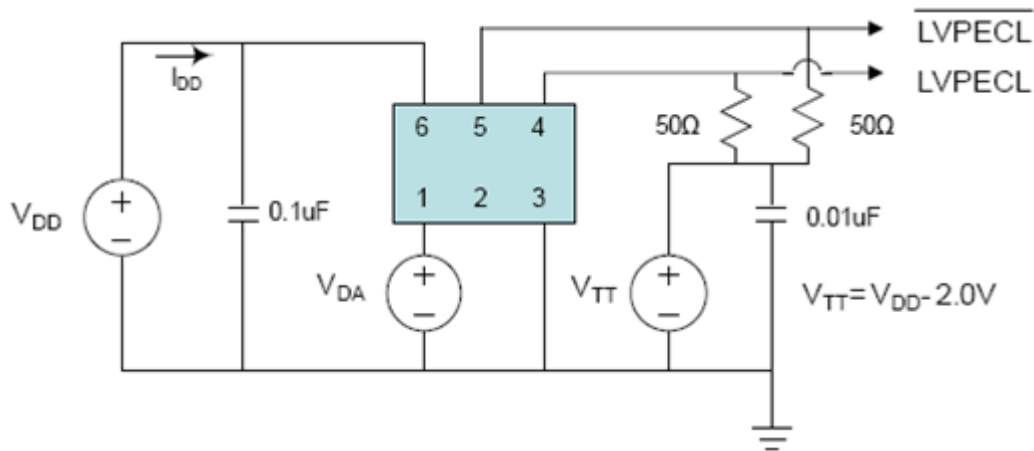


5.0 x 3.2 x 0.85 mm
RoHS/RoHS II Compliant
MSL Level = 1

LVPECL output



Test Circuit



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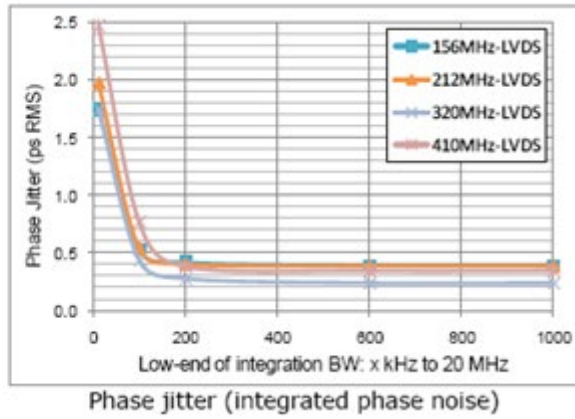
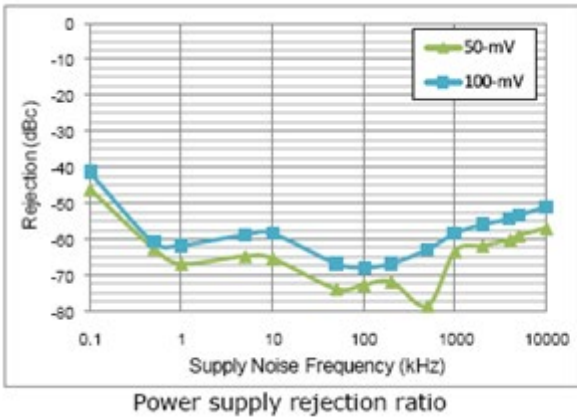
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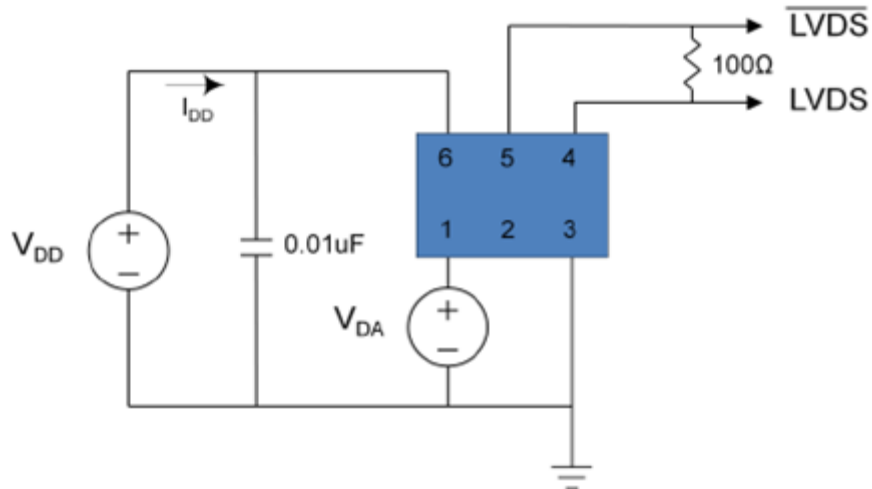
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5.0 x 3.2 x 0.85 mm
RoHS/RoHS II Compliant
MSL Level = 1

LVDS output



Test Circuit



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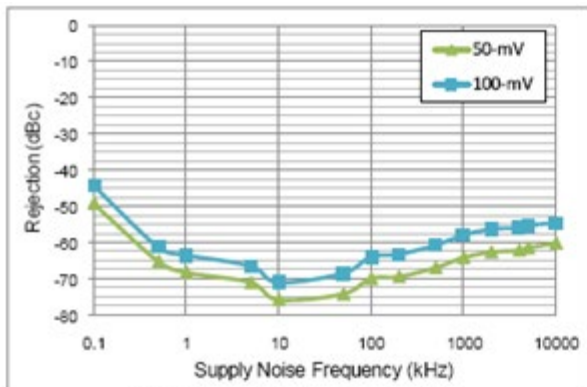


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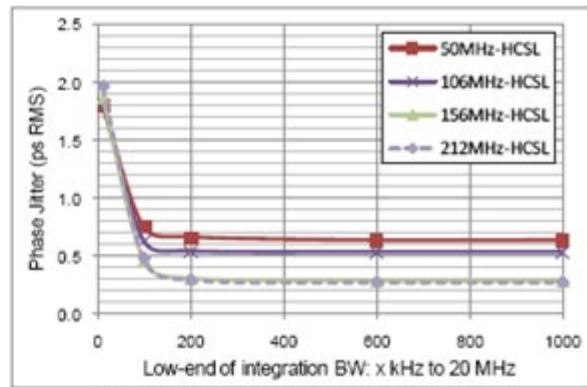


5.0 x 3.2 x 0.85 mm
RoHS/RoHS II Compliant
MSL Level = 1

HCSL output

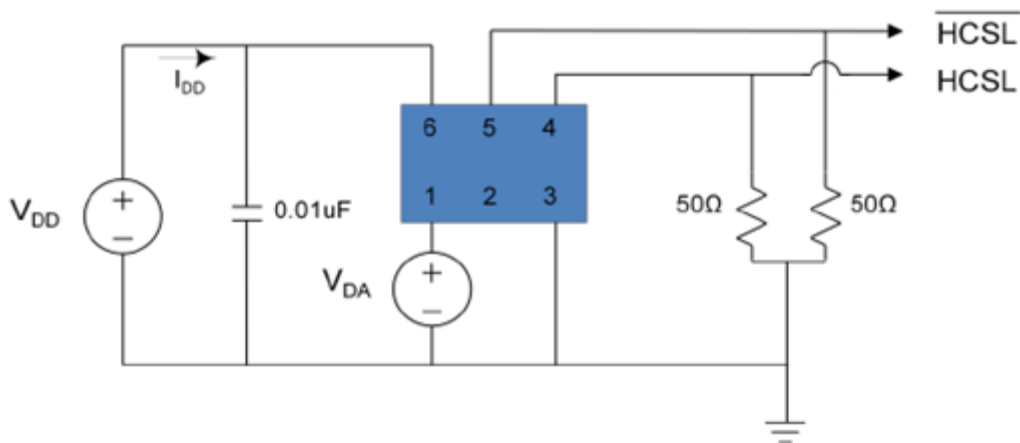


Power supply rejection ratio



Phase jitter (integrated phase noise)

Test Circuit



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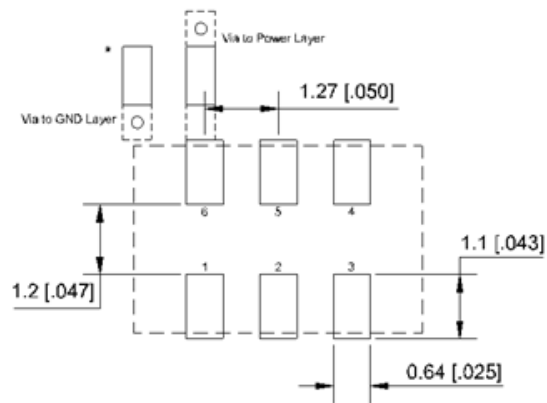
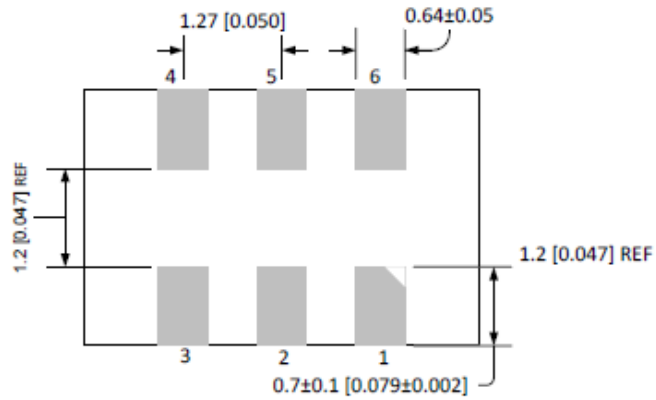
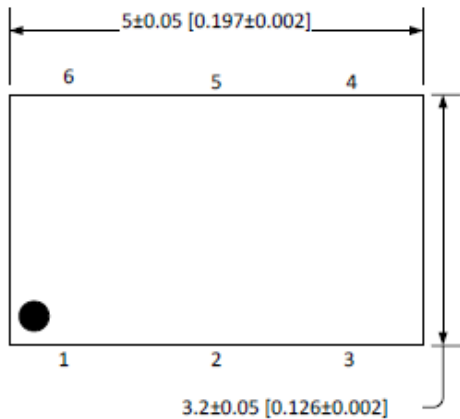


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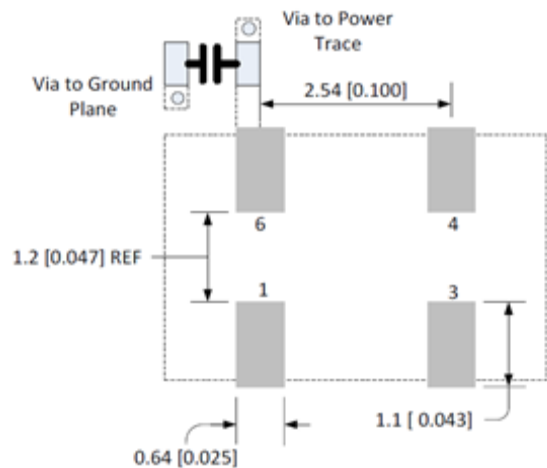
5.0 x 3.2 x 0.85 mm
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MSL Level = 1

Mechanical Dimensions



Recommended Land Pattern for LVPECL, LVDS, HCSL

Pin #	Function
1	Tri-state
2	NC
3	GND
4	Output
5	NC (CMOS) Output (LVPECL, LVDS, CSL)
6	Vdd



recommended Land Pattern for CMOS

Note: Recommend using an approximately 0.01uF bypass capacitor between PIN 6 and 3

Dimensions: mm (inches)



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Reflow Profile [JEDEC J-STD-020]

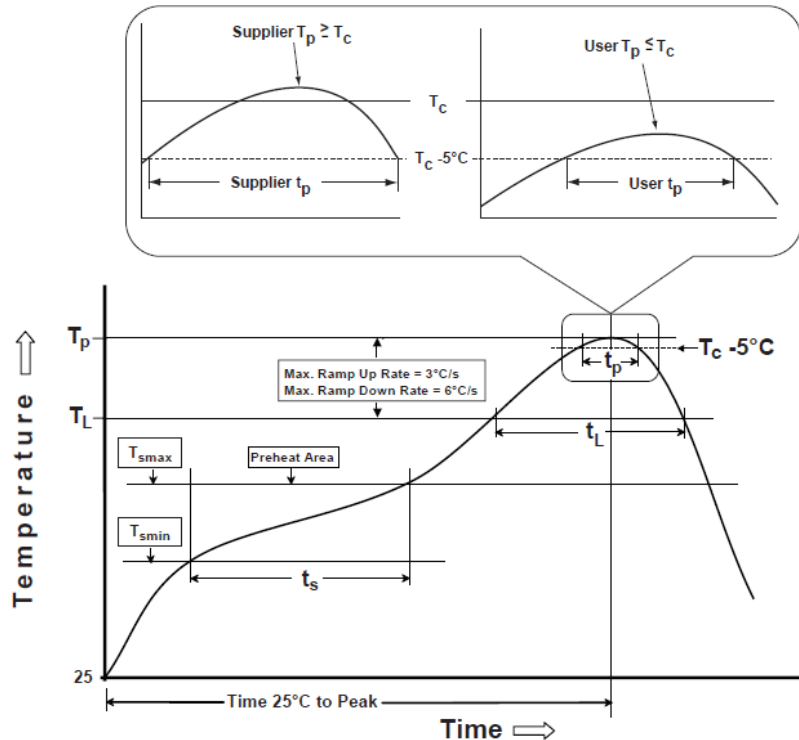


Table 1

SnPb Eutectic Process Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2

Pb-Free Process Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat / soak		
Temperature minimum (T_{smin})	100°C	150°C
Temperature maximum (T_{smax})	150°C	200°C
Time (T_{smin} to T_{smax}) (t_s)	60 - 120 sec.	60 - 120 sec.
Average ramp-up rate (T_{smax} to T_p)	3°C/sec. max	3°C/sec. max
Liquidous temperature (T_L)	183°C	217°C
Time at liquidous (t_L)	60 - 150 sec.	60 - 150 sec.
Peak package body temperature (T_p)*	see Table 1	see Table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20 sec.	30 sec.
Ramp-down rate (T_p to T_{smax})	6°C/sec. max	6°C/sec. max
Time 25°C to peak temperature	6 min. max	8 min. max
Reflow cycles	2 max	2 max

*Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

**Tolerance for time at peak profile temperature (t_p) is defined as supplier minimum and a user maximum.



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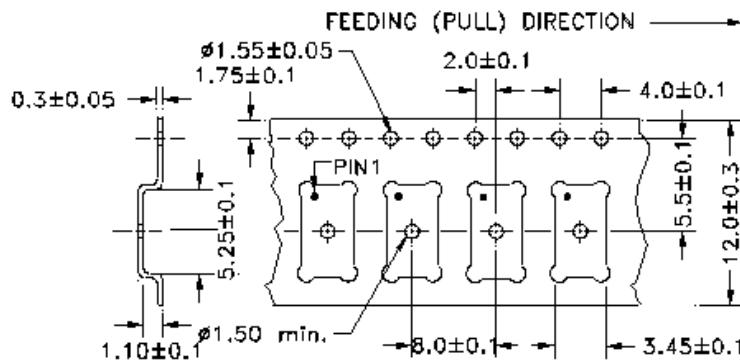


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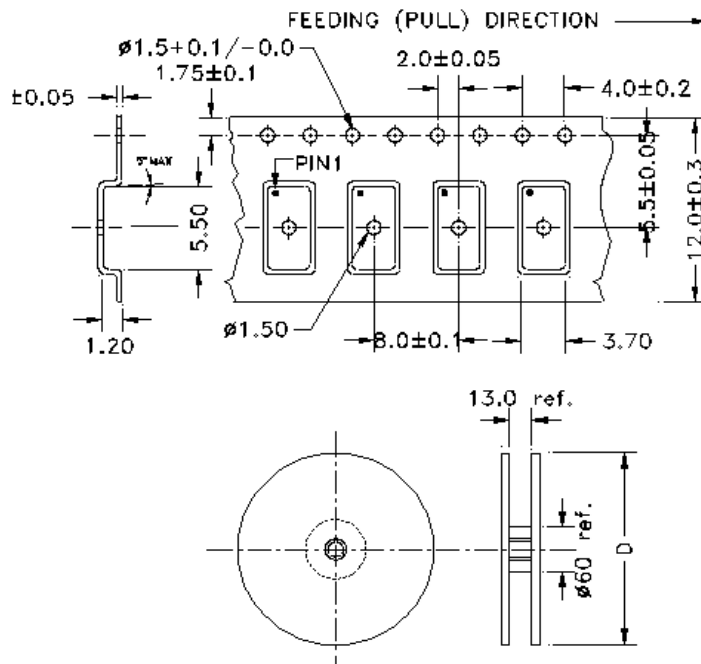
Packaging

T= 1,000pcs/reel (D=180mm)

Tape 1



Tape 2



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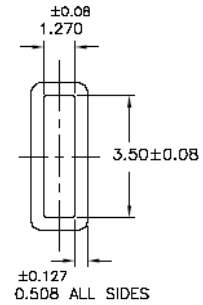
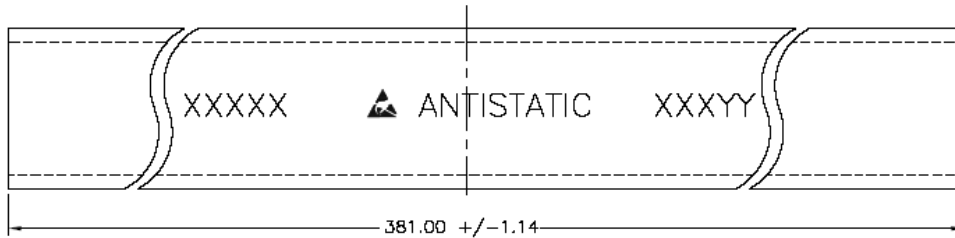


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Tube: 72 pcs/tube



Unit orientation in tube:



Dimensions: mm

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- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management