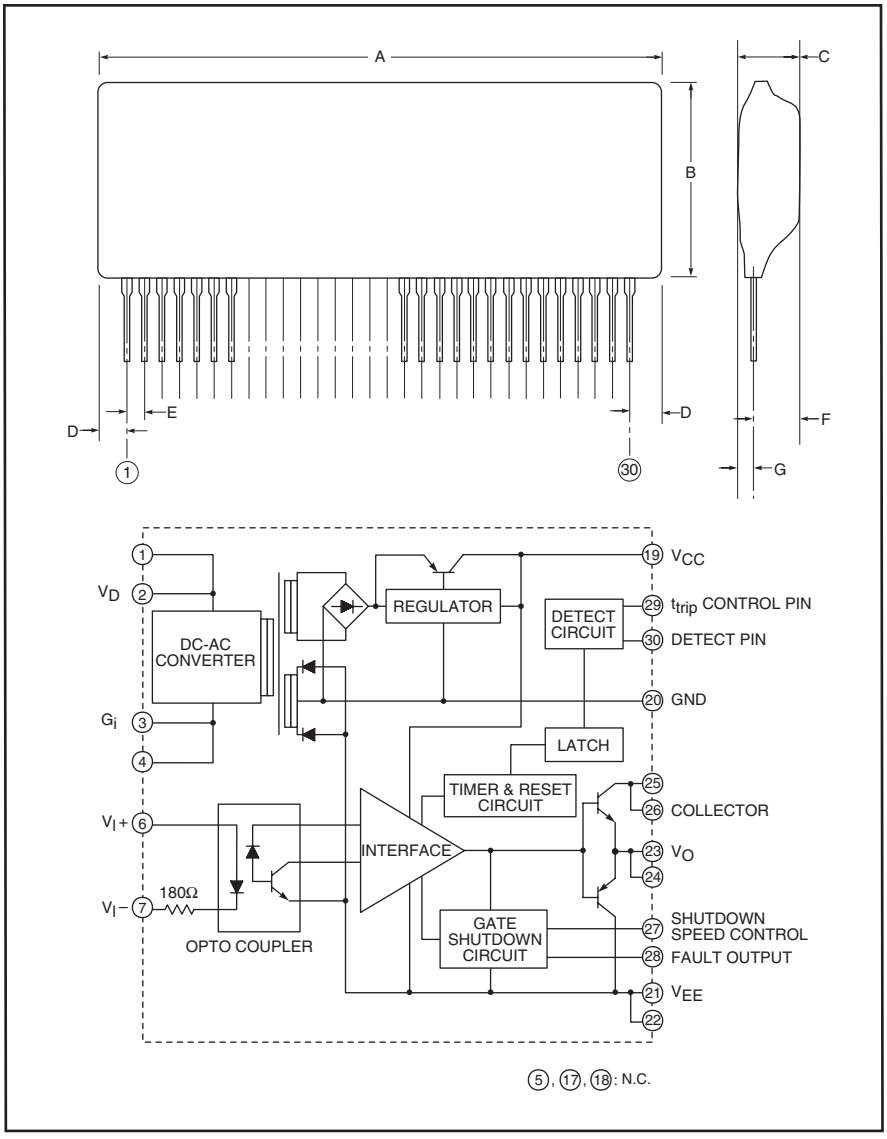
THE DATASHEET OF

VLA500K-01R

Powerex, Inc., 200 E. Hillis Street, Youngwood, Pennsylvania 15697-1800 (724) 925-7272

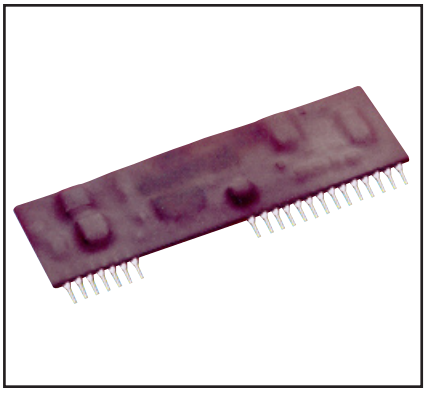
Hybrid IC
IGBT Gate Driver + DC/DC Converter



Outline Drawing and Circuit Diagram

Dimensions	Inches	Millimeters
A	3.27	83.0
B	1.3	33.0
C	0.67	17.0
D	0.2	5.0
E	0.1	2.54
F	0.45	11.5
G	0.24	6.0

Note: All dimensions listed are maximums except E.



Description:
VLA500K-01R is a hybrid integrated circuit designed for driving IGBT modules. This device is a fully isolated gate drive circuit consisting of an optimally isolated gate drive amplifier and an isolated DC-to-DC converter. The gate driver provides an over-current protection function based on desaturation detection.

Features:
- ☐ Built-in Isolated DC-to-DC Converter for Gate Drive
- ☐ SIP Outline Allows More Space on Mounting Area
- ☐ Built-in Short-Circuit Protection (With Fault Output)
- ☐ Variable Fall Time on Short-Circuit Protection
- ☐ Electrical Isolation Voltage Between Input and Output (4000 V_{rms} for 1 Minute)
- ☐ TTL Compatible Input

Application:
To drive IGBT modules for inverter or AC servo systems applications

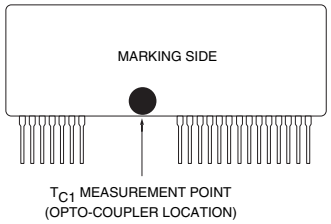
Recommended IGBT Modules:
600V module up to 600A
1200V module up to 1400A
1700V module up tp 1000A

VLA500K-01R
Hybrid IC IGBT Gate Driver +
DC/DC Converter

Absolute Maximum Ratings, T_a = 25°C unless otherwise specified

Characteristics	Symbol	VLA500K-01R	Units
Supply Voltage, DC	V_D	-1 ~ 16.5	Volts
Input Signal Voltage (Applied between Pin 6 - 7, 50% Duty Cycle, Pulse Width 1ms)	V_i	-1 ~ 7	Volts
Output Voltage (When the Output Voltage is "H")	V_O	V_{CC}	Volts
Output Current	I_{OHP}	-12	Amperes
(Pulse Width 2µs)	I_{OLP}	12	Amperes
Isolation Voltage (Sine Wave Voltage 60HZ, for 1 Minute, R.H. <60%)	V_{ISO}	4000	V_{rms}
Case Temperature1 (Surface Temperature Opto-coupler Location)***	T_{C1}	85	°C
Case Temperature2 (Surface Temperature Except Opto-coupler Location)	T_{C2}	100	°C
Operating Temperature (No Condensation Allowable)	T_{opr}	-20 to 60	°C
Storage Temperature (No Condensation Allowable)	T_{stg}	-25 to 100*	°C
Fault Output Current (Applied Pin 28)	I_{FO}	20	mA
Input Voltage to Pin 30 (Applied Pin 30)	V_{R30}	50	Volts
Gate Drive Current (Average)	I_{drive}	210**	mA

*Differs from temperature cycle condition.
**Refer to I_{drive} VS. T_a CHARACTERISTICS (TYPICAL) graph. (Needs Derating)
***T_{C1} Measurement Point (opto-coupler location)



Electrical and Mechanical Characteristics, T_a = 25°C unless otherwise specified, V_D = 15V, R_G = 2.2 Ω)

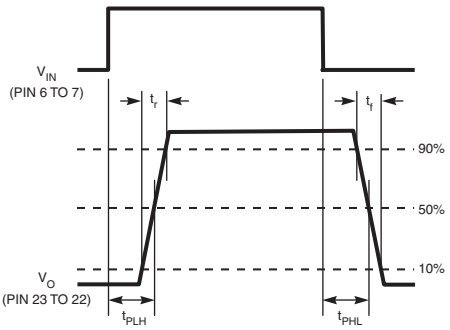
Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_D	Recommended Range	14.2	15	15.8	Volts
Pull-up Voltage on Input Side	V_{IN}	Recommended Range	4.75	5	5.25	Volts
"H" Input Current	I_{IH}	Recommended Range	15.2	16	19	mA
Switching Frequency	f	Recommended Range	—	—	20	kHz
Gate Resistance	R_G	Recommended Range	1	—	—	Ω
"H" Input Current	I_{IH}	V_{IN} = 5V	—	16	—	mA
Gate Positive Supply Voltage	V_{CC}	—	15.2	—	17.5	Volts
Gate Negative Supply Voltage	V_{EE}	—	-6	—	-11.5	Volts
Gate Supply Efficiency	E_{ta}	Load Current = 210mA	60	75	—	%
		$E_{ta} = (V_{CC} + \|V_{EE}\|) \times 0.21 / (15 \times I_D) \times 100$				
"H" Output Voltage	V_{OH}	10kΩ Connected Between Pin 23-20	14	15.3	16.5	Volts
"L" Output Voltage	V_{OL}	10kΩ Connected Between Pin 23-20	-5.5	—	-11	Volts
"L-H" Propagation Time	t_{PLH}	I_{IH} = 16mA	0.3	0.6	1	µs
"L-H" Rise Time	t_r	I_{IH} = 16mA	—	0.3	1	µs
"H-L" Propagation Time	t_{PHL}	I_{IH} = 16mA	0.6	1	1.3	µs
"H-L" Fall Time	t_f	I_{IH} = 16mA	—	0.3	1	µs

Electrical and Mechanical Characteristics, T_a = 25°C unless otherwise specified, V_D = 15V, R_G = 2.2 Ω)

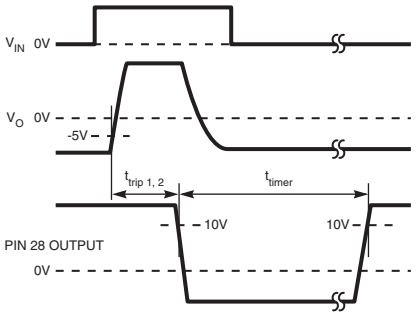
Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Timer	t_{timer}	Between Start and Cancel (Under Input Sign "L")	1	—	2	ms
Fault Output Current	I_{FO}	Applied Pin 28, R = 4.7kΩ	—	5	—	mA
Controlled Time Detect Short-Circuit 1	t_{trip1}	Pin 30 : 15V and More, Pin 29 : Open	—	2.8	—	µs
Controlled Time Detect Short-Circuit 2*	t_{trip2}	Pin 30 : 15V and More, Pin 29-21, 22 : 10pF (Connective Capacitance)	—	3.2	—	µs
SC Detect Voltage	V_{SC}	Collector Voltage of Module	15	—	—	Volts

*Length of wiring from C_{trip} to Pins 21, 22, and 29 must be less than 5cm.

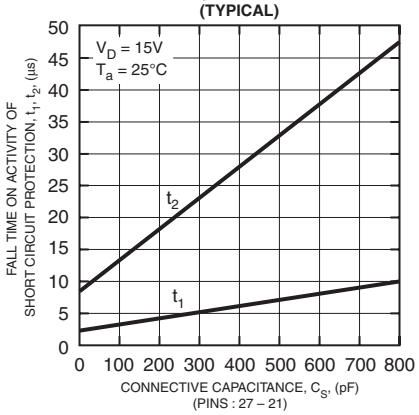
SWITCHING TIME DEFINITIONS



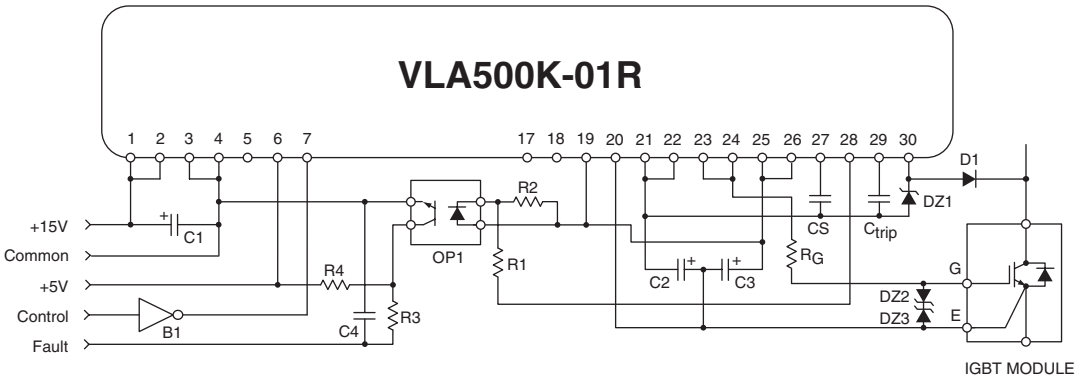
OPERATION OF SHORT CIRCUIT PROTECTION



t_1, t_2 VS. C_S CHARACTERISTICS (TYPICAL)



Application Circuit



Component Selection:

Design	Typical Value	Description
D1	0.5A	V_{CE} detection diode – fast recovery, $V_{rrm} > V_{CES}$ of IGBT being used (Note 1)
DZ1	30V, 0.5W	Detect input pin surge voltage protection (Note 2)
DZ2, DZ3	18V, 1.0W	Gate surge voltage protection
C1	100µF, 35V	V_D supply decoupling – Electrolytic, long life, low Impedance, 105°C (Note 3)
C2, C3	1mF, 35V	DC/DC output filter – Electrolytic, long life, low Impedance, 105°C (Note 3,4)
C4	0.01µF	Fault feedback signal noise filter
CS	0-1000pF	Adjust soft shutdown – Multilayer ceramic or film (see application note)
C_{trip}	0-200pF	Adjust trip time – Multilayer ceramic or film (see application note)
R1	4.7kΩ, 0.25W	Fault sink current limiting resistor
R2	3.3kΩ, 0.25W	Fault signal noise suppression resistor
R3	1kΩ, 0.25W	Fault feedback signal noise filter
R4	4.7kΩ, 0.25W	Fault feedback signal pull-up
OP1	NEC PS2501	Opto-coupler for fault feedback signal isolation
B1	CMOS Buffer	74HC04 or similar – Must actively pull high to maintain noise immunity

Notes:

(1) The V_{CE} detection diode should have a blocking voltage rating equal to or greater than the V_{CES} of the IGBT being driven. Recovery time should be less than 200ns to prevent application of high voltage to Pin 30.

(2) DZ1 is necessary to protect Pin 30 of the driver from voltage surges during the recovery of D1.

(3) Power supply input and output decoupling capacitors should be connected as close as possible to the pins of the gate driver.

(4) DC-to-DC converter output decoupling capacitors must be sized to have appropriate ESR and ripple current capability for the IGBT being driven.

General Description

The VLA500K-01R is a hybrid integrated circuit designed to provide gate drive for high power IGBT modules. This circuit has been optimized for use with Powerex NF-Series and A-Series IGBT modules. However, the output characteristics are compatible with most MOS gated power devices. The VLA500K-01R features a compact single-in-line package design. The upright mounting minimizes required printed circuit board space to allow efficient and flexible layout. The VLA500K-01R converts logic level control signals into fully isolated +15V/-8V gate drive with up to 12A of peak drive current. Isolated drive power is provided by a built in DC-to-DC converter and control signal isolation is provided by an integrated high speed opto-coupler. Short circuit protection is provided by means of destauration detection.

Short Circuit Protection

Figure 1 shows a block diagram of a typical desaturation detector. In this circuit, a high voltage fast recovery diode (D1) is connected to the IGBT's collector to monitor the collector to emitter voltage. When the IGBT is in the off state, V_{CE} is high and D1 is reverse biased. With D1 off the (+) input of the comparator is pulled up to the positive gate drive power supply (V+) which is normally +15V. When the IGBT turns on, the comparators (+) input is pulled down by D1 to the IGBT's $V_{CE(sat)}$. The (-) input of the comparator is supplied with a fixed voltage (V_{trip}). During a normal on-state condition the comparator's (+) input will be less than V_{trip} and it's output will be low. During a normal off-state condition the comparator's (+) input will be larger than V_{trip} and it's output will be high. If the IGBT turns on into a short circuit, the high current will cause the IGBT's collector-emitter voltage to rise above V_{trip} even though the gate of the IGBT is being driven on. This abnormal presence of high V_{CE} when the IGBT is supposed to be on is often called ***desaturation***. Desaturation can be detected by a logical AND of the driver's input signal and the comparator output. When the output of the AND goes high a short circuit is indicated. The output of the AND can be used to command the IGBT to shut down in order to protect it from the short circuit. A delay (t_{trip}) must be provided after the comparator output to allow for the normal turn on time of the IGBT. The t_{trip} delay is set so that the IGBT's V_{CE} has enough time to fall below V_{trip} during normal turn on switching. If t_{trip} is set too short, erroneous desaturation detection will occur. The maximum allowable t_{trip} delay is limited by the IGBT's short circuit withstanding capability. In typical applications using Powerex IGBT modules the recommended limit is 10µs.

Operation of the VLA500K-01R Desaturation Detector

The Powerex VLA500K-01R incorporates short circuit protection using desaturation detection as described above. A flow chart for the logical operation of the short-circuit protection is shown in Figure 2. When a desaturation is detected the hybrid gate driver performs a soft shutdown of the IGBT and starts a timed (t_{timer}) 1.5ms lock out. The soft turn-off helps to limit the transient voltage that may be generated while interrupting the large short circuit current flowing in the IGBT. During the lock out the driver pulls Pin 28 low to indicate the fault status. Normal operation of the driver will resume after the lock-out time has expired and the control input signal returns to its off state.

Adjustment of Trip Time

The VLA500K-01R has a default short-circuit detection time delay (t_{trip}) of approximately 3µs. This will prevent erroneous detection of short-circuit conditions as long as the series gate resistance (R_G) is near the minimum recommended value for the module being used. The 3µs delay is appropriate for most applications so adjustment will not be necessary. However, in some low frequency applications it may be desirable to use a

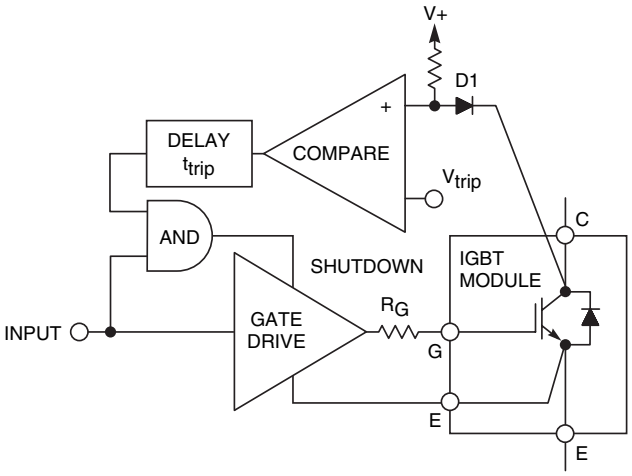


Figure 1. Desaturation Detector

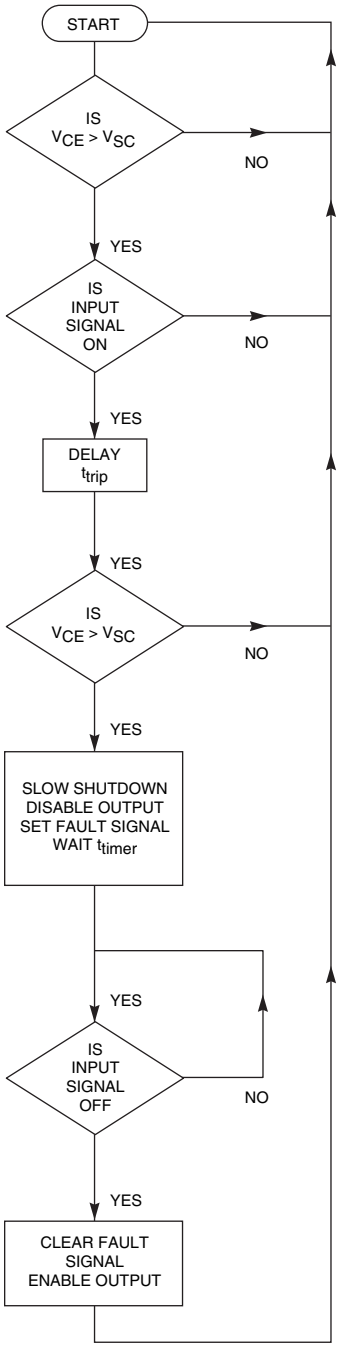


Figure 2. VLA500K-01R Desaturation Detector

larger series gate resistor to slow the switching of the IGBT, reduce noise, and limit turn-off transient voltages. When R_G is increased, the switching delay time of the IGBT will also increase. If the delay becomes long enough so that the voltage on the detect Pin 30 is greater than V_{SC} at the end of the t_{trip} delay the driver will erroneously indicate that a short circuit has occurred. To avoid this condition the VLA500K-01R has provisions for extending the t_{trip} delay by connecting a capacitor (C_{trip}) between Pin 29 and V_{EE} (Pins 21 and 22). A curve showing the effect of adding C_{trip} on time is given in the characteristic data section of this data sheet. The waveform defining trip time (t_{trip}) is shown in Figure 3. If t_{trip} is extended care must be exercised not to exceed the short-circuit withstanding capability of the IGBT module. Normally this will be satisfied for Powerex NF and A-Series IGBT modules as long as the total shut-down time does not exceed 10µs.

Adjustment of Soft Shutdown Speed

As noted above the VLA500K-01R provides a soft turn-off when a short circuit is detected in order to help limit the transient voltage surge that occurs when large short circuit currents are interrupted. The default shutdown speed will work for most applications so adjustment is usually not necessary. In this case C_S can be omitted. In some applications using large modules or parallel connected devices it may be helpful to make the shutdown even softer. This can be accomplished by connecting a capacitor (C_S) at Pin 27. A curve showing the effect of C_S on short circuit fall time (t_1, t_2) is given in the characteristic data section of this data sheet. The waveform defining the fall time characteristics is shown in Figure 3.

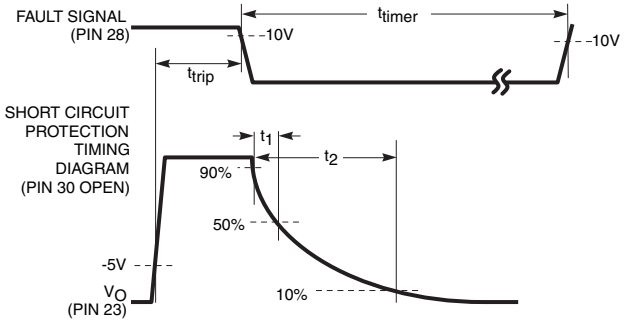


Figure 3. Adjustment of t_{trip} and Slow Shutdown Speed

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