THE DATASHEET OF

BUK7V4R2-40HX

BUK7V4R2-40H

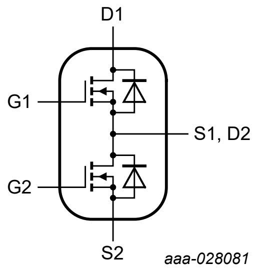
Dual N-channel 40 V, 4.2 mOhm standard level MOSFET in LFPAK56D (half-bridge configuration)

9 May 2023 — Product data sheet

1. General description

Dual, standard level N-channel MOSFET in an LFPAK56D package (half-bridge configuration), using Trench 9 TrenchMOS technology. This product has been designed and qualified to AEC-Q101.

An internal connection is made between the source (S1) of the high-side FET to the drain (D2) of the low-side FET, making the device ideal to use as a half-bridge switch in high-performance automotive PWM applications.



2. Features and benefits

- LFPAK56D package with half-bridge configuration enables:
  - Reduced PCB layout complexity
  - PCB shrinkage through reduced component footprint for 3-phase motor drive
  - Improved system level $R_{th(j-amb)}$ due to optimized package design
  - Lower parasitic inductance to support higher efficiency
  - Footprint compatibility with LFPAK56D Dual package
- Advanced AEC-Q101 grade Trench 9 silicon technology:
  - Low power losses, high power density
  - Superior avalanche performance
  - Repetitive avalanche rated
- LFPAK copper clip packaging provides high robustness and reliability
- Gull wing leads support high manufacturability and Automated Optical Inspection (AOI)

3. Applications

- 12 V automotive systems
- Powertrain, chassis, body and infotainment applications
- Brushless or brushed DC motor drive
- DC-to-DC systems
- LED lighting

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Limiting values FET1 and FET2							
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	40	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	-	98	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	85	W

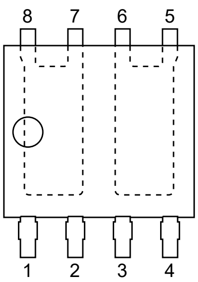
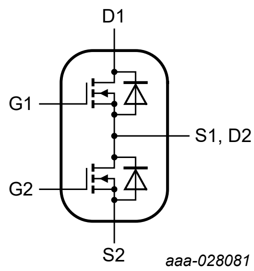
nexperia

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics FET1 and FET2							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A; T_j = 25 °C; Fig. 11		2.5	3.5	4.2	mΩ
Dynamic characteristics FET1 and FET2							
Q_{GD}	gate-drain charge	I_D = 20 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 13; Fig. 14		-	4.7	9.4	nC

[1] 98A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S2	source2		
2	G2	gate2		
3	S1, D2	source1, drain2		
4	G1	gate1		
5	D1	drain1		
6	D1	drain1		
7	S1, D2	source1, drain2		
8	S1, D2	source1, drain2	**LFPAK56D; Dual LFPAK (SOT1205)**	

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7V4R2-40H	LFPAK56D; Dual LFPAK	plastic, single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7V4R2-40H	`74V240H`

8. Limiting values

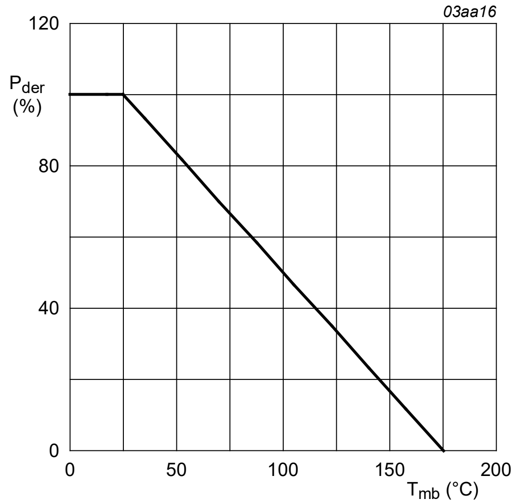
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Limiting values FET1 and FET2						
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	40	V
V_{GS}	gate-source voltage	DC; T_j = 25 °C		-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	85	W

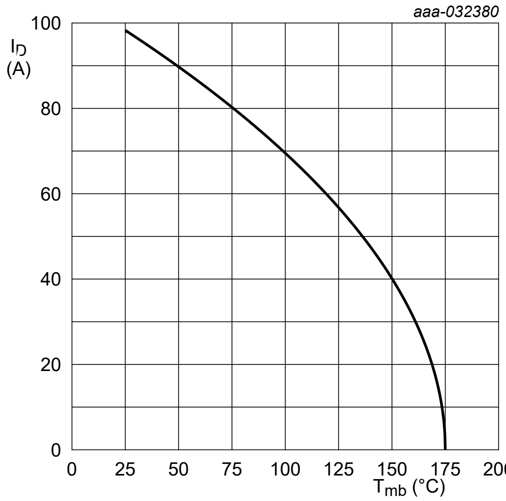
Symbol	Parameter	Conditions		Min	Max	Unit
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	98	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	69.5	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	393	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode FET1 and FET2						
I_S	source current	T_{mb} = 25 °C		-	85	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	393	A
Avalanche ruggedness FET1 and FET2						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 82.6 A; V_{sup} ≤ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4	[2] [3]	-	42.3	mJ
I_{AS}	non-repetitive avalanche current	V_{sup} = 40 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω	[4]	-	82.6	A

[1] 98A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[3] Refer to application note AN10273 for further information.
[4] Protected by 100% test



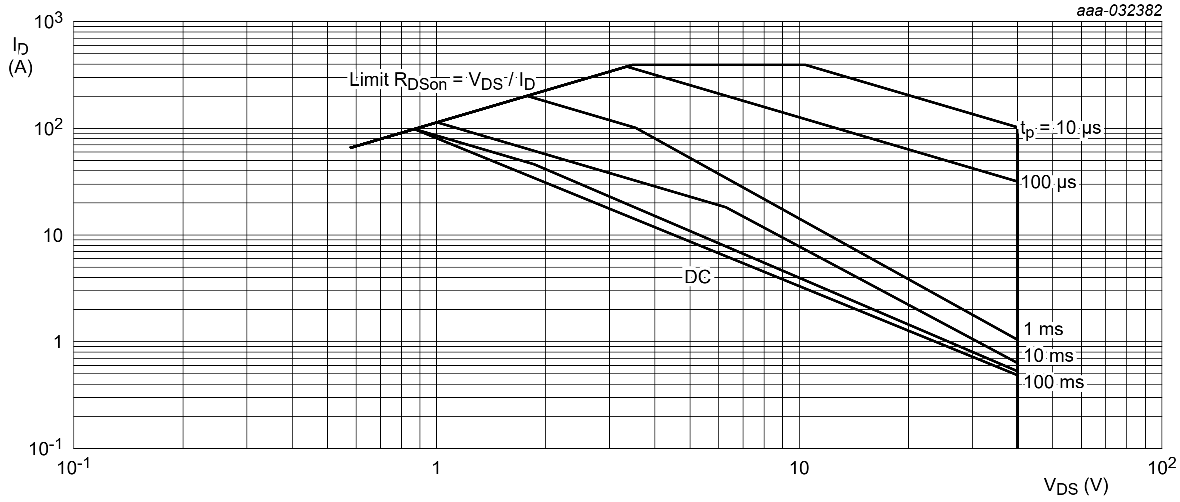
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



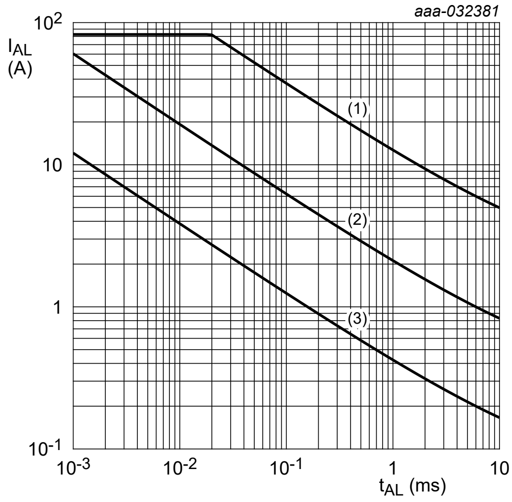
V_{GS} ≥ 10 V
(1) 98A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature, FET1 and FET2



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage, FET1 and FET2



(1) $T_{j\,(init)}$ = 25 °C; (2) $T_{j\,(init)}$ = 150 °C; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	1.64	1.76	K/W

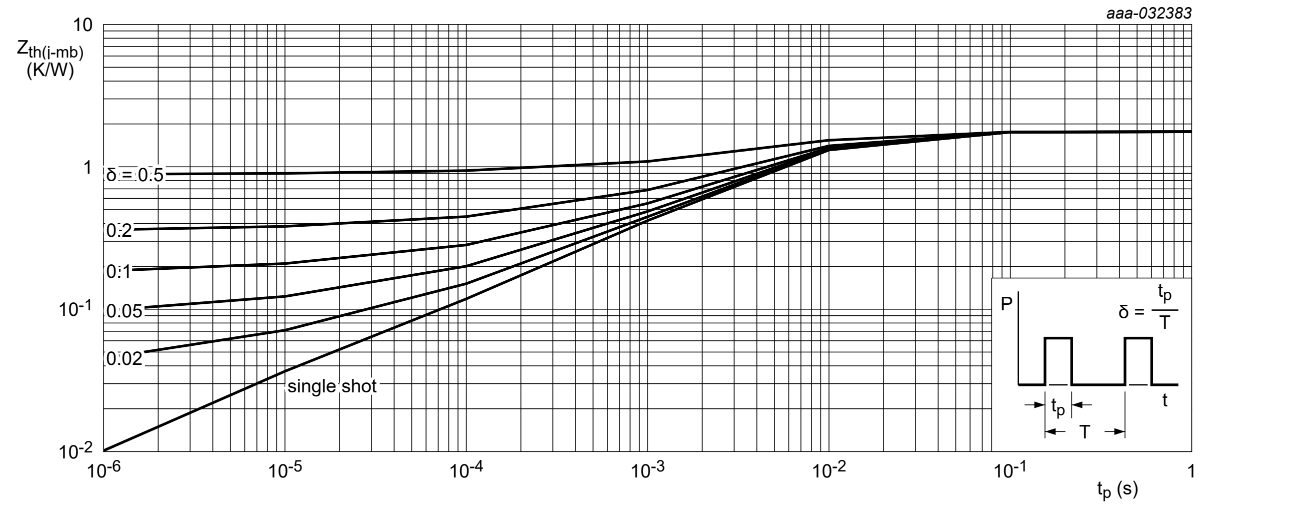


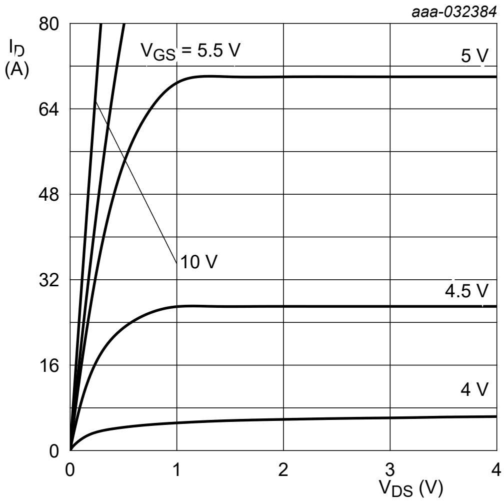
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration, FET1 and FET2

10. Characteristics

Table 7. Characteristics

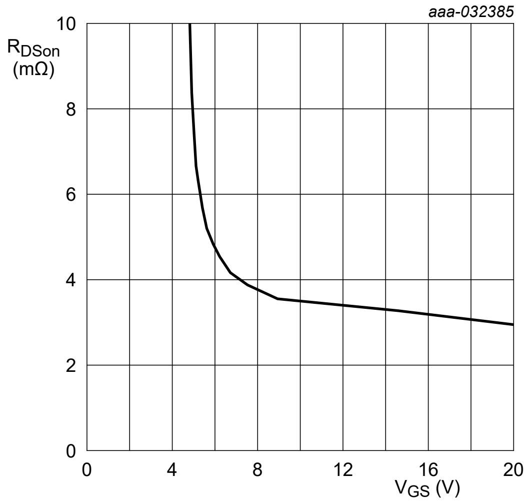
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics FET1 and FET2							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		40	43	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -40 °C		-	40.5	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		36	40	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 9; Fig. 10		2.4	3	3.6	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C; Fig. 10		1	-	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C; Fig. 10		-	-	4.3	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C		-	0.007	1	µA
		V_{DS} = 16 V; V_{GS} = 0 V; T_j = 125 °C		-	0.3	10	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C		-	53	500	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A; T_j = 25 °C; Fig. 11		2.5	3.5	4.2	mΩ
		V_{GS} = 10 V; I_D = 20 A; T_j = 105 °C; Fig. 12		3.4	5.2	6.4	mΩ
		V_{GS} = 10 V; I_D = 20 A; T_j = 125 °C; Fig. 12		3.7	5.8	7.2	mΩ
		V_{GS} = 10 V; I_D = 20 A; T_j = 175 °C; Fig. 12		4.5	7.2	8.8	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		0.72	1.8	4.5	Ω
Dynamic characteristics FET1 and FET2							
$Q_{G(tot)}$	total gate charge	I_D = 20 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 13; Fig. 14		-	26	37	nC
Q_{GS}	gate-source charge			-	7.8	12	nC
Q_{GD}	gate-drain charge			-	4.7	9.4	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 15		-	1850	2590	pF
C_{oss}	output capacitance			-	565	791	pF
C_{rss}	reverse transfer capacitance			-	91	200	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.5 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	7	-	ns
t_r	rise time			-	9	-	ns
$t_{d(off)}$	turn-off delay time			-	19	-	ns
t_f	fall time			-	11.8	-	ns
Source-drain diode FET1 and FET2							
V_{SD}	source-drain voltage	I_S = 20 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 16		-	0.81	1	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C		-	18.6	-	ns
Q_r	recovered charge			-	9.2	-	nC



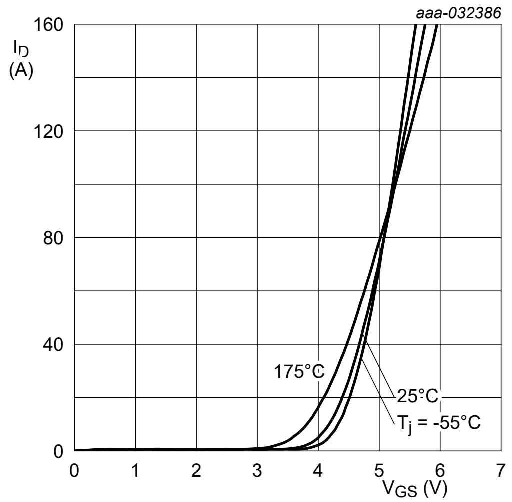
T_j = 25 °C

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values, FET1 and FET2



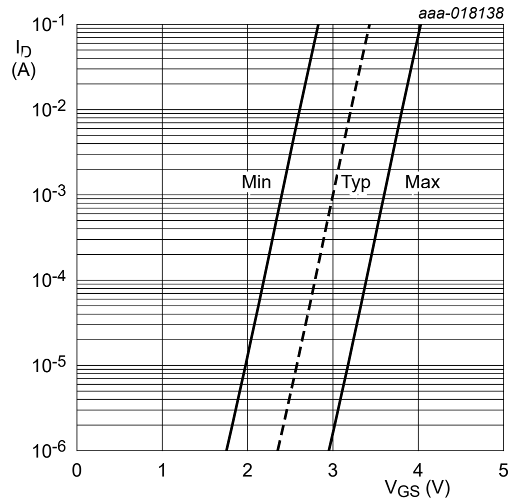
T_j = 25 °C; I_D = 20 A

Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values, FET1 and FET2



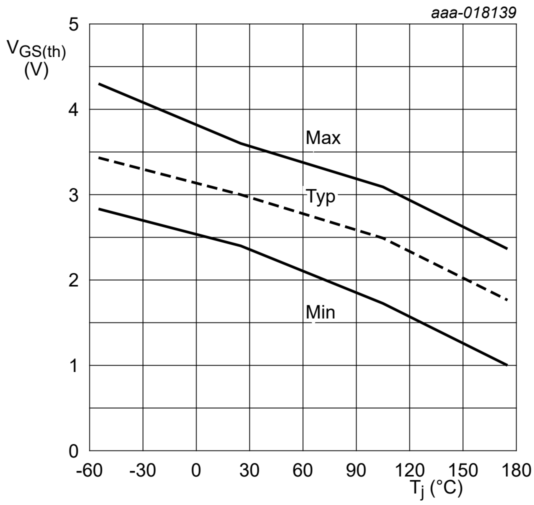
V_{DS} = 8 V

Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values, FET1 and FET2



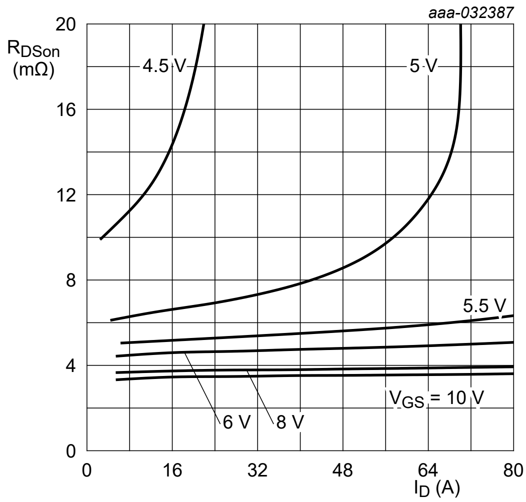
T_j = 25 °C; V_{DS} = 5 V

Fig. 9. Sub-threshold drain current as a function of gate-source voltage, FET1 and FET2



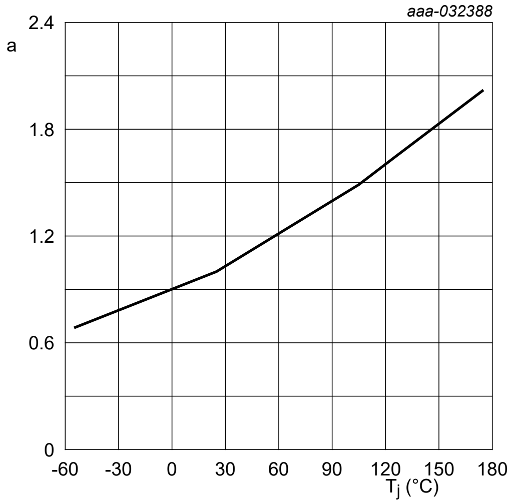
I_D = 1 mA ; V_{DS} = V_{GS}

Fig. 10. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2



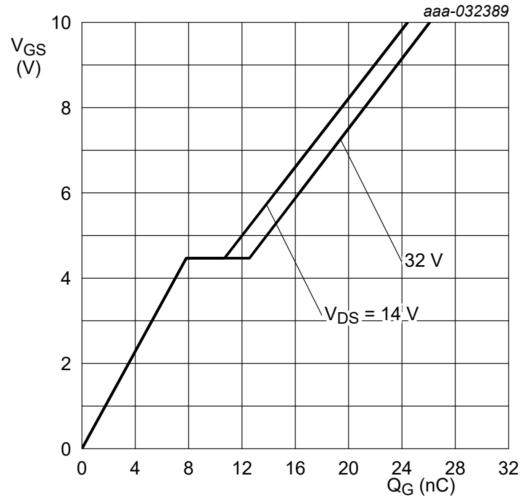
T_j = 25 °C

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values, FET1 and FET2



$$a = \frac{R_{DSon}}{R_{DSon\,(25°C)}}$$

Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature, FET1 and FET2



T_j = 25 °C; I_D = 20 A

Fig. 13. Gate-source voltage as a function of gate charge; typical values, FET1 and FET2

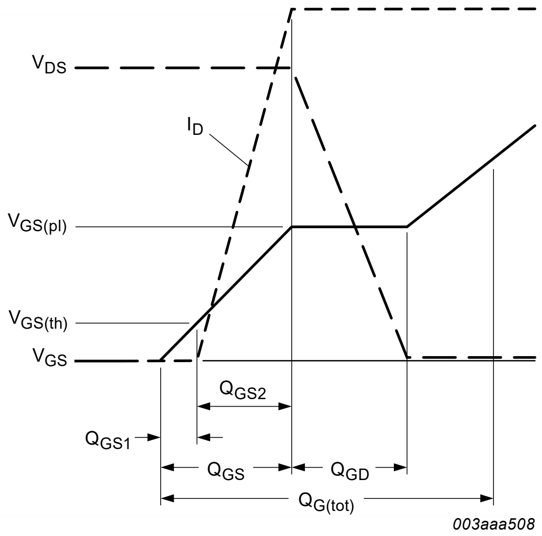
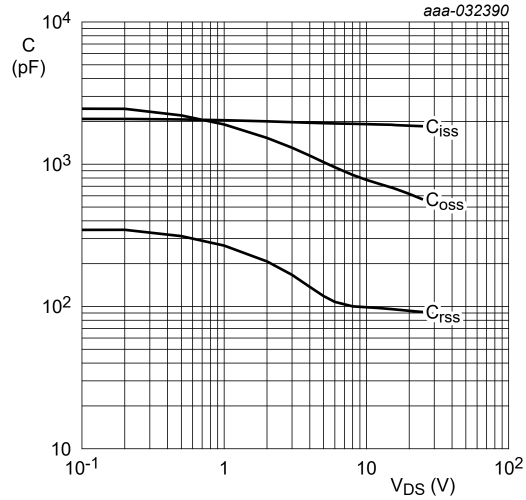
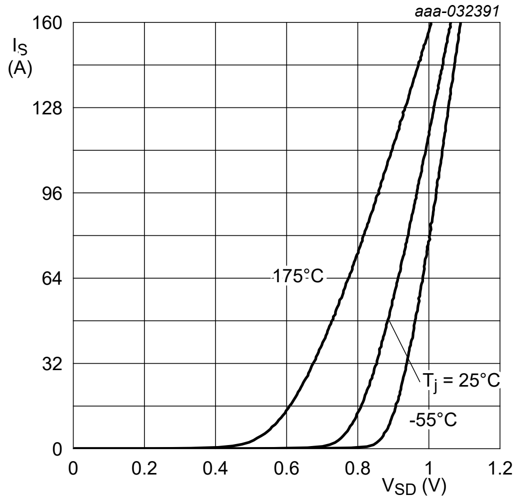


Fig. 14. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2

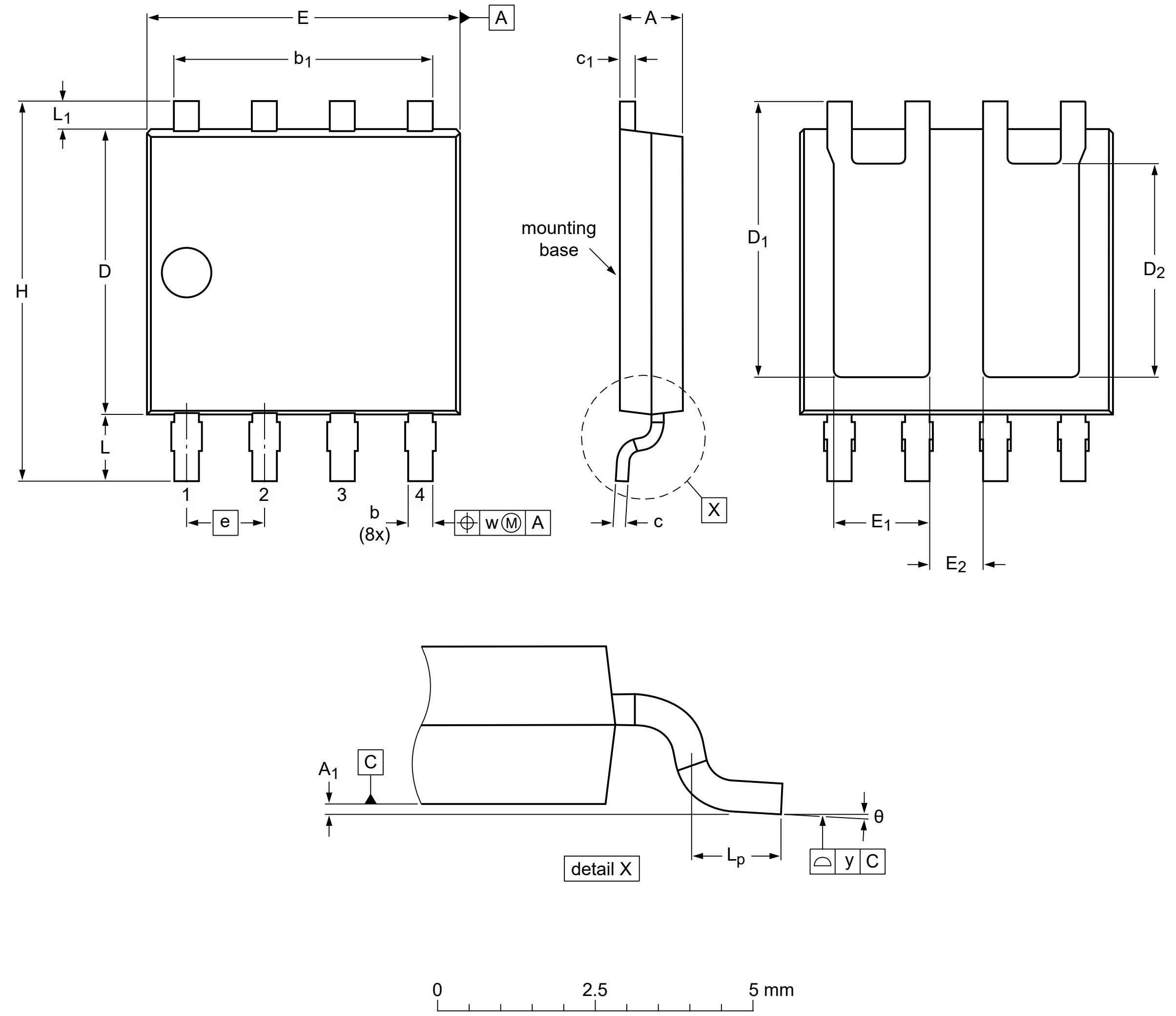


V_{GS} = 0 V

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET1 and FET2

11. Package outline

Plastic single ended surface mounted package LFPAK56D; 8 leads **SOT1205**



Dimensions

Unit		A	A_1	b	b_1	c	c_1	D(1)	D_1(1)	D_2 (ref)	E(1)	E_1(1)	E_2	e	H	L	L_1	L_p	w	y	θ
mm	max	1.05	0.1	0.50	4.4	0.25	0.30	4.70	4.55	3.5	5.30	1.8	0.85		6.2	1.3	0.55	0.85			8°
	nom													1.27					0.25	0.1	
	min	1.02	0.0	0.35	4.1	0.19	0.24	4.45	4.35	3.4	4.95	1.6	0.60		5.9	0.8	0.30	0.40			0°

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot1205_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1205						~~14-08-21~~ 14-10-28

Fig. 17. Package outline LFPAK56D; Dual LFPAK (SOT1205)

12. Soldering

Footprint information for reflow soldering of LFPAK56D package **SOT1205**

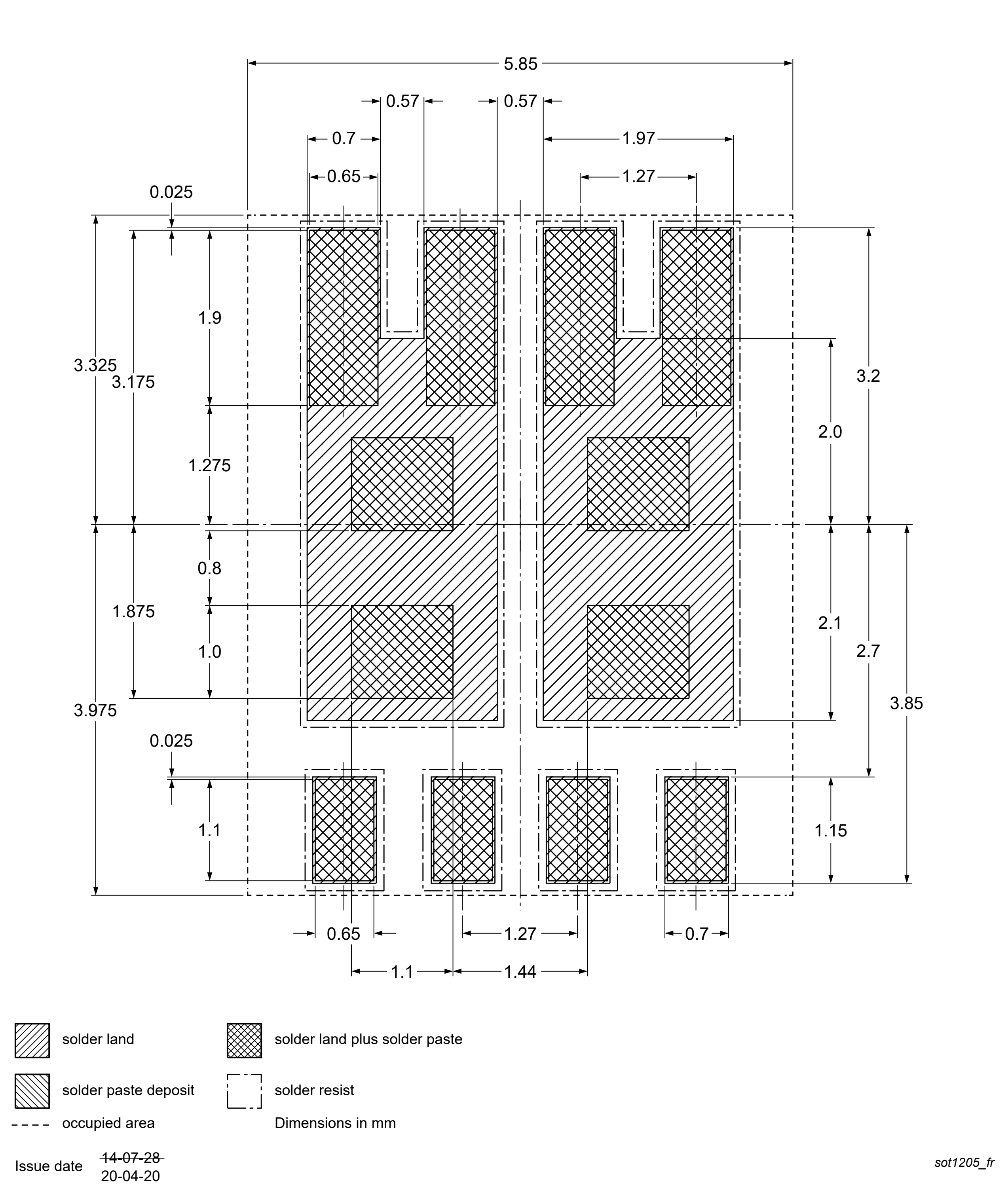


Fig. 18. Reflow soldering footprint for LFPAK56D; Dual LFPAK (SOT1205)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Contents

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