



**THE DATASHEET OF
CY96F386RSCPMC-GS188UJE2**



F²MC-16FX 16-bit Proprietary Microcontroller

CY96380 series is based on Cypress advanced 16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established 16LX series - thus allowing for easy migration of 16LX Software to the new 16FX products. 16FX improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time.

For highest processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 56MHz operation frequency from an external 4MHz resonator. The result is a minimum instruction cycle time of 17.8ns going together with excellent EMI behavior. An on-chip clock modulation circuit significantly reduces emission peaks in the frequency spectrum. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows to select suitable operation frequencies for peripheral resources independent of the CPU speed.

Features

Technology

- 0.18 μ m CMOS

CPU

- F²MC-16FX CPU
- Up to 56 MHz internal, 17.8 ns instruction cycle time
- Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers)
- 8-byte instruction execution queue
- Signed multiply (16-bit \cdot 16-bit) and divide (32-bit/16-bit) instructions available

System Clock

- On-chip PLL clock multiplier (x1 - x25, x1 when PLL stop)
- 3 MHz - 16 MHz external crystal oscillator clock (maximum frequency when using ceramic resonator depends on Q-factor).
- Up to 56 MHz external clock for devices with fast clock input feature
- 32-100 kHz subsystem quartz clock
- 100 kHz/2 MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog
- Clock source selectable from main- and subclock oscillator (part number suffix "W") and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals.
- Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode)
- Clock modulator

On-chip Voltage Regulator

- Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures

Low Voltage Reset

- Reset is generated when supply voltage is below minimum.

Code Security

- Protects ROM content from unintended read-out

Memory Patch Function

- Replaces ROM content
- Can also be used to implement embedded debug support

DMA

- Automatic transfer function independent of CPU, can be assigned freely to resources

Interrupts

- Fast Interrupt processing
- 8 programmable priority levels
- Non-Maskable Interrupt (NMI)

Timers

- Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)
- Watchdog Timer

CAN

- Supports CAN protocol version 2.0 part A and B
- ISO16845 certified
- Bit rates up to 1 Mbit/s
- 32 message objects
- Each message object has its own identifier mask
- Programmable FIFO mode (concatenation of message objects)
- Maskable interrupt
- Disabled Automatic Retransmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation

USART

- Full duplex USARTs (SCI/LIN)
- Wide range of baud rate settings using a dedicated reload timer
- Special synchronous options for adapting to different synchronous serial protocols
- LIN functionality working either as master or slave LIN device

I²C

- Up to 400 kbps
- Master and Slave functionality, 8-bit and 10-bit addressing

A/D Converter

- SAR-type
- 10-bit resolution
- Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger or reload timer

A/D Converter Reference Voltage switch

- 2 independent positive A/D converter reference voltages available

Reload Timers

- 16-bit wide
- Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
- Event count function

Free Running Timers

- Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4), Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency

Input Capture Units

- 16-bit wide
- Signals an interrupt upon external event
- Rising edge, falling edge or rising & falling edge sensitive

Output Compare Units

- 16-bit wide
- Signals an interrupt when a match with 16-bit I/O Timer occurs
- A pair of compare registers can be used to generate an output signal.

Programmable Pulse Generator

- 16-bit down counter, cycle and duty setting registers
- Interrupt at trigger, counter borrow and/or duty match
- PWM operation and one-shot operation
- Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock and Reload timer overflow as clock input
- Can be triggered by software or reload timer

Stepper Motor Controller

- Stepper Motor Controller with integrated high current output drivers
- Four high current outputs for each channel
- Two synchronized 8/10-bit PWMs per channel
- Internal prescaling for PWM clock: 1, 1/4, 1/5, 1/6, 1/8, 1/10, 1/12, 1/16 of peripheral clock
- Separate power supply for high current output drivers

LCD Controller

- LCD controller with up to 4 COM × 65 SEG
- Internal or external voltage generation
- Duty cycle: Selectable from options: 1/2, 1/3 and 1/4
- Fixed 1/3 bias
- Programmable frame period
- Clock source selectable from three options (peripheral clock, subclock or RC oscillator clock)
- On-chip drivers for internal divider resistors or external divider resistors
- On-chip data memory for display
- LCD display can be operated in Timer Mode
- Blank display: selectable
- All SEG, COM and V pins can be switched between general and specialized purposes
- External divided resistors can be also used to shut off the current when LCD is deactivated

Sound Generator

- 8-bit PWM signal is mixed with tone frequency from 16-bit reload counter
- PWM clock by internal prescaler: 1, 1/2, 1/4, 1/8 of peripheral clock

Real Time Clock

- Can be clocked either from sub oscillator (devices with part number suffix "W"), main oscillator or from the RC oscillator
- Facility to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
- Read/write accessible second/minute/hour registers
- Can signal interrupts every half second/second/minute/hour/day
- Internal clock divider and prescaler provide exact 1s clock

External Interrupts

- Edge sensitive or level sensitive
- Interrupt mask and pending bit per channel
- Each available CAN channel RX has an external interrupt for wake-up
- Selected USART channels SIN have an external interrupt for wake-up

Non Maskable Interrupt

- Disabled after reset
- Once enabled, can not be disabled other than by reset.
- Level high or level low sensitive
- Pin shared with external interrupt 0.

External Bus Interface

- 8-bit or 16-bit bidirectional data
- Up to 24-bit addresses
- 6 chip select signals
- Multiplexed address/data lines
- Non-multiplexed address/data lines
- Wait state request
- External bus master possible
- Timing programmable

Alarm Comparator

- Monitors an external voltage and generates an interrupt in case of a voltage lower or higher than the defined thresholds
- Threshold voltages defined externally or generated internally
- Status is readable, interrupts can be masked separately

I/O Ports

- Virtually all external pins can be used as general purpose I/O
- All push-pull outputs (except when used as I2C SDA/SCL line)
- Bit-wise programmable as input/output or peripheral signal
- Bit-wise programmable input enable
- Bit-wise programmable input levels: Automotive / CMOS-Schmitt trigger / TTL
- Bit-wise programmable pull-up resistor
- Bit-wise programmable output driving strength for EMI optimization

Package

- 120-pin plastic LQFP

Flash Memory

- Supports automatic programming, Embedded Algorithm
- Write/Erase/Erase-Suspend/Resume commands
- A flag indicating completion of the algorithm
- Number of erase cycles: 10,000 times
- Data retention time: 20 years
- Erase can be performed on each sector individually
- Sector protection
- Flash Security feature to protect the content of the Flash
- Low voltage detection during Flash erase

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Turn on sequence of power supply to			

1. Product Lineup

Features		CY96V300B	CY96(F)38x
Product type		Evaluation sample	Flash product: CY96F38x Mask ROM product: CY9638x
Product options			
YS		NA	Low voltage reset persistently on / Single clock
RS			Low voltage reset can be disabled / Single clock
YW			Low voltage reset persistently on / Dual clock
RW			Low voltage reset can be disabled / Dual clock
TS			indep. 32 KB Flash / Low voltage reset persistently on / Single clock
HS			indep. 32 KB Flash / Low voltage reset can be disabled / Single clock
TW			indep. 32 KB Flash / Low voltage reset persistently on / Dual clock
HW			indep. 32 KB Flash / Low voltage reset can be disabled / Dual clock
Flash/ROM	RAM		
128 KB	6 KB	ROM/Flash memory emulation by external RAM, 92KB internal RAM	CY96384Y, CY96384R
160 KB	8 KB		CY96385Y, CY96385R, CY96F385Y, CY96F385R
288 KB	16 KB		CY96F386Y, CY96F386R
416 KB	16 KB		CY96F387Y, CY96F387R
576 KB [Flash A: 544 KB, Flash B: 32 KB]	28 KB		CY96F388T, CY96F388H
832 KB [Flash A: 544 KB, Flash B: 288 KB]	32 KB		CY96F389Y, CY96F389R
Package		BGA416	LQM120
DMA		16 channels	7 channels
USART		10 channels	5 channels
I ² C		2 channels	1 channel
A/D Converter		40 channels	16 channels
A/D Converter Reference Voltage switch		yes	Only for CY96F386Y, CY96F386R, CY96F387Y, CY96F387R
16-bit Reload Timer		6 channels + 1 channel (for PPG)	4 channels + 1 channel (for PPG)
16-bit Free-Running Timer		4 channels	2 channels
16-bit Output Compare		12 channels	4 channels

Features	CY96V300B	CY96(F)38x
16-bit Input Capture	12 channels	8 channels
16-bit Programmable Pulse Generator	20 channels	8 channels
CAN Interface	5 channels	Other than below: 2 channels CY96384Y, CY96384R, CY96(F)385Y, CY96(F)385R, : 1 channel
Stepping Motor Controller	6 channels	5 channels
External Interrupts	16 channels	8 channels
Non-Maskable Interrupt	1 channel	
Sound generator	2 channels	2 channels
LCD Controller	4 COM x 72 SEG	4 COM x 65 SEG
Real Time Clock	1	
I/O Ports	136	94 for part number with suffix "W", 96 for part number with suffix "S"
Alarm comparator	2 channels	Other than below: 2 channels CY96384Y, CY96384R, CY96(F)385Y, CY96(F)385R, : 1 channel
External bus interface	Yes	
Chip select	6 signals	
Clock output function	2 channels	
Low voltage reset	Yes	
On-chip RC-oscillator	Yes	

2. Block Diagram

Block Diagram of CY96(F)38x



3. Pin Assignment

Pin Assignment of CY96(F)38x



4. Pin Function Description

Pin Function Description (1 of 3)

Pin name	Feature	Description
ADn	External bus	External bus interface (non multiplexed mode) data input/output. External bus interface (multiplexed mode) address output and data input/output
ADTG	ADC	A/D converter trigger input
ALARMn	Alarm comparator	Alarm Comparator n input
ALE	External bus	External bus Address Latch Enable output
An	External bus	External bus non-multiplexed address output
ANn	ADC	A/D converter channel n input
AV _{CC}	Supply	Analog circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AVRH2	ADC	Alternative A/D converter high reference voltage input
AVRL	ADC	A/D converter low reference voltage input
AV _{SS}	Supply	Analog circuits power supply
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock output function	Clock Output function n output
CKOTn_R	Clock output function	Relocated Clock Output function n output
CKOTXn	Clock output function	Clock Output function n inverted output
CKOTXn_R	Clock output function	Relocated Clock Output function n inverted output
COMn	LCD	LCD COM pins
ECLK	External bus	External bus clock output
CSn	External bus	External bus chip select n output
CSn_R	External bus	Relocated External bus chip select n output
DV _{CC}	Supply	SMC pins power supply
FRCKn	Free Running Timer	Free Running Timer n input
FRCKn_R	Free Running Timer	Relocated Free Running Timer n input
HAKX	External bus	External bus Hold Acknowledge
HRQ	External bus	External bus Hold Request
INn	ICU	Input Capture Unit n input
INn_R	ICU	Relocated Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input

Pin Function Description (2 of 3)

Pin name	Feature	Description
INTn_R	External Interrupt	Relocated External Interrupt n input
LBX	External bus	External Bus Interface Lower Byte select strobe output
MDn	Core	Input pins for specifying the operating mode.
NMI	External Interrupt	Non-Maskable Interrupt input
OUTn	OCU	Output Compare Unit n waveform output
OUTn_R	OCU	Relocated Output Compare Unit n waveform output
Pxx_n	GPIO	General purpose IO
PPGn	PPG	Programmable Pulse Generator n output
PPGn_R	PPG	Relocated Programmable Pulse Generator n output
PWMn	SMC	SMC PWM high current
RDX	External bus	External bus interface read strobe output
RDY	External bus	External bus interface external wait state request input
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCLn	I2C	I2C interface n clock I/O input/output
SDAn	I2C	I2C interface n serial data I/O input/output
SEGn	LCD	LCD segment n
SGA	Sound Generator	SG amplitude output
SGO	Sound Generator	SG sound/tone output
SGA_R	Sound Generator	Relocated SG amplitude output
SGO_R	Sound Generator	Relocated SG sound/tone output
SINn	USART	USART n serial data input
SOTn	USART	USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TINn_R	Reload Timer	Relocated Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TOTn_R	Reload Timer	Relocated Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
UBX	External bus	External Bus Interface Upper Byte select strobe output

Pin Function Description (3 of 3)

Pin name	Feature	Description
V _n	LCD	LCD voltage references
V _{CC}	Supply	Power supply
V _{SS}	Supply	Power supply
WOT	RTC	Real Timer clock output
WRHX	External bus	External bus High byte write strobe output
WRLX/WRX	External bus	External bus Low byte / Word write strobe output
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input (only for devices with suffix "W")
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output (only for devices with suffix "W")

5. Pin Circuit Type

Pin Circuit Types (1 of 2)

LQM120	
Pin No.	Circuit Type ^{*1}
1	Supply
2	F
3 to 11	J
12,13	N
14 to 21	K
22	Supply
23 to 24	G
25	Supply
26 to 29	K
30,31	Supply
32 to 35	K
36 to 40	M
41,42	Supply
43 to 52	M
53,54	Supply
55 to 59	M
60, 61	Supply
62 to 64	C
65, 66	A
67	Supply
68,69	B ^{*2}
68,69	H ^{*3}
70	E
71 to 89	J
90 to 91	Supply
92 to 112	J
113 to 116	L

Pin Circuit Types (2 of 2)

LQM120	
Pin No.	Circuit Type ^{*1}
117 to 119	H
120	Supply

*1: See 6. "I/O Circuit Type" for details on the I/O circuit types

*2: Devices with suffix "W"

*3: Devices without suffix "W"

6. I/O Circuit Type

Type	Circuit	Remarks
A		<p>High-speed oscillation circuit:</p> <ul style="list-style-type: none"> • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Programmable feedback resistor = approx. $2 * 0.5 \text{ M}\Omega$. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode
B		<p>Low-speed oscillation circuit:</p> <ul style="list-style-type: none"> • Programmable feedback resistor = approx. $2 * 5 \text{ M}\Omega$. Feedback resistor is grounded in the center when the oscillator is disabled
C		<ul style="list-style-type: none"> • Mask ROM and EVA device: CMOS Hysteresis input pin • Flash device: CMOS input pin
E		<ul style="list-style-type: none"> • CMOS Hysteresis input pin • Pull-up resistor value: approx. $50 \text{ k}\Omega$

Type	Circuit	Remarks
F		<ul style="list-style-type: none"> • Power supply input protection circuit
G		<ul style="list-style-type: none"> • A/D converter ref+ (AVRH/AVRH2) power supply input pin with protection circuit • Flash devices do not have a protection circuit against VCC for pins AVRH/AVRH2 • Devices without AVRH reference switch do not have an analog switch for the AVRL pin
H		<ul style="list-style-type: none"> • CMOS level output (programmable $I_{OL} = 5 \text{ mA}$, $I_{OH} = -5 \text{ mA}$ and $I_{OL} = 2 \text{ mA}$, $I_{OH} = -2 \text{ mA}$) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50 kΩ approx.

Type	Circuit	Remarks
J	 <p>pull-up control</p> <p>Pout</p> <p>Nout</p> <p>R</p> <p>Standby control for input shutdown</p> <p>Hysteresis input</p> <p>Hysteresis input</p> <p>Automotive input</p> <p>TTL input</p> <p>SEG, COM output</p>	<ul style="list-style-type: none"> • CMOS level output (programmable $I_{OL} = 5\text{ mA}$, $I_{OH} = -5\text{ mA}$ and $I_{OL} = 2\text{ mA}$, $I_{OH} = -2\text{ mA}$) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50 kΩ approx. • SEG or COM output
K	 <p>pull-up control</p> <p>Pout</p> <p>Nout</p> <p>R</p> <p>Standby control for input shutdown</p> <p>Hysteresis input</p> <p>Hysteresis input</p> <p>Automotive input</p> <p>TTL input</p> <p>Analog input</p> <p>SEG output</p>	<ul style="list-style-type: none"> • CMOS level output (programmable $I_{OL} = 5\text{ mA}$, $I_{OH} = -5\text{ mA}$ and $I_{OL} = 2\text{ mA}$, $I_{OH} = -2\text{ mA}$) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function. • Programmable pull-up resistor: 50 kΩ approx. • Analog input • SEG output

Type	Circuit	Remarks
L	 <p>The diagram for Type L shows a pull-up control circuit with a resistor and a PMOS transistor. The output node is connected to Pout and Nout. Below the output node, there is a resistor R connected to a logic input. This input is connected to four OR gates, each with a 'Standby control for input shutdown' input. The outputs of these OR gates are labeled: Hysteresis input, Hysteresis input, Automotive input, and TTL input. Below these are Analog input, SEG output, and Vx input.</p>	<ul style="list-style-type: none"> • CMOS level output (programmable $I_{OL} = 5\text{ mA}$, $I_{OH} = -5\text{ mA}$ and $I_{OL} = 2\text{ mA}$, $I_{OH} = -2\text{ mA}$) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50 kΩ approx. • Analog input • Vx input • SEG output
M	 <p>The diagram for Type M is similar to Type L but lacks the Analog input, SEG output, and Vx input connections. It features the same pull-up control, Pout, Nout, and resistor R circuit. The logic input after resistor R is connected to three OR gates with 'Standby control for input shutdown' inputs, leading to Hysteresis input, Hysteresis input, and Automotive input. Below these are TTL input.</p>	<ul style="list-style-type: none"> • CMOS level output (programmable $I_{OL} = 5\text{ mA}$, $I_{OH} = -5\text{ mA}$ and $I_{OL} = 2\text{ mA}$, $I_{OH} = -2\text{ mA}$, $I_{OL} = 30\text{ mA}$, $I_{OH} = -30\text{ mA}$) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50 kΩ approx.

Type	Circuit	Remarks
N	 <p>The diagram shows an input pin circuit. A pull-up resistor is connected to the input node, controlled by a 'pull-up control' signal. The input node is connected to the gates of two transistors, Pout and Nout. Below the input node, there is a resistor R connected to ground. Four input types are shown, each with a 'Standby control for input shutdown' signal: two Hysteresis inputs, one Automotive input, and one TTL input. Each input type is connected to the input node through an OR gate.</p>	<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 3 \text{ mA}$, $I_{OH} = -3 \text{ mA}$) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50 kΩ approx.

7. Memory Map

	CY96V300B		CY96(F)38x	
FF:FFF _H	Emulation ROM		USER ROM / External Bus ^{*4}	
DE:000 _H	External Bus		External Bus	
10:000 _H	Boot-ROM		Boot-ROM	
0F:E00 _H	Reserved		Reserved	
0E:000 _H	External RAM		Reserved	
02:000 _H	Internal RAM bank 1	RAMEND1 ^{*2} RAMSTART1 ^{*2}	Reserved Internal RAM bank 1 Reserved	RAM availability depending on the device
01:000 _H	ROM/RAM MIRROR		ROM/RAM MIRROR	
00:800 _H	Internal RAM bank 0	RAMSTART0 ^{*2}	Internal RAM bank 0 Reserved	External Bus end address ^{*2}
RAM-START0 ^{*3}	External Bus		External Bus	
00:0C0 _H	Peripherals		Peripherals	
00:038 _H	GPR ^{*1}		GPR ^{*1}	
00:018 _H	DMA		DMA	
00:010 _H	External Bus		External Bus	
00:00F _H	Peripheral		Peripheral	
00:000 _H				

*1: Unused GPR banks can be used as RAM area

*2: For External Bus end address and RAMSTART/END addresses, please refer to the table on the next page.

*3: For EVA device, RAMSTART0 depends on the configuration of the emulated device.

*4: For details about USER ROM area, see the 9. "User ROM Memory Map for Flash Devices" and 10. "User ROM Memory Map for Mask Rom Devices" on the following pages.

The External Bus area and DMA area are only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

8. RAMSTART/END and External Bus End Addresses

Devices	Bank 0 RAM size	Bank 1 RAM size	External Bus end address	RAMSTART0	RAMSTART1	RAMEND1
CY96384	6 KByte	-	00:61FF _H	00:6A40 _H	-	-
CY96385/F385	8 KByte	-	00:61FF _H	00:6240 _H	-	-
CY96F386, CY96F387	16 KByte	-	00:41FF _H	00:4240 _H	-	-
CY96F388	28 KByte	-	00:11FF _H	00:1240 _H	-	-
CY96F389	28 KByte	4KByte	00:11FF _H	00:1240 _H	01:8000 _H	01:8FFF _H

9. User ROM Memory Map for Flash Devices

Alternative mode CPU address	Flash memory mode address	CY96F385R CY96F385Y	CY96F386R CY96F386Y	CY96F387R CY96F387Y	
		Flash size 160kByte	Flash size 288kByte	Flash size 416kByte	
FF:FFFF _H	3F:FFFF _H	S39 - 64K	S39 - 64K	S39 - 64K	Flash A
FF:0000 _H	3F:0000 _H	S38 - 64K	S38 - 64K	S38 - 64K	
FE:FFFF _H	3E:FFFF _H				
FE:0000 _H	3E:0000 _H	External bus	S37 - 64K	S37 - 64K	
FD:FFFF _H	3D:FFFF _H				
FD:0000 _H	3D:0000 _H				
FC:FFFF _H	3C:FFFF _H	External bus	S36 - 64K	S36 - 64K	
FC:0000 _H	3C:0000 _H				
FB:FFFF _H	3B:FFFF _H				
FB:0000 _H	3B:0000 _H				
FA:FFFF _H	3A:FFFF _H	External bus	External bus	S35 - 64K	
FA:0000 _H	3A:0000 _H				
F9:FFFF _H	39:FFFF _H				
F9:0000 _H	39:0000 _H				
F8:FFFF _H	38:FFFF _H				
F8:0000 _H	38:0000 _H	External bus	External bus	S34 - 64K	
F7:FFFF _H	37:FFFF _H				
F7:0000 _H	37:0000 _H				
F6:FFFF _H	36:FFFF _H				
F6:0000 _H	36:0000 _H				
F5:FFFF _H	35:FFFF _H				
F5:0000 _H	35:0000 _H	External bus	External bus	External bus	
F4:FFFF _H	34:FFFF _H				
F4:0000 _H	34:0000 _H				
F3:FFFF _H	33:FFFF _H				
F3:0000 _H	33:0000 _H				
F2:FFFF _H	32:FFFF _H				
F2:0000 _H	32:0000 _H				
F1:FFFF _H	31:FFFF _H	Reserved	Reserved	Reserved	
F1:0000 _H	31:0000 _H				
F0:FFFF _H	30:FFFF _H				
F0:0000 _H	30:0000 _H				
E0:FFFF _H		Reserved	Reserved	Reserved	Flash A
E0:0000 _H					
DF:FFFF _H					
DF:8000 _H					
DF:7FFF _H	1F:7FFF _H				
DF:6000 _H	1F:6000 _H				
DF:5FFF _H	1F:5FFF _H				
DF:4000 _H	1F:4000 _H				
DF:3FFF _H	1F:3FFF _H				
DF:2000 _H	1F:2000 _H				
DF:1FFF _H	1F:1FFF _H				
DF:0000 _H	1F:0000 _H				
DE:FFFF _H		Reserved	Reserved	Reserved	
DE:0000 _H					

*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000_H - DF:007F_H

		CY96F388T CY96F388H		CY96F389R CY96F389Y		
Alternative mode CPU address	Flash memory mode address	Flash size 576kByte		Flash size 832kByte		
FF:FFF _H	3F:FFF _H	S39 - 64K		S39 - 64K	Flash A	
FF:000 _H	3F:000 _H					
FE:FFF _H	3E:FFF _H	S38 - 64K		S38 - 64K		
FE:000 _H	3E:000 _H					
FD:FFF _H	3D:FFF _H	S37 - 64K		S37 - 64K		
FD:000 _H	3D:000 _H					
FC:FFF _H	3C:FFF _H	S36 - 64K		S36 - 64K		
FC:000 _H	3C:000 _H					
FB:FFF _H	3B:FFF _H	S35 - 64K		S35 - 64K		
FB:000 _H	3B:000 _H					
FA:FFF _H	3A:FFF _H	S34 - 64K		S34 - 64K		
FA:000 _H	3A:000 _H					
F9:FFF _H	39:FFF _H	S33 - 64K		S33 - 64K		
F9:000 _H	39:000 _H					
F8:FFF _H	38:FFF _H	S32 - 64K		S32 - 64K		
F8:000 _H	38:000 _H					
F7:FFF _H	37:FFF _H	External bus		S31 - 64K	Flash B	
F7:000 _H	37:000 _H					
F6:FFF _H	36:FFF _H					S30 - 64K
F6:000 _H	36:000 _H					
F5:FFF _H	35:FFF _H				S29 - 64K	
F5:000 _H	35:000 _H					
F4:FFF _H	34:FFF _H				S28 - 64K	
F4:000 _H	34:000 _H					
F3:FFF _H	33:FFF _H	External bus		External bus		
F3:000 _H	33:000 _H					
F2:FFF _H	32:FFF _H					
F2:000 _H	32:000 _H					
F1:FFF _H	31:FFF _H					
F1:000 _H	31:000 _H					
F0:FFF _H	30:FFF _H					
F0:000 _H	30:000 _H					
E0:FFF _H						
E0:000 _H		Reserved		Reserved		
DF:FFF _H						
DF:800 _H						
DF:7FF _H	1F:7FF _H	SA3 - 8K		SA3 - 8K	Flash A	
DF:600 _H	1F:600 _H					
DF:5FF _H	1F:5FF _H	SA2 - 8K		SA2 - 8K		
DF:400 _H	1F:400 _H					
DF:3FF _H	1F:3FF _H	SA1 - 8K		SA1 - 8K		
DF:200 _H	1F:200 _H					
DF:1FF _H	1F:1FF _H	SA0 - 8K *1		SA0 - 8K *1		
DF:000 _H	1F:000 _H					
DE:FFF _H		Reserved		Reserved		
DE:800 _H						
DE:7FF _H	1E:7FF _H	SB3 - 8K		SB3 - 8K	Flash B	
DE:600 _H	1E:600 _H					
DE:5FF _H	1E:5FF _H	SB2 - 8K		SB2 - 8K		
DE:400 _H	1E:400 _H					
DE:3FF _H	1E:3FF _H	SB1 - 8K		SB1 - 8K		
DE:200 _H	1E:200 _H					
DE:1FF _H	1E:1FF _H	SB0 - 8K *2		SB0 - 8K *2		
DE:000 _H	1E:000 _H					

*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000_H - DF:007F_H
 *2: Sector SB0 contains the ROM Configuration Block RCBB at CPU address DE:0000_H - DE:002F_H

10. User ROM Memory Map for Mask Rom Devices

CPU address	CY96384	CY96385
	ROM size 128kByte	ROM size 160kByte
FF:FFF _H FF:000 _H	128K ROM	128K ROM
FE:FFF _H FE:000 _H		
FD:FFF _H		
DF:FFF _H DF:800 _H	Reserved	Reserved
DF:7FF _H DF:008 _H		32K ROM
DF:007 _H DF:000 _H		ROM configuration block RCB
DE:FFF _H DE:000 _H	Reserved	Reserved

11. Serial Programming Communication Interface

USART Pins for Flash Serial Programming (MD[2:0] = 010, Serial Communication Mode)

CY96F38x		
Pin Number	USART Number	Normal Function
LQFP-120		
8	USART0	SIN0
9		SOT0
10		SCK0
3	USART1	SIN1
4		SOT1
5		SCK1
56	USART2	SIN2
57		SOT2
58		SCK2

Note: If a Flash programmer and its software needs to use a handshaking pin, Cypress suggests to the tool vendor to support at least port P00_1 on pin 88.

If handshaking is used by the tool but P00_1 is not available in customer's application, Cypress suggests to the customer to check the tool manual or to contact the tool vendor for alternative handshaking pins.

12. I/O Map

I/O Map CY96(F)38x (Sheet 1 of 30)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000000 _H	I/O Port P00 - Port Data Register	PDR00	-	R/W
000001 _H	I/O Port P01 - Port Data Register	PDR01	-	R/W
000002 _H	I/O Port P02 - Port Data Register	PDR02	-	R/W
000003 _H	I/O Port P03 - Port Data Register	PDR03	-	R/W
000004 _H	I/O Port P04 - Port Data Register	PDR04	-	R/W
000005 _H	I/O Port P05 - Port Data Register	PDR05	-	R/W
000006 _H	I/O Port P06 - Port Data Register	PDR06	-	R/W
000007 _H	Reserved	-	-	-
000008 _H	I/O Port P08 - Port Data Register	PDR08	-	R/W
000009 _H	I/O Port P09 - Port Data Register	PDR09	-	R/W
00000A _H	I/O Port P10 - Port Data Register	PDR10	-	R/W
00000B _H	I/O Port P11 - Port Data Register	PDR11	-	R/W
00000C _H	I/O Port P12 - Port Data Register	PDR12	-	R/W
00000D _H	I/O Port P13 - Port Data Register	PDR13	-	R/W
00000E _H - 000017 _H	Reserved	-	-	-
000018 _H	ADC0 - Control Status register Low	ADCSL	ADCS	R/W
000019 _H	ADC0 - Control Status register High	ADCSH	-	R/W
00001A _H	ADC0 - Data Register Low	ADCRL	ADCR	R
00001B _H	ADC0 - Data Register High	ADCRH	-	R
00001C _H	ADC0 - Setting Register	-	ADSR	R/W
00001D _H	ADC0 - Setting Register	-	-	R/W
00001E _H	ADC0 - Extended Configuration Register	ADECR	-	R/W
00001F _H	Reserved	-	-	-
000020 _H	FRT0 - Data register of free-running timer	-	TCDT0	R/W
000021 _H	FRT0 - Data register of free-running timer	-	-	R/W
000022 _H	FRT0 - Control status register of free-running timer Low	TCCSL0	TCCS0	R/W
000023 _H	FRT0 - Control status register of free-running timer High	TCCSH0	-	R/W
000024 _H	FRT1 - Data register of free-running timer	-	TCDT1	R/W
000025 _H	FRT1 - Data register of free-running timer	-	-	R/W

I/O Map CY96(F)38x (Sheet 2 of 30)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000026 _H	FRT1 - Control status register of free-running timer Low	TCCSL1	TCCS1	R/W
000027 _H	FRT1 - Control status register of free-running timer High	TCCSH1	-	R/W
000028 _H	OCU0 - Output Compare Control Status	OCS0	-	R/W
000029 _H	OCU1 - Output Compare Control Status	OCS1	-	R/W
00002A _H	OCU0 - Compare Register	-	OCCP0	R/W
00002B _H	OCU0 - Compare Register	-	-	R/W
00002C _H	OCU1 - Compare Register	-	OCCP1	R/W
00002D _H	OCU1 - Compare Register	-	-	R/W
00002E _H	OCU2 - Output Compare Control Status	OCS2	-	R/W
00002F _H	OCU3 - Output Compare Control Status	OCS3	-	R/W
000030 _H	OCU2 - Compare Register	-	OCCP2	R/W
000031 _H	OCU2 - Compare Register	-	-	R/W
000032 _H	OCU3 - Compare Register	-	OCCP3	R/W
000033 _H	OCU3 - Compare Register	-	-	R/W
000034 _H - 00003F _H	Reserved	-	-	-
000040 _H	ICU0/ICU1 - Control Status Register	ICS01	-	R/W
000041 _H	ICU0/ICU1 - Edge register	ICE01	-	R/W
000042 _H	ICU0 - Capture Register Low	IPCPL0	IPCP0	R
000043 _H	ICU0 - Capture Register High	IPCPL0	-	R
000044 _H	ICU1 - Capture Register Low	IPCPL1	IPCP1	R
000045 _H	ICU1 - Capture Register High	IPCPL1	-	R
000046 _H	ICU2/ICU3 - Control Status Register	ICS23	-	R/W
000047 _H	ICU2/ICU3 - Edge register	ICE23	-	R/W
000048 _H	ICU2 - Capture Register Low	IPCPL2	IPCP2	R
000049 _H	ICU2 - Capture Register High	IPCPL2	-	R
00004A _H	ICU3 - Capture Register Low	IPCPL3	IPCP3	R
00004B _H	ICU3 - Capture Register High	IPCPL3	-	R
00004C _H	ICU4/ICU5 - Control Status Register	ICS45	-	R/W
00004D _H	ICU4/ICU5 - Edge register	ICE45	-	R/W
00004E _H	ICU4 - Capture Register Low	IPCPL4	IPCP4	R

I/O Map CY96(F)38x (Sheet 3 of 30)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
00004F _H	ICU4 - Capture Register High	IPCPH4	-	R
000050 _H	ICU5 - Capture Register Low	IPCPL5	IPCP5	R
000051 _H	ICU5 - Capture Register High	IPCPH5	-	R
000052 _H	ICU6/ICU7 - Control Status Register	ICS67	-	R/W
000053 _H	ICU6/ICU7 - Edge register	ICE67	-	R/W
000054 _H	ICU6 - Capture Register Low	IPCPL6	IPCP6	R
000055 _H	ICU6 - Capture Register High	IPCPH6	-	R
000056 _H	ICU7 - Capture Register Low	IPCPL7	IPCP7	R
000057 _H	ICU7 - Capture Register High	IPCPH7	-	R
000058 _H	EXTINT0 - External Interrupt Enable Register	ENIR0	-	R/W
000059 _H	EXTINT0 - External Interrupt Interrupt request Register	EIRR0	-	R/W
00005A _H	EXTINT0 - External Interrupt Level Select Low	ELVRL0	ELVR0	R/W
00005B _H	EXTINT0 - External Interrupt Level Select High	ELVRH0	-	R/W
00005C _H - 00005F _H	Reserved	-	-	-
000060 _H	RLT0 - Timer Control Status Register Low	TMCSRL0	TMCSR0	R/W
000061 _H	RLT0 - Timer Control Status Register High	TMCSRH0	-	R/W
000062 _H	RLT0 - Reload Register - for writing	-	TMRLR0	W
000062 _H	RLT0 - Reload Register - for reading	-	TMR0	R
000063 _H	RLT0 - Reload Register - for writing	-	-	W
000063 _H	RLT0 - Reload Register - for reading	-	-	R
000064 _H	RLT1 - Timer Control Status Register Low	TMCSRL1	TMCSR1	R/W
000065 _H	RLT1 - Timer Control Status Register High	TMCSRH1	-	R/W
000066 _H	RLT1 - Reload Register - for writing	-	TMRLR1	W
000066 _H	RLT1 - Reload Register - for reading	-	TMR1	R
000067 _H	RLT1 - Reload Register - for writing	-	-	W
000067 _H	RLT1 - Reload Register - for reading	-	-	R
000068 _H	RLT2 - Timer Control Status Register Low	TMCSRL2	TMCSR2	R/W
000069 _H	RLT2 - Timer Control Status Register High	TMCSRH2	-	R/W
00006A _H	RLT2 - Reload Register - for writing	-	TMRLR2	W
00006A _H	RLT2 - Reload Register - for reading	-	TMR2	R

I/O Map CY96(F)38x (Sheet 4 of 30)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
00006B _H	RLT2 - Reload Register - for writing	-	-	W
00006B _H	RLT2 - Reload Register - for reading			R
00006C _H	RLT3 - Timer Control Status Register Low	TMCSRL3	TMCSR3	R/W
00006D _H	RLT3 - Timer Control Status Register High	TMCSRH3	-	R/W
00006E _H	RLT3 - Reload Register - for writing	-	TMRLR3	W
00006E _H	RLT3 - Reload Register - for reading	-	TMR3	R
00006F _H	RLT3 - Reload Register - for writing	-	-	W
00006F _H	RLT3 - Reload Register - for reading			R
000070 _H	RLT6 - Timer Control Status Register Low (dedic. RLT for PPG)	TMCSRL6	TMCSR6	R/W
000071 _H	RLT6 - Timer Control Status Register High (dedic. RLT for PPG)	TMCSRH6	-	R/W
000072 _H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing	-	TMRLR6	W
000072 _H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading	-	TMR6	R
000073 _H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing	-	-	W
000073 _H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading	-	-	R
000074 _H	PPG3-PPG0 - General Control register 1 Low	GCN1L0	GCN10	R/W
000075 _H	PPG3-PPG0 - General Control register 1 High	GCN1H0	-	R/W
000076 _H	PPG3-PPG0 - General Control register 2 Low	GCN2L0	GCN20	R/W
000077 _H	PPG3-PPG0 - General Control register 2 High	GCN2H0	-	R/W
000078 _H	PPG0 - Timer register	-	PTMR0	R
000079 _H	PPG0 - Timer register	-	-	R
00007A _H	PPG0 - Period setting register	-	PCSR0	W
00007B _H	PPG0 - Period setting register	-	-	W
00007C _H	PPG0 - Duty cycle register	-	PDUT0	W
00007D _H	PPG0 - Duty cycle register	-	-	W
00007E _H	PPG0 - Control status register Low	PCNL0	PCN0	R/W
00007F _H	PPG0 - Control status register High	PCNH0	-	R/W
000080 _H	PPG1 - Timer register	-	PTMR1	R
000081 _H	PPG1 - Timer register	-	-	R
000082 _H	PPG1 - Period setting register	-	PCSR1	W

I/O Map CY96(F)38x (Sheet 5 of 30)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000083 _H	PPG1 - Period setting register	-	-	W
000084 _H	PPG1 - Duty cycle register	-	PDUT1	W
000085 _H	PPG1 - Duty cycle register	-	-	W
000086 _H	PPG1 - Control status register Low	PCNL1	PCN1	R/W
000087 _H	PPG1 - Control status register High	PCNH1	-	R/W
000088 _H	PPG2 - Timer register	-	PTMR2	R
000089 _H	PPG2 - Timer register	-	-	R
00008A _H	PPG2 - Period setting register	-	PCSR2	W
00008B _H	PPG2 - Period setting register	-	-	W
00008C _H	PPG2 - Duty cycle register	-	PDUT2	W
00008D _H	PPG2 - Duty cycle register	-	-	W
00008E _H	PPG2 - Control status register Low	PCNL2	PCN2	R/W
00008F _H	PPG2 - Control status register High	PCNH2	-	R/W
000090 _H	PPG3 - Timer register	-	PTMR3	R
000091 _H	PPG3 - Timer register	-	-	R
000092 _H	PPG3 - Period setting register	-	PCSR3	W
000093 _H	PPG3 - Period setting register	-	-	W
000094 _H	PPG3 - Duty cycle register	-	PDUT3	W
000095 _H	PPG3 - Duty cycle register	-	-	W
000096 _H	PPG3 - Control status register Low	PCNL3	PCN3	R/W
000097 _H	PPG3 - Control status register High	PCNH3	-	R/W
000098 _H	PPG7-PPG4 - General Control register 1 Low	GCN1L1	GCN11	R/W
000099 _H	PPG7-PPG4 - General Control register 1 High	GCN1H1	-	R/W
00009A _H	PPG7-PPG4 - General Control register 2 Low	GCN2L1	GCN21	R/W
00009B _H	PPG7-PPG4 - General Control register 2 High	GCN2H1	-	R/W
00009C _H	PPG4 - Timer register	-	PTMR4	R
00009D _H	PPG4 - Timer register	-	-	R
00009E _H	PPG4 - Period setting register	-	PCSR4	W
00009F _H	PPG4 - Period setting register	-	-	W
0000A0 _H	PPG4 - Duty cycle register	-	PDUT4	W

I/O Map CY96(F)38x (Sheet 6 of 30)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
0000A1 _H	PPG4 - Duty cycle register	-	-	W
0000A2 _H	PPG4 - Control status register Low	PCNL4	PCN4	R/W
0000A3 _H	PPG4 - Control status register High	PCNH4	-	R/W
0000A4 _H	PPG5 - Timer register	-	PTMR5	R
0000A5 _H	PPG5 - Timer register	-	-	R
0000A6 _H	PPG5 - Period setting register	-	PCSR5	W
0000A7 _H	PPG5 - Period setting register	-	-	W
0000A8 _H	PPG5 - Duty cycle register	-	PDUT5	W
0000A9 _H	PPG5 - Duty cycle register	-	-	W
0000AA _H	PPG5 - Control status register Low	PCNL5	PCN5	R/W
0000AB _H	PPG5 - Control status register High	PCNH5	-	R/W
0000AC _H	I2C0 - Bus Status Register	IBSR0	-	R
0000AD _H	I2C0 - Bus Control Register	IBCR0	-	R/W
0000AE _H	I2C0 - Ten bit Slave address Register Low	ITBAL0	ITBA0	R/W
0000AF _H	I2C0 - Ten bit Slave address Register High	ITBAH0	-	R/W
0000B0 _H	I2C0 - Ten bit Address mask Register Low	ITMKL0	ITMK0	R/W
0000B1 _H	I2C0 - Ten bit Address mask Register High	ITMKH0	-	R/W
0000B2 _H	I2C0 - Seven bit Slave address Register	ISBA0	-	R/W
0000B3 _H	I2C0 - Seven bit Address mask Register	ISMK0	-	R/W
0000B4 _H	I2C0 - Data Register	IDAR0	-	R/W
0000B5 _H	I2C0 - Clock Control Register	ICCR0	-	R/W
0000B6 _H - 0000BF _H	Reserved	-	-	-
0000C0 _H	USART0 - Serial Mode Register	SMR0	-	R/W
0000C1 _H	USART0 - Serial Control Register	SCR0	-	R/W
0000C2 _H	USART0 - TX Register	TDR0	-	W
0000C2 _H	USART0 - RX Register	RDR0	-	R
0000C3 _H	USART0 - Serial Status	SSR0	-	R/W
0000C4 _H	USART0 - Control/Com. Register	ECCR0	-	R/W
0000C5 _H	USART0 - Ext. Status Register	ESCR0	-	R/W
0000C6 _H	USART0 - Baud Rate Generator Register Low	BGRL0	BGR0	R/W

I/O Map CY96(F)38x (Sheet 7 of 30)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
0000C7 _H	USART0 - Baud Rate Generator Register High	BGRH0	-	R/W
0000C8 _H	USART0 - Extended Serial Interrupt Register	ESIR0	-	R/W
0000C9 _H	Reserved	-	-	-
0000CA _H	USART1 - Serial Mode Register	SMR1	-	R/W
0000CB _H	USART1 - Serial Control Register	SCR1	-	R/W
0000CC _H	USART1 - TX Register	TDR1	-	W
0000CC _H	USART1 - RX Register	RDR1	-	R
0000CD _H	USART1 - Serial Status	SSR1	-	R/W
0000CE _H	USART1 - Control/Com. Register	ECCR1	-	R/W
0000CF _H	USART1 - Ext. Status Register	ESCR1	-	R/W
0000D0 _H	USART1 - Baud Rate Generator Register Low	BGRL1	BGR1	R/W
0000D1 _H	USART1 - Baud Rate Generator Register High	BGRH1	-	R/W
0000D2 _H	USART1 - Extended Serial Interrupt Register	ESIR1	-	R/W
0000D3 _H	Reserved	-	-	-
0000D4 _H	USART2 - Serial Mode Register	SMR2	-	R/W
0000D5 _H	USART2 - Serial Control Register	SCR2	-	R/W
0000D6 _H	USART2 - TX Register	TDR2	-	W
0000D6 _H	USART2 - RX Register	RDR2	-	R
0000D7 _H	USART2 - Serial Status	SSR2	-	R/W
0000D8 _H	USART2 - Control/Com. Register	ECCR2	-	R/W
0000D9 _H	USART2 - Ext. Status Register	ESCR2	-	R/W
0000DA _H	USART2 - Baud Rate Generator Register Low	BGRL2	BGR2	R/W
0000DB _H	USART2 - Baud Rate Generator Register High	BGRH2	-	R/W
0000DC _H	USART2 - Extended Serial Interrupt Register	ESIR2	-	R/W
0000DD _H - 0000EF _H	Reserved	-	-	-
0000F0 _H - 0000FF _H	External Bus area	EXTBUS0	-	R/W
000100 _H	DMA0 - Buffer address pointer low byte	BAPL0	-	R/W
000101 _H	DMA0 - Buffer address pointer middle byte	BAPM0	-	R/W
000102 _H	DMA0 - Buffer address pointer high byte	BAPH0	-	R/W

I/O Map CY96(F)38x (Sheet 8 of 30)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000103 _H	DMA0 - DMA control register	DMACS0	-	R/W
000104 _H	DMA0 - I/O register address pointer low byte	IOAL0	IOA0	R/W
000105 _H	DMA0 - I/O register address pointer high byte	IOAH0	-	R/W
000106 _H	DMA0 - Data counter low byte	DCTL0	DCT0	R/W
000107 _H	DMA0 - Data counter high byte	DCTH0	-	R/W
000108 _H	DMA1 - Buffer address pointer low byte	BAPL1	-	R/W
000109 _H	DMA1 - Buffer address pointer middle byte	BAPM1	-	R/W
00010A _H	DMA1 - Buffer address pointer high byte	BAPH1	-	R/W
00010B _H	DMA1 - DMA control register	DMACS1	-	R/W
00010C _H	DMA1 - I/O register address pointer low byte	IOAL1	IOA1	R/W
00010D _H	DMA1 - I/O register address pointer high byte	IOAH1	-	R/W
00010E _H	DMA1 - Data counter low byte	DCTL1	DCT1	R/W
00010F _H	DMA1 - Data counter high byte	DCTH1	-	R/W
000110 _H	DMA2 - Buffer address pointer low byte	BAPL2	-	R/W
000111 _H	DMA2 - Buffer address pointer middle byte	BAPM2	-	R/W
000112 _H	DMA2 - Buffer address pointer high byte	BAPH2	-	R/W
000113 _H	DMA2 - DMA control register	DMACS2	-	R/W
000114 _H	DMA2 - I/O register address pointer low byte	IOAL2	IOA2	R/W
000115 _H	DMA2 - I/O register address pointer high byte	IOAH2	-	R/W
000116 _H	DMA2 - Data counter low byte	DCTL2	DCT2	R/W
000117 _H	DMA2 - Data counter high byte	DCTH2	-	R/W
000118 _H	DMA3 - Buffer address pointer low byte	BAPL3	-	R/W
000119 _H	DMA3 - Buffer address pointer middle byte	BAPM3	-	R/W
00011A _H	DMA3 - Buffer address pointer high byte	BAPH3	-	R/W
00011B _H	DMA3 - DMA control register	DMACS3	-	R/W
00011C _H	DMA3 - I/O register address pointer low byte	IOAL3	IOA3	R/W
00011D _H	DMA3 - I/O register address pointer high byte	IOAH3	-	R/W
00011E _H	DMA3 - Data counter low byte	DCTL3	DCT3	R/W
00011F _H	DMA3 - Data counter high byte	DCTH3	-	R/W
000120 _H	DMA4 - Buffer address pointer low byte	BAPL4	-	R/W

I/O Map CY96(F)38x (Sheet 9 of 30)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000121 _H	DMA4 - Buffer address pointer middle byte	BAPM4	-	R/W
000122 _H	DMA4 - Buffer address pointer high byte	BAPH4	-	R/W
000123 _H	DMA4 - DMA control register	DMACS4	-	R/W
000124 _H	DMA4 - I/O register address pointer low byte	IOAL4	IOA4	R/W
000125 _H	DMA4 - I/O register address pointer high byte	IOAH4	-	R/W
000126 _H	DMA4 - Data counter low byte	DCTL4	DCT4	R/W
000127 _H	DMA4 - Data counter high byte	DCTH4	-	R/W
000128 _H	DMA5 - Buffer address pointer low byte	BAPL5	-	R/W
000129 _H	DMA5 - Buffer address pointer middle byte	BAPM5	-	R/W
00012A _H	DMA5 - Buffer address pointer high byte	BAPH5	-	R/W
00012B _H	DMA5 - DMA control register	DMACS5	-	R/W
00012C _H	DMA5 - I/O register address pointer low byte	IOAL5	IOA5	R/W
00012D _H	DMA5 - I/O register address pointer high byte	IOAH5	-	R/W
00012E _H	DMA5 - Data counter low byte	DCTL5	DCT5	R/W
00012F _H	DMA5 - Data counter high byte	DCTH5	-	R/W
000130 _H	DMA6 - Buffer address pointer low byte	BAPL6	-	R/W
000131 _H	DMA6 - Buffer address pointer middle byte	BAPM6	-	R/W
000132 _H	DMA6 - Buffer address pointer high byte	BAPH6	-	R/W
000133 _H	DMA6 - DMA control register	DMACS6	-	R/W
000134 _H	DMA6 - I/O register address pointer low byte	IOAL6	IOA6	R/W
000135 _H	DMA6 - I/O register address pointer high byte	IOAH6	-	R/W
000136 _H	DMA6 - Data counter low byte	DCTL6	DCT6	R/W
000137 _H	DMA6 - Data counter high byte	DCTH6	-	R/W
000138 _H - 00017F _H	Reserved	-	-	-
000180 _H - 00037F _H	CPU - General Purpose registers (RAM access)	GPR_RAM	-	R/W
000380 _H	DMA0 - Interrupt select	DISEL0	-	R/W
000381 _H	DMA1 - Interrupt select	DISEL1	-	R/W
000382 _H	DMA2 - Interrupt select	DISEL2	-	R/W
000383 _H	DMA3 - Interrupt select	DISEL3	-	R/W

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Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000384 _H	DMA4 - Interrupt select	DISEL4	-	R/W
000385 _H	DMA5 - Interrupt select	DISEL5	-	R/W
000386 _H	DMA6 - Interrupt select	DISEL6	-	R/W
000387 _H - 00038F _H	Reserved	-	-	-
000390 _H	DMA - Status register low byte	DSRL	DSR	R/W
000391 _H	DMA - Status register high byte	DSRH	-	R/W
000392 _H	DMA - Stop status register low byte	DSSRL	DSSR	R/W
000393 _H	DMA - Stop status register high byte	DSSRH	-	R/W
000394 _H	DMA - Enable register low byte	DERL	DER	R/W
000395 _H	DMA - Enable register high byte	DERH	-	R/W
000396 _H - 00039F _H	Reserved	-	-	-
0003A0 _H	Interrupt level register	ILR	ICR	R/W
0003A1 _H	Interrupt index register	IDX	-	R/W
0003A2 _H	Interrupt vector table base register Low	TBRL	TBR	R/W
0003A3 _H	Interrupt vector table base register High	TBRH	-	R/W
0003A4 _H	Delayed Interrupt register	DIRR	-	R/W
0003A5 _H	Non Maskable Interrupt register	NMI	-	R/W
0003A6 _H - 0003AB _H	Reserved	-	-	-
0003AC _H	EDSU communication interrupt selection Low	EDSU2L	EDSU2	R/W
0003AD _H	EDSU communication interrupt selection High	EDSU2H	-	R/W
0003AE _H	ROM mirror control register	ROMM	-	R/W
0003AF _H	EDSU configuration register	EDSU	-	R/W
0003B0 _H	Memory patch control/status register ch 0/1	-	PFCS0	R/W
0003B1 _H	Memory patch control/status register ch 0/1	-	-	R/W
0003B2 _H	Memory patch control/status register ch 2/3	-	PFCS1	R/W
0003B3 _H	Memory patch control/status register ch 2/3	-	-	R/W
0003B4 _H	Memory patch control/status register ch 4/5	-	PFCS2	R/W
0003B5 _H	Memory patch control/status register ch 4/5	-	-	R/W
0003B6 _H	Memory patch control/status register ch 6/7	-	PFCS3	R/W

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Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
0003B7 _H	Memory patch control/status register ch 6/7	-	-	R/W
0003B8 _H	Memory Patch function - Patch address 0 low	PFAL0	-	R/W
0003B9 _H	Memory Patch function - Patch address 0 middle	PFAM0	-	R/W
0003BA _H	Memory Patch function - Patch address 0 high	PFAH0	-	R/W
0003BB _H	Memory Patch function - Patch address 1 low	PFAL1	-	R/W
0003BC _H	Memory Patch function - Patch address 1 middle	PFAM1	-	R/W
0003BD _H	Memory Patch function - Patch address 1 high	PFAH1	-	R/W
0003BE _H	Memory Patch function - Patch address 2 low	PFAL2	-	R/W
0003BF _H	Memory Patch function - Patch address 2 middle	PFAM2	-	R/W
0003C0 _H	Memory Patch function - Patch address 2 high	PFAH2	-	R/W
0003C1 _H	Memory Patch function - Patch address 3 low	PFAL3	-	R/W
0003C2 _H	Memory Patch function - Patch address 3 middle	PFAM3	-	R/W
0003C3 _H	Memory Patch function - Patch address 3 high	PFAH3	-	R/W
0003C4 _H	Memory Patch function - Patch address 4 low	PFAL4	-	R/W
0003C5 _H	Memory Patch function - Patch address 4 middle	PFAM4	-	R/W
0003C6 _H	Memory Patch function - Patch address 4 high	PFAH4	-	R/W
0003C7 _H	Memory Patch function - Patch address 5 low	PFAL5	-	R/W
0003C8 _H	Memory Patch function - Patch address 5 middle	PFAM5	-	R/W
0003C9 _H	Memory Patch function - Patch address 5 high	PFAH5	-	R/W
0003CA _H	Memory Patch function - Patch address 6 low	PFAL6	-	R/W
0003CB _H	Memory Patch function - Patch address 6 middle	PFAM6	-	R/W
0003CC _H	Memory Patch function - Patch address 6 high	PFAH6	-	R/W
0003CD _H	Memory Patch function - Patch address 7 low	PFAL7	-	R/W
0003CE _H	Memory Patch function - Patch address 7 middle	PFAM7	-	R/W
0003CF _H	Memory Patch function - Patch address 7 high	PFAH7	-	R/W
0003D0 _H	Memory Patch function - Patch data 0 Low	PFDL0	PFD0	R/W
0003D1 _H	Memory Patch function - Patch data 0 High	PFDH0	-	R/W
0003D2 _H	Memory Patch function - Patch data 1 Low	PFDL1	PFD1	R/W
0003D3 _H	Memory Patch function - Patch data 1 High	PFDH1	-	R/W
0003D4 _H	Memory Patch function - Patch data 2 Low	PFDL2	PFD2	R/W

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Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
0003D5 _H	Memory Patch function - Patch data 2 High	PFDH2	-	R/W
0003D6 _H	Memory Patch function - Patch data 3 Low	PFDL3	PFD3	R/W
0003D7 _H	Memory Patch function - Patch data 3 High	PFDH3	-	R/W
0003D8 _H	Memory Patch function - Patch data 4 Low	PFDL4	PFD4	R/W
0003D9 _H	Memory Patch function - Patch data 4 High	PFDH4	-	R/W
0003DA _H	Memory Patch function - Patch data 5 Low	PFDL5	PFD5	R/W
0003DB _H	Memory Patch function - Patch data 5 High	PFDH5	-	R/W
0003DC _H	Memory Patch function - Patch data 6 Low	PFDL6	PFD6	R/W
0003DD _H	Memory Patch function - Patch data 6 High	PFDH6	-	R/W
0003DE _H	Memory Patch function - Patch data 7 Low	PFDL7	PFD7	R/W
0003DF _H	Memory Patch function - Patch data 7 High	PFDH7	-	R/W
0003E0 _H - 0003F0 _H	Reserved	-	-	-
0003F1 _H	Memory Control Status Register A	MCSRA	-	R/W
0003F2 _H	Memory Timing Configuration Register A Low	MTCRAL	MTCRA	R/W
0003F3 _H	Memory Timing Configuration Register A High	MTCRAH	-	R/W
0003F4 _H	Reserved	-	-	-
0003F5 _H	Memory Control Status Register B	MCSRB	-	R/W
0003F6 _H	Memory Timing Configuration Register B Low	MTCRBL	MTCRB	R/W
0003F7 _H	Memory Timing Configuration Register B High	MTCRBH	-	R/W
0003F8 _H	Flash Memory Write Control register 0	FMWC0	-	R/W
0003F9 _H	Flash Memory Write Control register 1	FMWC1	-	R/W
0003FA _H	Flash Memory Write Control register 2	FMWC2	-	R/W
0003FB _H	Flash Memory Write Control register 3	FMWC3	-	R/W
0003FC _H	Flash Memory Write Control register 4	FMWC4	-	R/W
0003FD _H	Flash Memory Write Control register 5	FMWC5	-	R/W
0003FE _H - 0003FF _H	Reserved	-	-	-
000400 _H	Standby Mode control register	SMCR	-	R/W
000401 _H	Clock select register	CKSR	-	R/W
000402 _H	Clock Stabilisation select register	CKSSR	-	R/W

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Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000403 _H	Clock monitor register	CKMR	-	R
000404 _H	Clock Frequency control register Low	CKFCRL	CKFCR	R/W
000405 _H	Clock Frequency control register High	CKFCRH	-	R/W
000406 _H	PLL Control register Low	PLLCRL	PLLCR	R/W
000407 _H	PLL Control register High	PLLCRH	-	R/W
000408 _H	RC clock timer control register	RCTCR	-	R/W
000409 _H	Main clock timer control register	MCTCR	-	R/W
00040A _H	Sub clock timer control register	SCTCR	-	R/W
00040B _H	Reset cause and clock status register with clear function	RCCSRC	-	R
00040C _H	Reset configuration register	RCR	-	R/W
00040D _H	Reset cause and clock status register	RCCSR	-	R
00040E _H	Watch dog timer configuration register	WDTC	-	R/W
00040F _H	Watch dog timer clear pattern register	WDTCP	-	W
000410 _H - 000414 _H	Reserved	-	-	-
000415 _H	Clock output activation register	COAR	-	R/W
000416 _H	Clock output configuration register 0	COCR0	-	R/W
000417 _H	Clock output configuration register 1	COCR1	-	R/W
000418 _H	Clock Modulator control register	CMCR	-	R/W
000419 _H	Reserved	-	-	-
00041A _H	Clock Modulator Parameter register Low	CMPRL	CMPR	R/W
00041B _H	Clock Modulator Parameter register High	CMPRH	-	R/W
00041C _H - 00042B _H	Reserved	-	-	-
00042C _H	Voltage Regulator Control register	VRCR	-	R/W
00042D _H	Clock Input and LVD Control Register	CILCR	-	R/W
00042E _H - 00042F _H	Reserved	-	-	-
000430 _H	I/O Port P00 - Data Direction Register	DDR00	-	R/W
000431 _H	I/O Port P01 - Data Direction Register	DDR01	-	R/W
000432 _H	I/O Port P02 - Data Direction Register	DDR02	-	R/W
000433 _H	I/O Port P03 - Data Direction Register	DDR03	-	R/W

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Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000434 _H	I/O Port P04 - Data Direction Register	DDR04	-	R/W
000435 _H	I/O Port P05 - Data Direction Register	DDR05	-	R/W
000436 _H	I/O Port P06 - Data Direction Register	DDR06	-	R/W
000437 _H	Reserved	-	-	-
000438 _H	I/O Port P08 - Data Direction Register	DDR08	-	R/W
000439 _H	I/O Port P09 - Data Direction Register	DDR09	-	R/W
00043A _H	I/O Port P10 - Data Direction Register	DDR10	-	R/W
00043B _H	I/O Port P11 - Data Direction Register	DDR11	-	R/W
00043C _H	I/O Port P12 - Data Direction Register	DDR12	-	R/W
00043D _H	I/O Port P13 - Data Direction Register	DDR13	-	R/W
00043E _H - 000443 _H	Reserved	-	-	-
000444 _H	I/O Port P00 - Port Input Enable Register	PIER00	-	R/W
000445 _H	I/O Port P01 - Port Input Enable Register	PIER01	-	R/W
000446 _H	I/O Port P02 - Port Input Enable Register	PIER02	-	R/W
000447 _H	I/O Port P03 - Port Input Enable Register	PIER03	-	R/W
000448 _H	I/O Port P04 - Port Input Enable Register	PIER04	-	R/W
000449 _H	I/O Port P05 - Port Input Enable Register	PIER05	-	R/W
00044A _H	I/O Port P06 - Port Input Enable Register	PIER06	-	R/W
00044B _H	Reserved	-	-	-
00044C _H	I/O Port P08 - Port Input Enable Register	PIER08	-	R/W
00044D _H	I/O Port P09 - Port Input Enable Register	PIER09	-	R/W
00044E _H	I/O Port P10 - Port Input Enable Register	PIER10	-	R/W
00044F _H	I/O Port P11 - Port Input Enable Register	PIER11	-	R/W
000450 _H	I/O Port P12 - Port Input Enable Register	PIER12	-	R/W
000451 _H	I/O Port P13 - Port Input Enable Register	PIER13	-	R/W
000452 _H - 000457 _H	Reserved	-	-	-
000458 _H	I/O Port P00 - Port Input Level Register	PILR00	-	R/W
000459 _H	I/O Port P01 - Port Input Level Register	PILR01	-	R/W
00045A _H	I/O Port P02 - Port Input Level Register	PILR02	-	R/W

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Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
00045B _H	I/O Port P03 - Port Input Level Register	PILR03	-	R/W
00045C _H	I/O Port P04 - Port Input Level Register	PILR04	-	R/W
00045D _H	I/O Port P05 - Port Input Level Register	PILR05	-	R/W
00045E _H	I/O Port P06 - Port Input Level Register	PILR06	-	R/W
00045F _H	Reserved	-	-	-
000460 _H	I/O Port P08 - Port Input Level Register	PILR08	-	R/W
000461 _H	I/O Port P09 - Port Input Level Register	PILR09	-	R/W
000462 _H	I/O Port P10 - Port Input Level Register	PILR10	-	R/W
000463 _H	I/O Port P11 - Port Input Level Register	PILR11	-	R/W
000464 _H	I/O Port P12 - Port Input Level Register	PILR12	-	R/W
000465 _H	I/O Port P13 - Port Input Level Register	PILR13	-	R/W
000466 _H - 00046B _H	Reserved	-	-	-
00046C _H	I/O Port P00 - Extended Port Input Level Register	EPILR00	-	R/W
00046D _H	I/O Port P01 - Extended Port Input Level Register	EPILR01	-	R/W
00046E _H	I/O Port P02 - Extended Port Input Level Register	EPILR02	-	R/W
00046F _H	I/O Port P03 - Extended Port Input Level Register	EPILR03	-	R/W
000470 _H	I/O Port P04 - Extended Port Input Level Register	EPILR04	-	R/W
000471 _H	I/O Port P05 - Extended Port Input Level Register	EPILR05	-	R/W
000472 _H	I/O Port P06 - Extended Port Input Level Register	EPILR06	-	R/W
000473 _H	Reserved	-	-	-
000474 _H	I/O Port P08 - Extended Port Input Level Register	EPILR08	-	R/W
000475 _H	I/O Port P09 - Extended Port Input Level Register	EPILR09	-	R/W
000476 _H	I/O Port P10 - Extended Port Input Level Register	EPILR10	-	R/W
000477 _H	I/O Port P11 - Extended Port Input Level Register	EPILR11	-	R/W
000478 _H	I/O Port P12 - Extended Port Input Level Register	EPILR12	-	R/W
000479 _H	I/O Port P13 - Extended Port Input Level Register	EPILR13	-	R/W
00047A _H - 00047F _H	Reserved	-	-	-
000480 _H	I/O Port P00 - Port Output Drive Register	PODR00	-	R/W
000481 _H	I/O Port P01 - Port Output Drive Register	PODR01	-	R/W

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Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000482 _H	I/O Port P02 - Port Output Drive Register	PODR02	-	R/W
000483 _H	I/O Port P03 - Port Output Drive Register	PODR03	-	R/W
000484 _H	I/O Port P04 - Port Output Drive Register	PODR04	-	R/W
000485 _H	I/O Port P05 - Port Output Drive Register	PODR05	-	R/W
000486 _H	I/O Port P06 - Port Output Drive Register	PODR06	-	R/W
000487 _H	Reserved	-	-	-
000488 _H	I/O Port P08 - Port Output Drive Register	PODR08	-	R/W
000489 _H	I/O Port P09 - Port Output Drive Register	PODR09	-	R/W
00048A _H	I/O Port P10 - Port Output Drive Register	PODR10	-	R/W
00048B _H	I/O Port P11 - Port Output Drive Register	PODR11	-	R/W
00048C _H	I/O Port P12 - Port Output Drive Register	PODR12	-	R/W
00048D _H	I/O Port P13 - Port Output Drive Register	PODR13	-	R/W
00048E _H - 00049B _H	Reserved	-	-	-
00049C _H	I/O Port P08 - Port High Drive Register	PHDR08	-	R/W
00049D _H	I/O Port P09 - Port High Drive Register	PHDR09	-	R/W
00049E _H	I/O Port P10 - Port High Drive Register	PHDR10	-	R/W
00049F _H - 0004A7 _H	Reserved	-	-	-
0004A8 _H	I/O Port P00 - Pull-Up resistor Control Register	PUCR00	-	R/W
0004A9 _H	I/O Port P01 - Pull-Up resistor Control Register	PUCR01	-	R/W
0004AA _H	I/O Port P02 - Pull-Up resistor Control Register	PUCR02	-	R/W
0004AB _H	I/O Port P03 - Pull-Up resistor Control Register	PUCR03	-	R/W
0004AC _H	I/O Port P04 - Pull-Up resistor Control Register	PUCR04	-	R/W
0004AD _H	I/O Port P05 - Pull-Up resistor Control Register	PUCR05	-	R/W
0004AE _H	I/O Port P06 - Pull-Up resistor Control Register	PUCR06	-	R/W
0004AF _H	Reserved	-	-	-
0004B0 _H	I/O Port P08 - Pull-Up resistor Control Register	PUCR08	-	R/W
0004B1 _H	I/O Port P09 - Pull-Up resistor Control Register	PUCR09	-	R/W
0004B2 _H	I/O Port P10 - Pull-Up resistor Control Register	PUCR10	-	R/W
0004B3 _H	I/O Port P11 - Pull-Up resistor Control Register	PUCR11	-	R/W

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Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
0004B4 _H	I/O Port P12 - Pull-Up resistor Control Register	PUCR12	-	R/W
0004B5 _H	I/O Port P13 - Pull-Up resistor Control Register	PUCR13	-	R/W
0004B6 _H - 0004BB _H	Reserved	-	-	-
0004BC _H	I/O Port P00 - External Pin State Register	EPSR00	-	R
0004BD _H	I/O Port P01 - External Pin State Register	EPSR01	-	R
0004BE _H	I/O Port P02 - External Pin State Register	EPSR02	-	R
0004BF _H	I/O Port P03 - External Pin State Register	EPSR03	-	R
0004C0 _H	I/O Port P04 - External Pin State Register	EPSR04	-	R
0004C1 _H	I/O Port P05 - External Pin State Register	EPSR05	-	R
0004C2 _H	I/O Port P06 - External Pin State Register	EPSR06	-	R
0004C3 _H	Reserved	-	-	-
0004C4 _H	I/O Port P08 - External Pin State Register	EPSR08	-	R
0004C5 _H	I/O Port P09 - External Pin State Register	EPSR09	-	R
0004C6 _H	I/O Port P10 - External Pin State Register	EPSR10	-	R
0004C7 _H	I/O Port P11 - External Pin State Register	EPSR11	-	R
0004C8 _H	I/O Port P12 - External Pin State Register	EPSR12	-	R
0004C9 _H	I/O Port P13 - External Pin State Register	EPSR13	-	R
0004CA _H - 0004CF _H	Reserved	-	-	-
0004D0 _H	ADC analog input enable register 0	ADER0	-	R/W
0004D1 _H	ADC analog input enable register 1	ADER1	-	R/W
0004D2 _H	ADC analog input enable register 2	ADER2	-	R/W
0004D3 _H	ADC analog input enable register 3	ADER3	-	R/W
0004D4 _H	ADC analog input enable register 4	ADER4	-	R/W
0004D5 _H	Reserved	-	-	-
0004D6 _H	Peripheral Resource Relocation Register 0	PRRR0	-	R/W
0004D7 _H	Peripheral Resource Relocation Register 1	PRRR1	-	R/W
0004D8 _H	Peripheral Resource Relocation Register 2	PRRR2	-	R/W
0004D9 _H	Peripheral Resource Relocation Register 3	PRRR3	-	R/W
0004DA _H	Peripheral Resource Relocation Register 4	PRRR4	-	R/W

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Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
0004DB _H	Peripheral Resource Relocation Register 5	PRRR5	-	R/W
0004DC _H	Peripheral Resource Relocation Register 6	PRRR6	-	R/W
0004DD _H	Peripheral Resource Relocation Register 7	PRRR7	-	R/W
0004DE _H	Peripheral Resource Relocation Register 8	PRRR8	-	R/W
0004DF _H	Peripheral Resource Relocation Register 9	PRRR9	-	R/W
0004E0 _H	RTC - Sub Second Register L	WTBRL0	WTBR0	R/W
0004E1 _H	RTC - Sub Second Register M	WTBRH0	-	R/W
0004E2 _H	RTC - Sub-Second Register H	WTBR1	-	R/W
0004E3 _H	RTC - Second Register	WTSR	-	R/W
0004E4 _H	RTC - Minutes	WTMR	-	R/W
0004E5 _H	RTC - Hour	WTHR	-	R/W
0004E6 _H	RTC - Timer Control Extended Register	WTCER	-	R/W
0004E7 _H	RTC - Clock select register	WTCKSR	-	R/W
0004E8 _H	RTC - Timer Control Register Low	WTCRL	WTCR	R/W
0004E9 _H	RTC - Timer Control Register High	WTCRH	-	R/W
0004EA _H	CAL - Calibration unit Control register	CUCR	-	R/W
0004EB _H	Reserved	-	-	-
0004EC _H	CAL - Duration Timer Data Register Low	CUTDL	CUTD	R/W
0004ED _H	CAL - Duration Timer Data Register High	CUTDH	-	R/W
0004EE _H	CAL - Calibration Timer Register 2 Low	CUTR2L	CUTR2	R
0004EF _H	CAL - Calibration Timer Register 2 High	CUTR2H	-	R
0004F0 _H	CAL - Calibration Timer Register 1 Low	CUTR1L	CUTR1	R
0004F1 _H	CAL - Calibration Timer Register 1 High	CUTR1H	-	R
0004F2 _H - 0004F9 _H	Reserved	-	-	-
0004FA _H	RLT - Timer input select (for Cascading)	TMISR	-	R/W
0004FB _H - 00051F _H	Reserved	-	-	-
000520 _H	USART4 - Serial Mode Register	SMR4	-	R/W
000521 _H	USART4 - Serial Control Register	SCR4	-	R/W
000522 _H	USART4 - TX Register	TDR4	-	W

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Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000522 _H	USART4 - RX Register	RDR4	-	R
000523 _H	USART4 - Serial Status	SSR4	-	R/W
000524 _H	USART4 - Control/Com. Register (internal)	ECCR4	-	R/W
000525 _H	USART4 - Ext. Status Register	ESCR4	-	R/W
000526 _H	USART4 - Baud Rate Generator Register Low	BGRL4	BGR4	R/W
000527 _H	USART4 - Baud Rate Generator Register High	BGRH4	-	R/W
000528 _H	USART4 - Extended Serial Interrupt Register	ESIR4	-	R/W
000529 _H	Reserved	-	-	-
00052A _H	USART5 - Serial Mode Register	SMR5	-	R/W
00052B _H	USART5 - Serial Control Register	SCR5	-	R/W
00052C _H	USART5 - RX Register	TDR5	-	W
00052C _H	USART5 - TX Register	RDR5	-	R
00052D _H	USART5 - Serial Status	SSR5	-	R/W
00052E _H	USART5 - Control/Com. Register	ECCR5	-	R/W
00052F _H	USART5 - Ext. Status Register	ESCR5	-	R/W
000530 _H	USART5 - Baud Rate Generator Register Low	BGRL5	BGR5	R/W
000531 _H	USART5 - Baud Rate Generator Register High	BGRH5	-	R/W
000532 _H	USART5 - Extended Serial Interrupt Register	ESIR5	-	R/W
000533 _H - 00055F _H	Reserved	-	-	-
000560 _H	ALARM0 - Control Status Register	ACSR0	-	R/W
000561 _H	ALARM0 - Extended Control Status Register	AECSR0	-	R/W
000562 _H	ALARM1 - Control Status Register	ACSR1	-	R/W
000563 _H	ALARM1 - Extended Control Status Register	AECSR1	-	R/W
000564 _H	PPG6 - Timer register	-	PTMR6	R
000565 _H	PPG6 - Timer register	-	-	R
000566 _H	PPG6 - Period setting register	-	PCSR6	W
000567 _H	PPG6 - Period setting register	-	-	W
000568 _H	PPG6 - Duty cycle register	-	PDUT6	W
000569 _H	PPG6 - Duty cycle register	-	-	W
00056A _H	PPG6 - Control status register Low	PCNL6	PCN6	R/W

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Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
00056B _H	PPG6 - Control status register High	PCNH6	-	R/W
00056C _H	PPG7 - Timer register	-	PTMR7	R
00056D _H	PPG7 - Timer register	-	-	R
00056E _H	PPG7 - Period setting register	-	PCSR7	W
00056F _H	PPG7 - Period setting register	-		W
000570 _H	PPG7 - Duty cycle register	-	PDUT7	W
000571 _H	PPG7 - Duty cycle register	-	-	W
000572 _H	PPG7 - Control status register Low	PCNL7	PCN7	R/W
000573 _H	PPG7 - Control status register High	PCNH7	-	R/W
000574 _H 0005DF _H	Reserved	-	-	-
0005E0 _H	SMC0 - PWM control register	PWC0	-	R/W
0005E1 _H	SMC0 - Extended control register (Output enable)	PWEC0	-	R/W
0005E2 _H	SMC0 - PWM compare register PWM 1	-	PWC10	R/W
0005E3 _H	SMC0 - PWM compare register PWM 1	-	-	R/W
0005E4 _H	SMC0 - PWM compare register PWM 2	-	PWC20	R/W
0005E5 _H	SMC0 - PWM compare register PWM 2	-	-	R/W
0005E6 _H	SMC0 - PWM Select register	PWS10	-	R/W
0005E7 _H	SMC0 - PWM Select register	PWS20	-	R/W
0005E8 _H 0005E9 _H	Reserved	-	-	-
0005EA _H	SMC1 - PWM control register	PWC1	-	R/W
0005EB _H	SMC1 - Extended control register (Output enable)	PWEC1	-	R/W
0005EC _H	SMC1 - PWM compare register PWM 1	-	PWC11	R/W
0005ED _H	SMC1 - PWM compare register PWM 1	-	-	R/W
0005EE _H	SMC1 - PWM compare register PWM 2	-	PWC21	R/W
0005EF _H	SMC1 - PWM compare register PWM 2	-	-	R/W
0005F0 _H	SMC1 - PWM Select register	PWS11	-	R/W
0005F1 _H	SMC1 - PWM Select register	PWS21	-	R/W
0005F2 _H 0005F3 _H	Reserved	-	-	-
0005F4 _H	SMC2 - PWM control register	PWC2	-	R/W

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Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
0005F5 _H	SMC2 - Extended control register (Output enable)	PWEC2	-	R/W
0005F6 _H	SMC2 - PWM compare register PWM 1	-	PWC12	R/W
0005F7 _H	SMC2 - PWM compare register PWM 1	-	-	R/W
0005F8 _H	SMC2 - PWM compare register PWM 2	-	PWC22	R/W
0005F9 _H	SMC2 - PWM compare register PWM 2	-	-	R/W
0005FA _H	SMC2 - PWM Select register	PWS12	-	R/W
0005FB _H	SMC2 - PWM Select register	PWS22	-	R/W
0005FC _H - 0005FD _H	Reserved	-	-	-
0005FE _H	SMC3 - PWM control register	PWC3	-	R/W
0005FF _H	SMC3 - Extended control register (Output enable)	PWEC3	-	R/W
000600 _H	SMC3 - PWM compare register PWM 1	-	PWC13	R/W
000601 _H	SMC3 - PWM compare register PWM 1	-	-	R/W
000602 _H	SMC3 - PWM compare register PWM 2	-	PWC23	R/W
000603 _H	SMC3 - PWM compare register PWM 2	-	-	R/W
000604 _H	SMC3 - PWM Select register	PWS13	-	R/W
000605 _H	SMC3 - PWM Select register	PWS23	-	R/W
000606 _H - 000607 _H	Reserved	-	-	-
000608 _H	SMC4 - PWM control register	PWC4	-	R/W
000609 _H	SMC4 - Extended control register (Output enable)	PWEC4	-	R/W
00060A _H	SMC4 - PWM compare register PWM 1	-	PWC14	R/W
00060B _H	SMC4 - PWM compare register PWM 1	-	-	R/W
00060C _H	SMC4 - PWM compare register PWM 2	-	PWC24	R/W
00060D _H	SMC4 - PWM compare register PWM 2	-	-	R/W
00060E _H	SMC4 - PWM Select register	PWS14	-	R/W
00060F _H	SMC4 - PWM Select register	PWS24	-	R/W
000610 _H - 00061B _H	Reserved	-	-	-
00061C _H	LCD - Output Enable Register 0 (Seg 7-0)	LCDER0	-	R/W
00061D _H	LCD - Output Enable Register 1 (Seg 15-8)	LCDER1	-	R/W
00061E _H	LCD - Output Enable Register 2 (Seg 23-16)	LCDER2	-	R/W

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Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
00061F _H	LCD - Output Enable Register 3 (Seg 31-24)	LCDER3	-	R/W
000620 _H	LCD - Output Enable Register 4 (Seg 39-32)	LCDER4	-	R/W
000621 _H	LCD - Output Enable Register 5 (Seg 47-40)	LCDER5	-	R/W
000622 _H	LCD - Output Enable Register 6 (Seg 55-48)	LCDER6	-	R/W
000623 _H	LCD - Output Enable Register 7 (Seg 63-56)	LCDER7	-	R/W
000624 _H	LCD - Output Enable Register 8 (Seg 71-64)	LCDER8	-	R/W
000625 _H	Reserved	-	-	-
000626 _H	LCD - Output Enable Register V (Vx)	LCDVER	-	R/W
000627 _H	LCD - Extended Control Register	LECR	-	R/W
000628 _H	LCD - Common pin switching register	LCDCMR	-	R/W
000629 _H	LCD - Control Register	LCR	-	R/W
00062A _H	LCD - Data register for Segment 1-0	VRAM0	-	R/W
00062B _H	LCD - Data register for Segment 3-2	VRAM1	-	R/W
00062C _H	LCD - Data register for Segment 5-4	VRAM2	-	R/W
00062D _H	LCD - Data register for Segment 7-6	VRAM3	-	R/W
00062E _H	LCD - Data register for Segment 9-8	VRAM4	-	R/W
00062F _H	LCD - Data register for Segment 11-10	VRAM5	-	R/W
000630 _H	LCD - Data register for Segment 13-12	VRAM6	-	R/W
000631 _H	LCD - Data register for Segment 15-14	VRAM7	-	R/W
000632 _H	LCD - Data register for Segment 17-16	VRAM8	-	R/W
000633 _H	LCD - Data register for Segment 19-18	VRAM9	-	R/W
000634 _H	LCD - Data register for Segment 21-20	VRAM10	-	R/W
000635 _H	LCD - Data register for Segment 23-22	VRAM11	-	R/W
000636 _H	LCD - Data register for Segment 25-24	VRAM12	-	R/W
000637 _H	LCD - Data register for Segment 27-26	VRAM13	-	R/W
000638 _H	LCD - Data register for Segment 29-28	VRAM14	-	R/W
000639 _H	LCD - Data register for Segment 31-30	VRAM15	-	R/W
00063A _H	LCD - Data register for Segment 33-32	VRAM16	-	R/W
00063B _H	LCD - Data register for Segment 35-34	VRAM17	-	R/W
00063C _H	LCD - Data register for Segment 37-36	VRAM18	-	R/W

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Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
00063D _H	LCD - Data register for Segment 39-38	VRAM19	-	R/W
00063E _H	LCD - Data register for Segment 41-40	VRAM20	-	R/W
00063F _H	LCD - Data register for Segment 43-42	VRAM21	-	R/W
000640 _H	LCD - Data register for Segment 45-44	VRAM22	-	R/W
000641 _H	LCD - Data register for Segment 47-46	VRAM23	-	R/W
000642 _H	LCD - Data register for Segment 49-48	VRAM24	-	R/W
000643 _H	LCD - Data register for Segment 51-50	VRAM25	-	R/W
000644 _H	LCD - Data register for Segment 53-52	VRAM26	-	R/W
000645 _H	LCD - Data register for Segment 55-54	VRAM27	-	R/W
000646 _H	LCD - Data register for Segment 57-56	VRAM28	-	R/W
000647 _H	LCD - Data register for Segment 59-58	VRAM29	-	R/W
000648 _H	LCD - Data register for Segment 61-60	VRAM30	-	R/W
000649 _H	LCD - Data register for Segment 63-62	VRAM31	-	R/W
00064A _H	LCD - Data register for Segment 65-64	VRAM32	-	R/W
00064B _H - 00065F _H	Reserved	-	-	-
000660 _H	Peripheral Resource Relocation Register 10	PRRR10	-	R/W
000661 _H	Peripheral Resource Relocation Register 11	PRRR11	-	R/W
000662 _H	Peripheral Resource Relocation Register 12	PRRR12	-	R/W
000663 _H	Peripheral Resource Relocation Register 13	PRRR13	-	W
000664 _H - 0006DF _H	Reserved	-	-	-
0006E0 _H	External Bus - Area configuration register 0 Low	EACL0	EAC0	R/W
0006E1 _H	External Bus - Area configuration register 0 High	EACH0	-	R/W
0006E2 _H	External Bus - Area configuration register 1 Low	EACL1	EAC1	R/W
0006E3 _H	External Bus - Area configuration register 1 High	EACH1	-	R/W
0006E4 _H	External Bus - Area configuration register 2 Low	EACL2	EAC2	R/W
0006E5 _H	External Bus - Area configuration register 2 High	EACH2	-	R/W
0006E6 _H	External Bus - Area configuration register 3 Low	EACL3	EAC3	R/W
0006E7 _H	External Bus - Area configuration register 3 High	EACH3	-	R/W
0006E8 _H	External Bus - Area configuration register 4 Low	EACL4	EAC4	R/W

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Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
0006E9 _H	External Bus - Area configuration register 4 High	EACH4	-	R/W
0006EA _H	External Bus - Area configuration register 5 Low	EACL5	EAC5	R/W
0006EB _H	External Bus - Area configuration register 5 High	EACH5	-	R/W
0006EC _H	External Bus - Area select register 2	EAS2	-	R/W
0006ED _H	External Bus - Area select register 3	EAS3	-	R/W
0006EE _H	External Bus - Area select register 4	EAS4	-	R/W
0006EF _H	External Bus - Area select register 5	EAS5	-	R/W
0006F0 _H	External Bus - Mode register	EBM	-	R/W
0006F1 _H	External Bus - Clock and Function register	EBCF	-	R/W
0006F2 _H	External Bus - Address output enable register 0	EBAE0	-	R/W
0006F3 _H	External Bus - Address output enable register 1	EBAE1	-	R/W
0006F4 _H	External Bus - Address output enable register 2	EBAE2	-	R/W
0006F5 _H	External Bus - Control signal register	EBCS	-	R/W
0006F6 _H - 0006FF _H	Reserved	-	-	-
000700 _H	CAN0 - Control register Low	CTRLRL0	CTRLR0	R/W
000701 _H	CAN0 - Control register High (reserved)	CTRLRH0	-	R
000702 _H	CAN0 - Status register Low	STATRL0	STATR0	R/W
000703 _H	CAN0 - Status register High (reserved)	STATRH0	-	R
000704 _H	CAN0 - Error Counter Low (Transmit)	ERRCNTL0	ERRCNT0	R
000705 _H	CAN0 - Error Counter High (Receive)	ERRCNTH0	-	R
000706 _H	CAN0 - Bit Timing Register Low	BTRL0	BTR0	R/W
000707 _H	CAN0 - Bit Timing Register High	BTRH0	-	R/W
000708 _H	CAN0 - Interrupt Register Low	INTRL0	INTR0	R
000709 _H	CAN0 - Interrupt Register High	INTRH0	-	R
00070A _H	CAN0 - Test Register Low	TESTRL0	TESTR0	R/W
00070B _H	CAN0 - Test Register High (reserved)	TESTRH0	-	R
00070C _H	CAN0 - BRP Extension register Low	BRPERL0	BRPER0	R/W
00070D _H	CAN0 - BRP Extension register High (reserved)	BRPERH0	-	R
00070E _H - 00070F _H	Reserved	-	-	-

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Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000710 _H	CAN0 - IF1 Command request register Low	IF1CREQL0	IF1CREQ0	R/W
000711 _H	CAN0 - IF1 Command request register High	IF1CREQH0	-	R/W
000712 _H	CAN0 - IF1 Command Mask register Low	IF1CMSKL0	IF1CMSK0	R/W
000713 _H	CAN0 - IF1 Command Mask register High (reserved)	IF1CMSKH0	-	R
000714 _H	CAN0 - IF1 Mask 1 Register Low	IF1MSK1L0	IF1MSK10	R/W
000715 _H	CAN0 - IF1 Mask 1 Register High	IF1MSK1H0	-	R/W
000716 _H	CAN0 - IF1 Mask 2 Register Low	IF1MSK2L0	IF1MSK20	R/W
000717 _H	CAN0 - IF1 Mask 2 Register High	IF1MSK2H0	-	R/W
000718 _H	CAN0 - IF1 Arbitration 1 Register Low	IF1ARB1L0	IF1ARB10	R/W
000719 _H	CAN0 - IF1 Arbitration 1 Register High	IF1ARB1H0	-	R/W
00071A _H	CAN0 - IF1 Arbitration 2 Register Low	IF1ARB2L0	IF1ARB20	R/W
00071B _H	CAN0 - IF1 Arbitration 2 Register High	IF1ARB2H0	-	R/W
00071C _H	CAN0 - IF1 Message Control Register Low	IF1MCTRL0	IF1MCTR0	R/W
00071D _H	CAN0 - IF1 Message Control Register High	IF1MCTRH0	-	R/W
00071E _H	CAN0 - IF1 Data A1 Low	IF1DTA1L0	IF1DTA10	R/W
00071F _H	CAN0 - IF1 Data A1 High	IF1DTA1H0	-	R/W
000720 _H	CAN0 - IF1 Data A2 Low	IF1DTA2L0	IF1DTA20	R/W
000721 _H	CAN0 - IF1 Data A2 High	IF1DTA2H0	-	R/W
000722 _H	CAN0 - IF1 Data B1 Low	IF1DTB1L0	IF1DTB10	R/W
000723 _H	CAN0 - IF1 Data B1 High	IF1DTB1H0	-	R/W
000724 _H	CAN0 - IF1 Data B2 Low	IF1DTB2L0	IF1DTB20	R/W
000725 _H	CAN0 - IF1 Data B2 High	IF1DTB2H0	-	R/W
000726 _H - 00073F _H	Reserved	-	-	-
000740 _H	CAN0 - IF2 Command request register Low	IF2CREQL0	IF2CREQ0	R/W
000741 _H	CAN0 - IF2 Command request register High	IF2CREQH0	-	R/W
000742 _H	CAN0 - IF2 Command Mask register Low	IF2CMSKL0	IF2CMSK0	R/W
000743 _H	CAN0 - IF2 Command Mask register High (reserved)	IF2CMSKH0	-	R
000744 _H	CAN0 - IF2 Mask 1 Register Low	IF2MSK1L0	IF2MSK10	R/W
000745 _H	CAN0 - IF2 Mask 1 Register High	IF2MSK1H0	-	R/W

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Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000746 _H	CAN0 - IF2 Mask 2 Register Low	IF2MSK2L0	IF2MSK20	R/W
000747 _H	CAN0 - IF2 Mask 2 Register High	IF2MSK2H0	-	R/W
000748 _H	CAN0 - IF2 Arbitration 1 Register Low	IF2ARB1L0	IF2ARB10	R/W
000749 _H	CAN0 - IF2 Arbitration 1 Register High	IF2ARB1H0	-	R/W
00074A _H	CAN0 - IF2 Arbitration 2 Register Low	IF2ARB2L0	IF2ARB20	R/W
00074B _H	CAN0 - IF2 Arbitration 2 Register High	IF2ARB2H0	-	R/W
00074C _H	CAN0 - IF2 Message Control Register Low	IF2MCTRL0	IF2MCTR0	R/W
00074D _H	CAN0 - IF2 Message Control Register High	IF2MCTRH0	-	R/W
00074E _H	CAN0 - IF2 Data A1 Low	IF2DTA1L0	IF2DTA10	R/W
00074F _H	CAN0 - IF2 Data A1 High	IF2DTA1H0	-	R/W
000750 _H	CAN0 - IF2 Data A2 Low	IF2DTA2L0	IF2DTA20	R/W
000751 _H	CAN0 - IF2 Data A2 High	IF2DTA2H0	-	R/W
000752 _H	CAN0 - IF2 Data B1 Low	IF2DTB1L0	IF2DTB10	R/W
000753 _H	CAN0 - IF2 Data B1 High	IF2DTB1H0	-	R/W
000754 _H	CAN0 - IF2 Data B2 Low	IF2DTB2L0	IF2DTB20	R/W
000755 _H	CAN0 - IF2 Data B2 High	IF2DTB2H0	-	R/W
000756 _H - 00077F _H	Reserved	-	-	-
000780 _H	CAN0 - Transmission Request 1 Register Low	TREQR1L0	TREQR10	R
000781 _H	CAN0 - Transmission Request 1 Register High	TREQR1H0	-	R
000782 _H	CAN0 - Transmission Request 2 Register Low	TREQR2L0	TREQR20	R
000783 _H	CAN0 - Transmission Request 2 Register High	TREQR2H0	-	R
000784 _H - 00078F _H	Reserved	-	-	-
000790 _H	CAN0 - New Data 1 Register Low	NEWDT1L0	NEWDT10	R
000791 _H	CAN0 - New Data 1 Register High	NEWDT1H0	-	R
000792 _H	CAN0 - New Data 2 Register Low	NEWDT2L0	NEWDT20	R
000793 _H	CAN0 - New Data 2 Register High	NEWDT2H0	-	R
000794 _H - 00079F _H	Reserved	-	-	-
0007A0 _H	CAN0 - Interrupt Pending 1 Register Low	INTPND1L0	INTPND10	R
0007A1 _H	CAN0 - Interrupt Pending 1 Register High	INTPND1H0	-	R

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Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
0007A2 _H	CAN0 - Interrupt Pending 2 Register Low	INTPND2L0	INTPND20	R
0007A3 _H	CAN0 - Interrupt Pending 2 Register High	INTPND2H0	-	R
0007A4 _H - 0007AF _H	Reserved	-	-	-
0007B0 _H	CAN0 - Message Valid 1 Register Low	MSGVAL1L0	MSGVAL10	R
0007B1 _H	CAN0 - Message Valid 1 Register High	MSGVAL1H0	-	R
0007B2 _H	CAN0 - Message Valid 2 Register Low	MSGVAL2L0	MSGVAL20	R
0007B3 _H	CAN0 - Message Valid 2 Register High	MSGVAL2H0	-	R
0007B4 _H - 0007CD _H	Reserved	-	-	-
0007CE _H	CAN0 - Output enable register	COER0	-	R/W
0007CF _H	Reserved	-	-	-
0007D0 _H	SG0 - Sound Generator Control Register Low	SGCRL0	SGCR0	R/W
0007D1 _H	SG0 - Sound Generator Control Register High	SGCRH0	-	R/W
0007D2 _H	SG0 - Sound Generator Frequency Register	SGFR0	-	R/W
0007D3 _H	SG0 - Sound Generator Amplitude Register	SGAR0	-	R/W
0007D4 _H	SG0 - Sound Generator Decrement Register	SGDR0	-	R/W
0007D5 _H	SG0 - Sound Generator Tone Register	SGTR0	-	R/W
0007D6 _H	SG1 - Sound Generator Control Register Low	SGCRL1	SGCR1	R/W
0007D7 _H	SG1 - Sound Generator Control Register High	SGCRH1	-	R/W
0007D8 _H	SG1 - Sound Generator Frequency Register	SGFR1	-	R/W
0007D9 _H	SG1 - Sound Generator Amplitude Register	SGAR1	-	R/W
0007DA _H	SG1 - Sound Generator Decrement Register	SGDR1	-	R/W
0007DB _H	SG1 - Sound Generator Tone Register	SGTR1	-	R/W
0007DC _H - 0007FF _H	Reserved	-	-	-
000800 _H	CAN1 - Control register Low	CTRLRL1	CTRLR1	R/W
000801 _H	CAN1 - Control register High (reserved)	CTRLRH1	-	R
000802 _H	CAN1 - Status register Low	STATRL1	STATR1	R/W
000803 _H	CAN1 - Status register High (reserved)	STATRH1	-	R
000804 _H	CAN1 - Error Counter Low (Transmit)	ERRCNTL1	ERRCNT1	R
000805 _H	CAN1 - Error Counter High (Receive)	ERRCNTH1	-	R

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Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000806 _H	CAN1 - Bit Timing Register Low	BTRL1	BTR1	R/W
000807 _H	CAN1 - Bit Timing Register High	BTRH1	-	R/W
000808 _H	CAN1 - Interrupt Register Low	INTRL1	INTR1	R
000809 _H	CAN1 - Interrupt Register High	INTRH1	-	R
00080A _H	CAN1 - Test Register Low	TESTRL1	TESTR1	R/W
00080B _H	CAN1 - Test Register High (reserved)	TESTRH1	-	R
00080C _H	CAN1 - BRP Extension register Low	BRPERL1	BRPER1	R/W
00080D _H	CAN1 - BRP Extension register High (reserved)	BRPERH1	-	R
00080E _H - 00080F _H	Reserved	-	-	-
000810 _H	CAN1 - IF1 Command request register Low	IF1CREQL1	IF1CREQ1	R/W
000811 _H	CAN1 - IF1 Command request register High	IF1CREQH1	-	R/W
000812 _H	CAN1 - IF1 Command Mask register Low	IF1CMSKL1	IF1CMSK1	R/W
000813 _H	CAN1 - IF1 Command Mask register High (reserved)	IF1CMSKH1	-	R
000814 _H	CAN1 - IF1 Mask 1 Register Low	IF1MSK1L1	IF1MSK11	R/W
000815 _H	CAN1 - IF1 Mask 1 Register High	IF1MSK1H1	-	R/W
000816 _H	CAN1 - IF1 Mask 2 Register Low	IF1MSK2L1	IF1MSK21	R/W
000817 _H	CAN1 - IF1 Mask 2 Register High	IF1MSK2H1	-	R/W
000818 _H	CAN1 - IF1 Arbitration 1 Register Low	IF1ARB1L1	IF1ARB11	R/W
000819 _H	CAN1 - IF1 Arbitration 1 Register High	IF1ARB1H1	-	R/W
00081A _H	CAN1 - IF1 Arbitration 2 Register Low	IF1ARB2L1	IF1ARB21	R/W
00081B _H	CAN1 - IF1 Arbitration 2 Register High	IF1ARB2H1	-	R/W
00081C _H	CAN1 - IF1 Message Control Register Low	IF1MCTRL1	IF1MCTR1	R/W
00081D _H	CAN1 - IF1 Message Control Register High	IF1MCTRH1	-	R/W
00081E _H	CAN1 - IF1 Data A1 Low	IF1DTA1L1	IF1DTA11	R/W
00081F _H	CAN1 - IF1 Data A1 High	IF1DTA1H1	-	R/W
000820 _H	CAN1 - IF1 Data A2 Low	IF1DTA2L1	IF1DTA21	R/W
000821 _H	CAN1 - IF1 Data A2 High	IF1DTA2H1	-	R/W
000822 _H	CAN1 - IF1 Data B1 Low	IF1DTB1L1	IF1DTB11	R/W
000823 _H	CAN1 - IF1 Data B1 High	IF1DTB1H1	-	R/W

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Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000824 _H	CAN1 - IF1 Data B2 Low	IF1DTB2L1	IF1DTB21	R/W
000825 _H	CAN1 - IF1 Data B2 High	IF1DTB2H1	-	R/W
000826 _H - 00083F _H	Reserved	-	-	-
000840 _H	CAN1 - IF2 Command request register Low	IF2CREQL1	IF2CREQ1	R/W
000841 _H	CAN1 - IF2 Command request register High	IF2CREQH1	-	R/W
000842 _H	CAN1 - IF2 Command Mask register Low	IF2CMSKL1	IF2CMSK1	R/W
000843 _H	CAN1 - IF2 Command Mask register High (reserved)	IF2CMSKH1	-	R
000844 _H	CAN1 - IF2 Mask 1 Register Low	IF2MSK1L1	IF2MSK11	R/W
000845 _H	CAN1 - IF2 Mask 1 Register High	IF2MSK1H1	-	R/W
000846 _H	CAN1 - IF2 Mask 2 Register Low	IF2MSK2L1	IF2MSK21	R/W
000847 _H	CAN1 - IF2 Mask 2 Register High	IF2MSK2H1	-	R/W
000848 _H	CAN1 - IF2 Arbitration 1 Register Low	IF2ARB1L1	IF2ARB11	R/W
000849 _H	CAN1 - IF2 Arbitration 1 Register High	IF2ARB1H1	-	R/W
00084A _H	CAN1 - IF2 Arbitration 2 Register Low	IF2ARB2L1	IF2ARB21	R/W
00084B _H	CAN1 - IF2 Arbitration 2 Register High	IF2ARB2H1	-	R/W
00084C _H	CAN1 - IF2 Message Control Register Low	IF2MCTRL1	IF2MCTR1	R/W
00084D _H	CAN1 - IF2 Message Control Register High	IF2MCTRH1	-	R/W
00084E _H	CAN1 - IF2 Data A1 Low	IF2DTA1L1	IF2DTA11	R/W
00084F _H	CAN1 - IF2 Data A1 High	IF2DTA1H1	-	R/W
000850 _H	CAN1 - IF2 Data A2 Low	IF2DTA2L1	IF2DTA21	R/W
000851 _H	CAN1 - IF2 Data A2 High	IF2DTA2H1	-	R/W
000852 _H	CAN1 - IF2 Data B1 Low	IF2DTB1L1	IF2DTB11	R/W
000853 _H	CAN1 - IF2 Data B1 High	IF2DTB1H1	-	R/W
000854 _H	CAN1 - IF2 Data B2 Low	IF2DTB2L1	IF2DTB21	R/W
000855 _H	CAN1 - IF2 Data B2 High	IF2DTB2H1	-	R/W
000856 _H - 00087F _H	Reserved	-	-	-
000880 _H	CAN1 - Transmission Request 1 Register Low	TREQR1L1	TREQR11	R
000881 _H	CAN1 - Transmission Request 1 Register High	TREQR1H1	-	R
000882 _H	CAN1 - Transmission Request 2 Register Low	TREQR2L1	TREQR21	R

I/O Map CY96(F)38x (Sheet 30 of 30)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000883 _H	CAN1 - Transmission Request 2 Register High	TREQR2H1	-	R
000884 _H - 00088F _H	Reserved	-	-	-
000890 _H	CAN1 - New Data 1 Register Low	NEWDT1L1	NEWDT11	R
000891 _H	CAN1 - New Data 1 Register High	NEWDT1H1	-	R
000892 _H	CAN1 - New Data 2 Register Low	NEWDT2L1	NEWDT21	R
000893 _H	CAN1 - New Data 2 Register High	NEWDT2H1	-	R
000894 _H - 00089F _H	Reserved	-	-	-
0008A0 _H	CAN1 - Interrupt Pending 1 Register Low	INTPND1L1	INTPND11	R
0008A1 _H	CAN1 - Interrupt Pending 1 Register High	INTPND1H1	-	R
0008A2 _H	CAN1 - Interrupt Pending 2 Register Low	INTPND2L1	INTPND21	R
0008A3 _H	CAN1 - Interrupt Pending 2 Register High	INTPND2H1	-	R
0008A4 _H - 0008AF _H	Reserved	-	-	-
0008B0 _H	CAN1 - Message Valid 1 Register Low	MSGVAL1L1	MSGVAL11	R
0008B1 _H	CAN1 - Message Valid 1 Register High	MSGVAL1H1	-	R
0008B2 _H	CAN1 - Message Valid 2 Register Low	MSGVAL2L1	MSGVAL21	R
0008B3 _H	CAN1 - Message Valid 2 Register High	MSGVAL2H1	-	R
0008B4 _H - 0008CD _H	Reserved	-	-	-
0008CE _H	CAN1 - Output enable register	COER1	-	R/W
0008CF _H - 000BFF _H	Reserved	-	-	-

Note: Any write access to reserved addresses in the I/O map should not be performed. A read access to a reserved address results in reading 'X'.

Registers of resources which are described in this table, but which are not supported by the device, should also be handled as "Reserved".

13. Interrupt Vector Table

Interrupt Vector Table CY96(F)38x (Sheet 1 of 3)

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
0	3FC _H	CALLV0	No	-	
1	3F8 _H	CALLV1	No	-	
2	3F4 _H	CALLV2	No	-	
3	3F0 _H	CALLV3	No	-	
4	3EC _H	CALLV4	No	-	
5	3E8 _H	CALLV5	No	-	
6	3E4 _H	CALLV6	No	-	
7	3E0 _H	CALLV7	No	-	
8	3DC _H	RESET	No	-	
9	3D8 _H	INT9	No	-	
10	3D4 _H	EXCEPTION	No	-	
11	3D0 _H	NMI	No	-	Non-Maskable Interrupt
12	3CC _H	DLY	No	12	Delayed Interrupt
13	3C8 _H	RC_TIMER	No	13	RC Timer
14	3C4 _H	MC_TIMER	No	14	Main Clock Timer
15	3C0 _H	SC_TIMER	No	15	Sub Clock Timer
16	3BC _H	RESERVED	No	16	Reserved
17	3B8 _H	EXTINT0	Yes	17	External Interrupt 0
18	3B4 _H	EXTINT1	Yes	18	External Interrupt 1
19	3B0 _H	EXTINT2	Yes	19	External Interrupt 2
20	3AC _H	EXTINT3	Yes	20	External Interrupt 3
21	3A8 _H	EXTINT4	Yes	21	External Interrupt 4
22	3A4 _H	EXTINT5	Yes	22	External Interrupt 5
23	3A0 _H	EXTINT6	Yes	23	External Interrupt 6
24	39C _H	EXTINT7	Yes	24	External Interrupt 7
25	398 _H	CAN0	No	25	CAN Controller 0
26	394 _H	CAN1*	No	26	CAN Controller 1
27	390 _H	PPG0	Yes	27	Programmable Pulse Generator 0
28	38C _H	PPG1	Yes	28	Programmable Pulse Generator 1
29	388 _H	PPG2	Yes	29	Programmable Pulse Generator 2
30	384 _H	PPG3	Yes	30	Programmable Pulse Generator 3
31	380 _H	PPG4	Yes	31	Programmable Pulse Generator 4
32	37C _H	PPG5	Yes	32	Programmable Pulse Generator 5
33	378 _H	PPG6	Yes	33	Programmable Pulse Generator 6
34	374 _H	PPG7	Yes	34	Programmable Pulse Generator 7

Interrupt Vector Table CY96(F)38x (Sheet 2 of 3)

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
35	370 _H	RLT0	Yes	35	Reload Timer 0
36	36C _H	RLT1	Yes	36	Reload Timer 1
37	368 _H	RLT2	Yes	37	Reload Timer 2
38	364 _H	RLT3	Yes	38	Reload Timer 3
39	360 _H	PPGRLT	Yes	39	Reload Timer 6 - dedicated for PPG
40	35C _H	ICU0	Yes	40	Input Capture Unit 0
41	358 _H	ICU1	Yes	41	Input Capture Unit 1
42	354 _H	ICU2	Yes	42	Input Capture Unit 2
43	350 _H	ICU3	Yes	43	Input Capture Unit 3
44	34C _H	ICU4	Yes	44	Input Capture Unit 4
45	348 _H	ICU5	Yes	45	Input Capture Unit 5
46	344 _H	ICU6	Yes	46	Input Capture Unit 6
47	340 _H	ICU7	Yes	47	Input Capture Unit 7
48	33C _H	OCU0	Yes	48	Output Compare Unit 0
49	338 _H	OCU1	Yes	49	Output Compare Unit 1
50	334 _H	OCU2	Yes	50	Output Compare Unit 2
51	330 _H	OCU3	Yes	51	Output Compare Unit 3
52	32C _H	FRT0	Yes	52	Free Running Timer 0
53	328 _H	FRT1	Yes	53	Free Running Timer 1
54	324 _H	RTC0	No	54	Real Timer Clock
55	320 _H	CAL0	No	55	Clock Calibration Unit
56	31C _H	SG0	No	56	Sound Generator 0
57	318 _H	SG1	No	57	Sound Generator 1
58	314 _H	IIC0	Yes	58	I2C interface
59	310 _H	ADC0	Yes	59	A/D Converter
60	30C _H	ALARM0	No	60	Alarm Comparator 0
61	308 _H	ALARM1*	No	61	Alarm Comparator 1
62	304 _H	LINR0	Yes	62	LIN USART 0 RX
63	300 _H	LINT0	Yes	63	LIN USART 0 TX
64	2FC _H	LINR1	Yes	64	LIN USART 1 RX
65	2F8 _H	LINT1	Yes	65	LIN USART 1 TX
66	2F4 _H	LINR2	Yes	66	LIN USART 2 RX
67	2F0 _H	LINT2	Yes	67	LIN USART 2 TX
68	2EC _H	LINR4	Yes	68	LIN USART 4 RX
69	2E8 _H	LINT4	Yes	69	LIN USART 4 TX
70	2E4 _H	LINR5	Yes	70	LIN USART 5 RX
71	2E0 _H	LINT5	Yes	71	LIN USART 5 TX

Interrupt Vector Table CY96(F)38x (Sheet 3 of 3)

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
72	2DC _H	FLASH_A	No	72	Flash memory A (only Flash devices)
73	2D8 _H	FLASH_B	No	73	Flash memory B (only CY96F388/F389)

*: ALARM1 and CAN1 are not included on CY96384 and CY96(F)385 devices

14. Handling Devices

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage
- SMC power supply pins
- Serial communication

14.1 Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC} , $AVRH$) exceed the digital power-supply voltage.

14.2 Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register $PIER = 0$).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than $2\text{ k}\Omega$.

Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

14.3 External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration. See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

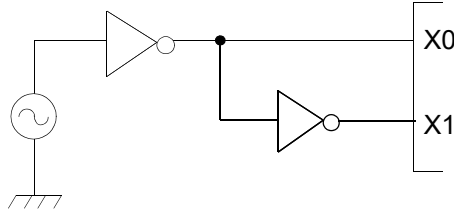
1. Single phase external clock

- When using a single phase external clock, X0 pin must be driven and X1 pin left open.



2. Opposite phase external clock

- When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.



14.4 Unused sub clock signal

If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

14.5 Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

14.6 Power supply pins (V_{CC}/V_{SS})

It is required that all V_{CC} -level as well as all V_{SS} -level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 μF between V_{CC} and V_{SS} as close as possible to V_{CC} and V_{SS} pins.

14.7 Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

14.8 Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC} , AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVRH or AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

14.9 Pin handling when not using the A/D converter

It is required to connect the unused pins of the A/D converter as $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = AVRL = V_{SS}$.

14.10 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50 μs from 0.2 V to 2.7 V.

14.11 Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the V_{CC} power supply voltage, a malfunction may occur. The V_{CC} power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that V_{CC} ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10% of the standard V_{CC} power supply voltage and the transient fluctuation rate becomes 0.1 $\text{V}/\mu\text{s}$ or less in instantaneous fluctuation for power supply switching.

14.12 SMC power supply pins

All DV_{SS} pins must be set to the same level as the V_{SS} pins.

The DV_{CC} power supply level can be set independently of the V_{CC} power supply level. However note that the SMC I/O pin state is undefined if DV_{CC} is powered on and V_{CC} is below 3 V. To avoid this, we recommend to always power V_{CC} before DV_{CC} .

14.13 Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

15. Electrical Characteristics

15.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}^{*1}$
AD Converter voltage references	AVRH, AVRL	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AVRH$, $AV_{CC} \geq AVRL$, $AVRH > AVRL$, $AVRL \geq AV_{SS}$
SMC Power supply	DV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	See *7
LCD power supply voltage	V0 to V3	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	V0 to V3 must not exceed V_{CC}
Input voltage	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_I \leq (D)V_{CC} + 0.3 V^{*2}$
Output voltage	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_O \leq (D)V_{CC} + 0.3 V^{*2}$
Maximum Clamp Current	I_{CLAMP}	-4.0	+4.0	mA	Applicable to general purpose I/O pins *3
Total Maximum Clamp Current	$\sum I_{CLAMP} $	-	40	mA	Applicable to general purpose I/O pins *3
"L" level maximum output current	I_{OL1}	-	15	mA	Normal outputs with driving strength set to 5mA
	I_{OLSMC}	-	40	mA	High current outputs with driving strength set to 30mA
"L" level average output current	I_{OLAV1}	-	5	mA	Normal outputs with driving strength set to 5mA
	$I_{OLAVSMC}$	-	30	mA	High current outputs with driving strength set to 30mA
"L" level maximum overall output current	$\sum I_{OL1}$	-	100	mA	Normal outputs
	$\sum I_{OLSMC}$	-	330	mA	High current outputs
"L" level average overall output current	$\sum I_{OLAV1}$	-	50	mA	Normal outputs
	$\sum I_{OLAVSMC}$	-	250	mA	High current outputs
"H" level maximum output current	I_{OH1}	-	-15	mA	Normal outputs with driving strength set to 5 mA
	I_{OHSMC}	-	-40	mA	High current outputs with driving strength set to 30 mA
"H" level average output current	I_{OHAV1}	-	-5	mA	Normal outputs with driving strength set to 5 mA
	$I_{OHAVSMC}$	-	-30	mA	High current outputs with driving strength set to 30 mA
"H" level maximum overall output current	$\sum I_{OH1}$	-	-100	mA	Normal outputs
	$\sum I_{OHSMC}$	-	-330	mA	High current outputs
"H" level average overall output current	$\sum I_{OHAV1}$	-	-50	mA	Normal outputs
	$\sum I_{OHASMC}$	-	-250	mA	High current outputs

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Permitted Power dissipation (CY96F385) *4	P _D	-	295 ^{*5}	mW	T _A =105°C
		-	595 ^{*5}	mW	T _A =85°C
		-	820 ^{*5}	mW	T _A =70°C
		-	370 ^{*5}	mW	T _A =125°C, no Flash program/erase *6
		-	670 ^{*5}	mW	T _A =105°C, no Flash program/erase *6
Permitted Power dissipation (CY96F386/F387/F388/F389) *4	P _D	-	370 ^{*5}	mW	T _A =105°C
		-	740 ^{*5}	mW	T _A =85°C
		-	1000 ^{*5}	mW	T _A =70°C
		-	460 ^{*5}	mW	T _A =125°C, no Flash program/erase *6
		-	800 ^{*5}	mW	T _A =105°C, no Flash program/erase *6
Permitted Power dissipation (CY96384/385) *4	P _D	-	310 ^{*5}	mW	T _A =105°C
		-	625 ^{*5}	mW	T _A =85°C
		-	800 ^{*5}	mW	T _A =70°C
		-	390 ^{*5}	mW	T _A =125°C *6
		-	700 ^{*5}	mW	T _A =105°C *6
Operating ambient temperature	T _A	0	+70	°C	CY96V300B
		-40	+105		
		-40	+125		*6
Storage temperature	T _{STG}	-55	+150	°C	

*1: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} neither when the power is switched on.

*2: V_I and V_O should not exceed (D)V_{CC} + 0.3 V. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of high current ports depend on DV_{CC}. Input/output voltages of standard ports depend on V_{CC}.

- *3:
- Applicable to all general purpose I/O pins (Pnn_m) except I/O pins with SEG or COM functionality.
 - Use within recommended operating conditions.
 - Use at DC voltage (current)
 - The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
 - The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
 - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
 - Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.

- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).
- No +B signal must be applied to any LCD I/O pin (including unused SEG/COM pins).
- Sample recommended circuits:



- *4: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
 The actual power dissipation depends on the customer application and can be calculated as follows:
 $P_D = P_{IO} + P_{INT}$
 $P_{IO} = \sum (V_{OL} * I_{OL} + V_{OH} * I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)
 $P_{INT} = V_{CC} * (I_{CC} + I_A)$ (internal power dissipation)
 I_{CC} is the total core current consumption into V_{CC} as described in the “DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming or the clock modulator.
 I_A is the analog current consumption into AV_{CC} .
- *5: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.
- *6: Please contact Cypress for reliability limitations when using under these conditions.
- *7: If DV_{CC} is powered before V_{CC} , then SMC I/O pins state is undefined. To avoid this, we recommend to always power V_{CC} before DV_{CC} . It is not necessary to set V_{CC} and DV_{CC} to the same value.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

15.2 Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, DV_{CC}	3.0	-	5.5	V	
Smoothing capacitor at C pin	C_S	3.5	4.7 - 10	15	μF	Use a low inductance capacitor (for example X7R ceramic capacitor)

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

15.3 DC characteristics
 $(T_A = -40^{\circ}\text{C to } 125^{\circ}\text{C}, V_{CC} = AV_{CC} = 3.0\text{V to } 5.5\text{V}, DV_{CC} = 3.0\text{V to } 5.5\text{V}, V_{SS} = AV_{SS} = DV_{SS} = 0\text{V})$

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IH}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	0.8 V_{CC}	-	(D) V_{CC} + 0.3	V	
			CMOS Hysteresis 0.7/0.3 input selected	0.7 V_{CC}	-	(D) V_{CC} + 0.3	V	(D) $V_{CC} \geq 4.5\text{ V}$
				0.74 V_{CC}	-	(D) V_{CC} + 0.3	V	(D) $V_{CC} < 4.5\text{ V}$
			AUTOMOTIVE Hysteresis input selected	0.8 V_{CC}	-	(D) V_{CC} + 0.3	V	
	TTL input selected	2.0	-	(D) V_{CC} + 0.3	V			
	V_{IHx0F}	X0	External clock in "Fast Clock Input mode"	0.8 V_{CC}	-	$V_{CC} +$ 0.3	V	Not available in CY96F386xxA/F387xxA
	V_{IHx0S}	X0,X1, X0A,X1A	External clock in "oscillation mode"	2.5	-	$V_{CC} +$ 0.3	V	
	V_{IHR}	RSTX	-	0.8 V_{CC}	-	$V_{CC} +$ 0.3	V	CMOS Hysteresis input
V_{IHM}	MD2-MD0	-	$V_{CC} -$ 0.3	-	$V_{CC} +$ 0.3	V		
Input L voltage	V_{IL}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	$V_{SS} -$ 0.3	-	0.2 (D) V_{CC}	V	
			CMOS Hysteresis 0.7/0.3 input selected	$V_{SS} -$ 0.3	-	0.3 (D) V_{CC}	V	
				AUTOMOTIVE Hysteresis input selected	$V_{SS} -$ 0.3	-	0.5 (D) V_{CC}	V
			$V_{SS} -$ 0.3		-	0.46 (D) V_{CC}		(D) $V_{CC} < 4.5\text{ V}$
			TTL input selected	$V_{SS} -$ 0.3	-	0.8	V	
	V_{ILx0F}	X0	External clock in "Fast Clock Input mode"	$V_{SS} -$ 0.3	-	0.2 V_{CC}	V	Not available in CY96F386xxA/F387xxA
	V_{ILx0S}	X0,X1, X0A,X1A	External clock in "oscillation mode"	$V_{SS} -$ 0.3	-	0.4	V	
	V_{ILR}	RSTX	-	$V_{SS} -$ 0.3	-	0.2 V_{CC}	V	CMOS Hysteresis input
V_{ILM}	MD2-MD0	-	$V_{SS} -$ 0.3	-	$V_{SS} +$ 0.3	V		

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $DV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = DV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output H voltage	V_{OH2}	Normal and High Current outputs	$4.5\text{ V} \leq (D)V_{CC} \leq 5.5\text{ V}$ $I_{OH} = -2\text{ mA}$	$(D)V_{CC} - 0.5$	-	-	V	Driving strength set to 2 mA
			$3.0\text{ V} \leq (D)V_{CC} < 4.5\text{ V}$ $I_{OH} = -1.6\text{ mA}$					
	V_{OH5}	Normal and High Current outputs	$4.5\text{ V} \leq (D)V_{CC} \leq 5.5\text{ V}$ $I_{OH} = -5\text{ mA}$	$(D)V_{CC} - 0.5$	-	-	V	Driving strength set to 5 mA
			$3.0\text{ V} \leq (D)V_{CC} < 4.5\text{ V}$ $I_{OH} = -3\text{ mA}$					
V_{OH30}	High current outputs	$4.5\text{ V} \leq DV_{CC} \leq 5.5\text{ V}$ $I_{OH} = -30\text{ mA}$	$DV_{CC} - 0.5$	-	-	V	Driving strength set to 30 mA	
		$3.0\text{ V} \leq DV_{CC} < 4.5\text{ V}$ $I_{OH} = -20\text{ mA}$						
V_{OH3}	3mA outputs	$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ $I_{OH} = -3\text{ mA}$	$V_{CC} - 0.5$	-	-	V		
		$3.0\text{ V} \leq V_{CC} < 4.5\text{ V}$ $I_{OH} = -2\text{ mA}$						

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $DV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = DV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output L voltage	V_{OL2}	Normal and High Current outputs	$4.5\text{ V} \leq (D)V_{CC} \leq 5.5\text{ V}$ $I_{OL} = +2\text{ mA}$	-	-	0.4	V	Driving strength set to 2 mA
			$3.0\text{ V} \leq (D)V_{CC} < 4.5\text{ V}$ $I_{OL} = +1.6\text{ mA}$					
	V_{OL5}	Normal and High Current outputs	$4.5\text{ V} \leq (D)V_{CC} \leq 5.5\text{ V}$ $I_{OL} = +5\text{ mA}$	-	-	0.4	V	Driving strength set to 5 mA
			$3.0\text{ V} \leq (D)V_{CC} < 4.5\text{ V}$ $I_{OL} = +3\text{ mA}$					
V_{OL30}	High current outputs	$4.5\text{ V} \leq DV_{CC} \leq 5.5\text{ V}$ $I_{OL} = +30\text{ mA}$	-	-	0.5	V	Driving strength set to 30 mA	
		$3.0\text{ V} \leq DV_{CC} < 4.5\text{ V}$ $I_{OL} = +20\text{ mA}$						
V_{OL3}	3mA outputs	$3.0\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ $I_{OL} = +3\text{ mA}$	-	-	0.4	V		
Input leak current	I_{IL}	Pnn_m	$V_{SS} < V_I < V_{CC}$ $AV_{SS}, AV_{RL} < V_I < AV_{CC}, AV_{RH}$	-1	-	+1	μA	Single port pin
Total LCD leak current	$\sum I_{LCD} $	all SEG/COM pins	$V_{CC} = 5.0\text{ V}$	-	0.5	10	μA	Maximum leakage current of all LCD pins
Internal LCD divide resistance	R_{LCD}	Between V3 and V_{SS}	$V_{CC} = 5.0\text{ V}$	25	40	65	$\text{k}\Omega$	
Pull-up resistance	R_{UP}	Pnn_m, RSTX	$V_{CC} = 3.3\text{ V} \pm 10\%$	40	100	160	$\text{k}\Omega$	
			$V_{CC} = 5.0\text{ V} \pm 10\%$	25	50	100	$\text{k}\Omega$	

Note: Input/output voltages of high current ports depend on DV_{CC} , of other ports on V_{CC} .

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $DV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = DV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)	Value			Remarks	
			Typ	Max	Unit		
Power supply current in Run modes*	I_{CCPLL}	PLL Run mode with CLKS1/2 = 48 MHz, CLKB = CLKP1/2 = 24 MHz (CLKRC and CLKSC stopped. Core voltage at 1.9 V)	+25°C	35	44	mA	CY96F385/F386/F387 at 0 Flash wait states
			+125°C	36	47		
			+25°C	38	46	mA	CY96F388/F389 at 0 Flash wait states
			+125°C	39	49		
			+25°C	16	22	mA	CY96384/385 at 0 ROM wait states
			+125°C	17	23.5		
		PLL Run mode with CLKS1/2 = CLKB = CLKP1 = 56 MHz, CLKP2 = 28 MHz (CLKRC and CLKSC stopped. Core voltage at 1.9 V)	+25°C	44	57	mA	CY96F386/F387 at 2 Flash wait states
			+125°C	45	60		
			+25°C	24	34	mA	CY96384/385 at 2 ROM wait states
			+125°C	25	35.5		
		PLL Run mode with CLKS1/2 = 72 MHz, CLKB = CLKP1 = 36 MHz, CLKP2 = 18 MHz (CLKRC and CLKSC stopped. Core voltage at 1.9 V)	+25°C	38	50	mA	CY96F386/F387 at 1 Flash wait state
			+125°C	39	53		
		PLL Run mode with CLKS1/2 = 80 MHz, CLKB = CLKP1 = 40 MHz, CLKP2 = 20 MHz (CLKRC and CLKSC stopped. Core voltage at 1.9 V)	+25°C	43	55	mA	CY96F385 at 1 Flash wait state
			+125°C	44	57		
			+25°C	48	60	mA	CY96F388/F389 at 1 Flash wait state
			+125°C	49	63		
		PLL Run mode with CLKS1/2 = 96 MHz, CLKB = CLKP1 = 48 MHz, CLKP2 = 24 MHz (CLKRC and CLKSC stopped. Core voltage at 1.9 V)	+25°C	25	35	mA	CY96384/385 at 1 ROM wait state
			+125°C	26	36.5		

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Condition (at T _A)	Value			Remarks	
			Typ	Max	Unit		
Power supply current in Run modes*	I _{CCMAIN}	Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4 MHz (CLKPLL, CLKSC and CLKRC stopped)	+25°C	4.5	5.5	mA	CY96F385 at 1 Flash wait state
			+125°C	5.1	7.5		
			+25°C	4.5	5.5	mA	CY96F386/F387 at 1 Flash wait state
			+125°C	5.1	8.5		
			+25°C	4.8	6	mA	CY96F388/F389 at 1 Flash wait state
			+125°C	5.4	8.5		
			+25°C	2.5	3.5	mA	CY96384/385 at 1 ROM wait state
			+125°C	3.1	5		
	I _{CCRCH}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 2 MHz (CLKMC, CLKPLL and CLKSC stopped)	+25°C	2.5	3.6	mA	CY96F385 at 1 Flash wait state
			+125°C	3.1	5.1		
			+25°C	2.9	4	mA	CY96F386/F387/F388/F389 at 1 Flash wait state
			+125°C	3.5	6.5		
			+25°C	1.7	2.7	mA	CY96384/385 at 1 ROM wait state
			+125°C	2.3	4.2		
	I _{CCRCL}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100 kHz, SMCR:LPMS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.4	0.6	mA	CY96F386/F387 at 1 Flash wait state
			+125°C	0.9	3.5		
			+25°C	0.4	0.6		CY96F388/F389 at 1 Flash wait state
			+125°C	0.9	2.9		
			+25°C	0.4	0.6		CY96384/385/F385 at 1 ROM/Flash wait state
			+125°C	0.9	2		
		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100 kHz, SMCR:LPMS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/ erasing allowed)	+25°C	0.15	0.25	mA	CY96F386/F387 at 1 Flash wait state
			+125°C	0.65	3.2		
			+25°C	0.15	0.25	mA	CY96F388/F389 at 1 Flash wait state
			+125°C	0.65	2.6		
+25°C			0.15	0.25	mA	CY96384/385/F385 at 1 ROM/Flash wait state	
+125°C			0.65	1.75			

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $DV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = DV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)	Value			Remarks	
			Typ	Max	Unit		
Power supply current in Run modes*	I_{CCSUB}	Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32 kHz (CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing allowed)	+25°C	0.1	0.2	mA	CY96F386/F387 at 1 Flash wait state
			+125°C	0.6	3		
			+25°C	0.1	0.2	mA	CY96F388/F389 at 1 Flash wait state
			+125°C	0.6	2.4		
			+25°C	0.1	0.2	mA	CY96384/385/F385 at 1 ROM/Flash wait state
			+125°C	0.6	1.7		

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $DV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = DV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes*	I_{CCSPLL}		+25°C	7.5	9	mA	CY96F385
			+125°C	8.2	10.5		
		PLL Sleep mode with CLKS1/2 = 48 MHz, CLKP1/2 = 24 MHz (CLKRC and CLKSC stopped. Core voltage at 1.9 V)	+25°C	9	10.5	mA	CY96F386/F387
			+125°C	9.7	13		
			+25°C	11	13	mA	CY96F388/F389
			+125°C	11.7	15.5		
			+25°C	7	8.5	mA	CY96384/385
			+125°C	7.7	10		
		PLL Sleep mode with CLKS1/2 = CLKP1 = 56 MHz, CLKP2 = 28 MHz (CLKRC and CLKSC stopped. Core voltage at 1.9 V)	+25°C	14	15.5	mA	CY96F386/F387
			+125°C	14.8	18		
			+25°C	12	13.5	mA	CY96384/385
			+125°C	12.8	15		
		PLL Sleep mode with CLKS1/2 = 72 MHz, CLKP1 = 36 MHz, CLKP2 = 18 MHz (CLKRC and CLKSC stopped. Core voltage at 1.9 V)	+25°C	10.5	12	mA	CY96F386/F387
			+125°C	11.3	14.5		
		PLL Sleep mode with CLKS1/2 = 80 MHz, CLKP1 = 40 MHz, CLKP2 = 20 MHz (CLKRC and CLKSC stopped. Core voltage at 1.9 V)	+25°C	14	17	mA	CY96F388/F389
			+125°C	14.8	19.5		
		PLL Sleep mode with CLKS1/2 = 96 MHz, CLKP1 = 48 MHz, CLKP2 = 24 MHz (CLKRC and CLKSC stopped. Core voltage at 1.9 V)	+25°C	13	14.5	mA	CY96384/385/F385
			+125°C	13.8	16		

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $DV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = DV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes*	$I_{CCSM\text{AIN}}$	Main Sleep mode with $\text{CLKS1/2} = \text{CLKP1/2} = 4\text{ MHz}$ (CLKPLL, CLKSC and CLKRC stopped)	+25°C	1.5	1.8	mA	CY96F386/F387
			+125°C	2	4.5		
			+25°C	1.6	2	mA	CY96F388/F389
			+125°C	2.1	4.2		
			+25°C	1.5	1.8	mA	CY96384/385/F385
			+125°C	2	3.3		
	$I_{CCSR\text{CH}}$	RC Sleep mode with $\text{CLKS1/2} = \text{CLKP1/2} = 2\text{ MHz}$ (CLKMC, CLKPLL and CLKSC stopped)	+25°C	0.9	1.4	mA	CY96F386/F387
			+125°C	1.5	4		
			+25°C	0.9	1.4	mA	CY96F388/F389
			+125°C	1.5	3.5		
			+25°C	0.9	1.4	mA	CY96384/385/F385
			+125°C	1.5	2.8		

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $DV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = DV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes*	I_{CCSRCL}	RC Sleep mode with $CLKS1/2 = CLKP1/2 = 100\text{ kHz}$, $SMCR:LPMSS = 0$ (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.3	0.5	mA	CY96F386/F387
			+125°C	0.8	3.4		
			+25°C	0.3	0.5	mA	CY96F388/F389
			+125°C	0.8	2.8		
			+25°C	0.3	0.5	mA	CY96384/385/F385
			+125°C	0.8	2		
	I_{CCSRCL}	RC Sleep mode with $CLKS1/2 = CLKP1/2 = 100\text{ kHz}$, $SMCR:LPMSS = 1$ (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.06	0.15	mA	CY96F386/F387
			+125°C	0.56	3		
			+25°C	0.06	0.15	mA	CY96F388/F389
			+125°C	0.56	2.4		
			+25°C	0.06	0.15	mA	CY96384/385/F385
			+125°C	0.56	1.6		
I_{CCSSUB}	Sub Sleep mode with $CLKS1/2 = CLKP1/2 = 32\text{ kHz}$ (CLKMC, CLKPLL and CLKRC stopped)	+25°C	0.04	0.12	mA	CY96F386/F387	
		+125°C	0.54	2.9			
		+25°C	0.04	0.12	mA	CY96F388/F389	
		+125°C	0.54	2.3			
		+25°C	0.04	0.12	mA	CY96384/385/F385	
		+125°C	0.54	1.55			
Power supply current in Timer modes*	I_{CCTPLL}	PLL Timer mode with $CLKMC = 4\text{MHz}$, $CLKPLL = 48\text{ MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9 V)	+25°C	1.6	2	mA	CY96F386/F387
			+125°C	2.1	4.8		
			+25°C	1.6	2	mA	CY96F388/F389
			+125°C	2.1	4.2		
			+25°C	1.6	2	mA	CY96384/385/F385
			+125°C	2.1	3.5		

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $DV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = DV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks	
				Typ	Max	Unit		
Power supply current in Timer modes*	$I_{CCTMAIN}$	Main Timer mode with CLKMC = 4 MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.35	0.5	mA	CY96F386/F387	
			+125°C	0.85	3.3			
			+25°C	0.35	0.5	mA		CY96F388/F389
			+125°C	0.85	2.7			
			+25°C	0.35	0.5	mA		CY96384/385/F385
			+125°C	0.85	2			
		Main Timer mode with CLKMC = 4 MHz, SMCR:LPMSS = 1 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.1	0.15	mA	CY96F386/F387	
			+125°C	0.6	2.9			
			+25°C	0.1	0.15	mA	CY96F388/F389	
			+125°C	0.6	2.3			
			+25°C	0.1	0.18		CY96384/385/F385	
			+125°C	0.6	1.6			
	I_{CCTRCH}	RC Timer mode with CLKRC = 2 MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.35	0.5	mA	CY9CY96F386/F387	
			+125°C	0.85	3.3			
			+25°C	0.35	0.5	mA	CY96F388/F389	
			+125°C	0.85	2.7			
			+25°C	0.35	0.5	mA	CY96384/385/F385	
			+125°C	0.85	2			
		RC Timer mode with CLKRC = 2 MHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.1	0.15	mA	CY96F386/F387	
			+125°C	0.6	2.9			
			+25°C	0.1	0.15	mA	CY96F388/F389	
			+125°C	0.6	2.3			
			+25°C	0.1	0.15	mA	CY96384/385/F385	
			+125°C	0.6	1.6			

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $DV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = DV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Timer modes*	I_{CCTRCL}	RC Timer mode with CLKRC = 100 kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.3	0.45	mA	CY96F386/F387
			+125°C	0.8	3.2		
			+25°C	0.3	0.45	mA	CY96F386/F387
			+125°C	0.8	2.6		
			+25°C	0.3	0.45	mA	CY96384/385/F385
			+125°C	0.8	1.95		
		RC Timer mode with CLKRC = 100 kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.05	0.1	mA	CY96F386/F387
			+125°C	0.55	2.8		
			+25°C	0.05	0.1	mA	CY96F388/F389
			+125°C	0.55	2.2		
	I_{CCTSUB}	Sub Timer mode with CLKSC = 32 kHz (CLKMC, CLKPLL and CLKRC stopped)	+25°C	0.03	0.1	mA	CY96F386/F387
			+125°C	0.53	2.8		
			+25°C	0.03	0.1	mA	CY96F388/F389
			+125°C	0.53	2.2		
+25°C			0.03	0.1	mA	CY96384/385/F385	
+125°C			0.53	1.55			

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $DV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = DV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Stop Mode	I_{CCH}	VRCR:LPMB[2:0] = 110 _B (Core voltage at 1.8 V)	+25°C	0.02	0.08	mA	CY96F386/F387
			+125°C	0.52	2.8		
			+25°C	0.02	0.08	mA	CY96F388/F389
			+125°C	0.52	2.2		
			+25°C	0.02	0.08	mA	CY96384/385/F385
			+125°C	0.52	1.5		
		VRCR:LPMB[2:0] = 000 _B (Core voltage at 1.2 V)	+25°C	0.015	0.06	mA	CY96F386/F387
			+125°C	0.4	2.3		
			+25°C	0.015	0.06	mA	CY96F388/F389
			+125°C	0.4	1.65		
			+25°C	0.015	0.06	mA	CY96384/385/F385
			+125°C	0.4	1.2		
Power supply current for active Low Voltage detector	I_{CCLVD}	Low voltage detector enabled (RCR:LVDE = 1)	+25°C	90	140	μA	This current must be added to all Power supply currents above
			+125°C	100	150		
Power supply current for active Clock modulator	I_{CCLOMO}	Clock modulator enabled (CM-CR:PDX = 1)	-	3	4.5	mA	Must be added to all current above
Flash Write/Erase current	$I_{CCFLASH}$	Current for one Flash module	-	15	40	mA	Must be added to all current above
Input capacitance	C_{IN}	-		15	30	pF	High current outputs
Input capacitance	C_{IN}	-	-	5	15	pF	Other than C, AV_{CC} , AV_{SS} , $AVRH$, $AVRL$, V_{CC} , V_{SS} , DV_{CC} , DV_{SS} , High current outputs

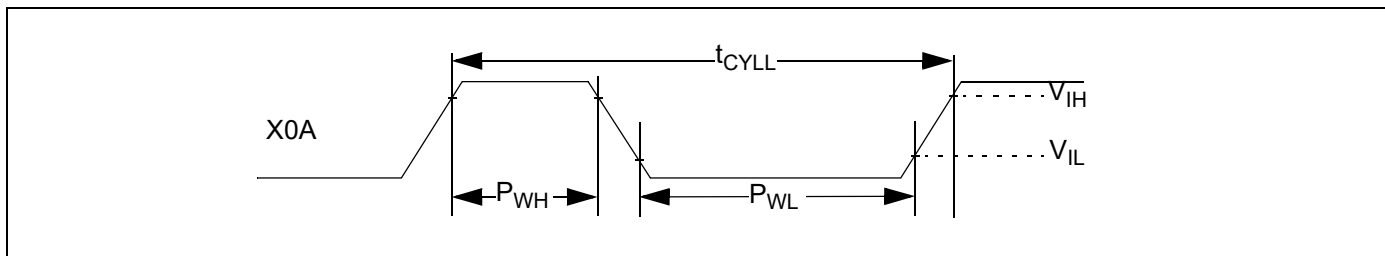
*: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32 kHz external clock connected to the Sub oscillator. See chapter "Standby mode and voltage regulator control circuit" of the Hardware Manual for further details about voltage regulator control.

15.4 AC Characteristics

Source Clock Timing

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $DV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = DV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	-	16	MHz	When using a crystal oscillator, PLL off
			0	-	16	MHz	When using an opposite phase external clock, PLL off
			3.5	-	16	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Clock frequency	f_{FCI}	X0	0	-	56	MHz	When using a single phase external clock in "Fast Clock Input mode" (not available in CY96F386xxA and CY96F387xxA), PLL off
			3.5	-	56	MHz	When using a single phase external clock in "Fast Clock Input mode" (not available in CY96F386xxA and CY96F387xxA), PLL on
Clock frequency	f_{CL}	X0A, X1A	32	32.768	100	kHz	When using an oscillation circuit
			0	-	100	kHz	When using an opposite phase external clock
		X0A	0	-	50	kHz	When using a single phase external clock
Clock frequency	f_{CR}	-	50	100	200	kHz	When using slow frequency of RC oscillator
			1	2	4	MHz	When using fast frequency of RC oscillator
PLL Clock frequency	f_{CLKVCO}	-	64	-	200	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL Phase Jitter	T_{PSKEW}	-	-	-	± 5	ns	For CLKMC (PLL input clock) ≥ 4 MHz
Input clock pulse width	P_{WH}, P_{WL}	X0,X1	8	-	-	ns	Duty ratio is about 30% to 70%
Input clock pulse width	P_{WHL}, P_{WLL}	X0A,X1A	5	-	-	μs	



Internal Clock Timing

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $DV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = DV_{SS} = 0\text{V}$)

Parameter	Symbol	Core Voltage Settings				Unit	Remarks
		1.8 V		1.9 V			
		Min	Max	Min	Max		
Internal System clock frequency (CLKS1 and CLKS2)	$f_{\text{CLKS1}}, f_{\text{CLKS2}}$	0	92	0	96	MHz	Others than below
		0	72	0	80	MHz	CY96F385/F388/F389
		0	68	0	74	MHz	CY96F386/F387
Internal CPU clock frequency (CLKB), internal peripheral clock frequency (CLKP1)	$f_{\text{CLKB}}, f_{\text{CLKP1}}$	0	52	0	56	MHz	Others than below
		0	36	0	40	MHz	CY96F385/F388/F389
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	0	28	0	32	MHz	Others than below
		0	26	0	28	MHz	CY96F386/F387

External Reset Timing

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $DV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = DV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Reset input time	t_{RSTL}	RSTX	500	-	-	ns	



Power On Reset Timing

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $DV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = DV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t_R	Vcc	0.05	-	30	ms	
Power off time	t_{OFF}	Vcc	1	-	-	ms	



If the power supply is changed too rapidly, a power-on reset may occur. We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.

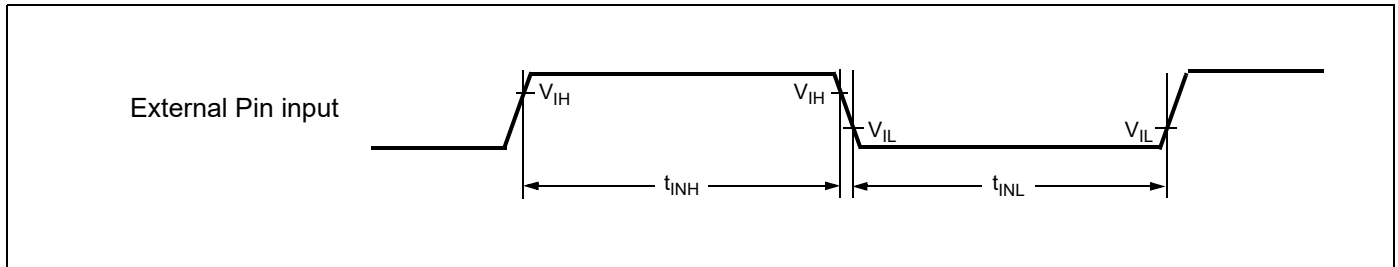


External Input Timing

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $DV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = DV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Used Pin input function
				Min	Max		
Input pulse width	t_{INH} t_{INL}	INTn(_R)	—	200	—	ns	External Interrupt
		NMI(_R)					NMI
		Pnn_m		$2 \cdot t_{CLKP1} + 200$ ($t_{CLKP1} = 1/f_{CLKP1}$)	—	ns	General Purpose IO
		TINn(_R)					Reload Timer
		TTGn(_R)					PPG Trigger input
		ADTG(_R)					AD Converter Trigger
		FRCKn(_R)					Free Running Timer external clock
		INn(_R)					Input Capture

Note : Relocated Resource Inputs have same characteristics

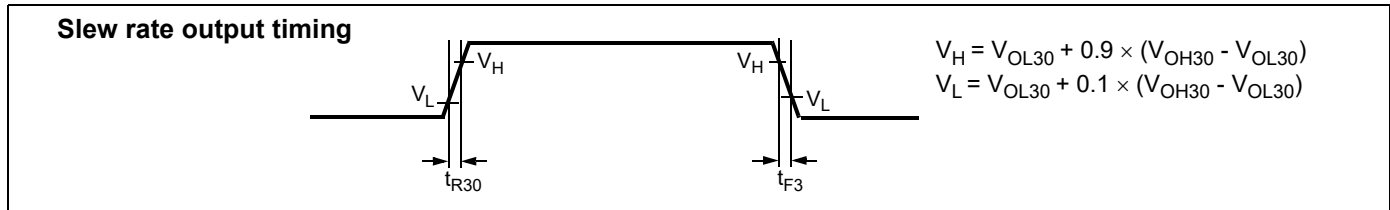


Slew Rate High Current Outputs

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $DV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = DV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Output rise/fall time	t_{R30} t_{F30}	I/O circuit type M	Output driving strength set to "30 mA"	15	—	ns	

Note : Relocated Resource Inputs have same characteristics



External Bus Timing

Note: The values given below are for an I/O driving strength $IO_{drive} = 5\text{ mA}$. If IO_{drive} is 2 mA, all the maximum output timing described in the different tables must then be increased by 10 ns.

Basic Timing

($T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $IO_{drive} = 5\text{ mA}$, $C_L = 50\text{ pF}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	—	25	—	ns	
	t_{CHCL}			$t_{CYC}/2-5$	$t_{CYC}/2+5$		
	t_{CLCH}			$t_{CYC}/2-5$	$t_{CYC}/2+5$		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	—	-20	20	ns	
	t_{CHCBL}			-20	20		
	t_{CLCBH}			-20	20		
	t_{CLCBL}			-20	20		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	—	-10	10	ns	
	t_{CHLL}			-10	10		
	t_{CLLH}			-10	10		
	t_{CLLL}			-10	10		
ECLK → address valid time (non-multiplexed)	t_{CHAV}	A[23:0], ECLK	EBM:NMS=1	-15	15	ns	
	t_{CLAV}			-15	15		
ECLK → address valid time (multiplexed)	t_{CHAV}	A[23:16], ECLK	EBM:NMS=0	-15	15	ns	
	t_{CLAV}			-15	15		
	t_{CLADV}	AD[15:0], ECLK	EBM:NMS=0	-15	15	ns	
	t_{CHADV}			-15	15		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX, WRHX, ECLK	—	-10	10	ns	
	t_{CHRWL}			-10	10		
	t_{CLRWH}			-10	10		
	t_{CLRWL}			-10	10		

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	—	30	—	ns	
	t_{CHCL}			$t_{CYC}/2-8$	$t_{CYC}/2+8$		
	t_{CLCH}			$t_{CYC}/2-8$	$t_{CYC}/2+8$		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	—	-25	25	ns	
	t_{CHCBL}			-25	25		
	t_{CLCBH}			-25	25		
	t_{CLCBL}			-25	25		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	—	-15	15	ns	
	t_{CHLL}			-15	15		
	t_{CLLH}			-15	15		
	t_{CLLL}			-15	15		
ECLK → address valid time (non-multiplexed)	t_{CHAV}	A[23:0], ECLK	EBM:NMS=1	-20	20	ns	
	t_{CLAV}			-20	20		
ECLK → address valid time (multiplexed)	t_{CHAV}	A[23:16], ECLK	EBM:NMS=0	-20	20	ns	
	t_{CLAV}			-20	20		
	t_{CLADV}	AD[15:0], ECLK	EBM:NMS=0	-20	20	ns	
	t_{CHADV}			-20	20		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX, WRHX, ECLK	—	-15	15	ns	
	t_{CHRWL}			-15	15		
	t_{CLRWH}			-15	15		
	t_{CLRWL}			-15	15		



Bus Timing (Read)
 $(T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}, V_{CC} = 5.0\text{ V} \pm 10\%, V_{SS} = 0.0\text{ V}, I_{Odrive} = 5\text{mA}, C_L = 50\text{pF})$

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width (multiplexed)	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 5$	—	ns	EBM:NMS = 0
			EACL:STS=1	$t_{CYC} - 5$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 5$	—		
Valid address ⇒ ALE ↓ time (multiplexed)	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 15$	—	ns	
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 15$	—		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 15$	—		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 15$	—		
	t_{ADVLL}	ALE, AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 15$	—	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 15$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 15$	—		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 15$	—		
ALE ↓ ⇒ Address valid time (multiplexed)	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 15$	—	ns	
			EACL:STS=1	-15	—		
Valid address ⇒ RDX ↓ time (non-multiplexed)	t_{AVRL}	RDX, A[23:0]	EBM:NMS= 1	$t_{CYC}/2 - 15$	—	ns	
Valid address ⇒ RDX ↓ time (multiplexed)	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0 EBM:NMS=0	$3t_{CYC}/2 - 15$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$5t_{CYC}/2 - 15$	—		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0 EBM:NMS=0	$t_{CYC} - 15$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$2t_{CYC} - 15$	—		
Valid address ⇒ Valid data input (non-multiplexed)	t_{AVDV}	A[23:0], AD[15:0]	EBM:NMS= 1	—	$2t_{CYC} - 55$	ns	w/o cycle extension

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ Valid data input (multiplexed)	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0 EBM:NMS=0	—	$3t_{CYC} - 55$	ns	w/o cycle extension
			EACL:ACE=1 EBM:NMS=0	—	$4t_{CYC} - 55$		
	$t_{ADV DV}$	AD[15:0]	EACL:ACE=0 EBM:NMS=0	—	$5t_{CYC}/2 - 55$	ns	w/o cycle extension
			EACL:ACE=1 EBM:NMS=0	—	$7t_{CYC}/2 - 55$		
RDX pulse width	t_{RLRH}	RDX	—	$3 t_{CYC}/2 - 5$	—	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	—	—	$3 t_{CYC}/2 - 50$	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	—	0	—	ns	
Address valid ⇒ Data hold time	t_{AXDX}	A[23:0], AD[15:0]	—	0	—	ns	
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 10$	—	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 - 10$	—		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:0], ECLK	—	$t_{CYC} - 15$	—	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYC}/2 - 15$	—		
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, ECLK	—	$t_{CYC}/2 - 10$	—	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 10$	—	ns	
			EACL:STS=1	- 10	—		
ECLK ↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	—	—	$t_{CYC} - 50$	ns	

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width (multiplexed)	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 8$	—	ns	EBM:NMS = 0
			EACL:STS=1	$t_{CYC} - 8$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 8$	—		
Valid address ⇒ ALE ↓ time (multiplexed)	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 20$	—	ns	
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 20$	—		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 20$	—		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 20$	—		
	t_{ADVLL}	ALE, AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 20$	—	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 20$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 20$	—		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 20$	—		
ALE ↓ ⇒ Address valid time (multiplexed)	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 20$	—	ns	
			EACL:STS=1	-20	—		
Valid address ⇒ RDX ↓ time (non-multiplexed)	t_{AVRL}	RDX, A[23:0]	EBM:NMS= 1	$t_{CYC}/2 - 20$	—	ns	
Valid address ⇒ RDX ↓ time (multiplexed)	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0 EBM:NMS=0	$3t_{CYC}/2 - 20$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$5t_{CYC}/2 - 20$	—		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0 EBM:NMS=0	$t_{CYC} - 20$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$2t_{CYC} - 20$	—		
Valid address ⇒ Valid data input (non-multiplexed)	t_{AVDV}	A[23:0], AD[15:0]	EBM:NMS= 1	—	$2t_{CYC} - 60$	ns	w/o cycle extension

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ Valid data input (multiplexed)	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0 EBM:NMS=0	—	$3t_{CYC} - 60$	ns	w/o cycle extension
			EACL:ACE=1 EBM:NMS=0	—	$4t_{CYC} - 60$		
	t_{AD-VDV}	AD[15:0]	EACL:ACE=0 EBM:NMS=0	—	$5t_{CYC}/2 - 60$	ns	w/o cycle extension
			EACL:ACE=1 EBM:NMS=0	—	$7t_{CYC}/2 - 60$		
RDX pulse width	t_{RLRH}	RDX	—	$3t_{CYC}/2 - 8$	—	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	—	—	$3t_{CYC}/2 - 55$	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	—	0	—	ns	
Address valid ⇒ Data hold time	t_{AXDX}	A[23:0]	—	0	—	ns	
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 15$	—	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 - 15$	—		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:0], ECLK	—	$t_{CYC} - 20$	—	ns	
	t_{AD-VCH}	AD[15:0], ECLK		$t_{CYC}/2 - 20$	—		
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, ECLK	—	$t_{CYC}/2 - 15$	—	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 15$	—	ns	
			EACL:STS=1	- 15	—		
ECLK ↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	—	—	$t_{CYC} - 55$	ns	

Bus Timing (Write)
 $(T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}, V_{CC} = 5.0\text{ V} \pm 10\%, V_{SS} = 0.0\text{ V}, I_{Odrive} = 5\text{mA}, C_L = 50\text{pF})$

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ WRX ↓ time (non-multiplexed)	t_{AVWL}	WRX, WRLX, WRHX, A[23:0]	EACL:STS=0 EBM:NMS=1	$t_{CYC}/2 - 15$	—	ns	
			EACL:STS=1 EBM:NMS=1	$t_{CYC} - 15$	—		
Valid address ⇒ WRX ↓ time (multiplexed)	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0 EBM:NMS=0	$3t_{CYC}/2 - 15$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$5t_{CYC}/2 - 15$	—		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0 EBM:NMS=0	$t_{CYC} - 15$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$2t_{CYC} - 15$	—		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	—	$t_{CYC} - 5$	—	ns	w/o cycle extension
Valid data output ⇒ WRX ↑ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	—	$t_{CYC} - 20$	—	ns	w/o cycle extension
WRX ↑ ⇒ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	—	$t_{CYC}/2 - 15$	—	ns	
WRX ↑ ⇒ Address valid time (non-multiplexed)	t_{WHAX}	WRX, WRLX, WRHX, A[23:0]	EACL:STS=1 EBM:NMS=1	- 15	—	ns	
			EACL:STS=0 EBM:NMS=1	$t_{CYC}/2 - 15$	—	ns	
WRX ↑ ⇒ Address valid time (multiplexed)	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	EBM:NMS=0	$t_{CYC}/2 - 15$	—	ns	
WRX ↑ ⇒ ALE ↑ time (multiplexed)	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC} - 10$	—	ns	EBM:NMS=0
			other EBM:ACE and EACL:STS setting	$t_{CYC} - 10$	—		
WRX ↓ ⇒ ECLK ↑ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	—	$t_{CYC}/2 - 10$	—	ns	
CSn ⇒ WRX time (non-multiplexed)	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:STS=0 EBM:NMS=1	—	$t_{CYC}/2 - 15$	ns	
			EACL:STS=1 EBM:NMS=1	—	$t_{CYC} - 15$		
CSn ⇒ WRX time (multiplexed)	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0 EBM:NMS=0	—	$3t_{CYC}/2 - 15$	ns	
			EACL:ACE=1 EBM:NMS=0	—	$5t_{CYC}/2 - 15$		

$(T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}, V_{CC} = 5.0\text{ V} \pm 10\%, V_{SS} = 0.0\text{ V}, I_{Odrive} = 5\text{ mA}, C_L = 50\text{ pF})$

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
WRX \Rightarrow CSn time (non-multiplexed)	t_{WHCSH}	WRX, WRLX, WRHX, CSn	EACL:STS=1 EBM:NMS=1	- 15	—	ns	
			EACL:STS=0 EBM:NMS=1	$t_{CYC}/2 - 15$	—	ns	
WRX \Rightarrow CSn time (multiplexed)	t_{WHCSH}	WRX, WRLX, WRHX, CSn	EBM:NMS=0	$t_{CYC}/2 - 15$	—	ns	

 $(T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}, V_{CC} = 3.0\text{ to } 4.5\text{ V}, V_{SS} = 0.0\text{ V}, I_{Odrive} = 5\text{ mA}, C_L = 50\text{ pF})$

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address \Rightarrow WRX \downarrow time (non-multiplexed)	t_{AVWL}	WRX, WRLX, WRHX, A[23:0]	EACL:STS=0 EBM:NMS=1	$t_{CYC}/2 - 20$	—	ns	
			EACL:STS=1 EBM:NMS=1	$t_{CYC} - 20$	—		
Valid address \Rightarrow WRX \downarrow time (multiplexed)	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0 EBM:NMS=0	$3t_{CYC}/2 - 20$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$5t_{CYC}/2 - 20$	—		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0 EBM:NMS=0	$t_{CYC} - 20$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$2t_{CYC} - 20$	—		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	—	$t_{CYC} - 8$	—	ns	w/o cycle extension
Valid data output \Rightarrow WRX \uparrow time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	—	$t_{CYC} - 25$	—	ns	w/o cycle extension
WRX \uparrow \Rightarrow Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	—	$t_{CYC}/2 - 20$	—	ns	
WRX \uparrow \Rightarrow Address valid time (non-multiplexed)	t_{WHAX}	WRX, WRLX, WRHX, A[23:0]	EACL:STS=1 EBM:NMS=1	- 20	—	ns	
			EACL:STS=0 EBM:NMS=1	$t_{CYC}/2 - 20$	—	ns	
WRX \uparrow \Rightarrow Address valid time (multiplexed)	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	EBM:NMS=0	$t_{CYC}/2 - 20$	—	ns	
WRX $\uparrow \Rightarrow$ ALE \uparrow time (multiplexed)	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC} - 15$	—	ns	EBM:NMS=0
			other EBM:ACE and EACL:STS setting	$t_{CYC} - 15$	—		
WRX $\downarrow \Rightarrow$ ECLK \uparrow time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	—	$t_{CYC}/2 - 15$	—	ns	

Ready Input Timing

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	35	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.



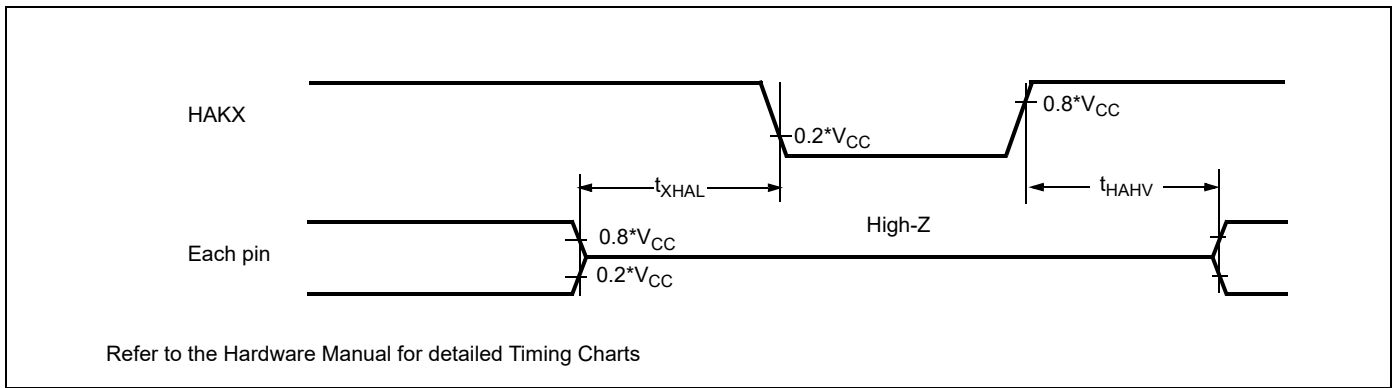
Hold Timing

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{ mA}$, $C_L = 50\text{ pF}$)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating \Rightarrow HAKX \downarrow time	t_{XHAL}	HAKX	—	$t_{CYC} - 20$	$t_{CYC} + 20$	ns	
HAKX \uparrow time \Rightarrow Pin valid time	t_{HAHV}	HAKX		$t_{CYC} - 20$	$t_{CYC} + 20$	ns	

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5 V , $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{ mA}$, $C_L = 50\text{ pF}$)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating \Rightarrow HAKX \downarrow time	t_{XHAL}	HAKX	—	$t_{CYC} - 25$	$t_{CYC} + 25$	ns	
HAKX \uparrow time \Rightarrow Pin valid time	t_{HAHV}	HAKX		$t_{CYC} - 25$	$t_{CYC} + 25$	ns	



USART Timing

WARNING: The values given below are for an I/O driving strength $I_{O_{drive}} = 5\text{ mA}$. If $I_{O_{drive}}$ is 2 mA, all the maximum output timing described in the different tables must then be increased by 10 ns.

($T_A = -40^\circ\text{C}$ to 125°C , $V_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$, $I_{O_{drive}} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	$V_{CC} = AV_{CC} = 4.5\text{ V}$ to 5.5 V		$V_{CC} = AV_{CC} = 3.0\text{ V}$ to 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal Shift Clock Mode	$4 t_{CLKP1}$	—	$4 t_{CLKP1}$	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn, SOTn		-20	+20	-30	+30	ns
SOT → SCK ↑ delay time	t_{OVSHI}	SCKn, SOTn		$N * t_{CLKP1} - 20$	—	$N * t_{CLKP1} - 30$	—	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCKn, SINn		$t_{CLKP1} + 45$	—	$t_{CLKP1} + 55$	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCKn, SINn		0	—	0	—	ns
Serial clock “L” pulse width	t_{SLSHE}	SCKn	External Shift Clock Mode	$t_{CLKP1} + 10$	—	$t_{CLKP1} + 10$	—	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn		$t_{CLKP1} + 10$	—	$t_{CLKP1} + 10$	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn, SOTn		—	$2 t_{CLKP1} + 45$	—	$2 t_{CLKP1} + 55$	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCKn, SINn		$t_{CLKP1}/2 + 10$	—	$t_{CLKP1}/2 + 10$	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCKn, SINn		$t_{CLKP1} + 10$	—	$t_{CLKP1} + 10$	—	ns
SCK fall time	t_{FE}	SCKn		—	20	—	20	ns
SCK rise time	t_{RE}	SCKn		—	20	—	20	ns

- Notes:
- AC characteristic in CLK synchronized mode.
 - C_L is the load capacity value of pins when testing.
 - Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “CY96300 Super series Hardware Manual”
 - t_{CLKP1} is the cycle time of the peripheral clock 1 (CLKP1), Unit : ns

*1: Parameter N depends on t_{SCYCI} and can be calculated as follows:

- if $t_{SCYCI} = 2 * k * t_{CLKP1}$, then $N = k$, where k is an integer > 2
- if $t_{SCYCI} = (2 * k + 1) * t_{CLKP1}$, then $N = k + 1$, where k is an integer > 1

Examples:

t_{scyci}	N
$4 * t_{CLKP1}$	2
$5 * t_{CLKP1}, 6 * t_{CLKP1}$	3
$7 * t_{CLKP1}, 8 * t_{CLKP1}$	4
...	...



I²C Timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

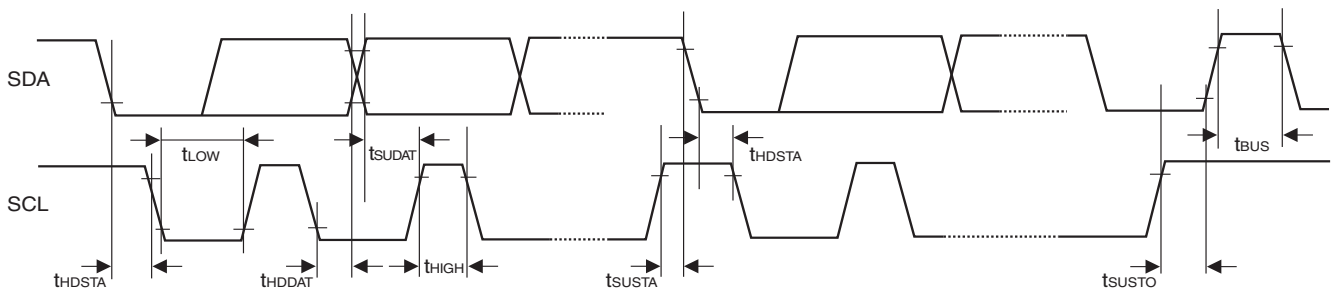
Parameter	Symbol	Condition	Standard-mode		Fast-mode* ⁴		Unit
			Min	Max	Min	Max	
SCL clock frequency	f _{SCL}	R = 1.7 kΩ, C = 50 pF* ¹	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL↓	t _{HDSTA}		4.0	—	0.6	—	μs
"L" width of the SCL clock	t _{LOW}		4.7	—	1.3	—	μs
"H" width of the SCL clock	t _{HIGH}		4.0	—	0.6	—	μs
Set-up time for a repeated START condition SCL↑→SDA↓	t _{SUSTA}		4.7	—	0.6	—	μs
Data hold time SCL↓→SDA↑	t _{HDDAT}		0	3.45* ²	0	0.9* ³	μs
Data set-up time SDA↓↑→SCL↑	t _{SUDAT}		250	—	100	—	ns
Set-up time for STOP condition SCL↑→SDA↑	t _{SUSTO}		4.0	—	0.6	—	μs
Bus free time between a STOP and START condition	t _{BUS}		4.7	—	1.3	—	μs

*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum t_{HDDAT} have only to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.

*3 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement t_{SUDAT} ≥ 250 ns must then be met.

*4 : For use at over 100 kHz, set the peripheral clock 1 to at least 6 MHz.



15.5 Analog Digital Converter
 $(T_A = -40\text{ }^\circ\text{C to } +125\text{ }^\circ\text{C}, 3.0\text{ V} \leq \text{AVRH} - \text{AVRL}, V_{CC} = \text{AV}_{CC} = 3.0\text{V to } 5.5\text{V}, V_{SS} = \text{AV}_{SS} = 0\text{V})$

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	-3	-	+3	LSB	
Nonlinearity error	-	-	-2.5	-	+2.5	LSB	
Differential nonlinearity error	-	-	-1.9	-	+1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL-1.5 LSB	AVRL+0.5 LSB	AVRL+2.5 LSB	V	
Full scale reading voltage	V_{FST}	ANn	AVRH-3.5 LSB	AVRH-1.5 LSB	AVRH+0.5 LSB	V	
Compare time	-	-	1.0	-	16,500	μs	$4.5\text{ V} \leq \text{AV}_{CC} \leq 5.5\text{ V}$
			2.0	-	-	μs	$3.0\text{ V} \leq \text{AV}_{CC} < 4.5\text{ V}$
Sampling time	-	-	0.5	-	-	μs	$4.5\text{ V} \leq \text{AV}_{CC} \leq 5.5\text{ V}$
			1.2	-	-	μs	$3.0\text{ V} \leq \text{AV}_{CC} < 4.5\text{ V}$
Analog port input current	I_{AIN}	ANn	-3	-	+3	μA	$\text{AV}_{SS}, \text{AVRL} < V_I < \text{AV}_{CC}, \text{AVRH}$
Analog input leakage current (during conversion)	I_{AIN}	ANn	-1	-	+1	μA	$T_A = 25\text{ }^\circ\text{C}, \text{AV}_{SS}, \text{AVRL} < V_I < \text{AV}_{CC}, \text{AVRH}$
			-3	-	+3	μA	$T_A = 125\text{ }^\circ\text{C}, \text{AV}_{SS}, \text{AVRL} < V_I < \text{AV}_{CC}, \text{AVRH}$
Analog input voltage range	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	AVRH	AVRH/AVRH2	0.75 AV_{CC}	-	AV_{CC}	V	
	AVRL	AVRL	AV_{SS}	-	0.25 AV_{CC}	V	
Power supply current	I_A	AV_{CC}	-	2.5	5	mA	A/D Converter active
	I_{AH}	AV_{CC}	-	-	5	μA	A/D Converter not operated
Reference voltage current	I_R	AVRH/AVRL	-	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH/AVRL	-	-	5	μA	A/D Converter not operated
Offset between input channels	-	ANn	-	-	4	LSB	

Note: The accuracy gets worse as $|\text{AVRH} - \text{AVRL}|$ becomes smaller.

Definition of A/D Converter Terms

Resolution: Analog variation that is recognized by an A/D converter.

Total error: Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error and nonlinearity error.

Nonlinearity error: Deviation between a line across zero-transition line (“00 0000 0000” <--> “00 0000 0001”) and full-scale transition line (“11 1111 1110” <--> “11 1111 1111”) and actual conversion characteristics.

Differential nonlinearity error: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Zero reading voltage: Input voltage which results in the minimum conversion value.

Full scale reading voltage: Input voltage which results in the maximum conversion value.



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$1 \text{ LSB} = (\text{Ideal value}) \frac{AVRH - AVRL}{1024} \text{ [V]}$$

N: A/D converter digital output value

$$V_{OT} (\text{Ideal value}) = AVRL + 0.5 \text{ LSB [V]}$$

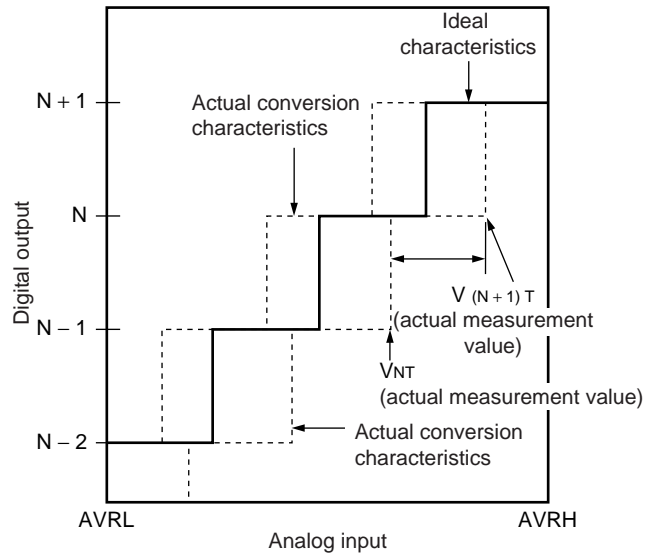
$$V_{FST} (\text{Ideal value}) = AVRH - 1.5 \text{ LSB [V]}$$

V_{NT} : A voltage at which digital output transitions from (N - 1) to N.

Nonlinearity error



Differential nonlinearity error



$$\text{Nonlinearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \text{ LSB [LSB]}$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N : A/D converter digital output value

V_{OT} : Voltage at which digital output transits from “000_H” to “001_H.”

V_{FST} : Voltage at which digital output transits from “3FE_H” to “3FF_H.”

Notes on A/D Converter Section

- ²About the external impedance of the analog input and the sampling time of the A/D converter (with sample and hold circuit):
If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

analog input circuit model:



Reference value:

- C = 8.5 pF (Max)

To satisfy the A/D conversion precision standard, the relationship between the external impedance and minimum sampling time must be considered and then either the resistor value and operating frequency must be adjusted or the external impedance must be decreased so that the sampling time (T_{samp}) is longer than the minimum value. Usually, this value is set to 7τ , where $\tau = RC$. If the external input resistance (R_{ext}) connected to the analog input is included, the sampling time is expressed as follows:

$$T_{\text{samp}} [\text{min}] = 7 \times (R_{\text{ext}} + 2.6 \text{ k}\Omega) \times C \text{ for } 4.5 \leq AV_{\text{CC}} \leq 5.5$$

$$T_{\text{samp}} [\text{min}] = 7 \times (R_{\text{ext}} + 12.1 \text{ k}\Omega) \times C \text{ for } 3.0 \leq AV_{\text{CC}} \leq 4.5$$

If the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

- ² About the error

The accuracy gets worse as $|AV_{\text{RH}} - AV_{\text{RL}}|$ becomes smaller.

15.6 Alarm Comparator
 $(T_A = -40\text{ }^\circ\text{C to } +125\text{ }^\circ\text{C}, V_{CC} = AV_{CC} = 3.0\text{V} - 5.5\text{V}, V_{SS} = AV_{SS} = 0\text{V})$

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I_{A5ALMF}	AV_{CC}	-	25	45	μA	Alarm comparator enabled in fast mode (one channel)
	I_{A5ALMS}		-	7	13	μA	Alarm comparator enabled in slow mode (one channel)
	I_{A5ALMH}		-	-	5	μA	Alarm comparator disabled
ALARM pin input current	I_{ALIN}	ALARM0, ALARM1	-1	-	+1	μA	$T_A = 25\text{ }^\circ\text{C}$
			-3	-	+3	μA	$T_A = 125\text{ }^\circ\text{C}$
ALARM pin input voltage range	V_{ALIN}		0	-	AV_{CC}	V	
External low threshold high->low transition	$V_{EVTL(H->L)}$		$0.36 * AV_{CC} - 0.25$	$0.36 * AV_{CC} - 0.1$	-	V	INTREF = 0
External low threshold low->high transition	$V_{EVTL(L->H)}$		-	$0.36 * AV_{CC} + 0.1$	$0.36 * AV_{CC} + 0.25$	V	
External high threshold high->low transition	$V_{EVTH(H->L)}$		$0.78 * AV_{CC} - 0.25$	$0.78 * AV_{CC} - 0.1$	-	V	
External high threshold low->high transition	$V_{EVTH(L->H)}$		-	$0.78 * AV_{CC} + 0.1$	$0.78 * AV_{CC} + 0.25$	V	
Internal low threshold high->low transition	$V_{IVTL(H->L)}$		0.9	1.1	-	V	INTREF = 1
Internal low threshold low->high transition	$V_{IVTL(L->H)}$		-	1.3	1.55	V	
Internal high threshold high->low transition	$V_{IVTH(H->L)}$		2.2	2.4	-	V	
Internal high threshold low->high transition	$V_{IVTH(L->H)}$		-	2.6	2.85	V	
Switching hysteresis	V_{HYS}		50	-	300	mV	
Comparison time	t_{COMPF}	-	0.1	1	μs	CMD = 1 (fast)	
	t_{COMPS}	-	1	10	μs	CMD = 0 (slow)	
Power-up stabilization time after enabling alarm comparator	t_{PD}	-	1	5	ms	Threshold levels specified above are not guaranteed within this time	
Slow/Fast mode transition time	t_{CMD}	-	100	500	μs		



15.7 Low Voltage Detector Characteristics
 $(T_A = -40\text{ }^{\circ}\text{C to } +125\text{ }^{\circ}\text{C}, V_{CC} = AV_{CC} = 3.0\text{V} - 5.5\text{V}, V_{SS} = AV_{SS} = 0\text{V})$

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Stabilization time	$T_{LV DSTAB}$	-	75	μs	After power-up or change of detection level
Level 0	V_{DL0}	2.7	2.9	V	CILCR:LVL[3:0]="0000"
Level 1	V_{DL1}	2.9	3.1	V	CILCR:LVL[3:0]="0001"
Level 2	V_{DL2}	3.1	3.3	V	CILCR:LVL[3:0]="0010"
Level 3	V_{DL3}	3.5	3.75	V	CILCR:LVL[3:0]="0011"
Level 4	V_{DL4}	3.6	3.85	V	CILCR:LVL[3:0]="0100"
Level 5	V_{DL5}	3.7	3.95	V	CILCR:LVL[3:0]="0101"
Level 6	V_{DL6}	3.8	4.05	V	CILCR:LVL[3:0]="0110"
Level 7	V_{DL7}	3.9	4.15	V	CILCR:LVL[3:0]="0111"
Level 8	V_{DL8}	4.0	4.25	V	CILCR:LVL[3:0]="1000"
Level 9	V_{DL9}	4.1	4.35	V	CILCR:LVL[3:0]="1001"
Level 10	V_{DL10}	not used			
Level 11	V_{DL11}	not used			
Level 12	V_{DL12}	not used			
Level 13	V_{DL13}	not used			
Level 14	V_{DL14}	not used			
Level 15	V_{DL15}	not used			

CILCR:LVL[3:0] are the low voltage detector level select bits of the CILCR register.

Levels 10 to 15 are not used in this device.

For correct detection, the slope of the voltage level must satisfy $\left| \frac{dV}{dt} \right| \leq 0.004 \frac{V}{\mu\text{s}}$.

Faster variations are regarded as noise and may not be detected.

The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of $V_{CC} = 2.7\text{ V}$. The electrical characteristics however are only valid in the specified range (usually down to 3.0 V).

Low Voltage Detector Operation

In the following figure, the occurrence of a low voltage condition is illustrated. For a detailed description of the reset and startup behavior, please refer to the corresponding hardware manual chapter.



15.8 FLASH Memory Program/erase Characteristics

($T_A = -40^{\circ}\text{C}$ to 105°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $DV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = DV_{SS} = 0\text{V}$)

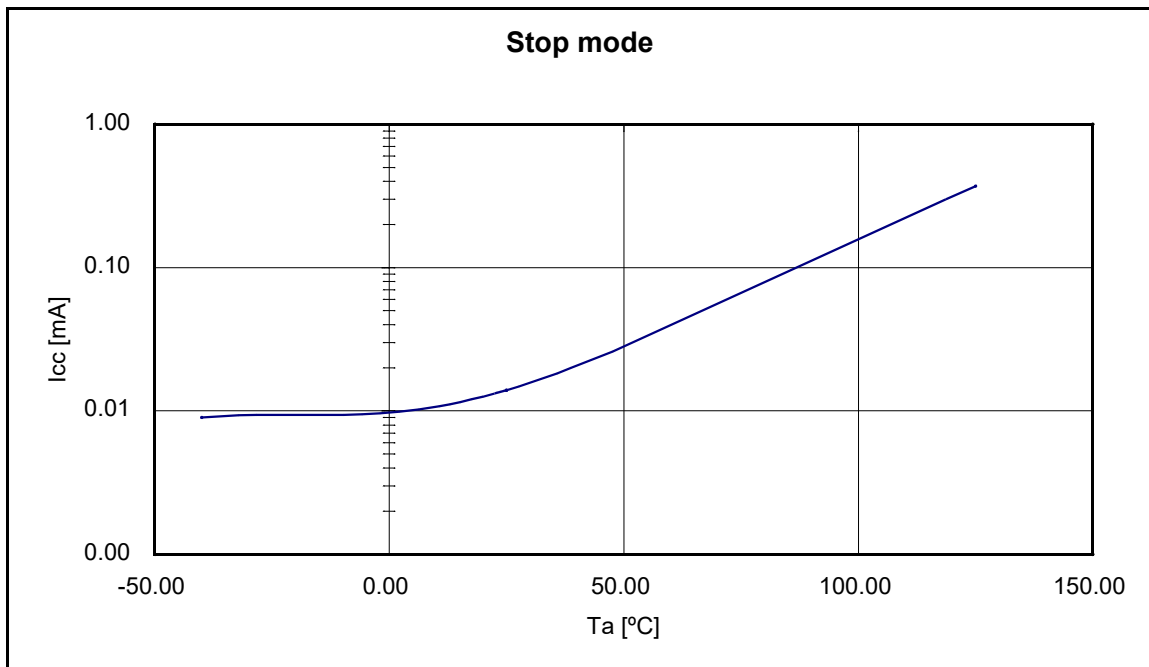
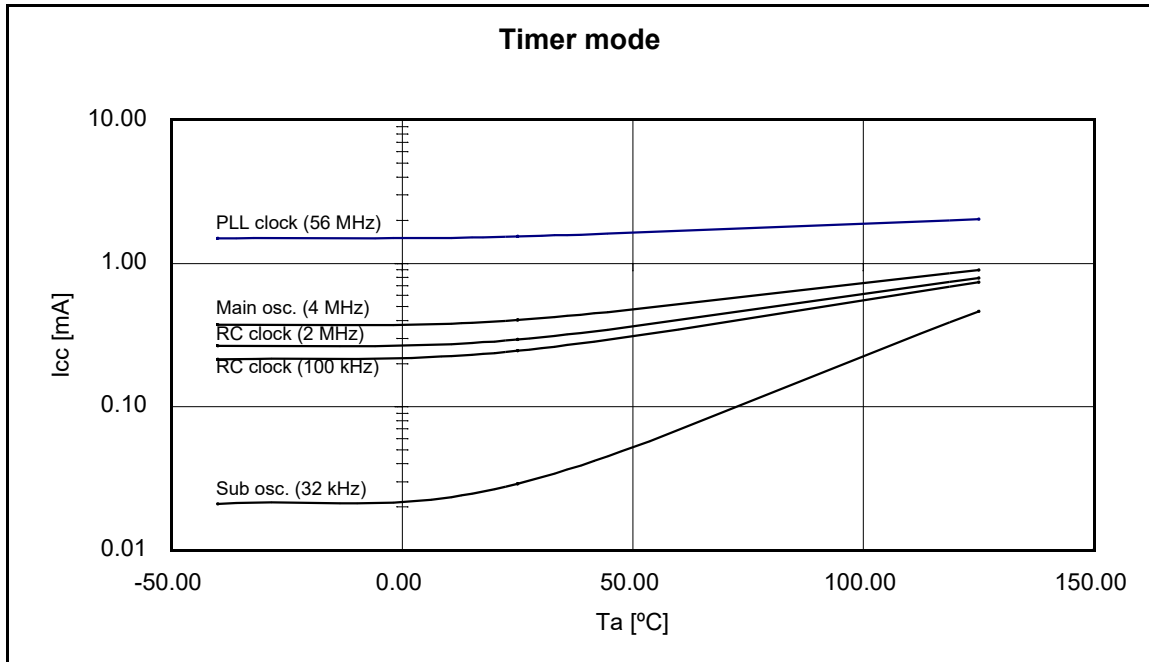
Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.9	3.6	s	Without erasure pre-programming time
Chip erase time	-	n*0.9	n*3.6	s	Without erasure pre-programming time (n is the number of Flash sector of the device)
Word (16-bit width) programming time	-	23	370	us	Without overhead time for submitting write command
Program/Erase cycle	10 000	-	-	cycle	
Flash data retention time	20	-	-	year	*1

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

16. Example Characteristics

The diagrams below show the characteristics of one measured sample with typical process parameters.





Used Settings

Mode	Selected Source Clock	Clock/Regulator Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = 56 MHz CLKP2 = 28 MHz Regulator in High Power Mode Core Voltage = 1.9 V
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4 MHz Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2 MHz Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100 kHz Regulator in High Power Mode Core Voltage = 1.8 V
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32 kHz Regulator in Low Power Mode A Core Voltage = 1.8 V
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = 56 MHz CLKP2 = 28 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.9 V
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100 kHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32 kHz (CLKB is stopped in this mode) Regulator in Low Power Mode A Core Voltage = 1.8 V

Used Settings

Mode	Selected Source Clock	Clock/Regulator Settings
Timer mode	PLL	CLKMC = 4 MHz, CLKPLL = 56 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.9 V
	Main osc.	CLKMC = 4 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	RC clock fast	CLKRC = 2 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	RC clock slow	CLKRC = 100 kHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	Sub osc.	CLKSC = 100 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode A, Core Voltage = 1.8 V
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode B, Core Voltage = 1.8 V

17. Package Dimension CY96(F)38x LQFP 120P

Package Type	Package Code
LQFP 120	LQM120



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.115	—	0.195
D	18.00 BSC		
D1	18.00 BSC		
e	0.50 BSC		
E	18.00 BSC		
E1	18.00 BSC		
L	0.45	0.60	0.75
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.

△ DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

△ DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.

△ D TO BE DETERMINED AT SEATING PLANE C.

△ DIMENSIONS D1 AND D2 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE.

DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

△ DETAIL B OF PIN IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

△ REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST PART OF THE BODY EXCEPTIVE OF MOLD DASH AND RAJURNS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.

△ DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (⊕) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED a MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RAJURNS OF THE LEAD FOOT.

△ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

△ A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

11 JEDFG SPECIFICATION NO. RPT-NA

002-16172 **

 PACKAGE OUTLINE, 120 LEAD LQFP
 18.0x18.0x1.7MM LQM 120 REV**

18. Ordering Information

Part Number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
CY96384RSBPMC-GSE2	ROM (128 KB)	No	No	120-pin Plastic LQFP (LQM120)
CY96384RWBPMC-GSE2		Yes		
CY96384RSCPMC-GSE2		No	No	120-pin Plastic LQFP (LQM120)
CY96384RWCPMC-GSE2		Yes		
CY96385RSCPMC-GSE2	ROM (160 KB)	No	No	120-pin Plastic LQFP (LQM120)
CY96F385RSAPMC-GS-UJE2	Flash A (160 KB)	No	No	120-pin Plastic LQFP (LQM120)
CY96F385RWAPMC-GS-UJE2		Yes		
CY96F385RSBPMC-GS-UJE2		No		
CY96F386RSBPMC-GS-UJE1	Flash A (288 KB)	No	No	120-pin Plastic LQFP (LQM120)
CY96F386RSBPMC-GS-UJE2		No		
CY96F386RWBPMC-GS-UJE2		Yes		
CY96F386RSCPMC-GS-UJE2		No		
CY96F387RSBPMC-GS-UJE2	Flash A (416 KB)	No	No	120-pin Plastic LQFP (LQM120)
CY96F387RWBPMC-G-UJE2		Yes		
CY96F387RSCPMC-GS-UJE2		No		
CY96F388HWBPMC-GS-UJE2	Flash A (544 KB) Flash B (32 KB)	Yes	No	120-pin Plastic LQFP (LQM120)
CY96F389RSBPMC-GS-UJE2	Flash A (544 KB) Flash B (288 KB)	No	No	120-pin Plastic LQFP (LQM120)

This datasheet is also valid for the following outdated devices:

CY96F386RSA, CY96F386RWA, CY96F387RSA, CY96F387RWA

19. Major Changes

Page	Section	Change Result
Rev *B		
-	Marketing Part Numbers changed from an MB prefix to a CY prefix.	
1	-	Deleted the following comment. Note: MB96384/385/F385/F388/F389 devices are under development and specification is preliminary. These products under development may change its specification without notice.
6	1. Product Lineup	Deleted the following comment. *1: These devices are under development and specification is preliminary. These products under development may change its specification without notice.
8 112 113	3. Pin Assignment 17. Package Dimension 18. Ordering Information	Package description modified to JEDEC description. (before) FPT-120P-M21 (after) LQM120
113	18. Ordering Information	Deleted the following comment. *1: These devices are under development and specification is preliminary. These products under development may change its specification without notice. Deleted the following parts number. - MB96384YSBPMC-GSE2 - MB96384YWBPMC-GSE2 - MB96385YSBPMC-GSE2 - MB96385RSBPMC-GSE2 - MB96385YWBPMC-GSE2 - MB96385RWBPMC-GSE2 - MB96F385YSAPMC-GSE2 - MB96F385YWAPMC-GSE2 - MB96F386YSBPMC-GSE2 - MB96F386YWBPMC-GSE2 - MB96F387YSBPMC-GSE2 - MB96F387YWBPMC-GSE2 - MB96F388TSAPMC-GSE2 - MB96F388HSAPMC-GSE2 - MB96F388TWAPMC-GSE2 - MB96F388HWAPMC-GSE2 - MB96F389YSAPMC-GSE2 - MB96F389RSAPMC-GSE2 - MB96F389YWAPMC-GSE2 - MB96F389RWAPMC-GSE2 - MB96V300BRB-ES (for evaluation)

Page	Section	Change Result
113	18. Ordering Information	<p>Revised the following parts number. (before)</p> <ul style="list-style-type: none"> - MB96384RSBPMC-GSE2 - MB96384RWBPMC-GSE2 - MB96F385RSAPMC-GSE2 - MB96F385RWAPMC-GSE2 - MB96F386RSBPMC-GSE2 - MB96F386RWBPMC-GSE2 - MB96F387RSBPMC-GSE2 - MB96F387RWBPMC-GSE2 <p>(after)</p> <ul style="list-style-type: none"> - CY96384RSBPMC-GSE2 - CY96384RWBPMC-GSE2 - CY96F385RSAPMC-GS-UJE2 - CY96F385RWAPMC-GS-UJE2 - CY96F386RSBPMC-GS-UJE2 - CY96F386RWBPMC-GS-UJE2 - CY96F387RSBPMC-GS-UJE2 - CY96F387RWBPMC-G-UJE2 <p>Added the following parts number.</p> <ul style="list-style-type: none"> - CY96384RSCPMC-GSE2 - CY96384RWCPMC-GSE2 - CY96385RSCPMC-GSE2 - CY96F385RSBPMC-GS-UJE2 - CY96F386RSBPMC-GS-UJE1 - CY96F386RSCPMC-GS-UJE1 - CY96F386RSCPMC-GS-UJE2 - CY96F387RSAPMC-GS-UJE2 - CY96F387RSCPMC-GS-UJE2 - CY96F388HSBPMC-GS-UJE1 - CY96F389RSBPMC-GS-UJE2 <p>Changed and deleted the parts number in Note. (before) MB96F386YSA, MB96F386RSA, MB96F386YWA, MB96F386RWA, MB96F387YSA, MB96F387RSA, MB96F387YWA, MB96F387RWA (after) CY96F386RSA, CY96F386RWA, CY96F387RSA, CY96F387RWA</p>

20. Revision History

Spansion Publication Number: **DS07-13803-2E**

Revision	Date	Modification
Prelim 1	2007-05-2	Creation
Prelim 2	2007-05-24	Electrical characteristics and memory description updates
Prelim 3	2007-08-09	Typo errors corrections, Flash memory programming interface update
Prelim 4	2007-08-31	Update of DC characteristics. new MB96F388 and MB96F389 added. LVD chapter added as well as an example characteristics chapter
Prelim 5	2007-09-06	Updates of the DC characteristics, interrupt vector table update, update of the LVD characteristics
Prelim 6	2007-11-14	Memory map for external bus modified. Modifications of the drawing of the pin circuits. Electrical characteristics updates. Rephrasing and typos corrections. Add Slew rate high current outputs chapter. Modification of the block diagram. Memory map modified for Flash. RAM memory map added. Pin circuit type corrected. Type L IO is now included.
Prelim 7	2007-12-12	Memory IO map modified New Flash/ROM configuration presentation Ordering information: MB96300B used as reference. Block diagram modified to included relocated pins. Main Flash becomes Flash memory A and Satellite flash becomes Flash memory B
Prelim 8	2008-02-04	<ul style="list-style-type: none"> • Devices under development added: MB96384/385/F385/F388/F389 • Block diagram corrected (existing resource pins) • Pin assignment: TTG8 -> TTG7 • Pin function table corrected • I/O circuit type diagrams corrected • Memory map cleaned up • "Flash sector configuration" replaced by corrected "User ROM Memory map for Flash devices", "ROM configuration" replaced by "User ROM Memory map for Mask ROM devices" • IO map table regenerated: <ul style="list-style-type: none"> - Port register: Naming style corrected - Memory control registers renamed (Main/Sat -> A/B) - addresses after 000BFFh removed • Absolute maximum ratings: Pd and Ta specified more precisely • Run and Sleep mode currents: more conditions added (1WS settings) • Run mode current spec in 48/24MHz mode corrected • Maximum CLKP2 frequency for MB96F386/F387 corrected • High current port input capacitance added • External bus timings: missing conditions added and readability improved • Alarm comparator spec updated (transition voltages defined) • MB96V300A removed • Ordering information updated • Typos and formatting corrected

Revision	Date	Modification
9	2009-01-09	<ul style="list-style-type: none"> • Format adjusted to official Fujitsu Microelectronics datasheet standard (mainly style changes and official notes and disclaimer added) • Numbering of Electrical Characteristics subchapters automated • Note about devices under development modified • I/O map: Note added about reserved addresses • Serial programming interface: Note about handshaking pins improved • ICCPLL for CLKS1/2=80MHz, CLKB=40MHz (F388/F389) increased by 5mA • ICCSPLL for CLKS1/2=80MHz, CLKB=40MHz (F388/F389) increased by 0.8mA (typ) and 1.3mA (max) • Updated ordering information: MB96384/385**A -> MB96384/385**B • Package code of MB96V300 corrected in ordering information • Internal LCD divider resistance value corrected: Typ 35kOhm -> 40kOhm, Max 50kOhm -> 65kOhm • Run and Sleep mode currents of ROM devices (MB96384/385) reduced • Added voltage condition to pull-up resistance and LCD divide resistance spec • Lineup: Term “Data Flash” replaced by “independent 32KB Flash” • Ordering information: column “Independent 32KB Data Flash” replaced by new column “Flash/ROM”, column “Remarks” removed • Official package dimension drawing with additional notes added • Empty pages removed • MB96384/385 and MB96F385/F388/F389 separated in DC spec and currents of these devices adjusted according to first evaluation results • Alarm comparator: Power supply current max values increased, comparison time reduced, mode transition time and power-up stabilization time newly added • Handling devices: Notes added about Serial communication and about using ceramic resonators. • Feature list and AC Characteristics: 16MHz maximum frequency is valid for crystal oscillators. For resonators, maximum frequency depends on Q-factor • AC characteristics: PLL phase skew spec added, CLKVCO min=64MHz • VOL3 spec improved: spec valid for 3mA load for full Vcc range • C-Pin cap spec updated: 4.7uF-10uF capacitor with tolerance permitted • “Preliminary” watermark removed

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: CY96380 Series F ² MC-16FX 16-bit Proprietary Microcontroller			
Document Number: 002-04582			
Revision	ECN	Submission Date	Description of Change
**	—	05/02/2007	Migrated to Cypress and assigned document number 002-04582. No change to document contents or format.
*A	5243006	04/28/2016	Updated to Cypress template
*B	6094799	03/12/2018	Revised the following items: Marketing Part Numbers changed from an MB prefix to a CY prefix. 3.Pin Assignments 17.Package Dimension 18.Ordering Information Added 19. Major Changes For details, please see 19.Major Changes
*C	6777565	01/22/2020	Added the following part number on 18. Ordering Information. CY96F388HWBPMC-GS-UJE2 Deleted the following parts number on 18. Ordering Information. CY96F386RSCPMC-GS-UJE1 CY96F387RSAPMC-GS-UJE2 CY96F388HSBPMC-GS-UJE1

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