



**THE DATASHEET OF
CY7S1041GE30-10BVXI**





Please note that Cypress is an Infineon Technologies Company.

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

4-Mbit (256K words × 16 bit) Static RAM with PowerSnooze™ and Error Correcting Code (ECC)

Features

- High speed
 - Access time (t_{AA}) = 10 ns / 15 ns
- Ultra-low power Deep-Sleep (DS) current
 - I_{DS} = 15 μ A
- Low active and standby currents
 - Active Current I_{CC} = 38-mA typical
 - Standby Current I_{SB2} = 6-mA typical
- Wide operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V
- Embedded ECC for single-bit error correction^[1]
- 1.0-V data retention
- TTL- compatible inputs and outputs
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- Available in Pb-free 44-pin TSOP II, 44-SOJ and 48-ball VFBGA

Functional Description

The CY7S1041G is a high-performance PowerSnooze™ static RAM organized as 256K words × 16 bits. This device features fast access times (10 ns) and a unique ultra-low power Deep-Sleep mode. With Deep-Sleep mode currents as low as 15 μ A, the CY7S1041G/ CY7S1041GE devices combine the best features of fast and low- power SRAMs in industry-standard package options. The device also features embedded ECC. logic which can detect and correct single-bit errors in the accessed location.

Deep-Sleep input (\overline{DS}) must be deasserted HIGH for normal operating mode.

To perform data writes, assert the Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW, and provide the data and address on device data pins (I/O_0 through I/O_{15}) and address pins (A_0 through A_{17}) respectively. The Byte High Enable (\overline{BHE}) and Byte Low Enable (\overline{BLE}) inputs control byte writes, and write data on the corresponding I/O lines to the memory location specified. \overline{BHE} controls I/O_8 through I/O_{15} and \overline{BLE} controls I/O_0 through I/O_7 .

To perform data reads, assert the Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) inputs LOW and provide the required address on the address lines. Read data is accessible on the I/O lines (I/O_0 through I/O_{15}). You can perform byte accesses by asserting the required byte enable signal (\overline{BHE} or \overline{BLE}) to read either the upper byte or the lower byte of data from the specified address location

The device is placed in a low-power Deep-Sleep mode when the Deep-Sleep input (\overline{DS}) is asserted LOW. In this state, the device is disabled for normal operation and is placed in a low power data retention mode. The device can be activated by deasserting the Deep-Sleep input (\overline{DS}) to HIGH.

The CY7S1041G is available in 44-pin TSOP II, 48-ball VFBGA and 44-pin (400-mil) Molded SOJ.

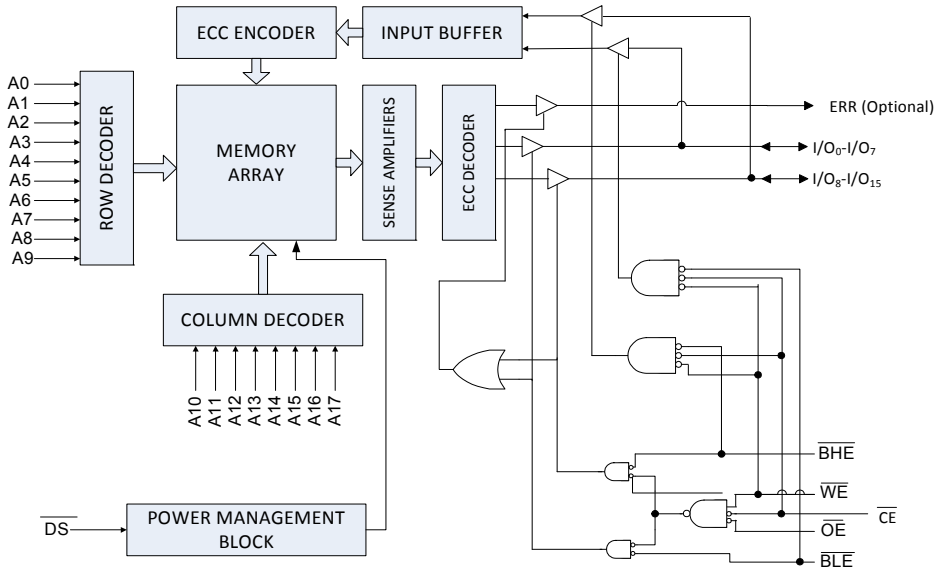
Product Portfolio

Product ^[2]	Range	V_{CC} Range (V)	Speed (ns)	Power Dissipation					
				Operating I_{CC} , (mA)		Standby, I_{SB2} (mA)		Deep-Sleep current (μ A)	
				$f = f_{max}$					
				Typ ^[3]	Max	Typ ^[3]	Max	Typ ^[3]	Max
CY7S1041G(E)18	Industrial	1.65 V–2.2 V	15	–	40	6	8	–	15
CY7S1041G(E)30		2.2 V–3.6 V	10	38	45				
CY7S1041G(E)		4.5–5.5 V	10	38	45				

Notes

1. This device does not support automatic write back on error detection.
2. ERR pin is available only for devices which have ERR option "E" in the ordering code. Refer [Ordering Information](#) for details.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = 1.8$ V (for V_{CC} range of 1.65 V – 2.2 V), $V_{CC} = 3$ V (for V_{CC} range of 2.2 V – 3.6 V), and $V_{CC} = 5$ V (for V_{CC} range of 4.5 V – 5.5 V), $T_A = 25$ °C.

Logic Block Diagram – CY7S1041G / CY7S1041GE



Contents

Pin Configurations	4	Ordering Information	16
Maximum Ratings	6	Ordering Code Definitions	16
Operating Range	6	Package Diagrams	17
DC Electrical Characteristics	6	Acronyms	20
Capacitance	7	Document Conventions	20
Thermal Resistance	7	Units of Measure	20
AC Test Loads and Waveforms	7	Document History Page	21
Data Retention Characteristics	8	Sales, Solutions, and Legal Information	22
Data Retention Waveform	8	Worldwide Sales and Design Support	22
Deep-Sleep Mode Characteristics	9	Products	22
AC Switching Characteristics	10	PSoC@Solutions	22
Switching Waveforms	11	Cypress Developer Community	22
Truth Table	15	Technical Support	22
ERR Output – CY7S1041GE	15		

Pin Configurations

Figure 1. 44-pin TSOP II / 44-SOJ pinout, CY7S1041G

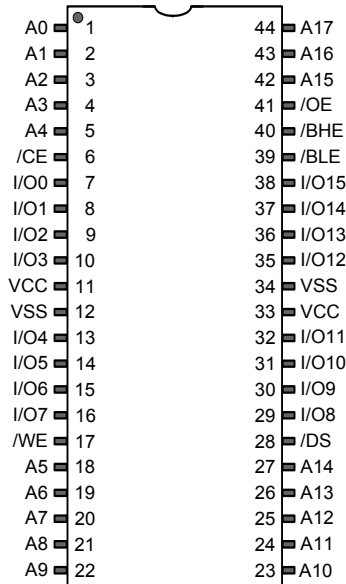


Figure 2. 48-ball VFBGA (6 × 8 × 1.0 mm) pinout, Single Chip Enable without ERR, CY7S1041G [4], Package/Grade ID: BVJXI [6]

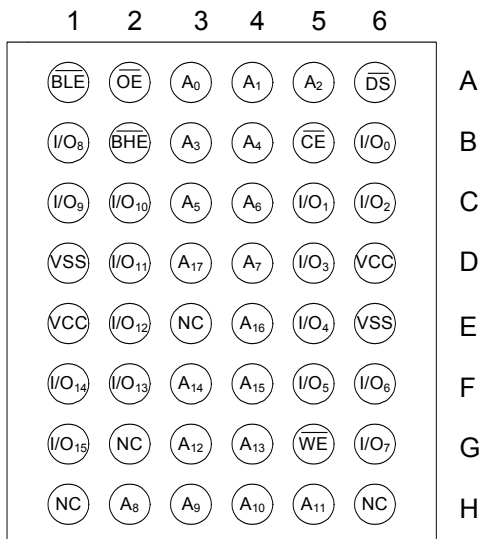
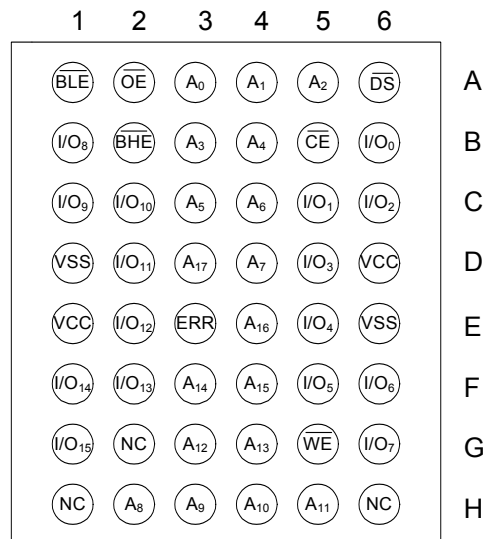


Figure 3. 48-ball VFBGA (6 × 8 × 1.0 mm) pinout, Single Chip Enable with ERR, CY7S1041GE [4, 5], Package/Grade ID: BVJXI [6]



Notes

- 4. NC pins are not connected internally to the die.
- 5. ERR is an output pin.
- 6. Package type BVJXI is JEDEC compliant compared to package type BVXI. The difference between the two is that the higher and lower byte I/Os (I/O_[7:0] and I/O_[15:8] balls are swapped).

Pin Configurations (continued)

Figure 4. 48-ball VFBGA (6 × 8 × 1.0 mm) pinout, Single Chip Enable without ERR, CY7S1041G^[7], Package/Grade ID: BVXI^[9]

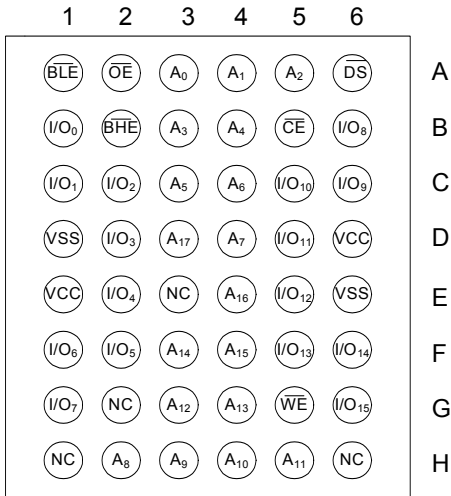
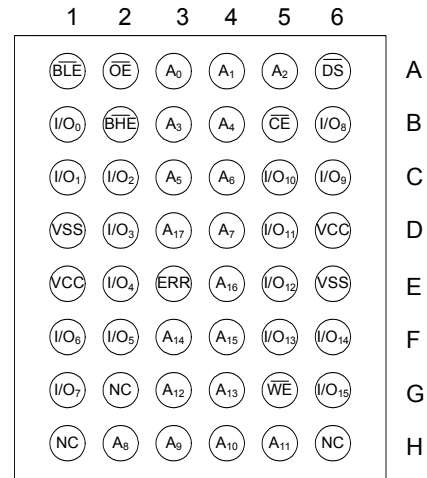


Figure 5. 48-ball VFBGA (6 × 8 × 1.0 mm) pinout, Single Chip Enable with ERR, CY7S1041GE^[7, 8], Package/Grade ID: BVXI^[9]



Notes

7. NC pins are not connected internally to the die.
8. ERR is an output pin.
9. Package type BVJXI is JEDEC compliant compared to package type BVXI. The difference between the two is that the higher and lower byte I/Os (I/O_[7:0] and I/O_[15:8] balls are swapped).

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C
 Ambient temperature
 with power applied -55 °C to +125 °C
 Supply voltage
 on V_{CC} relative to GND ^[10] -0.5 V to + 6.0 V
 DC voltage applied to outputs
 in HI-Z State ^[10] -0.5 V to $V_{CC} + 0.5$ V

DC input voltage ^[10] -0.5 V to $V_{CC} + 0.5$ V
 Current into outputs (LOW) 20 mA
 Static discharge voltage
 (MIL-STD-883, Method 3015) > 2001 V
 Latch-up current > 140 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	-40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

DC Electrical Characteristics

Over the Operating Range of -40 °C to +85 °C

Parameter	Description	Test Conditions	10 ns / 15 ns			Unit	
			Min	Typ ^[11]	Max		
V_{OH}	Output HIGH voltage	1.65 V to 2.2 V	$V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$	1.4	-	-	V
		2.2 V to 2.7 V	$V_{CC} = \text{Min}, I_{OH} = -1.0 \text{ mA}$	2	-	-	
		2.7 V to 3.0 V	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.2	-	-	
		3.0 V to 3.6 V	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	-	-	
		4.5 V to 5.5 V	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	-	-	
		4.5 V to 5.5 V	$V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$	$V_{CC} - 0.5$ ^[13]	-	-	
V_{OL}	Output LOW voltage	1.65 V to 2.2 V	$V_{CC} = \text{Min}, I_{OL} = 0.1 \text{ mA}$	-	-	0.2	V
		2.2 V to 2.7 V	$V_{CC} = \text{Min}, I_{OL} = 2 \text{ mA}$	-	-	0.4	
		2.7 V to 3.6 V	$V_{CC} = \text{Min}, I_{OL} = 8 \text{ mA}$	-	-	0.4	
		3.6 V to 5.5 V	$V_{CC} = \text{Min}, I_{OL} = 8 \text{ mA}$	-	-	0.4	
V_{IH} ^[10, 12]	Input HIGH voltage	1.65 V to 2.2 V		1.4	-	$V_{CC} + 0.2$	V
		2.2 V to 2.7 V		2	-	$V_{CC} + 0.3$	
		2.7 V to 3.6 V		2	-	$V_{CC} + 0.3$	
		3.6 V to 5.5 V		2	-	$V_{CC} + 0.5$	
V_{IL} ^[10, 12]	Input LOW voltage	1.65 V to 2.2 V		-0.2	-	0.4	V
		2.2 V to 2.7 V		-0.3	-	0.6	
		2.7 V to 3.6 V		-0.3	-	0.8	
		3.6 V to 5.5 V		-0.5	-	0.8	
I_{IX}	Input leakage current	$GND \leq V_{IN} \leq V_{CC}$		-1	-	+1	μA
I_{OZ}	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$, Output disabled		-1	-	+1	μA
I_{CC}	V_{CC} operating supply current	$V_{CC} = \text{Max}, I_{OUT} = 0 \text{ mA}$, CMOS levels	f = 100 MHz	-	38	45	mA
			f = 66.7 MHz	-	40	40	
I_{SB1}	Standby current – TTL inputs	$\text{Max } V_{CC}, \overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}		-	-	15	mA

Notes

- $V_{IL}(\text{min}) = -2.0 \text{ V}$ and $V_{IH}(\text{max}) = V_{CC} + 2 \text{ V}$ for pulse durations of less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = 1.8 \text{ V}$ (for V_{CC} range of 1.65 V – 2.2 V), $V_{CC} = 3 \text{ V}$ (for V_{CC} range of 2.2V – 3.6 V), and $V_{CC} = 5 \text{ V}$ (for V_{CC} range of 4.5 V – 5.5 V), $T_A = 25 \text{ }^\circ\text{C}$.
- For the DS pin, $V_{IH}(\text{min})$ is $V_{CC} - 0.2 \text{ V}$ and $V_{IL}(\text{max})$ is 0.2 V.
- This parameter is guaranteed by design and not tested.

DC Electrical Characteristics (continued)

Over the Operating Range of -40 °C to +85 °C

Parameter	Description	Test Conditions	10 ns / 15 ns			Unit
			Min	Typ ^[11]	Max	
I_{SB2}	Standby current – CMOS inputs	Max V_{CC} , $\overline{CE} \geq V_{CC} - 0.2 V$, $DS \geq V_{CC} - 0.2 V$, $V_{IN} \geq V_{CC} - 0.2 V$ or $V_{IN} \leq 0.2 V$, $f = 0$	-	6	8	mA
I_{DS}	Deep-Sleep current	Max V_{CC} , $\overline{CE} \geq V_{CC} - 0.2 V$, $DS \leq 0.2 V$, $V_{IN} \geq V_{CC} - 0.2 V$ or $V_{IN} \leq 0.2 V$, $f = 0$	-	-	15	μA

Capacitance

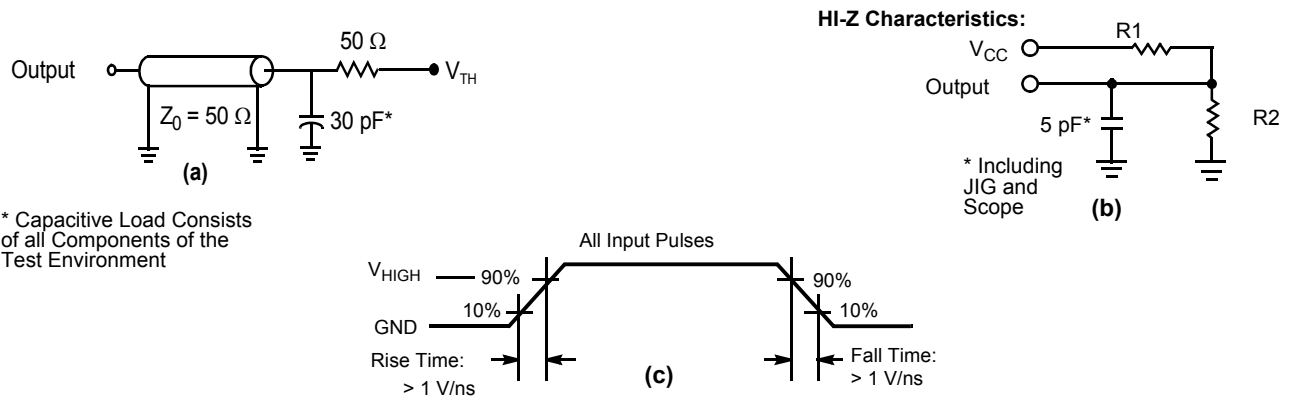
Parameter ^[14]	Description	Test Conditions	All packages	Unit
C_{IN}	Input capacitance	$T_A = 25\text{ }^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC}(\text{typ})$	10	pF
C_{OUT}	I/O capacitance		10	pF

Thermal Resistance

Parameter ^[14]	Description	Test Conditions	48-ball VFBGA	44-pin SOJ	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	31.35	55.37	68.85	$^\circ\text{C/W}$
Θ_{JC}	Thermal resistance (junction to case)		14.74	30.41	15.97	$^\circ\text{C/W}$

AC Test Loads and Waveforms

Figure 6. AC Test Loads and Waveforms ^[15]



Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	Ω
R2	1538	351	351	Ω
V_{TH}	$V_{CC}/2$	1.5	1.5	V
V_{HIGH}	1.8	3.0	3.0	V

Notes

- 14. Tested initially and after any design or process changes that may affect these parameters.
- 15. Full-device AC operation assumes a 100- μs ramp time from 0 to $V_{CC(\text{min})}$ or 100- μs wait time after V_{CC} stabilization.

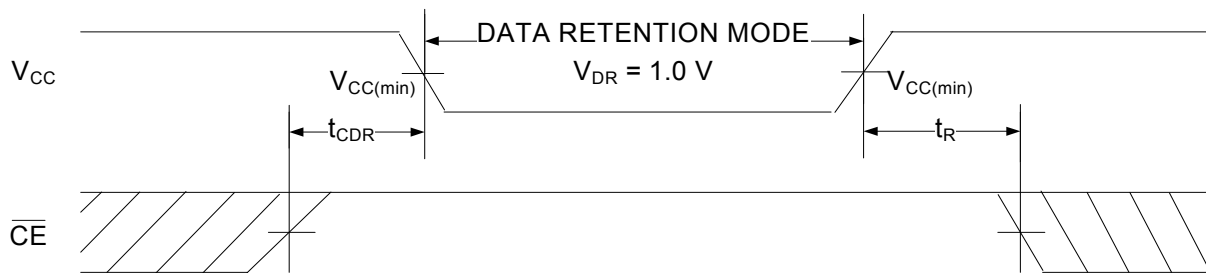
Data Retention Characteristics

Over the Operating Range of $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$

Parameter	Description	Conditions ^[16]	Min	Max	Unit
V_{DR}	V_{CC} for data retention		1.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR}$, $\overline{CE} \geq V_{CC} - 0.2\text{ V}$, $\overline{DS} \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	8	mA
$t_{CDR}^{[17]}$	Chip deselect to data retention time		0	–	ns
$t_R^{[17, 18]}$	Operation recovery time	$2.2\text{ V} < V_{CC} \leq 5.5\text{ V}$	10	–	ns
		$V_{CC} \leq 2.2\text{ V}$	15	–	ns

Data Retention Waveform

Figure 7. Data Retention Waveform ^[18]



Notes

16. \overline{DS} signal must be HIGH during Data Retention Mode.

17. These parameters are guaranteed by design

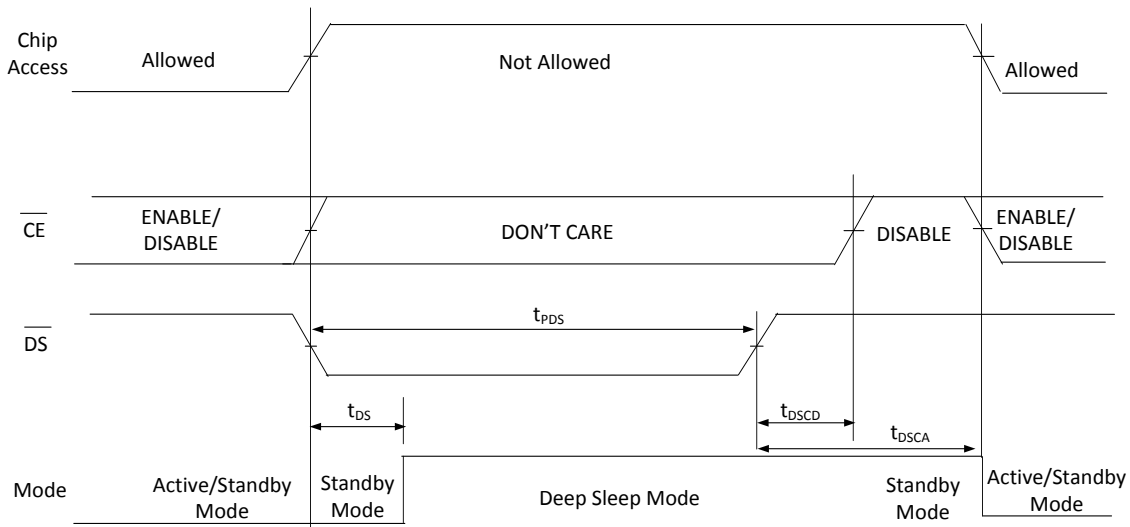
18. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(min)} \geq 100\text{ }\mu\text{s}$.

Deep-Sleep Mode Characteristics

Over the Operating Range of $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$

Parameter	Description	Conditions	Min	Max	Unit
I_{DS}	Deep-Sleep mode current	$V_{CC} = V_{CC}(\text{max})$, $\overline{DS} \leq 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	15	μA
$t_{PDS}^{[19]}$	Minimum time for \overline{DS} to be LOW for part to successfully exit Deep-Sleep mode		100	–	ns
$t_{DS}^{[20]}$	\overline{DS} assertion to Deep-Sleep mode transition time		–	1	ms
$t_{DSCD}^{[19]}$	\overline{DS} deassertion to chip disable	If $t_{PDS} \geq t_{PDS(\text{min})}$	–	100	μs
		If $t_{PDS} < t_{PDS(\text{min})}$	–	0	μs
t_{DSCA}	\overline{DS} deassertion to chip access (Active/Standby)	If $t_{PDS} \geq t_{PDS(\text{min})}$	300	–	μs
		If $t_{PDS} < t_{PDS(\text{min})}$			

Figure 8. Active, Standby, and Deep-Sleep Operation Modes



Note

19. \overline{CE} must be pulled HIGH within t_{DSCD} time of \overline{DS} deassertion to avoid SRAM data loss.

20. After assertion of \overline{DS} signal, device will take a maximum of t_{DS} time to stabilize to Deep-Sleep current I_{DS} . During this period, \overline{DS} signal must continue to be asserted to logic level LOW to keep the device in Deep-Sleep mode.

AC Switching Characteristics

Over the Operating Range of $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$

Parameter ^[21]	Description	10 ns		15 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	10	–	15	–	ns
t_{AA}	Address to data valid	–	10	–	15	ns
t_{OHA}	Data hold from address change	3	–	3	–	ns
t_{ACE}	\overline{CE} LOW to data valid	–	10	–	15	ns
t_{DOE}	\overline{OE} LOW to data valid	–	4.5	–	8	ns
t_{LZOE}	\overline{OE} LOW to low impedance ^[22, 23, 24]	0	–	0	–	ns
t_{HZOE}	\overline{OE} HIGH to HI-Z ^[22, 23, 24]	–	5	–	8	ns
t_{LZCE}	\overline{CE} LOW to low impedance ^[22, 23, 24]	3	–	3	–	ns
t_{HZCE}	\overline{CE} HIGH to HI-Z ^[22, 23, 24]	–	5	–	8	ns
t_{PU}	\overline{CE} LOW to power-up ^[24]	0	–	0	–	ns
t_{PD}	\overline{CE} HIGH to power-down ^[24]	–	10	–	15	ns
t_{DBE}	Byte enable to data valid	–	4.5	–	8	ns
t_{LZBE}	Byte enable to low impedance ^[22, 23, 24]	0	–	0	–	ns
t_{HZBE}	Byte disable to HI-Z ^[22, 23, 24]	–	6	–	8	ns
Write Cycle ^[25, 26]						
t_{WC}	Write cycle time	10	–	15	–	ns
t_{SCE}	\overline{CE} LOW to write end	7	–	12	–	ns
t_{AW}	Address setup to write end	7	–	12	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	\overline{WE} pulse width	7	–	12	–	ns
t_{SD}	Data setup to write end	5	–	8	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{LZWE}	\overline{WE} HIGH to low impedance ^[22, 23, 24]	3	–	3	–	ns
t_{HZWE}	\overline{WE} LOW to HI-Z ^[22, 23, 24]	–	5	–	8	ns
t_{BW}	Byte Enable to End of Write	7	–	12	–	ns

Notes

- Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3\text{ V}$) and $V_{CC}/2$ (for $V_{CC} < 3\text{ V}$), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3\text{ V}$) and 0 to V_{CC} (for $V_{CC} < 3\text{ V}$). Test conditions for the read cycle use output loading shown in part (a) of Figure 6 on page 7, unless specified otherwise.
- t_{HZOE} , t_{HZCE} , t_{HZWE} , t_{HZBE} , t_{LZOE} , t_{LZCE} , t_{LZWE} , and t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of Figure 6 on page 7. Transition is measured $\pm 200\text{ mV}$ from steady state voltage.
- At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
- These parameters are guaranteed by design
- The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$, $\overline{DS} = V_{IH}$ and \overline{BHE} or $\overline{BLE} = V_{IL}$. \overline{WE} , \overline{CE} , \overline{BHE} and \overline{BLE} signals must be LOW and \overline{DS} must be HIGH to initiate a write, and a HIGH transition of any of \overline{WE} , \overline{CE} , \overline{BHE} and \overline{BLE} signals or LOW transition on \overline{DS} signal can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- The minimum write pulse width for Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} LOW) should be the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 9. Read Cycle No. 1 of CY7S1041G (Address Transition Controlled) [27, 28, 29]

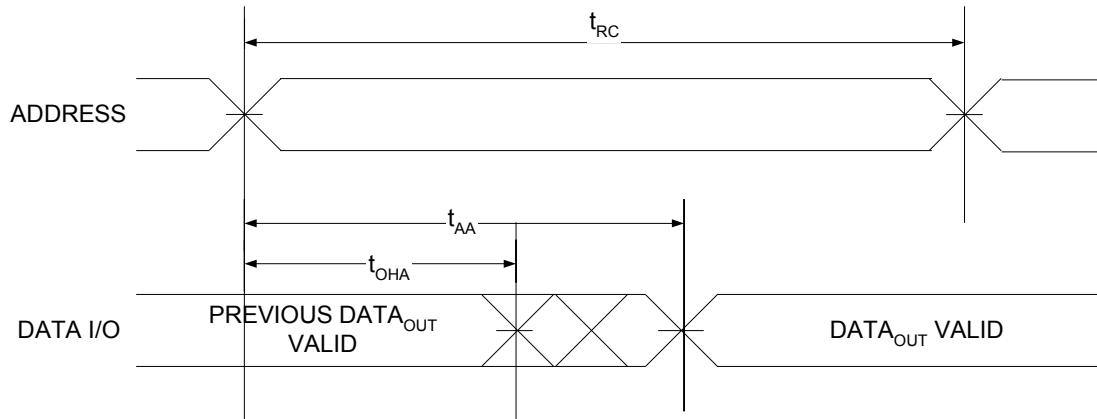
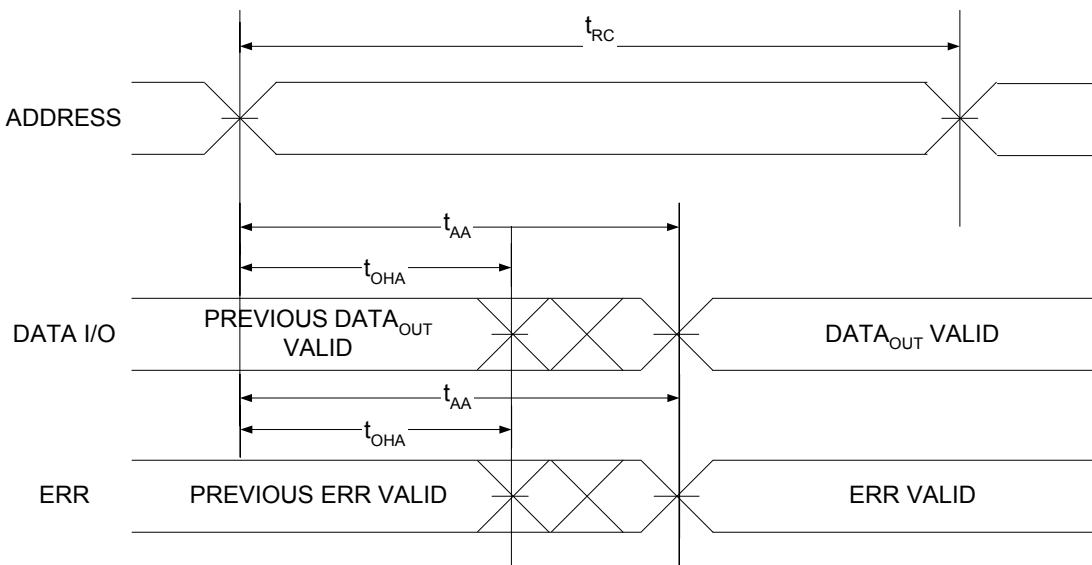


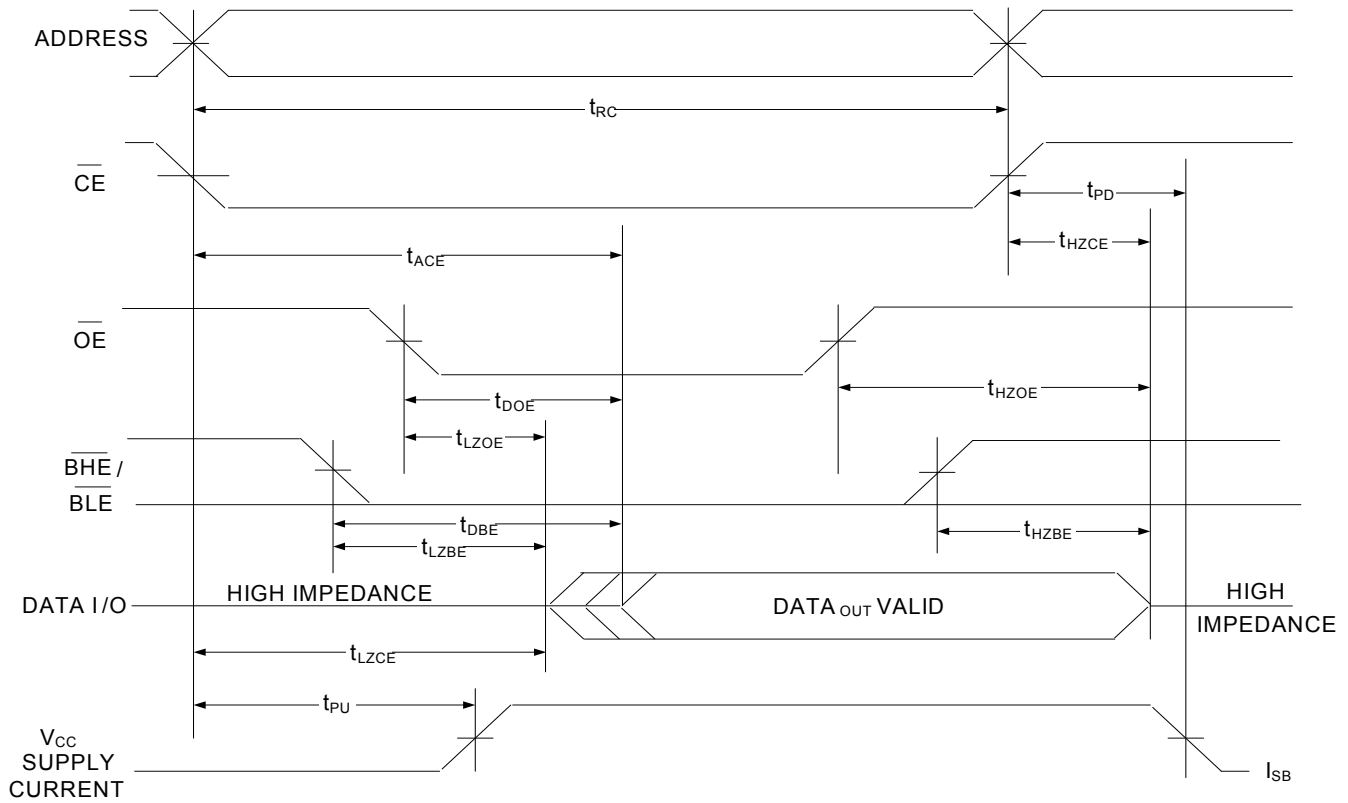
Figure 10. Read Cycle No. 2 of CY7S1041GE (Address Transition Controlled) [27, 28, 29]



Notes

- 27. The device is continuously selected. $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} .
- 28. \overline{WE} is HIGH for read cycle.
- 29. \overline{DS} is HIGH for chip access.

Switching Waveforms (continued)

Figure 11. Read Cycle No. 3 ($\overline{\text{OE}}$ Controlled) [30, 31, 32]

Notes

- 30. $\overline{\text{WE}}$ is HIGH for read cycle.
- 31. Address valid prior to or coincident with $\overline{\text{CE}}$ LOW transition.
- 32. $\overline{\text{DS}}$ must be HIGH for chip access

Switching Waveforms (continued)

Figure 12. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [33, 34, 35]

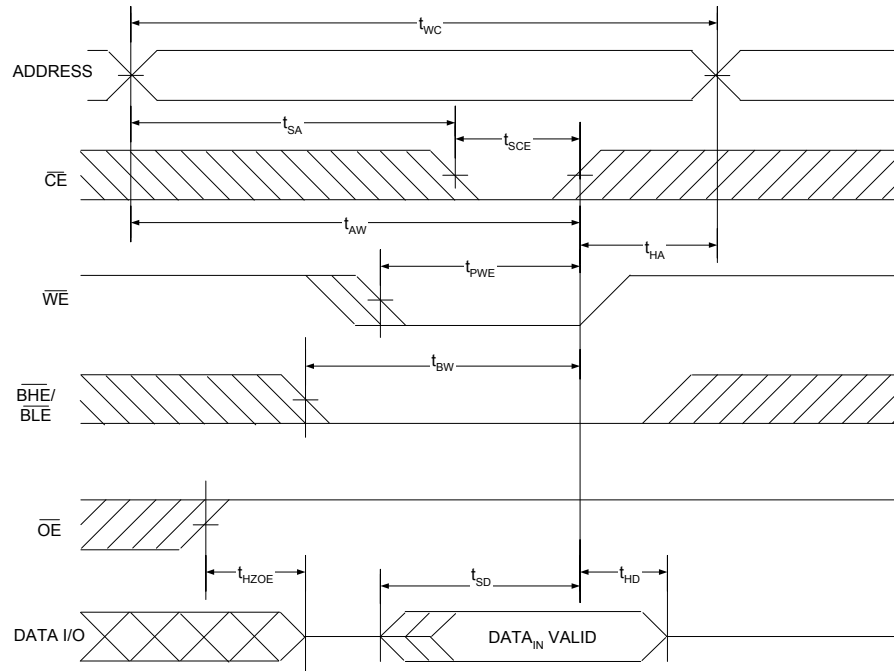
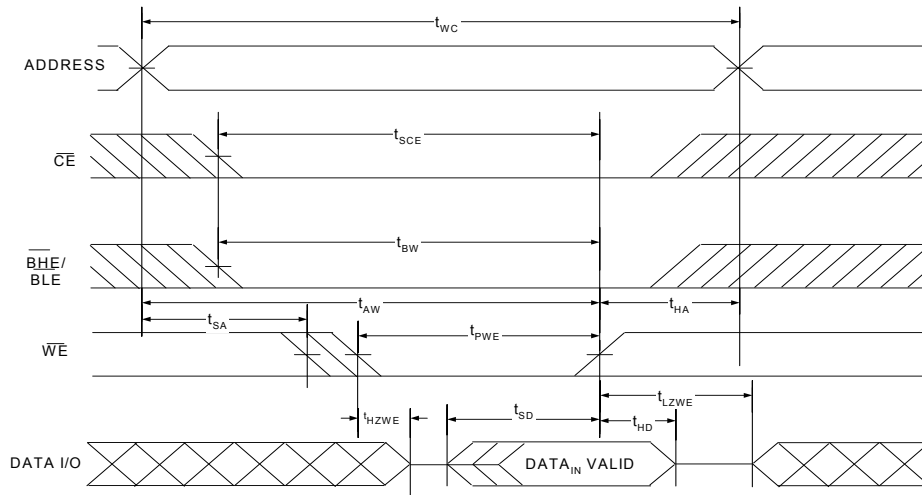


Figure 13. Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [33, 34, 35, 36]



Notes

33. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{\text{IL}}$, $\overline{\text{CE}} = V_{\text{IL}}$, $\overline{\text{DS}} = V_{\text{IH}}$ and $\overline{\text{BHE}}$ or $\overline{\text{BLE}} = V_{\text{IL}}$. $\overline{\text{WE}}$, $\overline{\text{CE}}$, $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$ signals must be LOW and $\overline{\text{DS}}$ must be HIGH to initiate a write, and a HIGH transition of any of $\overline{\text{WE}}$, $\overline{\text{CE}}$, $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$ signals or LOW transition on $\overline{\text{DS}}$ signal can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

34. Data I/O is in HI-Z state if $\overline{\text{CE}} = V_{\text{IH}}$, or $\overline{\text{OE}} = V_{\text{IH}}$ or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{\text{IH}}$.

35. $\overline{\text{DS}}$ must be HIGH for chip access.

36. The minimum write pulse width for Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) should be sum of t_{HZWE} and t_{SD} .

Switching Waveforms (continued)

Figure 14. Write Cycle No. 3 (\overline{WE} Controlled) [37, 38, 39]

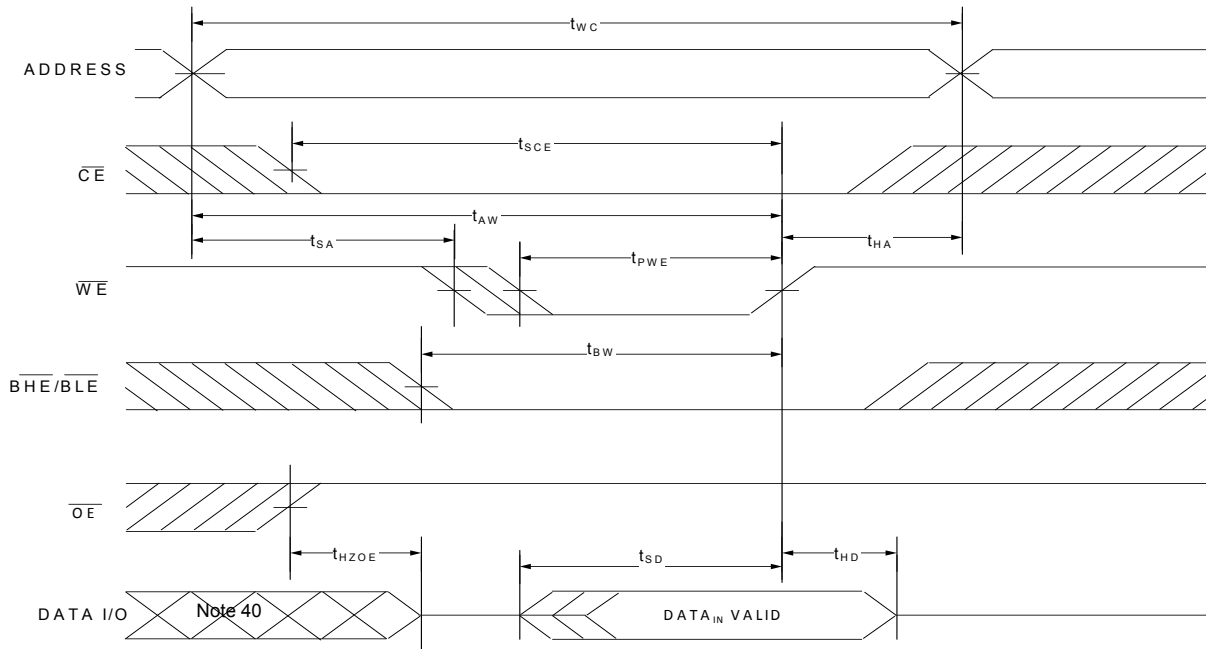
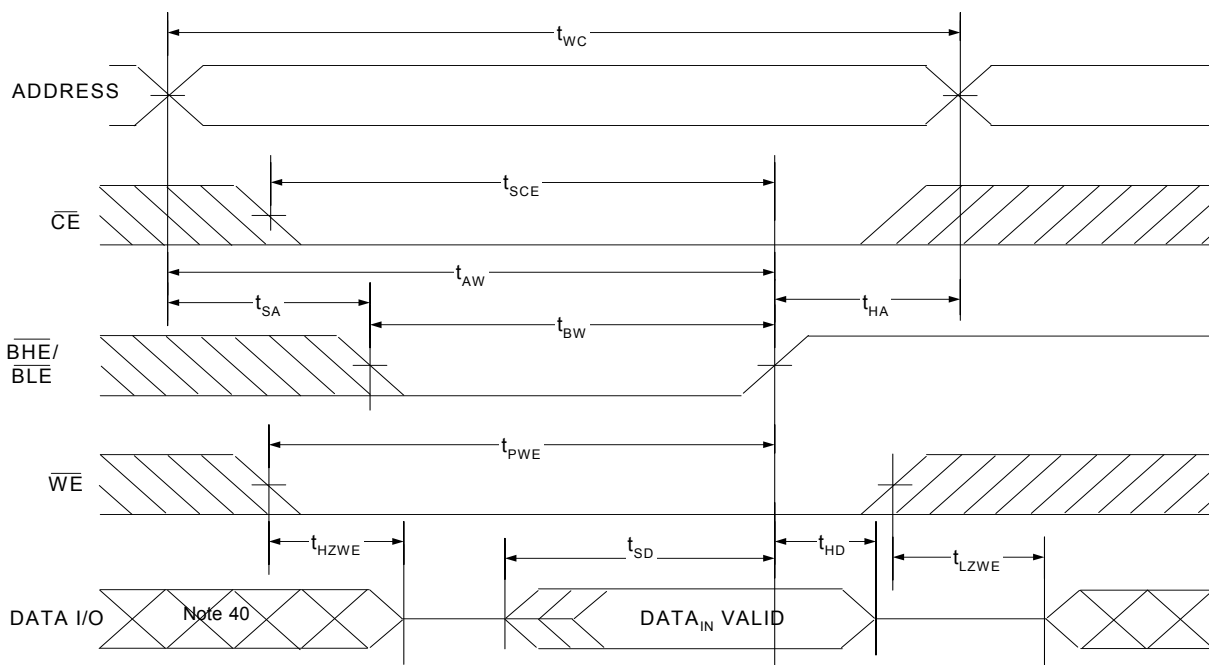


Figure 15. Write Cycle No. 4 (\overline{BLE} or \overline{BHE} Controlled) [37, 38, 39]



Notes

37. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$, $\overline{DS} = V_{IH}$ and \overline{BHE} or $\overline{BLE} = V_{IL}$. \overline{WE} , \overline{CE} , \overline{BHE} and \overline{BLE} signals must be LOW and \overline{DS} must be HIGH to initiate a write, and a HIGH transition of any of \overline{WE} , \overline{CE} , \overline{BHE} and \overline{BLE} signals or LOW transition on \overline{DS} signal can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

38. Data I/O is in HI-Z state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or $\overline{DS} = V_{IL}$ or \overline{BHE} , and/or $\overline{BLE} = V_{IH}$.

39. \overline{DS} must be HIGH for chip access.

40. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

\overline{DS}	\overline{CE}	\overline{OE}	\overline{WE}	\overline{BLE}	\overline{BHE}	I/O ₀ –I/O ₇	I/O ₈ –I/O ₁₅	Mode	Power
H	H	X ^[41]	X ^[41]	X ^[41]	X ^[41]	HIGH-Z	HIGH-Z	Standby	Standby (I _{SB})
H	L	L	H	L	L	Data out	Data out	Read all bits	Active (I _{CC})
H	L	L	H	L	H	Data out	HI-Z	Read lower bits only	Active (I _{CC})
H	L	L	H	H	L	HI-Z	Data out	Read upper bits only	Active (I _{CC})
H	L	X	L	L	L	Data in	Data in	Write all bits	Active (I _{CC})
H	L	X	L	L	H	Data in	HI-Z	Write lower bits only	Active (I _{CC})
H	L	X	L	H	L	HI-Z	Data in	Write upper bits only	Active (I _{CC})
H	L	H	H	X	X	HI-Z	HI-Z	Selected, outputs disabled	Active (I _{CC})
L ^[42]	X	X	X	X	X	HI-Z	HI-Z	Deep-Sleep	Deep-Sleep Ultra Low Power (I _{DS})

ERR Output – CY7S1041GE

Output ^[43]	Mode
0	Read operation, no single-bit error in the stored data.
1	Read operation, single-bit error detected and corrected.
HI-Z	Device deselected or outputs disabled or Write operation.

Notes

41. The input voltage levels on these pins should be either at V_{IH} or V_{IL}.

42. V_{IL} on DS must be ≤ 0.2 V.

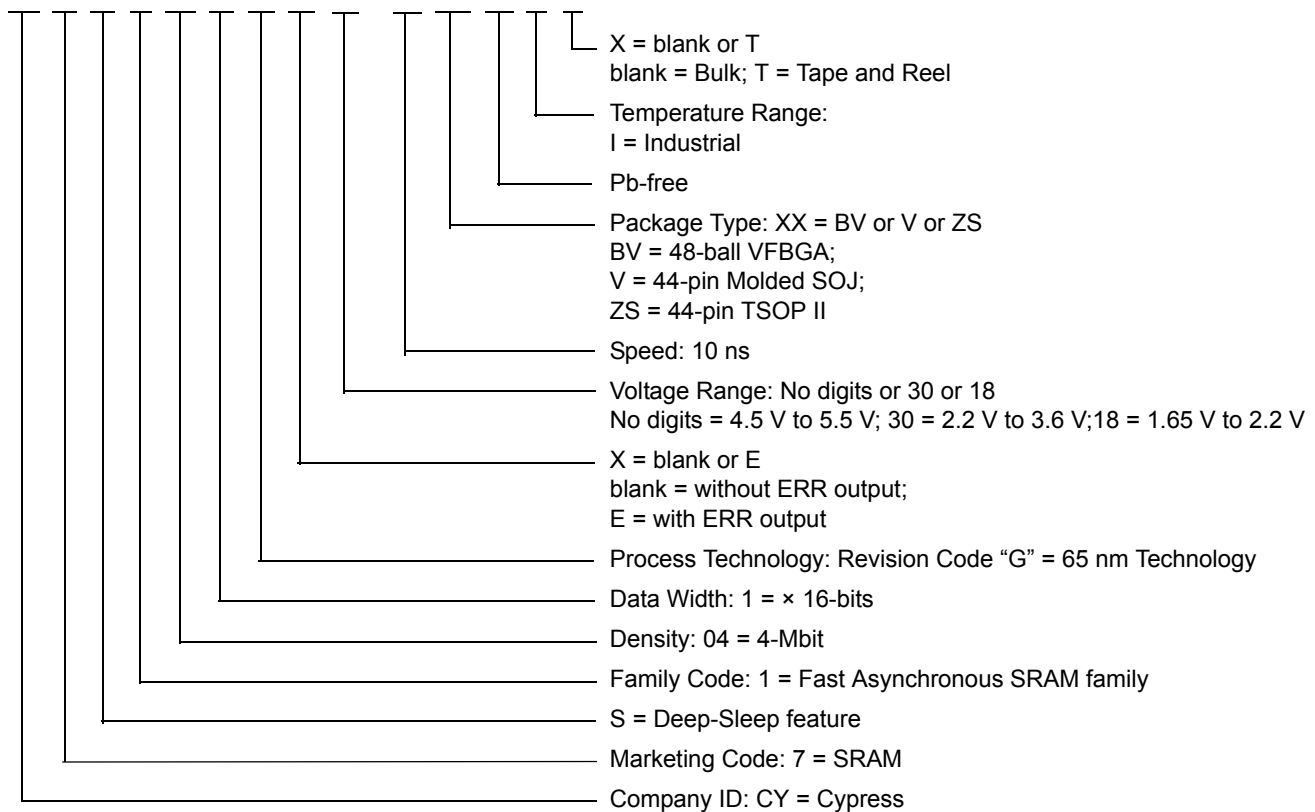
43. ERR is an Output pin. If not used, this pin should be left floating.

Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (All Pb-free)	Operating Range
10	2.2 V–3.6 V	CY7S1041GE30-10BVXI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm), ERR output	Industrial
		CY7S1041GE30-10BVXIT	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm), ERR output, Tape and Reel	
		CY7S1041G30-10BVXI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm)	
		CY7S1041G30-10BVXIT	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm), Tape and Reel	
		CY7S1041G30-10VXI	51-85082	44-pin SOJ (400 Mils)	
		CY7S1041G30-10VXIT	51-85082	44-pin SOJ (400 Mils), Tape and Reel	
		CY7S1041G30-10ZSXI	51-85087	44-pin TSOP II	
		CY7S1041G30-10ZSXIT	51-85087	44-pin TSOP II, Tape and Reel	
4.5 V–5.5 V		CY7S1041G-10ZSXI	51-85087	44-pin TSOP II	
		CY7S1041G-10ZSXIT	51-85087	44-pin TSOP II, Tape and Reel	

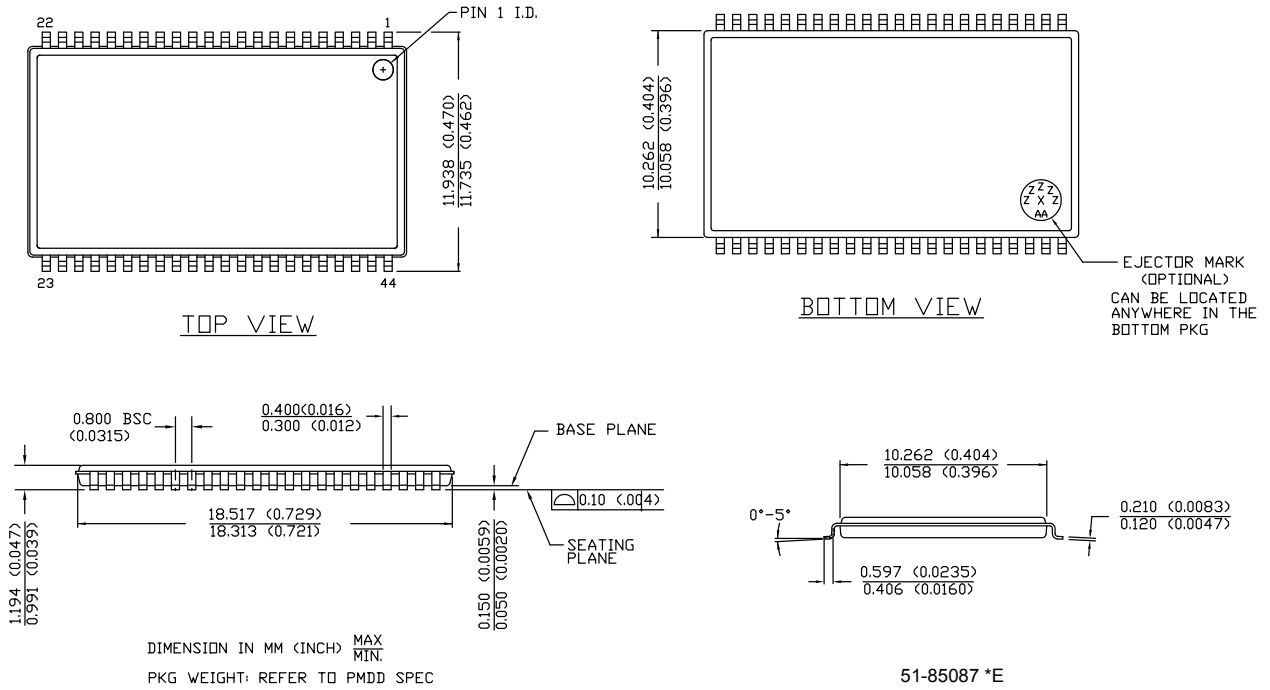
Ordering Code Definitions

CY 7 S 1 04 1 G X 30 - 10 XX X I X



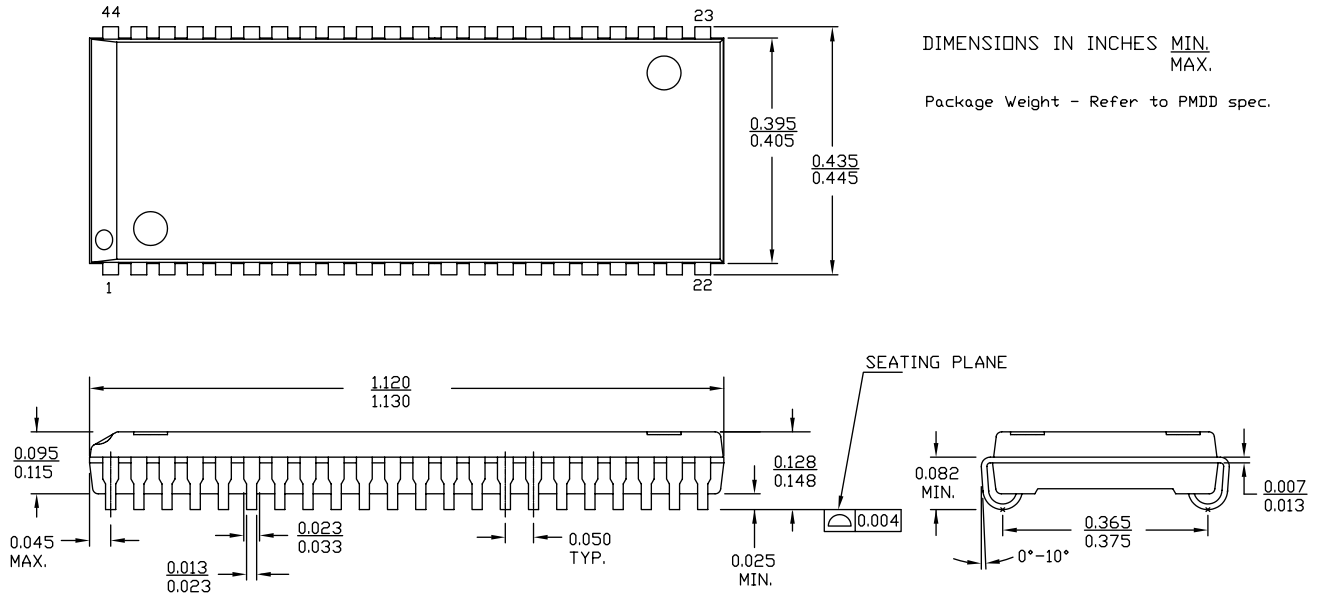
Package Diagrams

Figure 16. 44-pin TSOP II Package Outline, 51-85087



Package Diagrams (continued)

Figure 17. 44-pin SOJ (400 Mils) Package Outline, 51-85082



51-85082 *E

Acronyms

Acronym	Description
BHE	Byte High Enable
BLE	Byte Low Enable
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
ECC	Error Correcting Code
I/O	Input/Output
OE	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
WE	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7S1041G/CY7S1041GE, 4-Mbit (256K words × 16 bit) Static RAM with PowerSnooze™ and Error Correcting Code (ECC)				
Document Number: 001-92576				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*D	4867081	NILE	07/31/2015	Changed status from Preliminary to Final.
*E	5020880	VINI	11/19/2015	Updated Pin Configurations : Removed 44-pin SOJ package related information. Updated Thermal Resistance : Removed 44-pin SOJ package related information. Added 48-ball VFBGA package related information. Updated Ordering Information : Updated part numbers. Updated Ordering Code Definitions . Updated Package Diagrams : Removed spec 51-85082 *E.
*F	5432554	NILE	09/10/2016	Added 44-pin SOJ package related information in all instances across the document. Updated Logic Block Diagram – CY7S1041G / CY7S1041GE . Updated Maximum Ratings : Updated Note 10 (Replaced “2 ns” with “20 ns”). Updated DC Electrical Characteristics : Removed Operating Range “2.7 V to 3.6 V” and all values corresponding to V _{OH} parameter. Included Operating Ranges “2.7 V to 3.0 V” and “3.0 V to 3.6 V” and all values corresponding to V _{OH} parameter. Changed minimum value of V _{IH} parameter from 2.2 V to 2 V corresponding to Operating Range “3.6 V to 5.5 V”. Updated Ordering Information : Updated part numbers. Updated Ordering Code Definitions . Updated Package Diagrams : Added spec 51-85082 *E. Updated to new template. Completing Sunset Review.
*G	6015058	AESATMP9	01/05/2018	Updated logo and copyright.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm [®] Cortex [®] Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC[®] Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2014-2018. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress does not assume any liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View CY7S1041GE30-10BVXI on WIN SOURCE](#)
- ⊖ [Infineon Technologies](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management