



**THE DATASHEET OF  
CY7S1049G30-10VXIT**





## 4-Mbit (512K words × 8-bit) Static RAM with PowerSnooze™ and Error Correcting Code (ECC)

### Features

- High speed
  - Access time ( $t_{AA}$ ) = 10 ns / 15 ns
- Ultra-low power Deep-Sleep (DS) current
  - $I_{DS}$  = 15  $\mu$ A
- Low active and standby currents
  - Active Current  $I_{CC}$  = 38-mA typical
  - Standby Current  $I_{SB2}$  = 6-mA typical
- Wide operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V
- Embedded ECC for single-bit error correction<sup>[1, 2]</sup>
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- 1.0-V data retention
- TTL- compatible inputs and outputs
- Available in Pb-free 44-pin TSOP II, and 36-pin (400-mil) molded SOJ

### Functional Description

The CY7S1049G/CY7S1049GE<sup>[1]</sup> is a high-performance PowerSnooze™ static RAM organized as 512K words × 8 bits. This device features fast access times (10 ns) and a unique

ultra-low power Deep-Sleep mode<sup>[3]</sup>. With Deep-Sleep mode currents as low as 15  $\mu$ A, the CY7S1049G/CY7S1049GE devices combine the best features of fast and low- power SRAMs in industry-standard package options. The device also features embedded ECC. logic which can detect and correct single-bit errors in the accessed location.

Deep-Sleep input ( $\overline{DS}$ ) must be deasserted HIGH for normal operating mode.

To perform data writes, assert the Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW, and provide the data and address on device data pins (I/O<sub>0</sub> through I/O<sub>7</sub>) and address pins (A<sub>0</sub> through A<sub>18</sub>) respectively.

To perform data reads, assert the Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) inputs LOW and provide the required address on the address lines. Read data is accessible on the I/O lines (I/O<sub>0</sub> through I/O<sub>7</sub>).

The device is placed in a low-power Deep-Sleep mode when the Deep-Sleep input ( $\overline{DS}$ ) is asserted LOW. In this state, the device is disabled for normal operation and is placed in a low power data retention mode. The device can be activated by deasserting the Deep-Sleep input ( $\overline{DS}$ ) to HIGH.

The CY7S1049G is available in 44-pin TSOP II, and 36-pin Molded SOJ (400 Mils).

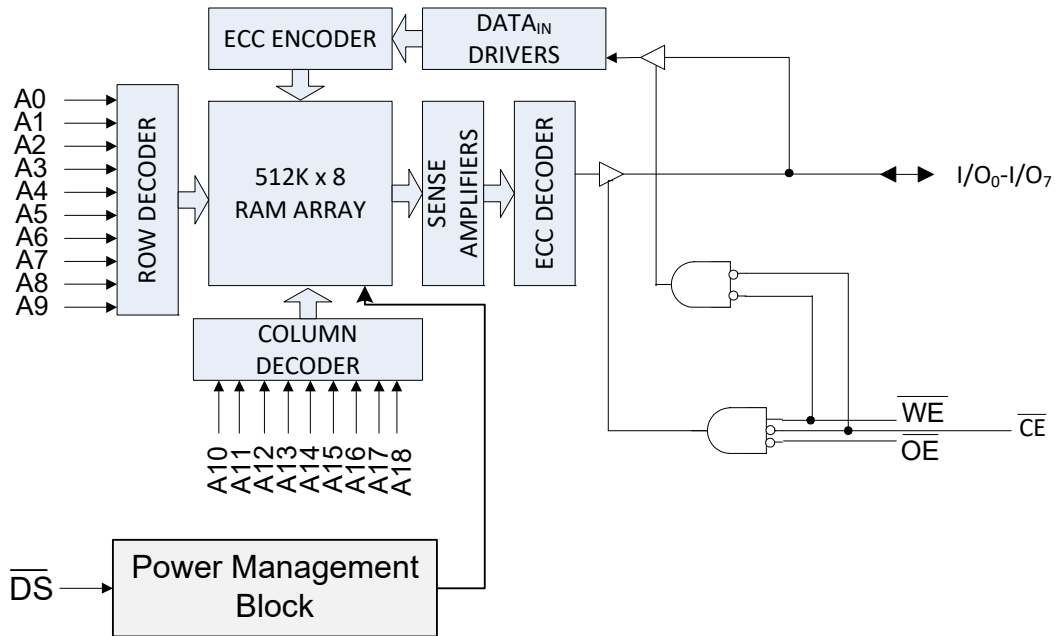
### Product Portfolio

Product <sup>[4]</sup>	Range	V <sub>CC</sub> Range (V)	Speed (ns)	Power Dissipation							
				Operating I <sub>CC</sub> (mA)		Standby, I <sub>SB2</sub> (mA)		Deep-Sleep current ( $\mu$ A)			
				f = f <sub>max</sub>		Typ <sup>[5]</sup>	Max	Typ <sup>[5]</sup>	Max	Typ <sup>[5]</sup>	Max
				Typ <sup>[5]</sup>	Max						
CY7S1049G(E)18	Industrial	1.65 V–2.2 V	15	–	40	6	8	–	15		
CY7S1049G(E)30		2.2 V–3.6 V	10	38	45						
CY7S1049G(E)		4.5–5.5 V	10	38	45						

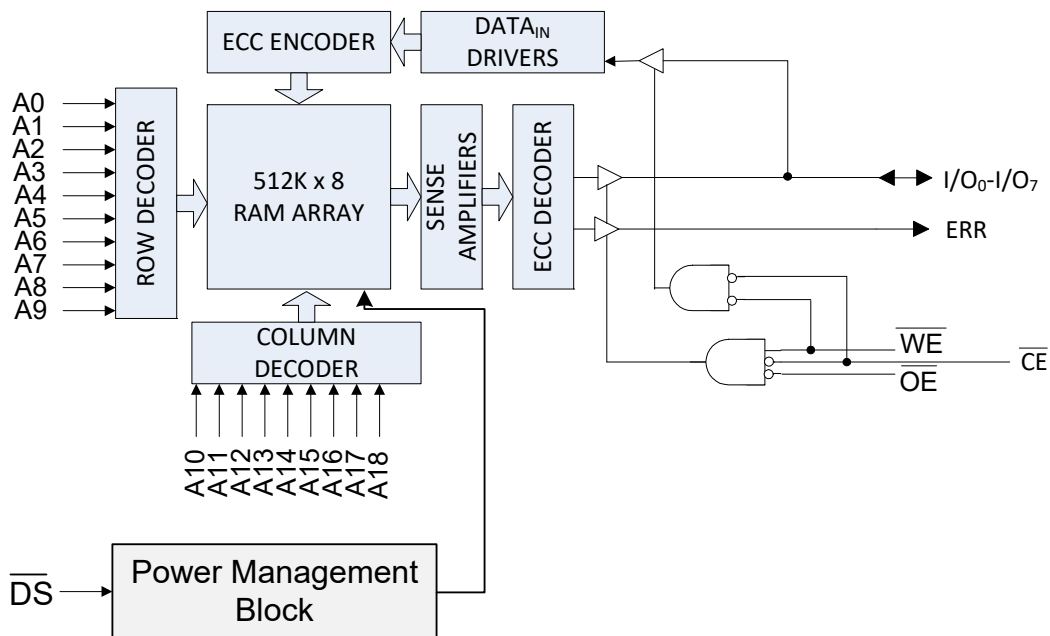
#### Notes

1. This device does not support automatic write back on error detection.
2. SER FIT Rate <0.1 FIT/Mb. Refer AN88889 for details.
3. Refer AN89371 for details on PowerSnooze™ feature.
4. ERR pin is available only for devices which have ERR option "E" in the ordering code. Refer Ordering Information on page 17 for details.
5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 1.8 V (for V<sub>CC</sub> range of 1.65 V–2.2 V), V<sub>CC</sub> = 3 V (for V<sub>CC</sub> range of 2.2 V–3.6 V), and V<sub>CC</sub> = 5 V (for V<sub>CC</sub> range of 4.5 V–5.5 V), T<sub>A</sub> = 25 °C.

**Logic Block Diagram – CY7S1049G**



**Logic Block Diagram – CY7S1049GE**



## Contents

<b>Pin Configurations</b> .....	<b>4</b>	<b>Ordering Information</b> .....	<b>17</b>
<b>Maximum Ratings</b> .....	<b>6</b>	Ordering Code Definitions .....	17
<b>Operating Range</b> .....	<b>6</b>	<b>Package Diagrams</b> .....	<b>18</b>
<b>DC Electrical Characteristics</b> .....	<b>6</b>	<b>Acronyms</b> .....	<b>19</b>
<b>Capacitance</b> .....	<b>7</b>	<b>Document Conventions</b> .....	<b>19</b>
<b>Thermal Resistance</b> .....	<b>7</b>	Units of Measure .....	19
<b>AC Test Loads and Waveforms</b> .....	<b>8</b>	<b>Document History Page</b> .....	<b>20</b>
<b>Data Retention Characteristics</b> .....	<b>9</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>21</b>
<b>Data Retention Waveform</b> .....	<b>9</b>	Worldwide Sales and Design Support .....	21
<b>Deep-Sleep Mode Characteristics</b> .....	<b>10</b>	Products .....	21
<b>AC Switching Characteristics</b> .....	<b>11</b>	PSoC® Solutions .....	21
<b>Switching Waveforms</b> .....	<b>12</b>	Cypress Developer Community .....	21
<b>Truth Table</b> .....	<b>16</b>	Technical Support .....	21
<b>ERR Output – CY7S1049GE</b> .....	<b>16</b>		

## Pin Configurations

Figure 1. 44-pin TSOP II pinout without ERR [6]

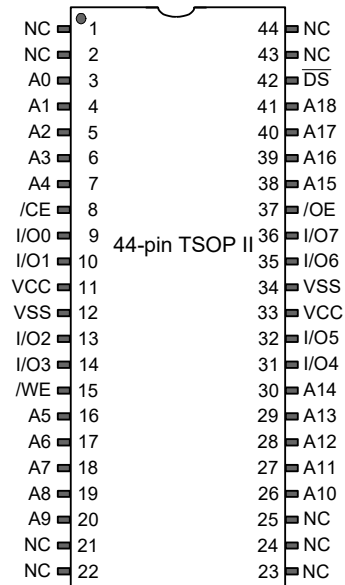
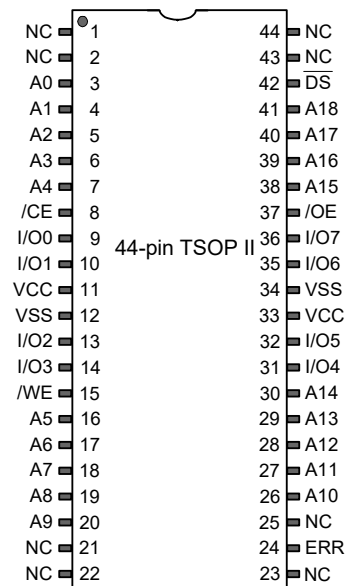


Figure 2. 44-pin TSOP II pinout with ERR [6, 7]



### Notes

6. NC pins are not connected internally to the die.
7. ERR is an output pin.

Pin Configurations (continued)

Figure 3. 36-pin SOJ pinout without ERR [8]

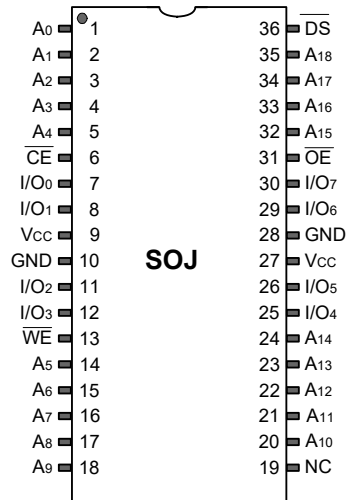
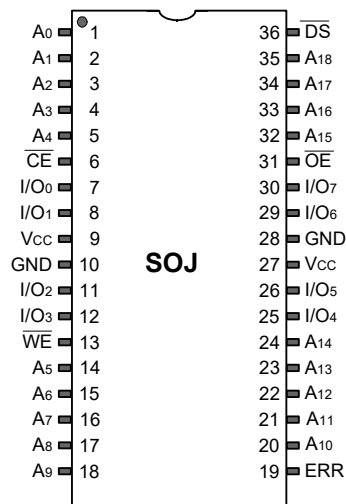


Figure 4. 36-pin SOJ pinout with ERR [8, 9]



Notes

- 8. NC pins are not connected internally to the die.
- 9. ERR is an output pin.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature  
with power applied ..... -55 °C to +125 °C

Supply voltage  
on V<sub>CC</sub> relative to GND <sup>[10]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V

DC voltage applied to outputs  
in HI-Z State <sup>[10]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V

DC input voltage <sup>[10]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage  
(MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 140 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

## DC Electrical Characteristics

Over the Operating Range of -40 °C to +85 °C

Parameter	Description	Test Conditions	10 ns/ 15 ns			Unit	
			Min	Typ <sup>[11]</sup>	Max		
V <sub>OH</sub>	Output HIGH voltage	1.65 V to 2.2 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1 mA	1.4	-	-	V
		2.2 V to 2.7 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -1.0 mA	2	-	-	
		2.7 V to 3.6 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.4	-	-	
		4.5 V to 5.5 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.4	-	-	
		4.5 V to 5.5 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> - 0.5 <sup>[12]</sup>	-	-	
V <sub>OL</sub>	Output LOW voltage	1.65 V to 2.2 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 0.1 mA	-	-	0.2	V
		2.2 V to 2.7 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 2 mA	-	-	0.4	
		2.7 V to 3.6 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8 mA	-	-	0.4	
		4.5 V to 5.5 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8 mA	-	-	0.4	
V <sub>IH</sub> <sup>[10, 13]</sup>	Input HIGH voltage	1.65 V to 2.2 V	-	1.4	-	V <sub>CC</sub> + 0.2	V
		2.2 V to 2.7 V	-	2	-	V <sub>CC</sub> + 0.3	
		2.7 V to 3.6 V	-	2	-	V <sub>CC</sub> + 0.3	
		4.5 V to 5.5 V	-	2	-	V <sub>CC</sub> + 0.5	
V <sub>IL</sub> <sup>[10, 13]</sup>	Input LOW voltage	1.65 V to 2.2 V	-	-0.2	-	0.4	V
		2.2 V to 2.7 V	-	-0.3	-	0.6	
		2.7 V to 3.6 V	-	-0.3	-	0.8	
		4.5 V to 5.5 V	-	-0.5	-	0.8	
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	-	+1	μA	
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output disabled	-1	-	+1	μA	
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA, CMOS levels	f = 100 MHz	-	38	45	mA
			f = 66.7 MHz	-	-	40	
I <sub>SB1</sub>	Standby current – TTL inputs	Max V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	-	-	15	mA	

### Notes

10. V<sub>IL</sub> (min) = -2.0 V and V<sub>IH</sub> (max) = V<sub>CC</sub> + 2 V for pulse durations of less than 20 ns.

11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 1.8 V (for V<sub>CC</sub> range of 1.65 V–2.2 V), V<sub>CC</sub> = 3 V (for V<sub>CC</sub> range of 2.2 V–3.6 V), and V<sub>CC</sub> = 5 V (for V<sub>CC</sub> range of 4.5 V–5.5 V), T<sub>A</sub> = 25 °C.

12. Guaranteed by design and not tested.

13. For the DS pin, V<sub>IH</sub> (min) is V<sub>CC</sub> - 0.2 V and V<sub>IL</sub> (max) is 0.2 V.

## DC Electrical Characteristics (continued)

Over the Operating Range of  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

Parameter	Description	Test Conditions	10 ns/ 15 ns			Unit
			Min	Typ <sup>[11]</sup>	Max	
$I_{SB2}$	Standby current – CMOS inputs	Max $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ , $\overline{DS} \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ , $f = 0$	–	6	8	mA
$I_{DS}$	Deep-Sleep current	Max $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ , $\overline{DS} \leq 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ , $f = 0$	–	–	15	$\mu\text{A}$

## Capacitance

Parameter <sup>[14]</sup>	Description	Test Conditions	All packages	Unit
$C_{IN}$	Input capacitance	$T_A = 25\text{ }^{\circ}\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC(\text{typ})}$	10	pF
$C_{OUT}$	I/O capacitance		10	pF

## Thermal Resistance

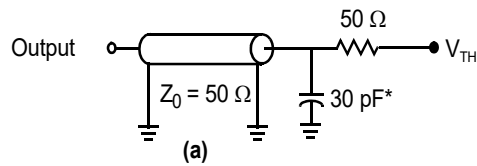
Parameter <sup>[14]</sup>	Description	Test Conditions	36-pin SOJ Package	44-pin TSOP II Package	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Still air, soldered on a $3 \times 4.5$ inch, four-layer printed circuit board	59.52	68.85	$^{\circ}\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		31.48	15.97	$^{\circ}\text{C/W}$

### Note

14. Tested initially and after any design or process changes that may affect these parameters.

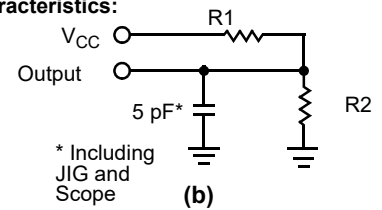
## AC Test Loads and Waveforms

Figure 5. AC Test Loads and Waveforms [15]

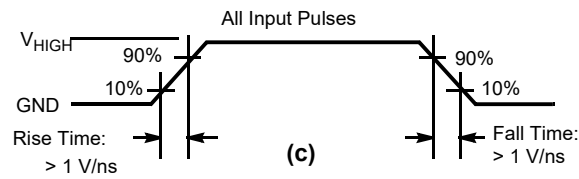


\* Capacitive Load Consists of all Components of the Test Environment

HI-Z Characteristics:



\* Including JIG and Scope



Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	$\Omega$
R2	1538	351	351	$\Omega$
$V_{TH}$	$V_{CC}/2$	1.5	1.5	V
$V_{HIGH}$	1.8	3.0	3.0	V

**Note**

15. Full-device AC operation assumes a 100- $\mu$ s ramp time from 0 to  $V_{CC(min)}$  or 100- $\mu$ s wait time after  $V_{CC}$  stabilization.

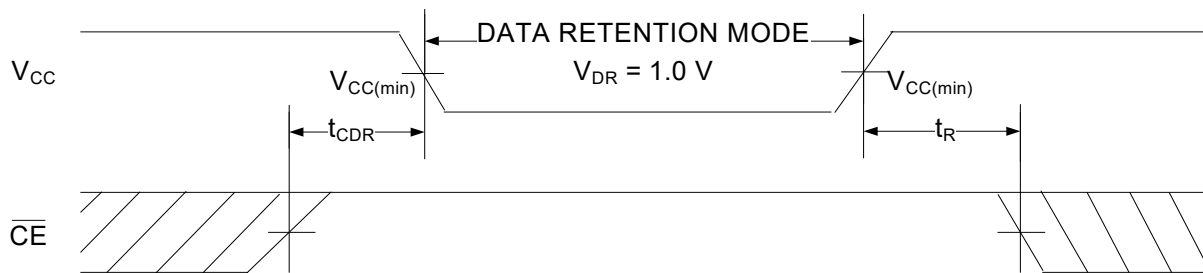
## Data Retention Characteristics

Over the Operating Range of  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

Parameter	Description	Conditions <sup>[16]</sup>	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention	–	1.0	–	V
$I_{CCDR}$	Data retention current	$V_{CC} = V_{DR}$ , $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ , $\overline{DS} \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	8	mA
$t_{CDR}$ <sup>[17]</sup>	Chip deselect to data retention time	–	0	–	ns
$t_R$ <sup>[17, 18]</sup>	Operation recovery time	$2.2\text{ V} < V_{CC} \leq 5.5\text{ V}$	10	–	ns
		$V_{CC} \leq 2.2\text{ V}$	15	–	ns

## Data Retention Waveform

Figure 6. Data Retention Waveform <sup>[18]</sup>



### Notes

16. DS signal must be HIGH during Data Retention Mode.

17. These parameters are guaranteed by design.

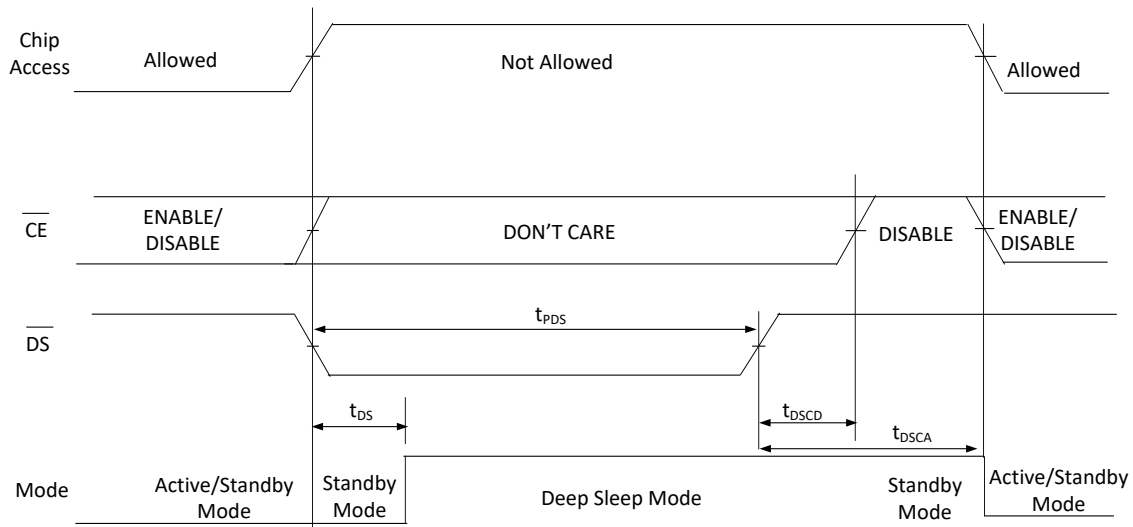
18. Full-device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(min.)} \geq 100\text{ }\mu\text{s}$ .

## Deep-Sleep Mode Characteristics

Over the Operating Range of  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

Parameter	Description	Conditions	Min	Max	Unit
$I_{DS}$	Deep-Sleep mode current	$V_{CC} = V_{CC}(\text{max})$ , $\overline{DS} \leq 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	15	$\mu\text{A}$
$t_{PDS}^{[19]}$	Minimum time for $\overline{DS}$ to be LOW for part to successfully exit Deep-Sleep mode	–	100	–	ns
$t_{DS}^{[20]}$	$\overline{DS}$ assertion to Deep-Sleep mode transition time	–	–	1	ms
$t_{DSCD}^{[19]}$	$\overline{DS}$ deassertion to chip disable	If $t_{PDS} \geq t_{PDS(\text{min})}$	–	100	$\mu\text{s}$
		If $t_{PDS} < t_{PDS(\text{min})}$	–	0	$\mu\text{s}$
$t_{DSCA}$	$\overline{DS}$ deassertion to chip access (Active/Standby)	If $t_{PDS} \geq t_{PDS(\text{min})}$	300	–	$\mu\text{s}$
		If $t_{PDS} < t_{PDS(\text{min})}$	–	–	–

**Figure 7. Active, Standby, and Deep-Sleep Operation Modes**



### Notes

19. CE must be pulled HIGH within  $t_{DSCD}$  time of  $\overline{DS}$  de-assertion to avoid SRAM data loss.

20. After assertion of  $\overline{DS}$  signal, device will take a maximum of  $t_{DS}$  time to stabilize to Deep-Sleep current  $I_{DS}$ . During this period,  $\overline{DS}$  signal must continue to be asserted to logic level LOW to keep the device in Deep-Sleep mode.

## AC Switching Characteristics

Over the Operating Range of  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

Parameter <sup>[21]</sup>	Description	10 ns		15 ns		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
$t_{RC}$	Read cycle time	10	–	15	–	ns
$t_{AA}$	Address to data valid	–	10	–	15	ns
$t_{OHA}$	Data hold from address change	3	–	3	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid	–	10	–	15	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	4.5	–	8	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low impedance <sup>[22, 23, 24]</sup>	0	–	0	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to HI-Z <sup>[22, 23, 24]</sup>	–	5	–	8	ns
$t_{LZCE}$	$\overline{CE}$ LOW to low impedance <sup>[22, 23, 24]</sup>	3	–	3	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to HI-Z <sup>[22, 23, 24]</sup>	–	5	–	8	ns
$t_{PU}$	$\overline{CE}$ LOW to power-up <sup>[24]</sup>	0	–	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to power-down <sup>[24]</sup>	–	10	–	15	ns
<b>Write Cycle <sup>[25, 26]</sup></b>						
$t_{WC}$	Write cycle time	10	–	15	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	7	–	12	–	ns
$t_{AW}$	Address setup to write end	7	–	12	–	ns
$t_{HA}$	Address hold from write end	0	–	0	–	ns
$t_{SA}$	Address setup to write start	0	–	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	7	–	12	–	ns
$t_{SD}$	Data setup to write end	5	–	8	–	ns
$t_{HD}$	Data hold from write end	0	–	0	–	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low impedance <sup>[22, 23, 24]</sup>	3	–	3	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to HI-Z <sup>[22, 23, 24]</sup>	–	5	–	8	ns

### Notes

21. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for  $V_{CC} \geq 3\text{ V}$ ) and  $V_{CC}/2$  (for  $V_{CC} < 3\text{ V}$ ), and input pulse levels of 0 to 3 V (for  $V_{CC} \geq 3\text{ V}$ ) and 0 to  $V_{CC}$  (for  $V_{CC} < 3\text{ V}$ ). Test conditions for the read cycle use output loading shown in part (a) of [Figure 5 on page 8](#), unless specified otherwise.
22.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZWE}$ ,  $t_{LZOE}$ ,  $t_{LZCE}$ , and  $t_{LZWE}$  are specified with a load capacitance of 5 pF as in (b) of [Figure 5 on page 8](#). Transition is measured  $\pm 200\text{ mV}$  from steady state voltage.
23. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
24. These parameters are guaranteed by design.
25. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{DS} = V_{IH}$  and  $\overline{WE}$ ,  $\overline{CE}$ , signals must be LOW and  $\overline{DS}$  must be HIGH to initiate a write, and a HIGH transition of any of  $\overline{WE}$ ,  $\overline{CE}$ , signals or LOW transition on  $\overline{DS}$  signal can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
26. The minimum write pulse width for Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be the sum of  $t_{HZWE}$  and  $t_{SD}$ .

## Switching Waveforms

Figure 8. Read Cycle No. 1 of CY7S1049G (Address Transition Controlled) [27, 28, 29]

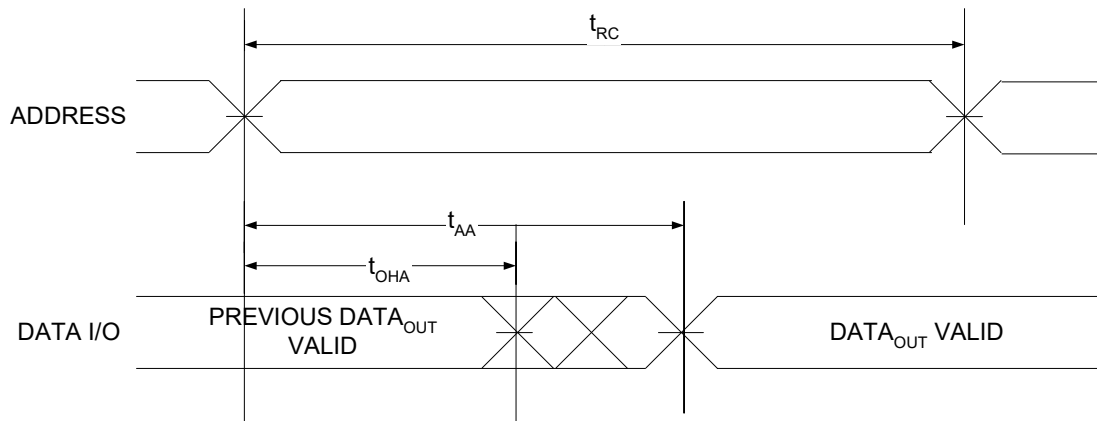
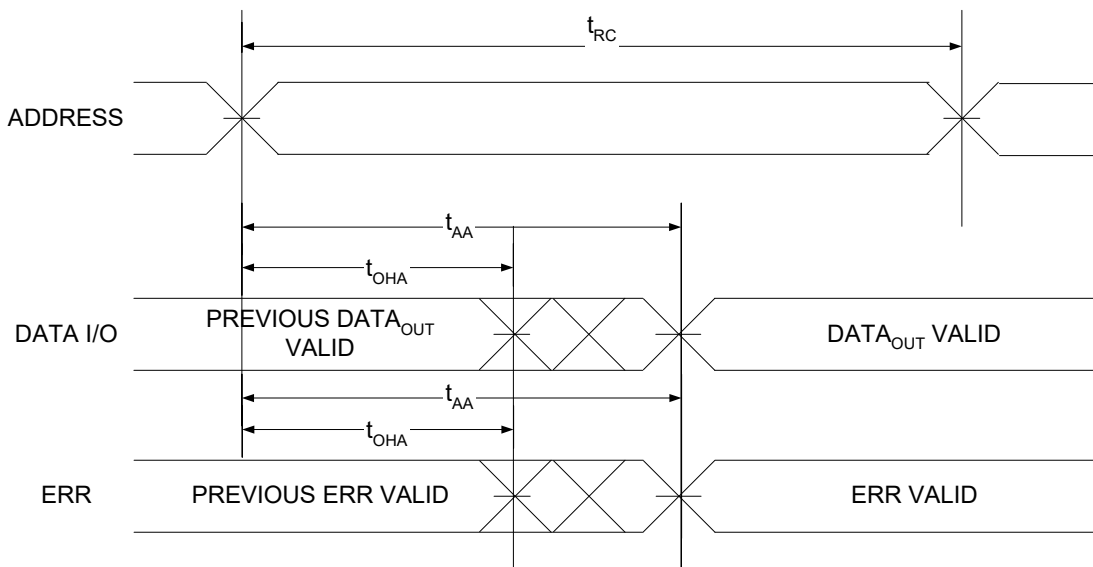


Figure 9. Read Cycle No. 2 of CY7S1041GE (Address Transition Controlled) [27, 28, 29]

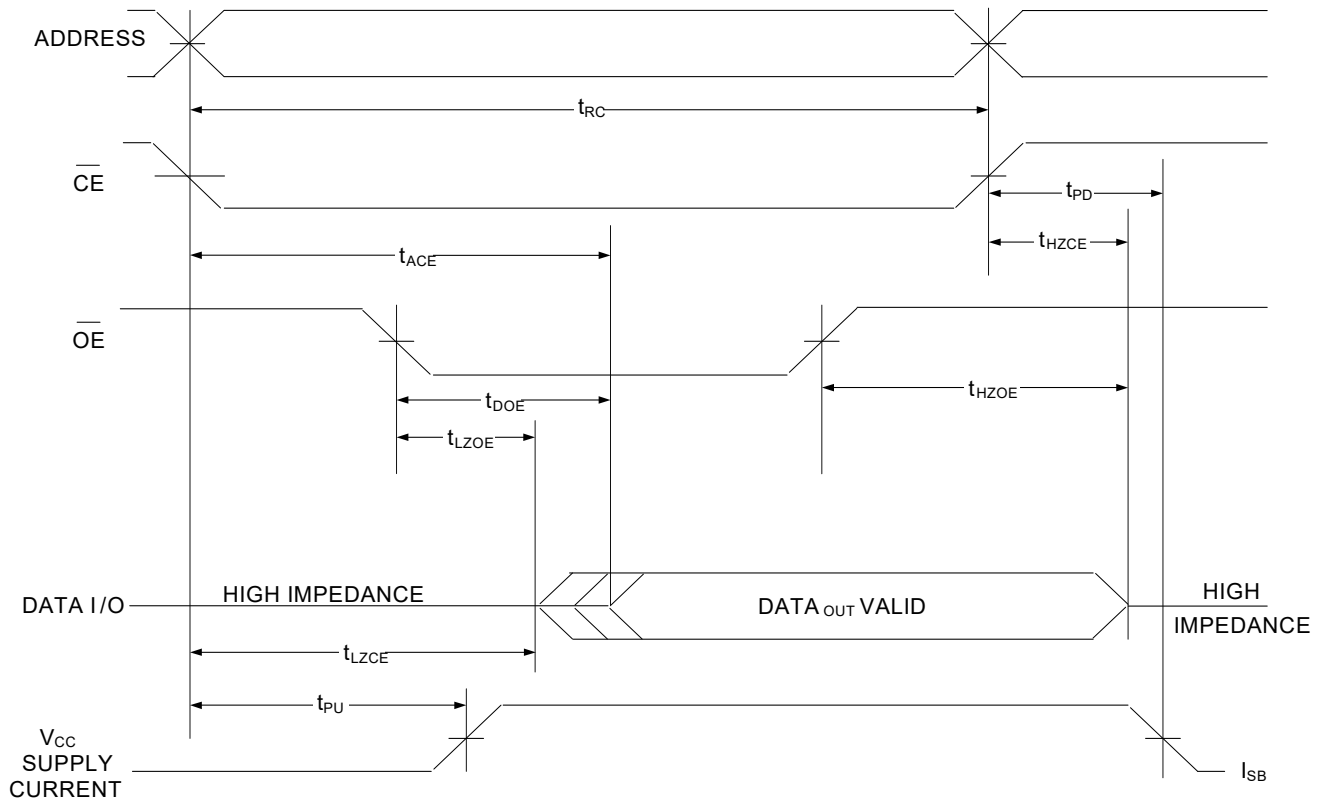


### Notes

- 27. The device is continuously selected.  $\overline{OE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ .
- 28.  $\overline{WE}$  is HIGH for read cycle.
- 29.  $\overline{DS}$  is HIGH for chip access.

Switching Waveforms (continued)

Figure 10. Read Cycle No. 3 ( $\overline{\text{OE}}$  Controlled) [30, 31, 32]



Notes

- 30.  $\overline{\text{WE}}$  is HIGH for read cycle.
- 31. Address valid prior to or coincident with  $\overline{\text{CE}}$  LOW transition.
- 32.  $\overline{\text{DS}}$  must be HIGH for chip access.

Switching Waveforms (continued)

Figure 11. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled) [33, 34, 35]

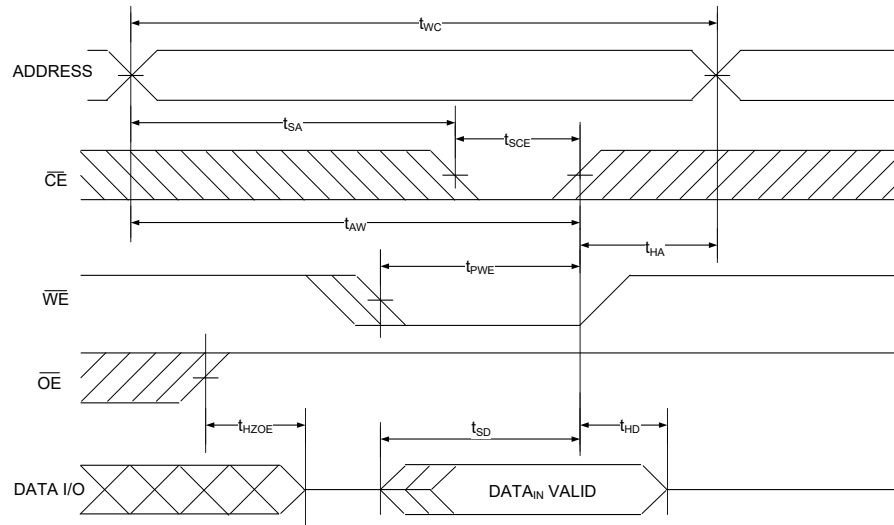
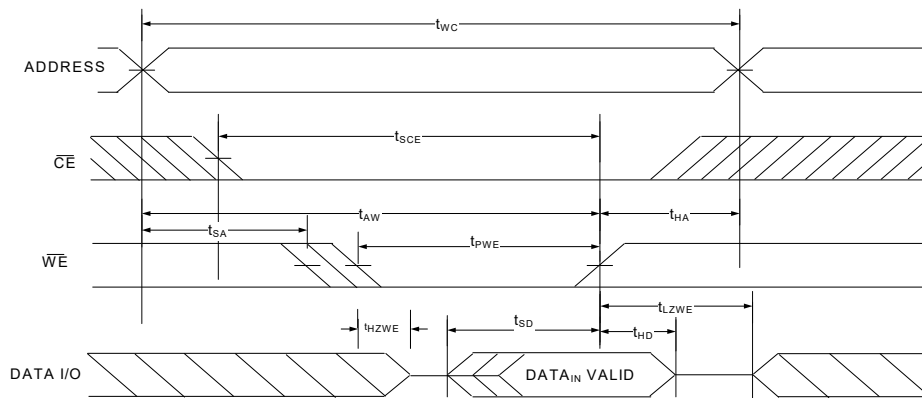


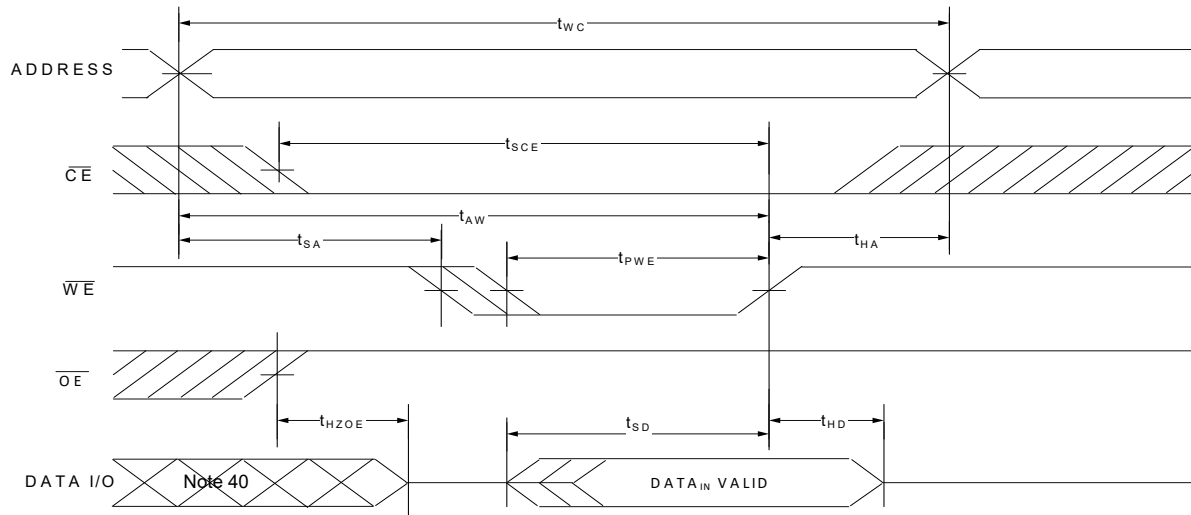
Figure 12. Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [33, 34, 35, 36]



Notes

33. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{IL}$ ,  $\overline{\text{CE}} = V_{IL}$ ,  $\overline{\text{DS}} = V_{IH}$  and  $\overline{\text{WE}}$ ,  $\overline{\text{CE}}$  signals must be LOW and  $\overline{\text{DS}}$  must be HIGH to initiate a write, and a HIGH transition of any of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}}$  signals or LOW transition on  $\overline{\text{DS}}$  signal can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
34. Data I/O is in HI-Z state if  $\overline{\text{CE}} = V_{IH}$ , or  $\overline{\text{OE}} = V_{IH}$ .
35.  $\overline{\text{DS}}$  must be HIGH for chip access.
36. The minimum write pulse width for Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) should be sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

**Switching Waveforms** (continued)

**Figure 13. Write Cycle No. 3 ( $\overline{WE}$  Controlled)** [37, 38, 39]

**Notes**

37. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{DS} = V_{IH}$  and  $\overline{WE}$ ,  $\overline{CE}$ , signals must be LOW and  $\overline{DS}$  must be HIGH to initiate a write, and a HIGH transition of any of  $\overline{WE}$ ,  $\overline{CE}$ , signals or LOW transition on  $\overline{DS}$  signal can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
38. Data I/O is in HI-Z state if  $\overline{CE} = V_{IH}$ , or  $\overline{OE} = V_{IH}$  or  $\overline{DS} = V_{IL}$ .
39.  $\overline{DS}$  must be HIGH for chip access.
40. During this period, the I/Os are in output state. Do not apply input signals.

### Truth Table

$\overline{DS}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	Mode	Power
H	H	X <sup>[41]</sup>	X <sup>[41]</sup>	HIGH-Z	Standby	Standby (I <sub>SB</sub> )
H	L	L	H	Data out	Read all bits	Active (I <sub>CC</sub> )
H	L	X	L	Data in	Write all bits	Active (I <sub>CC</sub> )
H	L	H	H	HI-Z	Selected, outputs disabled	Active (I <sub>CC</sub> )
L <sup>[42]</sup>	X	X	X	HI-Z	Deep-Sleep	Deep-Sleep Ultra Low Power (I <sub>DS</sub> )

### ERR Output – CY7S1049GE

Output <sup>[43]</sup>	Mode
0	Read operation, no single-bit error in the stored data.
1	Read operation, single-bit error detected and corrected.
High-Z	Device deselected / outputs disabled / Write operation

#### Notes

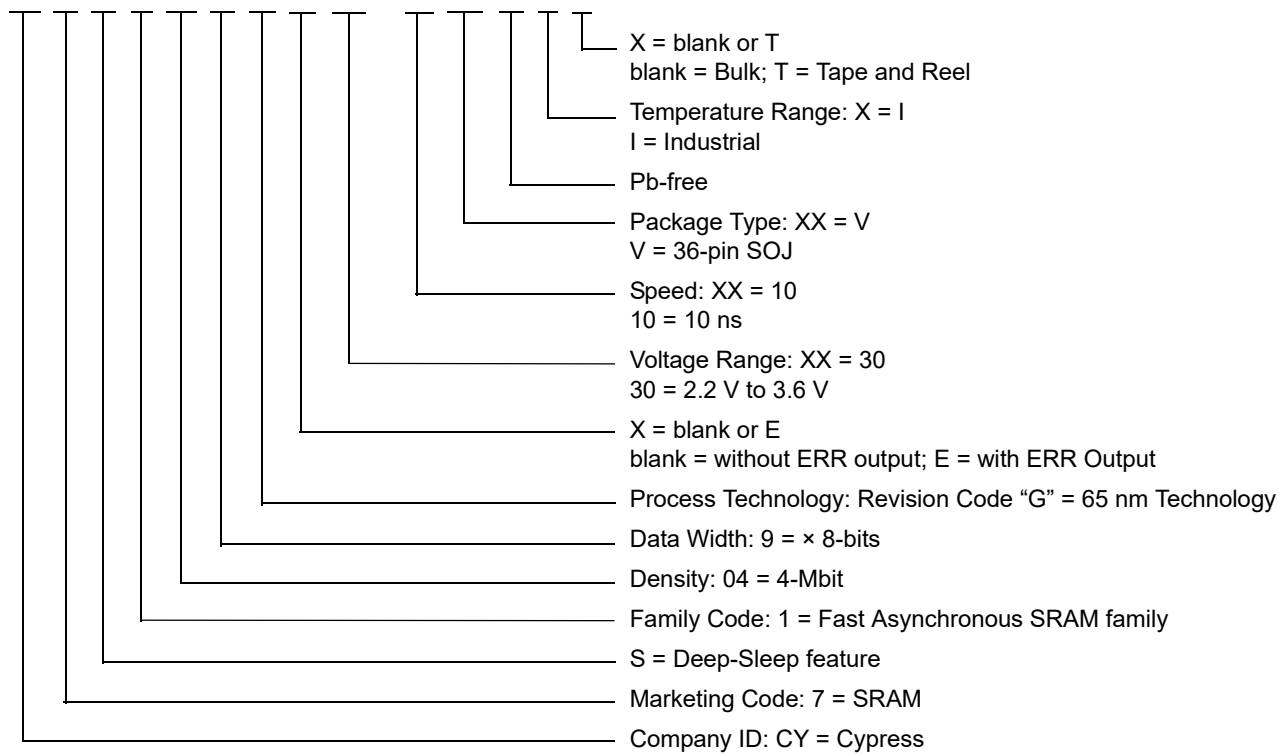
41. The input voltage levels on these pins should be either at V<sub>IH</sub> or V<sub>IL</sub>.  
 42. V<sub>IL</sub> on  $\overline{DS}$  must be  $\leq 0.2$  V.  
 43. ERR is an Output pin. If not used, this pin should be left floating.

### Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (All Pb-free)	Operating Range
10	2.2 V–3.6 V	CY7S1049G30-10VXI	51-85090	36-pin SOJ	Industrial
		CY7S1049G30-10VXIT	51-85090	36-pin SOJ, Tape and Reel	
		CY7S1049GE30-10VXI	51-85090	36-pin SOJ, ERR Output	
		CY7S1049GE30-10VXIT	51-85090	36-pin SOJ, ERR Output, Tape and Reel	

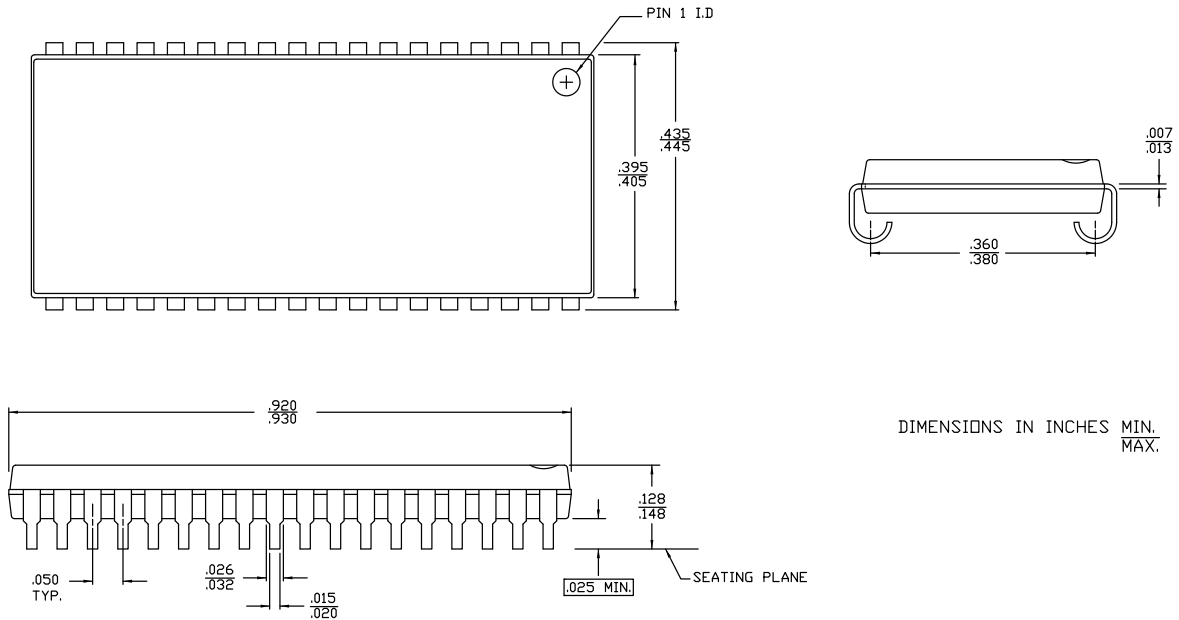
### Ordering Code Definitions

CY 7 S 1 04 9 G X XX - XX XX X X X



**Package Diagrams**

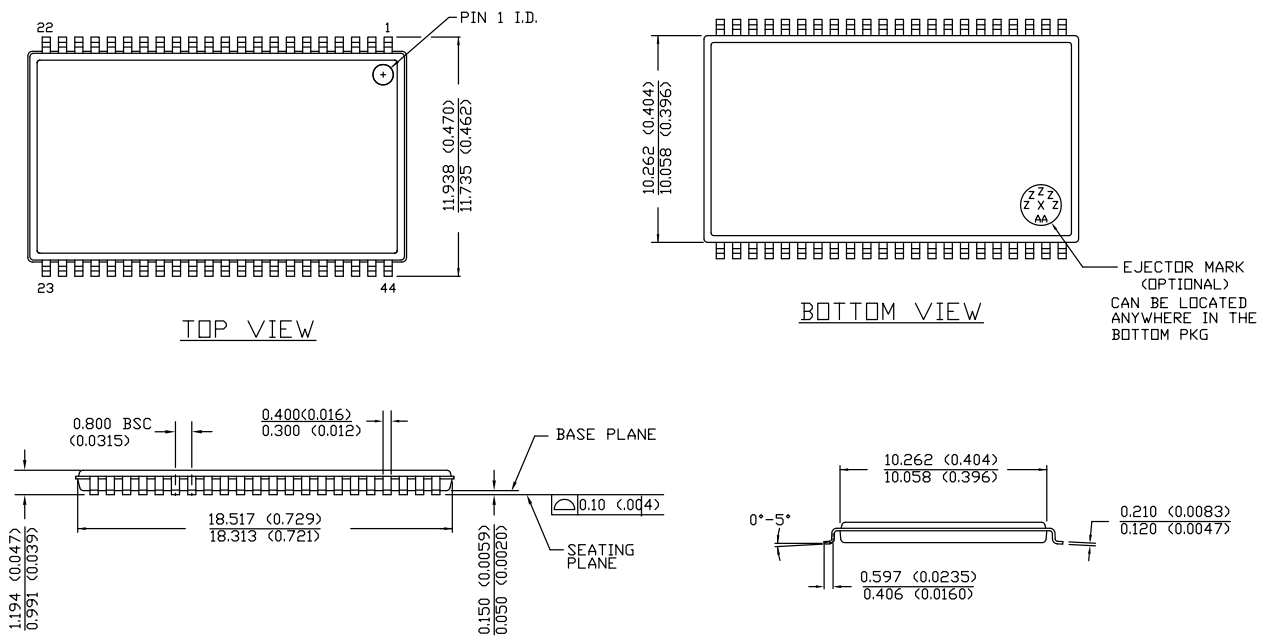
**Figure 14. 36-pin SOJ V36.4 (Molded) Package Outline, 51-85090**



DIMENSIONS IN INCHES MIN. MAX.

51-85090 \*G

**Figure 15. 44-pin TSOP II Package Outline, 51-85087**



TOP VIEW

BOTTOM VIEW

EJECTOR MARK (OPTIONAL) CAN BE LOCATED ANYWHERE IN THE BOTTOM PKG

DIMENSION IN MM (INCH) MAX MIN. PKG WEIGHT: REFER TO PMDD SPEC

51-85087 \*E

## Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SOJ	Small-Outline J-lead
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable
ECC	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7S1049G/CY7S1049GE, 4-Mbit (512K words × 8-bit) Static RAM with PowerSnooze™ and Error Correcting Code (ECC)				
Document Number: 001-95414				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*B	5025315	VINI	11/24/2015	Changed status from Preliminary to Final.
*C	5090263	NILE	01/18/2016	Updated <a href="#">Ordering Information</a> : Updated part numbers. Completing Sunset Review.
*D	5428860	NILE	09/07/2016	Updated <a href="#">Functional Description</a> : Added Note 1 and referred the same note in "CY7S1049G/CY7S1049GE". Updated <a href="#">Maximum Ratings</a> : Updated Note 10 (Replaced "2 ns" with "20 ns"). Updated <a href="#">DC Electrical Characteristics</a> : Changed minimum value of $V_{OH}$ parameter from 2.2 V to 2.4 V corresponding to Operating Range "2.7 V to 3.6 V" and Test Condition " $V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$ ". Changed minimum value of $V_{IH}$ parameter from 2.2 V to 2 V corresponding to Operating Range "4.5 V to 5.5 V". Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated to new template.
*E	5981584	AESATMP8	12/01/2017	Updated logo and Copyright.
*F	6120487	NILE	04/03/2018	Updated <a href="#">Features</a> : Referred Note 1 in "Embedded ECC for single-bit error correction". Added Note 2 and referred the same note in "Embedded ECC for single-bit error correction". Updated <a href="#">Functional Description</a> : Added Note 3 and referred the same note at the end of sentence "This device features fast access times (10 ns) and a unique ultra-low power Deep-Sleep mode". Updated to new template. Completing Sunset Review.

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