THE DATASHEET OF

CYPM1211-40LQXI

EZ-PD™ PMG1-S2 Power Delivery MCU

EZ-PD™ PMG1 family general description

EZ-PD™ PMG1 (Power Delivery Microcontroller Gen1) is a family of high-voltage USB-C Power Delivery (PD) microcontrollers (MCU). These chips include an Arm® Cortex®-M0/M0+ CPU and USB-C PD controller along with analog and digital peripherals. EZ-PD™ PMG1 is targeted for any embedded system that provides/consumes powers to/from a high-voltage USB-C PD port and leverages the microcontroller to provide additional control capability. **Figure 1** shows the EZ-PD™ PMG1 family segmentation.

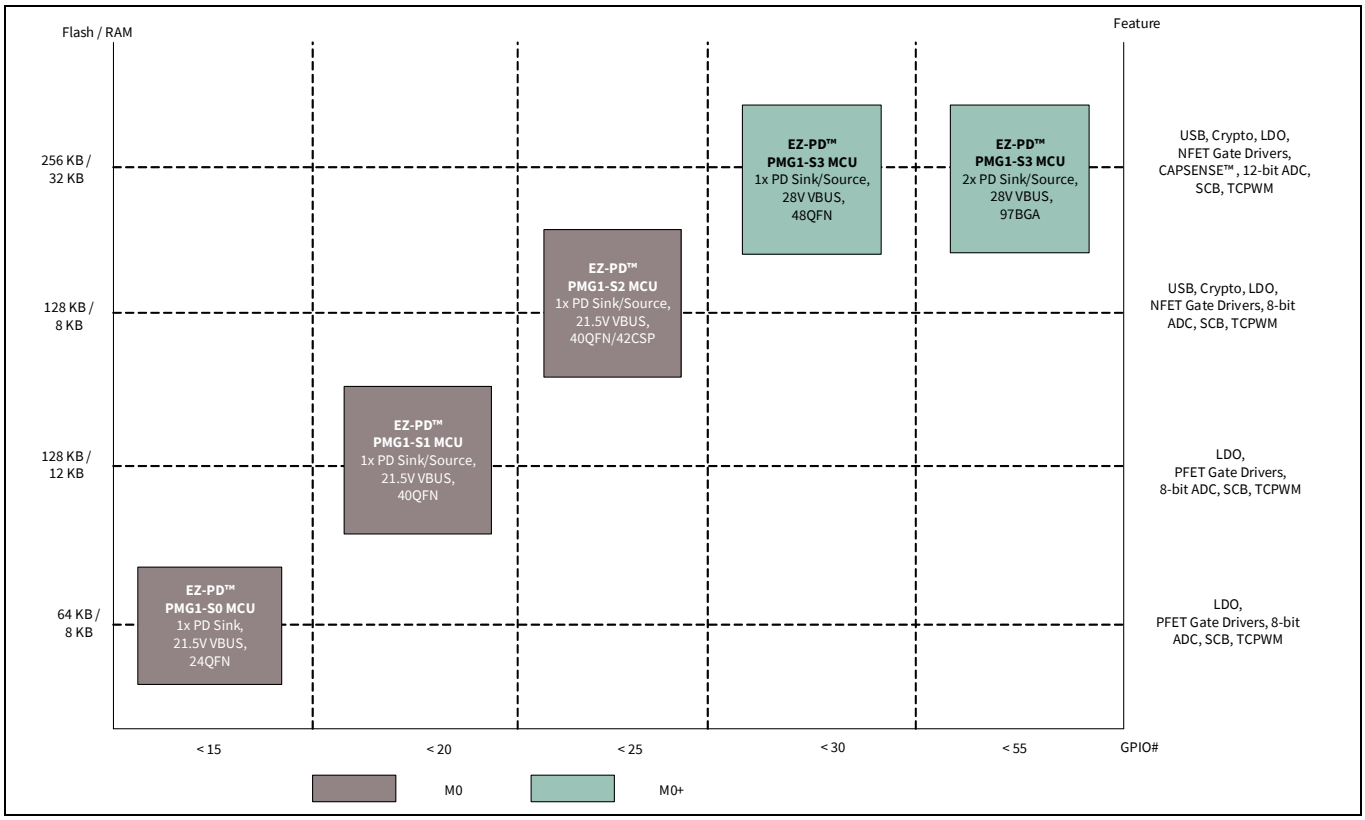


Figure 1 EZ-PD™ PMG1 family segmentation

Table 1 shows the comparison of features of different MCUs of the EZ-PD™ PMG1 family.

Table 1 Comparison of features of different EZ-PD™ PMG1 family MCUs

Subsystem or range	Item	EZ-PD™ PMG1-S0	EZ-PD™ PMG1-S1	EZ-PD™ PMG1-S2	EZ-PD™ PMG1-S3
CPU & Memory Subsystem	Core	Arm® Cortex®-M0	Arm® Cortex®-M0	Arm® Cortex®-M0	Arm® Cortex®-M0+
	Max Freq (MHz)	48	48	48	48
	Flash (KB)	64	128	128	256
	SRAM (KB)	8	12	8	32
Power Delivery	Power Delivery Ports	1	1	1	1 port for 48-QFN 2 ports for 97-BGA
	Role	Sink	DRP	DRP	DRP
	MOSFET Gate Drivers	1x PFET	2x PFET	2x NFET	Flexible 2x NFET
	Fault Protections	VBUS OVP and UVP	VBUS OVP, UVP, and OCP SCP and RCP (for Source Configuration only)	VBUS OVP, UVP, and OCP	VBUS OVP, UVP, and OCP SCP and RCP (for Source Configuration only)
USB	Integrated Full Speed USB 2.0 Device with Billboard Class support	No	No	Yes	Yes
Voltage Range	Supply (V)	VDDD (2.7 - 5.5) VBUS (4 - 21.5)	VSYS (2.75 - 5.5) VBUS (4 - 21.5)	VSYS (2.7 - 5.5) VBUS (4 - 21.5)	VSYS (2.8–5.5) VBUS (4–28)
	IO (V)	1.71 - 5.5	1.71 - 5.5	1.71 - 5.5	1.71 – 5.5
Digital	SCB (configurable as I2C/UART/SPI)	2	4	4	7 for 48-QFN (out of which only 5 can be configured as SPI and UART) 8 for 97-BGA
	TCPWM Block (configurable as timer, counter or pulse width modulator)	4	2	4	7 for 48-QFN 8 for 97-BGA
	Hardware Authentication Block (Crypto)	No	No	Yes (AES-128/192/256, SHA1, SHA2-224, SHA2-256, PRNG, CRC)	Yes (AES-128, SHA2-256, TRNG, Vector Unit)
Analog	ADC	2x 8-bit SAR	1x 8-bit SAR	2x 8-bit SAR	2x 8-bit SAR 1x 12-bit SAR
	On-chip Temperature Sensor	Yes	Yes	Yes	Yes

Table 1 Comparison of features of different EZ-PD™ PMG1 family MCUs *(continued)*

Subsystem or range	Item	EZ-PD™ PMG1-S0	EZ-PD™ PMG1-S1	EZ-PD™ PMG1-S2	EZ-PD™ PMG1-S3
Direct Memory Access (DMA)	DMA	No	No	No	Yes
GPIO	Max # of I/O	12(10+2 OVT)	17(15+2 OVT)	20(18+2 OVT)	26 (24+2 OVT) for 48-QFN 50 (48+2 OVT) for 97-BGA
Charging Standards	Charging Source	-	BC 1.2, AC	BC 1.2, AC	BC 1.2, AC, AFC and Quick Charge 3.0
	Charging Sink	BC 1.2, Apple Charging (AC)	BC 1.2, AC	BC 1.2, AC	BC 1.2, AC
ESD Protection	ESD Protection	Yes (Up to ± 8-kV contact discharge, up to ±15-kV air discharge, human body model (HBM), and charged device model (CDM))	Yes (HBM and CDM)	Yes (Up to ± 8-kV contact discharge, up to ±15-kV air discharge, Human body model and charged device model)	Yes (HBM and CDM)
Packages	Package Options	24-QFN (4x4 mm, 0.5-mm pitch)	40-QFN (6×6 mm, 0.5-mm pitch)	40-QFN (6×6 mm, 0.5-mm pitch) 42-CSP(2.63x3.18 mm, 0.4 mm pitch)	48-QFN (6x6 mm, 0.5-mm pitch) 97-BGA (6x6 mm, 0.5 mm and 0.65 mm pitch)

The rest of this document discusses the EZ-PD™ PMG1-S2 device in detail.

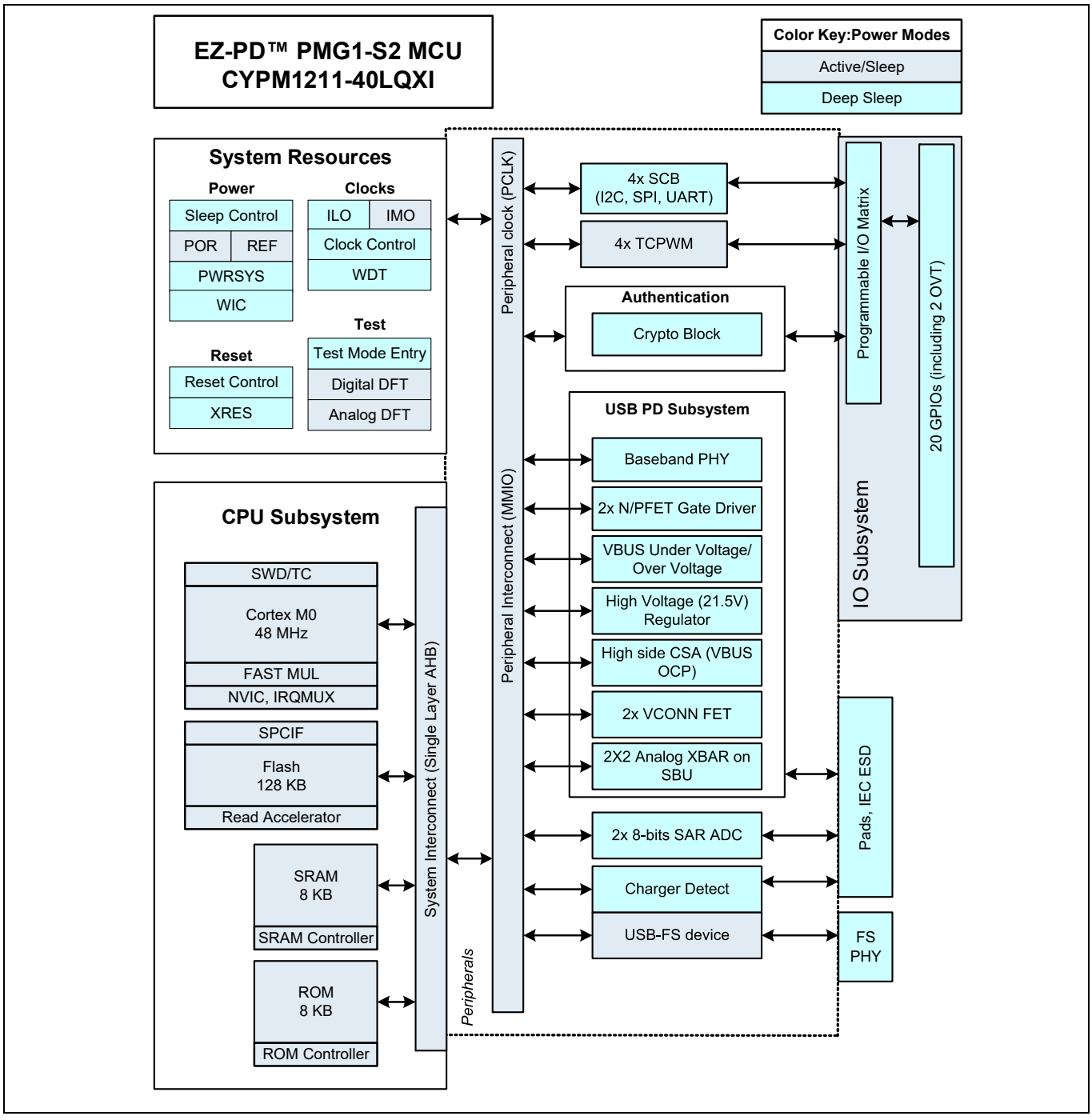
EZ-PD™ PMG1-S2 general description

EZ-PD™ PMG1-S2 has 128-KB flash, 8-KB SRAM, 20 GPIOs, full-speed USB device controller, a crypto engine for authentication, a 20V-tolerant regulator, and a pair of FETs to switch a 5 V (VCONN) supply. EZ-PD™ PMG1-S2 also integrates two pairs of gate drivers to control external VBUS FETs and system level ESD protection. EZ-PD™ PMG1-S2 is available in 40-QFN and 42-CSP package.

Features

- Type-C and USB PD support
  - Supports one USB Type-C port
  - Integrated USB Power Delivery 3.0 support
  - Integrated USB PD BMC transceiver
  - Integrated VCONN FETs
  - Configurable resistors R_P and R_D
  - Dead battery detection support
  - Integrated fast role swap and extended data messaging
  - Integrated hardware based overcurrent protection (OCP) and overvoltage protection (OVP)
- 32-bit MCU subsystem
  - 48-MHz ARM® Cortex®-M0 CPU
  - 128-KB Flash
  - 8-KB SRAM
- Integrated digital blocks
  - Hardware crypto block enables authentication
  - Full-Speed USB device controller supporting Billboard Device Class
  - Integrated timers and counters to meet response times required by the USB PD protocol
  - Four run-time reconfigurable serial communication blocks (SCBs) with reconfigurable I^2C, SPI, or UART functionality
- Clocks and oscillators
  - Integrated oscillator eliminating the need for external clock
- Power
  - VSYS(2.7 V–5.5 V)
  - VBUS (4.0 V–21.5 V)
  - 2x integrated dual-output gate drivers for external VBUS FET switch control
  - Independent supply voltage pin for GPIO that allows 1.71 V to 5.5 V signaling on the I/Os
  - Reset: 30 µA, Deep Sleep: 30 µA, Sleep: 3.5 mA
- System-level ESD protection
  - On CC, SBU, USBDP, USBDM, and VBUS pins
  - ± 8-kV Contact Discharge and ±15-kV Air Gap Discharge based on IEC61000-4-2 level 4C
- Packages
  - 40-pin QFN and 42-ball CSP
  - Supports industrial temperature range (–40°C to +105°C)

Block diagram



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1 Development support

The EZ-PD™ PMG1 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit **EZ-PD™ PMG1 MCU** webpage to find out more.

1.1 Documentation

A suite of documentation supports the EZ-PD™ PMG1 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software user guide: A step-by-step guide for using ModusToolbox™ software. The software user guide shows you how ModusToolbox™ software build process works in detail, how to use source control with ModusToolbox™ software, and much more.

Component datasheets: The flexibility of EZ-PD™ PMG1 allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all the information needed to select and use a particular component, including functional description, API documentation, example codes, and AC/DC specifications.

Application notes: This includes the getting started application note and the hardware design guidelines.

Technical reference manual: The technical reference manual (TRM) contains all the technical detail you need to use a EZ-PD™ PMG1 device, including a complete description of all EZ-PD™ PMG1 registers. The TRM is available in the Documentation section at **EZ-PD™ PMG1 MCU** webpage.

1.2 Online

In addition to print documentation, the **EZ-PD™ PMG1 MCU forums** connect you with fellow users and experts in PMG1 from around the world, 24 hours a day, 7 days a week.

1.3 Tools

With industry standard cores, programming, and debugging interfaces, the EZ-PD™ PMG1 family is part of a development tool ecosystem.

Visit us at **ModusToolbox™ software** for the latest information on the revolutionary, easy to use Eclipse IDE for ModusToolbox™, supported third party compilers, programmers, debuggers, and development kits.

1.4 Eclipse IDE for ModusToolbox™

ModusToolbox™ is an Eclipse-based development environment on Windows, macOS, and Linux platforms that includes the Eclipse IDE for ModusToolbox™. The Eclipse IDE for ModusToolbox™ brings together several device resources, middleware, and firmware to build an application. Using ModusToolbox™ software, you can enable and configure device resources and middleware libraries, write C/C++/assembly source code, and program and debug the device.

For additional details on using the ModusToolbox™ software, refer to **AN232553 - Getting started with EZ-PD™ PMG1 MCU on ModusToolbox™ software** and the documentation and help integrated into ModusToolbox™ software. As **Figure 2** shows, with the Eclipse IDE for ModusToolbox™, you can:

1. Create a new application based on a list of template applications, filtered by kit or device, or browse the collection of code examples online.
2. Configure device resources in Device Configurator to build your hardware system design in the workspace.
3. Add software components or middleware.
4. Develop your application firmware.

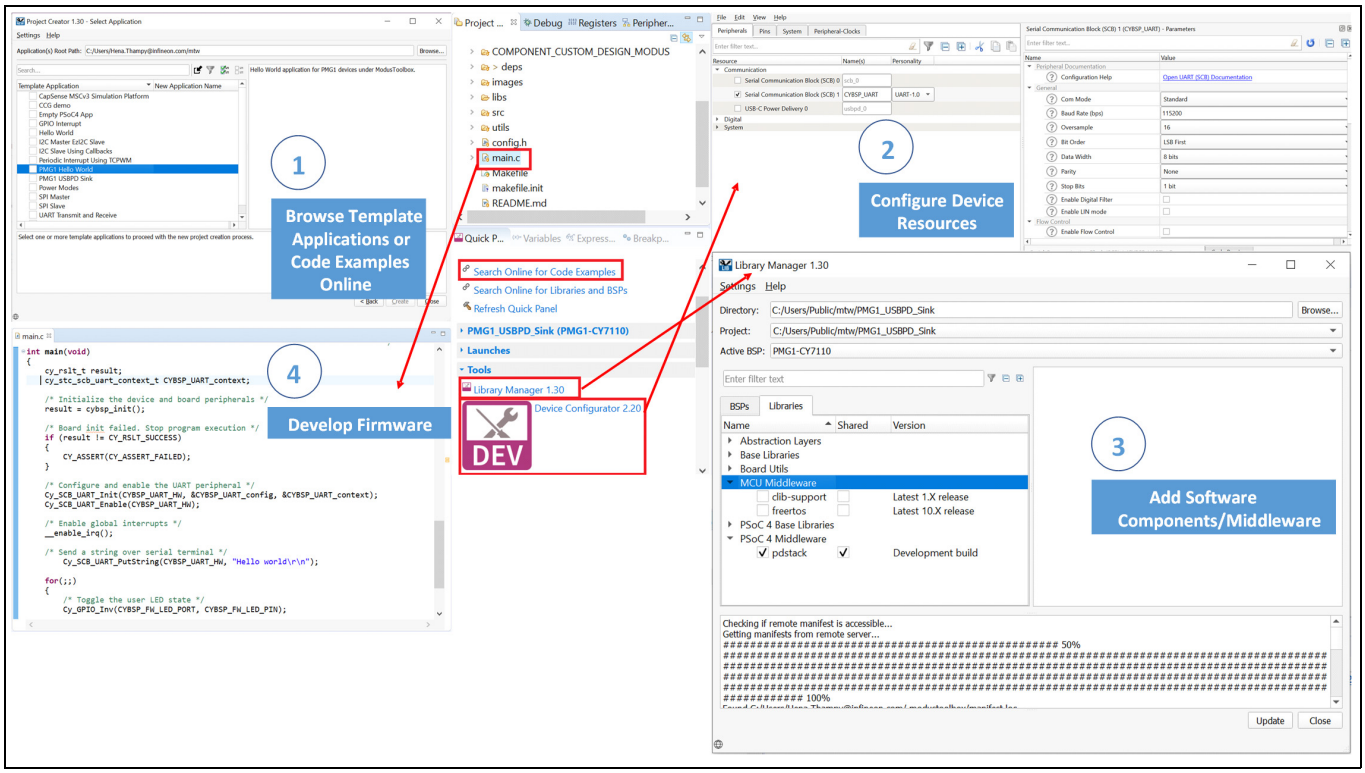

Figure 2 Eclipse IDE for ModusToolbox™ and middleware

2 Functional overview

2.1 CPU and memory subsystem

2.1.1 CPU

The Cortex®-M0 CPU in EZ-PD™ PMG1-S2 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. The Infineon implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex®-M0 CPU provides a nonmaskable interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for EZ-PD™ PMG1-S2 has four break-point (address) comparators and two watchpoint (data) comparators.

2.1.2 Flash

The EZ-PD™ PMG1-S2 device has a flash module with two banks of 64 KB flash, a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and with 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

2.1.3 SROM

A supervisory ROM that contains boot and configuration routines is provided.

2.2 Crypto block

EZ-PD™ PMG1-S2 integrates a crypto block for hardware assisted authentication of firmware images. It also supports field upgradeability of firmware in a trusted ecosystem. The EZ-PD™ PMG1-S2 crypto block provides cryptography functionality. It includes hardware acceleration blocks for advanced encryption standard (AES) block cipher, secure hash algorithm (SHA-1 and SHA-2), cyclic redundancy check (CRC) and pseudo random number generation.

2.3 Integrated billboard device

EZ-PD™ PMG1-S2 integrates a complete full speed USB 2.0 device controller capable of functioning as a Billboard class device. The USB 2.0 device controller can also support other device classes.

2.4 USB PD subsystem (USB PD SS)

The USB PD subsystem contains all of the blocks related to USB Type-C and Power Delivery. The subsystem consists of the following:

- Biphase marked coding (BMC) PHY: USB PD Transceiver with fast role swap (FRS) transmit and detect
- VCONN power FETs for the CC lines
- Analog crossbar to switch between the SBU1/SBU2 and AUX_P/AUX_N pins
- Programmable pull-up and pull-down termination on the AUX_P/AUX_N pins
- Hot plug detect (HPD) processor
- VBUS_C regulator (20V LDO)
- Power switch between VSYS supply and VBUS_C regulator output
- VBUS_C overvoltage (OV) and undervoltage (UV) detectors
- Current sense amplifier (CSA) for overcurrent detection

- Gate drivers for VBUS_P and VBUS_C external Power FETs
- VBUS_C discharge switch
- Charger detection/Emulation for USB BC1.2 and other proprietary protocols
- Two instances of 8-bit SAR ADCs
- 8-kV IEC ESD Protection on the following pins: VBUS_C, CC1, CC2, SBU1, SBU2, USBDP, USBDM

The EZ-PD™ PMG1-S2 USB PD subsystem interfaces to the pins of a USB Type-C connector. It includes a USB Type-C baseband transceiver and physical-layer logic. This transceiver performs the BMC and the 4b/5b encoding and decoding functions as well as integrating the 1.2-V analog front end (AFE). This subsystem integrates the required terminations to identify the role of the EZ-PD™ PMG1-S2 device, including R_P and R_D for UFP/DFP roles. It also integrates power FETs for supplying VCONN power to the CC1/CC2 pins from the VCONN_Source pin. The analog crossbar enables connecting either of the SBU1/SBU2 pins to either of the AUX_P/AUX_N pins to support DisplayPort sideband signaling. The integrated HPD processor can be used to control or monitor the HPD signal of a DisplayPort source or sink.

The overvoltage/undervoltage (OV/UV) block monitors the VBUS_C supply for programmable overvoltage and undervoltage conditions. The CSA amplifies the voltage across an external sense resistor, which is proportional to the current being drawn from the external DC-DC VBUS supply converter. The CSA output can either be measured with an ADC or configured to detect an overcurrent condition. The VBUS_P and VBUS_C gate drivers control the gates of external power FETs for the VBUS_C and VBUS_P supplies. The gate drivers can be configured to support both P and N type external power FETs. The gate drivers are configured by default for nFET devices. In applications using pFETs, the gate drivers must be appropriately configured. The OV/UV and CSA blocks can generate interrupts to automatically turn off the power FETs for the programmed overvoltage and overcurrent conditions. The VBUS_C discharge switch allows for discharging the VBUS_C line through an external resistor.

The USB PD subsystem also contains two 8-bit 125 ksps successive approximation register (SAR) ADCs for analog to digital conversions. The voltage reference for the ADCs is generated from the VDDD supply. Each ADC includes an 8-bit DAC and a comparator. The DAC output forms the positive input of the comparator. The negative input of the comparator is from a 4-input multiplexer. The four inputs of the multiplexer are a pair of global analog multiplex buses, an internal bandgap voltage and an internal voltage proportional to the absolute temperature. Each GPIO pin can be connected to the global analog multiplex buses through a switch, which allows either ADC to sample the pin voltage. When sensing the GPIO pin voltage with an ADC, the pin voltage must not exceed the VDDIO supply value.

2.5 Full-speed USB subsystem

The FSUSB subsystem contains a full-speed USB device controller as described in the **Integrated billboard device** section.

2.6 Peripherals

2.6.1 Serial communication blocks (SCB)

EZ-PD™ PMG1-S2 has four SCBs, which can be configured to implement an I^2C, SPI, or UART interface. The hardware I^2C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as master or slave.

In the I^2C mode, the SCB blocks are capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I^2C that creates a mailbox address range in the memory of EZ-PD™ PMG1-S2 and effectively reduce I^2C communication to reading from and writing to an array in memory. In addition, the blocks support 128-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripherals are compatible with the I^2C Standard-mode, Fast Mode, and Fast Mode Plus devices as defined in the NXP I^2C-bus specification and user manual (**UM10204**).

The I^2C bus I/Os are implemented with GPIO in open-drain modes.

The I^2C port on SCB 1-3 blocks of EZ-PD™ PMG1-S2 are not completely compliant with the I^2C specification in the following aspects:

- The GPIO cells for SCB 1's I^2C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast Mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast Mode and Fast Mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

2.6.2 Timer/counter/PWM block (TCPWM)

EZ-PD™ PMG1-S2 has four TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality.

2.7 GPIO

EZ-PD™ PMG1-S2 has up to 20 GPIOs (these GPIOs can be configured for GPIOs, SCB, SBU, and Aux signals) and SWD pins, which can also be used as GPIOs. The I^2C pins from SCB 0 are overvoltage-tolerant.

The GPIO block implements the following:

- Seven drive strength modes:
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

3 Power systems overview

Figure 3 shows an overview of the EZ-PD™ PMG1-S2 power system requirement. EZ-PD™ PMG1-S2 shall be able to operate from two possible external supply sources VBUS (4.0 V–21.5 V) or VSYS (2.7 V–5.5 V). The VBUS supply is regulated inside the chip with a low-dropout regulator (LDO) down to 3.3-V level. The chip's internal VDDD rail is intelligently switched between the output of the VBUS regulator and unregulated VSYS. The switched supply, VDDD is either used directly inside some analog blocks or further regulated down to VCCD which powers majority of the core using regulators. Besides Reset mode, EZ-PD™ PMG1-S2 has three different power modes: Active, Sleep and Deep Sleep, transitions between which are managed by the Power System. A separate power domain VDDIO is provided for the GPIOs. The VDDD and VCCD pins, both the output of regulators are brought out for connecting a 1-µF capacitor for the regulator stability only. These pins are not supported as power supplies. When EZ-PD™ PMG1-S2 is powered from VSYS that is greater than 3.3 V, the dedicated USB regulator allows USB operation.

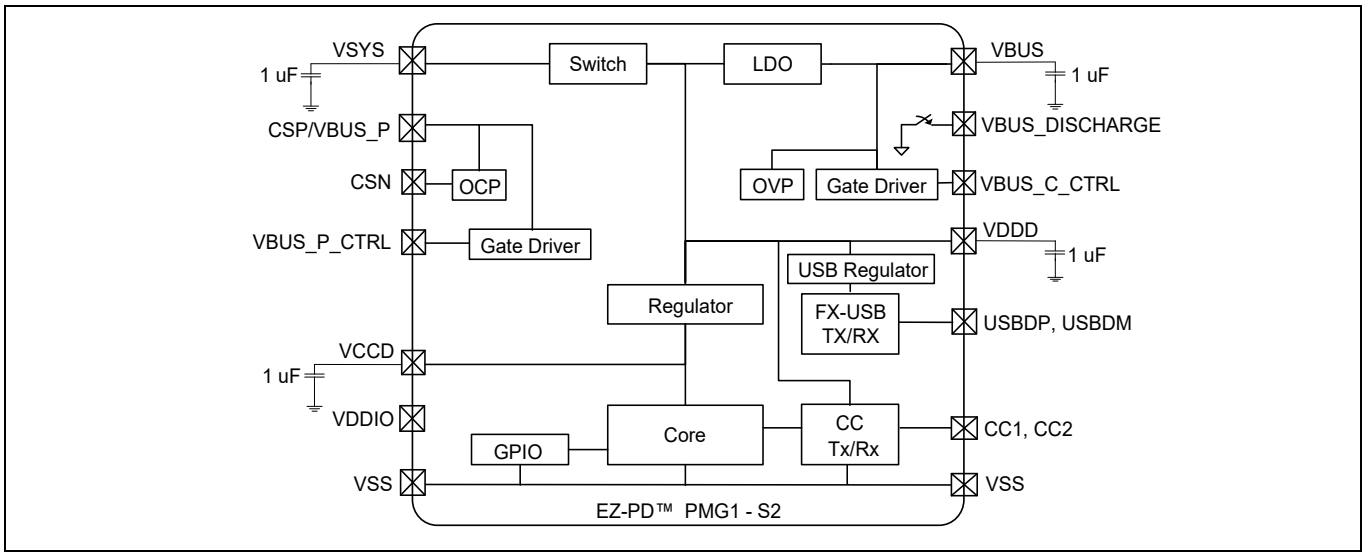

Figure 3 EZ-PD™ PMG1-S2 power system block diagram

Table 2 EZ-PD™ PMG1-S2 power modes

Mode	Description
RESET	Power is valid and XRES is not asserted. An internal reset source is asserted or SleepController is sequencing the system out of reset.
ACTIVE	Power is valid and CPU is executing instructions.
SLEEP	Power is valid and CPU is not executing instructions. All logic that is not operating is clock gated to save power.
DEEP SLEEP	Main regulator and most hard-IP are shut off. Deep Sleep regulator powers logic, but only low-frequency clock is available.

4 Pinouts

Table 3 EZ-PD™ PMG1-S2 pin description for CYPM1211-40LQXI

Group	40-pin QFN	42-ball CSP	Pin name	Description
GPIOs and serial interface	7	F6	P1.0/UART_2_TX/SPI_2_MISO	GPIO/UART_2_TX/SPI_2_MISO
	8	D5	P1.1/UART_2_RX/SPI_2_SEL	GPIO/UART_2_RX/SPI_2_SEL
	9	E5	P1.2/UART_0_RX/ UART_3_CTS/SPI_3_MOSI/ I2C_3_SCL	GPIO/UART_0_RX/UART_3_CTS/SPI_3_MOSI/I2C_3_SCL
	10	G6	P1.3/UART_0_TX/ UART_3_RTS/SPI_3_CLK/ I2C_3_SDA	GPIO/UART_0_TX/UART_3_RTS/SPI_3_CLK/I2C_3_SDA
	11	E4	P1.6/AUX_P/UART_1_TX/ SPI_1_MISO	DisplayPort AUX_P signal/GPIO/UART_1_TX/SPI_1_MISO
	12	F5	P1.4/SBU1/UART_3_TX/ SPI_3_MISO	USB Type-C SBU1 signal/GPIO/UART_3_TX/SPI_3_MISO
	13	G5	P1.5/SBU2/UART_3_RX/ SPI_3_SEL	USB Type-C SBU2 signal/GPIO/UART_3_RX/SPI_3_SEL
	14	G4	P1.7/AUX_N/UART_1_RX/ SPI_1_SEL	DisplayPort AUX_N signal/GPIO/UART_1_RX/SPI_1_SEL
	15	F4	P2.0/SWD_IO/UART_1_CTS/ SPI_1_CLK/I2C_1_SCL	GPIO / SWD_IO/UART_1_CTS/SPI_1_CLK/ I2C_1_SCL
	16	G3	P2.1/SWD_CLK/UART_1_RTS/ SPI_1_MOSI/I2C_1_SDA	GPIO/SWD_CLK/ UART_1_RTS/SPI_1_MOSI/ I2C_1_SDA
	23	E2	P2.4	GPIO
	24	D3	P2.5/UART_0_TX/SPI_0_MOSI	GPIO/UART_0_TX/SPI_0_MOSI
	25	D2	P2.6/UART_0_RX/SPI_0_CLK	GPIO/UART_0_RX/SPI_0_CLK
	27	C3	P0.0/GPIO_OVT/ UART_0_CTS/ SPI_0_SEL/I2C_0_SDA	P0.0/GPIO_OVT/UART_0_CTS/SPI_0_SEL/I2C_0_SDA/TCPWM_line_0
	28	C2	P0.1/GPIO_OVT/ UART_0_RTS/SPI_0_MISO/ I2C_0_SCL	P0.1/GPIO_OVT/UART_0_RTS/SPI_0_MISO/ I2C_0_SCL/TCPWM_line_1
	34	A2	P3.2	GPIO/TCPWM_line_0
	35	B2	P3.3	GPIO/TCPWM_line_1
	36	B3	P3.4/ UART_2_CTS/SPI_2_MOSI/ I2C_2_SDA	GPIO/UART_2_CTS/SPI_2_MOSI/I2C_2_SDA/TCPWM_line_2
	37	A3	P3.5/ UART_2_RTS/SPI_2_CLK/ I2C_2_SCL	GPIO/UART_2_RTS/SPI_2_CLK/I2C_2_SCL/ TCPWM_line_3
	38	B4	P3.6	GPIO
USB FS	21	F1	USBDP	USB 2.0 DP
	22	E1	USBDM	USB 2.0 DM
USB Type-C	3	B6, C5	CC2	USB PD connector detect/Configuration Channel 2
	5	C6, D6	CC1	USB PD connector detect/Configuration Channel 1

Table 3 EZ-PD™ PMG1-S2 pin description for CYPM1211-40LQXI *(continued)*

Group	40-pin QFN	42-ball CSP	Pin name	Description
VBUS	1	A5	VBUS_P_CTRL1	VBUS Gate Driver Control 1 for Producer Switch
	2	A6	VBUS_P_CTRL0	VBUS Gate Driver Control 0 for Producer Switch
	29	C1	VBUS_C_CTRL1	VBUS Gate Driver Control 1 for Consumer Switch
	30	C4	VBUS_C_CTRL0	VBUS Gate Driver Control 0 for Consumer Switch
	32	A1	VBUS_DISCHARGE	VBUS Discharge Control output
VBUS OCP/SCP/ RCP	39	A4	CSN	Current Sense Negative Input
	40	B5	CSP/VBUS_P	VBUS producer input. Connect this pin to a higher potential compared to CSN pin.
Reset	26	D1	XRES	External Reset Input. Internally pulled-up to VDDIO.
Power	4	D4	VCONN_Source	Input Supply Voltage for VCONN FETs VCON_Source = 5.0 V–5.5 V to supply VCONN > 4.75 V @ 1.5W VCONN_Source = 3.5 V – 5.5 V to supply VCONN > 3.00 V @ 1W
	17	G2	VDDD	VDDD supply Input/Output (2.7 V–5.5 V)
	18	F3	VDDIO	1.71 V–5.5 V supply for I/Os. This supply also powers the global analog multiplex buses.
	19	F2	VCCD	1.8-V regulator output for filter capacitor
	20	G1	VSYS	System power supply (2.7 V–5.5 V)
	31	B1	VBUS	VBUS Input
GND	33	E3	VSS	Ground Supply (GND)
	EPAD			
NC	6	E6	NC	Not connected

Table 4 SCBs and their functionality

Port	40-pin QFN	42-ball CSP	SCB function		
Pin	Pin #	Pin #	UART	SPI	I2C
P0.0	27	C3	UART_0_CTS	SPI_0_SEL	I2C_0_SDA
P0.1	28	C2	UART_0_RTS	SPI_0_MISO	I2C_0_SCL
P1.0	7	F6	UART_2_TX	SPI_2_MISO	-
P1.1	8	D5	UART_2_RX	SPI_2_SEL	-
P1.2	9	E5	UART_0_RX UART_3_CTS	SPI_3_MOSI	I2C_3_SCL
P1.3	10	G6	UART_0_TX UART_3_RTS	SPI_3_CLK	I2C_3_SDA
P1.4	12	F5	UART_3_TX	SPI_3_MISO	-
P1.5	13	G5	UART_3_RX	SPI_3_SEL	-
P1.6	11	E4	UART_1_TX	SPI_1_MISO	-
P1.7	14	G4	UART_1_RX	SPI_1_SEL	-
P2.0	15	F4	UART_1_CTS	SPI_1_CLK	I2C_1_SCL
P2.1	16	G3	UART_1_RTS	SPI_1_MOSI	I2C_1_SDA
P2.5	24	D3	UART_0_TX	SPI_0_MOSI	-
P2.6	25	D2	UART_0_RX	SPI_0_CLK	-
P3.4	36	B3	UART_2_CTS	SPI_2_MOSI	I2C_2_SDA
P3.5	37	A3	UART_2_RTS	SPI_2_CLK	I2C_2_SCL

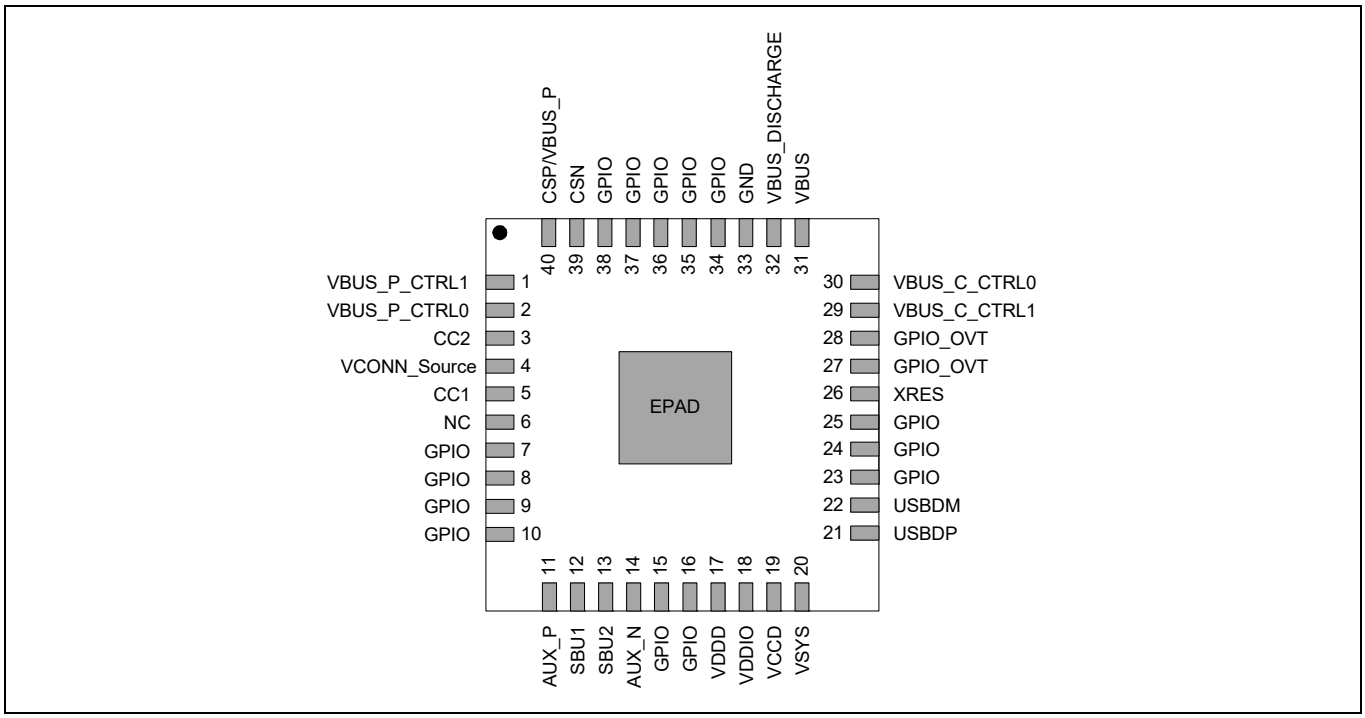

Figure 4 Pinout of 40-QFN package (top view)

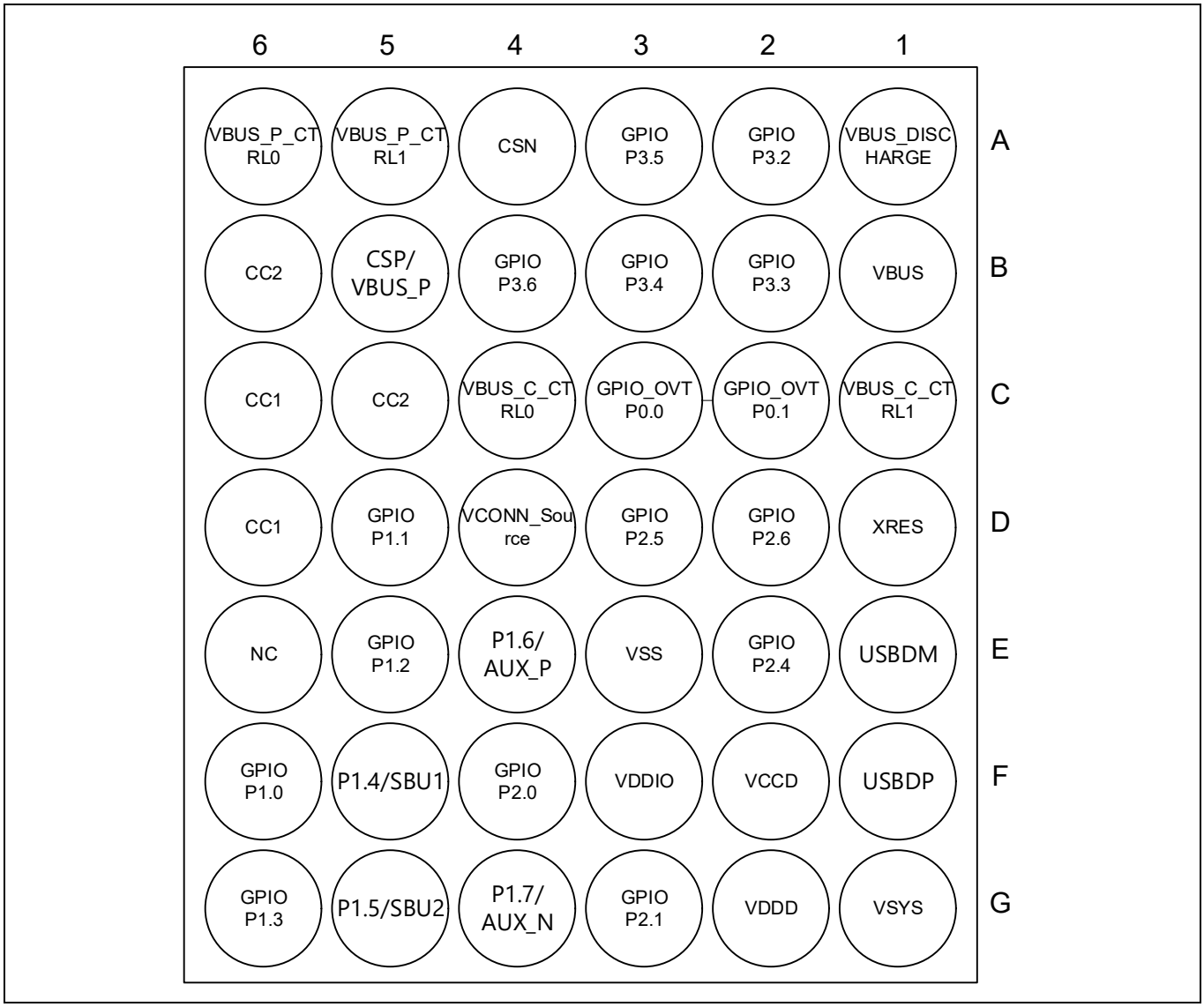

Figure 5 Pinout of 42-WLCSP bottom (balls up) view

5 Application diagrams

Figure 6 shows a Power Sink application using EZ-PD™ PMG1-S2. In this application, the Type-C receptacle is used for consuming power. The EZ-PD™ PMG1-S2 device negotiates power contracts with the source device connected to the Type-C receptacle. The device also controls and drives the consumer path FETs and monitors overvoltage/undervoltage conditions on the Type-C VBUS line.

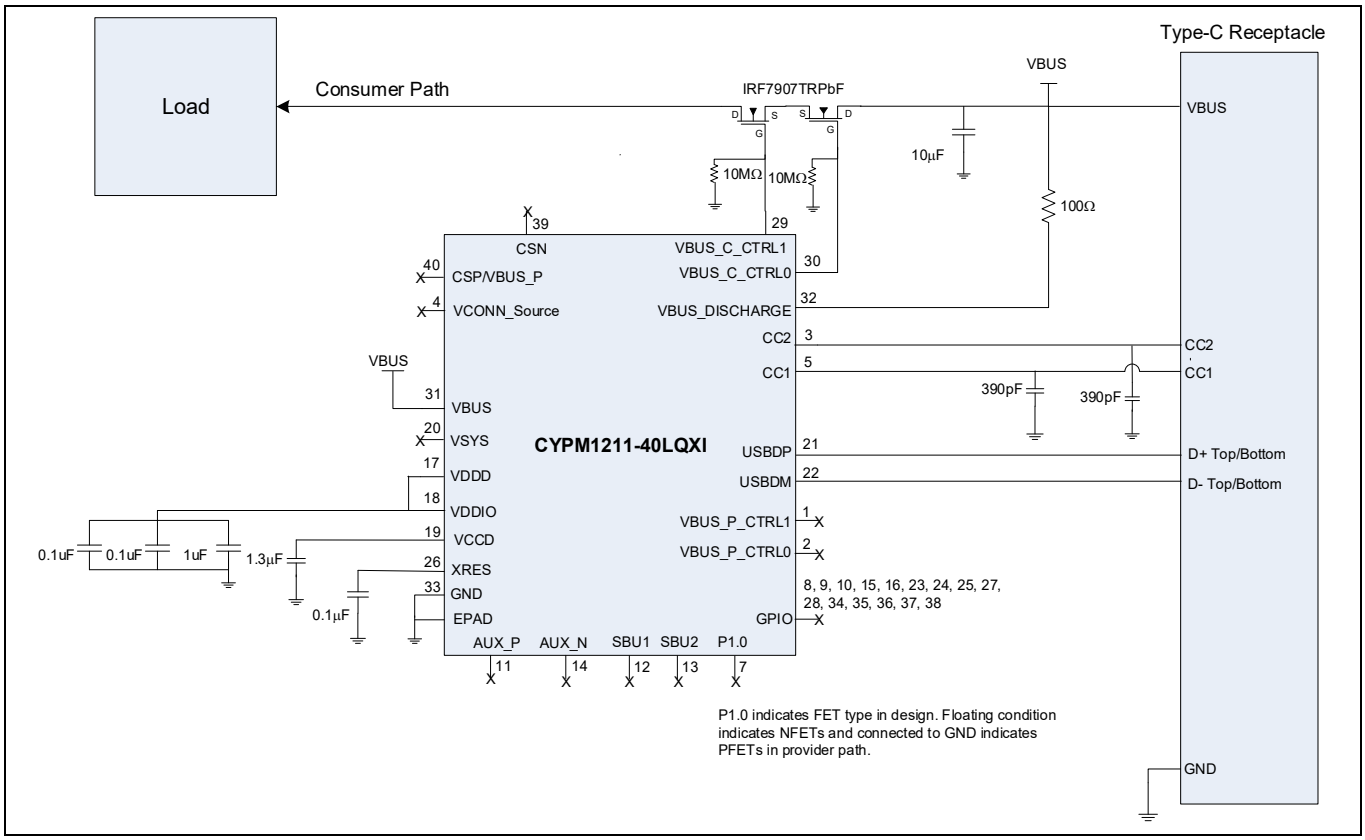

Figure 6 EZ-PD™ PMG1-S2 based sink application diagram

Figure 7 illustrates the application diagram of a power source using EZ-PD™ PMG1-S2 device. In this application, EZ-PD™ PMG1-S2 is used as DFP (power provider) only. The maximum power profile that can be supported in power source applications is up to 20 V, 100 W. EZ-PD™ PMG1-S2 can drive both types of FETs and the state of GPIO P1.0 (floating or grounded) indicates the type of FET (N-MOS or P-MOS FET) being used in the power provider path. To ensure quick discharge of VBUS when the power adapter cable is detached, a discharge path is provided with a resistor connected to the VBUS_DISCHARGE pin of the EZ-PD™ PMG1-S2 device.

The VBUS voltage on the Type-C port is monitored using internal circuits to detect under-voltage and overvoltage conditions. VBUS overcurrent can also be detected by sensing the current through the 10-mΩ sense resistor connected between "CSN" and "CSP/VBUS_P" pins. Any of these faults on the VBUS line can further be used to turn off the VBUS provider path using the provider path FETs which are controlled by high-voltage gate driver outputs (VBUS_P_CTRL0 and VBUS_P_CTRL1 pins).

The EZ-PD™ PMG1-S2 device is also capable of supporting proprietary charging protocols over the D+ and D- lines of the Type-C receptacle. By providing a 5-V source at the VCONN_Source pin of the EZ-PD™ PMG1-S2 device, the device also becomes capable of delivering VCONN supply over either the CC1 or CC2 pins of the Type-C connector.

Application diagrams

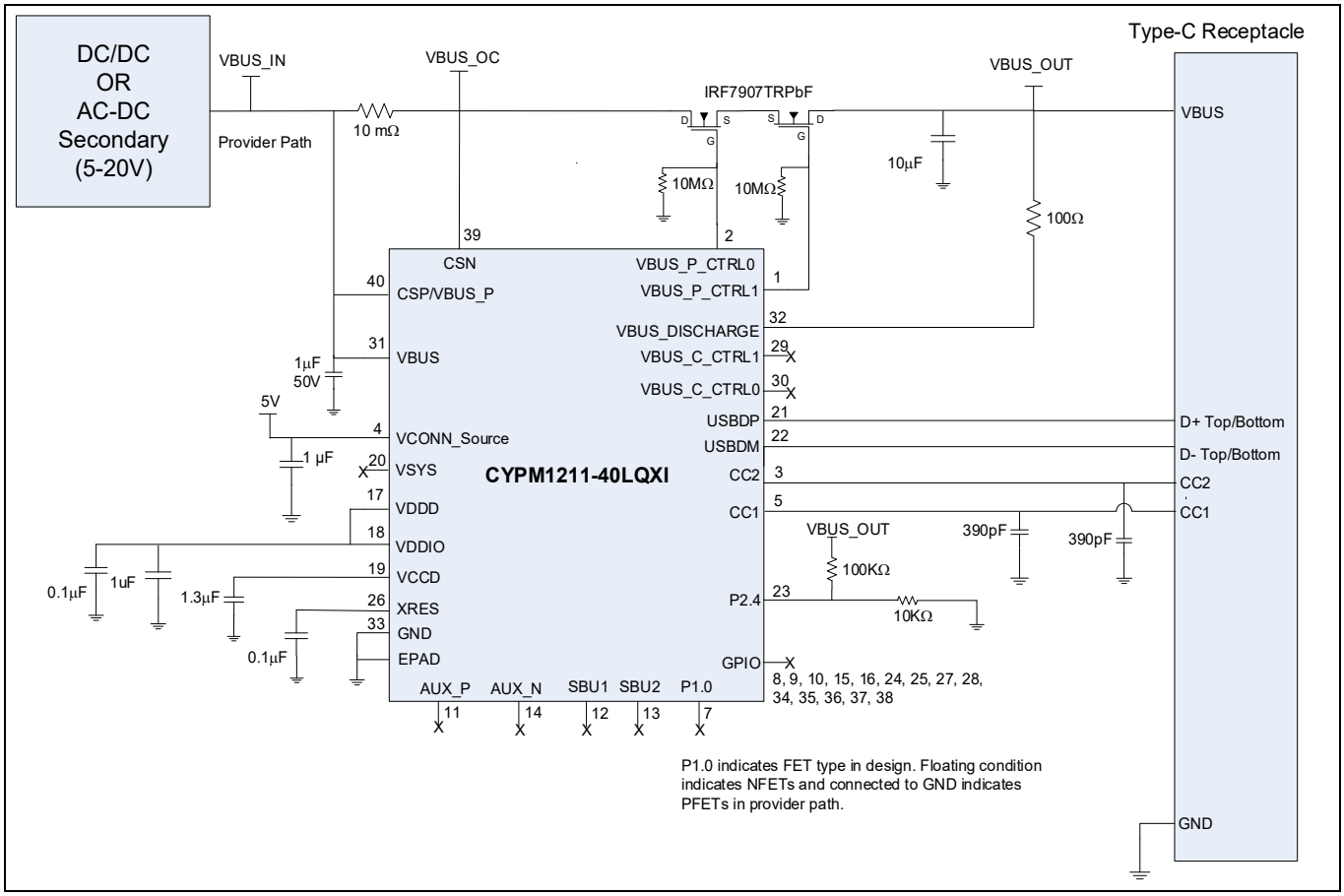

Figure 7 EZ-PD™ PMG1-S2 based source application diagram

Figure 8 illustrates a DRP application diagram using EZ-PD™ PMG1-S2 device. The Type-C port can be used as a power provider or a power consumer.

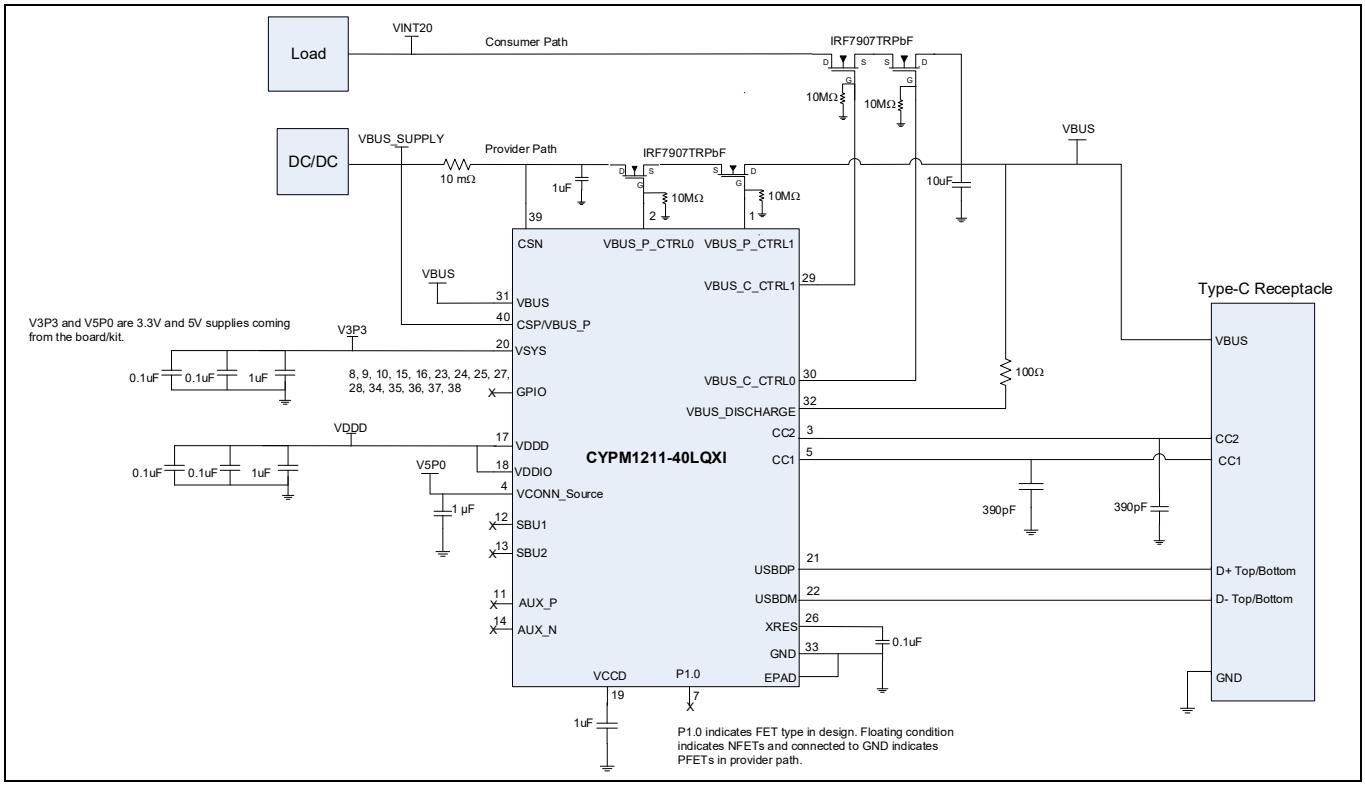

Figure 8 EZ-PD™ PMG1-S2 based DRP application diagram

6 Electrical specifications

6.1 Absolute maximum ratings

Table 5 Absolute maximum ratings[1]

Parameter	Description	Min	Typ	Max	Units	Details/conditions
V_{SYS_MAX}	Digital supply relative to V_{SS}	–	–	6	V[2]	Absolute max
$V_{CONN\_SOURCE\_MAX}$	Max supply voltage relative to V_{SS}	–	–	6	V	
$V_{BUS\_MAX\_ON}$	Max supply voltage relative to V_{SS}, V_{BUS} regulator enabled	–	–	26	V	
$V_{BUS\_MAX\_OFF}$	Max supply voltage relative to V_{SS}, V_{BUS} regulator enabled 100% of the time	–	–	24.5	V	
	Max supply voltage relative to V_{SS}, V_{BUS} regulator enabled 25% of the time	–	–	26	V	
V_{DDIO_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	
V_{GPIO_ABS}	GPIO voltage	–0.5[3]	–	V_{DDIO} + 0.5	V	
$V_{GPIO\_OVT\_ABS}$	OVT GPIO voltage	–0.5	–	6	V	
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
V_{CC_ABS}	Max voltage on CC1 and CC2 pins	–	–	6	V	
$I_{GPIO\_INJECTION}$	GPIO injection current, Max for V_{IH} > VDDD, and Min for V_{IL} < V_{SS}	–0.5	–	0.5	mA	Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model (ESD-HBM)	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model (ESD-CDM)	500	–	–	V	–
LU	Pin current for latch-up	–100	–	100	mA	Tested at 125°C
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000	–	–	V	Contact discharge on CC1, CC2, VBUS, USBDP, USBDM, SBU1 and SBU2 pins
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2	15000	–	–	V	Air discharge for CC1, CC2, VBUS, USBDP, USBDM, SBU1 and SBU2 pins

Notes

1. Usage above the absolute maximum conditions listed in **Table 5** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.
2. All voltages are relative to Ground unless otherwise specified.
3. In a system, if the negative spike exceeds the minimum voltage specified here, it is recommended to add Schottky diode to clamp the negative spike.

6.2 Pin based absolute maximum ratings

Table 6 Pin based absolute maximum ratings

S. No.	Pin (40 QFN)	Pin (42 CSP)	Name	Absolute minimum (V)	Absolute maximum (V)	Remarks
1	7	F6	P1.0	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
2	8	D5	P1.1	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
3	9	E5	P1.2	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
4	10	G6	P1.3	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
5	11	E4	P1.6	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
6	12	F5	P1.4	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
7	13	G5	P1.5	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
8	14	G4	P1.7	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
9	15	F4	P2.0	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
10	16	G3	P2.1	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
11	23	E2	P2.4	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
12	24	D3	P2.5	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
13	25	D2	P2.6	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
14	27	C3	P0.0	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
15	28	C2	P0.1	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
16	34	A2	P3.2	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
17	35	B2	P3.3	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
18	36	B3	P3.4	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
19	37	A3	P3.5	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
20	38	B4	P3.6	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
21	21	F1	USBDP	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
22	22	E1	USBDM	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5
23	3	B6, C5	CC2	–	6	–
24	5	C6, D6	CC1	–	6	–
25	1	A5	VBUS_P_CTRL1	-0.5	26	–
26	2	A6	VBUS_P_CTRL0	-0.5	26	–
27	29	C1	VBUS_C_CTRL1	-0.5	26	–
28	30	C4	VBUS_C_CTRL0	-0.5	26	–
29	32	A1	VBUS_-DISCHARGE	–	26	–
30	39	A4	CSN	–	26	–
31	40	B5	CSP/VBUS_P	–	26	–
32	26	D1	XRES	-0.5	6	Maximum voltage cannot exceed VDDIO + 0.5

Table 6 Pin based absolute maximum ratings *(continued)*

S. No.	Pin (40 QFN)	Pin (42 CSP)	Name	Absolute minimum (V)	Absolute maximum (V)	Remarks
33	4	D4	VCONN_Source	–	6	–
34	17	G2	VDDD	–	6	This is an output only pin
35	18	F3	VDDIO	–	VDDD	–
36	19	F2	VCCD	–	1.95	This is an output only pin
37	20	G1	VSYS	–	6	–
38	31	B1	VBUS	–	26	–
39	33	E3	VSS	–	–	–
40	EPAD		VSS	–	–	–
41	6	E6	NC	–	–	–

6.3 Device-level specifications

All specifications are valid for –40°C ≤ T_A ≤ 105°C and T_J ≤ 120°C, except where noted.

Table 7 DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.PWR#1	VSYS	–	2.7	–	5.5	V	UFP Mode.
SID.PWR#1_A	VSYS	–	3	–	5.5	V	DFP/DRP or Gate Driver Modes
SID.PWR#23	VCONN	Power supply input voltage	2.7	–	5.5	V	–
SID.PWR#13	VDDIO	IO supply voltage	1.71	–	5.5[4]	V	2.7 V < VDDD < 5.5 V
SID.PWR24	VCCD	Output voltage for core logic	–	1.8	–	V	–
SID.PWR#4	IDD	Supply current	–	25	–	mA	From VSYS or VBUS VBUS = 5 V, T_A = 25°C / VSYS = 5 V, TA = 25°C FS USB, CC IO in Tx or Rx, no I/O sourcing current, 2 SCBs at 1 Mbps, CPU at 24 MHz.
SID.PWR#1_B	VSYS	Power supply for USB operation	4.5	–	5.5	V	USB configured, USB Regulator enabled
SID.PWR#1_C	VSYS	Power supply for USB operation	3.15	–	3.45	V	USB configured, USB Regulator disabled
SID.PWR#1_D	VSYS	Power supply for charger detect/emulation operation	3.15	–	5.5	V	–40°C to +85°C T_A
SID.PWR#27	VBUS	Power supply input voltage	3.5	–	21.5	V	FS USB disabled. Total current consumption from VBUS <15 mA.
SID.PwR#28	VBUS	Power supply input voltage for USB operation	4.5	–	21.5	V	FS USB configured, USB Regulator disabled
SID.PWR#30	VBUS_P	Power supply input voltage	4.00	–	21.5	V	–
SID.PWR#15	C_{efc}	External regulator voltage bypass for VCCD	1	1.3	1.6	µF	X5R ceramic or better
SID.PWR#16	C_{exc}	Power supply decoupling capacitor for VSYS	0.8	1	–	µF	X5R ceramic or better
Sleep Mode. VSYS = 2.7 V to 5.5 V. Typical values measured at V_{DD} = 3.3 V and TA = 25°C.							
SID25A	I_{DD20A}	CC, I^2C, WDT wakeup on. IMO at 48 MHz.	–	3.5	–	mA	VSYS = 3.3 V, T_A = 25°C, All blocks except CPU are on, CC IO on, USB in Suspend Mode, no I/O sourcing current
Deep Sleep Mode							

Note

4. If VDDIO > VDDD, GPIO P2.4 cannot be used. It must be left unconnected. See **Table 3** for pin numbers.

Table 7 DC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID_DS	I_{DD_DS}	VSYS = 3.0 to 3.6 V. CC Attach, I^2C, WDT Wakeup on.	–	30	–	µA	Power Source = VSYS, DFP Mode, Type-C Not Attached. CC Attach, I^2C and WDT enabled for Wakeup.
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted. This does not include current drawn due to the XRES internal pull-up resistor.	–	30	–	µA	Power Source = VSYS = 3.3 V, Type-C device not attached, T_A = 25°C

Table 8 AC specifications (guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.CLK#4	F_{CPU}	CPU input frequency	DC	–	48	MHz	All VDDD
SID.PWR#20	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	–
SID.PWR#21	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	35	µs	–
SID.XRES#5	T_{XRES}	External reset pulse width	5	–	–	µs	All VDDIO
SYS.FES#1	$T_{\_PWR\_RDY}$	Power-up to “Ready to accept I^2C/CC command”	–	5	25	ms	–

6.3.1 I/O

Table 9 I/O DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID.GIO#37	V_{IH_CMOS}	Input voltage HIGH threshold	0.7 × VDDIO	–	–	V	CMOS input
SID.GIO#38	V_{IL_CMOS}	Input voltage LOW threshold	–	–	0.3 × VDDIO	V	CMOS input
SID.GIO#39	$V_{IH\_VDDIO2.7-}$	LVTTL input, VDDIO < 2.7 V	0.7 × VDDIO	–	–	V	–
SID.GIO#40	$V_{IL\_VDDIO2.7-}$	LVTTL input, VDDIO < 2.7 V	–	–	0.3 × VDDIO	V	–
SID.GIO#41	$V_{IH\_VDDIO2.7+}$	LVTTL input, VDDIO ≥ 2.7 V	2.0	–	–	V	–
SID.GIO#42	$V_{IL\_VDDIO2.7+}$	LVTTL input, VDDIO ≥ 2.7 V	–	–	0.8	V	–
SID.GIO#33	V_{OH_3V}	Output voltage HIGH level	VDDIO – 0.6	–	–	V	I_{OH} = 4 mA at 3 V VDDIO
SID.GIO#34	$V_{OH\_1.8V}$	Output voltage HIGH level	VDDIO – 0.5	–	–	V	I_{OH} = 1 mA at 1.8 V VDDIO
SID.GIO#35	$V_{OL\_1.8V}$	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 1.8 V VDDIO
SID.GIO#36	V_{OL_3V}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 3 V VDDIO for SBU and AUX pins
SID.GIO#5	R_{PU}	Pull-up resistor value	3.5	5.6	8.5	kΩ	+25°C T_A, all VDDIO
SID.GIO#6	R_{PD}	Pull-down resistor value	3.5	5.6	8.5	kΩ	+25°C T_A, all VDDIO
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25°C T_A, all VDDIO. Guaranteed by characterization.
SID.GIO#17	C_{PIN}	Max pin capacitance	–	3.0	7	pF	All VDDIO, all packages, all I/Os except SBU and AUX. Guaranteed by characterization.
SID.GIO#17A	C_{PIN_SBU}	Max pin capacitance	–	16	18	pF	All VDDIO, all packages, SBU pins only. Guaranteed by characterization.
SID.GIO#17B	C_{PIN_AUX}	Max pin capacitance	–	12	14	pF	All VDDIO, all packages, AUX pins only. Guaranteed by characterization.

Table 9 I/O DC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID.GIO#43	V_{HYSTTL}	Input hysteresis, LVTTL VDDIO > 2.7 V	15	40	–	mV	Guaranteed by characterization
SID.GIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × VDDIO	–	–	mV	VDDIO < 4.5 V. Guaranteed by characterization.
SID69	I_{DIODE}	Current through protection diode to VDDIO/Vss	–	–	100	µA	Guaranteed by characterization
SID.GIO#45	I_{TOT_GPIO}	Maximum total sink chip current	–	–	85	mA	Guaranteed by characterization
OVT							
SID.GIO#46	I_{IHS}	Input current when Pad > VDDIO for OVT inputs	–	–	10.00	µA	Per I^2C specification

Table 10 I/O AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID70	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	3.3 V VDDIO, C_{load} = 25 pF
SID71	T_{FALLF}	Fall time in Fast Strong mode	2	–	12	ns	3.3 V VDDIO, C_{load} = 25 pF

6.3.2 XRES

Table 11 XRES DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID.XRES#1	V_{IH_XRES}	Input voltage HIGH threshold on XRES pin	0.7 × VDDIO	–	–	V	CMOS input
SID.XRES#2	V_{IL_XRES}	Input voltage LOW threshold on XRES pin	–	–	0.3 × VDDIO	V	CMOS input
SID.XRES#3	C_{IN_XRES}	Input capacitance on XRES pin	–	–	7	pF	Guaranteed by characterization
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis on XRES pin	–	0.05 × VDDIO	–	mV	Guaranteed by characterization

6.4 Digital peripherals

The following specifications apply to the timer/counter/PWM peripherals in the timer mode.

6.4.1 Pulse width modulation (PWM) for GPIO pins

Table 12 PWM AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.TCPWM.3	$T_{CPWMFREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS. Maximum = 48 MHz.
SID.TCPWM.4	$T_{PWMENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events

Table 12 PWM AC specifications

(guaranteed by characterization) *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.TCPWM.5	T_{PWMEXT}	Output trigger pulse width	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	T_{CRES}	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between quadrature-phase inputs

6.4.2 I²C

Table 13 Fixed I²C DC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	60	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	185	µA	–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	390	µA	–
SID152	I_{I2C4}	I²C enabled in Deep Sleep mode	–	–	1.4	µA	–

Table 14 Fixed I²C AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

Table 15 Fixed UART DC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID160	I_{UART1}	Block current consumption at 100 Kb/s	–	–	125	µA	–
SID161	I_{UART2}	Block current consumption at 1000 Kb/s	–	–	312	µA	–

Table 16 Fixed UART AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

Table 17 Fixed SPI DC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID163	I_{SPI1}	Block current consumption at 1 Mb/s	–	–	360	µA	–
SID164	I_{SPI2}	Block current consumption at 4 Mb/s	–	–	560	µA	–
SID165	I_{SPI3}	Block current consumption at 8 Mb/s	–	–	600	µA	–

Table 18 Fixed SPI AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID166	F_{SPI}	SPI operating frequency (Master; 6X oversampling)	–	–	8	MHz	–

Table 19 Fixed SPI master mode AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID167	T_{DMO}	MOSI Valid after SClock driving edge	–	–	15	ns	–
SID168	T_{DSI}	MISO Valid before SClock capturing edge	20	–	–	ns	Full clock, late MISO sampling
SID169	T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to slave capturing edge

Table 20 Fixed SPI slave mode AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID170	T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns	–
SID171	T_{DSO}	MISO valid after Sclock driving edge	–	–	$42 + 3 \times T_{CPU}$	ns	$T_{CPU} = 1/F_{CPU}$
SID171A	T_{DSO_EXT}	MISO valid after Sclock driving edge in Ext Clk mode	–	–	48	ns	–
SID172	T_{HSO}	Previous MISO data hold time	0	–	–	ns	–
SID172A	$T_{SSELSCK}$	SSEL valid to first SCK Valid edge	100	–	–	ns	–

6.5 System resources

6.5.1 Power-on reset (POR) with brown out SWD interface

Table 21 Imprecise power-on reset (IPOR)

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID185	$V_{RISEIPOR}$	Power-on Reset (POR) rising trip voltage	0.80	–	1.50	V	–
SID186	$V_{FALLIPOR}$	POR falling trip voltage	0.70	–	1.4	V	–

Table 22 Precise power-on reset (POR)

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID190	$V_{FALLPPOR}$	Brown-out detect (BOD) trip voltage in active/sleep modes	1.48	–	1.62	V	–
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.1	–	1.5	V	–

Table 23 SWD interface specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.SWD#1	F_SWDCLK1	3.3 V ≤ VDDIO ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#2	F_SWDCLK2	1.8 V ≤ VDDIO ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#3	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID.SWD#4	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID.SWD#5	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.50 × T	ns	Guaranteed by characterization
SID.SWD#6	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

6.5.2 Internal main oscillator

Table 24 IMO DC specifications

(guaranteed by design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000	µA	–

Table 25 IMO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 24, 36, and 48 MHz (trimmed)	–	–	±2	%	$-25°C \le T_A \le 85°C$, all VDDD
SID226	$T_{STARTIMO}$	IMO start-up time	–	–	7	µs	Guaranteed by characterization
SID229	$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	Guaranteed by characterization
SID.CLK#1	F_{IMO}	IMO frequency	24	–	48	MHz	All VDDD

6.5.3 Internal low-speed oscillatorpower down

Table 26 ILO DC specifications

(guaranteed by design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID231	I_{ILO1}	I_{LO} operating current	–	0.3	1.05	µA	–
SID233	$I_{ILOLEAK}$	I_{LO} leakage current	–	2	15	nA	–

Table 27 ILO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID234	$T_{STARTILO1}$	I_{LO} start-up time	–	–	2	ms	Guaranteed by characterization
SID238	$T_{ILODUTY}$	I_{LO} duty cycle	40	50	60	%	Guaranteed by characterization
SID.CLK#5	F_{ILO}	I_{LO} frequency	20	40	80	kHz	–

Table 28 PD DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.PD.1	R_P_std	DFP CC termination for default USB Power	64	80	96	µA	–
SID.PD.2	R_P_1.5A	DFP CC termination for 1.5 A power	166	180	194.4	µA	–
SID.PD.3	R_P_3.0A	DFP CC termination for 3.0 A power	304	330	356.4	µA	–
SID.PD.4	R_D	UFP CC termination	4.59	5.1	5.61	kΩ	–
SID.PD.5	R_D_DB	UFP Dead Battery CC termination on CC1 and CC2, valid for 1.5 A and 3.0 A R_P termination values	4.08	5.1	6.12	kΩ	UFP Dead Battery CC termination on CC1 and CC2. For Default R_P termination, the voltage on CC1 and CC2 is guaranteed to be <1.32 V.
SID.PD.15	$V_{gndoffset}$	Ground offset tolerated by BMC receiver	–400	–	400	mV	Relative to the remote BMC transmitter. Guaranteed by characterization.

Table 29 CSA specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.CSA.1	Out_E_Trim_15_DS	Overall error at Av = 15 using deep sleep reference	–7.00	–	7.00	%	Guaranteed by characterization.
SID.CSA.2	Out_E_Trim_15_BG	Overall error at Av = 15 using bandgap reference	–4.50	–	4.50	%	Guaranteed by characterization.
SID.CSA.3	Out_E_Trim_100	Overall error at Av = 100 using either bandgap or deep sleep reference	–24.50	–	24.50	%	–

Table 30 UV/OV specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.UVOV.1	$V_{THUVOV1}$	Voltage threshold accuracy, $V_{BUS} \leq 16$ V	–6		6	%	Tested at VBUS = 3.75 V, 4.5 V, 5.25 V, 12 V, 16 V
SID.UVOV.2	$V_{THUVOV2}$	Voltage threshold accuracy, $V_{BUS} > 16$ V	–10		10	%	Tested at VBUS = 20 V

6.5.4 Gate driver specifications

Table 31 Gate driver DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
DC.NGDO.1	VGS1	Gate to source overdrive	5	–	16.5	V	1. Gate driver supply voltage ≥ 5 V, where gate driver supply voltage = VBUS _P for VBUS_P_CTRL_ outputs, and VBUS_C for VBUS_C_CTRL_ outputs. 2. Gate driver current = 0 3. Gate driver configuration = NFET 4. Gate driver pump clock divider = 1
DC.NGDO.2	VGS2	Gate to source overdrive	3.75	–	16.5	V	1. Gate driver supply voltage ≥ 3.75 V, where Gate driver supply voltage = VBUS _P for VBUS_P_CTRL_ outputs, and VBUS_C for VBUS_C_CTRL_ outputs. 2. Gate driver current = 0 3. Gate driver configuration = NFET 4. Gate driver pump clock divider = 1
DC.NGDO.6	R_{PD}	Resistance when “pull down” enabled	–	–	5	kΩ	–

Table 32 Gate driver AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
AC.NGDO.1	T_{ON}	Gate turn-on time to gate_driver_supply_voltage + 5 V for supply voltage ≥ 5 V and VBUS * 2 for supply voltage < 5 V	–	–	1	ms	1. Gate driver configuration = NFET 2. Load = The gate of a SI9936 MOSFET

6.5.5 SBU

Table 33 Analog crossbar switch specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID.SBU.1	Ron_sw	Switch ON resistance	–	–	10	Ω	Voltage input from 0 V to 3.6 V
SID.SBU.2	Rpu_aux_1	AUX_P/N pull-up resistance – 100k	80	–	120	kΩ	–
SID.SBU.3	Rpu_aux_2	AUX_P/N pull-up resistance – 1M	0.8	–	1.2	MΩ	–
SID.SBU.4	Rpd_aux_1	AUX_P/N pull-down resistance – 100k	80	–	120	kΩ	–
SID.SBU.5	Rpd_aux_2	AUX_P/N pull-down resistance – 1M	0.8	–	1.2	MΩ	–
SID.SBU.6	Rpd_aux_3	AUX_P/N pull-down resistance – 470k	329	–	611	kΩ	–
SID.SBU.7	Rpd_aux_4	AUX_P/N pull-down resistance – 4.7M	3.29	–	6.11	MΩ	–

6.5.6 Charger detect

Table 34 Charger detect specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID.CD.1	VDAT_REF	BC1.2 Data detect voltage threshold	250	–	400	mV	–
SID.CD.2	VDM_SRC	BC1.2 DM voltage source	500	–	700	mV	With current sink of 25 µA–175 µA
SID.CD.3	VDP_SRC	BC1.2 DP voltage source	500	–	700	mV	With current sink of 25 µA–175 µA
SID.CD.4	IDM_SINK	BC1.2 DM current sink	25	–	175	µA	–
SID.CD.5	IDP_SINK	BC1.2 DP current sink	25	–	175	µA	–
SID.CD.6	IDP_SRC	BC1.2 DP DCD current source	7	–	13	µA	–
SID.CD.7	RDP_UP	USB FS DP pull-up termination	0.9	–	1.575	kΩ	–
SID.CD.8	RDM_UP	USB FS DM pull-up termination	0.9	–	1.575	kΩ	–
SID.CD.9	RDP_DWN	USB FS DP pull-down termination	14.25	–	24.8	kΩ	–
SID.CD.10	RDM_DWN	USB FS DM pull-down termination	14.25	–	24.8	kΩ	–
SID.CD.11	RDAT_LKG	DP/DM data line leakage termination	300	–	500	kΩ	The charger detect function and data line leakage is enabled.
SID.CD.12	RDCP_DAT	BC1.2 DCP port resistance between DP and DM	–	–	40	Ω	–
SID.CD.13	VSETH	USB FS logic threshold	1.26	–	1.54	V	–

6.5.7 Analog to digital converter

Table 35 ADC DC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	–1.5	–	1.5	LSB	–
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5	LSB	–
SID.ADC.4	Gain Error	Gain error	–1	–	1	LSB	–

Table 36 ADC AC specifications

(guaranteed by design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.ADC.5	SLEW_Max	Rate of change of sampled voltage signal	–	–	3	V/ms	–

Table 37 VBUS_C regulator DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.20vreg.1	VBUSREG	VBUS regulator output voltage measured at VDDD for VBUS = 4.5 V to 21.5 V	3	–	3.6	V	VBUS = 4.5 V - 21.5 V range. VDDD voltage measured with no load and a load of 30 mA.
SID.20vreg.2	VBUSREG2	VBUS regulator output voltage measured at VDDD for VBUS = 3.5 V to 21.5 V	3	–	3.6	V	VBUS = 4.5 V - 21.5 V range. VDDD voltage measured with no load and a load of 15 mA.
SID.20vreg.6	VBUSLINREG	VBUS regulator line regulation for VBUS from 4.5 V to 21.5 V	–	–	0.5	%/V	VBUS supply varied from 4.5 V to 21.5 V and the change in the VDDD measured. Guaranteed by characterization.
SID.20vreg.8	VBUSLOADREG	VBUS regulator load regulation for VBUS from 4.5 V to 21.5 V	–	–	0.2	%/mA	Supply of 4.5 V - 21.5 V applied on VBUS and the load current swept from 0 to 30 mA. The change in VDDD is measured. Guaranteed by characterization.

Table 38 VBUS_C regulator AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
AC.20vreg.1	T_{START}	Regulator start-up time	–	–	120	µs	Apply VBUS and measure start time on VDDD pin.
AC.20vreg.2	T_{STOP}	Regulator power down time	–	–	1	µs	Time from assertion of an internal disable signal to for load current on VDDD to decrease from 30 mA to 10 µA.

Table 39 VSYS switch specification

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.vddsw.1	Res_sw	Resistance from VSYS supply input to the output supply VDDD	–	–	1.5	Ω	Measured with a load current of 5 mA - 10 mA on VDDD.

6.5.8 Memory

Table 40 Flash AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.MEM#3	FLASH_ERASE	Row erase time	–	–	15.5	ms	–
SID.MEM#4	FLASH_WRITE	Row (Block) write time (erase and program)	–	–	20	ms	–
SID.MEM#8	FLASH_ROW_PGM	Row program time after erase	–	–	7	ms	–
SID178	TBULKERASE	Bulk erase time (64k bytes)	–	–	35	ms	–
SID180	TDEVPROG	Total device program time	–	–	7.5	s	Guaranteed by characterization
SID182	FRET1	Flash retention, $T_A \leq 55°C$, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A	FRET2	Flash retention, $T_A \leq 85°C$, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization
SID182B	FRET3	Flash retention, $T_A \leq 105°C$, 10 K P/E cycles	3	–	–	years	Guaranteed by characterization

7 Ordering information

Table 41 lists the EZ-PD™ PMG1-S2 part numbers and features.

Table 41 EZ-PD™ PMG1-S2 Ordering information

MPN	Application	Termination resistor	Role	Package	Si ID
CYPM1211-40LQXI CYPM1211-40LQXIT	DRP applications	R_P[6], R_D[5], R_{D_DB}[7]	DRP	40-pin QFN	1D20
CYPM1211-42FNXIT				42-ball CSP	1D21

7.1 Ordering code definitions

The part numbers are of the form CYPM1ABC-DEFGHIJ where the fields are defined as follows.

Table 42 EZ-PD™ PMG1-S2 ordering code definitions

Field	Description	Values	Meaning
CY	Cypress prefix	CY	Company ID
PM	Marketing code	PM	PM = Power Delivery MCU family
1	MCU Family generation	1	Product family generation
A	Family	0	S0
		1	S1
		2	S2
		3	S3
B	PD Ports	1	1-PD port
		2	2-PD port
C	Application specific	X	Application specific
DE	Pin	XX	Number of pins in the package
FG	Package code	LQ	QFN
		BZ	BGA
		FN	CSP
H	Lead free	X	Lead: X = Pb-free
I	Temperature range	I	Industrial
J	Only for T&R	T	Tape and reel

Notes
5. Termination resistor denoting an upstream facing port.
6. Termination resistor denoting a downstream facing port.
7. Termination resistor denoting dead battery termination.

8 Packaging

Table 43 Package characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	Industrial	–40	25	85	°C
		Extended Industrial			105	
T_J	Operating junction temperature	Industrial	–40	25	100	
		Extended Industrial			125	
T_{JA}	Package θ_{JA} (40-pin QFN)	–	–	–	17	°C/W
T_{JC}	Package θ_{JC} (40-pin QFN)	–	–	–	2	
T_{JA}	Package θ_{JA} (42-pin CSP)	–	–	–	34	
T_{JC}	Package θ_{JC} (42-pin CSP)	–	–	–	0.3	

Table 44 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time within 5°C of peak temperature
40-pin QFN	260°C	30 seconds
42-ball CSP		

Table 45 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
40-pin QFN	MSL 3
42-ball CSP	MSL 1

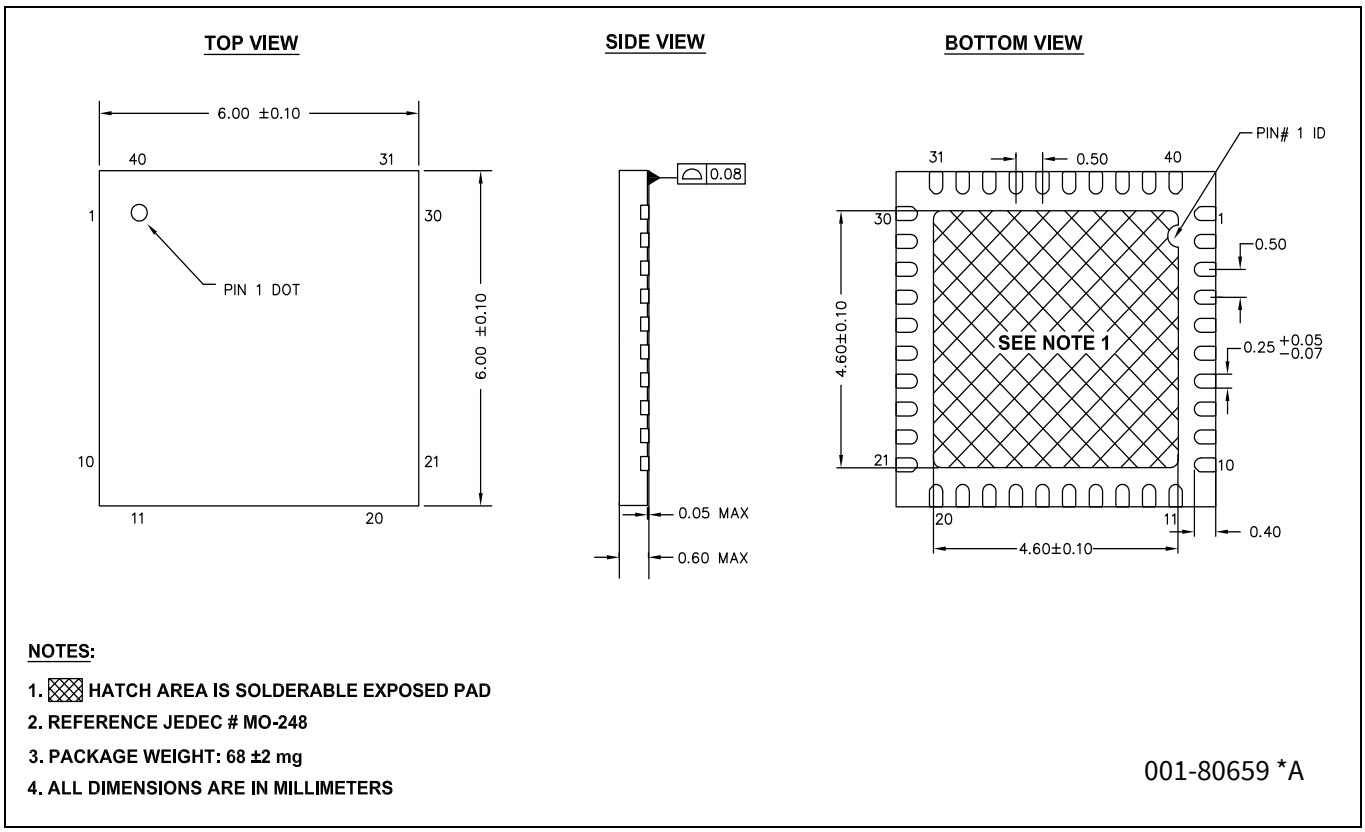

Figure 9 40-pin QFN package outline, 001-80659

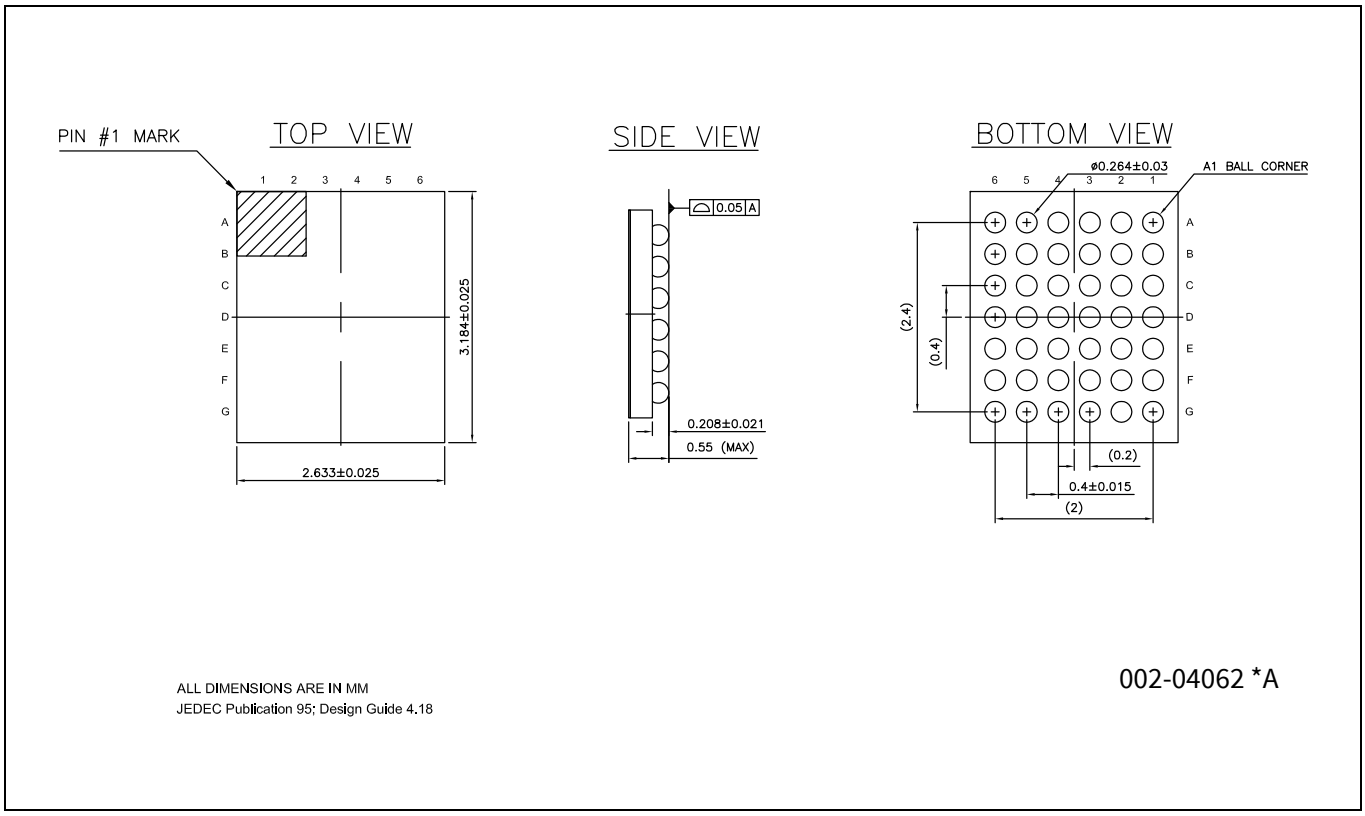

Figure 10 42-ball CSP package outline, 002-04062

9 Acronyms

Table 46 Acronyms used in this document

Acronym	Description
ADC	analog-to-digital converter
AES	advanced encryption standard
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus
API	application programming interface
Arm®	advanced RISC machine, a CPU architecture
BMC	Biphase Mark Code
CC	configuration channel
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role port
EEPROM	electrically erasable programmable read-only memory
EMCA	electronically marked cable assembly, a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FS	full-speed
GPIO	general-purpose input/output
HPD	hot plug detect
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
IOSS	input/output subsystem
I/O	input/output, see also GPIO
LDO	low-dropout regulator
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
MMIO	memory mapped input/output
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller
opamp	operational amplifier
OCP	overcurrent protection

Table 46 Acronyms used in this document *(continued)*

Acronym	Description
OVP	overvoltage protection
OVT	over voltage tolerant
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PRNG	pseudo random number generation
PWM	pulse-width modulator
RAM	random-access memory
RCP	reverse current protection, supported in Source Configuration only
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCB	serial communication block
SCL	I^2C serial clock
SCP	short circuit protection, supported in Source Configuration only
SDA	I^2C serial data
S/H	sample and hold
SHA	secure hash algorithm
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TCPWM	timer/counter pulse-width modulator
TRNG	true random number generation
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USB PD	USB Power Delivery
USB-FS	USB Full-Speed
USBIO	USB input/output, PMG1-S2 pins used to connect to a USB port
USB PD SS	USB PD subsystem
UVP	under voltage protection
VDM	vendor defined messages
XRES	external reset I/O pin

10 Document conventions

10.1 Units of measure

Table 47 Units of measure

Symbol	Unit of measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kiloohm
Mbps	megabits per second
MHz	megahertz
MΩ	megaohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Revision history

Document revision	Date	Description of change
**	2020-10-23	New datasheet.
*A	2021-02-25	Updated **EZ-PD™ PMG1 family general description**. Updated **Eclipse IDE for ModusToolbox™**. Updated **Application diagrams**. Added footnotes 1, 2, and 3. Removed V_{CONN_MAX} parameter from **Table 5**.
*B	2021-06-11	Removed Preliminary status of the datasheet. Updated **Table 3**. Updated **Acronyms**.
*C	2022-05-18	Added **Pin based absolute maximum ratings**. Migrated to IFX template.
*D	2022-07-04	Updated **Figure 1**. Added **Figure 5** and **Figure 10**. Updated **Table 1**, **Table 3**, **Table 4**, **Table 6**, **Table 41**, **Table 43**, **Table 44**, **Table 45**. Updated Block diagram.

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