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EZ-PD™ PMG1-S0 Power Delivery MCU

EZ-PD™ PMG1 family general description

EZ-PD™ PMG1 (Power Delivery Microcontroller Gen1) is a family of high-voltage USB-C Power Delivery (PD) microcontrollers (MCU). These chips include an Arm® Cortex®-M0/M0+ CPU and USB-C PD controller along with analog and digital peripherals. EZ-PD™ PMG1 is targeted for any embedded system that provides/consumes powers to/from a high-voltage USB-C PD port and leverages the microcontroller to provide additional control capability. **Figure 1** shows the EZ-PD™ PMG1 family segmentation.

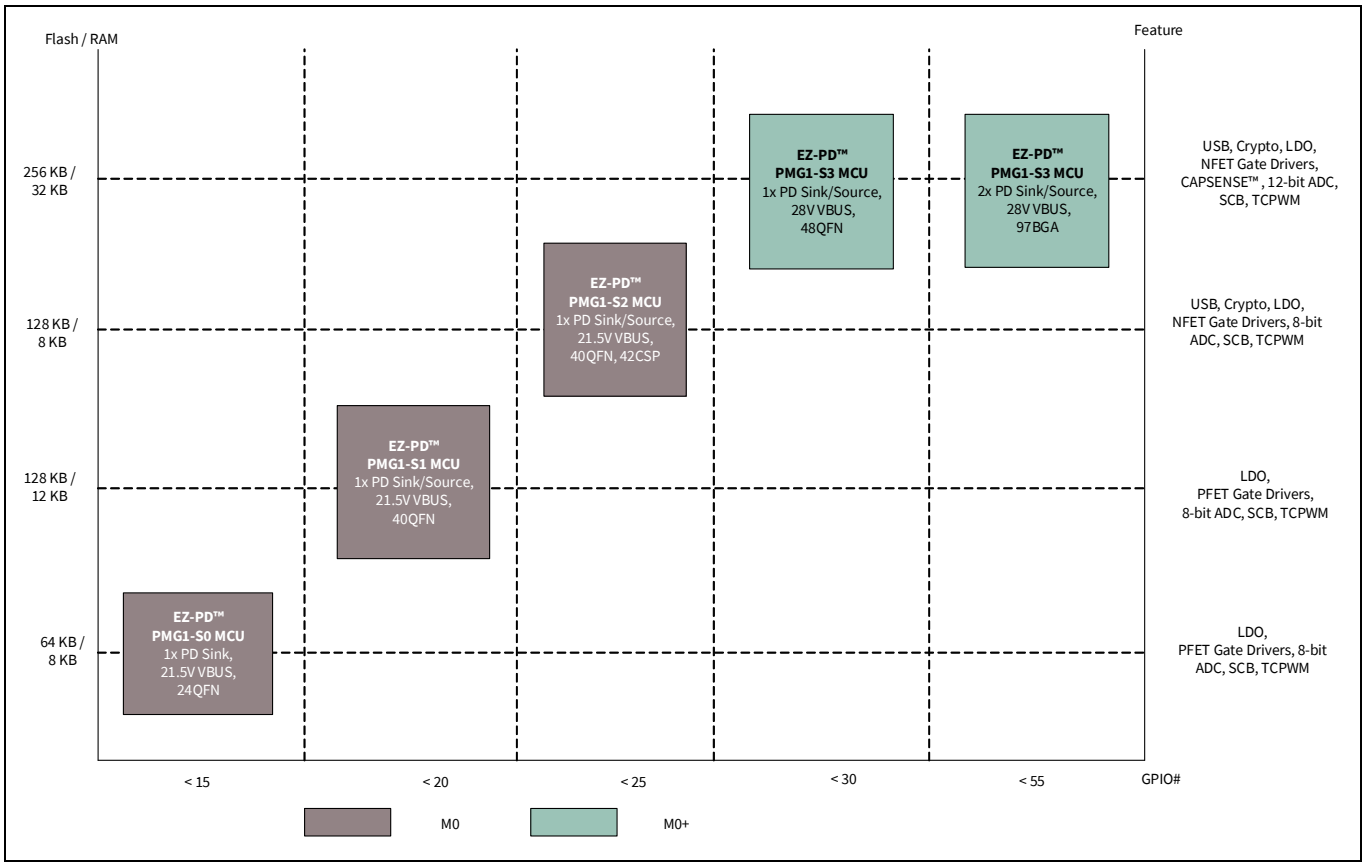


Figure 1 EZ-PD™ PMG1 family segmentation

Table 1 shows the comparison of features of different MCUs of the EZ-PD™ PMG1 family.

Table 1 Comparison of features of different MCUs of the EZ-PD™ PMG1 family

Subsystem or range	Item	EZ-PD™ PMG1-S0	EZ-PD™ PMG1-S1	EZ-PD™ PMG1-S2	EZ-PD™ PMG1-S3
CPU and Memory Sub-system	Core	Arm® Cortex®-M0	Arm® Cortex®-M0	Arm® Cortex®-M0	Arm® Cortex®-M0+
	Max freq (MHz)	48	48	48	48
	Flash (KB)	64	128	128	256
	SRAM (KB)	8	12	8	32
Power Delivery	Power Delivery Ports	1	1	1	1 port for 48-QFN 2 ports for 97-BGA
	Role	Sink	DRP	DRP	DRP
	MOSFET Gate Drivers	2x PFET	2x PFET	2x NFET	Flexible 2x NFET
	Fault Protections	VBUS OVP and UVP	VBUS OVP, UVP, and OCP. SCP and RCP (for Source Configuration only).	VBUS, OVP, UVP, and OCP	VBUS OVP, UVP, and OCP. SCP and RCP (for Source Configuration only).
USB	Integrated Full Speed USB 2.0 Device with Billboard Class Support	No	No	Yes	Yes
Voltage Range	Supply (V)	VDDD (2.7–5.5) VBUS (4–21.5)	VSYS (2.75–5.5) VBUS (4– 21.5)	VSYS (2.7–5.5) VBUS (4–21.5)	VSYS (2.8–5.5) VBUS (4–28)
	IO (V)	1.71 - 5.5	1.71 - 5.5	1.71 - 5.5	1.71 - 5.5
Digital	SCB (configurable as I2C/UART/SPI)	2	4	4	7 for 48-QFN (out of which only 5 can be configured as SPI and UART) 8 for 97-BGA
	TCPWM Block (configurable as timer, counter or pulse-width modulator)	4	2	4	7 for 48-QFN 8 for 97-BGA
	Hardware Authentication Block (Crypto)	No	No	Yes (AES-128/192/256, SHA1, SHA2-224, SHA2-256, PRNG10, CRC)	Yes (AES-128, SHA2-256, TRNG, Vector Unit)
Analog	ADC	2x 8-bit SAR	1x 8-bit SAR	2x 8-bit SAR	2x 8-bit SAR 1x 12-bit SAR
	On-chip Temperature Sensor	Yes	Yes	Yes	Yes

Table 1 Comparison of features of different MCUs of the EZ-PD™ PMG1 family *(continued)*

Subsystem or range	Item	EZ-PD™ PMG1-S0	EZ-PD™ PMG1-S1	EZ-PD™ PMG1-S2	EZ-PD™ PMG1-S3
Direct Memory Access (DMA)	DMA	No	No	No	Yes
GPIO	Max # of I/O	12 (10 + 2 OVT)	17 (15 + 2 OVT)	20 (18 + 2 OVT)	26 (24 + 2 OVT) for 48-QFN 50 (48 + 2 OVT) for 97-BGA
Charging Standards	Charging Source	-	BC 1.2, AC	BC 1.2, AC	BC 1.2, AC, AFC, and Quick Charge 3.0
	Charging Sink	BC 1.2, Apple Charging (AC)	BC 1.2, AC	BC 1.2, AC	BC 1.2, AC
ESD Protection	ESD Protection	Yes (up to ±8-kV Contact discharge, up to ±15-kV Air Discharge, human body model (HBM), and charged device model (CDM))	Yes (HBM and CDM)	Yes (up to ± 8-kV Contact discharge, up to ±15-kV Air Discharge, HBM and CDM)	Yes (HBM and CDM)
Packages	Package Options	24-QFN (4 × 4 mm, 0.5 mm pitch)	40-QFN (6 × 6 mm, 0.5 mm pitch)	40-QFN (6 × 6 mm, 0.5 mm pitch) 42-CSP (2.63 × 3.18 mm, 0.4 mm pitch)	48-QFN (6 × 6 mm, 0.5 mm pitch) 97-BGA (6 × 6 mm, 0.5 mm and 0.65 mm pitch)

The rest of the document discusses the EZ-PD™ PMG1-S0 device in detail.

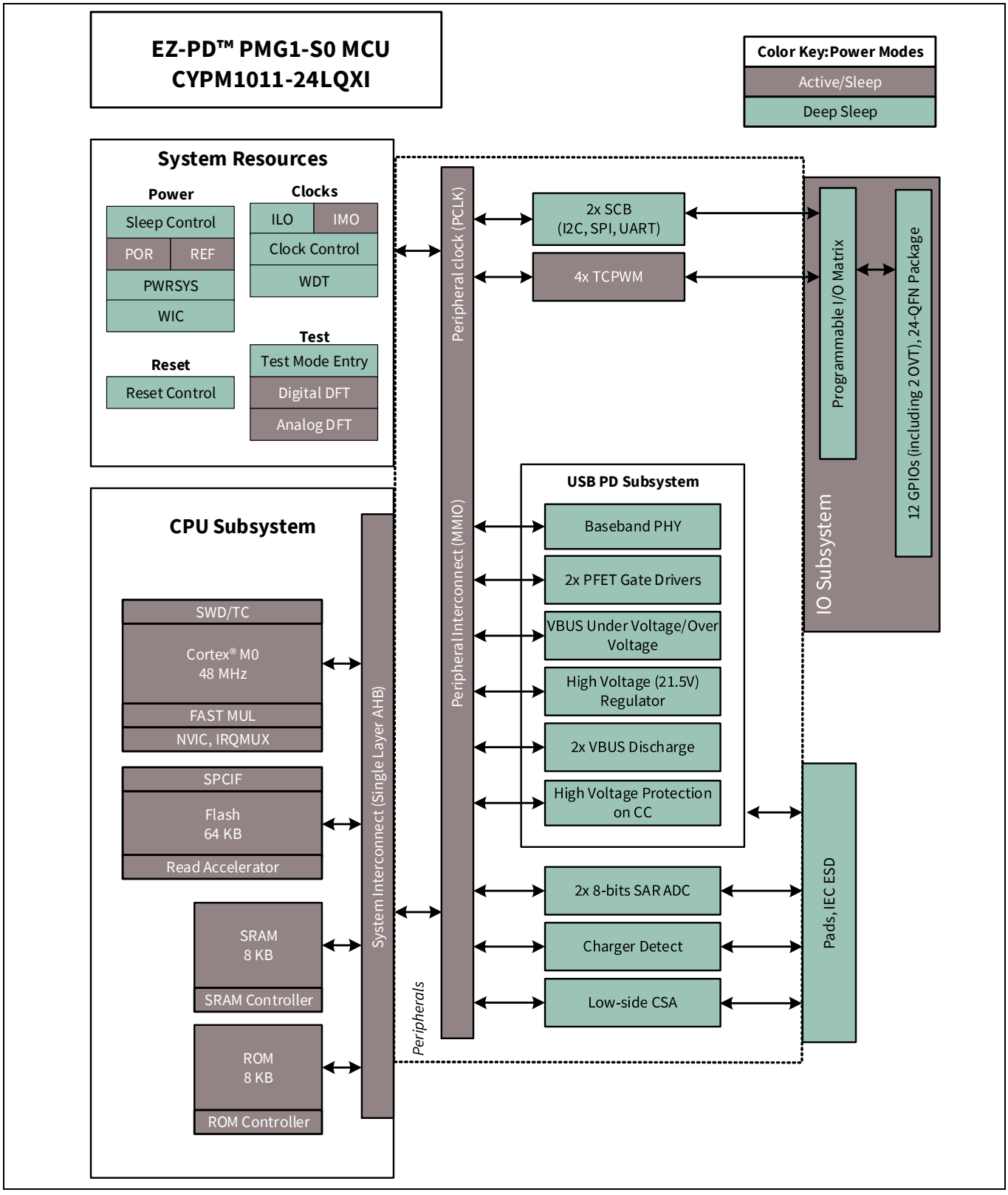
EZ-PD™ PMG1-S0 general description

EZ-PD™ PMG1-S0 includes 64-KB flash, a complete Type-C USB-PD transceiver, a pull-down termination resistor R_D to support Sink on the Type-C port, and system-level ESD protection. It is available in a 24-pin QFN package.

Features

- Type-C Support and USB PD Support
  - Supports USB PD 3.0 Version 2.0 Spec
  - Termination resistor R_D
  - Supports one USB Type-C port
- Legacy/proprietary charging block
  - Supports Apple charging 2.4A, BC 1.2
  - Integrates all required terminations on USBDP/DM lines
- System-level fault protection
  - VBUS to CC short protection
  - On-chip overvoltage protection (OVP) and undervoltage protection (UVP)
  - Low-side current sense amplifier (CSA) for overcurrent protection (OCP) and short circuit protection (SCP)
- 32-bit MCU subsystem
  - Arm® Cortex®-M0 CPU
  - 64-KB Flash
  - 8-KB SRAM
- Clocks and oscillators
  - Integrated oscillator eliminating the need for external clock
- Power
  - VDDD (2.7 V–5.5 V)
  - VBUS (4.0 V–21.5 V)
- System-Level ESD protection
  - On CC, VBUS_MON, USBDP, USBDM, P2.2, and P2.3 pins
  - ± 8-kV contact discharge and ±15-kV Air Gap discharge based on IEC61000-4-2 level 4C
- Packages
  - 24-pin QFN
  - Supports extended industrial temperature range (–40°C to +105°C)

Block diagram



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1 Development support

The EZ-PD™ PMG1 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit **EZ-PD™ PMG1 MCU** webpage to find out more.

1.1 Documentation

A suite of documentation supports the EZ-PD™ PMG1 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software user guide: A step-by-step guide for using ModusToolbox™ software. The software user guide shows you how ModusToolbox™ software build process works in detail, how to use source control with ModusToolbox™ software, and much more.

Component datasheets: The flexibility of EZ-PD™ PMG1 allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all the information needed to select and use a particular component, including functional description, API documentation, example codes, and AC/DC specifications.

Application notes: This includes the getting started application note and the hardware design guidelines.

Technical reference manual: The technical reference manual (TRM) contains all the technical detail you need to use a EZ-PD™ PMG1 device, including a complete description of all EZ-PD™ PMG1 registers. The TRM is available in the Documentation section at **EZ-PD™ PMG1 MCU** webpage.

1.2 Online

In addition to print documentation, the **EZ-PD™ PMG1 MCU forums** connect you with fellow users and experts in PMG1 from around the world, 24 hours a day, 7 days a week.

1.3 Tools

With industry standard cores, programming, and debugging interfaces, the EZ-PD™ PMG1 MCU family is part of a development tool ecosystem.

Visit us at **ModusToolbox™ software** for the latest information on the revolutionary, easy to use Eclipse IDE for ModusToolbox™, supported third party compilers, programmers, debuggers, and development kits.

1.4 Eclipse IDE for ModusToolbox™

ModusToolbox™ software is an Eclipse-based development environment on Windows, macOS, and Linux platforms that includes the Eclipse IDE for ModusToolbox™. The Eclipse IDE for ModusToolbox™ brings together several device resources, middleware, and firmware to build an application. Using ModusToolbox™ software, you can enable and configure device resources and middleware libraries, write C/C++/assembly source code, and program and debug the device.

For additional details on using the ModusToolbox™ software, refer to **AN232553 - Getting started with EZ-PD™ PMG1 MCU on ModusToolbox™ software** and the documentation and help integrated into ModusToolbox™ software. As **Figure 2** shows, with the Eclipse IDE for ModusToolbox™, you can:

1. Create a new application based on a list of template applications, filtered by kit or device, or browse the collection of code examples online.
2. Configure device resources in Device Configurator to build your hardware system design in the workspace.
3. Add software components or middleware.
4. Develop your application firmware.

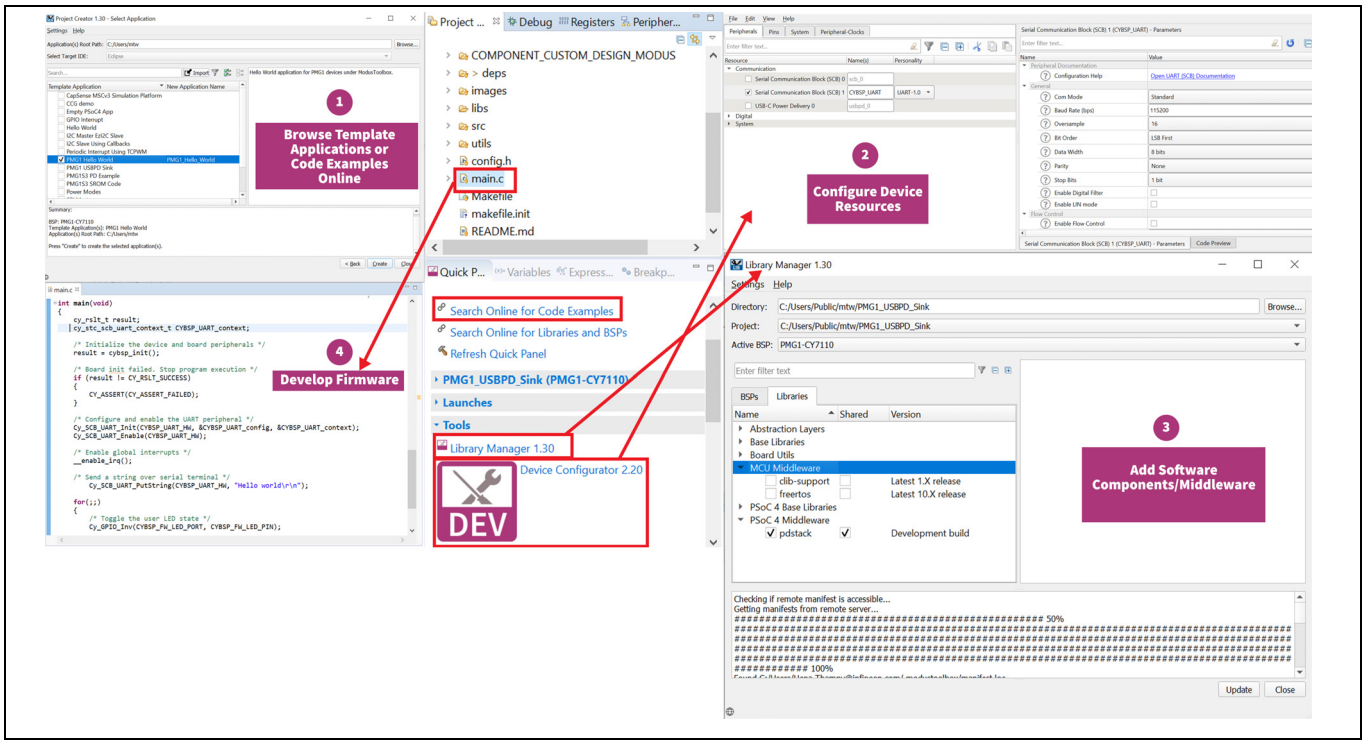


Figure 2 Eclipse IDE for ModusToolbox™ and middleware

2 Functional overview

2.1 MCU subsystem

2.1.1 CPU

The Cortex®-M0 CPU in EZ-PD™ PMG1-S0 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating.

The CPU also includes a serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for EZ-PD™ PMG1-S0 has four break-point (address) comparators and two watchpoint (data) comparators.

2.1.2 Flash

The EZ-PD™ PMG1-S0 device has a flash module with one bank of 64-KB flash, a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block.

2.1.3 SROM

A supervisory ROM that contains boot and configuration routines is provided.

2.2 USB PD subsystem (SS)

The USB PD subsystem provides the interface to the Type-C USB port. This subsystem comprises a high-voltage regulator, OVP, and supply switch blocks. This subsystem also includes all ESD required and supported on the Type-C port.

2.2.1 USB PD physical layer

The USB PD physical layer consists of a transmitter and receiver that communicate BMC-encoded data over the CC channel based on the PD 3.0 standard. All communication is half-duplex. The Physical Layer or PHY practices collision avoidance to minimize communication errors on the channel.

The USBPD block includes the R_D termination resistor and switch as required by the USB Type-C spec. The termination resistor is required to implement connection detection, plug orientation detection, and for establishing the sink power role. A dead-battery R_D termination enables identification as a sink while the EZ-PD™ PMG1-S0 device is not powered.

2.2.2 ADC

The ADC is a low-footprint 8-bit 125 ksps SAR ADC that is available for general-purpose A-D conversion applications in the chip. This ADC can be accessed from all GPIOs and the USBDP/DM pins through an on-chip analog mux. EZ-PD™ PMG1-S0 contains two instances of the ADC. The voltage reference for the ADCs is generated either from the VDDD supply or from internal bandgap. When sensing the GPIO pin voltage with an ADC, the pin voltage cannot exceed the VDDIO supply value.

2.2.3 Charger detection

The charger detection block connected to the USBDP/DM pins allow EZ-PD™ PMG1-S0 to detect conventional battery chargers conforming to BC 1.2, and Apple charging standard.

2.2.4 VBUS UVP and OVP

The EZ-PD™ PMG1-S0 chip has an integrated hardware block for VBUS OVP/UVP with configurable thresholds and response times on the Type C port.

2.2.5 VBUS short protection

EZ-PD™ PMG1-S0 provides four VBUS short protection pins: CC1, CC2, P2.2, and P2.3. These pins are protected from accidental shorts to high-voltage VBUS. Accidental shorts may occur because the CC1 and CC2 pins are placed next to the VBUS pins in the USB Type-C connector. A Power Delivery controller without the high-voltage VBUS short protection will be damaged in the event of accidental shorts. When the protection circuit is triggered,

EZ-PD™ PMG1-S0 can handle up to 17 V forever and between 17 V to 22 VDC for 1000 hours on the OVT pins. When a VBUS short event occurs on the CC pins, a temporary high-ringing voltage is observed due to the RLC elements in the USB Type-C cable. Without EZ-PD™ PMG1-S0 connected, this ringing voltage can be twice (44 V) the maximum VBUS voltage (21.5 V). However, when EZ-PD™ PMG1-S0 is connected, it is capable of clamping temporary high-ringing voltage and protecting the CC pin using IEC ESD protection diodes.

2.2.6 Low-side current sense amplifier (CSA)

EZ-PD™ PMG1-S0 chip also has an integrated low-side current sense amplifier that is capable of detecting current levels ranging from 100 mA to 5.5 A across a 5 mΩ external resistor, which can be used to implement overcurrent protection (OCP).

2.2.7 PFET gate drivers on VBUS path

EZ-PD™ PMG1-S0 has two integrated PFET gate drivers to drive external PFETs on the VBUS consumer paths. The VBUS_FET_CTRL_0 gate driver has an active pull-up, and thus can drive high, low or High-Z.

The VBUS_FET_CTRL_1 gate driver can drive only low or high-Z, thus requiring an external pull-up. These pins are VBUS voltage-tolerant.

2.2.8 VBUS discharge FETs

EZ-PD™ PMG1-S0 also has two integrated VBUS discharge FETs used to discharge VBUS to meet the USB PD specification timing on a detach condition.

2.3 Integrated digital blocks

2.3.1 Serial communication blocks (SCB)

EZ-PD™ PMG1-S0 has two SCBs, which can be configured to implement an I^2C, SPI, or UART interface. The hardware I^2C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as master or slave.

In the I^2C mode, the SCB blocks are capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I^2C that creates a mailbox address range in the memory of EZ-PD™ PMG1-S0 and effectively reduce I^2C communication to reading from and writing to an array in memory. In addition, the blocks support 8-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripherals are compatible with the I^2C Standard-mode, Fast Mode, and Fast Mode Plus devices as defined in the NXP I^2C-bus specification and user manual (**UM10204**). The I^2C bus I/Os are implemented with GPIO in open-drain modes.

The I^2C port on the SCB blocks of EZ-PD™ PMG1-S0 are not completely compliant with the I^2C spec in the following aspects:

- The GPIO cells for SCB 1's I^2C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast Mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast Mode and Fast Mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

2.3.2 Timer/counter/PWM block (TCPWM)

EZ-PD™ PMG1-S0 has four TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality. The block can be used to measure the period and pulse width of an input signal (timer), find the number of times a particular event occurs (counter), generate PWM signals, or decode quadrature signals.

2.4 I/O subsystem

EZ-PD™ PMG1-S0 has up to 12 GPIOs of which, some of them can be re-purposed to support functions of SCB (I^2C, UART, SPI). GPIO pins P0.0 and P0.1 are overvoltage-tolerant (OVT) (up to 6 V).

The GPIO block implements the following:

- Seven drive strength modes
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Port pins P1.0 and P1.1 can be configured to indicate fault for OVP/UVP conditions. The two fault conditions can be mapped to two GPIOs can be OR’ed to indicate over one GPIO.

3 Power systems overview

EZ-PD™ PMG1-S0 can operate from two possible external supply sources: VBUS (4.0 V–21.5 V) or VDDD (2.7 V–5.5 V). When powered through VBUS, the internal regulator generates VDDD of 3.3 V for chip operation. The regulated supply, VDDD, is either used directly inside some analog blocks or further regulated down to VCCD (1.8 V), which powers majority of the core using the regulators. EZ-PD™ PMG1-S0 has three different power modes: Active, Sleep, and Deep Sleep. Transitions between these power modes are managed by the power system. When powered through the VBUS pin, VDDD cannot be used to power external devices and should be connected to a 1-µF capacitor for the regulator stability only. These pins are not supported as power supplies. Refer to the application diagrams for capacitor connections.

Table 2 EZ-PD™ PMG1-S0 power modes

Mode	Description
Power-on Reset (POR)	Power is valid and an internal reset source is asserted or SleepController is sequencing the system out of reset.
ACTIVE	Power is valid and CPU is executing instructions.
SLEEP	Power is valid and CPU is not executing instructions. All logic that is not operating is clock gated to save power.
DEEP SLEEP	Main regulator and most blocks are shut off. DeepSleep regulator powers logic, but only low-frequency clock is available.

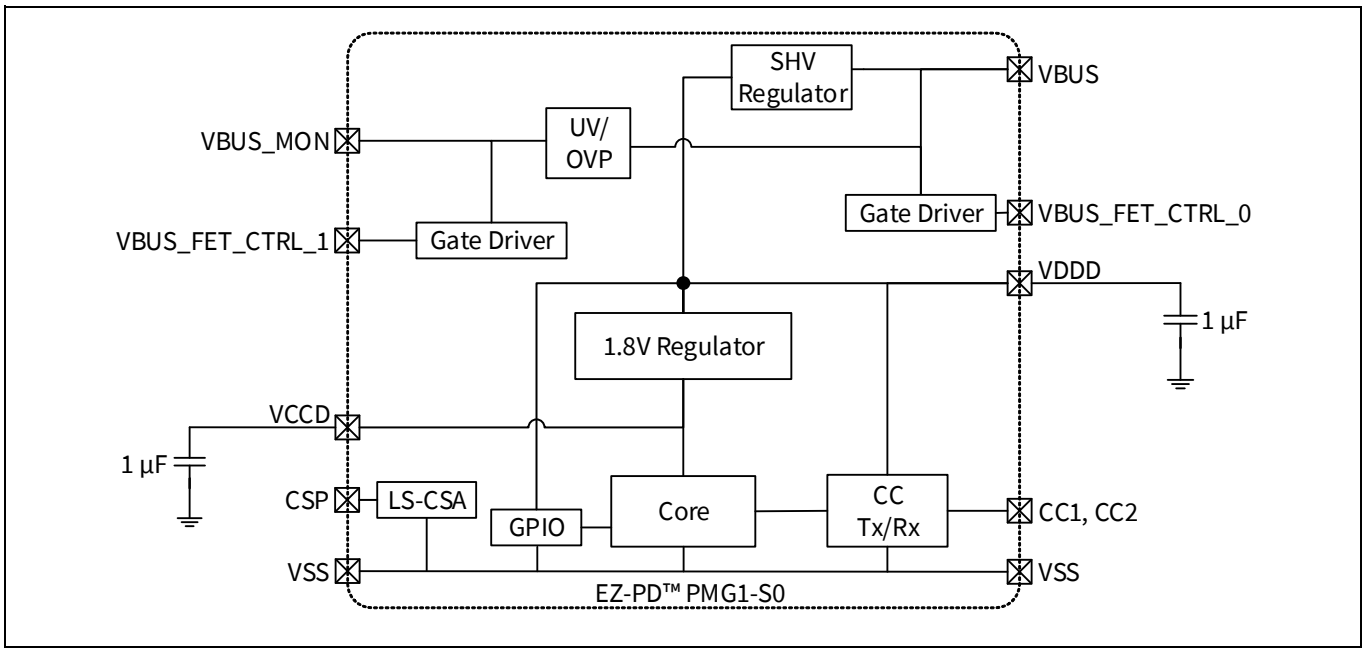


Figure 3 Power system requirement block diagram

4 Pinouts

Table 3 EZ-PD™ PMG1-S0 pin descriptions

Group	24-pin QFN	Pin name	Description
GPIOs and serial interface	1	P1.0/UART_1_CTS/ SPI_0_SEL/I2C_1_SDA	Port 1 pin 0: GPIO/UART_1_CTS/SPI_0_SEL/I2C_1_SDA[1]/ TCPWM_line_2[4], Programmable OVP/UVP Fault indication
	2	P1.1/UART_1_RTS/ SPI_0_MISO/I2C_1_SCL	Port 1 pin 1: GPIO/UART_1_RTS/SPI_0_MISO/I2C_1_SCL[1] / TCPWM_line_3[5], Programmable OVP/UVP Fault indication
	5	P1.2/UART_1_TX1/ SPI_0_MOSI	Port 1 pin 2: GPIO/UART_1_TX1/SPI_0_MOSI
	6	P1.3/UART_1_RX1/ SPI_0_CLK	Port 1 pin 3: GPIO/UART_1_RX1/SPI_0_CLK
	7	P0.0/SWD_IO/ UART_0_CTS/ SPI_1_MOSI/I2C_0_SDA	Port 0 pin 0: GPIO/OVT/SWD_IO/UART_0_CTS/SPI_1_MOSI/I2C_0_SDA/ TCPWM_line_0[2]
	8	P0.1/SWD_CLK/ UART_0_RTS/ SPI_1_MISO/I2C_0_SCL	Port 0 pin 1: GPIO/OVT/SWD_CLK/UART_0_RTS/SPI_1_MISO/I2C_0_SCL/T CPWM_line_1[3]
	9	P2.0/UART_0_TX0/ SPI_1_SEL	Port 2 pin 0: GPIO/TCPWM_line_2/UART_0_TX0/SPI_1_SEL This pin is internally pulled up during the Power-On I/O initialization time (see **Table 8** for more details). Also, this is an output only pin that can be used in open drain mode of operation only.
	10	P2.1/UART_0_RX0/ SPI_1_CLK	Port 2 pin 1: GPIO/TCPWM_line_3/UART_0_RX0/SPI_1_CLK
	12	P2.2/UART_0_TX1/ I2C_1_SDA	Port 2 pin 2: GPIO with Open drain with pull-up assist. Configurable as GPIO_20VT[6]/ UART_0_TX1/ I2C_1_SDA/TCPWM_line_0/IEC. Tolerant to temporary short to VBUS pin.
	13	P2.3/UART_0_RX1/ I2C_1_SCL	Port 2 pin 3: GPIO with Open drain with pull-up assist. Configurable as GPIO_20VT/ UART_0_RX1/ I2C_1_SCL/TCPWM_line_1/IEC. Tolerant to temporary short to VBUS pin.
	16	P3.1/USBDM/ UART_1_RX0	USBDM/Port 3 pin 1: GPIO/UART_1_RX0/BC 1.2/Apple Charging/IEC
	17	P3.0/USBDP/ UART_1_TX0	USBDP/Port 3 pin 0: GPIO/UART_1_TX0/BC 1.2/Apple Charging/IEC
USB Type-C	14	CC2	Communication Channel 2 with Dead-battery R_D Bonding Option/IEC. Tolerant to temporary short to VBUS pin.
	15	CC1	Communication Channel 1 with Dead-battery R_D Bonding Option/IEC. Tolerant to temporary short to VBUS pin.

Notes

1. Out of the two SCB blocks (SCB0 and SCB1), while the SCB0's I2C functionality is mapped out to the P0.0/P0.1 GPIO pins, the I2C functionality of SCB1 provides flexibility to have it mapped either on P1.0/P1.1 OR P2.2/P2.3 GPIO pins.
2. TCPWM_line_0 can be mapped to port pins P0.0 or P2.2.
3. TCPWM_line_1 can be mapped to port pins P0.1 or P2.3.
4. TCPWM_line_2 can be mapped to port pins P1.0 or P2.0.
5. TCPWM_line_3 can be mapped to port pins P1.1 or P2.1.
6. See **Table 11** and **Table 12** for specifications related to these pins.

Table 3 EZ-PD™ PMG1-S0 pin descriptions *(continued)*

Group	24-pin QFN	Pin name	Description
VBUS	3	VBUS_FET_CTRL_0	External PMOS FET control (30-V Tolerant) with internal pull-up 0: Path ON 1: Path OFF
	4	VBUS_FET_CTRL_1	External PMOS FET Control (30-V Tolerant) 0: Path ON Z: Path OFF To use this pin, provide external pull-up
	11	VBUS_MON	Type C VBUS Monitor with Internal Discharge FET
Power	18	VBUS	VBUS Power IN (4.0 V–21.5 V) with Internal Discharge FET
	23	VDDD	Output of internal 3.3-V regulator. Connect 1 µF and 2x 100 nF capacitors.
	24	VCCD	Output of internal 1.8-V regulator (not intended for use as a power source). Connect a 1 µF decoupling capacitor.
GND	19	CSP	Current Sense Positive input for low-side CSA
	22	GND	Ground
	EPAD	GND	Ground
NC	20	NC	Not connected
	21	NC	Not connected

Table 4 SCBs and their functionality

Port	24-QFN	SCB function			TCPWM	Fault indicator	Protection capability		USB charging signal		IEC4
Pin	Pin#	UART	SPI	I2C			VBUS Short	OVT	BC1.2	Apple	
P0.0	7	UART_0_CTS	SPI_1_MOSI	I2C_0_SDA	TCPWM_line_0:0	–	–	Yes	–	–	–
P0.1	8	UART_0_RTS	SPI_1_MISO	I2C_0_SCL	TCPWM_line_1:0	–	–	Yes	–	–	–
P1.0	1	UART_1_CTS	SPI_0_SEL	I2C_1_SDA:1	TCPWM_line_2:1	Yes	–	-	–	–	–
P1.1	2	UART_1_RTS	SPI_0_MISO	I2C_1_SCL:1	TCPWM_line_3:1	Yes	–	-	–	–	–
P1.2	5	UART_1_TX1	SPI_0_MOSI	–	–	–	–	–	–	–	–
P1.3	6	UART_1_RX1	SPI_0_CLK	–	–	–	–	–	–	–	–
P2.0	9	UART_0_TX0	SPI_1_SEL	–	TCPWM_line_2:0	–	–	–	–	–	–
P2.1	10	UART_0_RX0	SPI_1_CLK	–	TCPWM_line_3:0	–	–	–	–	–	–
P2.2	12	UART_0_TX1	–	I2C_1_SDA:0	TCPWM_line_0:1	–	Yes	–	–	–	Yes
P2.3	13	UART_0_RX1	–	I2C_1_SCL:0	TCPWM_line_1:1	–	Yes	–	–	–	Yes
P3.0	17	UART_1_TX0	–	–	–	–	–	–	USBDP	USBDP	Yes
P3.1	16	UART_1_RX0	–	–	–	–	–	–	USBDM	USBDM	Yes

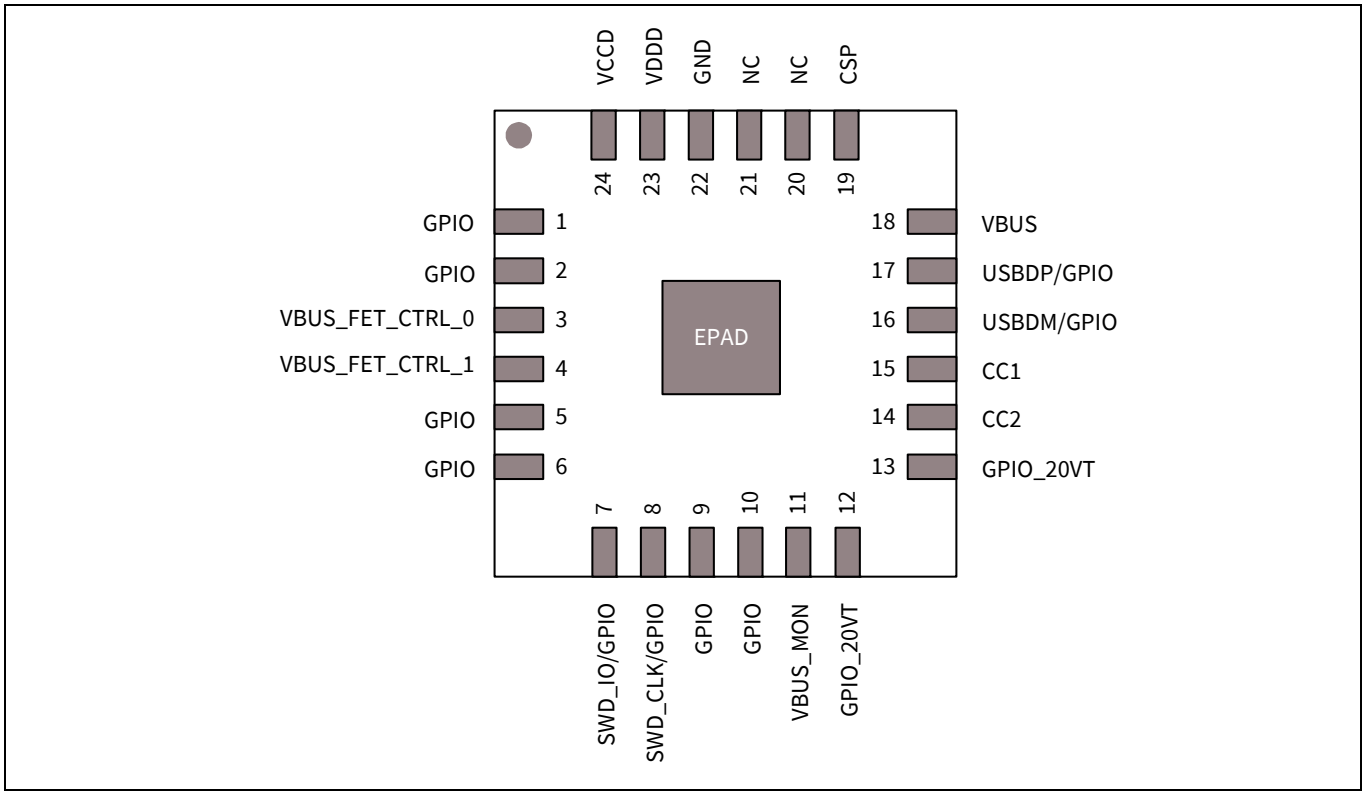


Figure 4 Pinout of 24-QFN package (top view)

5 Application diagram

Figure 5 illustrates the Sink application using EZ-PD™ PMG1-S0. It has two main parts: USB Type-C receptacle to provide the input power to the application and load used as the output power.

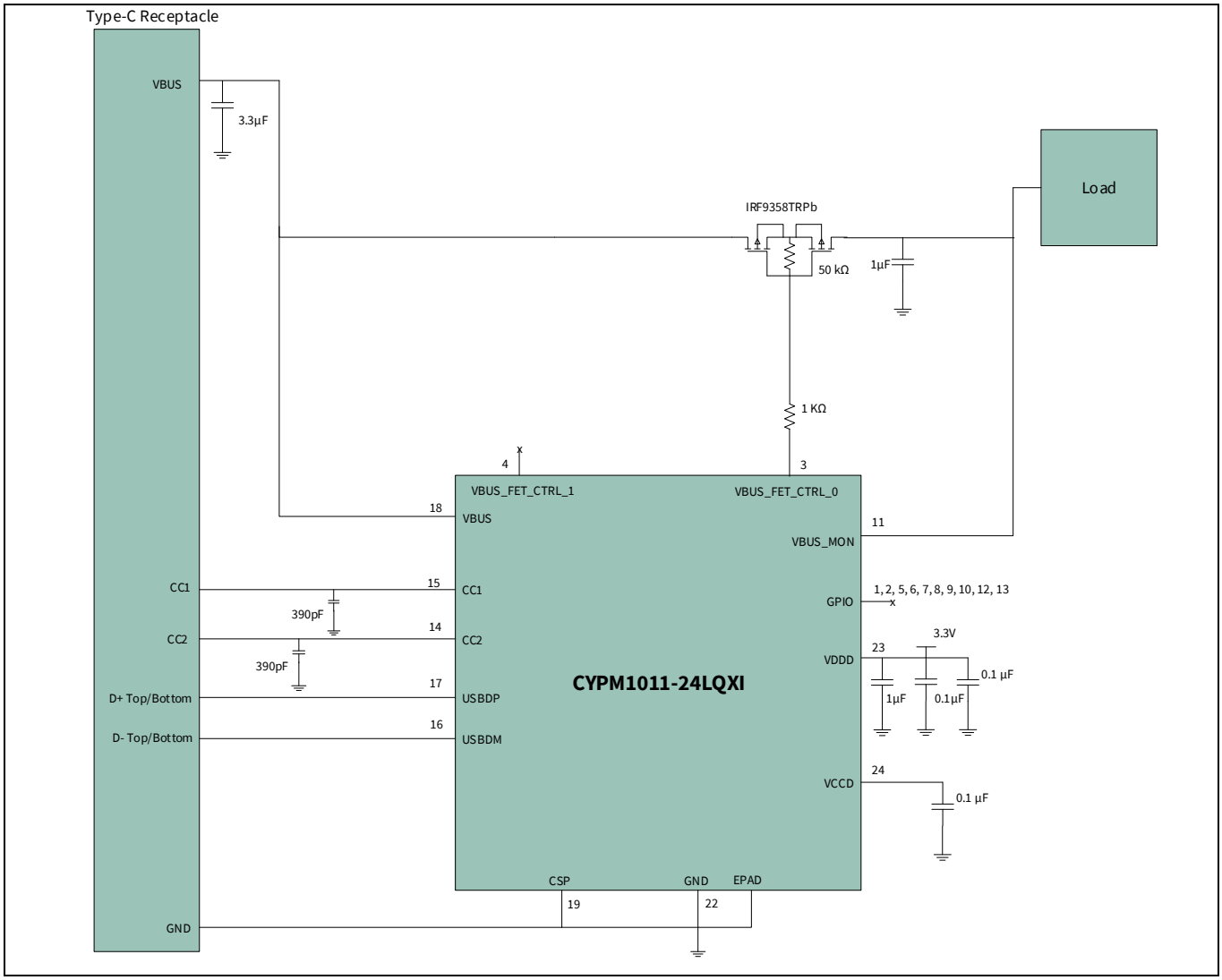


Figure 5 EZ-PD™ PMG1-S0 based sink application diagram

6 Electrical specifications

6.1 Absolute maximum ratings

Table 5 Absolute maximum ratings[7]

Parameter	Description	Min	Typ	Max	Units	Details/conditions
V_{BUS_MAX}	Max supply voltage relative to V_{SS} on VBUS and VBUS_MON pins	–	–	30	V[8]	Absolute max
V_{DDD_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	
$V_{CC_PIN_ABS}$	Max voltage on CC1, CC2 pins and port pins P2.2 and P2.3 for applicable devices	–	–	22[9]	V	
V_{GPIO_ABS}	GPIO voltage	–0.5[10]	–	V_{DDD} +0.5	V	
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
$I_{GPIO_injection}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$	–0.5	–	0.5	mA	Absolute max, current injected per pin
$V_{GPIO_OVT_ABS}$	OVT GPIO voltage	–0.5	–	6	V	Applicable to port pins P0.0 and P0.1
ESD_HBM	Electrostatic discharge human body model (ESD-HBM)	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model (ESD-CDM)	500	–	–	V	–
LU	Pin current for latch-up	–100	–	100	mA	–
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000	–	–	V	Contact discharge on CC1, CC2, VBUS, P2.2 and P2.3 pins
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2	15000	–	–	V	Air discharge for USBDP, USBDM, CC1, CC2, VBUS, P2.2 and P2.3 pins

Notes

7. Usage above the absolute maximum conditions listed in **Table 5** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.
8. All voltages are relative to Ground unless otherwise specified.
9. As per USB PD specification, maximum allowed VBUS = 21.5 V.
10. In a system, if the negative spike exceeds the minimum voltage specified here, it is recommended to add Schottky diode to clamp the negative spike.

6.2 Pin based absolute maximum ratings

Table 6 Pin based absolute maximum ratings

S. No.	Pin (24 QFN)	Name	Absolute minimum (V)	Absolute maximum (V)	Remarks
1	1	P1.0	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
2	2	P1.1	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
3	5	P1.2	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
4	6	P1.3	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
5	7	P0.0	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
6	8	P0.1	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
7	9	P2.0	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
8	10	P2.1	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
9	12	P2.2	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
10	13	P2.3	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
11	16	P3.1	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
12	17	P3.0	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
13	14	CC2	-0.5	22	–
14	15	CC1	-0.5	22	–
15	3	VBUS_FET_CTRL_0	-0.5	30	This is an output only pin
16	4	VBUS_FET_CTRL_1	-0.5	30	This is an output only pin
17	11	VBUS_MON	–	30	–
18	18	VBUS	–	30	–
19	23	VDDD	–	6	–
20	24	VCCD	–	1.95	This is an output only pin
21	19	CSP	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
22	22	GND	–	–	–
23	EPAD	GND	–	–	–
24	20	NC	–	–	–
25	21	NC	–	–	–

6.3 Device-level specifications

All specifications are valid for –40°C ≤ T_A ≤ 105°C and T_J ≤ 120°C, except where noted.

Table 7 DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#2	V_{DDD}	Power supply input voltage	2.7	–	5.5	V	Sink mode, –40°C ≤ T_A ≤ 105°C.
SID.PWR#3	V_{BUS_IN}	Power supply input voltage	4.0	–	21.5	V	–40°C ≤ T_A ≤ 105°C.
SID.PWR#5	V_{CCD}	Output voltage for core logic	–	1.8	–	V	–
SID.PWR#13	C_{exc}	Power supply decoupling capacitor for V_{DDD}	0.8	1	–	µF	X5R ceramic or better

Table 7 DC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#14	C_{exv}	Power supply decoupling capacitor for VBUS	–	0.1	–	µF	X5R ceramic or better
Active Mode. Typical values measured at V_{DDD} = 5.0 V or V_{BUS} = 5.0 V and T_A = 25°C.							
SID.PWR#8	I_{DD_A}	Supply current from V_{BUS} or V_{DDD}	–	10	–	mA	V_{DDD} = 5 V OR V_{BUS} = 5 V, T_A = 25°C. CC1/CC2 in Tx or Rx, no I/O sourcing current, 2 SCBs at 1 Mbps, ADC/UVOV ON, CPU at 24 MHz.
Sleep Mode. Typical values measured at V_{DD} = 3.3 V and T_A = 25°C.							
SID25A	I_{DD_S}	CC, I^2C, WDT wakeup on. IMO at 24 MHz.	–	3	–	mA	V_{DDD} = 3.3 V, T_A = 25°C, All blocks except CPU are on, CC IO on, ADC/UVOV On.
Deep Sleep Mode. Typical values measured at T_A = 25°C.							
SID_DS_A_SNK	$I_{DD_PB_DS_A_SNK}$	V_{BUS} = 4.0 to 21.5 V. CC, I^2C, WDT Wakeup on	–	500	–	µA	Power sink application V_{BUS} = 21.5 V, T_A = 25°C, Part is in deep sleep. Attached, CC I/O on, ADC/UVOV On.

Table 8 AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID.CLK#4	F_{CPU}	CPU input frequency	DC	–	48	MHz	All V_{DDD}
SID.PWR#17	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	–
SID.PWR#18	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	35	µs	–
SYS.FES#1	$T_{_PWR_RDY}$	Power-up to “Ready to accept I^2C/CC command”	–	5	25	ms	–
SID.PWR#18A	$T_{POR_HIZ_T}$	Power-on I/O Initialization Time	–	3	–	ms	–

6.3.1 I/O

Table 9 I/O DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.GIO#37	V_{IH_CMOS}	Input voltage HIGH threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID.GIO#38	V_{IL_CMOS}	Input voltage LOW threshold	–	–	0.3 × V_{DDD}	V	CMOS input
SID.GIO#39	$V_{IH_VDDD2.7-}$	LVTTL input, V_{DDD} < 2.7 V	0.7× V_{DDD}	–	–	V	–
SID.GIO#40	$V_{IL_VDDD2.7-}$	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 × V_{DDD}	V	–
SID.GIO#41	$V_{IH_VDDD2.7+}$	LVTTL input, V_{DDD} ≥ 2.7 V	2.0	–	–	V	–
SID.GIO#42	$V_{IL_VDDD2.7+}$	LVTTL input, V_{DDD} ≥ 2.7 V	–	–	0.8	V	–
SID.GIO#33	V_{OH_3V}	Output voltage HIGH level	V_{DDD} – 0.6	–	–	V	I_{OH} = 4 mA at 3-V V_{DDD}
SID.GIO#36	V_{OL_3V}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 10 mA at 3-V V_{DDD}
SID.GIO#5	R_{PU}	Pull-up resistor value	3.5	5.6	8.5	kΩ	+25°C T_A, all V_{DDD}
SID.GIO#6	R_{PD}	Pull-down resistor value	3.5	5.6	8.5	kΩ	+25°C T_A, all V_{DDD}
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25°C T_A, 3-V V_{DDD}
SID.GIO#17	C_{PIN_A}	Max pin capacitance	–	–	22	pF	Capacitance on USBDP, USBDM pins. Guaranteed by characterization.
SID.GIO#17A	C_{PIN}	Max pin capacitance	–	3	7	pF	–40°C to +85°C T_A, All V_{DDD}, all other I/O_S. Guaranteed by characterization.
SID.GIO#43	V_{HYSTTL}	Input hysteresis, LVTTL V_{DDD} > 2.7 V	15	40	–	mV	Guaranteed by characterization.
SID.GIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDD}	–	–	mV	V_{DDD} < 4.5 V. Guaranteed by characterization.
SID69	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	Guaranteed by design.
SID.GIO#45	I_{TOT_GPIO}	Maximum total sink chip current	–	–	85	mA	Guaranteed by design.
OVT							
SID.GIO#46	I_{IHS}	Input current when Pad > V_{DDD} for OVT inputs	–	–	10.00	µA	Per I^2C specification

Table 10 I/O AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID70	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{load} = 25 pF
SID71	T_{FALLF}	Fall time in Fast Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{load} = 25 pF

Table 11 GPIO_20VT DC specifications (Applicable to port pins P2.2 and P2.3 only)

(guaranteed by characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.GPIO_20VT#4	GPIO_20VT_I_LU	GPIO_20VT Latch up current limits	–140	–	140	mA	Max / min current in to any input or output, pin-to-pin, pin-to-supply
SID.GPIO_20VT#5	GPIO_20VT_RPU	GPIO_20VT Pull-up resistor value	1	–	25	kΩ	+25°C T_A, 1.4 V to GPIO_20VT_Voh(min)
SID.GPIO_20VT#6	GPIO_20VT_RPD	GPIO_20VT Pull-down resistor value	2.5	–	20	kΩ	+25°C T_A, 1.4-V to V_{DDD}
SID.GPIO_20VT#16	GPIO_20VT_IIL	GPIO_20VT Input leakage current (absolute value)	–	–	2	nA	+25°C T_A, 3-V V_{DDD}
SID.GPIO_20VT#17	GPIO_20VT_CPIN	GPIO_20VT pin capacitance	15	–	25	pF	–40°C to +85°C T_A, All V_{DDD}, F = 1 MHz
SID.GPIO_20VT#36	GPIO_20VT_Vol	GPIO_20VT output voltage LOW level.	–	–	0.4	V	I_{OL} = 2 mA
SID.GPIO_20VT#41	GPIO_20VT_Vih_LVTTL	GPIO_20VT LVTTL input voltage HIGH level.	2	–	–	V	$V_{DDD} \geq 2.7$ V
SID.GPIO_20VT#42	GPIO_20VT_Vil_LVTTL	GPIO_20VT LVTTL input voltage LOW level.	–	–	0.8	V	$V_{DDD} \geq 2.7$ V
SID.GPIO_20VT#43	GPIO_20VT_Vhysttl	GPIO_20VT Input hysteresis LVTTL	15	40	–	mV	$V_{DDD} \geq 2.7$ V
SID.GPIO_20VT#69	GPIO_20VT_IDIODE	GPIO_20VT Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	–

Table 12 GPIO_20VT AC specifications (applicable to port pins P2.2 and P2.3 only)

(guaranteed by characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.GPIO_20VT#70	GPIO_20VT_-TriseF	GPIO_20VT Rise time in Fast Strong Mode	1	-	45	ns	All V_{DDD}, C_{load} = 25 pF
SID.GPIO_20VT#71	GPIO_20VT_T-fallF	GPIO_20VT Fall time in Fast Strong Mode	2	-	15	ns	All V_{DDD}, C_{load} = 25 pF

6.4 Digital peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

6.4.1 Pulse width modulation (PWM) for GPIO pins

Table 13 PWM AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.TCPWM.3	$T_{CPWMFREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS. Maximum = 48 MHz.
SID.TCPWM.4	$T_{PWMENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events
SID.TCPWM.5	T_{PWMEXT}	Output trigger pulse width	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	T_{CRES}	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between quadrature-phase inputs

6.4.2 I^2C

Table 14 Fixed I^2C DC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	100	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135	µA	–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	310	µA	–
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	1.4	–	µA	–

Table 15 Fixed I^2C AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

Table 16 Fixed UART DC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID160	I_{UART1}	Block current consumption at 100 kbps	–	–	20	µA	–
SID161	I_{UART2}	Block current consumption at 1000 kbps	–	–	312	µA	–

Table 17 Fixed UART AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

Table 18 Fixed SPI DC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID163	I_{SPI1}	Block current consumption at 1 Mb/s	–	–	360	µA	–
SID164	I_{SPI2}	Block current consumption at 4 Mb/s	–	–	560	µA	–
SID165	I_{SPI3}	Block current consumption at 8 Mb/s	–	–	600	µA	–

Table 19 Fixed SPI AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID166	F_{SPI}	SPI operating frequency (Master; 6X oversampling)	–	–	8	MHz	–

Table 20 Fixed SPI master mode AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID167	T_{DMO}	MOSI Valid after SClock driving edge	–	–	15	ns	–
SID168	T_{DSI}	MISO Valid before SClock capturing edge	20	–	–	ns	Full clock, late MISO sampling
SID169	T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to slave capturing edge

Table 21 Fixed SPI slave mode AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID170	T_{DMI}	MOSI Valid before Sclock capturing edge	40	–	–	ns	–
SID171	T_{DSO}	MISO Valid after Sclock driving edge	–	–	$42+3\times T_{CPU}$	ns	$T_{CPU} = 1/F_{CPU}$
SID171A	T_{DSO_EXT}	MISO Valid after Sclock driving edge in Ext Clk mode	–	–	48	ns	–
SID172	T_{HSO}	Previous MISO data hold time	0	–	–	ns	–
SID172A	$T_{SSELSCK}$	SSEL Valid to first SCK Valid edge	100	–	–	ns	–

6.5 System resources

6.5.1 Power-on reset (POR) with brown out SWD interface

Table 22 Imprecise power-on reset (PRES)

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID185	$V_{RISEIPOR}$	Power-on reset (POR) rising trip voltage	0.80	–	1.50	V	–
SID186	$V_{FALLIPOR}$	POR falling trip voltage	0.70	–	1.4	V	–

Table 23 Precise power-on reset (POR)

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID190	$V_{FALLPPOR}$	Brown-out detect (BOD) trip voltage in active/sleep modes	1.48	–	1.62	V	–
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.1	–	1.5	V	–

Table 24 SWD interface specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.SWD#1	F_SWDCLK1	3.3 V ≤ VDDD ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#2	F_SWDCLK2	2.7 V ≤ VDDD ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#3	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID.SWD#4	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID.SWD#5	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.50 × T	ns	–
SID.SWD#6	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	–

6.5.2 Internal main oscillator

Table 25 IMO DC specifications

(guaranteed by design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000	µA	–

Table 26 IMO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 24, 36, and 48 MHz (trimmed)	–	–	±2	%	–
SID226	$T_{STARTIMO}$	IMO start-up time	–	–	7	µs	Guaranteed by characterization.
SID228	$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	Guaranteed by characterization.
SID.CLK#1	F_{IMO}	IMO frequency	24	36	48	MHz	Only 3 frequencies supported: 24 MHz, 36 MHz, and 48 MHz.

6.5.3 Internal low-speed oscillator power down

Table 27 ILO DC specifications

(guaranteed by design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID231	I_{ILO1}	I_{LO} operating current	–	0.3	1.05	µA	–
SID233	$I_{ILOLEAK}$	I_{LO} leakage current	–	2	15	nA	–

Table 28 ILO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID234	$T_{STARTILO1}$	I_{LO} start-up time	–	–	2	ms	Guaranteed by characterization
SID238	$T_{ILODUTY}$	I_{LO} duty cycle	40	50	60	%	Guaranteed by characterization
SID.CLK#5	F_{ILO}	I_{LO} frequency	20	40	80	kHz	–

Table 29 PD DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.PD.4	R_D	UFP CC termination	4.59	5.1	5.61	kΩ	–
SID.PD.5	R_{D_DB}	UFP (Power Bank) Dead Battery CC Termination on CC1 and CC2	4.08	5.1	6.12	kΩ	All supplies forced to 0V and 1.32 V applied at CC1 or CC2
SID.PD.6	$V_{gndoffset}$	Ground offset tolerated by BMC receiver	–500	–	500	mV	Relative to the remote BMC transmitter.

Table 30 UV/OV specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID.UVOV.1	V_{THOV1}	Overvoltage threshold accuracy, 4.0 V to 11.0 V	–3	–	3	%	Active mode
SID.UVOV.2	V_{THOV2}	Overvoltage threshold accuracy, 11 V to 27.4 V	–3.2	–	3.2	%	
SID.UVOV.3	V_{THUV1}	Undervoltage threshold accuracy, 2.7 V to 3.3 V	-4	–	4	%	
SID.UVOV.4	V_{THUV2}	Undervoltage threshold accuracy, 3.3 V to 4.0 V	–3.5	–	3.5	%	
SID.UVOV.5	V_{THUV3}	Undervoltage threshold accuracy, 4.0 V to 11.0 V	–3	–	3	%	
SID.UVOV.6	V_{THUV4}	Undervoltage threshold accuracy, 11.0 V to 22.0 V	–2.9	–	2.9	%	

Table 31 UV/OV AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.UVOV.AC.1	T_{OV_GPIO}	Delay from OV threshold trip to output GPIO toggle	–	–	20	µs	Available on P1.0 or P1.1
SID.UVOV.AC.2	T_{OV_GATE}	Delay from OV threshold trip to external PFET power gate turn off	–	–	50	µs	–
SID.UVOV.AC.3	T_{UV_GPIO}	Delay from UV threshold trip to output GPIO toggle	–	–	20	µs	Available on P1.0 or P1.1

Table 32 LS-CSA specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.LSCSA.1	Cin_inp	CSP input capacitance	7	–	10	pF	Guaranteed by characterization
SID.LSCSA.2	Csa_Acc1	CSA accuracy 5 mV < Vsense < 10 mV	–15	–	15	%	Active mode
SID.LSCSA.3	Csa_Acc2	CSA accuracy 10 mV < Vsense < 15 mV	–10	–	10	%	
SID.LSCSA.4	Csa_Acc3	CSA accuracy 15 mV < Vsense < 20 mV	–6	–	6	%	
SID.LSCSA.5	Csa_Acc4	CSA accuracy 20 mV < Vsense < 30 mV	–5	–	5	%	
SID.LSCSA.6	Csa_Acc5	CSA accuracy 30 mV < Vsense < 50 mV	–4	–	4	%	
SID.LSCSA.7	Csa_Acc6	CSA accuracy 50 mV < Vsense	–4	–	4	%	
SID.LSCSA.8	Csa_SCP_ Acc1	CSA SCP 80 mV	– 16.5	–	30	%	

Table 32 LS-CSA specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.LSCSA.9	Csa_SCP_Acc2	CSA SCP 100 mV	–13.4	–	24	%	Active mode
SID.LSCSA.10	Csa_SCP_Acc3	CSA SCP 150 mV	–9.4	–	16	%	
SID.LSCSA.11	Csa_SCP_Acc4	CSA SCP 200 mV	–7.5	–	12	%	
SID.LSCSA.12	Av	Nominal gain values supported: 5, 10, 20, 35, 50, 75, 125, 150	5	–	150	V/V	–
SID.LSCSA.24	Av1_E_Trim	Gain Error	–3	–	3	%	Guaranteed by characterization
SID.LSCSA.31	Av_E_SCP	Gain Error of SCP stage	–3.5	–	3.5	%	Guaranteed by characterization

Table 33 LS-CSA AC specifications
(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.LSCSA.AC.1	T_{OCP_GPIO}	Delay from OCP threshold trip to output GPIO toggle	–	–	20	µs	Available on P1.0 or P1.1
SID.LSCSA.AC.2	T_{OCP_Gate}	Delay from OCP threshold trip to external PFET power gate turn off	–	–	50	µs	–
SID.LSCSA.AC.3	T_{SCP_GPIO}	Delay from SCP threshold trip to output GPIO toggle	–	–	15	µs	Available on P1.0 or P1.1
SID.LSCSA.AC.4	T_{SCP_Gate}	Delay from SCP threshold trip to external PFET power gate turn off	–	–	50	µs	–
SID.LSCSA.AC.5	T_{SR_GPIO}	Delay from SR threshold trip to output GPIO toggle	–	–	20	µs	Available on P1.0 or P1.1

6.5.4 Gate driver specifications

Table 34 Gate driver DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.GD.1	R_{PD}	Pull-down resistance	–	–	3	kΩ	Applicable on VBUS_FET_CTRL_0 and VBUS_FET_CTRL_1 to turn ON external PFET.
SID.GD.2	R_{PU}	Pull-up resistance	–	–	4	kΩ	Applicable on VBUS_FET_CTRL_0 to turn OFF external PFET
SID.GD.3	I_{PD0}	Pull-down current sink at drive strength of 1	25	–	75	µA	I-mode (current mode) pull down at 5 V. Applicable on VBUS_FET_CTRL_0 and VBUS_FET_CTRL_1 to turn ON external PFET
SID.GD.4	I_{PD1}	Pull-down current sink at drive strength of 2	50	–	150	µA	
SID.GD.5	I_{PD2}	Pull-down current sink at drive strength of 4	140	–	300	µA	
SID.GD.6	I_{PD3}	Pull-down current sink at drive strength of 8	280	–	580	µA	
SID.GD.7	I_{PD4}	Pull-down current sink at drive strength of 16	560	–	1200	µA	
SID.GD.8	I_{PD5}	Pull-down current sink at drive strength of 32	1120	–	2300	µA	
SID.GD.9	I_leak_p1	Pin leakage on VBUS_FET_CTRL_0	–	0.003	–	µA	+25°C T_J, 5-V V_{DDD}, 20-V V_{BUS}
SID.GD.10	I_leak_c1	Pin leakage on VBUS_FET_CTRL_1	–	0.003	–	µA	+25°C T_J, 5-V V_{DDD}, 20-V V_{BU}
SID.GD.11	I_leak_p2	Pin leakage on VBUS_FET_CTRL_0	–	–	2	µA	+85°C T_J, 5-V V_{DDD}, 20-V V_{BU}
SID.GD.12	I_leak_c2	Pin leakage on VBUS_FET_CTRL_1	–	–	2	µA	+85°C T_J, 5-V V_{DDD}, 20-V V_{BU}
SID.GD.13	I_leak_p3	Pin leakage on VBUS_FET_CTRL_0	–	–	7	µA	+125°C T_J, 5-V V_{DDD}, 20-V V_{BU}
SID.GD.14	I_leak_c3	Pin leakage on VBUS_FET_CTRL_1	–	–	7	µA	+125°C T_J, 5-V V_{DDD}, 20-V V_{BU}

Table 35 Gate driver AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.GD.15	T_{PD1}	Pull down delay on VBUS_FET_CTRL_1	–	–	2	µs	Cload = 2 nF, Delay to VBUS –1.5 V from initiation of falling edge, VBUS = 5 V to 20 V, 50 KΩ tied between VBUS_FET_CTRL_1 and VBUS
SID.GD.16	$T_{r_discharge}$	Discharge rate of output node on VBUS_FET_CTRL_1	–	–	5	V/µs	80% to 20%, 50 KΩ tied between VBUS_FET_CTRL_1 and VBUS, Cload = 2 nF, Vinitial = 24 V
SID.GD.17	T_{PD2}	Pull down delay on VBUS_FET_CTRL_0	–	–	2	µs	Cload = 2 nF, Delay to VBUS –1.5 V from initiation of falling edge, V_{BUS} = 5 V to 20 V, 50 KΩ tied between VBUS_FET_CTRL_0 and VBUS
SID.GD.18	T_{PU}	Pull up delay on VBUS_FET_CTRL_0	–	–	18	µs	Cload = 2 nF, Delay to VBUS–1.5 V from initiation of falling edge, VBUS = 5 V to 20 V, 50 KΩ tied between VBUS_FET_CTRL_0 and VBUS
SID.GD.19	SR_{PU}	Output slew rate on VBUS_FET_CTRL_0	–	–	5	V/µs	Cload = 2 nF, 20% to 80% of VBUS_FET_CTRL_0 range
SID.GD.20	SR_{PD}	Output slew rate on VBUS_FET_CTRL_0	–	–	5	V/µs	Cload = 2 nF, 80% to 20% of VBUS_FET_CTRL_0 range

Table 36 VBUS discharge specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / conditions
SID.VBUS.DISC.6	I1	20-V NMOS ON current for DS = 1	0.15	–	1	mA	Measured at 0.5 V
SID.VBUS.DISC.7	I2	20-V NMOS ON current for DS = 2	0.4	–	2	mA	
SID.VBUS.DISC.8	I4	20-V NMOS ON current for DS = 4	0.9	–	4	mA	
SID.VBUS.DISC.9	I8	20-V NMOS ON current for DS = 8	2	–	8	mA	
SID.VBUS.DISC.10	I16	20-V NMOS ON current for DS = 16	4	–	10	mA	
SID.VBUS.DISC.11	VBUS_Stop_Error	Error percentage of final V_{BUS} value from setting	–	–	10	%	When V_{BUS} is discharged to 5 V. Guaranteed by characterization.

Table 37 VBUS short protection specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID.VSP.1	V_SHORT_TRIGGER	Short-to-VBUS system-side clamping voltage on the CC/P2.2/P2.3 pins	–	9	–	V	Guaranteed by characterization.

Table 38 VBUS DC regulator specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.VREG.2	VBUS_DETECT	VBUS detect threshold voltage	1.08	–	2.62	V	–

Table 39 VBUS AC regulator specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.VREG.3	T_{start}	Total startup time for the regulator supply outputs	–	–	200	µs	Guaranteed by characterization.

6.5.5 ADC

Table 40 ADC DC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	–2.5	–	2.5	LSB	Reference voltage generated from VDDD
SID.ADC.2A	INL	Integral non-linearity	–1.5	–	1.5	LSB	Reference voltage generated from bandgap
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5	LSB	Reference voltage generated from VDDD
SID.ADC.3A	DNL	Differential non-linearity	–1.5	–	1.5	LSB	Reference voltage generated from bandgap
SID.ADC.4	Gain Error	Gain error	–1.5	–	1.5	LSB	–
SID.ADC.6	V_{REF_ADC2}	ADC reference voltage when generated from band gap.	1.96	2.0	2.04	V	Reference voltage generated from bandgap

Table 41 ADC AC specifications

(guaranteed by design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.ADC.7	SLEW_Max	Rate of change of sampled voltage signal	–	–	3	V/ms	–

6.5.6 Memory

Table 42 Flash AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID.MEM#3	FLASH_ERASE	Row erase time	–	–	15.5	ms	–40°C ≤ T_A ≤ 85°C, all V_{DDD}
SID.MEM#4	FLASH_WRITE	Row (Block) write time (erase and program)	–	–	20	ms	–40°C ≤ T_A ≤ 85°C, all V_{DDD}
SID.MEM#8	FLASH_ROW_PGM	Row program time after erase	–	–	7	ms	25°C ≤ T_A ≤ 55°C, all V_{DDD}
SID178	$T_{BULKERASE}$	Bulk erase time (32 KB)	–	–	35	ms	–
SID180	$T_{DEVPROG}$	Total device program time	–	–	7.5	s	–
SID182	F_{RET1}	Flash retention, T_A ≤ 55°C, 100K P/E cycles	20	–	–	years	–
SID182A	F_{RET2}	Flash retention, T_A ≤ 85°C, 10K P/E cycles	10	–	–	years	–
SID182B	F_{RET3}	Flash retention, T_A ≤ 105°C, 10K P/E cycles	3	–	–	years	–

7 Ordering information

Table 43 lists the EZ-PD™ PMG1-S0 part numbers and features.

Table 43 EZ-PD™ PMG1-S0 ordering information

MPN	Application	Type-C ports	Termination resistor	Role	Package type	Si ID
CYPM1011-24LQXI CYPM1011-24LQXIT	Power sink applications	1	R_D, $R_{D\text{-}DB}$	UFP	24-pin QFN	0x2020

7.1 Ordering code definitions

The part numbers are of the form CYPM1ABC-DEFGHIJ, where the fields are defined as shown in Table 44.

Table 44 EZ-PD™ PMG1-S0 ordering code definitions

Field	Description	Values	Meaning
CY	Infineon prefix	CY	Company ID
PM	Marketing code	PM	PM = Power Delivery MCU family
1	MCU Family generation	1	Product Family Generation
A	Family	0	S0
		1	S1
		2	S2
		3	S3
B	PD ports	1	1-PD port
		2	2-PD port
C	Application specific	X	Application specific
DE	Pin	XX	Number of pins in the package
FG	Package code	LQ	QFN
		BZ	BGA
		FN	CSP
H	Lead free	X	Lead: X = Pb-free
I	Temperature range	I	Industrial
J	Only for T&R	T	Tape and reel

8 Packaging

Table 45 Package characteristics

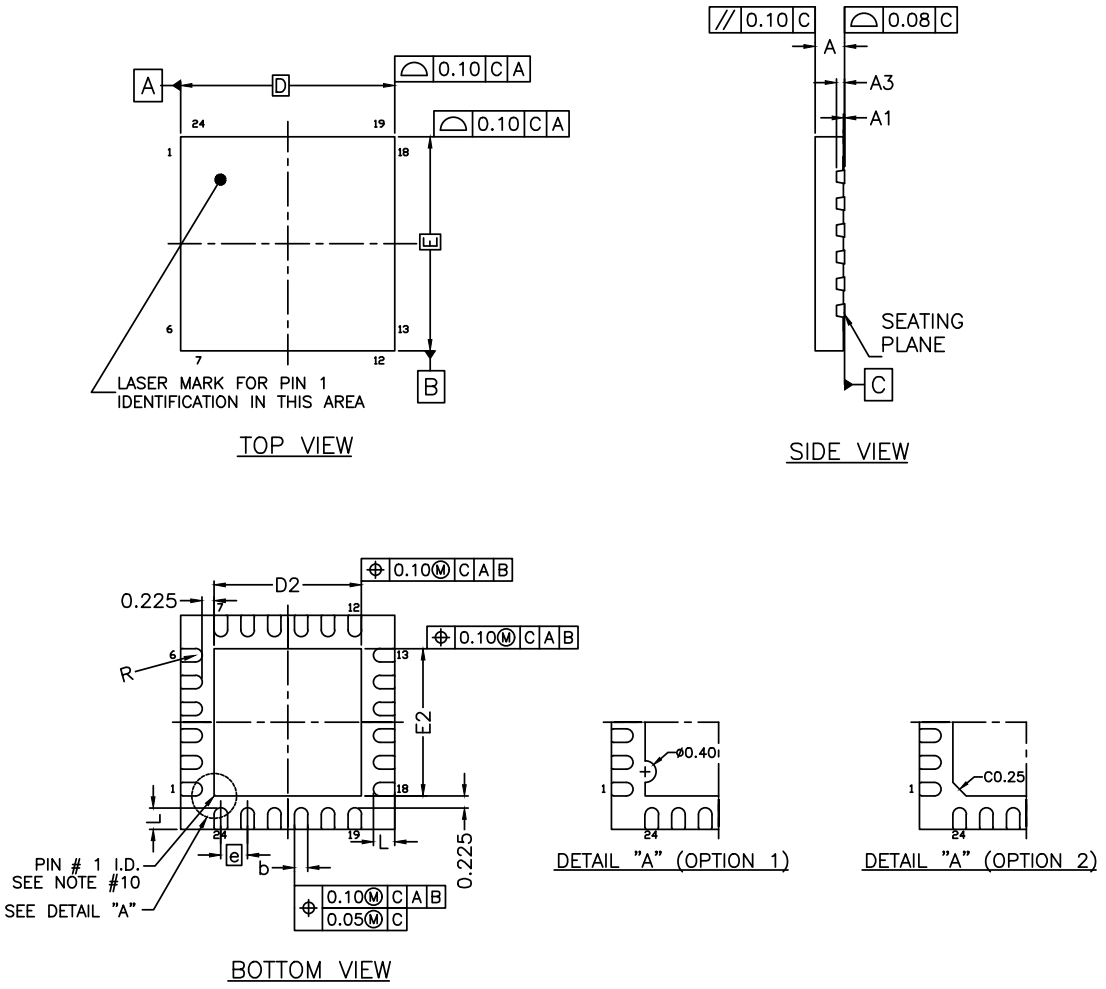
Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	Extended Industrial	-40	25	105	°C
T_J	Operating junction temperature	Extended Industrial	-40	25	120	°C
T_{JA}	Package θ_{JA} (24-QFN)	–	–	–	19.98	°C/W
T_{JC}	Package θ_{JC} (24-QFN)	–	–	–	4.78	°C/W

Table 46 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time within 5°C of peak temperature
24-pin QFN	260°C	30 seconds

Table 47 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
24-pin QFN	MSL3



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	0.60
A1	0.00	—	0.05
A3 (Option 1)	0.152 REF		
A3 (Option 2)	0.127 REF		
b	0.18	0.25	0.30
D	4.00 BSC		
D2	2.65	2.75	2.85
E	4.00 BSC		
E2	2.65	2.75	2.85
L	0.30	0.40	0.50
e	0.50 BSC		
R	0.09	—	—

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. PACKAGE WARPAGE MAX 0.08 mm.
7. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY TO TERMINALS.
9. JEDEC SPECIFICATION NO. REF: N.A.
10. INDEX FEATURE CAN EITHER BE AN OPTION 1 : "MOUSE BITE" OR OPTION 2 : CHAMFER.

002-16934 *E

Figure 6 24-pin QFN package outline

9 Acronyms

Table 48 Acronyms used in this document

Acronym	Description
ADC	analog-to-digital converter
AES	advanced encryption standard
API	application programming interface
Arm®	advanced RISC machine, a CPU architecture
CC	configuration channel
CPU	central processing unit
CS	current sense
CSA	current sense amplifier
CRC	cyclic redundancy check, an error-checking protocol
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role port
EEPROM	electrically erasable programmable read-only memory
EMCA	electronically marked cable assembly, a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FS	full-speed
GPIO	general-purpose input/output
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO
LDO	low-dropout regulator
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller
OCP	over current protection
opamp	operational amplifier
OTP	over temperature protection
OVP	overvoltage protection
OVT	overvoltage tolerant

Table 48 Acronyms used in this document *(continued)*

Acronym	Description
PCB	printed circuit board
PD	power delivery
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PRNG	pseudo random number generation
PWM	pulse-width modulator
RAM	random-access memory
RCP	reverse current protection, supported in Source Configuration only
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCB	serial communication block
SCL	I^2C serial clock
SCP	short circuit protection, supported in Source Configuration only
SDA	I^2C serial data
S/H	sample and hold
SHA	secure hash algorithm
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TCPWM	timer counter pulse-width modulator
TRNG	true random number generation
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USBIO	USB input/output, PMG1-S0 pins used to connect to a USB port
UVP	undervoltage protection
XRES	external reset I/O pin

10 Document conventions

10.1 Units of measure

Table 49 Units of measure

Symbol	Unit of measure
°C	degrees celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kiloohm
Mbps	megabits per second
MHz	megahertz
MΩ	megaohm
Msps	mega samples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Revision history

Document revision	Date	Description of changes
**	2020-10-23	New datasheet.
*A	2021-02-24	Updated **Figure 1** and **Figure 2**. Updated **Table 1** with latest values for GPIO, TCPWM, and SCB counts for PMG1-S3. Added note in **Figure 1** and **Table 1**. Added links in **Development support**. Updated **Application diagram**. Changed D+/D- pin names to USBDP/USBDM. Added Notes 7, 8, and 10 in **Electrical specifications**. Updated **Acronyms**. Updated Copyright year.
*B	2021-05-27	Updated **Table 3**. Changed datasheet status from preliminary to final.
*C	2022-05-18	Added **Pin based absolute maximum ratings**. Updated **Figure 6**. Migrated to IFX template.
*D	2022-07-21	Updated MOSFET gate drivers for EZ-PD™ PMG1-S0 in **Table 1** Addition of CSP pin for current measurement: • Updated **Figure 1**, **Block diagram**, **Figure 4**, and **Figure 5** • Updated **Table 1**, **Table 3**, **Table 6**, **Table 48**, and **Table 49** • Added **Table 32** and **Table 33**. • Added section **“Low-side current sense amplifier (CSA)”** on page 11

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