THE DATASHEET OF

A1445EEWLT-P

A1444 and A1445

Low-Voltage Full-Bridge Brushless DC Motor Driver with Hall Commutation, Externally Controlled Speed Regulation, Soft Switching, and Reverse Battery, Short Circuit, and Thermal Shutdown Protection

Last Time Buy

These parts are in production but have been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available.

Date of status change: November 1. 2010

Deadline for receipt of LAST TIME BUY orders: April 30, 2011

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, refer to the A1442 and A1448.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

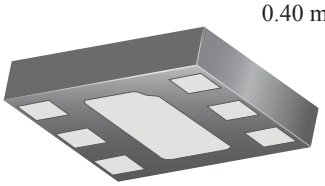
A1444 and A1445

Low-Voltage Full-Bridge Brushless DC Motor Driver with Hall Commutation, Externally Controlled Speed Regulation, Soft Switching, and Reverse Battery, Short Circuit, and Thermal Shutdown Protection

Features and Benefits

- Low voltage operation: 1.8 to 4.2 V
- Externally controlled motor speed regulation
- Fast motor startup and braking function allows faster start-stop cycles
- Reverse voltage protection on the VDD and $\overline{\text{SLEEP}}$ pins
- Output short circuit and thermal shutdown protection
- Soft switching algorithm for reduced audible switching noise and EMI interference
- Unidirectional operating mode results in motor rotation in only one direction
- Chopper stabilization reduces Hall signal offset drifts and results in increased signal accuracy over full operating temperature range
- Sleep mode pin allows device enable/disable for reducing average power consumption
- Antistall feature guarantees continuous rotation
- Single-chip solution for high reliability
- Miniature MLP/DFN package

Package:



6-contact MLP/DFN
1.5 mm × 2 mm.
0.40 mm maximum overall height
(EW package)

Approximate size

Description

The A1444 and A1445 are full-bridge motor drivers designed to drive low-voltage brushless DC (BLDC) motors in applications that require rotor speed control and fast rotor start-stop cycles. A high density CMOS semiconductor process allows the integration of a Hall element, a full-bridge output driver, and PWM speed control logic into one monolithic IC. Commutation of the motor is achieved by use of a single Hall element to detect the rotational position of an alternating-pole ring magnet. Low-voltage design techniques have been employed to achieve full device functionality down to a V_{DD} of 1.8 V. The voltage applied to the PDC pin is used to externally control the maximum speed of the motor by adjusting the PWM duty cycle of the output driver.

The A1444 and A1445 employ a soft switching algorithm to reduce audible switching noise and EMI interference. The externally controlled speed regulation and braking functions can be used to create motor designs requiring faster start-stop cycles. The A1444 and A1445 have different selectable internal PWM duty cycle options to accommodate a wide range of motor designs. Each device has a braking function enable pin that also includes a micropower sleep mode for battery management in portable electronic devices. This feature eliminates the requirement for a FET transistor to switch the device on and off.

The devices are optimized for vibration motor applications that require fast start-stop cycles, such as in cellular phones,

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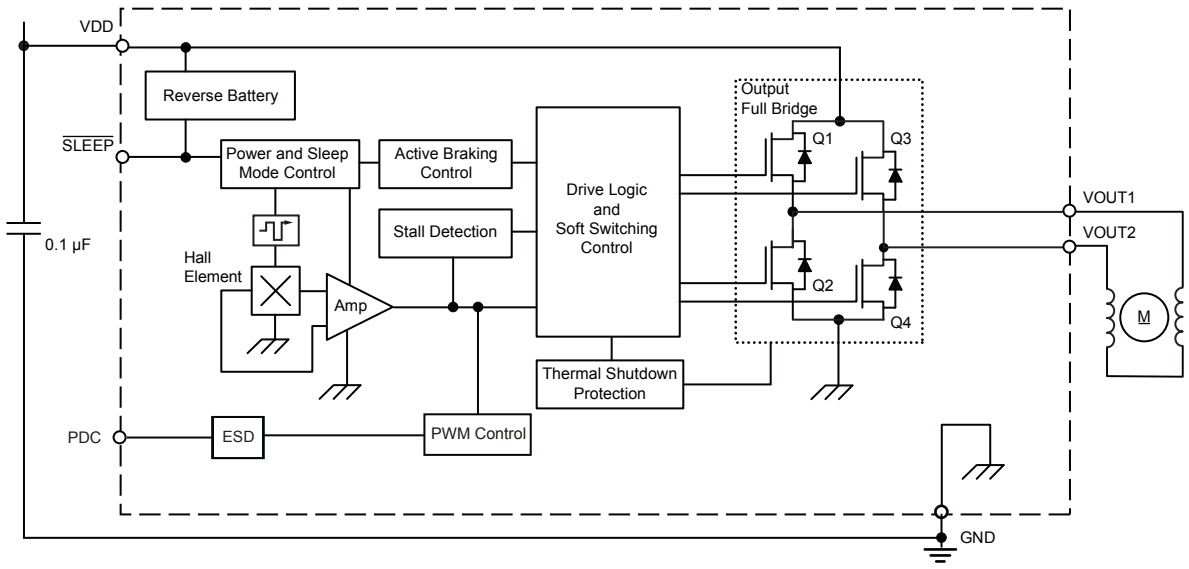
Functional Block Diagram



Description (continued)

pagers, and hand-held video game controllers. The devices can also be used for low-power fan motors rated at 5 V. This fully integrated single-chip solution provides enhanced reliability, including reverse battery protection and output short circuit protection.

The small package outline and low profile make this device ideally suited for use in applications where printed circuit board area and component headroom are at a premium. It is available in a lead (Pb) free (leadframe plating nickel palladium) 6-contact MLP/DFN microleadframe package for surface mount assembly. The underside of the package also features an exposed pad for enhanced thermal dissipation.

Selection Guide

Part Number	Packing[1]	Package
~~A1444EEWLT-P[2]~~	3000 pieces per 7-in. reel	1.5 mm × 2 mm , 0.38 mm nominal overall package height, 6-contact MLP/DFN with exposed thermal pad
~~A1445EEWLT-P[2]~~		

[1]Contact Allegro for additional packing options

[2]Variant is in production but has been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change: May 4, 2009.

Absolute Maximum Ratings

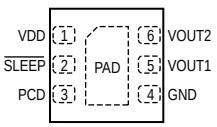
Characteristic	Symbol	Notes	Rating	Units
Forward Supply Voltage	V_{DD}		5.0	V
Reverse Supply Voltage	V_{RDD}		–5.0	V
Forward Output Voltage	V_{OUT}	V_{DD} > 0 V	0 to V_{DD} + 0.3	V
Reverse Output Voltage	V_{ROUT}	V_{DD} > 0 V	–0.3	V
$\overline{\text{SLEEP}}$ Input Voltage	V_{IN}		0 to V_{DD} + 0.3	V
$\overline{\text{SLEEP}}$ Reverse Input Voltage	V_{RIN}		–5.0	V
PDC Input Voltage	V_{PDC}		–0.3 to V_{DD} + 0.3	V
Continuous Output Current	I_{OUT}	Positive I_{LOAD} flow is from VOUT1 to VOUT2, T_J < T_J(max)	±250	mA
Peak Output Current	$I_{OUT(pk)}$	<1 ms	±500	mA
Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

Thermal Characteristics may require derating at maximum conditions, see Power Derating section

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	On 2-layer PCB, with 0.23 in.^{2} copper area each side	125	°C/W
		On 4-layer PCB based on JEDEC standard	64	°C/W

*Additional thermal information available on the Allegro website

Pin-out Diagram



Terminal List

Number	Name	Function
1	VDD	Supply voltage
2	$\overline{\text{SLEEP}}$	Toggles sleep and enable modes, low sleep mode voltage initiates motor braking and low power mode
3	PDC	Voltage on this pin selects among discrete internal PWM duty cycle values to control motor speed
4	GND	Ground
5	VOUT1	First output
6	VOUT2	Second output

ELECTRICAL CHARACTERISTICS Valid over supply voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.[1]	Max.	Unit
Supply Voltage	V_{DD}	$T_J < T_J$(max)		2.0	–	4.2	V
Extended Supply Voltage[2]	V_{DDE}	$T_J < T_J$(max)		1.8	–	4.2	V
Supply Current	$I_{DD(ON)}$	$V_{IN} > V_{INHI}$, T_A = 25°C, no load		–	4	6	mA
		$V_{IN} < V_{INLO}$, T_A = 25°C		–	–	10	µA
Total Output On-Resistance[3]	$R_{DS(on)}$	I_{OUT} = 50 mA, V_{DD} = 2 V, T_A = 25°C		–	3.9	–	Ω
		I_{OUT} = 50 mA, V_{DD} = 3 V, T_A = 25°C		–	2.6	–	Ω
		I_{OUT} = 50 mA, V_{DD} = 4 V, T_A = 25°C		–	2.2	–	Ω
Reverse Battery Current	I_{RDD}	V_{RDD} = –4.2 V, current flowing out of VDD pin, T_A = 25°C		–	–	–10	mA
$\overline{\text{SLEEP}}$ Input Threshold	V_{INHI}			0.7 × V_{DD}	–	–	V
	V_{INLO}			–	–	0.2 × V_{DD}	V
$\overline{\text{SLEEP}}$ Input Current	I_{IN}	V_{DD} = 3.6 V		–	1.0	5	µA
$\overline{\text{SLEEP}}$ Reverse Input Current	I_{RIN}	V_{RIN} = –4.2 V, current flowing out of $\overline{\text{SLEEP}}$ pin, T_A = 25°C		–	–	–10	mA
Restart Delay[4]	t_{RS}	V_{DD} = 3.6 V		–	100	–	ms
Hall Chopping Settling Time[5]	$t_{S(CHOP)}$			–	160	–	µs
Thermal Shutdown Limit	T_{JTSD}	Device is active		–	165	–	°C
Thermal Shutdown Hysteresis	$T_{JTSD(HYS)}$	Device is active		–	20	–	°C
Internal PWM Frequency	f_{PWM}			–	40	–	kHz
PDC High Level Threshold	V_{PDCH}	PDC input going from low to high state		V_{DD}–0.5	–	V_{DD}	V
PDC Low Level Threshold	V_{PDCL}	PDC input going from high to low state		0	–	0.5	V
PDC Input Current[6]	I_{PDCH}	Steady state condition, PDC pin high		–	–	30	µA
	I_{PDCL}	Steady state condition, PDC pin low state		–30	–	–	µA
Internal PWM Duty Cycle	DC_{PWM}	A1444	$V_{PDC} < V_{PDCL}$, $V_{DD} = V_{DDN}$, $S_{ROT} > S_{ROT(th)}$	–	56	–	%
			PDC Pin Floating, $V_{DD} = V_{DDN}$, $S_{ROT} > S_{ROT(th)}$	–	62	–	%
			$V_{PDC} > V_{PDCH}$, $V_{DD} = V_{DDN}$, $S_{ROT} > S_{ROT(th)}$	–	68	–	%
		A1445	$V_{PDC} < V_{PDCL}$, $V_{DD} = V_{DDN}$, $S_{ROT} > S_{ROT(th)}$	–	71	–	%
			PDC Pin Floating, $V_{DD} = V_{DDN}$, $S_{ROT} > S_{ROT(th)}$	–	80	–	%
			$V_{PDC} > V_{PDCH}$, $V_{DD} = V_{DDN}$, $S_{ROT} > S_{ROT(th)}$	–	89	–	%

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ELECTRICAL CHARACTERISTICS (continued) valid over supply voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
Magnetic Switchpoints	B_{OP}	2 V ≤ V_{DD} ≤ 4 V	–	35	75	G
	B_{RP}	2 V ≤ V_{DD} ≤ 4 V	–75	–35	–	G
	B_{HYS}	2 V ≤ V_{DD} ≤ 4 V	–	70	–	G
Output Polarity	VOUT1	B < B_{RP}	–	LOW	–	V
		B > B_{OP}	–	HIGH	–	V
	VOUT2	B < B_{RP}	–	HIGH	–	V
		B > B_{OP}	–	LOW	–	V

[1]Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions, such as T_A = 25°C. Performance may vary for individual units, within the specified maximum and minimum limits.
[2]Device operates with lower supply voltages, down to 1.8 V, with slight variation in specification of magnetic switchpoints and Total Output On-Resistance.
[3]Total Output On-Resistance = $R_{DS(on)Q1}$ + $R_{DS(on)Q4}$, or $R_{DS(on)Q2}$ + $R_{DS(on)Q3}$, where Qx refers to the internal full-bridge transistors.
[4]Restart Delay is the duration required from power-up of the device to valid device output.
[5]Hall Chopping Settling Time is the delay from power-on of the device to the initial valid device output.
[6]Positive current is defined as flowing into the device.

Functional Description

Soft Switching

The A1444 and A1445 devices include a soft switching algorithm that controls the output switching slew rate for both output pins. As a result, the devices are ideal for use in applications requiring low audible switching noise and low EMI interference.

Braking and Sleep Mode

The $\overline{\text{SLEEP}}$ pin accepts an external signal that enables braking and a sleep mode. During braking, the device reverses the polarity of the output bridge for a fixed time period, then the device enters sleep mode. In sleep mode, the device current consumption gets reduced to an extremely low level, conserving battery power.

Antistall Algorithm

If a stall condition occurs, the device will execute an antistall algorithm to restart the motor.

Device Start-up

The start-up behavior of the device output is determined by the applied magnetic field, as specified in the Electrical Characteristics table.

Speed Control

When the rate of rotation exceeds the specified threshold, $S_{ROT(th)}$, the A1444/A1445 output bridge becomes controlled by an internally generated PWM signal. The duty cycle of the internal PWM signal regulates the maximum motor rpm. The PWM duty cycle, however, is user-selectable through the state of the PDC pin. The PWM duty cycle options are given in the Electrical Characteristics table.

Application Information

Two typical application circuits are shown in figures 1 and 2. The application circuit in figure 1 shows the device $\overline{\text{SLEEP}}$ pin controlled by the user. In this case, the device is powered continuously and the average supply current would switch between low and high values depending on the state of the $\overline{\text{SLEEP}}$ pin.

Figure 2 illustrates an applications circuit where the device supply pin and $\overline{\text{SLEEP}}$ pin are connected together. When power is applied to the device, it enters enable mode and operates with high average supply current.

Note that:

- No external diode is required for reverse battery protection because the protection is fully integrated into the IC.
- Thermal shutdown also is integrated to protect the device against inadvertent output shorts during manufacturing or testing.
- In these figures, the PDC pin is tied to GND. Alternatively, the PDC pin could be tied to any of the voltage rails or left floating, which will determine the internal PWM duty cycle as specified in the Electrical Characteristics table.

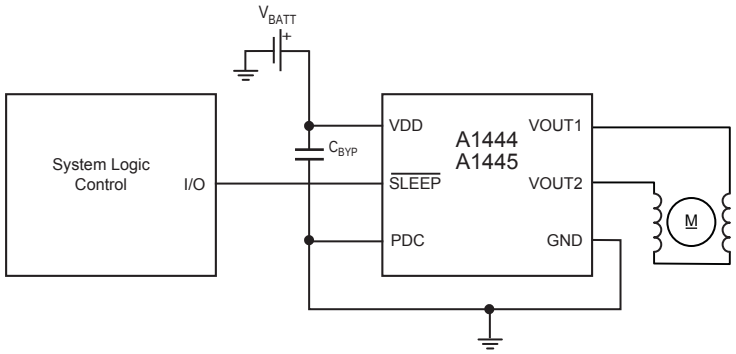


Figure 1. Application circuit showing user-controlled sleep/enable mode, while the A144x remains powered at all times

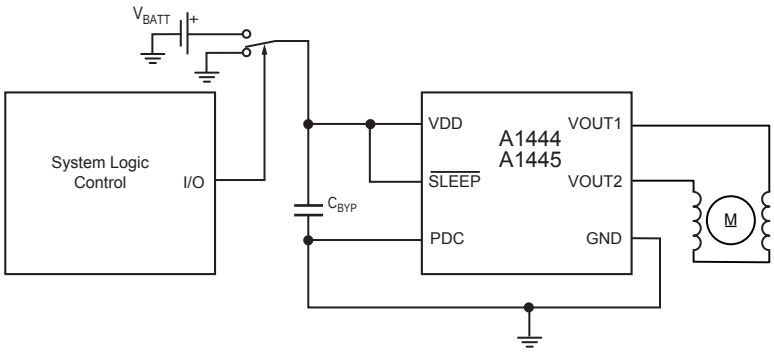


Figure 2. Application circuit showing simultaneous user control of power supply and sleep mode.

Power Derating

The device must be operated below the maximum junction temperature of the device, T_J (max). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The package thermal resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the effective thermal conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at various P_D levels.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For a load of 30 Ω, and given common conditions such as: T_A= 25°C, V_{DD} = 3 V, I_{DD} = 85 mA, V_{LOAD} = 2.43 V, I_{LOAD} = 83 mA, and $R_{\theta JA}$ = 250 °C/W,

then:

$$P_D = V_{DD} \times I_{DD} - V_{LOAD} \times I_{LOAD}$$

$$= 3\ V \times 83\ mA - 2.43\ V \times 81\ mA$$

$$= 52.17\ mW$$

$$\Delta T = P_D \times R_{\theta JA}$$

$$= 52.17\ mW \times 250\ °C/W$$

$$= 13°C$$

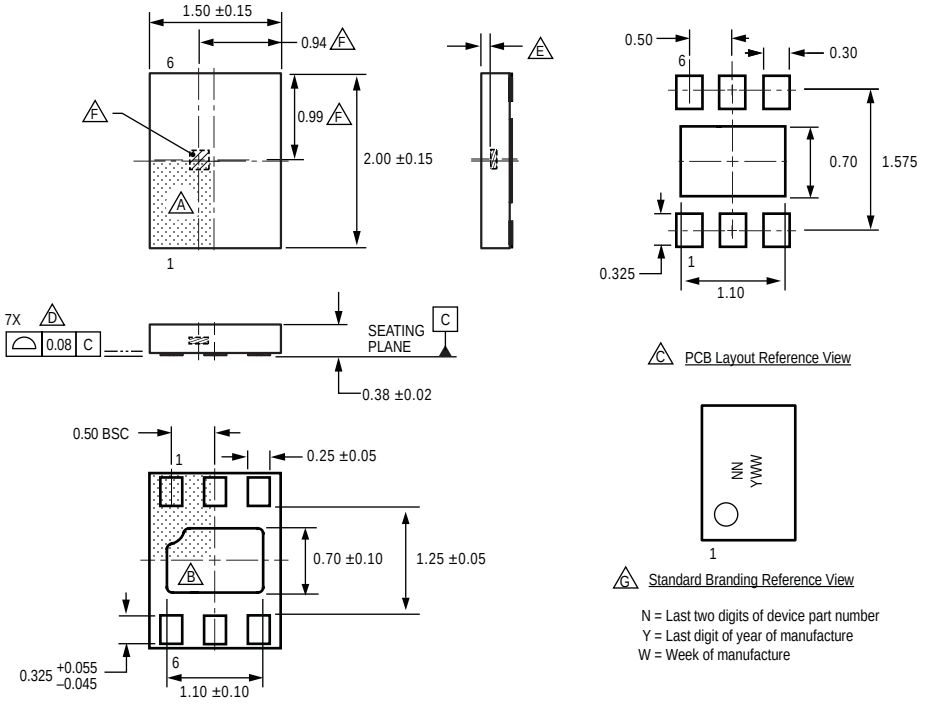
$$T_J = T_A + \Delta T$$

$$= 25°C + 13°C$$

$$= 38°C$$

A worst-case estimate, P_D(max), represents the maximum allowable power level, without exceeding T_J(max), at a selected $R_{\theta JA}$ and T_A.

Package EW, 6 pin MLP/DFN



For Reference Only, not for tooling use (refernce DWG-2856; similar to JEDEC Type 1, MO-229X2BCD)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P200X200X100-9M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Active Area Depth 0.15 mm REF

F Hall Element (not to scale)

G Branding scale and appearance at supplier discretion

The products described herein are manufactured under one or more of the following U.S. patents: 5,045,920; 5,264,783; 5,442,283; 5,389,889; 5,581,179; 5,517,112; 5,619,137; 5,621,319; 5,650,719; 5,686,894; 5,694,038; 5,729,130; 5,917,320; and other patents pending.

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