THE DATASHEET OF

APEK8650KLY-01-MH-DK

Low Input Voltage, Adjustable Frequency 2 A Synchronous Buck Regulator with EN/SYNC and Power OK

FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- Operating voltage range: 2.5 to 5.5 V
- UVLO stop threshold: 2.25 V (max)
- Adjustable switching frequency (f_{OSC}): 0.25 to 2.45 MHz
- Synchronizes to external clock: 1.2× to 1.5× f_{OSC} (typ)
- Internal 70 mΩ high-side switching MOSFET
- Internal 55 mΩ low-side switching MOSFET
- Capable of at least 2.0 A steady-state output current
- Sleep mode supply current less than 3 µA
- Adjustable output voltage as low as 0.8 V with ±1% accuracy from –40°C to 125°C
- Soft start time externally set via the SS pin
- Pre-biased startup capable
- Externally adjustable compensation

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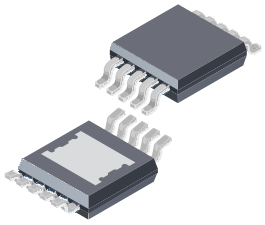
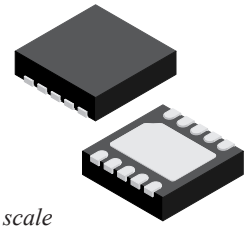
PACKAGES:

10-pin MSOP with exposed thermal pad (suffix LY)



10-pin DFN with exposed thermal pad (suffix EJ)



Not to scale

DESCRIPTION

The A8650 is an adjustable frequency, high output current, PWM regulator that integrates a high-side P-channel MOSFET and a low-side N-channel MOSFET. The A8650 incorporates current-mode control to provide simple compensation, excellent loop stability, and fast transient response. The A8650 uses external compensation to accommodate a wide range of power components to optimize transient response without sacrificing stability. The A8650 regulates input voltages from 2.5 to 5.5 V, down to output voltages as low as 0.8 V, and is able to supply at least 2.0 A of load current.

The A8650 features include an externally adjustable switching frequency, an externally set soft start time to minimize inrush currents, an EN/SYNC input to either enable V_{OUT} and/or synchronize the PWM switching frequency, and a Power OK (POK) output to indicate when V_{OUT} is within regulation. The sleep mode current of the A8650 control circuitry is less than 3 µA. Protection features include V_{IN} undervoltage lockout

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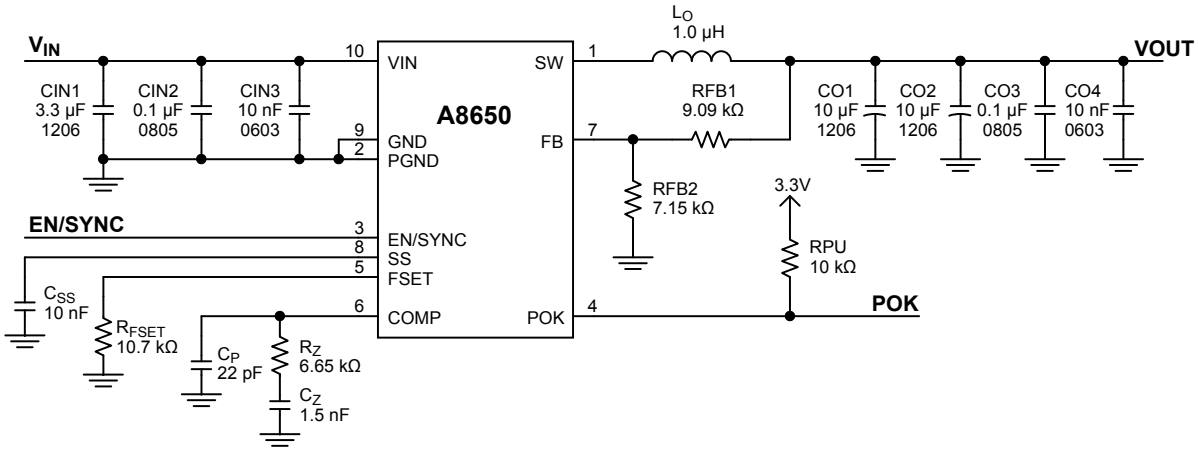
APPLICATIONS:

- GPS/Infotainment
- Automobile Audio
- Home Audio
- Network and Telecom

Typical Application Diagram



Typical application schematic, configured for V_{IN} = 5 V , V_{OUT} = 1.8 V, I_{OUT} = 2.0 A at 2 MHz

FEATURES AND BENEFITS (continued)

- Stable with ceramic output capacitors
- Enable input, and Power OK (POK) output
- Cycle-by-cycle current limiting (OCP)
- Hiccup mode short circuit protection (HIC)
- Overvoltage protection (OVP)
- Overtemperature protection (TSD)
- Open circuit and adjacent pin short circuit tolerant
- Short to ground tolerant at every pin

DESCRIPTION (continued)

(UVLO), cycle-by-cycle overcurrent protection (OCP), hiccup mode short circuit protection (HIC), overvoltage protection (OVP), and thermal shutdown (TSD). In addition, the A8650 provides open circuit, adjacent pin short circuit, and short to ground protection at every pin to satisfy the most demanding automotive applications.

The A8650 is available in both 10-pin MSOP and DFN packages with an exposed pad for enhanced thermal dissipation. It is lead (Pb) free, with 100% matte tin leadframe plating.

SELECTION GUIDE

Part Number	Operating Ambient Temperature Range T_A, (°C)	Package	Packing	Leadframe Plating
A8650KLYTR-T	–40 to 125	10-pin MSOP with exposed thermal pad	4000 pieces per 13-in. reel	100% matte tin
A8650KEJTR-T	–40 to 125	10-pin DFN with exposed thermal pad	1500 pieces per 7-in reel	100% matte tin

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
VIN Pin to GND	V_{IN}		–0.3 to 6	V
SW to GND [2]	V_{SW}	Continuous	–0.3 to V_{IN} + 0.3	V
		t < 50 ns	–1.0, V_{IN} + 2.0	V
All other pins			–0.3 to 6.0	V
Operating Ambient Temperature	T_A	K temperature range	–40 to 125	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

[1] Operation at levels beyond the ratings listed in this table may cause permanent damage to the device. The Absolute Maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to Absolute Maximum-rated conditions for extended periods may affect device reliability.

[2] SW has internal clamp diodes to GND and V_{IN}. Applications that forward bias these diodes should take care not to exceed the IC package power dissipation limits.

THERMAL CHARACTERISTICS: May require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance (LY)	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	48	°C/W
Package Thermal Resistance (EJ)	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	45	°C/W

*Additional thermal information available on the Allegro website.

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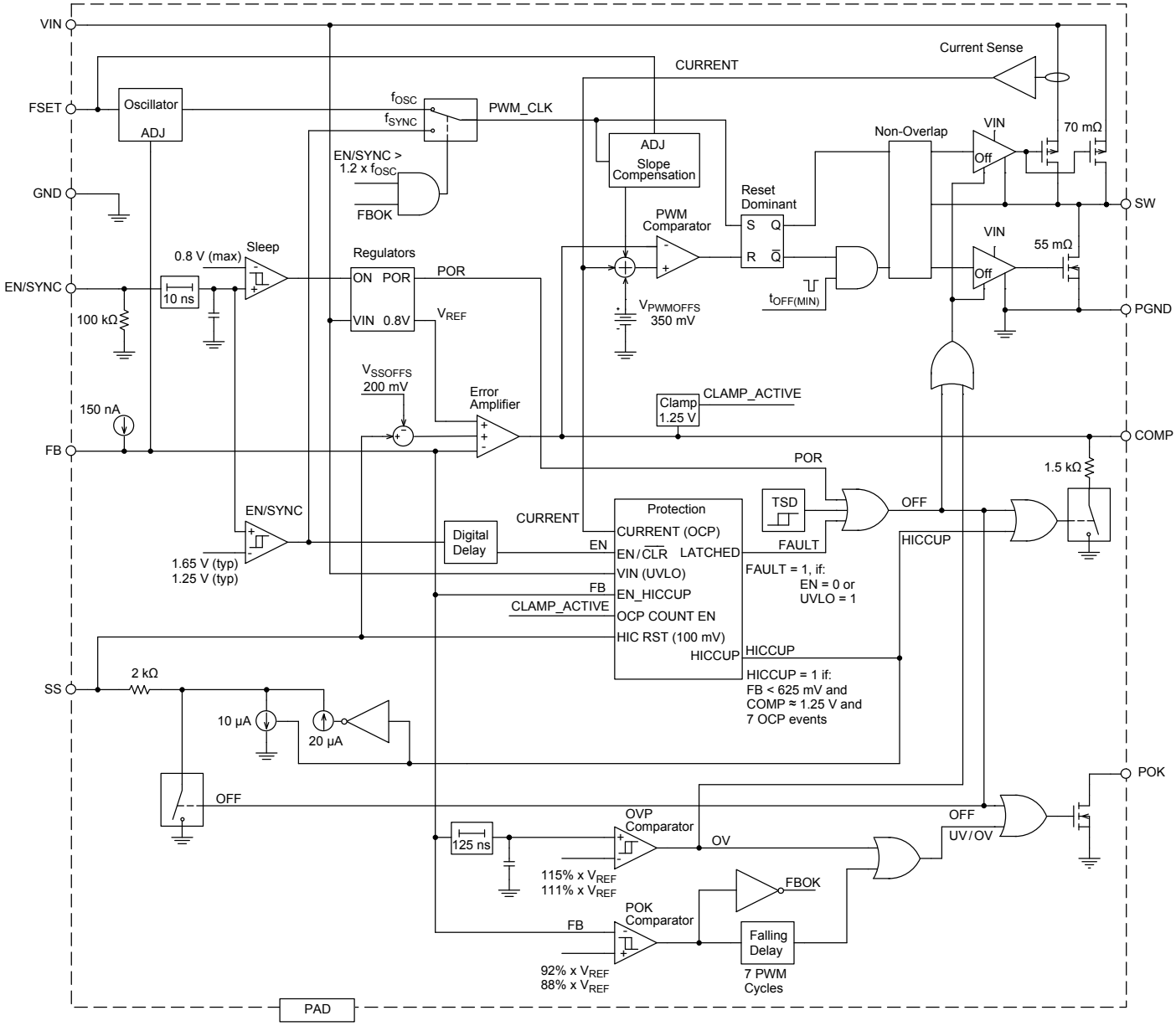
FUNCTIONAL BLOCK DIAGRAM



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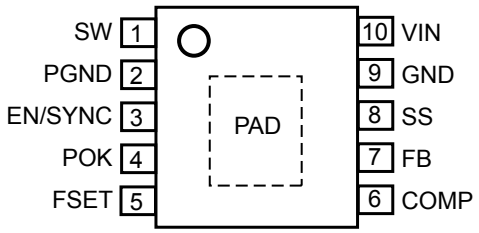
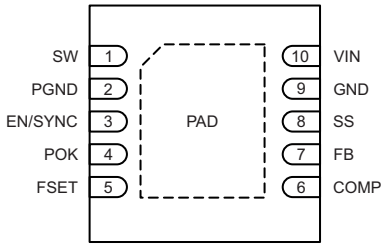
PINOUT DIAGRAMS AND TERMINAL LIST TABLE



Package LY, 10-Pin MSOP Pinout Diagram



Package EJ, 10-Pin DFN Pinout Diagram

Terminal List Table

Number	Name	Function
1	SW	The drain of both the internal high- and low-side MOSFETs. The output inductor (L_O) should be connected to this pin. L_O should be placed as close as possible to this pin and connected with relatively wide traces.
2	PGND	Power ground connection.
3	EN/SYNC	Enable and synchronization input. This pin is a logic input that turns the regulator on or off: set this pin to logic high to turn the regulator on or set this pin to logic low to turn the regulator off. This pin also functions as a synchronization input to allow the PWM frequency to be set by an external clock.
4	POK	Power OK output signal. This pin is an open drain output that transitions from low impedance to high impedance when the output is within the final regulation voltage.
5	FSET	Frequency setting pin. A resistor, R_{FSET}, from this pin to GND sets the PWM switching frequency. See figure 10 and/or equation 2 to determine the value of R_{FSET}.
6	COMP	Output of the error amplifier and compensation node for the current mode control loop. Connect a series RC network from this pin to GND for loop compensation. See the Design and Component Selection sections of this datasheet for further details.
7	FB	Feedback (negative) input to the error amplifier. Connect a resistor divider from the regulator output node, VOUT, to this pin to program the output voltage.
8	SS	Soft start pin. Connect a capacitor, C_{SS}, from this pin to GND to set the soft start time. This capacitor also determines the hiccup period during overcurrent.
9	GND	Ground connection.
10	VIN	Power input for the control circuits and the source of the internal high-side P-channel MOSFET. Connect this pin to a power supply of 2.5 to 5.5 V. A high quality ceramic capacitor should be placed very close to this pin.
–	PAD	Exposed pad of the package providing enhanced thermal dissipation. This pad must be connected to the ground plane(s) of the PCB with at least 6 vias, directly in the pad.

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ELECTRICAL CHARACTERISTICS: Valid at –40°C ≤ T_A = T_J ≤ 125°C, V_{IN} = 5 V; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
INPUT VOLTAGE SPECIFICATIONS						
Operating Input Voltage Range	V_{IN}		2.5	–	5.5	V
VIN UVLO Start Threshold	$V_{INUVSTART}$	V_{IN} rising	2.00	2.22	2.45	V
VIN UVLO Stop Threshold	$V_{INUVSTOP}$	V_{IN} falling	1.80	2.02	2.25	V
VIN UVLO Hysteresis	$V_{INUVHYS}$		–	200	–	mV
INPUT CURRENTS						
Input Quiescent Current	I_Q	$V_{EN/SYNC}$ = 5 V, V_{FB} = 1.0 V, no PWM switching	–	2	4	mA
Input Sleep Supply Current	I_{QSLEEP}	V_{IN} = V_{SW} = 5 V, $V_{EN/SYNC}$ ≤ 0.4 V	–	1	3	µA
REFERENCE VOLTAGE						
Reference (Feedback) Voltage	V_{REF}	2.5 < V_{IN} < 5.5 V, V_{FB} = V_{COMP}	792	800	808	mV
ERROR AMPLIFIER						
Feedback Input Bias Current [1]	I_{FB}	V_{COMP} = 0.7 V, V_{FB} regulated so that I_{COMP} = 0 A	–	–150	–300	nA
Open Loop Voltage Gain [2]	A_{VOL}		–	65	–	dB
Transconductance	g_m	I_{COMP} = 0 µA, V_{SS} > 500 mV	550	750	950	µA/V
		0 V < V_{SS} < 500 mV	–	250	–	µA/V
Source Current	$I_{EA(SRC)}$	V_{FB} < 0.8 V, V_{COMP} = 0.7 V	–	–50	–	µA
Sink Current	$I_{EA(SINK)}$	V_{FB} > 0.8 V, V_{COMP} = 0.7 V	–	+50	–	µA
Maximum Output Voltage	$V_{EAO(MAX)}$		1.00	1.25	1.50	V
COMP Pull Down Resistance	R_{COMP}	FAULT = 1, HICCUP = 1, or EN/SYNC = low	–	1.5	–	kΩ
PULSE WIDTH MODULATION (PWM)						
PWM Ramp Offset	$V_{PWMOFFS}$	V_{COMP} for 0% duty cycle	–	350	–	mV
High-Side MOSFET Minimum Controllable On-Time	$t_{ON(MIN)}$		–	65	105	ns
Low-Side MOSFET Minimum On-Time	$t_{OFF(MIN)}$	Does not include total gate driver non-overlap time, 2 x t_{NO}	–	50	100	ns
Gate Driver Non-Overlap Time [2]	t_{NO}		–	15	–	ns
COMP to SW Current Gain	g_{mPOWER}		–	4.5	–	A/V
Slope Compensation [2]	S_E	f_{sw} = 2.0 MHz	1.65	2.35	2.85	A/µs
		f_{sw} = 0.25 MHz	0.21	0.29	0.36	A/µs
MOSFET PARAMETERS						
High-Side MOSFET On-Resistance [3]	$R_{DS(ON)HS}$	T_A = 25°C, I_{DS} = 100 mA	–	70	80	mΩ
		I_{DS} = 100 mA	–	–	145	mΩ
SW Node Rise Time [2]	$t_{R(SW)}$	V_{IN} = 5 V	–	12	–	ns
High-Side MOSFET Leakage [4]	$I_{LKG(HS)}$	$V_{EN/SYNC}$ ≤ 0.4 V, V_{SW} = 0 V, V_{IN} = 5 V, –40˚C < T_A = T_J < 85˚C	–	–	4	µA
		T_A = T_J = 125˚C	–	5	25	µA

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ELECTRICAL CHARACTERISTICS (Continued): Valid at $-40°C \le T_A = T_J \le 125°C$, V_{IN} = 5 V; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
MOSFET PARAMETERS (continued)						
Low-Side MOSFET On-Resistance [3]	$R_{DS(on)LS}$	T_A = 25°C, I_{DS} = 100 mA	–	55	65	mΩ
		I_{DS} = 100 mA	–	–	115	mΩ
Low-Side MOSFET Leakage [4]	$I_{LKG(LS)}$	$V_{EN/SYNC} \le 0.4$ V, V_{SW} = 5 V, $-40°C < T_A = T_J < 85°C$	–	–	1	µA
		$V_{EN/SYNC} \le 0.4$ V, V_{SW} = 5 V, $T_A = T_J$ = 125°C	–	4	10	µA
OSCILLATOR FREQUENCY						
Oscillator Frequency	f_{OSC}	R_{FSET} = 8.45 kΩ	2.20	2.45	2.70	MHz
		R_{FSET} = 23.2 kΩ	0.90	1.00	1.10	MHz
		R_{FSET} = 100 kΩ	–	250	–	kHz
SYNCHRONIZATION TIMING						
Synchronization Frequency Range	$f_{SW(MULT)}$	Relative to f_{OSC}(typ)	1.2 × f_{OSC}	–	1.5 × f_{OSC}	–
Synchronized PWM Frequency	f_{SYNC}		–	–	2.9	MHz
Synchronization Input Duty Cycle	D_{SYNC}		–	–	80	%
Synchronization Input Pulse Width	t_{PWSYNC}	V_{IN} = 3.3 V, $V_{EN/SYNC}$ = 3.3 V pulse input	200	–	–	ns
Synchronization Input Edge Rise Time [2]	t_{rSYNC}		–	10	15	ns
Synchronization Input Edge Fall Time [2]	t_{fSYNC}		–	10	15	ns
ENABLE/SYNCHRONIZATION INPUT						
EN/SYNC High Threshold	$V_{EN/SYNC(H)}$	$V_{EN/SYNC}$ rising	–	–	1.8	V
EN/SYNC Low Threshold	$V_{EN/SYNC(L)}$	$V_{EN/SYNC}$ falling	0.8	–	–	V
EN/SYNC Hysteresis	$V_{EN/SYNC(HYS)}$	$V_{EN/SYNC(H)} - V_{EN/SYNC(L)}$	–	200	–	mV
EN/SYNC Digital Delay	t_{SLEEP}	$V_{EN/SYNC}$ transitioning low	–	32	–	PWM cycles
EN/SYNC Input Resistance	$R_{EN/SYNC}$		50	100	–	kΩ
EN/SYNC Pulse Rejection	$t_{EN/SYNCR}$	V_{IN} = 3.3 V, $V_{EN/SYNC}$ = 1.3 V pulse input	–	10	–	ns
OVERCURRENT PROTECTION (OCP) AND HICCUP MODE						
Pulse-by-Pulse Current Limit	$I_{LIM(5\%)}$	Duty Cycle = 5%	3.5	4.1	4.7	A
	$I_{LIM(90\%)}$	Duty Cycle = 90%	2.3	3.1	4.2	A
Hiccup Disable Threshold	HIC_{DIS}	V_{FB} rising	–	750	–	mV
Hiccup Enable Threshold	HIC_{EN}	V_{FB} falling	–	625	–	mV
OCP / HICCUP Count Limit	OCP_{LIMIT}	Hiccup enabled, OCP pulses	–	7	–	counts

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ELECTRICAL CHARACTERISTICS (Continued): Valid at –40°C ≤ T_A = T_J ≤ 125°C, V_{IN} = 5 V; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SOFT START (SS PIN)						
SS Offset Voltage	V_{SSOFFS}	V_{SS} rising due to I_{SSSU}	120	200	270	mV
SS Fault/Hiccup Reset Voltage	V_{SS_RESET}	V_{SS} falling due to I_{SSHIC}	–	100	120	mV
SS Startup (Source) Current	I_{SSSU}	V_{SS} = 1 V, HICCUP = FAULT = 0	−10	–20	−30	µA
SS Hiccup (Sink) Current	I_{SSHIC}	V_{SS} = 0.5 V, HICCUP = 1	5	10	20	µA
SS Input Resistance	R_{SS}	FAULT = 1 or EN/SYNC = low	–	2	–	KΩ
SS to VOUT Delay Time	$t_{SS(DELAY)}$	C_{SS} = 22 nF	–	175	–	µs
VOUT Soft Start Ramp Time	t_{SS}	C_{SS} = 22 nF	–	880	–	µs
SS Switching Frequency	$f_{SW(SS)}$	V_{FB} = 0 V	–	f_{SW} / 3	–	–
		V_{FB} ≥ 600 mV	–	f_{SW}	–	–
POWER OK (POK PIN) OUTPUT						
POK Output Voltage	V_{POK}	I_{POK} = 4 mA	–	–	0.4	V
POK Undervoltage Threshold	POK_{UV}	V_{FB} rising, as a percent of V_{REF}	89	92	95	%
POK Undervoltage Hysteresis	POK_{UVHYS}	V_{FB} falling, as a percent of V_{REF}	–	4	–	%
POK Overvoltage Threshold	POK_{OV}	V_{FB} rising, as a percent of V_{REF}	112	115	118	%
POK Overvoltage Hysteresis	POK_{OVHYS}	V_{FB} falling, as a percent of V_{REF}	–	4	–	%
POK Digital Delay	POK_{DLY}	V_{FB} rising only	–	7	–	PWM cycles
POK Leakage	$I_{POK(LKG)}$	V_{POK} = 5 V, V_{COMP} ≤ 0.3 V	–	–	1	µA
THERMAL SHUTDOWN PROTECTION (TSD)						
Thermal Shutdown Threshold [2]	T_{TSD}	Temperature rising	155	170	185	°C
Thermal Shutdown Hysteresis [2]	T_{TSDHYS}	Temperature falling	–	20	–	°C

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] T_A = T_J = 25˚C ensured by design and characterization, not production tested.
[4] T_A = T_J = 85˚C ensured by design and characterization, not production tested.

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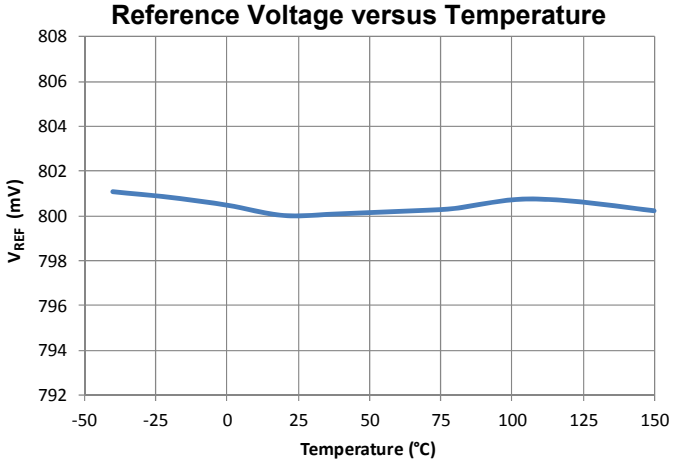
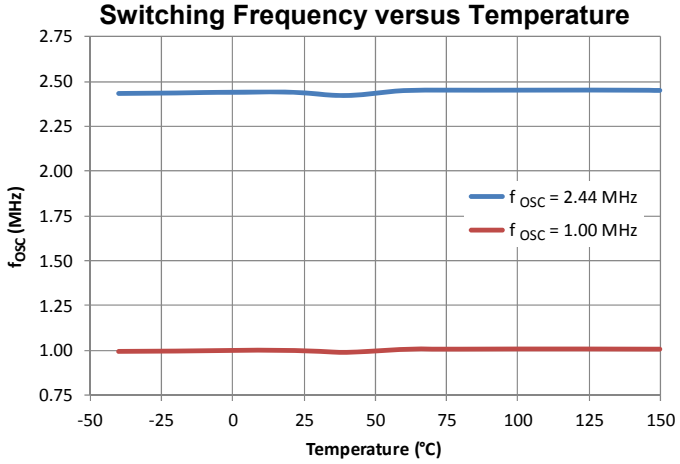
CHARACTERISTIC PERFORMANCE

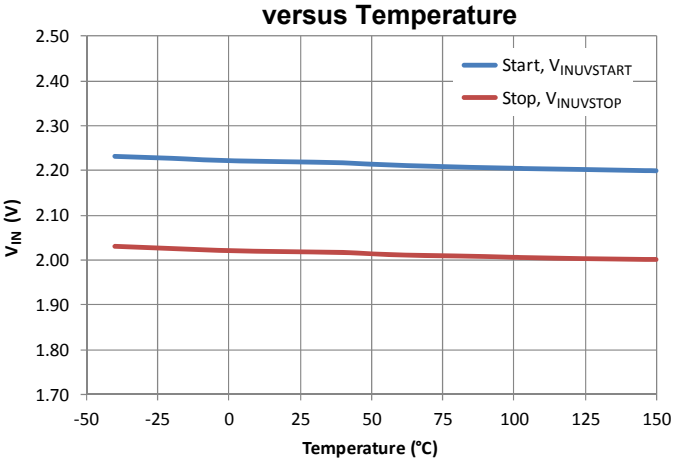
Reference Voltage versus Temperature



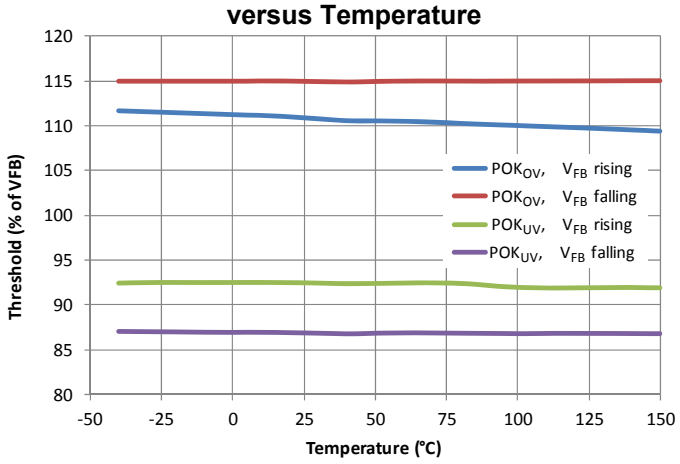
Switching Frequency versus Temperature



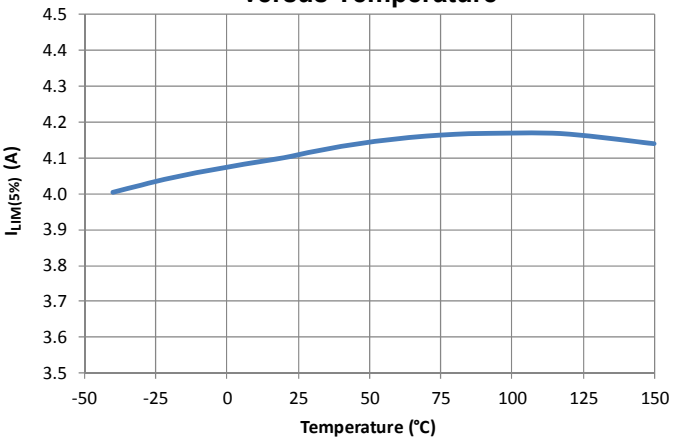
VIN UVLO Start and Stop Thresholds versus Temperature



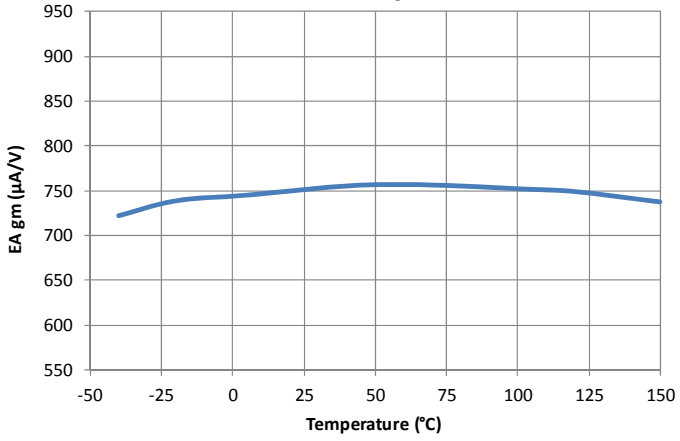
POK_{OV} and POK_{UV} Thresholds versus Temperature



Cycle-by-Cycle Current Limit at $t_{ON(MIN)}$ versus Temperature



Error Amplifier Transconductance versus Temperature



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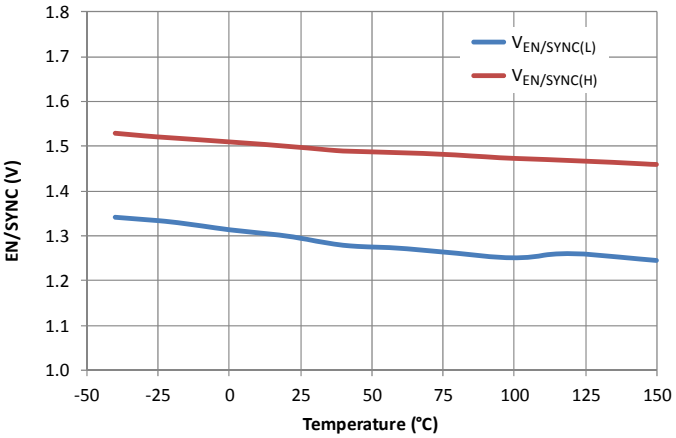
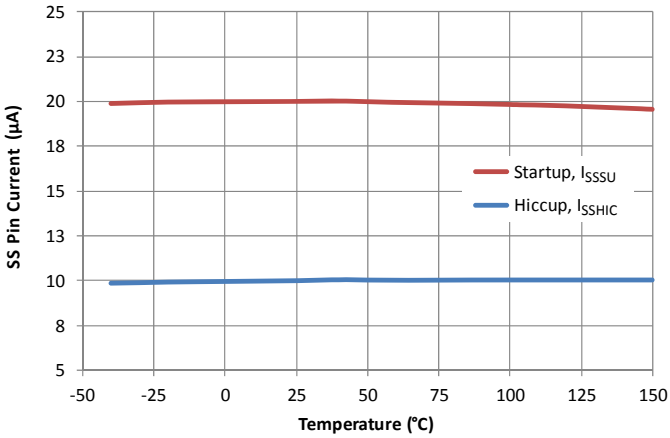
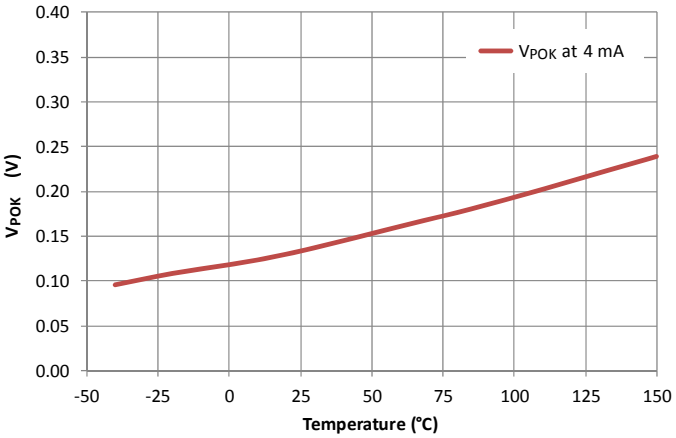
EN/SYNC High and Low Thresholds versus Temperature



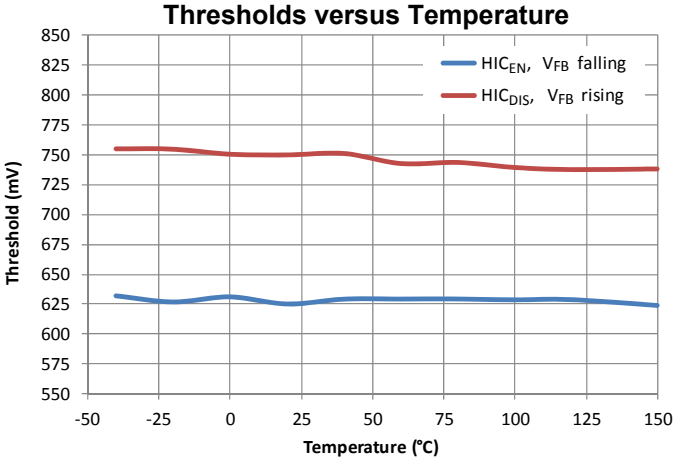
Soft Start Startup and Hiccup Currents versus Temperature



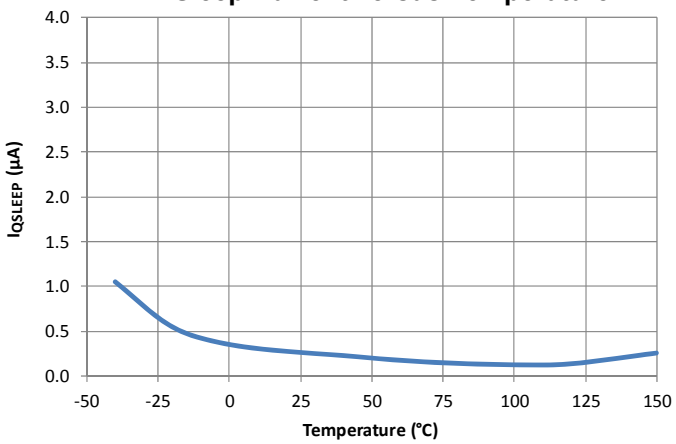
POK Low Output Voltage versus Temperature



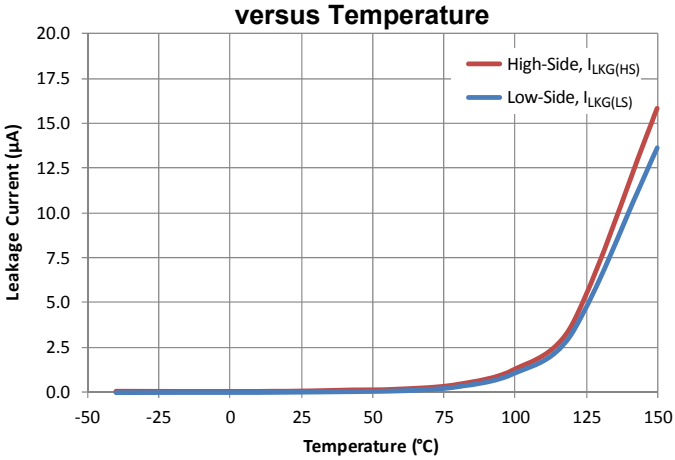
Hiccup Enable and Disable Thresholds versus Temperature



VIN Sleep Current versus Temperature



High- and Low-Side MOSFETs Leakage versus Temperature



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FUNCTIONAL DESCRIPTION

Overview

The A8650 is a synchronous PWM regulator that incorporates all the control and protection circuitry necessary to satisfy a wide range of low voltage applications. The A8650 employs current mode control to provide fast transient response, simple compensation, and excellent stability.

The features of the A8650 include a ±1% precision reference, an adjustable switching frequency, a transconductance error amplifier, an enable/synchronization input, integrated power MOSFETs, adjustable soft-start time, pre-bias startup capability, low current sleep mode, and a Power OK (POK) output.

The protection features of the A8650 include undervoltage lockout (UVLO), cycle-by-cycle overcurrent protection (OCP), hiccup mode short circuit protection (HIC), overvoltage protection (OVP), and thermal shutdown (TSD). In addition, the A8650 provides open circuit, adjacent pin short circuit, and pin-to-ground short circuit protection.

Reference Voltage

The A8650 incorporates an internal reference that allows output voltages as low as 0.8 V. The accuracy of the internal reference is ±1% across the entire operating temperature range. The output voltage of the regulator is adjusted by connecting a resistor divider (RFB1 and RFB2 in the typical application schematic) from VOUT to the FB pin of the A8650.

Oscillator/Switching Frequency

The base PWM switching frequency, f_{OSC}, of the A8650 is adjustable from 250 kHz to 2.45 MHz and has an accuracy of ±12% across the operating temperature range. The base frequency is used to set the device switching frequency, f_{SW}, which can also be further increased by the optional synchronization function (described later in the section on EN/SYNC operation).

Connecting a resistor from the FSET pin to GND, as shown in the typical application schematic, sets the base switching frequency. An FSET resistor with ±1% tolerance is recommended. A graph of f_{OSC} versus R_{FSET}, and an equation to calculate R_{FSET}, are provided in the Component Selection section of this datasheet.

Transconductance Error Amplifier

The primary function of the transconductance error amplifier is to regulate the A8650 output voltage. The error amplifier is shown in figure 1 as a device with three inputs, two positive and one negative. The negative input simply is connected to the FB pin and is used to sense the feedback voltage for regulation. The two positive inputs are connected to the soft start and reference voltages, and the error amplifier performs an analog OR selection between them. It regulates to either the soft start pin voltage minus the Soft Start Offset (200 mV (typ)) or the A8650 internal reference, whichever is lower.

To stabilize the regulator, a series RC compensation network (R_Z C_Z) must be connected from the error amplifier output (COMP pin) to GND as shown in the typical application schematic. In most applications, an additional, low value capacitor (C_P) should be connected in parallel with the R_Z C_Z compensation network to roll-off the loop gain at higher frequencies. However, if the C_P capacitor is too large, the phase margin of the regulator may be reduced.

If the regulator is disabled or a fault occurs, the COMP pin is immediately pulled to GND via an internal 1.5 kΩ pull-down and PWM switching is inhibited.

Slope Compensation

The A8650 incorporates internal slope compensation to allow PWM duty cycles near or above 50% to accommodate a wide range of input/output voltages, switching frequencies, and inductor values. As shown in the functional block diagram, the slope compensation signal is added to the sum of the current sense and PWM Ramp Offset ($V_{PWMOFFS}$). The amount of slope compensation is scaled directly with the base switching frequency (f_{OSC}, set by R_{FSET}). However, the amount of slope compensation does

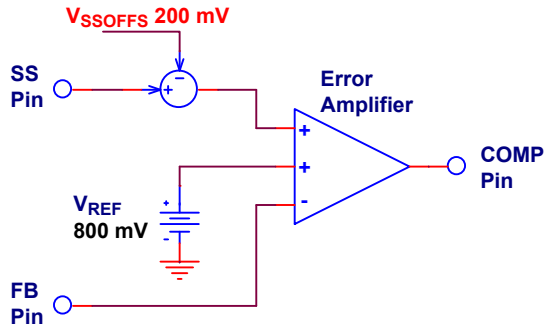

Figure 1. A8650 Error Amplifier

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not change when the synchronization function is used to alter the switching frequency.

Sleep Mode

If the voltage at the EN/SYNC pin is low for more than 32 PWM clock cycles, the A8650 discharges the soft start capacitor (via a 2 kΩ pulldown) until $V_{SS} \approx 100$ mV. At that time the A8650 will enter sleep mode and draw less than I_{QSLEEP} (3 µA (max)) from V_{IN}. However, the total current drawn by the VIN pin will be the sum of the current drawn by the control circuitry plus any leakage due to the high- and low-side MOSFETs ($I_{LKG(HS)}$, and $I_{LKG(LS)}$).

Enable/Synchronization (EN/SYNC) Input

The enable/synchronization (EN/SYNC) input provides three functions: enabling/disabling the A8650 with system control, enabling/disabling the A8650 automatically, and synchronizing the output PWM frequency synchronization to an external clock signal input.

When EN/SYNC is being used as a system controlled enabling/disabling logic input, when EN/SYNC is kept high, the A8650 turns on and, provided there are no fault conditions, V_{OUT} will ramp to its final voltage in a time set by the soft start capacitor (C_{SS}). When EN/SYNC is brought low for more than 32 PWM clock cycles (see figure 2) the voltage at the soft start pin is discharged by a 2 kΩ pulldown, and V_{SS} will decay quickly starting from the input voltage level. When V_{SS} drops below ≈ 100 mV, the A8650 will enter sleep mode and draw less than 3 µA from the input. A timing diagram showing startup and shutdown using EN/SYNC is shown in figure 8. The short delay (the 32 PWM clock cycles between when EN/SYNC transitions to low and when PWM switching stops) is necessary because the enable circuitry must distinguish between the relatively constant enabling/disabling function logic levels and the longest allowed pulses generated when the EN/SYNC frequency synchronization function also is being used.

When used in the frequency synchronization function, EN/SYNC accepts an external clock to scale the PWM switching frequency (f_{SW}) from 1.2× to 1.5× above the base frequency (f_{OSC}) set by the R_{FSET} resistor. The applied clock pulses must satisfy the pulse width, duty cycle, and rise/fall time requirements shown in the Electrical Characteristics table in this datasheet. Note that when EN/SYNC is used as a synchronization input, soft start still occurs at the base frequency (f_{OSC}) and synchronization to the external clock occurs only after soft start is complete (when $V_{FB} > POK_{UV}$).

Finally, when used to automatically enable the A8650, the EN/SYNC input pin is connected to V_{IN} via a resistor, as shown in figure 3. The series resistance is recommended to prevent large V_{IN} capacitors from discharging into the EN/SYNC pin at power-down.

Power MOSFETs

The A8650 includes a 70 mΩ, high-side P-channel MOSFET capable of delivering up to 4.1 A at 5% duty cycle. The A8650 also includes a 55 mΩ, low-side N-channel MOSFET to provide synchronous rectification.

The low-side MOSFET continues to conduct when the inductor current crosses zero to maintain constant conduction mode (CCM). This helps to minimize EMI/EMC for noise sensitive

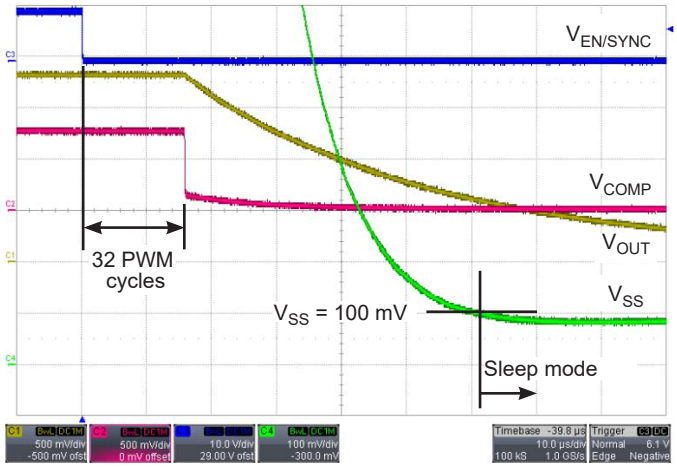

Figure 2. PWM switching stops 32 PWM cycles after EN/SYNC transitions low, and sleep mode begins when V_{SS} decays to V_{SS_RESET} (100 mV)

Figure 3. External circuit for automatically enabling the A8650 from VIN

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applications by eliminating the SW output high-frequency ringing associated with discontinuous conduction mode (DCM). When a fault occurs or the A8650 is disabled, the SW pin becomes high impedance by turning off both the upper and lower MOSFETs.

Pulse Width Modulation (PWM)

A high-speed PWM comparator, capable of pulse widths less than 105 ns, is included in the A8650. The inverting input of the comparator is connected to the output of the error amplifier. The non-inverting input is connected to the sum of the current sense signal, the slope compensation, and the PWM Ramp Offset ($V_{PWMOFFS}$).

At the beginning of each PWM cycle, the PWM_CLK signal sets the PWM flip flop and the high-side MOSFET is turned on. When the summation of the current sense signal, the slope compensation, and the DC PWM Ramp Offset rises above the error amplifier voltage, the comparator resets the PWM flip flop and the high-side MOSFET is turned off. After a short delay to prevent cross-conduction (t_{NO}), the low-side MOSFET is turned on. The PWM flip flop is reset dominant so, if the output voltage of the error amplifier drops below the PWM Ramp Offset, then PWM 0% duty cycle (that is, pulse skipping) operation is achieved.

Current Sense Amplifier

A high-bandwidth current sense amplifier monitors the current in the high-side MOSFET. The current signal is supplied to the PWM comparator, the cycle-by-cycle current limiter, and the hiccup mode counter.

Soft Start (Startup) and Inrush Current Control

Inrush currents to the regulator are controlled by the soft start function. When the A8650 is enabled, after all faults are cleared the soft start pin will source approximately 20 µA (I_{SSSU}) and the voltage on the soft start capacitor (C_{SS}) will ramp upward from 0 V. When the voltage at the soft start pin exceeds the Soft Start Offset (V_{SSOFFS}, 200 mV(typ)), the error amplifier output slews upward and, shortly thereafter, PWM switching will begin. As shown in figure 4, there is a short delay ($t_{SS(DELAY)}$) between when the EN/SYNC pin transitions high and when the soft start voltage reaches 200 mV.

After the A8650 starts switching, the error amplifier will regulate the voltage at the FB pin to the soft start pin voltage minus the Soft Start Offset voltage. After switching starts, the voltage at the SS pin will rise from 200 mV to 1000 mV, a difference of 800 mV. At the same time, the voltage at the FB pin will rise from 0 V to 800 mV and the regulator output voltage will rise from 0 V to the setpoint determined by the feedback resistor divider (RFB1 and RFB2).

When the voltage at the soft start pin reaches approximately 1000 mV, the error amplifier will change mode and begin regulating to the A8650 internal reference, 800 mV. The voltage at the soft start pin will continue to rise to approximately V_{IN}. Complete soft start operation is shown in figure 4.

During startup, the PWM switching frequency is scaled linearly from f_{OSC} / 3 to f_{OSC} as the voltage at the FB pin ramps from 0 V to 600 mV. This is done to prevent the output inductor current from climbing to a level that may damage the A8650 when the input voltage is high and the output of the regulator is either shorted or soft starting a relatively high capacitance or very heavy load.

Pre-Biased Startup

If the output capacitors are pre-biased, the A8650 will shift the startup routine parameters to prevent discharging the output capacitors. Normally, PWM switching starts when the voltage at the soft start pin reaches approximately 200 mV. However, in the case with pre-biasing, the voltage at the FB pin (V_{FB}) is non-zero. Switching will not start until the voltage at the soft-start

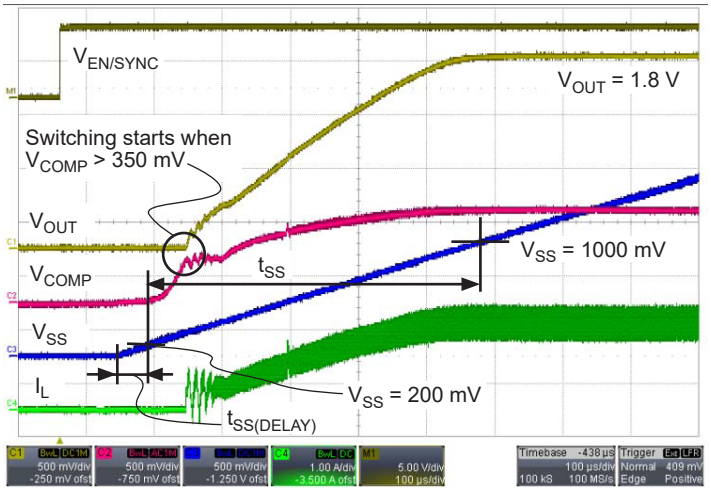

Figure 4. Startup to V_{OUT} = 1.8 V, at I_{OUT} = 2.0 A with C_{SS} = 10 nF

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pin increases to approximately V_{FB} + 200 mV. At this voltage, the error amplifier output will slew upward. Shortly thereafter, PWM switching starts and V_{OUT} ramps upward from the pre-bias level. Figure 5 shows startup when the output voltage is pre-biased to 0.9 V.

Power OK (POK) Output

The Power OK (POK) output is an open drain output, so an external pull-up resistor must be connected to it. An internal comparator monitors the voltage at the FB pin and controls the internal open drain N-MOSFET at the POK pin. POK is high when the voltage at the FB pin is within regulation. The POK output is pulled low if any of the following are true:

- V_{FB} is rising, and is < 92% of the internal reference voltage, or
- V_{FB} is rising, and is > 115% of the internal reference voltage, or
- EN/SYNC is low for more than 32 PWM clock cycles, or
- VIN pin UVLO occurs, or
- Thermal Shutdown (TSD) occurs.

If the A8650 is running and EN/SYNC transitions low for more than 32 PWM clock cycles, then POK will transition low and remain low only as long as the internal circuitry is able to enhance the open-drain output device. When V_{IN} fully collapses, POK will return to the high impedance state. The POK comparator incorporates hysteresis to prevent chattering due to voltage ripple at the FB pin.

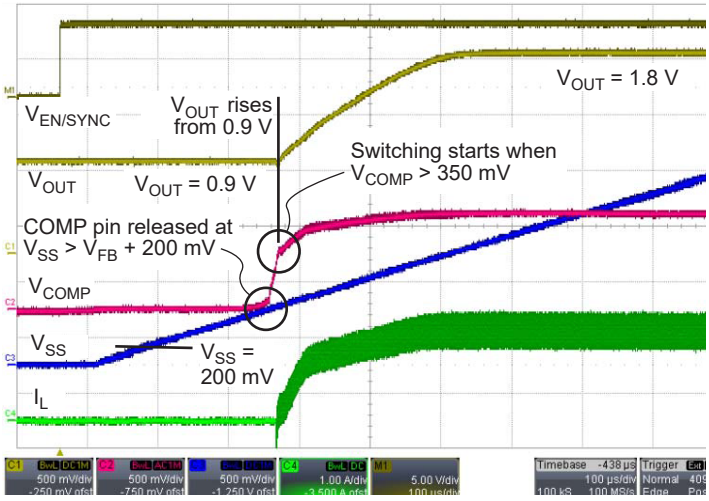

Figure 5. Startup to V_{OUT} = 1.8 V, V_{OUT} pre-biased to 0.9 V

Protection Features

Undervoltage Lockout (UVLO)

An undervoltage lockout (UVLO) comparator monitors the voltage at the VIN pin and keeps the regulator disabled if the voltage is below the lockout threshold ($V_{INUVSTART}$). The UVLO comparator incorporates enough hysteresis ($V_{INUVHYS}$) to prevent on/off cycling of the regulator due to IR drops in the VIN path during heavy loading or during startup. Figure 8 shows the A8650 operation for a UVLO-initiated startup (EN/SYNC = high, V_{IN} ramps up).

Thermal Shutdown (TSD)

The A8650 protects itself from overheating by means of an internal thermal monitoring circuit. If the junction temperature exceeds the thermal shutdown threshold (T_{TSD}, 170°C (typ)) the voltages at the soft start and COMP pins will be pulled to GND and both the high-side and low-side MOSFETs will be turned off. The A8650 will automatically restart when the junction temperature decreases more than the thermal shutdown hysteresis (T_{TSDHYS}, 20°C(typ)). Figure 8 shows the A8650 operation during and after a TSD event.

Overvoltage Protection (OVP)

The A8650 uses the FB pin to provide a basic level of overvoltage protection. An overvoltage condition could occur if the load current decreases very quickly or the regulator output is pulled high by some external voltage. When an overvoltage condition is detected, POK is pulled low and PWM switching stops. The COMP and soft start pins are not directly affected by OVP. If the regulator output decreases back to the allowed operating range, POK will transition to high and PWM switching will resume.

Cycle-by-Cycle Overcurrent Protection (OCP)

The A8650 monitors the current in the high-side MOSFET and if the current exceeds the cycle-by-cycle overcurrent threshold (I_{LIM}) then the high-side MOSFET is turned off. Normal PWM operation resumes on the next clock pulse from the oscillator. The A8650 includes leading edge blanking to prevent falsely triggering the cycle-by-cycle current limit when the upper MOSFET is turned on.

Because of the addition of the slope compensation ramp to the inductor current, the A8650 delivers more current at lower duty cycles and less current at higher duty cycles. For a given duty cycle, this results in a little more current being available at lower switching frequencies than at higher frequencies.

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Figure 6 shows the typical and worst-case cycle-by-cycle current limits versus duty cycle, at 2.45 MHz and 250 kHz.

Output Short Circuit (Hiccup Mode) Protection

Hiccup mode protects the A8650 when the load is either too high or when the output of the regulator is shorted to ground. When the voltage at the FB pin is below the Hiccup Enable Threshold (HIC_{EN}, 625 mV(typ)) hiccup mode protection is enabled. When the voltage at the FB pin is above the Hiccup Disable Threshold (HIC_{DIS}, 750 mV(typ)) hiccup mode protection is disabled.

Hiccup Mode overcurrent protection monitors the number of overcurrent events using an up/down counter. An overcurrent pulse increments the counter by one and a PWM cycle without an overcurrent pulse decrements the counter by one. If more than seven consecutive overcurrents are detected, then the hiccup latch is set and PWM switching is stopped. The HICCUP signal causes the COMP pin to be pulled low. Hiccup mode also enables a current sink connected to the soft start pin (nominally 10 µA) so, when hiccup occurs, the voltage at the soft start pin ramps downward.

When the voltage at the soft start pin decays to a low level (V_{SS_RESET}, 100 mV (typ)), the hiccup latch is cleared and the 10 µA soft start pin current sink is turned off. Also, the soft start pin begins charging the soft start capacitor with 20 µA, so the voltage at the soft start pin begins to ramp upward. When the voltage at the soft start pin exceeds the Soft Start Offset (V_{SSOFFS}, 200 mV (typ)) the error amplifier will force the voltage at the COMP pin to quickly ramp upward and, shortly thereafter, PWM switching will resume. If the short circuit at the regulator output remains, another hiccup cycle will occur. Hiccup cycles will repeat until the short circuit is removed or the regulator is disabled. If the short circuit is removed, the A8650 will soft start normally and the output voltage will be ramped to the setpoint level. Hiccup mode operation is shown in both figures 7 and 8.

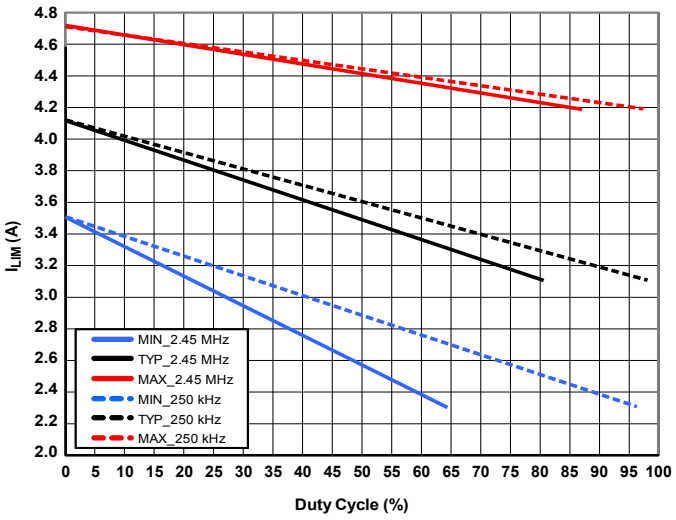

Figure 6. Cycle-by-cycle current limiting versus duty cycle; at f_{SW} = 250 kHz (dashed curves) and f_{SW} = 2.45 MHz (solid curves)

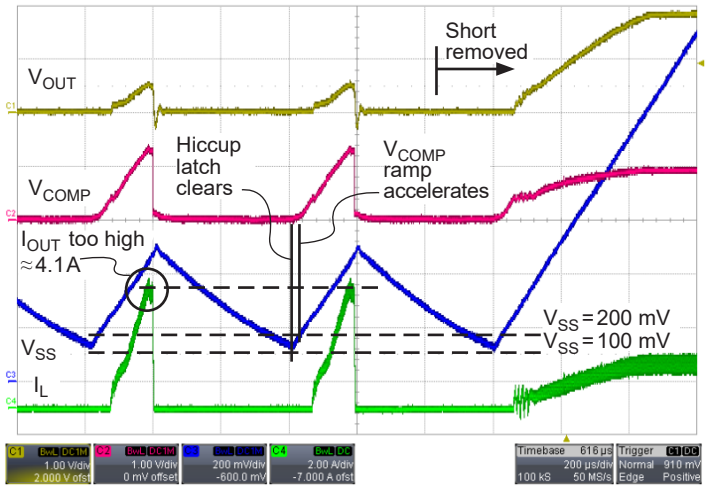

Figure 7. Hiccup mode operation and recovery

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TABLE 1. Summary of A8650 Fault Modes and Operation

Fault Mode	V_{SS}	V_{COMP}	High-Side MOSFET and f_{SW}	Low-Side MOSFET	POK State	Reset Condition
Output hard short to ground (V_{OUT} = V_{FB} = 0 V)	Hiccup after V_{COMP} ≈ 1.25 V and 7 overcurrent faults	Clamped to ≈1.25 V for I_{LIM}, then pulled low during hiccup	Controlled by V_{COMP}. f_{SW} / 3 if 0< V_{FB}<200 mV	Active during $t_{OFF(MIN)}$, Off during hiccup	Pulled low	Auto, if short removed
Output overcurrent (heavy load) and V_{FB} < HIC_{DIS}	Hiccup after V_{COMP} ≈ 1.25 V and 7 overcurrent faults	Clamped to ≈1.25 V for I_{LIM}, then pulled low during hiccup	Controlled by V_{COMP}. f_{SW} / 3 if 0< V_{FB}< 200 mV, f_{SW} / 3 to f_{SW} if 200 mV < V_{FB} < 600 mV	Active during $t_{OFF(MIN)}$, Off during hiccup	Pulled low	Auto, if the load decreases
SW hard short to ground	Not affected; hiccup may occur when the short is removed	Clamped to ≈1.25 V for I_{LIM}, then pulled low if hiccup occurs	Controlled by V_{COMP}. turned off if V_{SW} ≈ 0 V and blanking time expires, f_{SW} / 3 if 0 < V_{FB} < 200 mV	Active during $t_{OFF(MIN)}$, Off if hiccup occurs when the short is removed	Depends on V_{OUT}	Auto, if short removed
SW soft short to ground	Hiccup after V_{COMP} ≈ 1.25 V and 7 overcurrent faults	Clamped to ≈1.25 V for I_{LIM}, then pulled low during hiccup	Controlled by V_{COMP}. f_{SW} / 3 if 0<VFB< 200 mV, f_{SW} / 3 to f_{SW} if 200 mV < V_{FB} < 600 mV	Active during $t_{OFF(MIN)}$, Off during hiccup	Depends on V_{OUT}	Auto, if short removed
FB pin open (FB pin floats high due to negative bias current)	Not affected	Transitions low via loop response as V_{FB} floats high	Off. f_{SW} / 3 if 0< V_{FB}< 200 mV, f_{SW} / 3 to f_{SW} if 200 mV < V_{FB}< 600 mV	Off. Disabled if V_{COMP} < 200 mV (to limit negative SW current)	Pulled low	Auto, if FB pin connected to V_{OUT}
Output overvoltage (V_{FB} > 115% × V_{REF})	Not affected	Transitions low via loop response because V_{FB} > V_{REF}	Off. f_{SW} / 3 if 0< V_{FB}< 200 mV, f_{SW} / 3 to f_{SW} if 200 mV < V_{FB}< 600 mV	Off. Disabled if V_{COMP} < 200 mV (to limit negative SW current)	Pulled low	Auto, if V_{FB} returns to the allowed operating range
Output undervoltage (V_{FB} < 92% × V_{REF})	Not affected	Transitions high via loop response because V_{FB} < V_{REF}	Controlled by V_{COMP}. f_{SW} / 3 if 0<V_{FB}< 200 mV, f_{SW} / 3 to f_{SW} if 200 mV < V_{FB} < 600 mV	Active during $t_{OFF(MIN)}$	Pulled low	Auto, if V_{FB} returns to the allowed operating range
VIN dropout or EN/SYNC glitches low for > 32 PWM cycles	Pulled low and latched until V_{SS} < V_{SS_RESET}	Pulled low and latched until V_{SS} > V_{SSOFFS}	Off	Off	Pulled low	Auto, if V_{IN} recovers or if EN/SYNC returns high
Thermal shutdown (TSD)	Pulled low and latched until V_{SS} < V_{SS_RESET}	Pulled low and latched until V_{SS} > V_{SSOFFS}	Off	Off	Pulled low	Auto, if the junction cools down

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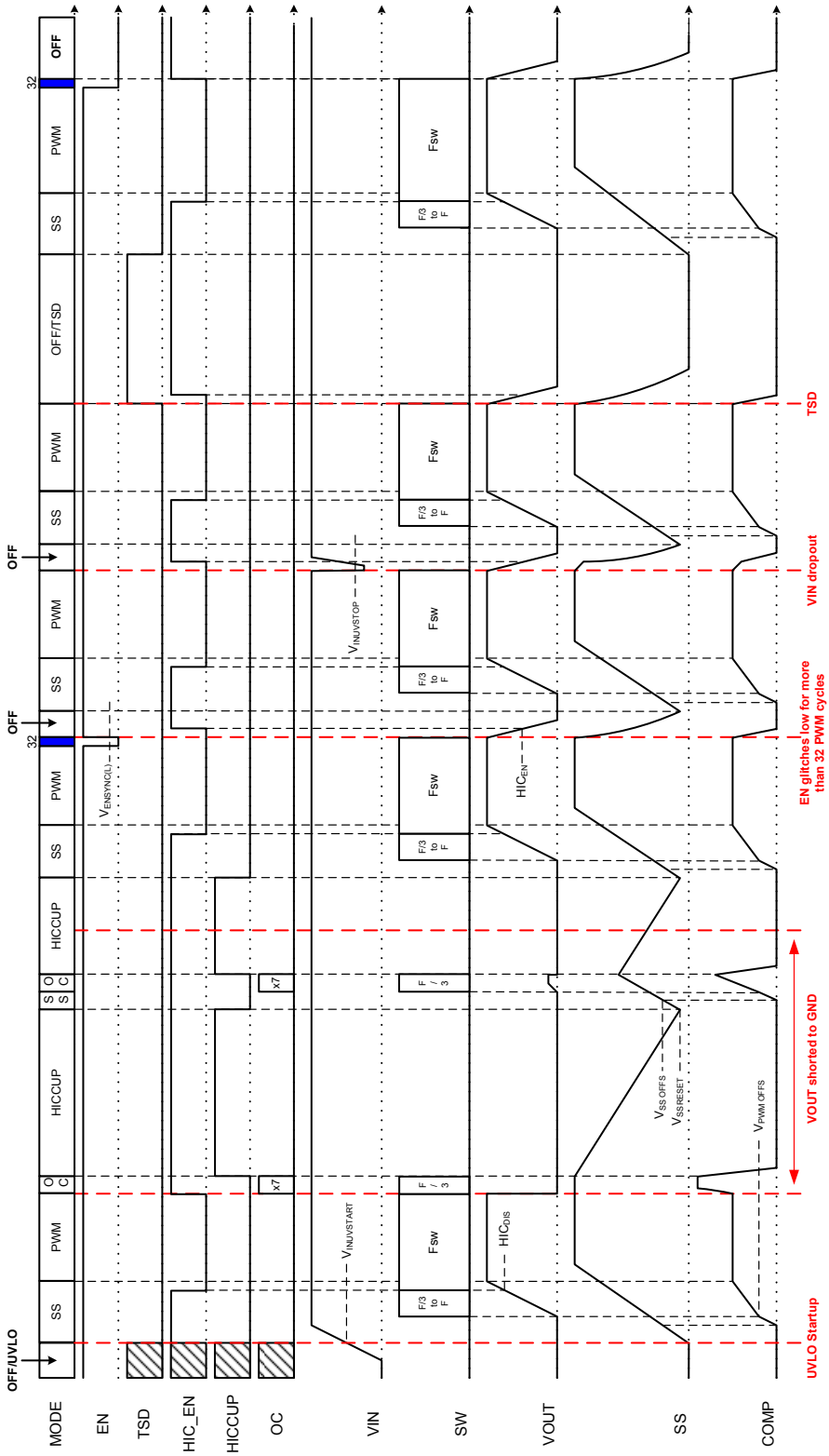

Figure 8. A8650 timing diagram

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APPLICATION INFORMATION

Design and Component Selection

Setting the Output Voltage (VOUT, R_{FB1}, R_{FB2})

The output voltage of the A8650 is determined by connecting a resistor divider from the output node (VOUT) to the FB pin as shown in figure 9. There are trade-offs when choosing the value of the feedback resistors. If the series combination (R_{FB1}+R_{FB2}) is relatively low, then the light-load efficiency of the regulator will be reduced. So, to maximize that efficiency, it is best to choose high-value resistors. On the other hand, if the parallel combination (R_{FB1}//R_{FB2}) is too high, then the regulator may be susceptible to noise coupling into the FB pin.

In general, to produce the target output voltage, V_{OUT}:

$$\frac{R_{FB1}}{R_{FB2}} = \left(\frac{V_{OUT}}{0.8\ (V)} - 1 \right) \quad (1)$$

Table 2 shows the most common output voltages and recommended feedback resistors, assuming <0.2% efficiency loss at light load of 100 mA, and a parallel combination of 4 kΩ presented to the FB pin. For optimal system accuracy, it is recommended that the feedback resistors have ≤1% tolerances.

Base PWM Switching Frequency (R_{FSET})

The base PWM switching frequency is set by connecting a resistor from the FSET pin to ground. Figure 10 is a graph showing the relationship between the typical switching frequency (y-axis) and the FSET resistor (x-axis). For a particular base switching

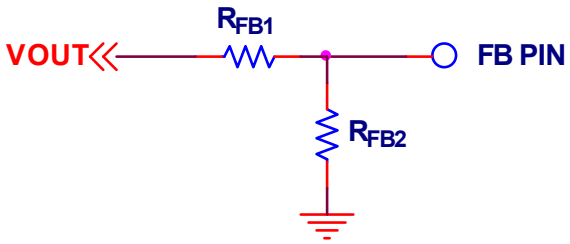

Figure 9. Connecting a feedback resistor divider

Table 2. Recommended Feedback Resistor Values

V_{OUT} (V)	R_{FB1} (VOUT to FB pin) (kΩ)	R_{FB2} (FB pin to GND) (kΩ)
1.2	6.04	12.1
1.5	7.50	8.45
1.8	9.09	7.15
2.5	12.4	5.76
3.3	16.5	5.23

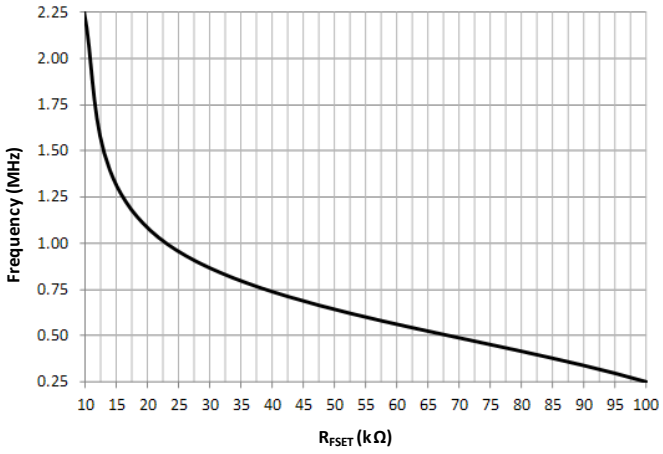

Figure 10. PWM switching frequency versus R_{FSET}

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frequency (f_{OSC}), the FSET resistor can be calculated as follows:

$$R_{FSET} = \left(\frac{24900}{f_{OSC}} - 1.7 \right) \quad (2)$$

where f_{OSC} is in kHz and R_{FSET} is in kΩ.

The oscillator frequency will be the final output switching frequency (unless the synchronization function is applied), so when the oscillator frequency is being chosen, the designer should be aware of the minimum controllable on-time, $t_{ON(MIN)}$, of the A8650. If the system required on-time is less than the A8650 minimum controllable on-time, then switch node jitter will occur and the output voltage will have increased ripple or oscillations.

The minimum oscillator frequency required should be calculated as follows:

$$f_{SWMAX} = \frac{V_{OUT}}{t_{ON(MIN)} \times V_{IN(MAX)}} \quad (3)$$

where

V_{OUT} is the output voltage,

$t_{ON(MIN)}$ is the minimum controllable on-time of the A8650 (worst case 105 ns), and

$V_{IN(MAX)}$ is the maximum required operational input voltage (not the peak surge voltage).

If the A8650 PWM synchronization function is employed, then the oscillator frequency should be chosen such that jitter will not result at the maximum synchronized switching frequency, determined from equation 3:

$$1.5 \times f_{SW} < f_{SWMAX} \quad (4)$$

Output Inductor (L_O)

When considering a peak current mode regulator, it is common knowledge that, without adequate slope compensation, the system will become unstable when the duty cycle is near or above 50%. However, the slope compensation in the A8650 is a fixed value (S_E). Therefore, it is important to calculate an inductor value so the falling slope of the inductor current (S_F) will work well with the A8650 slope compensation.

Equations 5 and 6 can be used to calculate a range of values for the output inductor based on the well-known approach of providing slope compensation that matches 50% to 100% of the falling slope of the inductor current:

$$\left(\frac{V_{OUT}}{2 \times S_E} \right) \leq L_O \leq \left(\frac{V_{OUT}}{S_E} \right) \quad (5)$$

where L_O is in µH.

In equation 5, the slope compensation (S_E) is a function of switching frequency, as follows:

$$S_E = 1.175 \times f_{OSC} \quad (6)$$

where S_E is in A/µs and f_{SW} is in MHz.

More recently, Dr. Raymond Ridley presented a formula to calculate the amount of slope compensation required to critically damp the double poles at half the PWM switching frequency:

$$L_O \geq \frac{V_{OUT}}{S_E} \left(1 - 0.18 \times \frac{V_{IN}(min)}{V_{OUT}} \right) \quad (7)$$

This formula allows the inclusion of the duty cycle (D), which should be calculated at the minimum input voltage to ensure optimal stability. Also, to avoid dropout (that is, saturation of the buck regulator), V_{IN}(min) must be approximately 0.75 to 1.0 V above V_{OUT} when calculating the inductor value with equation 7.

If equations 6 or 7 yield an inductor value that is not a standard value, then the next closest available value should be used. The final inductor value should allow for 10% to 20% of initial tolerance and 10% to 20% of inductor saturation.

The saturation current of the inductor should be higher than the peak current capability of the A8650. Ideally, for output short circuit conditions, the inductor should not saturate even at the highest cycle-by-cycle current limit at minimum duty cycle ($I_{LIM(5\%)}$; 4.7 A(max)). This may be too costly. At the very least, the inductor should not saturate given the peak operating current according to the following equation:

$$I_{PEAK} = 4.1 - \frac{S_E \times (V_{OUT})}{1.15 \times f_{SW} \times V_{IN}(max)} \quad (8)$$

where V_{IN}(max) is the maximum continuous input voltage, such as 5.5 V.

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Starting with equation 8, and subtracting half of the inductor ripple current, provides us with an interesting equation to predict the typical DC load capability of the regulator at a given duty cycle (D):

$$I_{OUT(DC)} = 4.1 - \frac{S_E \times D}{f_{SW}} - \frac{V_{OUT} \times (1 - D)}{2 \times f_{SW} \times L_O} \quad (9)$$

where D is V_{OUT}/V_{IN}. After an inductor is chosen, it should be tested during output short circuit conditions. The inductor current should be monitored using a current probe. A good design would ensure neither the inductor nor the regulator are damaged when the output is shorted to ground at maximum input voltage and the highest expected ambient temperature.

Output Capacitors

The output capacitors filter the output voltage to provide an acceptable level of ripple voltage and they store energy to help maintain voltage regulation during a load transient. The voltage rating of the output capacitors must support the output voltage with sufficient design margin.

The output voltage ripple (ΔV_{OUT}) is a function of the output capacitor parameters: C_{OUT}, ESR_{COUT}, and ESL_{COUT}:

$$\Delta V_{OUT} = \Delta I_L \times ESR_{COUT} + \frac{V_{IN} - V_{OUT}}{L_O} \times ESL_{COUT} + \frac{\Delta I_L}{8 f_{SW} C_{OUT}} \quad (10)$$

The type of output capacitors will determine which terms of equation 10 are dominant. For ceramic output capacitors the ESR_{COUT} and ESL_{COUT} are virtually zero, so the output voltage ripple will be dominated by the third term of equation 10:

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 f_{SW} C_{OUT}} \quad (11)$$

To reduce the voltage ripple of a design using ceramic output capacitors, simply: increase the total capacitance, reduce the inductor current ripple (that is, increase the inductor value), or increase the switching frequency.

For electrolytic output capacitors the value of capacitance will be relatively high, so the third term in equation 10 will be very small. The output voltage ripple will be determined primarily by the first two terms of equation 10:

$$\Delta V_{OUT} = \Delta I_L \times ESR_{COUT} + \frac{V_{IN} - V_{OUT}}{L_O} \times ESL_{COUT} \quad (12)$$

To reduce the voltage ripple of a design using electrolytic output capacitors, simply: decrease the equivalent ESR_{COUT} and ESL_{COUT} by using a high(er) quality capacitor, or add more capacitors in parallel, or reduce the inductor current ripple (that is, increase the inductor value).

The ESR of some electrolytic capacitors can be quite high so we recommend choosing a quality capacitor that clearly documents the ESR or the total impedance in the data sheet. Also, the ESR of electrolytic capacitors usually increases significantly at cold ambients, as much as 10×, which increases the output voltage ripple and, in most cases, significantly reduces the stability of the system.

The transient response of the regulator depends on the number and type of output capacitors. In general, minimizing the ESR of the output capacitance will result in a better transient response. The ESR can be minimized by simply adding more capacitors in parallel or by using higher quality capacitors. At the instant of a fast load transient (di/dt), the output voltage will change by the amount

$$\Delta V_{OUT} = \Delta I_{LOAD} \times ESR_{COUT} + \frac{di}{dt} ESL_{COUT} \quad (13)$$

After the load transient occurs, the output voltage will deviate from its nominal value for a short time. This time will depend on the system bandwidth, the output inductor value, and output capacitance. Eventually, the error amplifier will bring the output voltage back to its nominal value.

The speed at which the error amplifier will bring the output voltage back to its setpoint will depend mainly on the closed-loop bandwidth of the system. A higher bandwidth usually results in a shorter time to return to the nominal voltage. However, a higher bandwidth system may be more difficult to obtain acceptable gain and phase margins. Selection of the compensation components (R_Z, C_Z, C_P) are discussed in more detail in the Compensation Components section of this datasheet.

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Input Capacitors

Three factors should be considered when choosing the input capacitors. First, they must be chosen to support the maximum expected input voltage with adequate design margin. Second, their rms current rating must be higher than the expected rms input current to the regulator. Third, they must have enough capacitance and a low enough ESR to limit the input voltage dv/dt to something much less than the hysteresis of the V_{IN} pin UVLO circuitry (200 mV (typ)) at maximum loading and minimum input voltage.

The input capacitor(s) must limit the voltage deviations at the VIN pin to something significantly less than the A8650 VIN pin UVLO hysteresis during maximum load and minimum input voltage. The minimum input capacitance can be calculated as follows:

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1-D)}{0.85 \times f_{SW} \times \Delta V_{IN(MIN)}} \quad (14)$$

where $\Delta V_{IN(MIN)}$ is chosen to be much less than the hysteresis of the VIN pin UVLO comparator ($\Delta V_{IN(MIN)} \leq 100$ mV is recommended), and f_{SW} is the nominal PWM output frequency.

The D × (1–D) term in equation 14 has an absolute maximum value of 0.25 at 50% duty cycle. So, for example, a very conservative design, based on: I_{OUT} = 2.0 A, f_{SW} = 85% of 2 MHz, D × (1–D) = 0.25, and ΔV_{IN} = 100 mV, yields:

$$C_{IN} \geq \frac{2.0\ (A) \times 0.25}{1.7\ (MHz) \times 100\ (mV)} = 2.9\ \mu F$$

The input capacitors must deliver the rms current according to:

$$I_{rms} = I_{OUT} \sqrt{D \times (1-D)} \quad (15)$$

where the duty cycle D = V_{OUT}/V_{IN}.

Figure 11 shows the normalized input capacitor rms current versus duty cycle. To use this graph, simply find the operational duty cycle (D) on the x-axis and determine the input/output current multiplier on the y-axis. For example, at a 20% duty cycle, the input/output current multiplier is 0.40. Therefore, if the regulator is delivering 2.0 A of steady-state load current, the input capacitor(s) must support 0.40 × 2.0 A or 0.8 A_{RMS}.

A good design should consider the DC-bias effect on a ceramic capacitor. As the applied voltage approaches the rated value, the capacitance value decreases. This effect is very pronounced with the Y5V and Z5U temperature characteristic devices (as much as 90% reduction) so these types should be avoided. The X5R and X7R type capacitors should be the primary choices due to their stability versus both DC bias and temperature.

For all ceramic capacitors, the DC bias effect is even more pronounced on smaller case sizes so a good design will use the largest affordable case size (such as 1206 or 1210). Also, it is advisable to select input capacitors with plenty of design margin in the voltage rating to accommodate the worst-case transient input voltage.

Soft Start and Hiccup Mode Timing (C_{SS})

The soft start time of the A8650 is determined by the value of the capacitance at the soft start pin, C_{SS}. When the A8650 is enabled the voltage at the soft start pin will start from 0 V and will be charged by the soft start current, I_{SSSU}. However, PWM switching will not begin instantly because the voltage at the soft start pin must rise above 200 mV. The soft start delay ($t_{SS(DELAY)}$) can be calculated using the following equation:

$$t_{SS(DELAY)} = C_{SS} \times \left(\frac{200\ (mV)}{I_{SSSU}} \right) \quad (16)$$

If the A8650 is starting into a very heavy load a very fast soft start time may cause the regulator to exceed the cycle-by-cycle overcurrent threshold. This occurs because the total of the full load current, the inductor ripple current, and the additional current required to charge the output capacitors:

$$I_{CO} = C_{OUT} \times V_{OUT} / t_{SS} \quad (17)$$

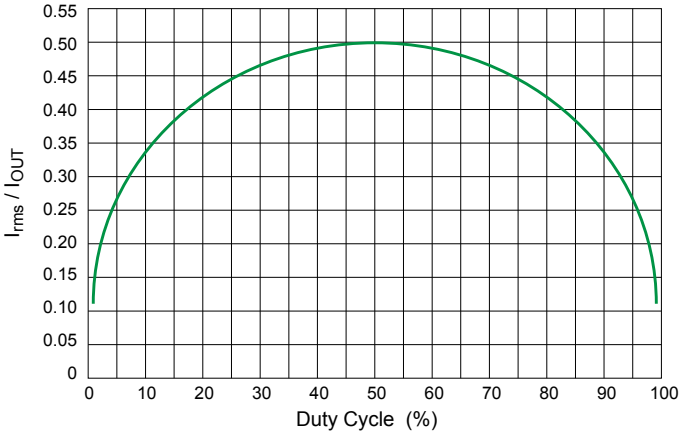

Figure 11. Input capacitor ripple versus duty cycle

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is higher than the cycle-by-cycle current threshold, as shown in figure 12. This phenomenon is more pronounced when using high value electrolytic type output capacitors. To avoid prematurely triggering hiccup mode the soft start capacitor, C_{SS}, should be calculated according to:

$$C_{SS} \geq \frac{I_{SSSU} \times V_{OUT} \times C_{OUT}}{0.8\ (V) \times I_{CO}} \quad (18)$$

where V_{OUT} is the output voltage, C_{OUT} is the output capacitance, I_{CO} is the amount of current allowed to charge the output capacitance during soft start (recommend 0.1 A < I_{CO} < 0.3 A). Higher values of I_{CO} result in faster soft start times. However, lower values of I_{CO} ensure that hiccup mode is not falsely triggered. Allegro recommends starting the design with an I_{CO} of 0.1 A and increasing it only if the soft start time is too slow. If a non-standard capacitor value for C_{SS} is calculated, the next larger value should be used.

The output voltage ramp time, t_{SS}, can be calculated by using either of the following methods:

$$t_{SS} = V_{OUT} \times \frac{C_{OUT}}{I_{CO}} \quad (19)$$

or

$$t_{SS} = 0.8\ (V) \times \frac{C_{SS}}{I_{SSSU}} \quad (20)$$

When the A8650 is in hiccup mode, the soft start capacitor is used as a timing capacitor and sets the hiccup period. The soft start pin charges the soft start capacitor with I_{SSSU} during a startup attempt, and discharges the same capacitor with I_{SSHIC} between startup attempts. Because the ratio I_{SSSU} / I_{SSHIC} is approximately 2:1, the time between hiccups will be about two times as long as the startup time. Therefore, the effective duty-cycle of the A8650 will be very low and the junction temperature will be kept low.

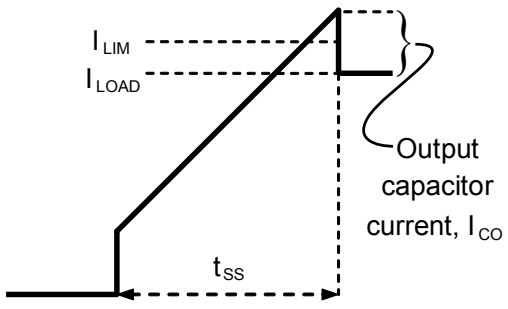

Figure 12. Output current (I_{CO}) during startup

Compensation Components (R_Z, C_Z, C_P)

To compensate the system, it is important to understand where the buck power stage, load resistance, and output capacitance form their poles and zeros in frequency. Also, its important to understand not only that the (Type II) compensated error amplifier introduces a zero and two more poles, but also where these should be placed to maximize system stability, provide a high bandwidth, and optimize the transient response.

First, consider the power stage of the A8650, the output capacitors, and the load resistance. This circuitry is commonly referred as the *control-to-output* (CO) transfer function. The low frequency gain of this circuitry depends on the COMP to SW current gain (g_{mPOWER}), and the value of the load resistor (R_L). The DC gain ($G_{CO(0HZ)}$) of the control-to-output is:

$$G_{CO(0Hz)} = g_{mPOWER} \times R_L \quad (21)$$

The control-to-output transfer function has a pole (f_{P1}), formed by the output capacitance (C_{OUT}) and load resistance (R_L), located at:

$$f_{P1} = \frac{1}{2\pi \times R_L \times C_{OUT}} \quad (22)$$

The control-to-output transfer function also has a zero (f_{Z1}) formed by the output capacitance (C_{OUT}) and its associated ESR:

$$f_{Z1} = \frac{1}{2\pi \times ESR \times C_{OUT}} \quad (23)$$

For a design with very low-ESR type output capacitors (such as ceramic capacitors), the ESR zero (f_{Z1}) is usually at a very high frequency, so it can be ignored. On the other hand, if the ESR zero falls below or near the 0 dB crossover frequency of the system (as is the case with electrolytic output capacitors), then it should be cancelled by the pole formed by the C_P capacitor and the R_Z resistor (discussed and identified later as f_{P3}).

A Bode plot of the control-to-output transfer function for the A8650 circuit shown in the typical application schematic on the front page (V_{OUT} = 1.8 V, I_{OUT} = 2.0 A, R_L = 0.9 Ω) is shown in figure 13. The pole at f_{P1} can easily be seen at 8.8 kHz while the ESR zero, f_{Z1}, occurs at a very high frequency, 4 MHz (this is

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typical for a design using ceramic output capacitors). Note, there is more than 90° of total phase shift because of the double-pole at half the switching frequency.

Next, consider the feedback resistor divider, (R_{FB1} and R_{FB2}), the error amplifier (g_m), and the compensation network R_Z C_Z C_P. It greatly simplifies the transfer function derivation if $R_O >> R_Z$, and $C_Z >> C_P$. In most cases, $R_O > 2$ MΩ, 1 kΩ < R_Z < 100 kΩ, 220 pF < C_Z < 47 nF, and C_P < 50 pF, so the following equations are very accurate.

The low frequency gain of the control section ($G_{C(0Hz)}$) is formed by the feedback resistor divider and the error amplifier. It can be calculated as:

$$G_{C(0Hz)} = \frac{R_{FB2}}{R_{FB1}+R_{FB2}} \times g_m \times R_O = \frac{V_{FB}}{V_{OUT}} \times g_m \times R_O = \frac{V_{FB}}{V_{OUT}} \times A_{VOL} \quad (24)$$

where

V_{OUT} is the output voltage,

V_{FB} is the reference voltage (0.8 V),

g_m is the error amplifier transconductance (750 µA/V), and

R_O is the error amplifier output impedance (A_{VOL}/g_m).

The transfer function of the Type-II compensated error amplifier has a (very) low frequency pole (f_{P2}) dominated by the output error amplifier output impedance (R_O) and the C_Z compensation capacitor:

$$f_{P2} = \frac{1}{2\pi \times R_O \times C_Z} \quad (25)$$

The transfer function of the Type-II compensated error amplifier also has frequency zero (f_{Z2}) dominated by the R_Z resistor and the C_Z capacitor:

$$f_{Z2} = \frac{1}{2\pi \times R_Z \times C_Z} \quad (26)$$

Lastly, the transfer function of the Type-II compensated error amplifier has a (very) high frequency pole (f_{P3}) dominated by the R_Z resistor and the C_P capacitor:

$$f_{P3} = \frac{1}{2\pi \times R_Z \times C_P} \quad (27)$$

A Bode plot of the error amplifier and its compensation network is shown in figure 14, f_{P2}, f_{P3}, and f_{Z2} are indicated on the magnitude plot. Notice that the zero (f_{Z2} at 16 kHz) has been placed so that it is just above the pole at f_{P1} previously shown in the control-to-output Bode plot at 8.8 kHz, figure 13. Placing f_{Z2} just above f_{P1} will result in excellent phase margin, but relatively slow transient recovery time, as will be shown later.

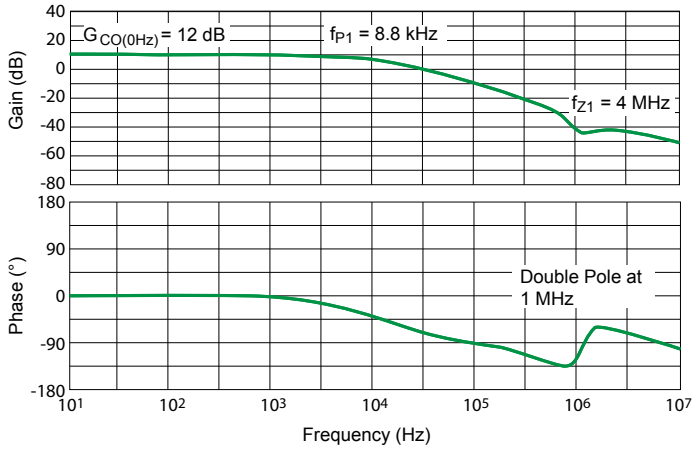

Figure 13. Control-to-Output Bode plot

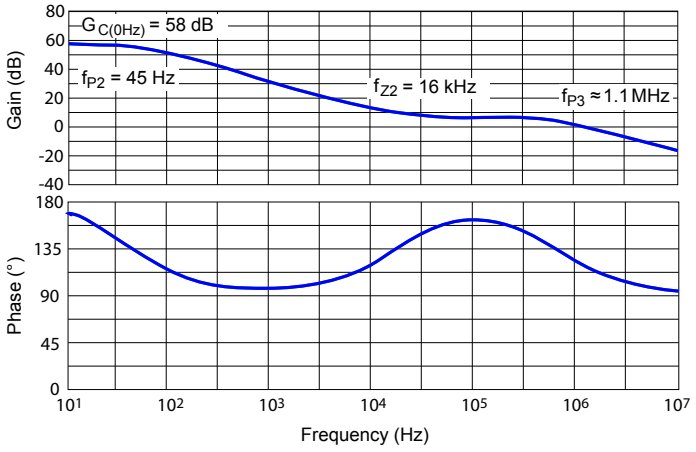

Figure 14. Type-II compensated error amplifier Bode plot

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Finally, consider the combined Bode plot of both the control-to-output and the compensated error amplifier, the red curve shown in figure 15. Careful examination of this plot shows that the magnitude and phase of the entire system (in red) are simply the sum of the error amplifier response (blue) and the control-to-output response (green). As shown in figure 15, the bandwidth of this system (f_c) is 72 kHz, the phase margin is 73 degrees, and the gain margin is 27 dB.

A Generalized Tuning Procedure

This section presents a methodology to systematically apply the design considerations provided above.

1. Choose the system bandwidth (f_C). This is the frequency at which the magnitude of the gain crosses 0 dB. Recommended values for f_C, based on the PWM switching frequency, are in the range $f_{SW} / 20 < f_C < f_{SW} / 7.5$. A higher value of f_C generally provides a better transient response, while a lower value of f_C generally makes it easier to obtain higher gain and phase margins.

2. Calculate the R_Z resistor value. This sets the system bandwidth (f_C):

$$R_Z = f_C \times \frac{V_{OUT}}{V_{FB}} \times \frac{2\pi \times C_{OUT}}{g_{mPOWERx} \times g_m} \quad (28)$$

3. Determine the frequency of the pole (f_{P1}). This pole is formed by C_{OUT} and R_L. Use equation 22 (repeated here):

$$f_{P1} = \frac{1}{2\pi \times R_L \times C_{OUT}}$$

4. Calculate a range of values for the C_Z capacitor. Use the following:

$$\frac{4}{2\pi \times R_Z \times f_C} < C_Z < \frac{1}{2\pi \times R_Z \times 1.5 \times f_{P1}} \quad (29)$$

To maximize system stability (that is, to have the greatest gain margin), use a higher value of C_Z. To optimize transient recovery time, although at the expense of some phase margin, use a lower value of C_Z.

Figure 16 compares the output voltage recovery time due to a 1 A load transient for the system shown in figure 15 (f_{Z2} = 16 kHz, 73° phase margin) and a system with f_{Z2} at 50 kHz. The system with f_{Z2} at 50 kHz has only 51° of phase margin, but recovers to within 0.5% much faster (≈3×) than the other system.

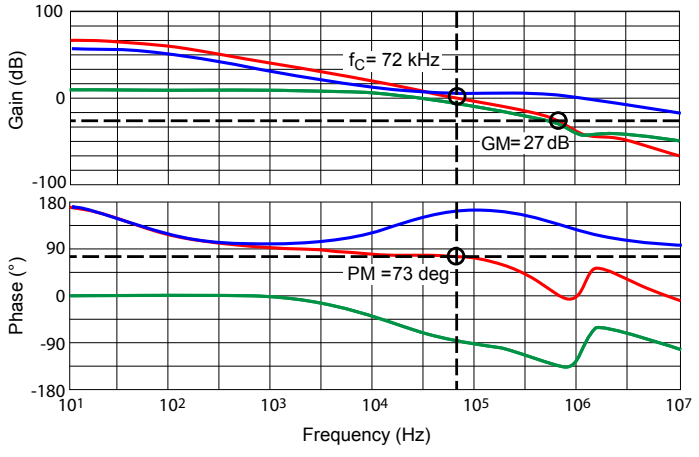

Figure 15. Bode plot of the complete system (red curve)

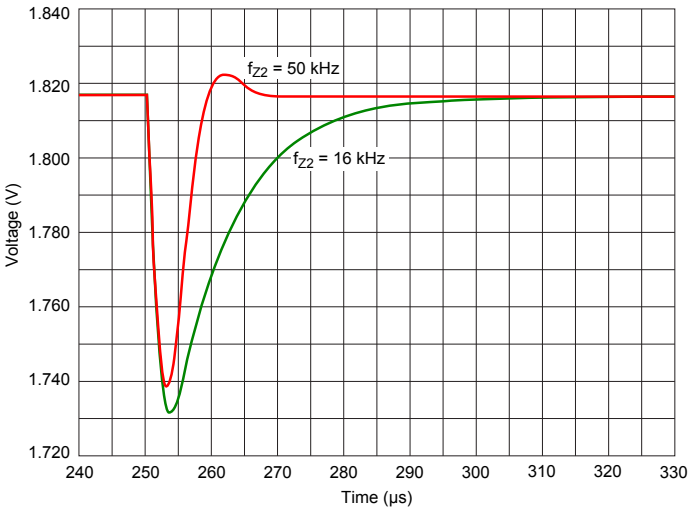

Figure 16. Transient recovery comparison for f_{Z2} at 16 kHz/73° and 50 kHz/51°

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5. Calculate the frequency of the ESR zero (f_{Z1}) formed by the output capacitor(s). Use equation 23 (repeated here):

$$f_{Z1} = \frac{1}{2\pi \times \text{ESR} \times C_{OUT}}$$

If f_{Z1} is at least one decade higher than the target crossover frequency (f_C) then f_{Z1} can be ignored. This is usually the case for a design using ceramic output capacitors. Use equation 27 to calculate the value of C_P by setting f_{P3} to either 5 × f_C or f_{SW} / 2, whichever is higher.

Alternatively, if f_{Z1} is near or below the target crossover frequency (f_C), then use equation 27 to calculate the value of C_P by setting f_{P3} equal to f_{Z1}. This is usually the case for a design using high ESR electrolytic output capacitors.

Power Dissipation and Thermal Calculations

The power dissipated in the A8650 is the sum of the power dissipated from the VIN supply current (P_{IN}), the power dissipated due to the switching of the internal power high-side MOSFET (P_{SW1}), the power dissipated due to the rms current being conducted by the high- and low-side MOSFETs (P_{COND1} and P_{COND2}), the power dissipated by the low-side MOSFET body diode during the non-overlap times, and the power dissipated by the internal gate drivers ($P_{DRIVER1}$ and $P_{DRIVER2}$).

The power dissipated from the VIN supply current can be calculated using the following equation:

$$P_{IN} = V_{IN} \times I_Q + (V_{IN} - V_{GS}) \times (Q_{G1} + Q_{G2}) \times f_{SW} \quad (30)$$

where

V_{IN} is the input voltage,
I_Q is the input quiescent current drawn by the A8650 (nominally 2 mA),
V_{GS} is the MOSFET gate drive voltage, typically 5.0 V,
Q_{G1} and Q_{G2} are the internal high- and low-side MOSFET gate charges (approximately 3.3 nC and 1.4 nC respectively), and
f_{SW} is the PWM switching frequency.

The switching losses dissipated by the internal high-side MOSFET during PWM switching can be calculated using the following equation:

$$P_{SW1} = \frac{V_{IN} \times I_{OUT} \times (t_r + t_f) \times f_{SW}}{2} \quad (31)$$

where

V_{IN} is the input voltage,
I_{OUT} is the output current,
f_{SW} is the PWM switching frequency, and
t_r and t_f are the rise and fall times measured at the SW node. Approximate values for t_r range from 10 to 15 ns. The fall time is usually about 50% faster than the rise time.

The conduction losses dissipated by the high-side MOSFET while it is conducting can be calculated using the following equation:

$$P_{COND1} = I^2_{rms(FET)} \times R_{DS(on)HS} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(I^2_{OUT} + \frac{\Delta I_L^2}{12}\right) \times R_{DS(on)HS} \quad (32)$$

where

I_{OUT} is the regulator output current,
ΔI_L is the peak-to-peak inductor ripple current, and
$R_{DS(on)HS}$ is the on-resistance of the high-side MOSFET.

The conduction losses dissipated by the low-side MOSFET while it is conducting can be calculated using the following equation:

$$P_{COND2} = I^2_{rms(FET)} \times R_{DS(on)LS} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(I^2_{OUT} + \frac{\Delta I_L^2}{12}\right) \times R_{DS(on)LS} \quad (33)$$

where

I_{OUT} is the regulator output current,
ΔI_L is the peak-to-peak inductor ripple current, and
$R_{DS(on)LS}$ is the on-resistance of the low-side MOSFET.

The $R_{DS(on)}$of the MOSFETs has some initial tolerance plus an increase from self-heating and elevated ambient temperatures. A conservative design should accommodate an $R_{DS(on)}$ with at least a 15% initial tolerance plus 0.39%/°C increase due to temperature.

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The power dissipated by the low-side MOSFET body diode during the non-overlap time can be calculated as follows:

$$P_{NO} = V_{SD} \times I_{OUT} \times 2 \times t_{NO} \times f_{SW} \quad (34)$$

where

V_{SD} is the source-to-drain voltage of the low-side MOSFET (typically 0.60 V), and
t_{NO} is the non-overlap time (15 ns (typ)).

The power dissipated by the internal gate drivers can be calculated using the following equation:

$$P_{DRIVERS} = (Q_{G1} + Q_{G2}) \times V_{GS} \times f_{SW} \quad (35)$$

where

Q_{G1} and Q_{G2} are the internal gate charges to drive the high- and low-side MOSFETs to V_{GS} (approximately 3.3 nC and 1.4 nC at 5 V, respectively), and
f_{SW} is the PWM switching frequency.

Finally, the total power dissipated by the A8650 (P_{TOTAL}) is the sum of the previous equations:

$$P_{TOTAL} = P_{IN} + P_{SW1} + P_{COND1} + P_{COND2} + P_{NO} + P_{DRIVERS} \quad (36)$$

The average junction temperature can be calculated with the following equation:

$$T_J = P_{TOTAL} \times R_{\theta JA} + T_A \quad (37)$$

where

P_{TOTAL} is the total power dissipated as described in equation 36,
$R_{\theta JA}$ is the junction-to-ambient thermal resistance (48°C/W on a 4-layer PCB), and
T_A is the ambient temperature.

The maximum junction temperature will be dependent on how efficiently heat can be transferred from the PCB to ambient air. It is critical that the thermal pad on the bottom of the IC should be connected to a at least one ground plane using multiple vias.

As with any regulator, there are limits to the amount of heat that can be dissipated before risking thermal shutdown. There are trade-offs between: ambient operating temperature, input voltage, output voltage, output current, switching frequency, PCB thermal resistance, airflow, and other nearby heat sources. Even a small amount of airflow will reduce the junction temperature considerably.

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PCB Component Placement and Routing

A good PCB layout is critical if the A8650 is to provide clean, stable output voltages. Follow these guidelines to ensure a good PCB layout. Figure 17 shows a typical synchronous buck regulator schematic with the critical power paths/loops. Figure 18 shows an example PCB component placement and routing with the same critical power paths/loops as shown in the schematic.

1. Place the ceramic input capacitors as close as possible to the VIN pin and ground the capacitors at the PGND pin. The ceramic input capacitors and the A8650 must be on the same layer. Connect the input capacitors, the VIN pin, and the PGND pin with a wide trace. This critical loop is shown as trace 1 in figures 17 and 18.

2. Place the output inductor (L_O) as close as possible to the SW pin. The output inductor and the A8650 must be on the same layer. Connect the SW pin to the output inductor with a relatively wide trace or polygon. For EMI/EMC reasons, its best to minimize the area of this trace/polygon. This critical trace is shown as trace 2 in figure 17. Also, keep low-level analog signals (like FB and COMP) away from the SW metal.

3. Place the output capacitors relatively close to the output inductor and the A8650. Ideally, the output capacitors, output inductor and the A8650 should be on the same layer. Connect the output inductor and the output capacitors with a fairly wide trace. The output capacitors must use a ground plane to make a very low-inductance connection back to the PGND pin. These critical connections are shown as trace 3 in figures 17 and 18.

4. Place the feedback resistor divider (R_{FB1} and R_{FB2}) very close to the FB pin. Orient R_{FB2} such that the ground side is as close as possible to the A8650.

5. Place the compensation components (R_Z, C_Z, and C_P) as close as possible to the COMP pin. Orient C_Z and C_P such that their ground connections are as close as possible to the A8650.

6. Place and ground the FSET resistor as close as possible to the FSET pin.

7. The output voltage sense trace (from VOUT to R_{FB1}) should be connected as close as possible to the load to obtain the best load regulation.

8. The thermal pad under the IC should be connected to a ground plane (preferably on the top and bottom layers) with as many vias as possible. Allegro recommends vias with an approximately 0.25 to 0.30 mm hole and a 0.13 to 0.18 mm ring.

9. Place the soft start capacitor (C_{SS}) as close as possible to the SS pin. Place a via to the GND plane as close as possible to this component.

10. When connecting the input and output ceramic capacitors to a power or ground plane, use multiple vias and place the vias as close as possible to the component pads. Do not use thermal reliefs (spokes) around the pads for the input and output ceramic capacitors.

11. EMI/EMC issues are always a concern. Allegro recommends having locations for an RC snubber from SW to ground. The snubber components can be placed on the back of the PCB and populated only if necessary. The resistor should be 0805 or 1206 size.

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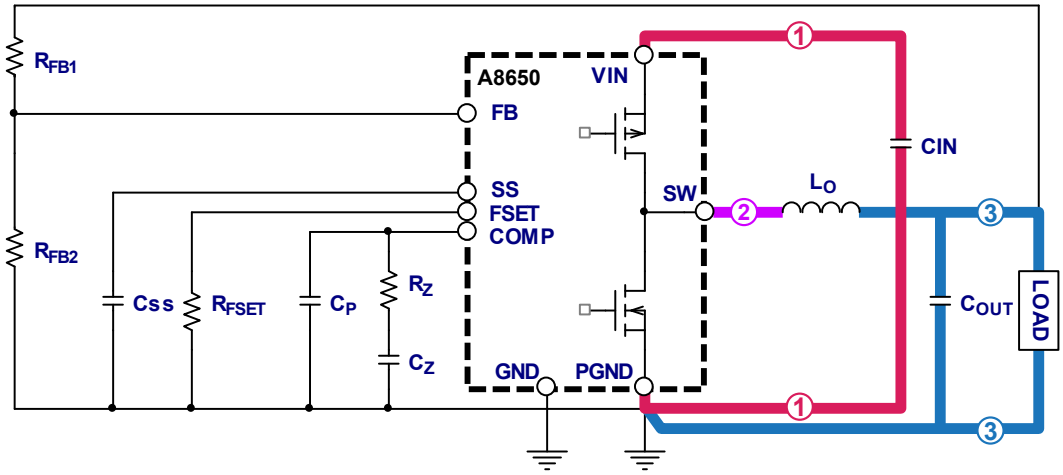

Figure 17. Typical synchronous buck converter with critical paths/loops shown; a single-point ground is recommended, which could be the exposed thermal pad, under the IC

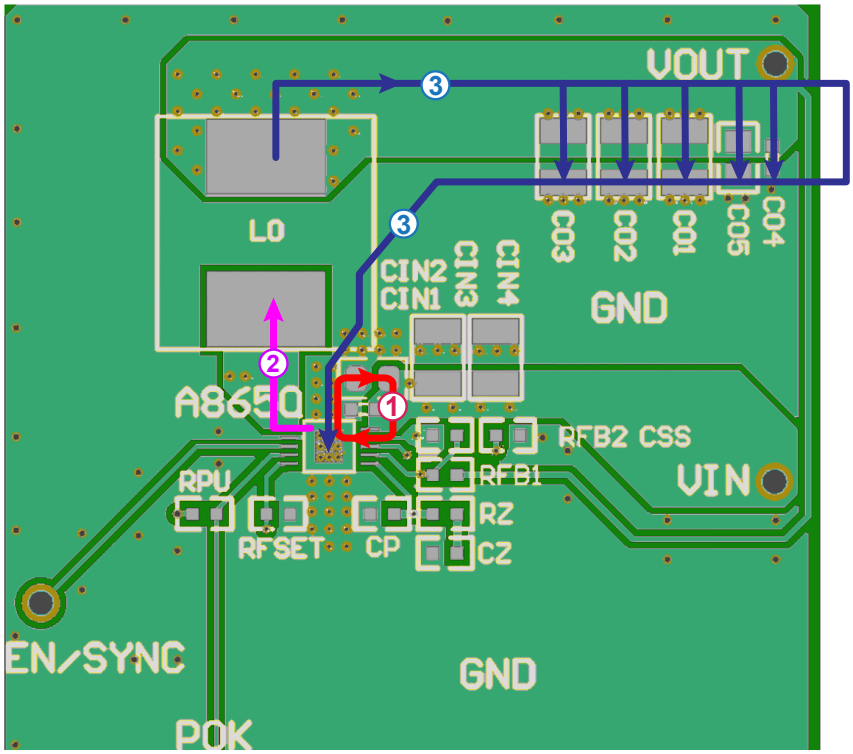

Figure 18. Example PCB component placement and routing

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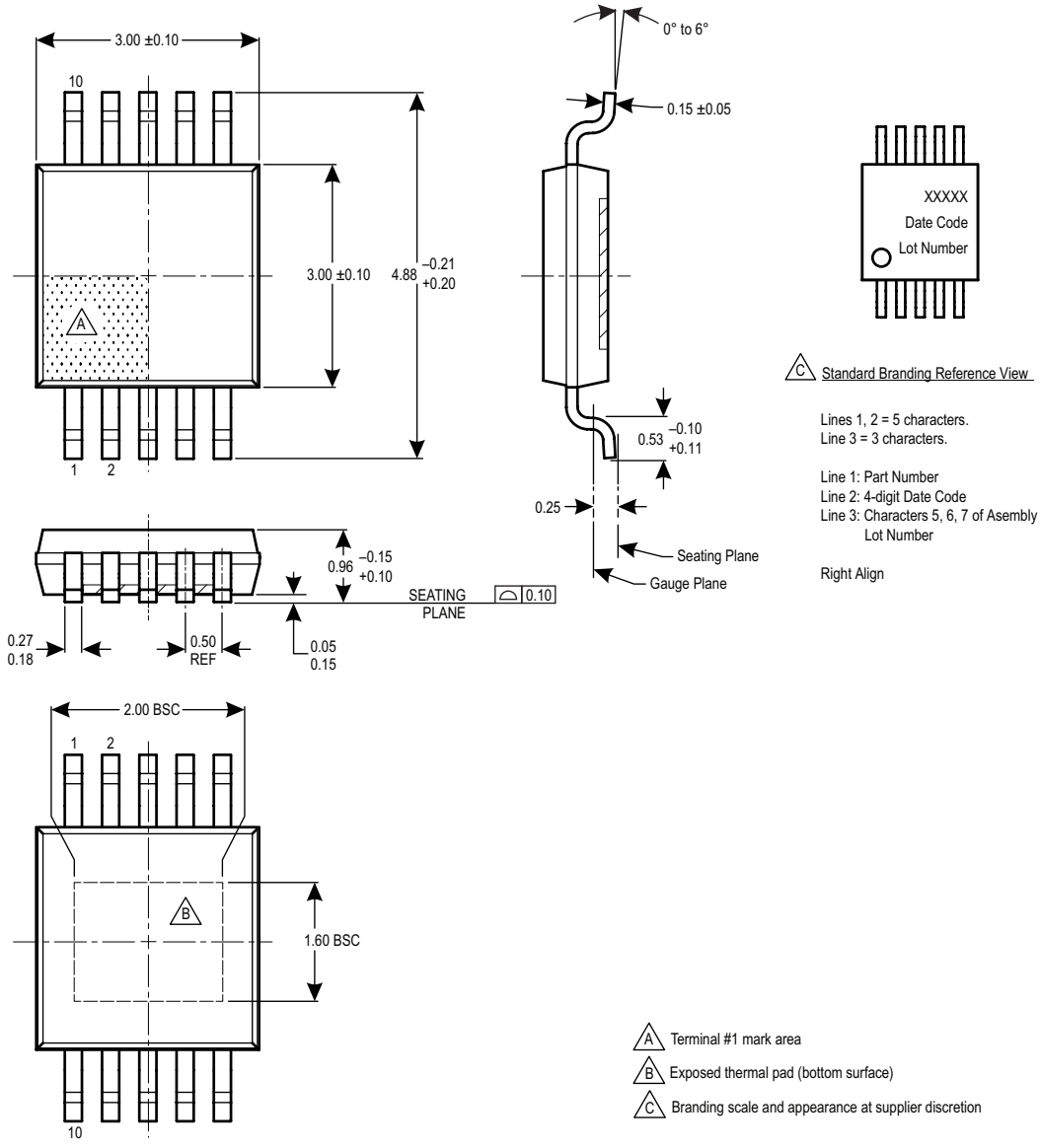
(Reference Allegro DWG-0000390, Rev. 2 and JEDEC MO-187)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



Package LY, 10-Pin MSOP
with Exposed Thermal Pad

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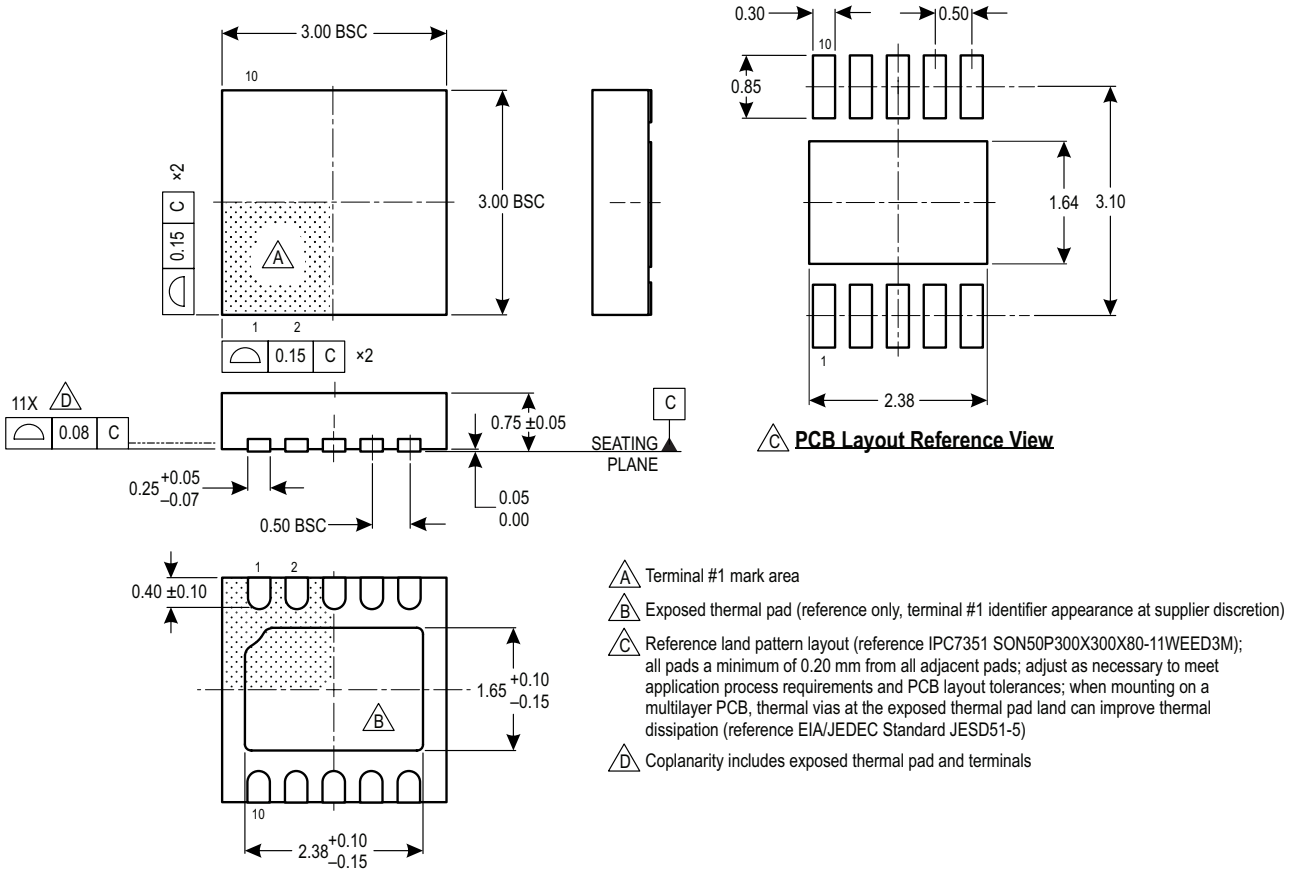
(Reference DWG-0000372)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P300X300X80-11WEED3M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Package EJ, 10-Pin DFN
with Exposed Thermal Pad

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REVISION HISTORY

Number	Date	Description
6	January 13, 2014	Miscellaneous conforming edits
7	October 27, 2014	Revised equation 7
8	November 20, 2015	Added EJ 10-Pin DFN Package
9	April 22, 2020	Minor editorial updates
10	June 11, 2021	Updated Package Outline Drawings (page 29-30)
11	November 2, 2023	Corrected package drawing (page 30)

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