THE DATASHEET OF

ASEK759ECB-200B-T-DK

ACS759xCB

Thermally Enhanced, Fully Integrated, Hall-Effect-Based Linear Current Sensor IC with 100 µΩ Current Conductor and Optimized Performance at 3.3 V

FEATURES AND BENEFITS

- Industry-leading noise performance through proprietary amplifier and filter design techniques
- Integrated shield greatly reduces capacitive coupling from current conductor to die due to high dV/dt signals, and prevents offset drift in high-side, high-voltage applications
- Total output error improvement through gain and offset trim over temperature
- Small package size, with easy mounting capability
- Monolithic Hall IC for high reliability
- Ultralow power loss: 100 µΩ internal conductor resistance
- Galvanic isolation allows use in economical, high-side current sensing in high-voltage systems

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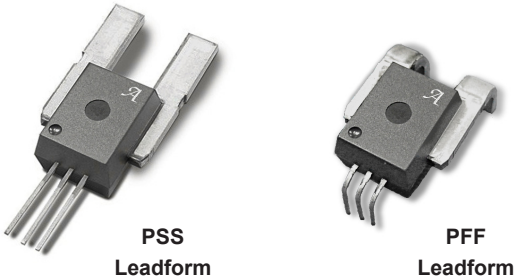
TÜV America Certificate Number: U8V 15 05 54214 037

UL Certified File No.: US-29755-UL

PACKAGE: 5-Pin CB Package



PSS Leadform **PFF Leadform**

Additional leadforms available for qualifying volumes

DESCRIPTION

The Allegro™ ACS759 family of current sensor ICs provides economical and precise solutions for AC or DC current sensing. Typical applications include motor control, load detection and management, power supply and DC-to-DC converter control, inverter control, and overcurrent fault detection.

The device consists of a precision, low-offset linear Hall circuit with a copper conduction path located near the die. Applied current flowing through this copper conduction path generates a magnetic field which the Hall IC converts into a proportional voltage. Device accuracy is optimized through the close proximity of the magnetic signal to the Hall transducer. A precise, proportional output voltage is provided by the low-offset, chopper-stabilized BiCMOS Hall IC, which is programmed for accuracy at the factory.

High-level immunity to current conductor dV/dt and stray electric fields, offered by Allegro proprietary integrated shield technology, for low output voltage ripple and low offset drift in high-side, high-voltage applications.

The output of the device has a positive slope ($>V_{CC}/2$) when an increasing current flows through the primary copper conduction path (from terminal 4 to terminal 5), which is the path used for current sampling. The internal resistance of this conductive path is 100 µΩ typical, providing low power loss.

The thickness of the copper conductor allows survival of the device at high overcurrent conditions. The terminals of the conductive path are electrically isolated from the signal leads

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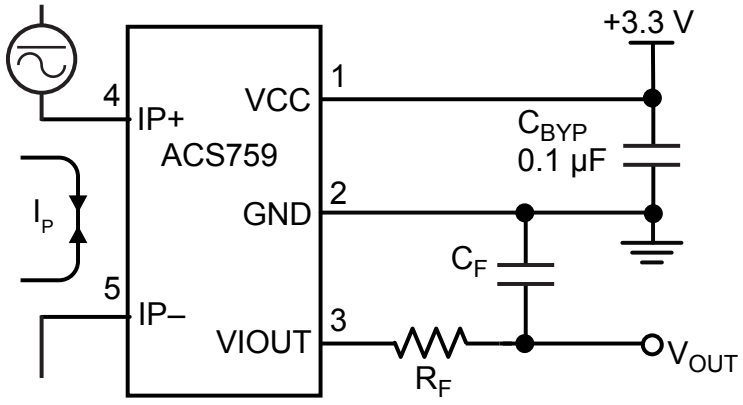

Application 1: The ACS759 outputs an analog signal, V_{OUT}, that varies linearly with the bidirectional AC or DC primary current, I_P, within the range specified. C_F is for optimal noise management, with values that depend on the application.

Typical Application

FEATURES AND BENEFITS (continued)

- 3.0 to 3.6 V, single supply operation
- 120 kHz typical bandwidth
- 3 µs output rise time in response to step input current
- Output voltage proportional to AC or DC currents
- Factory-trimmed for accuracy
- Extremely stable output offset voltage
- Nearly zero magnetic hysteresis

DESCRIPTION (continued)

(pins 1 through 3). This allows the ACS759 family of sensor ICs to be used in applications requiring electrical isolation without the use of opto-isolators or other costly isolation techniques.

The device is fully calibrated prior to shipment from the factory. The ACS759 family is lead (Pb) free. All leads are plated with 100% matte tin, and there is no Pb inside the package. The heavy gauge leadframe is made of oxygen-free copper.

SELECTION GUIDE

Part Number [1]	Package		Primary Sampled Current, I_P (A)	Sensitivity Sens (Typ.) (mV/A) [2]	Current Directionality	T_{OP} (°C)	Packing [3]
	Terminals	Signal Pins					
ACS759LCB-050B-PFF-T	Formed	Formed	±50	26.4	Bidirectional	–40 to 150	34 pieces per tube
ACS759LCB-100B-PFF-T	Formed	Formed	±100	13.2	Bidirectional		
ACS759KCB-150B-PFF-T	Formed	Formed	±150	8.8	Bidirectional	–40 to 125	
ACS759KCB-150B-PSS-T	Straight	Straight	±150	8.8	Bidirectional		
ACS759ECB-200B-PFF-T	Formed	Formed	±200	6.6	Bidirectional	–40 to 85	
ACS759ECB-200B-PSS-T	Straight	Straight	±200	6.6	Bidirectional		

[1] Additional leadform options available for qualified volumes.
[2] With V_{CC} = 3.3 V.
[3] Contact Allegro for additional packing options.

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		8	V
Reverse Supply Voltage	V_{RCC}		–0.5	V
Forward Output Voltage	V_{IOUT}		28	V
Reverse Output Voltage	V_{RIOUT}		–0.5	V
Output Source Current	$I_{OUT(Source)}$	VIOUT to GND	3	mA
Output Sink Current	$I_{OUT(Sink)}$	VCC to VIOUT	1	mA
Nominal Operating Ambient Temperature	T_{OP}	Range E	–40 to 85	°C
		Range K	–40 to 125	°C
		Range L	–40 to 150	°C
Maximum Junction	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 165	°C

ISOLATION CHARACTERISTICS

Characteristic	Symbol	Notes	Rating	Unit
Dielectric Strength Test Voltage*	V_{ISO}	Agency type-tested for 60 seconds per UL standard 60950-1, 2nd Edition	4800	VAC
Working Voltage for Basic Isolation	V_{WFSI}	For basic (single) isolation per UL standard 60950-1, 2nd Edition	990	VDC or V_{pk}
			700	V_{rms}
Working Voltage for Reinforced Isolation	V_{WFRI}	For reinforced (double) isolation per UL standard 60950-1, 2nd Edition	636	VDC or V_{pk}
			450	V_{rms}

* Allegro does not conduct 60-second testing. It is done only during the UL certification process.

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THERMAL CHARACTERISTICS: May require derating at maximum conditions

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Mounted on the Allegro evaluation board with 2800 mm^2 (1400 mm^2 on component side and 1400 mm^2 on opposite side) of 4 oz. copper connected to the primary leadframe and with thermal vias connecting the copper layers. Performance is based on current flowing through the primary leadframe and includes the power consumed by the PCB.	7	°C/W

[1] Additional thermal information available on the Allegro website.

TYPICAL OVERCURRENT CAPABILITIES [2][3]

Characteristic	Symbol	Notes	Rating	Unit
Overcurrent	I_{POC}	T_A = 25°C, 1 second duration, 1% duty cycle	1200	A
		T_A = 85°C, 1 second duration, 1% duty cycle	900	A
		T_A = 150°C, 1 second duration, 1% duty cycle	600	A

[2] Test was done with Allegro evaluation board. The maximum allowed current is limited by T_J(max) only.
[3] For more overcurrent profiles, please see FAQ on the Allegro website, www.allegromicro.com.

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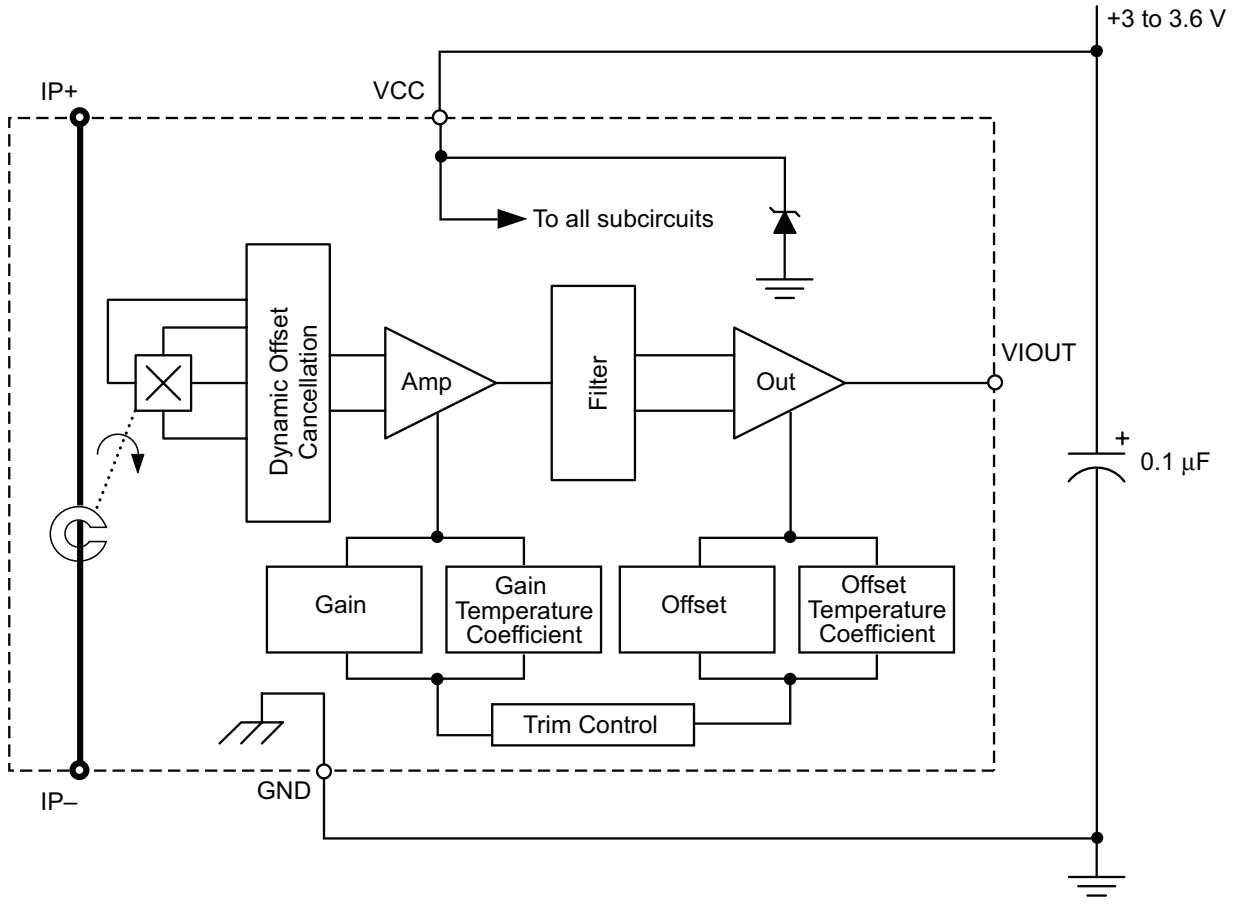
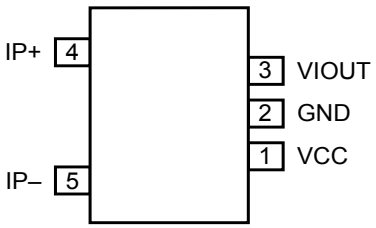


Functional Block Diagram



Pinout Diagram

Terminal List

Number	Name	Description
1	VCC	Device power supply terminal
2	GND	Signal ground terminal
3	VIOUT	Analog output signal
4	IP+	Terminal for current being sampled
5	IP–	Terminal for current being sampled

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COMMON OPERATING CHARACTERISTICS [1]: Valid at T_{OP} = –40°C to 150°C and V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		3	3.3	3.6	V
Supply Current	I_{CC}	Output open	–	10	13.5	mA
Power-On Delay	t_{POD}	T_A = 25°C	–	10	–	µs
Rise Time [2]	t_r	I_P step = 60% of I_P+, 10% to 90% rise time, T_A = 25°C, C_{OUT} = 0.47 nF	–	3	–	µs
Propagation Delay Time [2]	t_{PROP}	T_A = 25°C, C_{OUT} = 0.47 nF	–	1	–	µs
Response Time	$t_{RESPONSE}$	Measured as sum of t_{PROP} and t_r	–	4	–	µs
Internal Bandwidth [3]	BW_i	–3 dB; T_A = 25°C, C_{OUT} = 0.47 nF	–	120	–	kHz
Output Load Resistance	$R_{LOAD(MIN)}$	VIOUT to GND	4.7	–	–	kΩ
Output Load Capacitance	$C_{LOAD(MAX)}$	VIOUT to GND	–	–	10	nF
Primary Conductor Resistance	$R_{PRIMARY}$	T_A = 25°C	–	100	–	µΩ
Symmetry [2]	E_{SYM}	Over half-scale of I_P	–	100	–	%
Quiescent Output Voltage [4]	$V_{IOUT(Q)}$	I_P = 0 A, T_A = 25°C	–	V_{CC}/2	–	V
Ratiometry [2]	V_{RAT}	V_{CC} = 3 to 3.6 V	–	100	–	%

[1] Device is factory-trimmed at 3.3 V, for optimal accuracy.
[2] See Characteristic Definitions section of this datasheet.
[3] Calculated using the formula BW_i = 0.35 / t_r.
[4] $V_{IOUT(Q)}$ may drift over the lifetime of the device by as much as ±20 mV.

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*X*050B PERFORMANCE CHARACTERISTICS [1]: T_{OP} = –40°C to 150°C, V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Primary Sampled Current	I_P		–50	–	50	A
Sensitivity	$Sens_{TA}$	Full scale of I_P applied for 5 ms, T_A = 25°C	–	26.4	–	mV/A
	$Sens_{(TOP)HT}$	Full scale of I_P applied for 5 ms, T_{OP} = 25°C to 150°C	–	26.5	–	mV/A
	$Sens_{(TOP)LT}$	Full scale of I_P applied for 5 ms, T_{OP} = –40°C to 25°C	–	26	–	mV/A
Noise [2]	V_{NOISE}	T_A= 25°C, 10 nF on VIOUT pin to GND	–	6.6	–	mV
Nonlinearity	E_{LIN}	Up to full scale of I_P, I_P applied for 5 ms	–	<±1	–	%
Electrical Offset Voltage [3]	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–	±5	–	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 150°C	–	±10	–	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –40°C to 25°C	–	±25	–	mV
Magnetic Offset Error	I_{ERROM}	I_P = 0 A, T_A = 25°C, after excursion of 50 A	–	125	–	mA
Total Output Error [4]	$E_{TOT(HT)}$	Over full scale of I_P, I_P applied for 5 ms, T_{OP} = 25°C to 150°C	–	±1.5	–	%
	$E_{TOT(LT)}$	Over full scale of I_P, I_P applied for 5 ms, T_{OP} = –40°C to 25°C	–	±3.5	–	%

[1] See Characteristic Performance Data page for parameter distributions over temperature range.
[2] ±3 sigma noise voltage.
[3] $V_{OE(TOP)}$ drift is referred to ideal $V_{IOUT(Q)} = {}^1/_2\ V_{CC}$.
[4] Percentage of I_P. Output filtered.

*X*100B PERFORMANCE CHARACTERISTICS [1]: T_{OP} = –40°C to 150°C, V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Primary Sampled Current	I_P		–100	–	100	A
Sensitivity	$Sens_{TA}$	Full scale of I_P applied for 5 ms, T_A = 25°C	–	13.2	–	mV/A
	$Sens_{(TOP)HT}$	Full scale of I_P applied for 5 ms, T_{OP} = 25°C to 150°C	–	13.2	–	mV/A
	$Sens_{(TOP)LT}$	Full scale of I_P applied for 5 ms, T_{OP} = –40°C to 25°C	–	13	–	mV/A
Noise [2]	V_{NOISE}	T_A= 25°C, 10 nF on VIOUT pin to GND	–	4	–	mV
Nonlinearity	E_{LIN}	Up to full scale of I_P, I_P applied for 5 ms	–	<±1	–	%
Electrical Offset Voltage [3]	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–	±5	–	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 150°C	–	±10	–	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –40°C to 25°C	–	±25	–	mV
Magnetic Offset Error	I_{ERROM}	I_P = 0 A, T_A = 25°C, after excursion of 100 A	–	185	–	mA
Total Output Error [4]	$E_{TOT(HT)}$	Over full scale of I_P, I_P applied for 5 ms, T_{OP} = 25°C to 150°C	–	±1.8	–	%
	$E_{TOT(LT)}$	Over full scale of I_P, I_P applied for 5 ms, T_{OP} = –40°C to 25°C	–	±4	–	%

[1] See Characteristic Performance Data page for parameter distributions over temperature range.
[2] ±3 sigma noise voltage.
[3] $V_{OE(TOP)}$ drift is referred to ideal $V_{IOUT(Q)} = {}^1/_2\ V_{CC}$.
[4] Percentage of I_P. Output filtered.

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*X*150B PERFORMANCE CHARACTERISTICS [1]: T_{OP} = –40°C to 125°C, V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Primary Sampled Current	I_P		–150	–	150	A
Sensitivity	$Sens_{TA}$	Full scale of I_P applied for 5 ms, T_A = 25°C	–	8.7	–	mV/A
	$Sens_{(TOP)HT}$	Full scale of I_P applied for 5 ms, T_{OP} = 25°C to 125°C	–	8.8	–	mV/A
	$Sens_{(TOP)LT}$	Full scale of I_P applied for 5 ms, T_{OP} = –40°C to 25°C	–	8.6	–	mV/A
Noise [2]	V_{NOISE}	T_A= 25°C, 10 nF on VIOUT pin to GND	–	3	–	mV
Nonlinearity	E_{LIN}	Up to full scale of I_P, I_P applied for 5 ms	–	<±1	–	%
Electrical Offset Voltage [3]	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–	±5	–	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 125°C	–	±5	–	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –40°C to 25°C	–	±10	–	mV
Magnetic Offset Error	I_{ERROM}	I_P = 0 A, T_A = 25°C, after excursion of 150 A	–	235	–	mA
Total Output Error [4]	$E_{TOT(HT)}$	Over full scale of I_P, I_P applied for 5 ms, T_{OP} = 25°C to 125°C	–	±2	–	%
	$E_{TOT(LT)}$	Over full scale of I_P, I_P applied for 5 ms, T_{OP} = –40°C to 25°C	–	±4	–	%

[1] See Characteristic Performance Data page for parameter distributions over temperature range.
[2] ±3 sigma noise voltage.
[3] $V_{OE(TOP)}$ drift is referred to ideal $V_{IOUT(Q)} = {}^1/_2\ V_{CC}$.
[4] Percentage of I_P. Output filtered.

*X*200B PERFORMANCE CHARACTERISTICS[1]: T_{OP} = –40°C to 85°C, V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Primary Sampled Current	I_P		–200	–	200	A
Sensitivity	$Sens_{TA}$	Full scale of I_P applied for 5 ms, T_A = 25°C	–	6.6	–	mV/A
	$Sens_{(TOP)HT}$	Full scale of I_P applied for 5 ms, T_{OP} = 25°C to 85°C	–	6.7	–	mV/A
	$Sens_{(TOP)LT}$	Full scale of I_P applied for 5 ms, T_{OP} = –40°C to 25°C	–	6.5	–	mV/A
Noise [2]	V_{NOISE}	T_A= 25°C, 10 nF on VIOUT pin to GND	–	2	–	mV
Nonlinearity	E_{LIN}	Up to full scale of I_P, I_P applied for 5 ms	–	<±1	–	%
Electrical Offset Voltage [3]	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–	±5	–	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 85°C	–	±5	–	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –40°C to 25°C	–	±10	–	mV
Magnetic Offset Error	I_{ERROM}	I_P = 0 A, T_A = 25°C, after excursion of 200 A	–	268	–	mA
Total Output Error [4]	$E_{TOT(HT)}$	Over full scale of I_P, I_P applied for 5 ms, T_{OP} = 25°C to 85°C	–	±2	–	%
	$E_{TOT(LT)}$	Over full scale of I_P, I_P applied for 5 ms, T_{OP} = –40°C to 25°C	–	±4	–	%

[1] See Characteristic Performance Data page for parameter distributions over temperature range.
[2] ±3 sigma noise voltage.
[3] $V_{OE(TOP)}$ drift is referred to ideal $V_{IOUT(Q)} = {}^1/_2\ V_{CC}$.
[4] Percentage of I_P. Output filtered.

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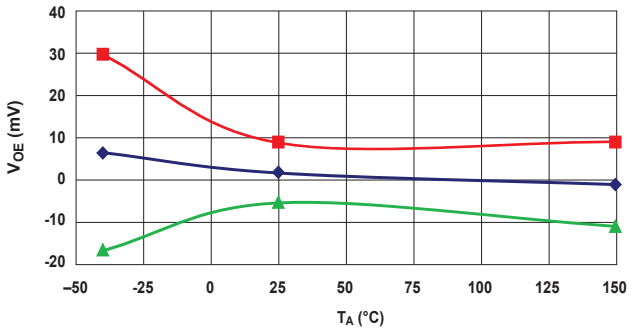
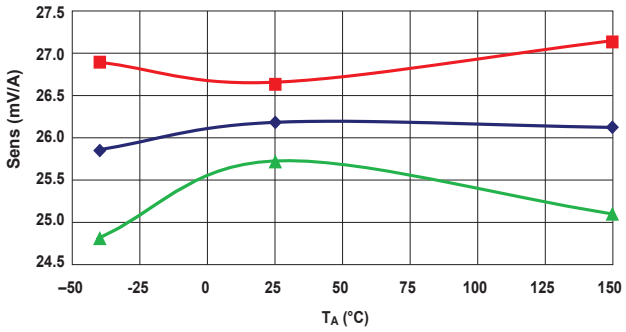
CHARACTERISTIC PERFORMANCE DATA
Data taken using the ACS759LCB-050B

Accuracy Data

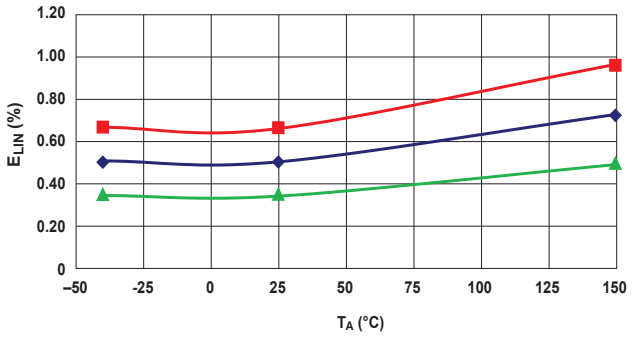
Electrical Offset Voltage versus Ambient Temperature



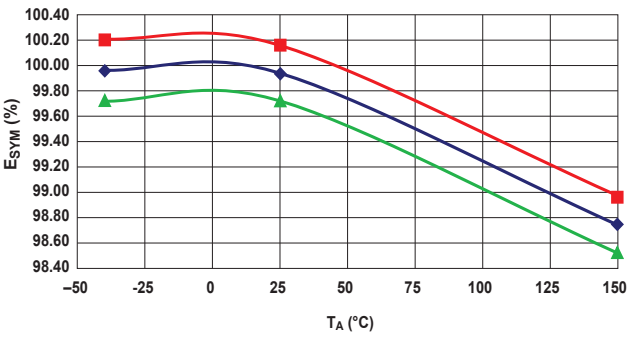
Sensitivity versus Ambient Temperature



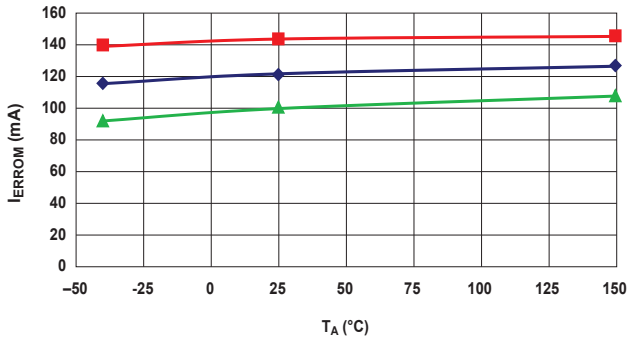
Nonlinearity versus Ambient Temperature



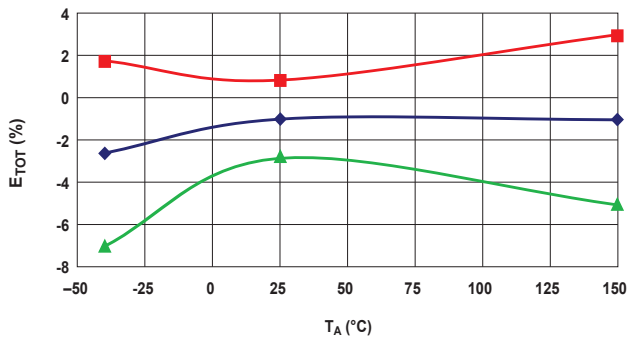
Symmetry versus Ambient Temperature

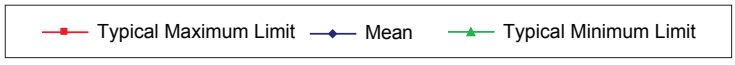


Magnetic Offset Error versus Ambient Temperature



Total Output Error versus Ambient Temperature





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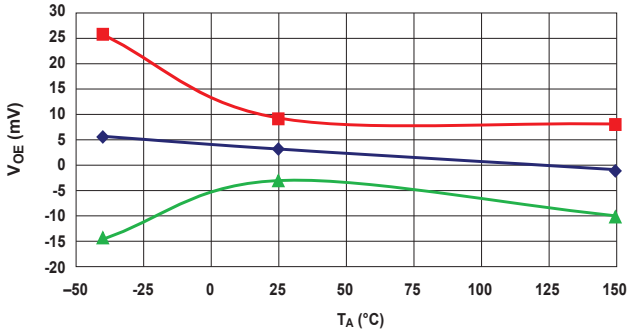
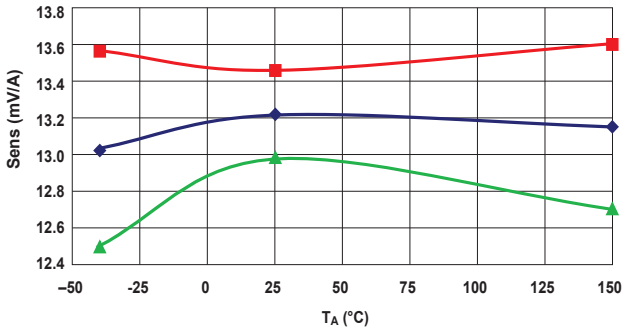
CHARACTERISTIC PERFORMANCE DATA
Data taken using the ACS759LCB-100B

Accuracy Data

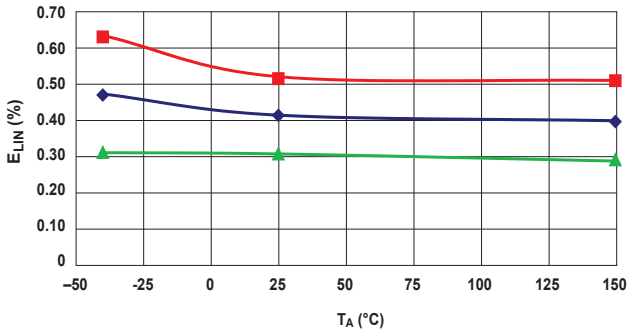
Electrical Offset Voltage versus Ambient Temperature



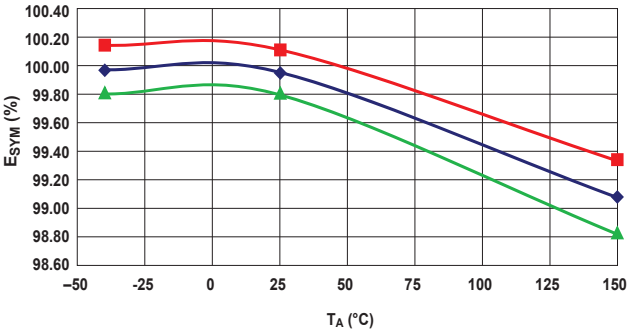
Sensitivity versus Ambient Temperature



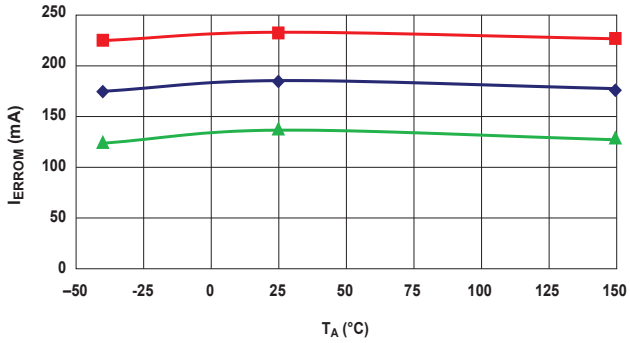
Nonlinearity versus Ambient Temperature



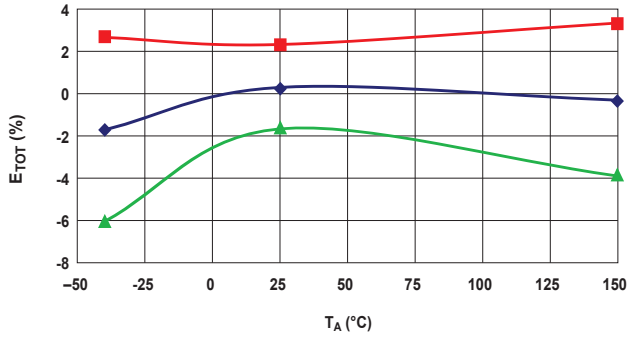
Symmetry versus Ambient Temperature

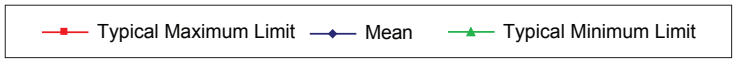


Magnetic Offset Error versus Ambient Temperature



Total Output Error versus Ambient Temperature





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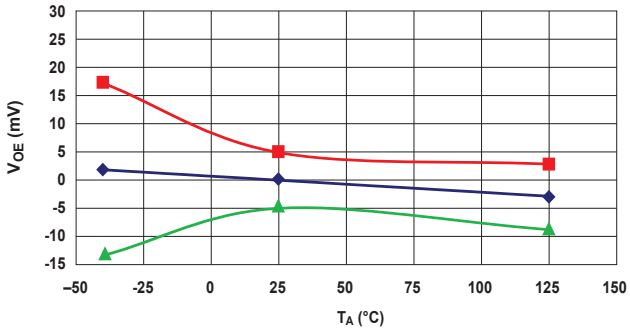
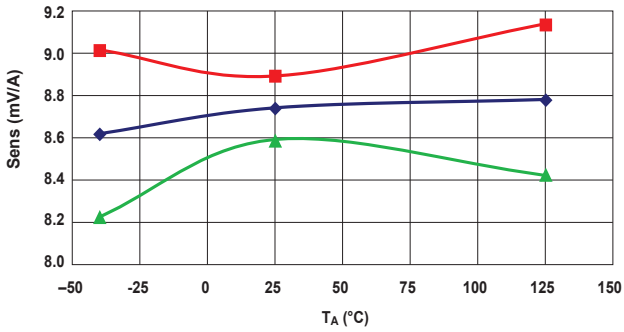
CHARACTERISTIC PERFORMANCE DATA
Data taken using the ACS759LCB-150B

Accuracy Data

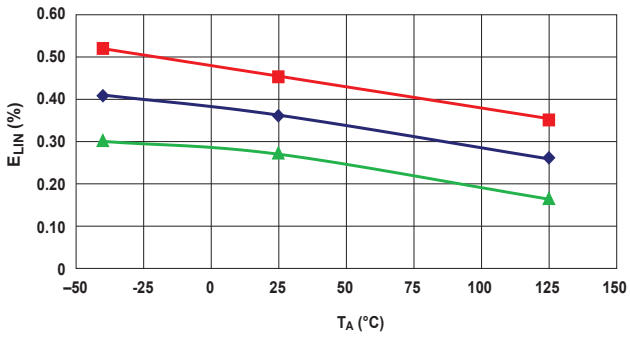
Electrical Offset Voltage versus Ambient Temperature



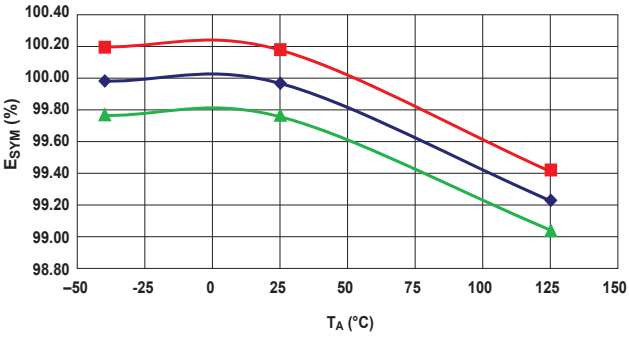
Sensitivity versus Ambient Temperature



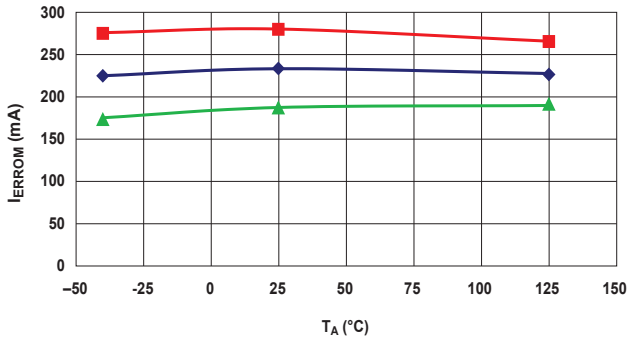
Nonlinearity versus Ambient Temperature



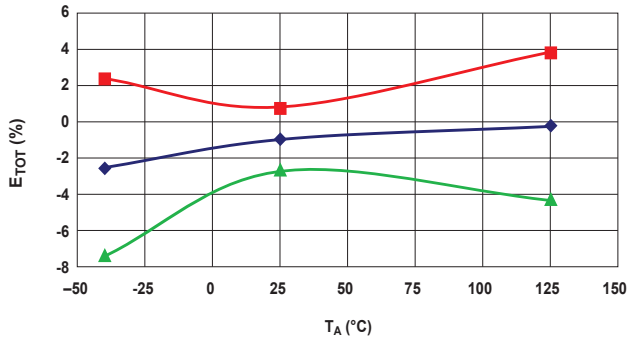
Symmetry versus Ambient Temperature

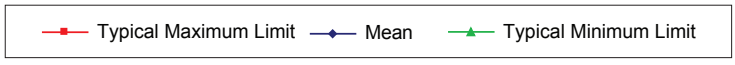


Magnetic Offset Error versus Ambient Temperature



Total Output Error versus Ambient Temperature





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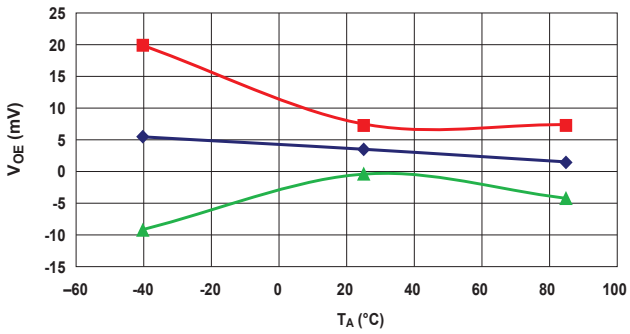
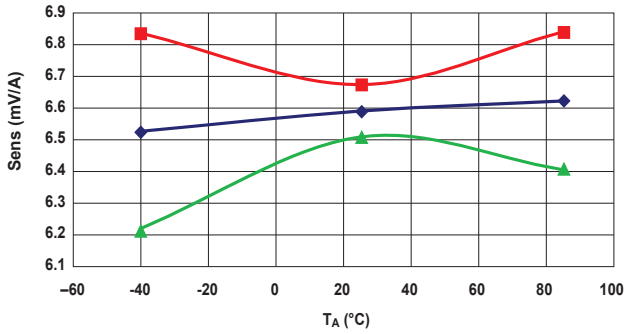
CHARACTERISTIC PERFORMANCE DATA
Data taken using the ACS759LCB-200B

Accuracy Data

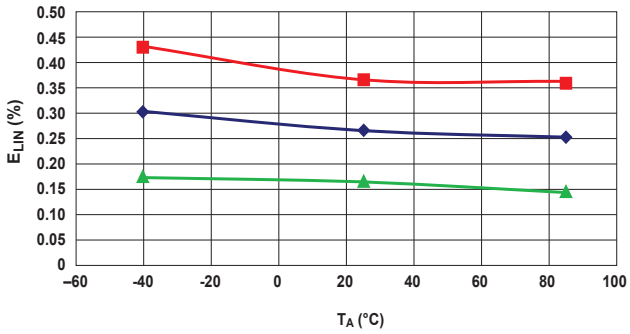
Electrical Offset Voltage versus Ambient Temperature



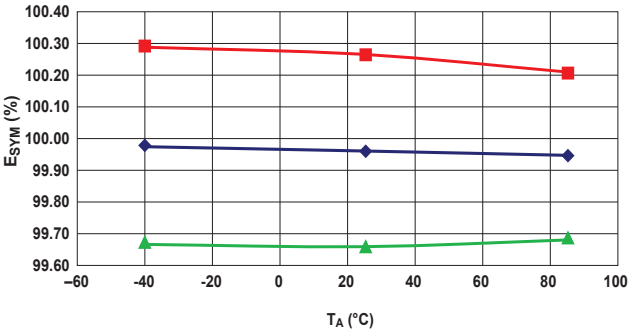
Sensitivity versus Ambient Temperature



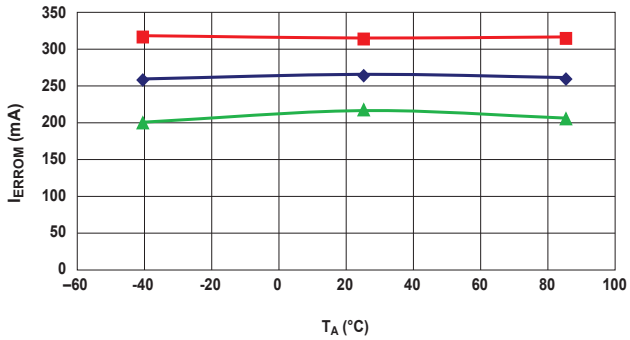
Nonlinearity versus Ambient Temperature



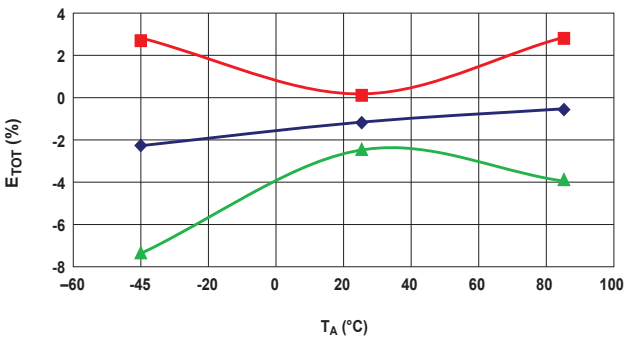
Symmetry versus Ambient Temperature

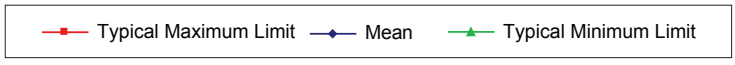


Magnetic Offset Error versus Ambient Temperature



Total Output Error versus Ambient Temperature





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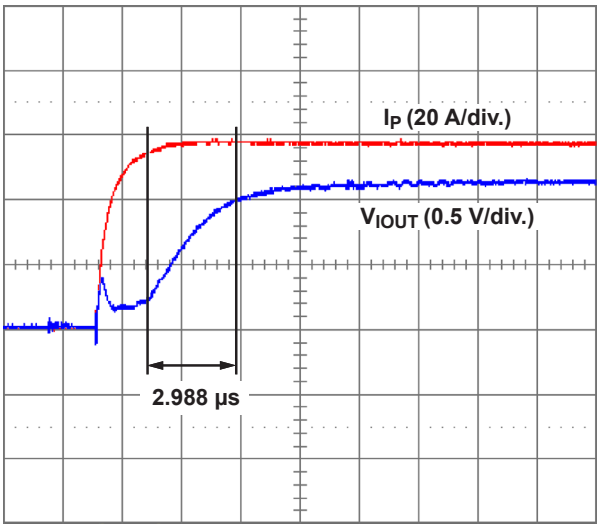
CHARACTERISTIC PERFORMANCE DATA

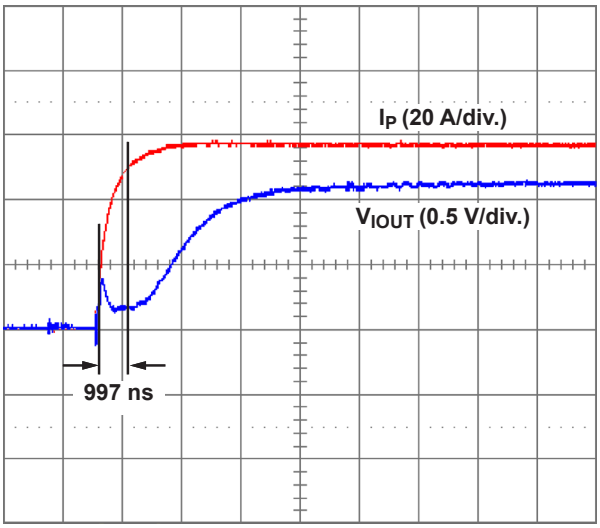
Data taken using the ACS759LCB-100

Timing Data

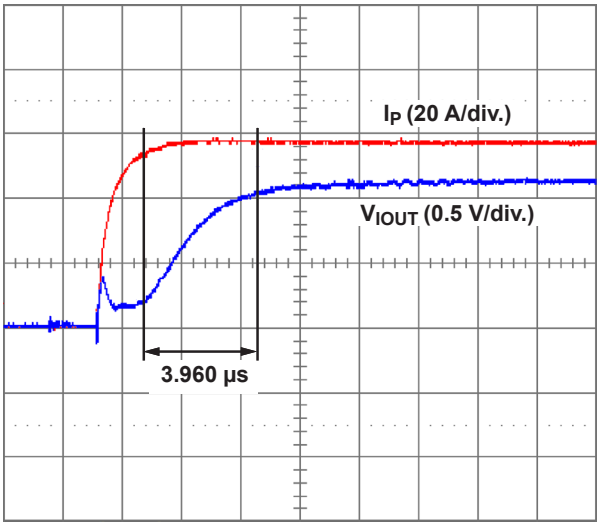
Rise Time



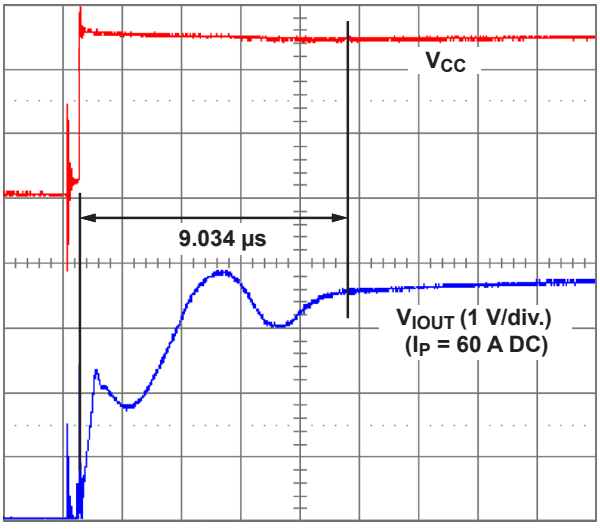
Propagation Delay Time



Response Time



Power-on Delay



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CHARACTERISTIC DEFINITIONS

Definitions of Accuracy Characteristics

Sensitivity (Sens). The change in device output in response to a 1 A change through the primary conductor. The sensitivity is the product of the magnetic circuit sensitivity (G/A) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is programmed at the factory to optimize the sensitivity (mV/A) for the half-scale current of the device.

Noise (V_{NOISE}). The noise floor is derived from the thermal and shot noise observed in Hall elements. Dividing the noise (mV) by the sensitivity (mV/A) provides the smallest current that the device is able to resolve.

Nonlinearity (E_{LIN}). The degree to which the voltage output from the IC varies in direct proportion to the primary current through its half-scale amplitude. Nonlinearity in the output can be attributed to the saturation of the flux concentrator approaching the half-scale current. The following equation is used to derive the linearity:

$$100\left\{1-\left[\frac{\Delta \text{ gain} \times \%\text{ sat}\,(V_{\text{IOUT\_half-scale amperes}} - V_{\text{IOUT(Q)}})}{2\,(V_{\text{IOUT\_quarter-scale amperes}} - V_{\text{IOUT(Q)}})}\right]\right\}$$

where

Δ gain = the gain variation as a function of temperature changes from 25°C,
% sat = the percentage of saturation of the flux concentrator, which becomes significant as the current being sampled approaches half-scale $\pm I_P$, and
$V_{\text{IOUT\_half-scale amperes}}$ = the output voltage (V) when the sampled current approximates half-scale $\pm I_P$.

Symmetry (E_{SYM}). The degree to which the absolute voltage output from the IC varies in proportion to either a positive or negative half-scale primary current. The following equation is used to derive symmetry:

$$100\left(\frac{V_{\text{IOUT\_+ half-scale amperes}} - V_{\text{IOUT(Q)}}}{V_{\text{IOUT(Q)}} - V_{\text{IOUT\_–half-scale amperes}}}\right)$$

Ratiometry. The device features a ratiometric output. This means that the quiescent voltage output, V_{IOUTQ}, and the magnetic sensitivity, Sens, are proportional to the supply voltage, V_{CC}.

The ratiometric change (%) in the quiescent voltage output is defined as:

$$\Delta V_{\text{IOUTQ}(\Delta V)} = \frac{V_{\text{IOUTQ}(V_{CC})} / V_{\text{IOUTQ}(3.3V)}}{V_{CC} / 3.3\text{ (V)}} \times 100\ (\%$$

and the ratiometric change (%) in sensitivity is defined as:

$$\Delta \text{Sens}_{(\Delta V)} = \frac{\text{Sens}_{(V_{CC})} / \text{Sens}_{(3.3V)}}{V_{CC} / 3.3\text{ (V)}} \times 100\ (\%)$$

Quiescent output voltage ($V_{IOUT(Q)}$). The output of the device when the primary current is zero. For bidirectional devices, it nominally remains at $V_{CC}/2$. Thus, V_{CC} = 3.3 V translates into $V_{IOUT(QBI)}$ = 1.65 V. For unidirectional devices, it nominally remains at 0.1 × V_{CC}. Thus, V_{CC} = 3.3 V translates into $V_{IOUT(QUNI)}$ = 0.33 V. Variation in $V_{IOUT(Q)}$ can be attributed to the resolution of the Allegro linear IC quiescent voltage trim, magnetic hysteresis, and thermal drift.

Electrical offset voltage (V_{OE}). The deviation of the device output from its ideal quiescent value of $V_{CC}/2$ for bidirectional and 0.1 × V_{CC} for unidirectional devices, due to nonmagnetic causes.

Magnetic offset error (I_{ERROM}). The magnetic offset is due to the residual magnetism (remnant field) of the core material. The magnetic offset error is highest when the magnetic circuit has been saturated, usually when the device has been subjected to a full-scale or high-current overload condition. The magnetic offset is largely dependent on the material used as a flux concentrator. The larger magnetic offsets are observed at the lower operating temperatures.

Total Output Error (E_{TOT}). The maximum deviation of the actual output from its ideal value, also referred to as *accuracy*, illustrated graphically in the output voltage versus current chart on the following page.

E_{TOT} is divided into four areas:

- **0 A at 25°C.** Accuracy at the zero current flow at 25°C, without the effects of temperature.
- **0 A over Δ temperature.** Accuracy at the zero current flow including temperature effects.
- **Half-scale current at 25°C.** Accuracy at the the half-scale current at 25°C, without the effects of temperature.
- **Half-scale current over Δ temperature.** Accuracy at the half-scale current flow including temperature effects.

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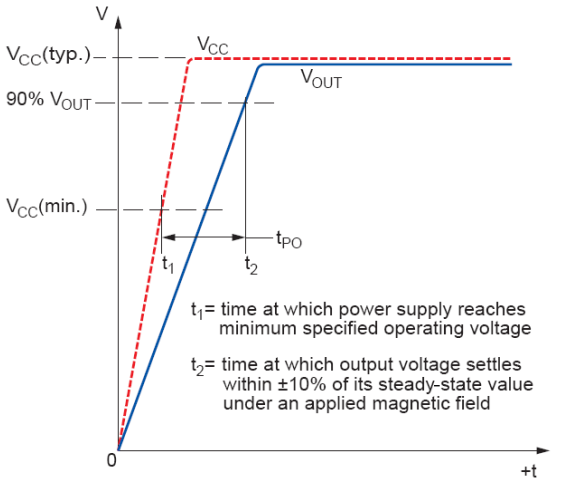
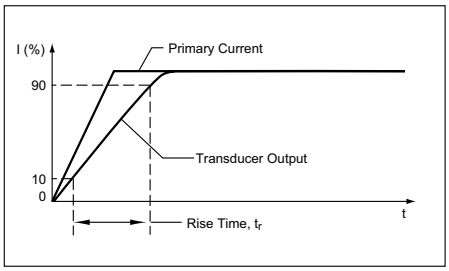
Definitions of Dynamic Response Characteristics

Power-On Time (t_{PO}). When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field.

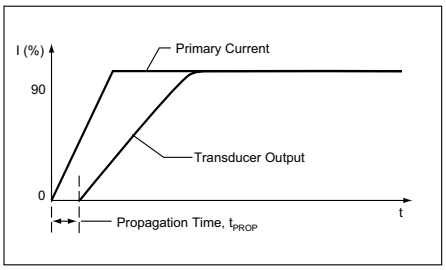
Power-On Time, t_{PO} , is defined as the time it takes for the output voltage to settle within ±10% of its steady-state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage, V_{CC}(min), as shown in the chart at right.



Rise time (t_r). The time interval between a) when the device reaches 10% of its full-scale value, and b) when it reaches 90% of its full scale value. The rise time to a step response is used to derive the bandwidth of the device, in which $f(-3\ \text{dB}) = 0.35 / t_r$. Both t_r and $t_{RESPONSE}$ are detrimentally affected by eddy current losses observed in the conductive IC ground plane.



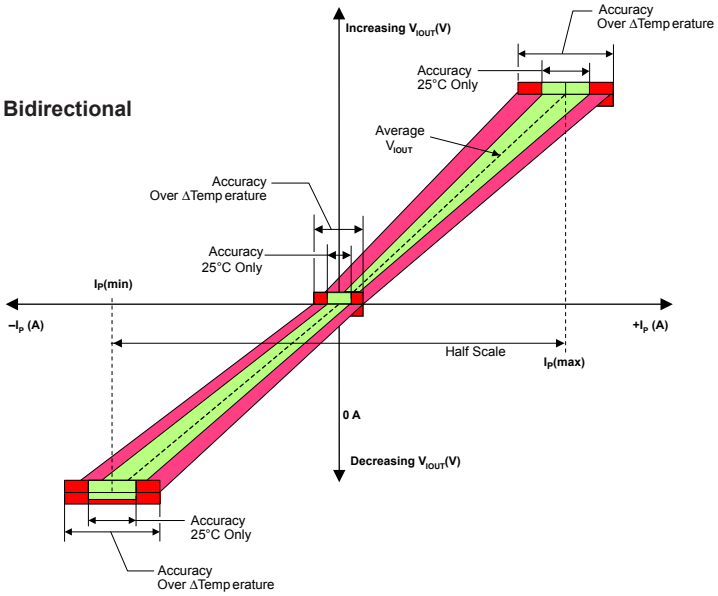
Propagation delay (t_{PROP}). The time required for the device output to reflect a change in the primary current signal. Propagation delay is attributed to inductive loading within the linear IC package, as well as in the inductive loop formed by the primary conductor geometry. Propagation delay can be considered as a fixed time offset and may be compensated.



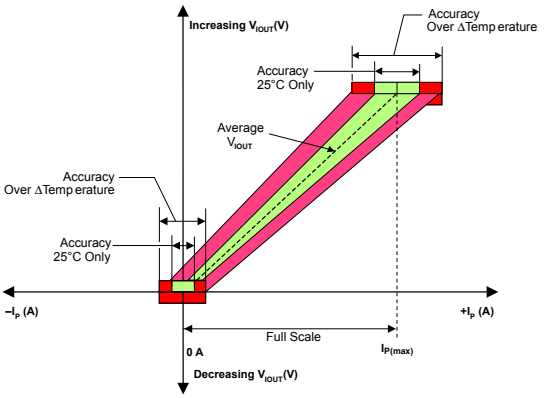
Output Voltage versus Sampled Current

Total Output Error at 0 A and at Half-Scale Current

Bidirectional



Unidirectional



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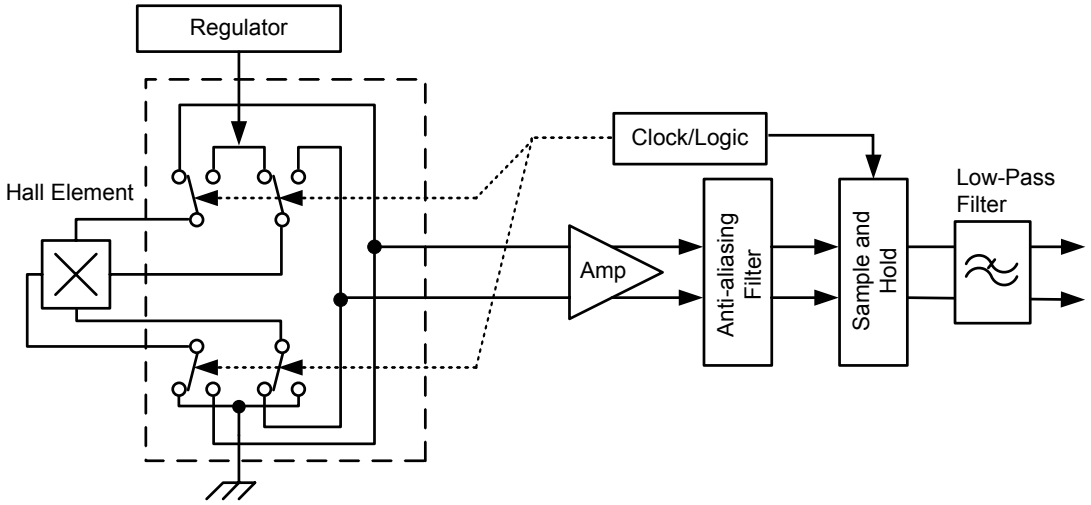
Chopper Stabilization Technique

Chopper Stabilization is an innovative circuit technique that is used to minimize the offset voltage of a Hall element and an associated on-chip amplifier. The technique nearly eliminates Hall IC output drift induced by temperature or package stress effects.

This offset reduction technique is based on a signal modulation-demodulation process. Modulation is used to separate the undesired DC offset signal from the magnetically induced signal in the frequency domain. Then, using a low-pass filter, the modulated DC offset is suppressed while the magnetically induced signal passes through the filter. The anti-aliasing filter prevents aliasing from happening in applications with high frequency signal components which are beyond the user's frequency range of interest.

As a result of this chopper stabilization approach, the output voltage from the Hall IC is desensitized to the effects of temperature and mechanical stress. This technique produces devices that have an extremely stable Electrical Offset Voltage, are immune to thermal stress, and have precise recoverability after temperature cycling.

This technique is made possible through the use of a BiCMOS process that allows the use of low-offset and low-noise amplifiers in combination with high-density logic integration and sample and hold circuits.



Concept of Chopper Stabilization Technique

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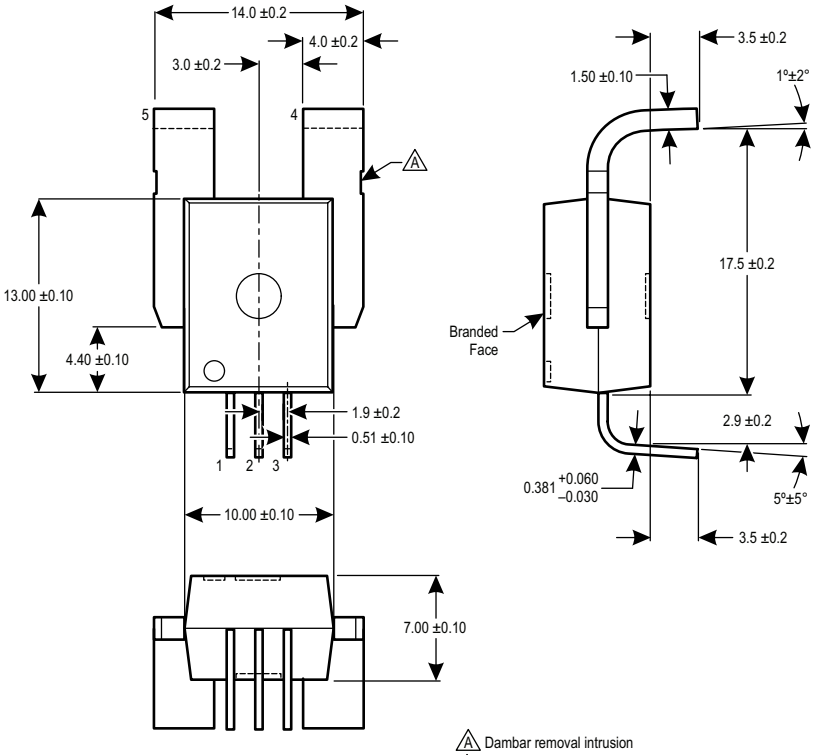
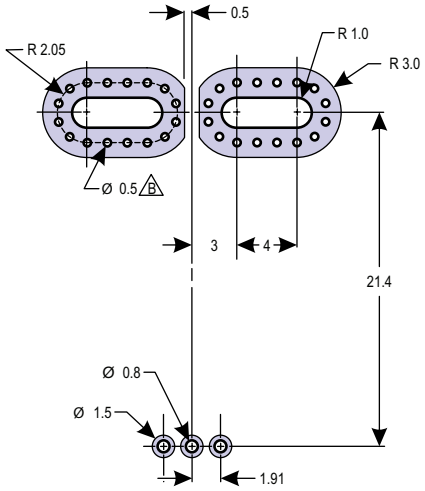
PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

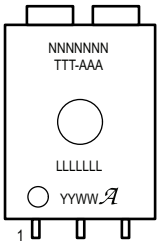
(Reference DWG-9111 & DWG-9110)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Dambar removal intrusion
B Perimeter through-holes recommended
C Branding scale and appearance at supplier discretion



B PCB Layout Reference View



C Standard Branding Reference View

N = Device part number
T = Temperature code
A = Amperage range
L = Lot number
Y = Last two digits of year of manufacture
W = Week of manufacture
𝒜 = Supplier emblem

Creepage distance, current terminals to signal pins: 7.25 mm
Clearance distance, current terminals to signal pins: 7.25 mm
Package mass: 4.63 g typical

Package CB, 5-pin Package, Leadform PFF

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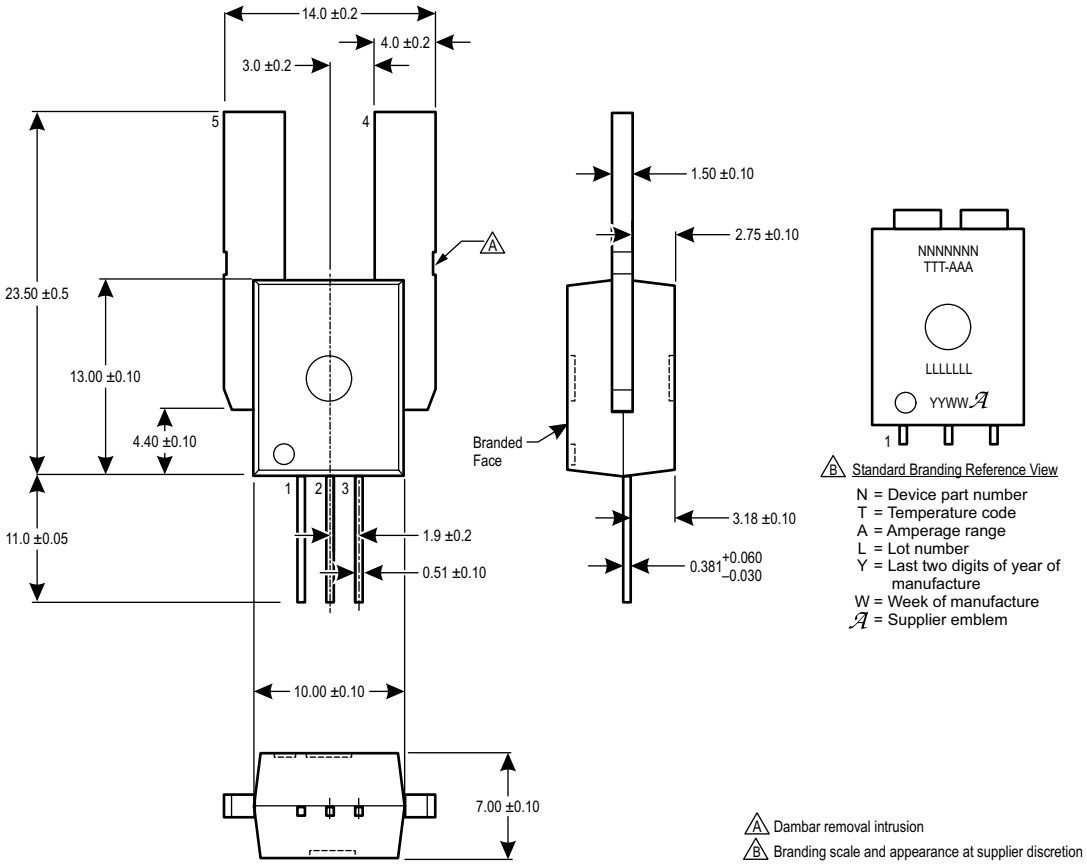
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



Creepage distance, current terminals to signal pins: 7.25 mm
Clearance distance, current terminals to signal pins: 7.25 mm
Package mass: 4.63 g typical

Package CB, 5-pin Package, Leadform PSS

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REVISION HISTORY

Number	Date	Description
1	January, 2013	Update Isolation certifications and specifications; update to current terminology
2	April 8, 2015	Updated TUV certification and reformatted document
3	November 2, 2016	Updated PCB Layout Reference View in Package Outline Drawing on page 17
4	June 5, 2017	Updated product status
5	June 1, 2018	Updated recommended substitution
6	December 5, 2018	Updated TUV/UL Certification
7	May 31, 2019	Updated TUV certificate mark
8	February 3, 2020	Updated product status

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- Shortage Management
- Alternative Solution
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