THE DATASHEET OF

A6273KLWTR

8-Bit Latched, DMOS Power Driver

Discontinued Product

These parts are no longer in production The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: April 28, 2007

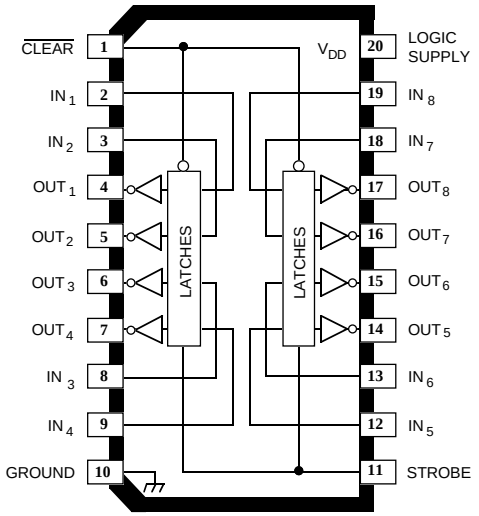
Recommended Substitutions:

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

6273

Data Sheet
26180.120

8-BIT LATCHED DMOS POWER DRIVER



Dwg. PP-015-2A

Note that the A6273KA (DIP) and the A6273KLW (SOIC) are electrically identical and share a common terminal number assignment.

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Output Voltage, V_O ..... **50 V**
Output Drain Current,
Continuous, I_O ..... **250 mA***
Peak, I_{OM} ..... **750 mA*†**
Peak, I_{OM} ..... **2.0 A†**
Single-Pulse Avalanche Energy,
E_{AS} ..... **75 mJ**
Logic Supply Voltage, V_{DD} ..... **7.0 V**
Input Voltage Range,
V_I ..... **-0.3 V to +7.0 V**
Package Power Dissipation,
P_D ..... **See Graph**
Operating Temperature Range,
T_A ..... **-40°C to +125°C**
Storage Temperature Range,
T_S ..... **-55°C to +150°C**

* Each output, all outputs on.

† Pulse duration ≤ 100 µs, duty cycle ≤ 2%.

Caution: These CMOS devices have input static protection (Class 3) but are still susceptible to damage if exposed to extremely high static electrical charges.

The A6273KA and A6273KLW combine eight (positive-edge-triggered D-type) data latches and DMOS outputs for systems requiring relatively high load power. Driver applications include relays, solenoids, and other medium-current or high-voltage peripheral power loads. The CMOS inputs and latches allow direct interfacing with microprocessor-based systems. Use with TTL may require appropriate pull-up resistors to ensure an input logic high.

The DMOS output inverts the DATA input. All of the output drivers are disabled (the DMOS sink drivers turned OFF) with the CLEAR input low. The A6273KA/KLW DMOS open-drain outputs are capable of sinking up to 750 mA.

The A6273KA is furnished in a 20-pin dual in-line plastic package. The A6273KLW is furnished in a 20-lead wide-body, small-outline plastic package (SOIC) with gull-wing leads for surface-mount applications. Copper lead frames, reduced supply current requirements, and low on-state resistance allow both devices to sink 150 mA from all outputs continuously, to ambient temperatures over 85°C.

FEATURES

- 50 V Minimum Output Clamp Voltage
- 250 mA Output Current (all outputs simultaneously)
- 1.3 Ω Typical $r_{DS(on)}$
- Low Power Consumption
- Replacements for TPIC6273N and TPIC6273DW

Always order by complete part number:

Part Number	Package	$R_{\theta JA}$	$R_{\theta JC}$
A6273KA	20-pin DIP	55°C/W	25°C/W
A6273KLW	20-lead SOIC	70°C/W	17°C/W

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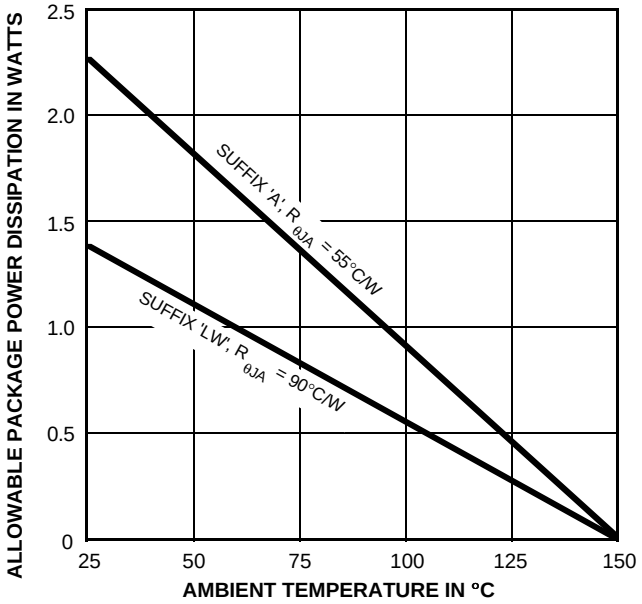
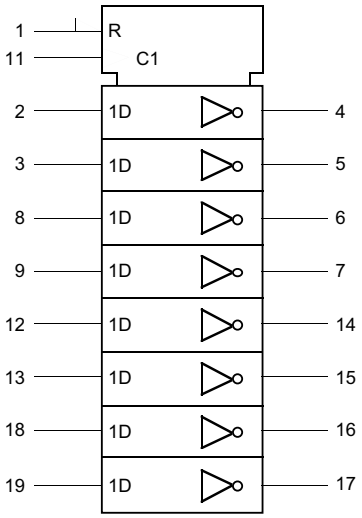
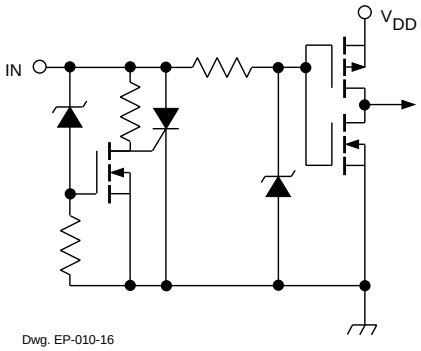


Dwg. GS-004B

LOGIC SYMBOL



Dwg. FP-046-1A



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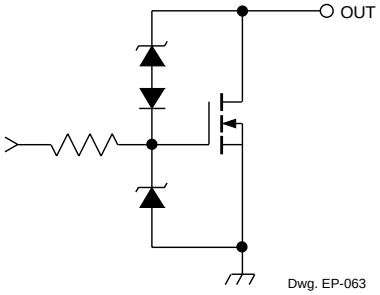
LOGIC INPUTS



Dwg. EP-063

DMOS POWER DRIVER OUTPUT

FUNCTION TABLE

Inputs			
$\overline{\text{CLEAR}}$	STROBE	IN_X	OUT_X
L	X	X	H
H	⌐	H	L
H	⌐	L	H
H	L	X	R

L = Low Logic Level
H = High Logic Level
X = Irrelevant
R = Previous State

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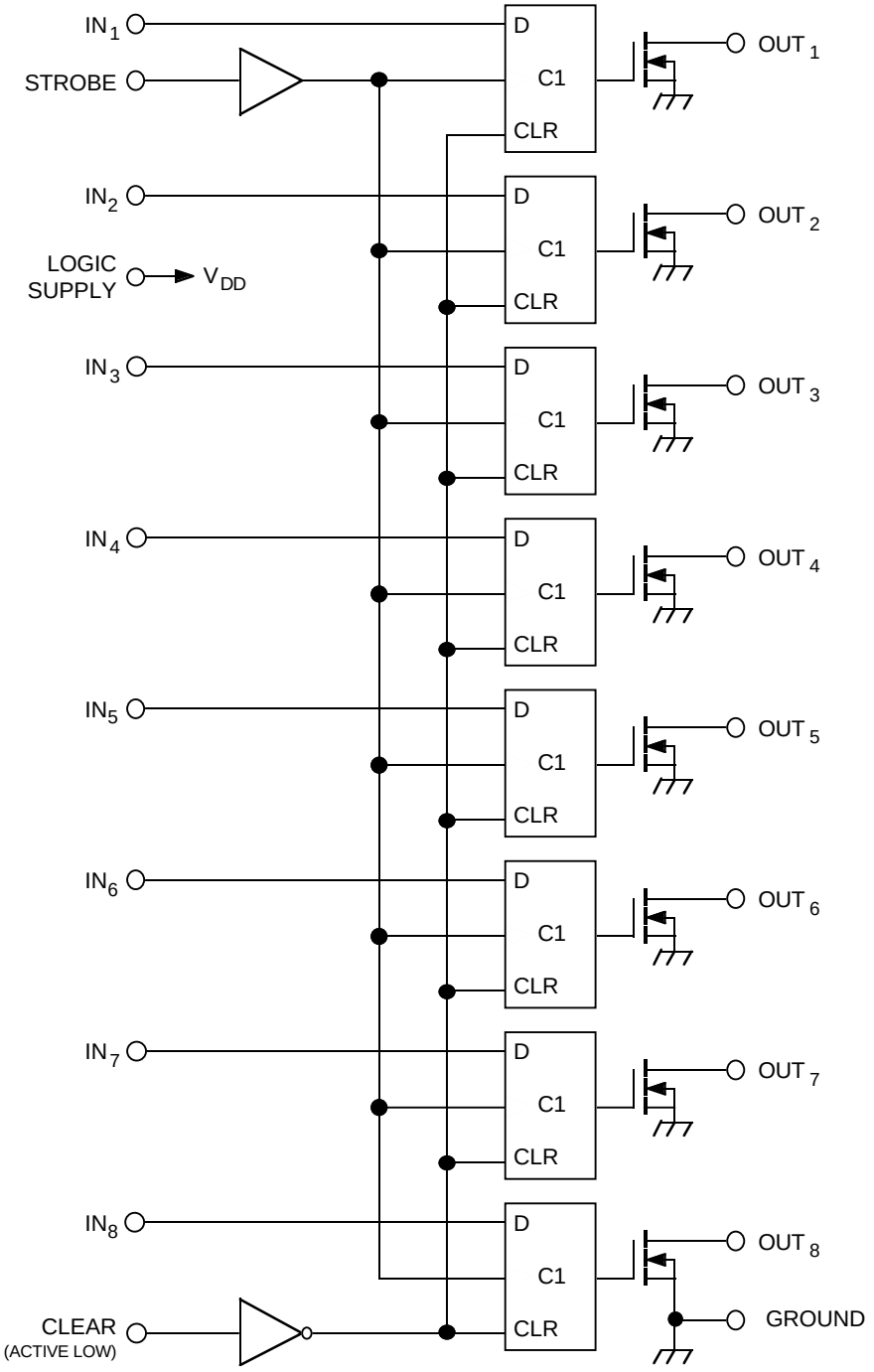
FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-016-2

RECOMMENDED OPERATING CONDITIONS

over operating temperature range

Logic Supply Voltage Range, V_{DD} ..... 4.5 V to 5.5 V
High-Level Input Voltage, V_{IH} ..... $\geq 0.85V_{DD}$
Low-level input voltage, V_{IL} ..... $\leq 0.15V_{DD}$

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V, $t_{ir} = t_{if} \leq 10$ ns (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Logic Supply Voltage	V_{DD}	Operating	4.5	5.0	5.5	V
Output Breakdown Voltage	$V_{(BR)DSX}$	I_O = 1 mA	50	—	—	V
Off-State Output Current	I_{DSX}	V_O = 40 V	—	0.05	1.0	µA
		V_O = 40 V T_A = 125°C	—	0.15	5.0	µA
Static Drain-Source On-State Resistance	$r_{DS(on)}$	I_O = 250 mA, V_{DD} = 4.5 V	—	1.3	2.0	Ω
		I_O = 250 mA, V_{DD} = 4.5 V, T_A = 125°C	—	2.0	3.2	Ω
		I_O = 500 mA, V_{DD} = 4.5 V (see note)	—	1.3	2.0	Ω
Nominal Output Current	$I_{O(nom)}$	$V_{DS(on)}$ = 0.5 V, T_A = 85°C	—	250	—	mA
Logic Input Current	I_{IH}	$V_I = V_{DD}$ = 5.5 V	—	—	1.0	µA
	I_{IL}	V_I = 0, V_{DD} = 5.5 V	—	—	-1.0	µA
Prop. Delay Time	t_{PLH}	I_O = 250 mA, C_L = 30 pF	—	625	—	ns
	t_{PHL}	I_O = 250 mA, C_L = 30 pF	—	150	—	ns
Output Rise Time	t_r	I_O = 250 mA, C_L = 30 pF	—	675	—	ns
Output Fall Time	t_f	I_O = 250 mA, C_L = 30 pF	—	400	—	ns
Supply Current	$I_{DD(off)}$	V_{DD} = 5.5 V, Outputs OFF	—	15	100	µA
	$I_{DD(on)}$	V_{DD} = 5.5 V, Outputs ON	—	150	300	µA

Typical Data is at V_{DD} = 5 V and is for design information only.

NOTE — Pulse test, duration ≤100 µs, duty cycle ≤2%.

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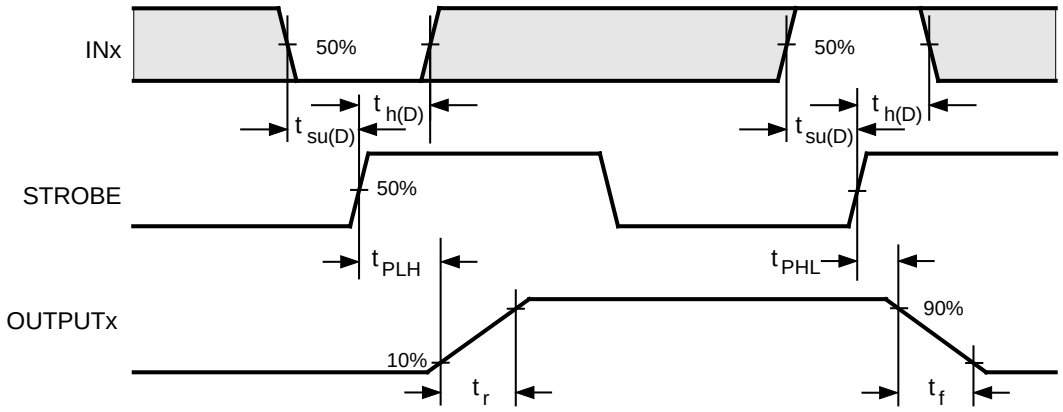
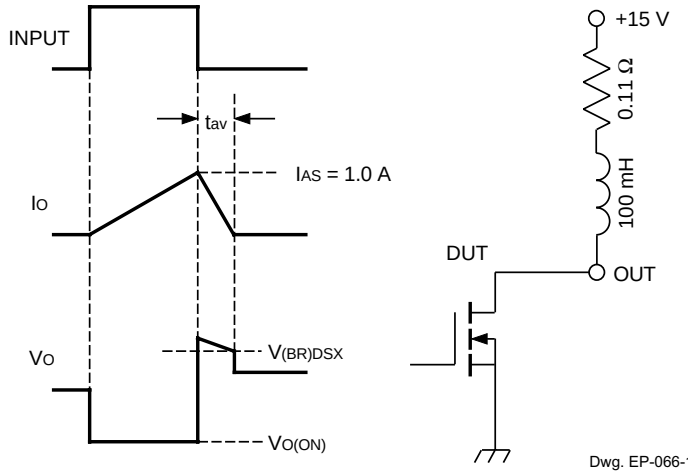
TIMING REQUIREMENTS



Dwg. WP-036-1

Input Active Time Before Strobe
(Data Set-Up Time), $t_{su(D)}$ ..... **20 ns**
Input Active Time After Strobe
(Data Hold Time), $t_{h(D)}$ ..... **20 ns**
Input Pulse Width, $t_{w(D)}$ ..... **40 ns**
Input Logic High, V_{IH} ..... **≥ 0.85V_{DD}**
Input Logic Low, V_{IL} ..... **≤ 0.15V_{DD}**

TEST CIRCUIT



Dwg. EP-066-1

Single-Pulse Avalanche Energy Test Circuit and Waveforms

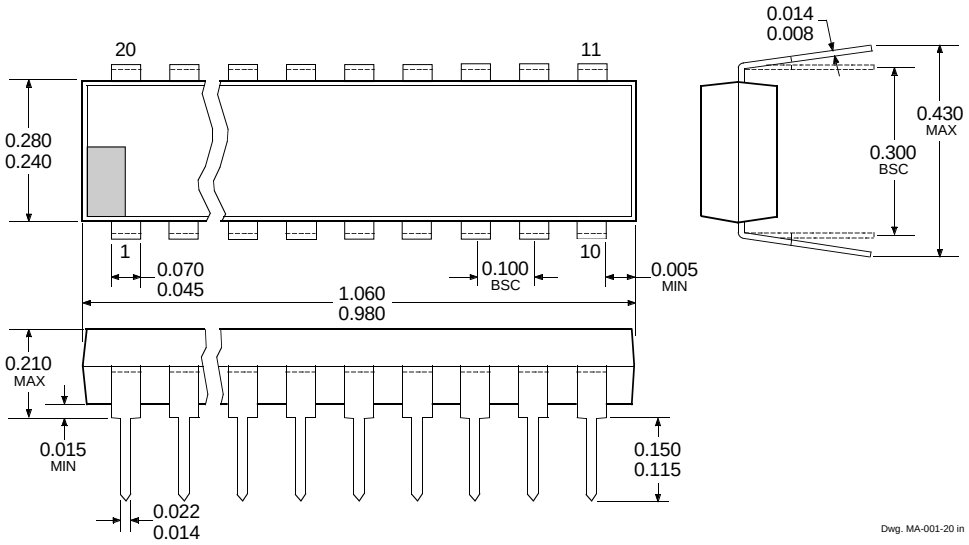
$E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{AV}/2$

TERMINAL DESCRIPTIONS

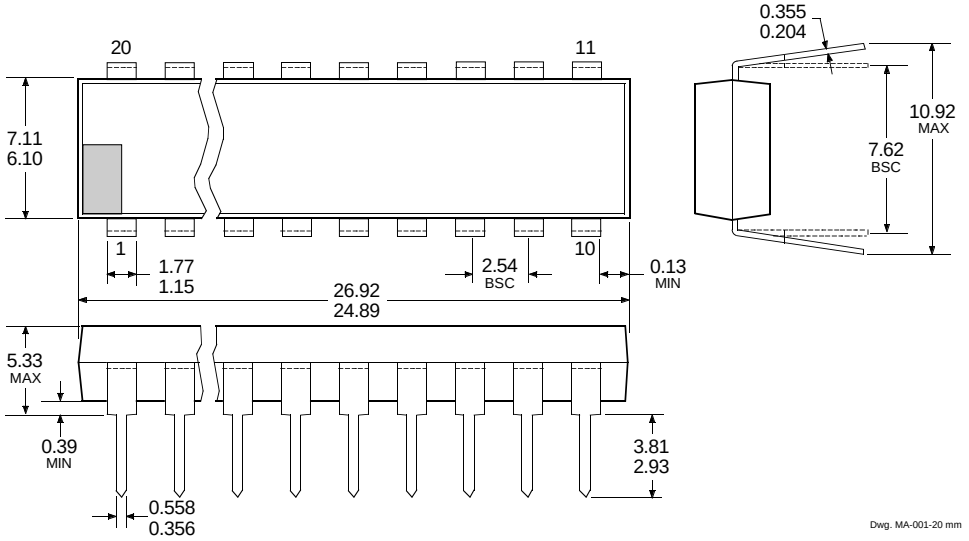
Terminal No.	Terminal Name	Function
1	CLEAR	When (active) LOW, all latches are reset and all outputs go HIGH (turn OFF).
2	IN_1	CMOS data input to a latch. When strobed, the output then inverts the data input (IN_1 = HIGH, OUT_1 = LOW).
3	IN_2	CMOS data input to a latch. When strobed, the output then inverts the data input (IN_2 = HIGH, OUT_2 = LOW).
4	OUT_1	Current-sinking, open-drain DMOS output.
5	OUT_2	Current-sinking, open-drain DMOS output.
6	OUT_3	Current-sinking, open-drain DMOS output.
7	OUT_4	Current-sinking, open-drain DMOS output.
8	IN_3	CMOS data input to a latch. When strobed, the output then inverts the data input (IN_3 = HIGH, OUT_3 = LOW).
9	IN_4	CMOS data input to a latch. When strobed, the output then inverts the data input (IN_4 = HIGH, OUT_4 = LOW).
10	GROUND	Reference terminal for all voltage measurements.
11	STROBE	A CMOS dynamic input to all latches. Data on each IN_x terminal is loaded into its associated latch on a low-to-high STROBE transition.
12	IN_5	CMOS data input to a latch. When strobed, the output then inverts the data input (IN_5 = HIGH, OUT_5 = LOW).
13	IN_6	CMOS data input to a latch. When strobed, the output then inverts the data input (IN_6 = HIGH, OUT_6 = LOW).
14	OUT_5	Current-sinking, open-drain DMOS output.
15	OUT_6	Current-sinking, open-drain DMOS output.
16	OUT_7	Current-sinking, open-drain DMOS output.
17	OUT_8	Current-sinking, open-drain DMOS output.
18	IN_7	CMOS data input to a latch. When strobed, the output then inverts the data input (IN_7 = HIGH, OUT_7 = LOW).
19	IN_8	CMOS data input to a latch. When strobed, the output then inverts the data input (IN_8 = HIGH, OUT_8 = LOW).
20	LOGIC SUPPLY	(V_{DD}) The logic supply voltage (typically 5 V).

A6273KA

Dimensions in Inches
(controlling dimensions)



Dimensions in Millimeters
(for reference only)

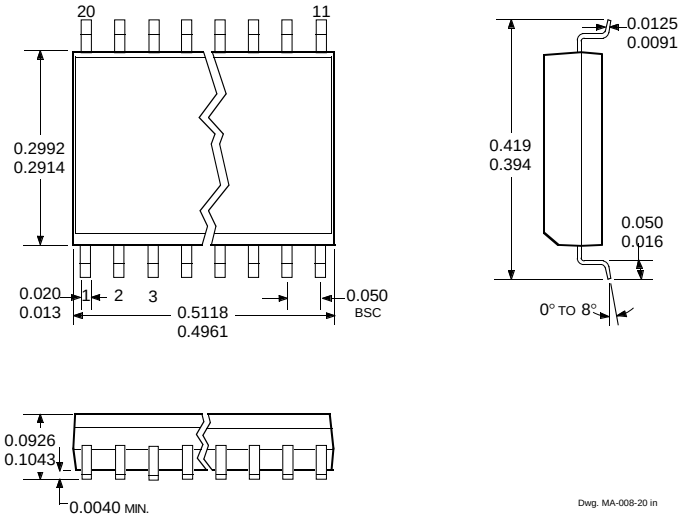


NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Lead thickness is measured at seating plane or below.
4. Supplied in standard sticks/tubes of 18 devices.

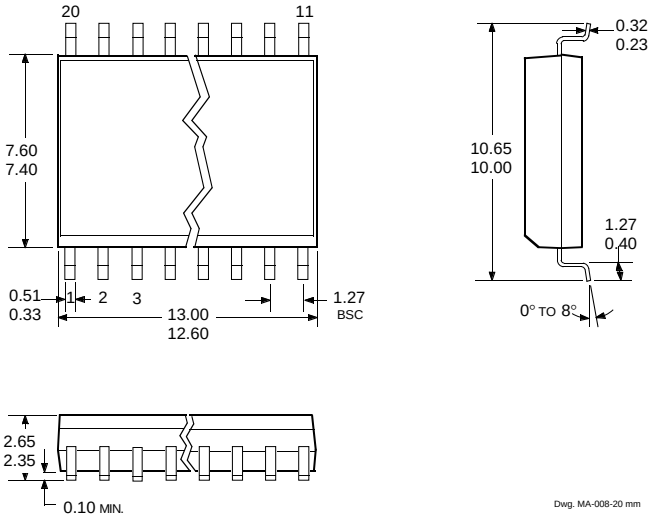
6273
8-BIT LATCHED DMOS POWER DRIVER

A6273KLW

Dimensions in Inches
(for reference only)



Dimensions in Millimeters
(controlling dimensions)



NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Supplied in standard sticks/tubes of 37 devices or add 'TR' to part number for tape and reel.

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8-BIT LATCHED DMOS POWER DRIVER

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POWER INTERFACE DRIVERS

Function	Output Ratings*		Part Number†
SERIAL-INPUT LATCHED DRIVERS			
8-Bit (saturated drivers)	-120 mA	50 V‡	5895
8-Bit	350 mA	50 V	5821
8-Bit	350 mA	80 V	5822
8-Bit	350 mA	50 V‡	5841
8-Bit	350 mA	80 V‡	5842
8-Bit (constant-current LED driver)	75 mA	17 V	6275
8-Bit (constant-current LED driver)	120 mA	24 V	6277
8-Bit (DMOS drivers)	250 mA	50 V	6595
8-Bit (DMOS drivers)	350 mA	50 V‡	6A595
8-Bit (DMOS drivers)	100 mA	50 V	6B595
10-Bit (active pull-downs)	-25 mA	60 V	5810-F and 6810
12-Bit (active pull-downs)	-25 mA	60 V	5811
16-Bit (constant-current LED driver)	75 mA	17 V	6276
20-Bit (active pull-downs)	-25 mA	60 V	5812-F and 6812
32-Bit (active pull-downs)	-25 mA	60 V	5818-F and 6818
32-Bit	100 mA	30 V	5833
32-Bit (saturated drivers)	100 mA	40 V	5832
PARALLEL-INPUT LATCHED DRIVERS			
4-Bit	350 mA	50 V‡	5800
8-Bit	-25 mA	60 V	5815
8-Bit	350 mA	50 V‡	5801
8-Bit (DMOS drivers)	100 mA	50 V	6B273
8-Bit (DMOS drivers)	250 mA	50 V	6273
SPECIAL-PURPOSE DEVICES			
Unipolar Stepper Motor Translator/Driver	1.25 A	50 V‡	5804
Addressable 8-Bit Decoder/DMOS Driver	250 mA	50 V	6259
Addressable 8-Bit Decoder/DMOS Driver	350 mA	50 V‡	6A259
Addressable 8-Bit Decoder/DMOS Driver	100 mA	50 V	6B259
Addressable 28-Line Decoder/Driver	450 mA	30 V	6817

* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits. Negative current is defined as coming out of (sourcing) the output.

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ Internal transient-suppression diodes included for inductive-load protection.

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