THE DATASHEET OF

MC34CM3120EPR2

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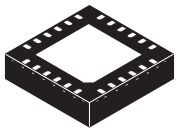
IO-link master transceiver

CM3120

IO-LINK TRANSCEIVER



EP SUFFIX
48 QFN

The CM3120 is an IO-Link master physical layer dedicated to the industrial market. It includes two fully-featured IO-Link channels, which can work in three different operation modes. This circuit integrates an IO-Link frame handler fully compliant with the IO-Link v1.1 specification, and which implements most of the IO-Link communication tasks. The frame handler significantly decreases load of the master microcontroller. The CM3120 also provides several protection and monitoring mechanisms such as overcurrent, overvoltage, and overtemperature.

Features

- Two IO-Link channels with three different operation modes (SIO, UART, and frame handler)
- Protection mechanisms (overcurrent, overtemperature, overvoltage)
- Configurable through a SPI interface
- Operating voltage range from 8.0 V to 32 V
- Suitable for 2/4/8/16 port-applications
- Can operate as a Master or Device
- Two integrated LED drivers
- Integrated hardware frame handler (supports all IO-link v1.1 frames and COM1, COM2, and COM3 baud rates)
- Integrated NMOS gate drivers to control current to the C/Q and L+ lines

Applications

- Factory automation
- Fieldbus gateways
- Programmable logic controllers
- Process controllers

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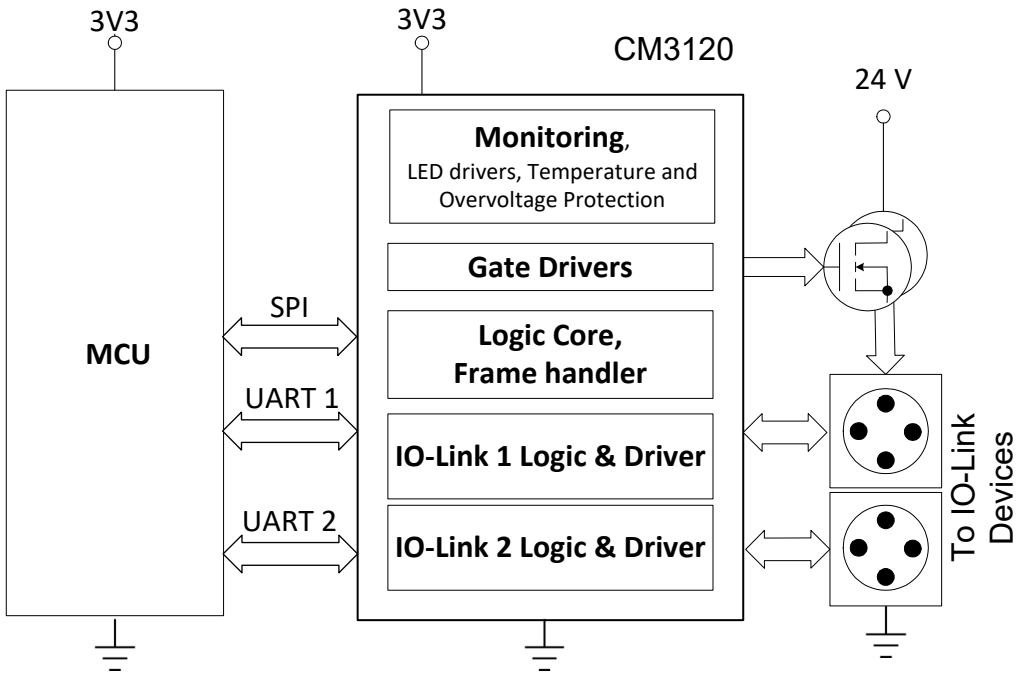

Figure 1. CM3120 simplified application diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

1 Orderable parts

Table 1. Orderable part variations

Part number [1]	Temperature (T_A)	V_{DD} voltage	Package
MC34CM3120EP	-40 °C to 85 °C	5.0 V	QFN48 with exposed pad (7.0 mm x 7.0 mm)

Notes
1. To order parts in Tape and Reel, add the R2 suffix to the part number.

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2 Internal block diagram

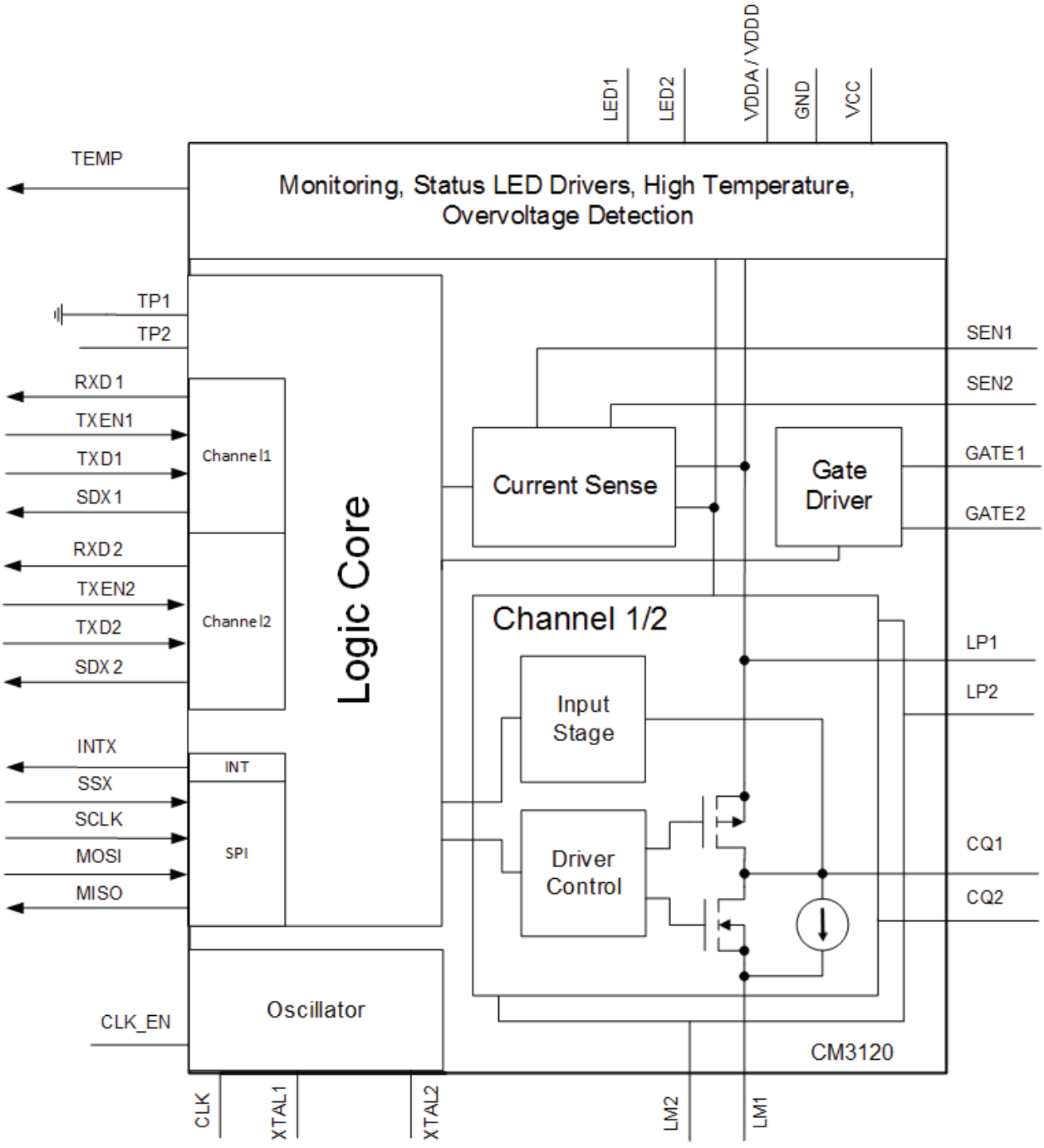

Figure 2. CM3120 simplified internal block diagram

3 Pin connections

3.1 Pinout diagram

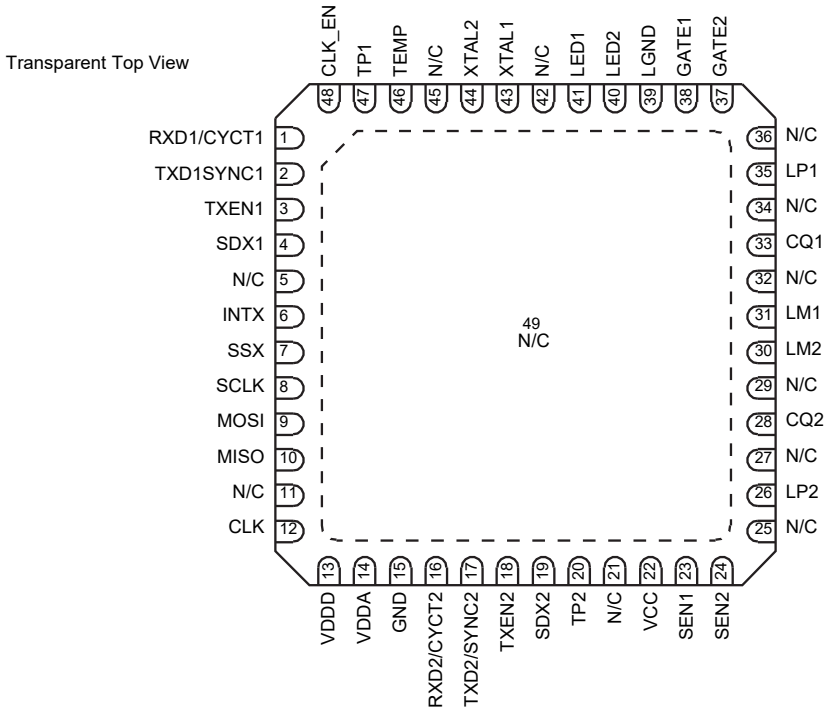

Figure 3. CM3120 pin connections

Functional descriptions of many of these pins can be found in the Functional Pin Description section beginning on page 9.

3.2 Pin definitions

Table 2. CM3120 pin definitions

Pin	Pin name	Pin function	Definition
1	RXD1/ CYCT1	OUT	RXD1: CQ1 input; inverted
2	TXD1/ SYNC1	IN	TXD1: CQ1 output; internal pull-down; inverted
3	TXEN1	IN	CQ1 driver enable; active high, internal pull-down
4	SDX1	OUT	Device 1 short detected; active low
5, 11, 21, 25, 27, 29, 32, 34, 36, 42, 45	NC	NC	Not Connected
6	INTX	OUT	SPI interrupt signal; active low
7	SSX	IN	SPI slave select; active low; internal pull-up
8	SCLK	IN	SPI clock; internal pull-down
9	MOSI	IN	SPI data in; internal pull-down
10	MISO	OUT	SPI data out; tri-state if SSX is high

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Table 2. CM3120 pin definitions (continued)

Pin	Pin name	Pin function	Definition
12	CLK	OUT	Buffered clock feed through
13	VDDD	PWR	3.3 V digital voltage supply
14	VDDA	PWR	3.3 V analog voltage supply
15	GND	PWR	Ground
16	RXD2/ CYCT2	OUT	RXD2: CQ2 input; inverted
17	TXD2/ SYNC2	IN	RXD2: CQ2 output; internal pull-down; inverted
18	TXEN2	IN	CQ2 driver enable; active high, internal pull-down
19	SDX2	OUT	Device 2 short detected; active low
20	TP2	OUT	Test Point 2; leave open
22	VCC	PWR	24 V main voltage supply
23	SEN1	IN	Sense input channel 1
24	SEN2	IN	Sense input channel 2
26	LP2	PWR	Sensor supply channel 1
28	CQ2	IN/OUT	IO-Link channel 2
30	LM2	PWR	Sensor ground 2
31	LM1	PWR	Sensor ground channel 1
33	CQ1	IN/OUT	IO-Link channel 1
35	LP1	PWR	Sensor supply channel 1
37	GATE2	OUT	NMOS gate driver channel 2
38	GATE1	OUT	NMOS gate driver channel 1
39	LGND	PWR	LED ground
40	LED2	IN	LED driver channel 2
41	LED1	IN	LED driver channel 1
43	XTAL1	IN	Crystal input; external clock source input
44	XTAL2	OUT	Crystal feedback
46	TEMP	OUT	High temperature indication
47	TP1	IN	Test Point 1; internal pull-down; leave open or tie to ground
48	CLK_EN	IN	Enable buffered clock feed through; internal pull-down

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4 Electrical characteristics

4.1 Maximum ratings

Stress(es) beyond those listed under Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the following operational sections of the specifications is not implied. Exposure to maximum rating condition(s) for extended periods may affect device reliability.

Table 3. Maximum ratings

T_A = 25 °C ±1.0 °C, unless otherwise specified. All voltages are with respect to ground unless otherwise noted.

Symbol	Rating	Min.	Max.	Unit	Notes
Electrical ratings					
V_{CC}	Supply Voltage - Static	-0.7	36	V	
P_{TOT_QFN48}	Power Dissipation, QFN48 Package on Multilayer PCB, Pad soldered, T_{AMB} = 60 °C	—	2.0	W	
V_{ESD}	ESD Voltage • Human Body Model (HBM)	—	2000	V	(2)
	FIT Rate	—	50	FIT	
Thermal ratings					
T_A	Operating Temperature	-40	85	°C	
T_J	Maximum Temperature Junction	—	150	°C	
T_{JC_QFN48}	Thermal Resistance Case, Junction to Case	—	0.5	°C/W	
T_{JA_QFN48}	Thermal Resistance Ambient, Junction to Ambient	—	29	°C/W	
T_{STG}	Storage Ambient Temperature	-55	155	°C	
T_{SOLDER}	Lead Soldering Temperature (within 10 s)	—	260	°C	

Notes

2. Human Body Model (HBM) per EIA/JESD22-A114-B for all pins

4.2 Electrical characteristics

Table 4. CM3120 electrical characteristics

Characteristics noted under conditions: Typical values are at T_A = 25 °C ±1.0 °C, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
General parameters						
V_{CC}	Main Supply Voltage	8.0	24	32	V	
I_{VCC}	Quiescent Current Main Supply	—	—	5.0	mA	
V_{DD}	Pad Supply Voltage	3.1	3.3	3.5	V	
I_{VDD}	Quiescent Current Pad Supply	—	—	5.0	mA	
IO-link channels						
V_{CQ}	Permissible Voltage Range	-0.3	—	V_{CC} + 0.3	V	
I_{CQ_LOAD}	Load or Discharge Current. can be disabled; see CFG1/2 (0x2F/0x4F) on page 25	—	10	15	mA	
I_{CQH}	DC Driver Current 'H'	—	—	300	mA	
I_{CQL}	DC Driver Current 'L'	—	—	300	mA	

ARCHIVE INFORMATION

Table 4. CM3120 electrical characteristics (continued)

Characteristics noted under conditions: Typical values are at T_A = 25 °C ±1.0 °C, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
IO-link channels (continued)						
V_{RESH}	Residual Voltage 'H', Voltage drop at I_{CQH_MAX}	—	—	3.0	V	
V_{RESL}	Residual Voltage 'L', Voltage drop at I_{CQL_MAX}	—	—	3.0	V	
I_{PEAKH}	Output Peak Current 'H', Duration t_{PEAK} = 1.0 ms	0.5	1.0	—	A	
I_{PEAKL}	Output Peak Current 'L', Duration t_{PEAK} = 1.0 ms	0.5	1.0	—	A	
C_{LOAD}	Capacitive Load	—	1.0	—	nF	
t_{RISE}	Output Driver Rise Time, CNOM=1.0 nF	—	—	300	ns	
t_{FALL}	Output Driver Fall Time, CNOM=1.0 nF	—	—	300	ns	
t_{BBM}	Break Before Make Delay	—	—	50	ns	
t_{DETH}	Input Detection Time 'H'	—	—	300	ns	
t_{DETH}	Input Detection Time 'L'	—	—	300	ns	
V_{THH_IOL}	Input Threshold 'H', IO-Link mode; see CFG1/2 (0x2F/0x4F) on page 25	10.5	—	13	V	
V_{THL_IOL}	Input Threshold 'L", IO-Link mode; see CFG1/2 (0x2F/0x4F) on page 25	8.0	—	11.5	V	
V_{HYS_IOL}	Hysteresis Input Threshold, IO-Link mode; see CFG1/2 (0x2F/0x4F) on page 25	—	2.0	—	V	
V_{THH_RAT}	Input Threshold 'H', Ratiometric mode; see CFG1/2 (0x2F/0x4F) on page 25	0.55 V_{CC}	—	—	V	
V_{THL_RAT}	Input Threshold 'L', Ratiometric mode; see CFG1/2 (0x2F/0x4F) on page 25	—	—	0.4 V_{CC}	V	
V_{HYS_RAT}	Hysteresis Input Threshold, Ratiometric mode; see CFG1/2 (0x2F/0x4F) on page 25	—	0.0125 V_{CC}	—	V	
NMOS gate drivers						
t_{GATE_ON}	On Switching Time, CGATE = 1.0 nF	—	1.0	—	ms	
t_{GATE_OFF}	Off Switching Time, CGATE = 1.0 nF	—	10	—	µs	
V_{GATE}	Output Voltage, VCC ≥ 15 V	V_{CC} +4.0	—	V_{CC} +8.0	V	
C_{GATE}	External Capacitance	—	1.0	—	nF	
I_{TGSL}	Transistor Leakage Current, Gate to Source (external NMOS)	—	—	1.0	µA	
Oscillator						
f_{OSC}	Frequency, External crystal	—	14,7456	—	MHz	
t_{OSC_START}	Startup Time	—	30	—	ms	
t_{OSC_RISE}	Rise Time	—	5.0	—	ns	
t_{OSC_FALL}	Fall Time	—	5.0	—	ns	
C_{OUT_MAX}	CLK Pin Driving Capability	—	—	15	pF	
Digital pads						
V_{INH}	Input Voltage 'H'	0.7 V_{DD}	—	—	V	
V_{INL}	Input Voltage 'L'	—	—	0.3 V_{DD}	V	
V_{IHYST}	Input Hysteresis	—	340	—	mV	
C_{IN}	Input Capacitance	—	5.0	—	pF	
I_{ILEAK}	Input Leakage Current, No pull-up/pull-down	-1.0	—	1.0	µA	

ARCHIVE INFORMATION

Table 4. CM3120 electrical characteristics (continued)

Characteristics noted under conditions: Typical values are at T_A = 25 °C ±1.0 °C, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
Digital pads (continued)						
V_{OUTH}	Output Voltage 'H'	0.8 V_{DD}	—	—	V	
V_{OUTL}	Output Voltage 'L'	—	—	0.4	V	
I_{OLEAK}	Output Leakage Current, Tri-state Active	—	—	1.0	µA	
C_{OUT}	Output Capacitance	—	-5.0	—	pF	
I_{OUT}	Output Driving Current	6.0	—	—	mA	
I_{IH}	Weak Pull-up Current, V_{IN} = 0 V	—	-30	—	µA	
I_{IL}	Weak Pull-down Current, V_{IN} = V_{DD}	—	30	—	µA	
Serial peripheral interface						
f_{SPI}	SPI Clock Frequency	1.0	—	20	MHz	
t_{SPI_CLK}	SPI Clock Period	50	—	1000	ns	
t_{SPI_S}	SPI Start Clock After Select	25	—	—	ns	
t_{SPI_E}	SPI End of Select After Clock	25	—	—	ns	
t_{SPI_I}	SPI Idle Between Access	100	—	—	ns	
Current sensing						
V_{EXT_SD}	Ext. Short Detection Threshold	—	200	—	mV	
I_{EXT_SD}	Ext. Short Detection Current, R_{SHUNT} = 500 mΩ	—	400	—	mA	
I_{INT_SD}	Int. Short Detection Current	—	350	—	mA	
$t_{OVLDDET}$	Driver Overload Detection Time, Configurable, see Error! Reference source not found.	0.1	—	6.4	ms	
$t_{OVLDDIS}$	Driver Overload Polling Time, see Error! Reference source not found.	1.0	—	6400	ms	
$t_{SHORTDET}$	Short-circuit Detection Time, Configurable; see SHRT1/2 (0x22/0x42) on page 19	0.1	—	336	ms	
Monitoring thresholds						
VCC_{OK_MIN}	Min. Voltage Monitor Threshold	—	7.5	—	V	
VCC_{OK_MAX}	Max. Voltage Monitor Threshold	—	34	—	V	
VCC_{OK_HYST}	Voltage Monitor Hysteresis	—	0.6	—	V	
T_{INT}	Temperature Monitor Threshold	—	125	150	°C	
T_{INT_HYST}	Temperature Monitor Hysteresis	—	10	—	°C	
LEDs						
V_{LED}	LED Permissible Voltage Range	-0.3	—	V_{DD} +0.3		
I_{LED_5MA}	LED Current 5.0 mA	4.5	—	5.5		
I_{LED_10MA}	LED Current 10 mA	9.0	—	11		
$BITS_{LED}$	LED Sequence Bits, Configurable; see LHLD1/2 (0x2E/0x4E) on page 25	—	8.0	—		
t_{HLDL}	Bit High Hold Time, Configurable; see LHLD1/2 (0x2E/0x4E) on page 25	50	—	800		
t_{HLDH}	Bit Low Hold Time, Configurable; see LHLD1/2 (0x2E/0x4E) on page 25	50	—	800		

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5 Functional description

5.1 Clocking

The IC is clocked by connecting an external 14.7456 MHz quartz at the XTAL1 and XTAL2 pins. It is possible to daisy chain or directly connect multiple CM3120 chips to the CLK pin for clocking. The CLK pin is then connected to the XTAL1 pin of the other chip(s). Clock feed through is enabled by default and can be disabled by pulling the CLK_EN pin high.

5.2 Operational modes

There are three possible operational modes for each CM3120 IO-Link Channels - Standard I/O, UART, and Frame Handler mode. The channel mode can be configured in the MODE register.

5.2.1 Standard I/O (SIO)

If a channel is configured in the Standard I/O mode, the mode of the output stage is freely configurable. The SIO register allows the user to choose between an N, P, or Push-Pull driving mode via the DRV bits. The TXEN and TXD bits of this register enable direct control over the output driver. The RXD bit in the MISO status nibble reflects the current state of the CQ pin.

In this mode, it is also possible to control and observe the channel using the TXEN, TXD, and RXD pins. The corresponding pin and register values get logically ORed. Therefore, either the unused pin or register values should be zero, to allow control via the desired interface. Since the sense of TXD to CQ is inverted, it is possible to connect a standard microcontroller UART interface with a high idle state to the TXD/RXD pins.

5.2.2 UART

If a channel is configured in UART mode, the output stage is set into Push-Pull mode and the output cannot be controlled via the SIO register or the external pins. It is required to define the used COM speed in the MODE register. By default, the channel listens for incoming UART transactions at the CQ pin. If a character is received, an interrupt is triggered and the data can be read back from the UART register. A transaction is started by writing the data to the UART register. The received UART data is not buffered. Receiving multiple characters, while not reading them back, causes data loss. This is indicated by the OFLW bit in the MISO status nibble.

5.2.3 Frame handler

The Frame Handler mode extends the UART interface. Like in UART mode, the output stage is set into Push-Pull mode and the output cannot be controlled via the SIO register or the external pins. It is required to define the used COM speed in the MODE register. It mostly automates the transaction of frames, defined by the IO-Link protocol. Therefore an automated CRC check for incoming and an automated CRC computation for outgoing messages is integrated. The frame handler also monitors the specified timing constraints and takes care to comply with them as well.

5.2.3.1 Device mode

Configured as a device, the frame handler listens for incoming master transactions and triggers an interrupt, if a part or the complete device message is received. The interrupt behavior can be modified using the IMSK and TRSH register. Parity or checksum errors during the transaction is indicated by the MISO status nibble. The received data can be read back via the FHD register by multiple SPI transactions or single/multiple bulk SPI transactions.

After successfully receiving an incoming master message, the frame handler waits for the user to write the complete message data into the frame buffer via the FHD register. This can be done by multiple SPI transactions or by a single bulk SPI transaction. The transaction always starts immediately after the first byte is written into the frame buffer.

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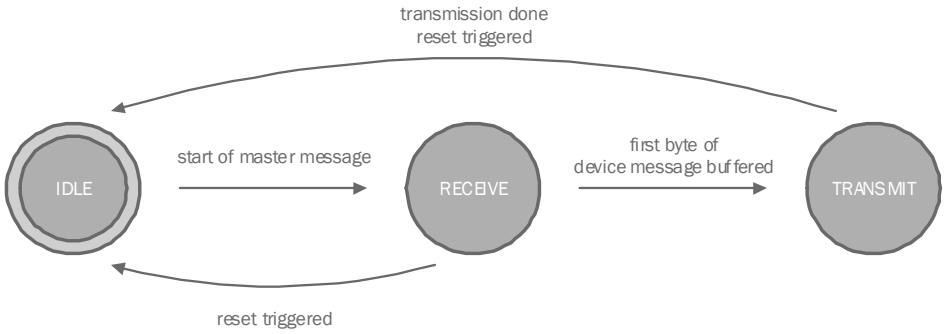

Figure 4. Device mode sequence

5.2.3.2 Skip and reset function

It is possible to reset the frame handler or skip an invalid frame from any state. This can be done by writing one to the RST or the SKIP bit of the FHC register. Skipping a frame causes the frame handler to ignore the rest of an incoming message, without triggering any additional interrupt. A soft reset is done after receiving the rest of invalid message or if a timeout was detected. Skipping a frame has no effect on the cycle timer. Resetting a frame immediately resets the frame handler into its idle state and also causes a reset of the cycle timer.

5.3 Interrupt handling

The chip utilizes two modes of interrupt handling. The active mode can be switched with the IMODE bit in the INT register. Interrupt mode 1 is active by default.

5.3.1 Mode 1

Interrupts are triggered on rising edges of the WURQ, RXRDY, TXRDY, or TOUT bits in the SPI Status. If CQ is configured as an input in SIO mode, interrupts are also triggered on any edge of the RXD bit. Changes of the STATE bits in the SPI Status also trigger interrupts, depending on the IMSK register settings. Trigger conditions can be the start of frame transmission or reception or reaching a defined fill level of the buffer. An interrupt is always triggered after a frame is completely received.

Another trigger condition is any change of values in the STAT register. This is why the microcontroller should always deal with an interrupt by reading back the STAT register. The interrupt is cleared while reading the status register.

5.3.2 Mode 2

The interrupt triggering conditions are the same as described in Interrupt mode 1. Mode 2 differs in how interrupts are handled. First, the interrupt origin can be determined by reading the INT register. The interrupt then needs to be actively cleared by the user. This is done by writing a one to the appropriate bit ISTAT, ICH1, or ICH2 in the INT register. The INTX pin remains in its active state until all interrupts are cleared.

5.3.3 Interrupt masking

To reduce the amount of triggered interrupts in frame handler mode, the user can deactivate the triggering of interrupts at certain conditions in the IMSK register. All frame handler interrupts are listed in the Table 5.

Table 5. Frame handler interrupts

Interrupt	Name	Description
SOT	Start of Transaction Interrupt	Triggers when the chip starts transmitting its message
SOR	Start of Reception Interrupt	Triggers as soon as the chip starts receiving a message
LVL	Message Level Interrupt	Triggers if a defined amount of buffered characters is reached
MSG	End of Message Interrupt	Triggers after the last character of a message was received
CYCT	Cycle Time Interrupt	Triggers when the configured cycle time has passed

The MSG interrupt is always active. By default, all other interrupts are masked. If the LVL interrupt is active, an interrupt is triggered if the input buffer reaches a defined fill level. The current amount of buffered characters can be queried in the BLVL register. The threshold for buffered characters which triggers the LVL interrupt is configured in the TRSH register.

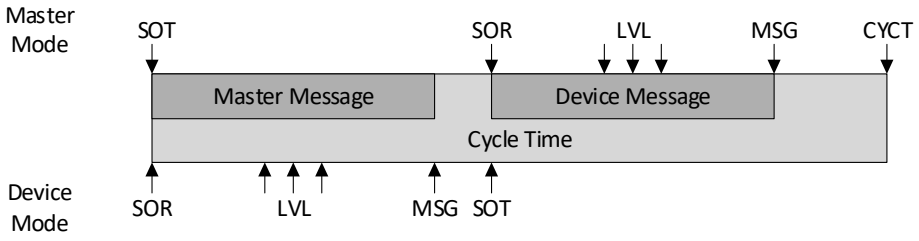

Figure 5. Interrupt Trigger Positions

It is also possible to mask the short detected (SD) interrupt of the STAT register. Otherwise an interrupt gets triggered as soon as a short is detected.

5.4 Protection features

The CM3120 IO-Link Master integrates various features to protect the IO-Link master and connected IO-Link devices. Different configuration options allow the user to take individual safety measures and to prevent damage.

5.4.1 Current sensing

5.4.1.1 Internal/external mode

There are two possible methods implemented to detect a high load at the IO-Link supply voltage - an internal and an external current sensing mechanism. Both mechanisms cannot be active at the same time. The user has to choose, which one should be used for each channel. The current sensing mode is configured by the SDINT bit in the CFG register. The SD bit in the STAT register and the SDX pins always reflect the current sensing state.

The internal current sensing mechanism does not need any external circuitry to work, but has the limitation to only detect currents IMHS and IMLS at the CM3120 CQ pin with a fixed current threshold. High currents IDEV from a connected device cannot be detected. Therefore the short protection feature for devices is not feasible in this mode. The usage of an external NMOS transistor is still possible.

The external current sensing can detect high currents IMHS and IMLS at the CQ pin and IDEV of a connected device. External shunts with a typical resistance of 0.5 Ω needs to be applied for a current threshold of 400 mA. It is possible to adjust the high current detection threshold by changing the shunts resistance value. The voltage drop over the shunt is defined with 200 mV. Current sensing over a shunt and an external NMOS transistor allow the usage of the short protection feature.

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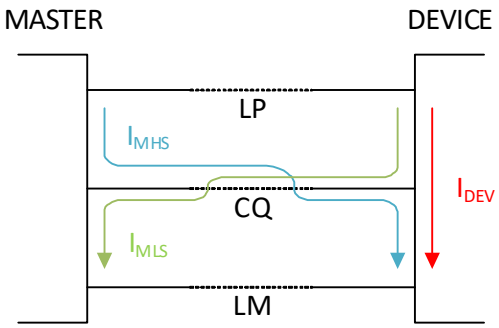


Figure 6. High Current Detection

5.4.1.2 Overload/short protection

The Overload Protection protects master and device from high loads at the channel output CQ. The output driver of a channel is automatically disabled if high currents are detected for a time > $t_{OVLDDET}$. The channel stays disabled and gets re-enabled after a time $t_{OVLDDIS}$. If the high load at CQ still persists, the channel is disabled again. This high current polling reduces the power dissipation of the chip and reduces the risk of overheating. The feature can be used in conjunction with the internal and external current sensing. Timing is configured in the OVLD register. It is also possible to disable this feature.

The short protection feature detects shorted or defective devices and disables their power supply, if NMOS transistors are used for power supply switching. If a high current is detected for a time > $t_{SHRTDIS}$, the gate driver gets disabled and the device is powered down. The gate driver stays disabled, but can be switched on again manually by the user. The feature can only be used in conjunction with the external current sensing. Timing is configured in the SHRT register.

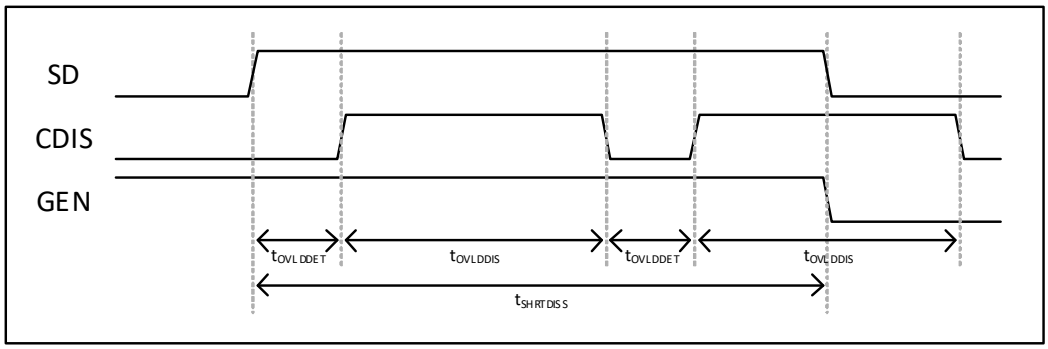


Figure 7. Overload/short protection timing

The current state of the channel (CDIS) and the gate driver (GEN) is always reflected in the STAT register. The IO-Link specification allows high currents while powering on a device. To avoid automatic disabling of the gate driver during power-on, $t_{SHRTDIS}$ should be configured > 50 ms. Time can be reduced again after the power-on phase.

5.4.2 Voltage/temperature monitoring

The chip is equipped with a voltage monitor which observes the VCC supply voltage of the chip and a temperature monitor which observes the die temperature. By default, the chip is configured to automatically disable all channels if the die temperature is too high or the VCC supply voltage is out of range. The monitor states can be read back from the PROT register. The automatic protection feature is also controlled via the PROT register.

ARCHIVE INFORMATION

5.5 Additional IO-link features

5.5.1 Automated wake-up

The automated wake-up procedure is started, if the chip is configured in SIO mode and a one is written to the WURQ bit in the SIO register. If the procedure is active, the WURQ bit is set to one and can be aborted by writing a one to the WURQ bit. During the procedure, the chip is set into frame Handler mode and runs the wake-up procedure which complies to the IO-Link standard (CM3120 reference documents on page 36 - IO-Link Spec v1.1, 7.3.2.2). After the procedure is finished, an interrupt is triggered and the chip stays in IO-Link mode. If a timeout is indicated, the procedure failed. Otherwise the chip is configured and the detected COM mode can be read back using the CFG register.

5.5.2 Cycle timer

A cycle timer is available for channels configured as a frame handler in master mode. It enables the user to comply with the configured IO-Link cycle times without further effort. The cycle time is set up in the CYCT register. The format of this register resembles the defined structure in the IO-Link.

It is possible to configure cycle times that are shorter than 400 µs. Although this is not recommended, since the standard states 400 µs as minimum cycle time (CM3120 reference documents on page 36 - IO-Link Spec v1.1, A.3.7). If the register is zero, the cycle timer gets disabled.

When the cycle timer is active, a new master message transaction will not start until the configured cycle time has passed. If the cycle time is over and no new data is available to start the message transaction, the EOC bit in the MISO Status Nibble will indicate the end of a cycle.

It is possible to reset the frame handler without resetting the cycle timer by triggering a soft reset, using the SKIP bit in the FHC register. The cycle timer will be reset together with the frame handler when a hard reset is triggered using the RST bit in the FHC register.

5.5.3 Channel synchronization

The CM3120 provides a synchronization feature which can be enabled by the SYNC bit in the FHC register. If enabled, TXD (SYNC) and RXD (CYCT) pins are used for synchronization purposes and do not have their default behavior in frame handler mode. The CYCT pins indicate if the cycle time has passed with a high level. It is also possible to enable the cycle time interrupt for a channel over the CYCT bit in the IMSK register. If this interrupt is enabled the TOUT bit in the MISO status nibble is also used to indicate the end of a cycle.

The channels waits for the start of transmission until a configured cycle time has passed. The output buffer is filled and the SYNC pin is toggled or a synchronization request is triggered over the SYNC register. This requests can be broadcasted to different chips, specifically triggering different channels on each chip by using the SMSK register. This gives a fine granularity for synchronizing channels, even over multiple chips.

Table 6. Sample configuration

Chip	MODE1/2	FHC1/2	CYCT1/2	SMSK
IC1	0h0A / 0h0A	0h0E / 0h0E	0h14 / 0h00	0h09
IC2	0h0A / 0h0A	0h0E / 0h0E	0h14 / 0h00	0h09
IC3	0h0A / 0h0A	0h0E / 0h06	0h00 / 0h00	0h04

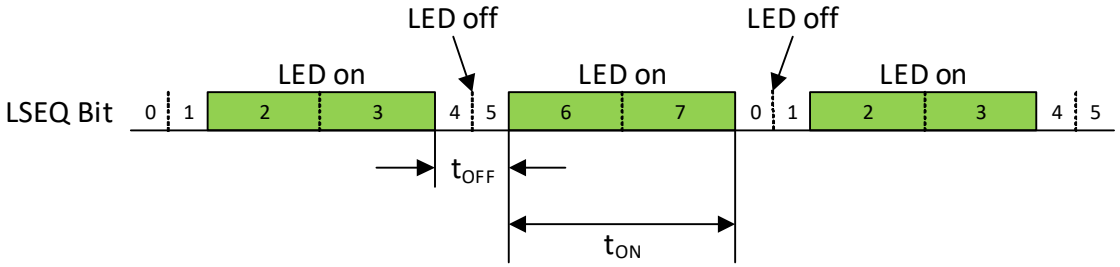
As an example, there are three CM3120 chips with the configurations from Table 6. If a synchronization request is broadcast via the SPI by writing a one to the ST1 bit in the SYNC register, channel 1 from IC1 and IC2 start their transactions as soon as the configured cycle time has passed. If a one is written to the ST2 bit of the sync register, channel 2 of IC1 and IC2 and channel 1 of IC3 start their transactions immediately.

5.5.4 LED drivers

The chip integrates an LED driver for each of the two channels. The LEDs are controlled by the LSEQ and LHLD registers. There are various ways of influencing the timing of a blinking sequence. It is also possible to synchronize the LED blinking sequences over each channel or various chips. This is done by writing one to the SYNC registers PRE and LED bits. The user can choose between two driver strengths of 5.0 mA or 10 mA using the ILED bit in the CFG register.

ARCHIVE INFORMATION

As an example, writing LSEQ 0hCC and LHLD 0h80 resembles the specified blinking sequence for channels operating in IO-Link mode, starting with the “LED off” state (CM3120 reference documents on page 36 - IO-Link Spec v1.1, 10.9.3).



t_{HLDL} = 50 ms + 50 ms * HLDL = 50 ms
t_{OFF} = 2 * t_{HLDL} = 100 ms
t_{HLDL} = 50 ms + 50 ms * HLDH = 450 ms
t_{ON} = 2 * t_{HLDL} = 900 ms

Figure 8. IO-link LED timing

5.6 Serial peripheral interface

5.6.1 Transaction format

The CM3120 is configured as an SPI slave and uses the CPOL=0, CPHA=0 configuration. During each transaction, a minimum number of two bytes must be transferred. For bulk access to the frame handler buffers via the FHD1/2 registers, n bytes can be transferred. The first byte after a falling SSX edge reflects always the current state of the two channels. The format depends on the configured modes.

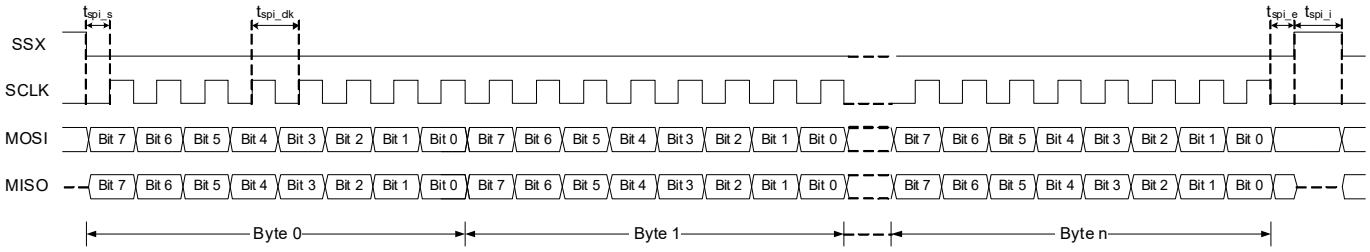


Figure 9. SPI timing diagram

ARCHIVE INFORMATION

5.6.2 MOSI format

Table 7. Mosi Format

Bit	7	6	5	4	3	2	1	0
1st Byte	ADR							RW
2nd Byte	DATA							
	…							
nth Byte	DATA							

ADR		Address for register access
	0x20-0x3F	Channel 1 registers
	0x40-0x5F	Channel 2 registers
	0x60-0x7F	Control registers
RW		Register access type
	0b0	write to address
	0b1	read from address
DATA		Value for write access
	0x00-0xFF	3rd -nth byte is optional; ignored on read access

5.6.3 MISO format

Table 8. MISO Format

Bit	7	6	5	4	3	2	1	0
1st Byte	STAT2				STAT1			
2nd Byte	DATA							
	…							
nth Byte	DATA							

STAT1/2		Status code for channel 1/2
	0x0-0xF	Format is dependent on configured mode
DATA		Current value on read access to register
	0x00-0xFF	3rd -nth byte is optional; not valid on write access

ARCHIVE INFORMATION

5.6.4 MISO status nibble

Table 9. MISO status nibble

Name	STAT Bit 3	STAT Bit 2	STAT Bit 1	STAT Bit 0
Standard I/O	WURQ	RXD	TXEN	TXD
UART	OFLW	RXERR	RXRDY	TXRDY
Frame Handler	TOUT/EOC	STATE		

TXD		Current channel output value
	0b0	Channel is driven high
	0b1	Channel is driven low
TXEN		Current output enable state
	0b0	Channel driver is disable
	0b1	Channel driver is enabled
RXD		Current channel input value
	0b0	Channel input is driven high
	0b1	Channel input is driven low
WURQ		Wake-up pulse indicator
	0b0	No wake-up pulse is detected
	0b1	Wake-up pulse is detected
TXRDY		UART transmit state indicator
	0b0	TX is busy
	0b1	TX us ready for transmission
RXRDY		UART receive state indicator
	0b0	RX is busy
	0b1	RX is ready for receiving
RXERR		UART RX parity error
	0b0	no parity error detected
	0b1	parity error detected
OFLW		UART RX overflow indicator
	0b0	no data overflow detected
	0b1	data overflow is detected, byte is lost
STATE		Reflects the current frame handler state
	0b000	Idle
	0b001	transmission output required
	0b010	transmission active; no further output required
	0b011	transmission active; further output required
	0b100	receiving active
	0b101	receiving active; new input available
	0b110	receiving active; message erroneous
	0b111	receiving active; message erroneous; new input available

ARCHIVE INFORMATION

Table 9. MISO status nibble (continued)

TOUT/EOC		Frame timeout / End of cycle time
	0b0	no timeout detected / cycle time not passed
	0b1	timeout detected / cycle time passed

5.7 Register description

5.7.1 Register overview

Table 10. Register description

Address	Name	Description	Access
0x00-0x1F	-	Reserved	-
0x20	MODE1	Channel 1 – Mode	R/W
0x21	OVLD1	Channel 1 – Overload Protection	R/W
0x22	SHRT1	Channel 1 – Short Protection	R/W
0x23	SIO1	Channel 1 – SIO Control	R/W
0x24	UART1	Channel 1 – UART Data	R/W
0x25	FHC1	Channel 1 – FH Control	R/W
0x26	OD1	Channel 1 – On-Request Length	R/W
0x27	MPD1	Channel 1 – Master PD Length	R/W
0x28	DPD1	Channel 1 – Device PD Length	R/W
0x29	CYCT1	Channel 1 – Cycle Time	R/W
0x2A	FHD1	Channel 1 – FH Data	R/W
0x2B	BLVL1	Channel 1 – FH Buffer Level	R
0x2C	IMSK1	Channel 1 – Interrupt Masking	R/W
0x2D	LSEQ1	Channel 1 – LED Sequence	R/W
0x2E	LHLD1	Channel 1 – LED Hold Times	R/W
0x2F	CFG1	Channel 1 – Configuration	R/W
0x30	TRSH1	Channel 1 – Threshold Level	R/W
0x31-0x3F	-	Reserved	-
0x40	MODE2	Channel 2 – Mode	R/W
0x41	OVLD2	Channel 2 – Overload Protection	R/W
0x42	SHRT2	Channel 2 – Short Protection	R/W
0x43	SIO2	Channel 2 – SIO Control	R/W
0x44	UART2	Channel 2 – UART Data	R/W
0x45	FHC2	Channel 2 – FH Control	R/W
0x46	OD2	Channel 2 – On-Request Length	R/W
0x47	MPDL2	Channel 2 – Master PD Length	R/W
0x48	DPDL2	Channel 2 – Device PD Length	R/W
0x49	CYCT2	Channel 2 – Cycle Time	R/W
0x4A	FHD2	Channel 2 – FH Data	R/W

ARCHIVE INFORMATION

Table 10. Register description (continued)

Address	Name	Description	Access
0x4B	BLVL2	Channel 2 – FH Buffer Level	R
0x4C	IMSK2	Channel 2 – Interrupt Masking	R/W
0x4D	LSEQ2	Channel 2 – LED Sequence	R/W
0x4E	LHLD2	Channel 2 – LED Hold Times	R/W
0x4F	CFG2	Channel 2 – Configuration	R/W
0x50	TRSH2	Channel 2 – Threshold Level	R/W
0x51-0x5F	-	reserved	-
0x60	STAT	IC Status	R
0x61	SMSK	Channel Synchronization Masks	R/W
0x62	SYNC	Synchronization Triggers	W
0x63	PROT	Channel Protection	R/W
0x64	INT	Interrupt Register	R/W
0x65-0x6F	-	Reserved	-
0x70	REV	Revision Code	R
0x71-0x7F	-	Reserved	-

5.7.2 MODE1/2 (0x20/0x40)

Table 11. MODE1/2 (0x20/0x40)

Bit	7	6	5	4	3	2	1	0
Name	Reserved				COM		MODE	
Access	-				R/W		R/W	

Default:0b00000000

MODE		Selects the channel operation mode
	0b00	Standard I/O
	0b01	UART
	0b10	Frame Handler
	0b11	reserved
COM		Selects the UART communication speed
	0b00	Disabled
	0b01	COM1 – 4.8 kBd
	0b10	COM2 – 38.4 kBd
	0b11	COM3 – 230.4 kBd

ARCHIVE INFORMATION

5.7.3 OVLD1/2 (0x21/0x41)

Table 12. OVLD1/2 (0x21/0x41)

Bit	7	6	5	4	3	2	1	0
Name	ADIS		MULT					
Access	R/W		R/W					

Default:0b10000000

ADIS		Channel overload protection mode
	0b00	Disabled
	0b01	Enabled; FACTOR=10
	0b10	Enabled; FACTOR=100
	0b11	Enabled; FACTOR=1000
MULT		Multiplier for overload detection/disable time
	0-63	Multiplier value

NOTE: disabling this feature may cause damage to master and/or device
$t_{OVLDDET}$ = 100 µs + 100 µs * MULT
$t_{OVLDDIS}$ = $t_{OVLDDET}$ * FACTOR

5.7.4 SHRT1/2 (0x22/0x42)

Table 13. SHRT1/2 (0x22/0x42)

Bit	7	6	5	4	3	2	1	0
Name	BASE		MULT					
Access	R/W		R/W					

Default:0b00000101

BASE		Base/offset for channel short detection time
	0b00	BASE is 100 µs; OFFSET is 100 µs; disabled if MULT is 0
	0b01	BASE is 400 µs; OFFSET is 6.8 ms
	0b10	BASE is 1.6 ms; OFFSET is 33.6 ms
	0b11	BASE is 3.2 ms; OFFSET is 134.4 ms
MULT		Multiplier for short detection time
	0-63	Multiplier value

NOTE: disabling this feature may cause damage to master and/or device
$t_{SHRTDET}$ = OFFSET + BASE * MULT

ARCHIVE INFORMATION

5.7.5 SIO1/2 (0x23/0x43)

Table 14. SIO1/2 (0x23/0x43)

Bit	7	6	5	4	3	2	1	0
Name	WURQ	reserved			DRV		TXEN	TXD
Access	R/W	-			R/W		R/W	R/W

Default:0b00001100

TXD		Driver output value
	0b0	Drive CQ high
	0b1	Drive CQ low
TXEN		Driver output state
	0b0	Disable output driver
	0b1	Enable output driver
DRV		Driver output mode
	0b00	Multiplier value
	0b01	N-mode
	0b10	P-mode
	0b11	Push-Pull
WURQ		Start/abort automated wake-up procedure
	0b0	Automated wake-up is not running; writing 0b1 starts procedure
	0b1	Automated wake-up is running; writing 0b1 aborts procedure

5.7.6 UART1/2 (0x24/0x44)

Table 15. UART1/2 (0x24/0x44)

Bit	7	6	5	4	3	2	1	0
Name	DATA							
Access	R/W							

Default:0b00000000

DATA		Received/transmitted value over UART
	0-255	read returns received value, write transmits value

ARCHIVE INFORMATION

5.7.7 FHC1/2 (0x25/0x45)

Table 16. FHC1/2 (0x25/0x45)

Bit	7	6	5	4	3	2	1	0
Name	RST	SKIP	reserved		SYNC	MAS	CRC	TOUT
Access	W	W	-		R/W	R/W	R/W	R/W

Default:0b00000110

TOUT		Timeout behavior
	0b0	Strict timeout detection
	0b1	Relaxed timeout detection (+ 3 t_{BIT})
CRC		Automatic checksum calculation
	0b0	Disabled, sending a master message will start immediately
	0b1	Enabled
MAS		Frame handler mode
	0b0	Slave mode
	0b1	Master mode
SYNC		Channel synchronization
	0b0	Disabled
	0b1	Enabled; master mode only
SKIP		Skip a frame
	0b1	Resets frame handler without resetting cycle time counter
RST		Reset frame handler
	0b1	Resets frame handler and cycle time counter

5.7.8 OD1/2 (0x26/0x46)

Table 17. OD1/2 (0x26/0x46)

Bit	7	6	5	4	3	2	1	0
Name	LEN							
Access	R/W							

Default:0b00000001

LEN		On-Request Data length
	1-32	Data length in bytes; valid values according to IO-Link spec: 1, 2, 8, 32. See CM3120 reference documents on page 36

ARCHIVE INFORMATION

5.7.9 MPD1/2 (0x27/0x47)

Table 18. MPD1/2 (0x27/0x47)

Bit	7	6	5	4	3	2	1	0
Name	LEN							
Access	R/W							

Default:0b00000000

LEN		Master Process Data length
	0-32	Data length in bytes

5.7.10 DPD1/2 (0x28/0x48)

Table 19. DPD1/2 (0x28/0x48)

Bit	7	6	5	4	3	2	1	0
Name	LEN							
Access	R/W							

Default:0b00000000

LEN		Device Process Data length
	0-32	Data length in bytes

5.7.11 CYCT1/2 (0x29/0x49)

Table 20. CYCT1/2 (0x29/0x49)

Bit	7	6	5	4	3	2	1	0
Name	BASE		MULT					
Access	R/W		R/W					

Default:0b00000000

BASE		Base/offset for cycle time
	0b00	BASE is 100 µs; no OFFSET; disabled if MULT is 0
	0b01	BASE is 400 µs; OFFSET is 6.4 ms
	0b10	BASE is 1.6 ms; OFFSET is 32 ms
	0b11	Reserved
MULT		Multiplier for cycle time
	0-63	Multiplier value

t_{CYC} = OFFSET + BASE * MULT

ARCHIVE INFORMATION

5.7.12 FHD1/2 (0x2A/0x4A)

Table 21. FHD1/2 (0x2A/0x4A)

Bit	7	6	5	4	3	2	1	0
Name	DATA							
Access	R/W							

Default:0b00000000

DATA		Received/transmitted value over frame handler
	0-255	Read returns buffed input data, write buffers output data

5.7.13 BLVL1/2 (0x2B/0x4B)

Table 22. BLVL1/2 (0x2B/0x4B)

Bit	7	6	5	4	3	2	1	0
Name	FCNT							
Access	R/W							

Default:0b00000000

FCNT		Fill count of frame handler input buffer
	0-64	Current input buffer fill count

5.7.14 IMSK1/2 (0x2C/0x4C)

Table 23. IMSK1/2 (0x2C/0x4C)

Bit	7	6	5	4	3	2	1	0
Name	reserved			SD	SOR	SOT	CYCT	LVL
Access	-			R/W	R/W	R/W	R/W	R/W

Default:0b00011111

LVL		Level interrupt
	0b0	Enabled; interrupt trigger level is defined in corresponding TRSH registers
	0b1	Disabled; no interrupt is triggered
CYCT		Cycle time interrupt
	0b0	Enabled; interrupt is triggered after end of cycle, only in master mode
	0b1	Disabled; no interrupt is triggered
SOT		Start of transmission interrupt
	0b0	Enabled; interrupt is triggered on start of transmission
	0b1	Disabled; no interrupt is triggered
SOR		Start of reception interrupt
	0b0	Enabled; interrupt is triggered on start of reception
	0b1	Disabled; no interrupt is triggered
SD		Short detection interrupt
	0b0	Enabled; interrupt is directly triggered when a short gets detected
	0b1	Disabled; no interrupt is triggered

5.7.15 LSEQ1/2 (0x2D/0x4D)

Table 24. LSEQ1/2 (0x2D/0x4D)

Bit	7	6	5	4	3	2	1	0
Name	SEQ							
Access	R/W							

Default:0b00000000

SEQ		LED blinking sequence
	0x00	Always off
	0x01-0xFE	Blinking; 0b0 represents off-state; 0b1 represents on-state; LSB processed first
	0xFF	Always on

ARCHIVE INFORMATION

5.7.16 LHLD1/2 (0x2E/0x4E)

Table 25. LHLD1/2 (0x2E/0x4E)

Bit	7	6	5	4	3	2	1	0
Name	HLDH				HLDL			
Access	R/W				R/W			

Default:0b00000000

HLDL		LED hold time configuration for off-state
	0-15	Base time multiplier
HLDH		LED hold time configuration for on-state
	0-15	Base time multiplier

t_{HLDL} = 50 ms + 50 ms * HLDL
t_{HLDH} = 50 ms + 50 ms * HLDH

5.7.17 CFG1/2 (0x2F/0x4F)

Table 26. CFG1/2 (0x2F/0x4F)

Bit	7	6	5	4	3	2	1	0
Name	GEN	reserved			ILED	SDINT	RAT	ICQ
Access	R/W	-			R/W	R/W	R/W	R/W

Default:0b00000000

ICQ		Current sink configuration for C/Q
	0b0	Current sink disabled
	0b1	10 mA current sink enabled
RAT		Input threshold configuration for C/Q
	0b0	Static input threshold according to IO-Link specification. See CM3120 reference documents on page 36
	0b1	Ratiometric input threshold for lower LP voltages
SDINT		Short detection mode
	0b0	External short detection; shunt required
	0b1	Internal short detection; no shunt required
ILED		LED driving current
	0b0	5.0 mA driving current
	0b1	10 mA driving current
GEN		Gate driver enable
	0b0	Disabled
	0b1	Enabled

ARCHIVE INFORMATION

5.7.18 TRSH1/2 (0x30/0x50)

Table 27. TRSH1/2 (0x30/0x50)

Bit	7	6	5	4	3	2	1	0
Name	TLVL							
Access	R/W							

Default:0b00000000

TLVL		Input buffer threshold level
	0-63	Trigger interrupt after TLVL received characters; activate in IMSK register

5.7.19 STAT (0x60)

Table 28. STAT (0x60)

Bit	7	6	5	4	3	2	1	0
Name	TEMP	VCCOK	GDIS2	CDIS2	SD2	GDIS1	CDIS1	SD1
Access	R	R	R	R	R	R	R	R

Default:0b01100100

SD1/2		Short detected indicator
	0b0	No short detected
	0b1	Short detected
CDIS1/2		Channel disabled indicator
	0b0	Channel driver enabled
	0b1	Channel driver disabled
GDIS1/2		Gate disabled indicator
	0b0	Gate driver enabled
	0b1	Gate driver disabled
VCCOK		VCC Voltage monitor
	0b0	Voltage too high/low
	0b1	Voltage inside valid range; (VCC_{OK_MIN} < VCC) or (VCC > VCC_{OK_MAX})
TEMP		Temperature monitor
	0b0	Temperature okay; $\vartheta_{JUNC} \leq \vartheta_{INT}$
	0b1	High temperature detected; $\vartheta_{JUNC} > \vartheta_{INT}$

ARCHIVE INFORMATION

5.7.20 SMSK (0x61)

Table 29. SMSK (0x61)

Bit	7	6	5	4	3	2	1	0
Name	SC4		SC3		SC2		SC1	
Access	R/W		R/W		R/W		R/W	

Default:0b00000000

SC1-4 Synchronization masks 1-4

- 0b00 disable synchronization signals
- 0b01 enable synchronization signal for channel 1
- 0b10 enable synchronization signal for channel 2
- 0b11 enable synchronization signals for channels 1 and 2

5.7.21 SYNC (0x62)

Table 30. SYNC (0x62)

Bit	7	6	5	4	3	2	1	0
Name	reserved		PRE	LED	ST4	ST3	ST2	ST1
Access	-		W	W	W	W	W	W

Default:0b00000000

ST1-4 Synchronous start of transmission trigger

- 0b1 Write 0b1 to trigger start of transmission; depends on corresponding SC1-4 mask

LED LED output synchronization

- 0b1 Write 0b1 to trigger synchronization

PRE LED prescaler synchronization

- 0b1 Write 0b1 to trigger synchronization

ARCHIVE INFORMATION

5.7.22 PROT (0x63)

Table 31. PROT (0x63)

Bit	7	6	5	4	3	2	1	0
Name	reserved	TEMP	VCCH	VCCL	reserved	PTEMP	PVCCH	PVCCL
Access	-	R	R	R	-	R/W	R/W	R/W

Default:0b00000111

PVCCL		VCC low voltage protection
	0b0	Protection disabled
	0b1	Protection enabled; disable outputs driver if VCC < VCC_{OK_MIN}
PVCCH		VCC high voltage protection
	0b0	Protection disabled
	0b1	Protection enabled; disable outputs driver if VCC > VCC_{OK_MAX}
PTEMP		High temperature protection
	0b0	Protection disabled
	0b1	Protection enabled; disable output driver if $\vartheta_{JUNC} > \vartheta_{INT}$
VCCL		VCC low voltage monitor
	0b0	Voltage not too low
	0b1	Voltage too low; $VCC < VCC_{OK\_MIN}$
VCCH		VCC high voltage monitor
	0b0	Voltage not too high
	0b1	Voltage too high; $VCC > VCC_{OK\_MAX}$
TEMP		Temperature monitor
	0b0	Temperature okay; $\vartheta_{JUNC} \leq \vartheta_{INT}$
	0b1	High temperature detected; $\vartheta_{JUNC} > \vartheta_{INT}$

ARCHIVE INFORMATION

5.7.23 INT (0x64)

Table 32. INT (0x64)

Bit	7	6	5	4	3	2	1	0
Name	IMODE	reserved				ISTAT	ICH2	ICH1
Access	R/W	-				R/W	R/W	R/W

Default:0b00000000

ICH1/2		Channel 1/2 interrupt
	0b0	No channel 1/2 interrupt
	0b1	Channel 1/2 interrupt occurred; write 0b1 to clear
ISTAT		Status interrupt
	0b0	No status interrupt
	0b1	Status interrupt occurred; write 0b1 to clear
IMODE		Interrupt mode
	0b0	Interrupt mode 1
	0b1	Alternative interrupt mode 2

5.7.24 REV (0x70)

Table 33. REV (0x70)

Bit	7	6	5	4	3	2	1	0
Name	MAJ				MIN			
Access	R				R			

Default:0b00100001

MAJ		Major revision code
	2	Latest major revision code
MIN		Minor revision code
	1	Latest minor revision code

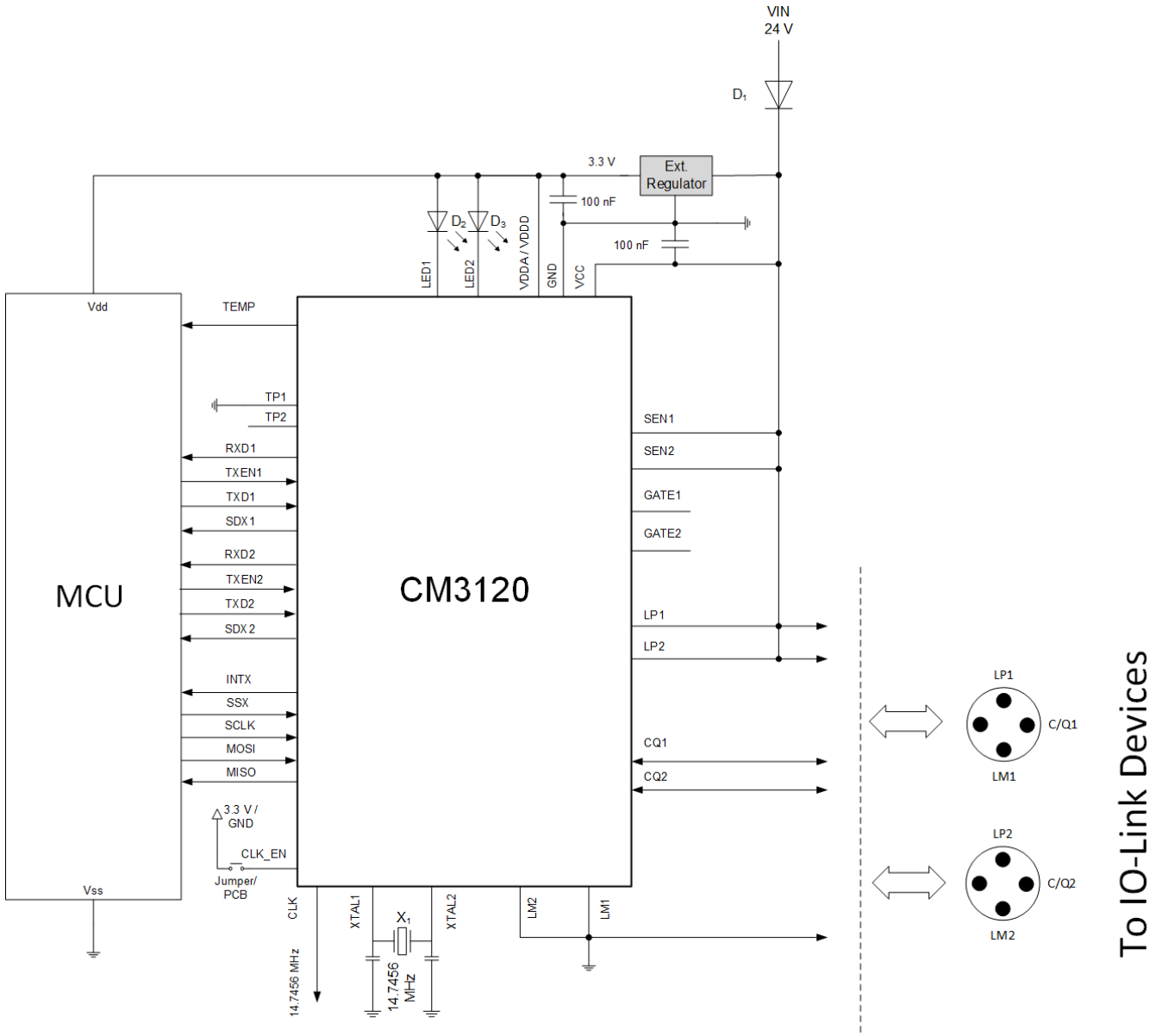
ARCHIVE INFORMATION

6 Typical applications

6.1 Introduction

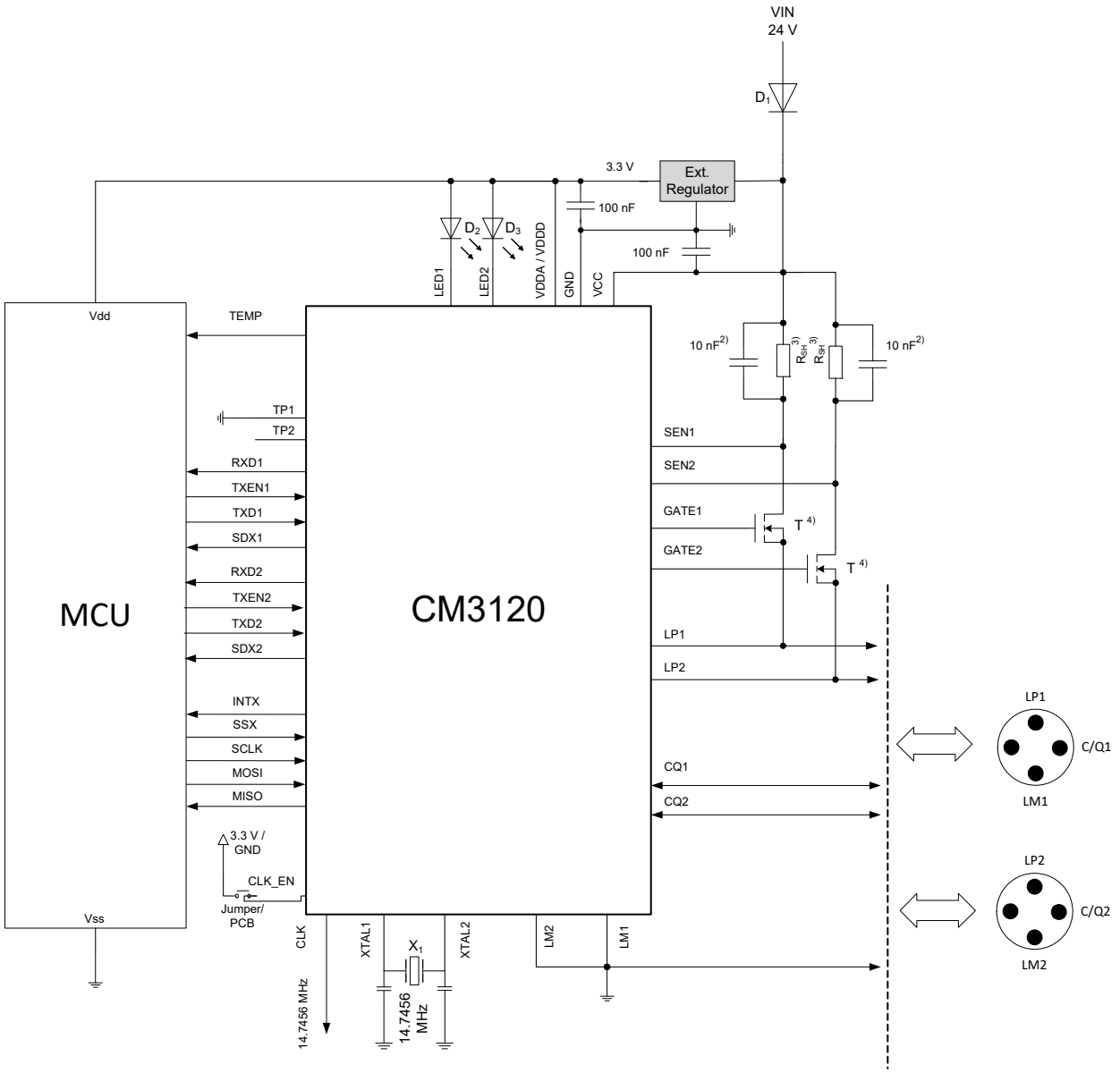
The CM3120 can be configured in different applications. Figure 10 and Figure 11 show the CM3120 in a typical application.

6.1.1 Application diagram



1) Surge protection circuitry for channels needs to be applied externally.

Figure 10. Application diagram using internal drivers/internal current sense

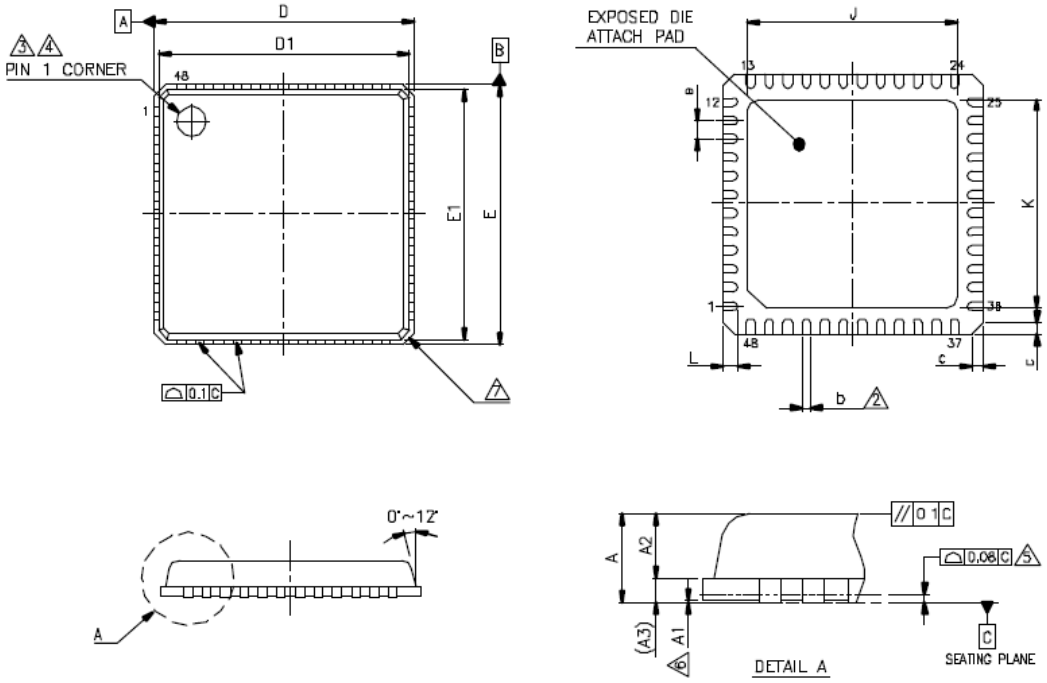


1) Surge protection circuitry for channels needs to be applied externally.
2) Optional
3) Typically 0.5 Ω
4) e.g. PMPB85ENEA

Figure 11. Application diagram using external drivers/external current sense

7 Packaging

7.1 Package mechanical dimensions



ARCHIVE INFORMATION

Symbol	A	A1	A2	A3	b	C	D	D1	E	E1	e	J	K	L
Min	0.80	0.00	0.65	0.203 REF.	0.18	0.24	7.00 BSC.	6.75 BSC.	7.00 BSC.	6.75 BSC.	0.50 BSC.	3.50	3.50	0.30
Typ	0.90	0.02	-		0.25	0.42						3.70	3.70	0.40
Max	1.00	0.05	1.00		0.30	0.60						3.90	3.90	0.50

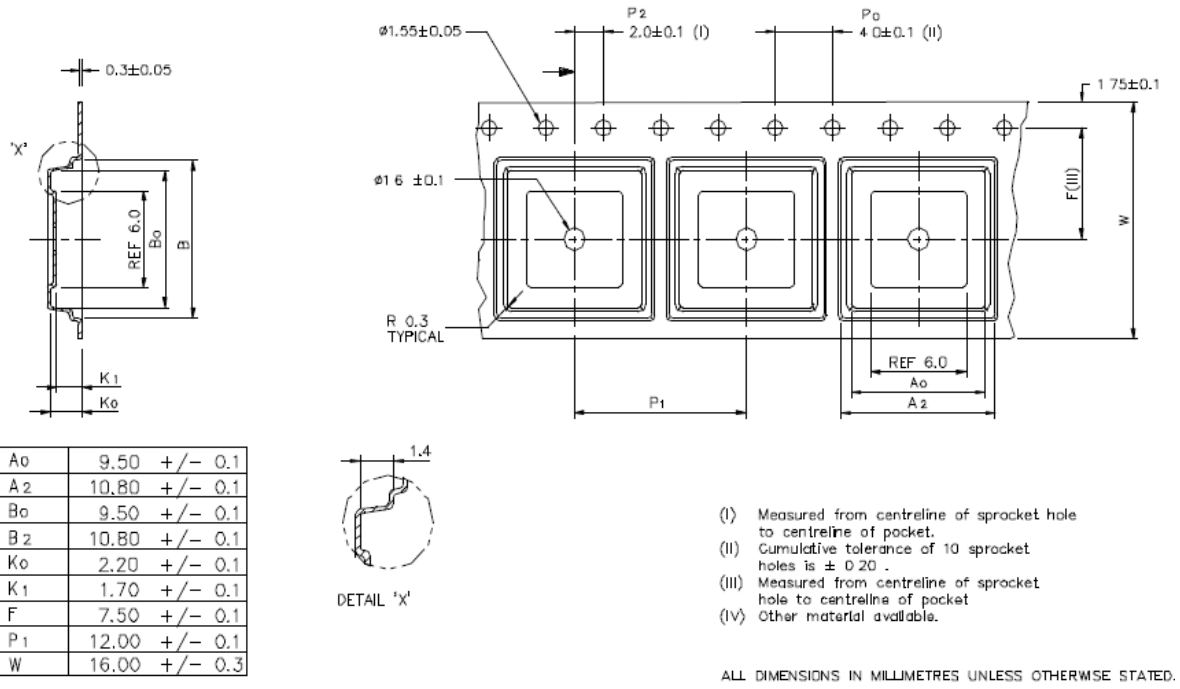
UNIT: mm

NOTES :
1. JEDEC : MO-220-J.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (0.012 INCHES MAXIMUM).
3. DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
7. APPLIED ONLY TO TERMINALS.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

ARCHIVE INFORMATION

8 Tape and reel information

8.1 Tape package

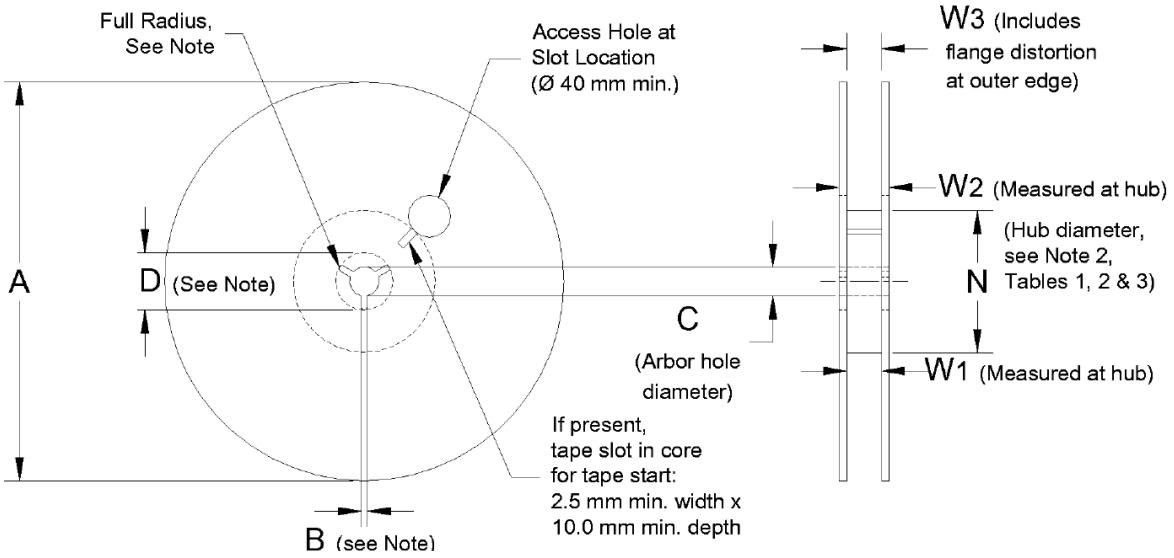


Ao	9.50 +/− 0.1
A2	10.80 +/− 0.1
Bo	9.50 +/− 0.1
B2	10.80 +/− 0.1
Ko	2.20 +/− 0.1
K1	1.70 +/− 0.1
F	7.50 +/− 0.1
P1	12.00 +/− 0.1
W	16.00 +/− 0.3

Figure 12. Tape package

ARCHIVE INFORMATION

8.2 Reel information



Symbol	A	B	C	D	W_1 QFN48
Min	-	1.5	12.8	20.2	17.25
Typ	-	-	13.0	-	-
Max	330	-	13.5	-	17.75

Figure 13. Reel package

9 Reference section

Table 34. CM3120 reference documents

Description	URL
Reference web sites	**Reference URL locations**
IO-Link Interface and System	http://www.io-link.com/share/Downloads/Spec-Interface/IOL-Interface-Spec_10002_V112_Jul13.pdf

10 Revision history

Revision	Date	Description of changes
1.0	9/2015	• Initial release
	8/2016	• Updated to NXP document form and style

ARCHIVE INFORMATION

How to Reach Us:

Home Page:
NXP.com

Web Support:
http://www.nxp.com/support

Document Number: CM3120
Rev. 1.0
7/2016

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