WINSOURCE ELECTRONICS

THE DATASHEET OF

MAX31341CETB+T

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MAX31341B/ MAX31341C

Low-Current, Real-Time Clock with I²C Interface and Power Management

General Description

The MAX31341B/MAX31341C low-current, real-time clock (RTC) is a time-keeping device that provides nanoamperes time-keeping current, extending battery life. The MAX31341B/MAX31341C supports 6pF high-ESR crystals, which broaden the pool of usable crystals for the devices. This device is accessed through an I²C serial interface. The device features one digital Schmitt trigger input and one programmable threshold analog input. The device generates an interrupt output on a falling or rising edge of the digital input (D1), or when the analog input (AIN) voltage crosses a programmed threshold in either direction. An integrated power-on reset function ensures deterministic default register status upon power-up.

Other features include two time-of-day alarms, interrupt outputs, a programmable square-wave output, a serial bus timeout mechanism, and a 64-byte RAM for user data storage. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in 24-hour format. The MAX31341B/MAX31341C also includes an input for synchronization. When a reference clock (e.g., 32kHz, 50Hz/60Hz Power Line, GPS 1PPS) is present at the CLKIN pin and the enable external clock input bit (ECLK) is set to 1, the MAX31341B/MAX31341C RTC is frequency-locked to the external clock and the clock accuracy is determined by the external source.

The device is available in a lead (Pb)-free/RoHS-compliant, 12-pin, 2mm x 1.5mm WLP with 0.5mm pitch and a 10-pin, 3mm x 3mm TDFN. The device supports the -40°C to +85°C extended temperature range.

Applications

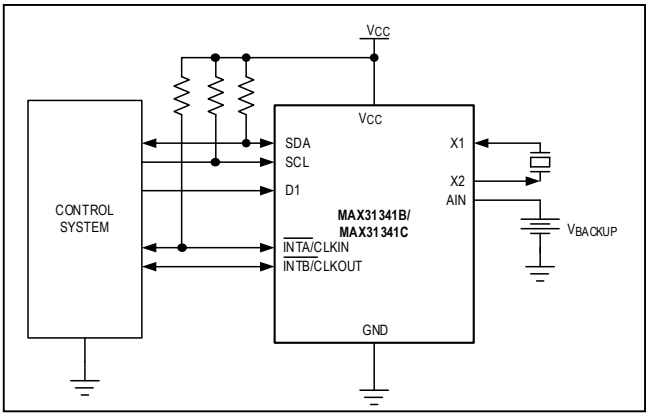
- Medical
- Wearables
- Point-of-Sale (POS)
- Telematics
- Portable Instruments
- Portable Audio

Ordering Information appears at end of data sheet.

Benefits and Features

- Increases Battery Life
  - 180nA Timekeeping Current
  - Wide Range of External Crystals with C_L = 6pF and ESR up to 100kΩ for Minimal Current Draw
  - Trickle Charger for External Super Capacitor or Rechargeable Battery
- Provides Flexible Configurability
  - A Schmitt Trigger Input to Trigger Interrupt
  - One Analog Input with Adjustable Threshold to Trigger Interrupt
  - Programmable Square-Wave Output for Clock Monitoring
- Saves Board Space
  - Integrated Load Capacitors for Crystal Oscillator
  - 2mm x 1.5mm, 12-Bump WLP with 0.5mm Pitch
  - 3mm x 3mm, 10-pin TDFN
- Value Add Features for Ease-of-Use
  - +1.6V to +3.6V Operating Voltage Range
  - Countdown Timer with Repeat and Pause Functions
  - 64-Byte RAM for User Data Storage
- Integrated Protection
  - Power-On Reset for Default Configuration
  - Automatic Switchover to Backup Battery or Super Capacitor on Power Fail
  - Lockup-Free Operation with Bus Timeout

Typical Operating Circuit



maxim integrated™

Absolute Maximum Ratings

Voltage Range on Any Pin Relative to Ground -0.3V to +6V
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -55°C to +150°C
Soldering Temperature ..... See the IPC/JEDEC J-STD-020A Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

12 WLP

PACKAGE CODE	W121A2+1
Outline Number	21-0009
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	49°C/W
Junction to Case (θ_{JC})	N/A

10 TDFN

PACKAGE CODE	T1033-4
Outline Number	21-0137
Land Pattern Number	90-0061
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	54°C/W
Junction to Case (θ_{JC})	9°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	41°C/W
Junction to Case (θ_{JC})	9°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{CC} = +1.6V to +3.6V, typical values at V_{CC} = +3.0V, unless otherwise noted. Limits are 100% tested at T_A = +25°C. Note 1.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Operating Voltage Range	V_{CC}	Full operation (Note 2)	1.6		3.6	V
Minimum Timekeeping Voltage	V_{CCTMIN}	(Note 2, Note 3)		1.0		V
Timekeeping Current: CLKIN = GND or CLKIN = V_{CC}	I_{CCT}	V_{CC} = +1.6V (Note 3)		180	330	nA
		V_{CC} = +3.0V		210	370	
		V_{CC} = +3.6V		220	390	
Data Retention Current (Oscillator Stopped and I²C Enabled)	I_{BATDR}			5		nA
Maximum Supply Power-Up Slew Rate	T_{VCCR}			3		V/µs
Maximum Supply Switchover Slew Rate	T_{VCCF}	Power-fail voltage = 2.2V		1.4		V/ms
BATTERY BACKUP AND ANALOG THRESHOLD (AIN)						
Backup Supply Voltage	V_{AIN}		1.6		3.6	V
Comparator Threshold Voltage	V_{TH1}	Programmable Power-Fail Voltage if *Power Management* mode is enabled through I²C		1.3		V
	V_{TH2}			1.7		
	V_{TH3}			2.0		
	V_{TH4}			2.2		
Trickle-Charge Current-Limiting Resistance	R1	Measured at V_{AIN} = 0V		3.3		kΩ
	R2	Measured at V_{AIN} = 0V		6.4		
	R3	Measured at V_{AIN} = 0V		11.3		
SCHMITT TRIGGER INPUT (D1)						
Rising Input Threshold Voltage	V_{T+}	V_{CC} = 3.0V		1.65	2	V
		V_{CC} = 1.6V		0.9	1.25	
Falling Input Threshold Voltage	V_{T-}	V_{CC} = 3.0V	0.7	0.9		V
		V_{CC} = 1.6V	0.35	0.6		
Input Leakage	I_{LI}		-0.1		+0.1	µA
LOGIC INPUTS AND OUTPUTS						
Logic 1 Input	V_{IH}	V_{CC} = 1.6V (Note 1, Note 2)	0.75 x V_{CC}		V_{CC} + 0.3	V
		V_{CC} = 3.0V (Note 1, Note 2)	0.7 x V_{CC}		V_{CC} + 0.3	
Logic 0 Input	V_{IL}	(Note 1, 2)	-0.3		0.3 x V_{CC}	V

Electrical Characteristics (continued)

(V_{CC} = +1.6V to +3.6V, typical values at V_{CC} = +3.0V, unless otherwise noted. Limits are 100% tested at T_A = +25°C. Note 1.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage (SCL, CLKIN/$\overline{INTA}$)	I_{IL}	Input clock enabled	-0.1		+0.1	µA
Output Leakage (CLKIN/$\overline{INTA}$, CLKOUT/$\overline{INTB}$)	I_O	Input clock disabled	-1.0		+1.0	µA
Output Logic 1 V_{OH} = +1.0V (CLKOUT/$\overline{INTB}$)	I_{OH}	V_{CC} ≥ 1.6V	-1.0			mA
Output Logic 0, V_{OL} = +0.4V (SDA, CLKIN/$\overline{INTA}$, CLKOUT/$\overline{INTB}$)	I_{OL}	V_{CC} ≥ 1.6V	2			mA
AC ELECTRICAL CHARACTERISTICS						
SCL Clock Frequency	f_{SCL}	(Note 4)	10		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(Note 5)	0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Note 6, Note 7)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	V_{CC} = 3.0V (Note 8)	100			ns
Setup Time for a Repeated, START Condition	$t_{SU:STA}$		0.6			µs
Minimum Rise Time of Both SDA and SCL Signals	t_{RMIN}	(Note 9)		20 + $0.1C_B$		ns
Maximum Rise Time of Both SDA and SCL Signals	t_{RMAX}			300		ns
Minimum Fall Time for Both SDA and SCL Signals	t_{FMIN}	(Note 9)		20 + $0.1C_B$		ns
Maximum Fall Time for Both SDA and SCL Signals	t_{FMAX}			300		ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Maximum Capacitive Load for Each Bus Line	C_B	(Note 9)		400		pF
I/O Capacitance	$C_{I/O}$	(Note 10)		10		pF
SCL Spike Suppression	t_{SP}	(Note 10)		37		ns
Oscillator Stop Flag (OSF) Delay	t_{OSF}	(Note 11)		30	100	ms
Timeout Interval	$t_{TIMEOUT}$	(Note 12)	25		35	ms

Electrical Characteristics – Crystal Parameters

(V_{CC} = +1.6V to +3.6V, typical values at V_{CC} = +3.0V, unless otherwise noted. Limits are 100% tested at T_A = +25°C. Note 1.)

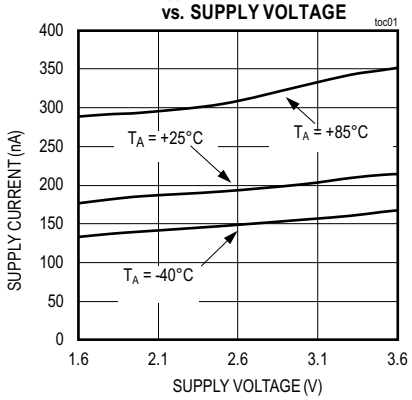
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O			32.768		kHz
Maximum Series Resistance	ESR			100		kΩ
Load Capacitance	C_L			6		pF

Note 1: Limits at -40°C and +85°C are guaranteed by design; not production tested.
Note 2: Voltage referenced to ground.
Note 3: Specified with I^2C bus inactive. Oscillator operational. (INTCN = 1, ECLK = 0).
Note 4: The minimum SCL clock frequency is limited by the bus timeout feature, which resets the serial bus interface if SCL is held low for $t_{TIMEOUT}$.
Note 5: After this period, the first clock pulse is generated.
Note 6: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 7: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.
Note 8: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geq 250ns$ must then be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT} = 1000 + 250 = 1250ns$ before the SCL line is released.
Note 9: C_B is the total capacitance of one bus line, including all connected devices, in pF.
Note 10: Guaranteed by design; not 100% production tested.
Note 11: The parameter t_{OSF} is the period of time the oscillator must be stopped for the OSF flag to be set over V_{CC} range.
Note 12: The MAX31341B/MAX31341C can detect any single SCL clock held low longer than $t_{TIMEOUTMIN}$. The device I^2C interface is in reset state and can receive a new START condition when SCL is held low for at least $t_{TIMEOUTMAX}$. Once the device detects this condition, the SDA output is released. The oscillator must be running for this function to work.

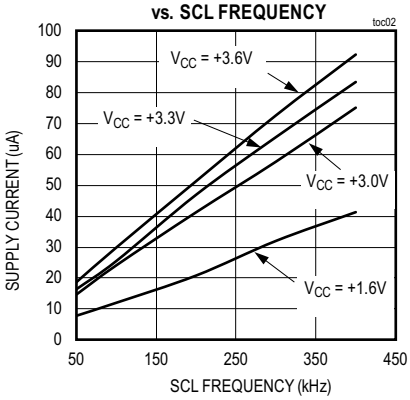
Typical Operating Characteristics

V_{CC} = 3.6V; T_A = +25°C, unless noted otherwise (T_A = +25°C, unless otherwise noted.)

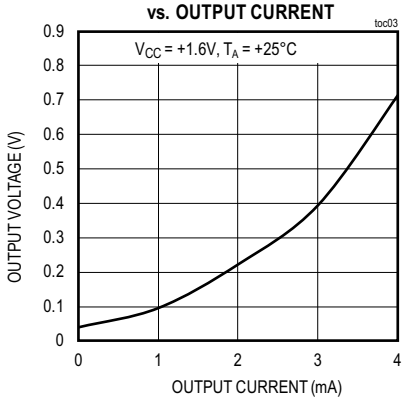
I_{CC} SUPPLY CURRENT vs. SUPPLY VOLTAGE



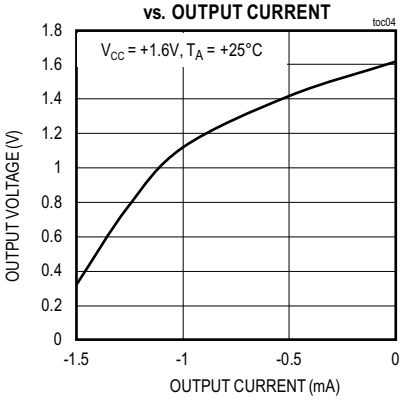
POWER SUPPLY CURRENT vs. SCL FREQUENCY



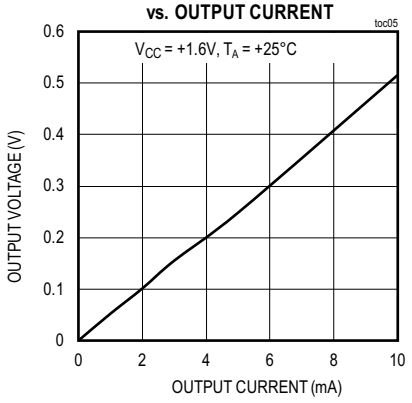
CLKOUT/INTB OUTPUT VOLTAGE LOW vs. OUTPUT CURRENT



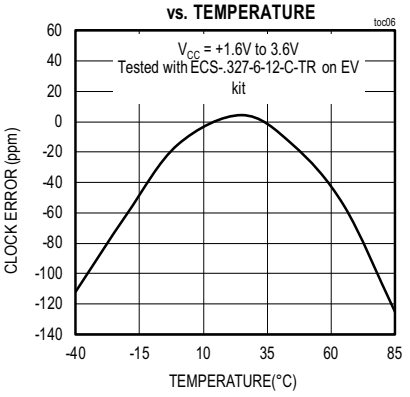
CLKOUT/INTB OUTPUT VOLTAGE HIGH vs. OUTPUT CURRENT



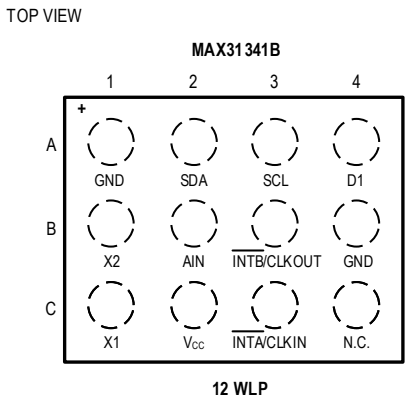
CLKOUT/INTA OUTPUT VOLTAGE LOW vs. OUTPUT CURRENT



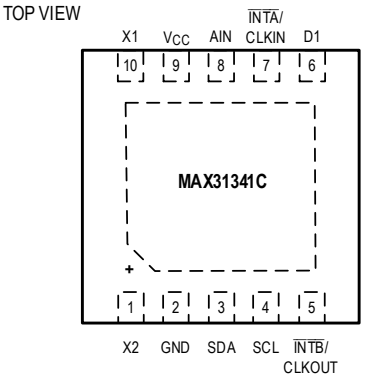
CLOCK ERROR vs. TEMPERATURE



Pin Configuration



12 WLP

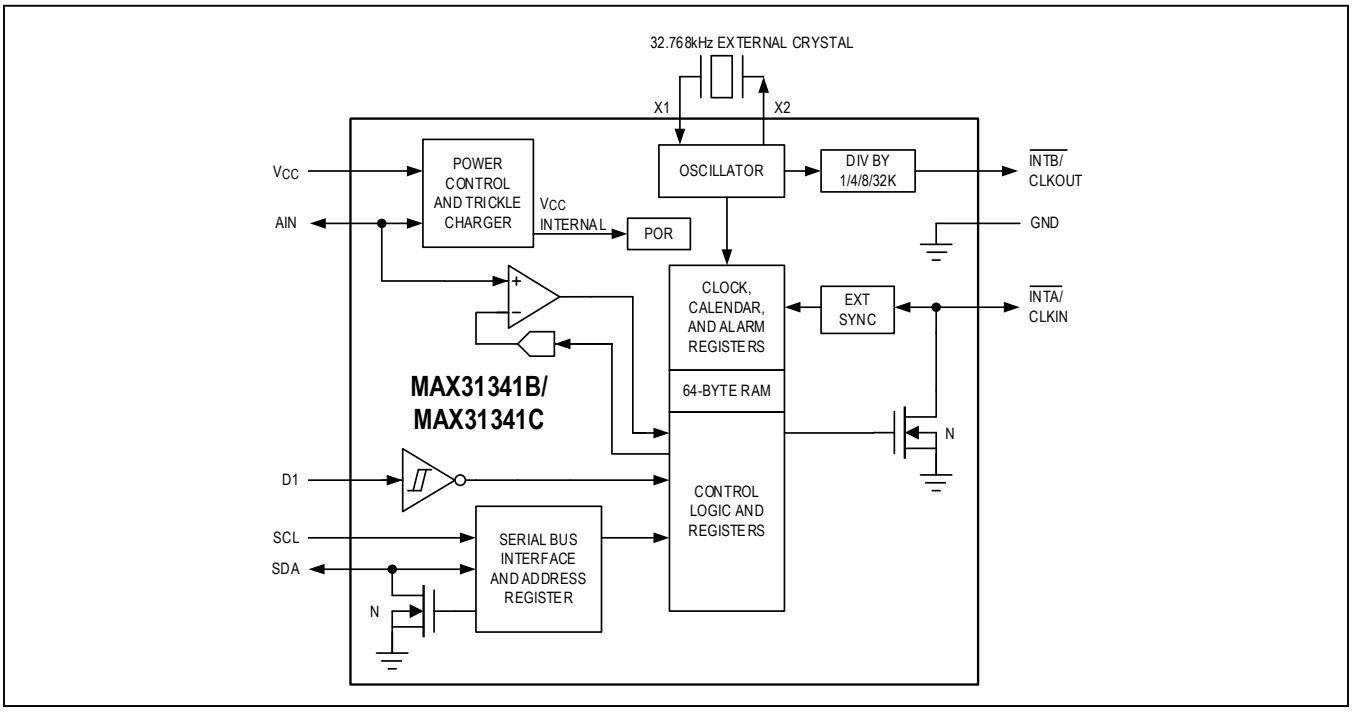


TDFN
3mm x 3mm x 0.75mm

Pin Description

PIN		NAME	FUNCTION
MAX31341B	MAX31341C		
A1, B4	2	GND	Ground.
A2	3	SDA	Serial-Data Input/Output. SDA is the input/output pin for the I²C serial interface. The SDA pin is open-drain and requires an external pullup resistor.
A3	4	SCL	Serial-Clock Input. SCL is used to synchronize data movement on the serial interface.
A4	6	D1	Digital Input.
B1	1	X2	Second Crystal Input for an External 32.768kHz Crystal with 6pF Load Capacitance.
B2	8	AIN	Analog Input for Programmable Threshold Comparator; Backup Battery Input; and Trickle Charger Output. Connect to GND when backup battery is not used.
B3	5	$\overline{\text{INTB}}$, CLK-OUT	Square-Wave Clock or Active-Low Interrupt Output. This pin is used to output a programmable square wave or an alarm interrupt signal. This is a CMOS push-pull output and does not require an external pullup resistor. If not used, this pin can be left unconnected. Refer to Table 2.
C1	10	X1	First Crystal Input for an External 32.768kHz Crystal with 6pF Load Capacitance.
C2	9	VCC	Supply Voltage.
C3	7	$\overline{\text{INTA}}$, CLKIN	Clock Input/Active-Low Interrupt Output. This I/O pin is used to output an alarm interrupt or accept an external clock input to drive the RTC counter. In the output mode, this is an open drain and requires an external pullup resistor. If not used, connect this pin to ground. Refer to Table 2.
C4		NC	Not connected.

Functional Diagram



Detailed Description

Introduction

The MAX31341B/MAX31341C low-current, real-time clock (RTC) is a timekeeping device that provides nanoamperes timekeeping current, extending battery life. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for each month, including corrections for leap year through 2199. The clock operates in 24-hour format.

The MAX31341B/MAX31341C is accessed through an I2C serial interface. The device features one digital Schmitt trigger input and one programmable threshold analog input. The device generates an interrupt output on a falling or rising edge of the digital input (D1) or when the analog input (AIN) voltage crosses a programmed threshold in either direction. An integrated power-on reset function ensures deterministic default register status upon power-up. Soft reset is required after a brown out or brief blackout. Other features include two time-of-day alarms, two interrupts, a programmable square-wave output, a countdown timer, 64-byte RAM and a bus timeout mechanism that resets the I2C bus if it remains inactive for a minimum of $t_{TIMEOUT}$.

The MAX31341B/MAX31341C uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. The device supports high-ESR crystals, which broadens the pool of usable crystals for the device. It uses a 6pF crystal, which decreases oscillator current draw. The MAX31341B/MAX31341C also accepts an external clock reference for synchronization. The external clock can be a 32.768kHz, 50Hz, 60Hz, or 1Hz source. When the enable oscillator bit (OSCONZ) is set to 0, the MAX31341B/MAX31341C uses the oscillator for timekeeping. If the enable external clock input bit (ECLK) is set to 1, the time base derived from the oscillator is compared to the 1Hz signal that is derived from the CLKIN signal. The conditioned signal drives the RTC time and date counters. When the external clock is lost or when the frequency differs more than ±0.8% from the crystal frequency, the LOS flag is asserted.

Address and data are transferred serially through an I2C serial interface.

Clock/Calendar

The time and calendar information are obtained by reading the appropriate I2C register(s) when Rd_RTC bit is set. The time and calendar data are set or initialized by writing the appropriate register followed by a SET_RTC bit of Config_reg2 register transition from 0 to 1. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format.

The century bit (bit 7 of the Month register) is toggled when the Years register overflows from 99 to 00. The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation. When reading or writing the time and date registers, secondary buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the secondary buffers are synchronized to the internal registers on any I2C START and when the register pointer rolls over to zero. The time information is read from these secondary registers, while the clock continues to run. This eliminates the need to reread the registers in case the main registers update during a read.

I2C Interface

The I2C interface is guaranteed to operate when V_{CC} is between 1.6V and 3.6V. The I2C interface is accessible whenever V_{CC} is at a valid level. To prevent invalid device operation, the I2C interface should not be accessed when V_{CC} is below +1.6V. The slave address is defined as the 7 most significant bits (MSBs) sent by the master after a START condition. The address is 0xD2 (left justified with LSB set to 0). The eight bit is used to defined a write or read operation.

If a microcontroller connected to the MAX31341B/MAX31341C resets during I2C communications, it is possible that the microcontroller and the MAX31341B/MAX31341C could become unsynchronized. When the microcontroller resets, the MAX31341B/MAX31341C I2C interface can be placed into a known state by holding SCL low for $t_{TIMEOUT}$. Doing so limits the minimum frequency at which the I2C interface can be operated. If data is being written to the device when the interface timeout is exceeded, prior to the acknowledge, the incomplete byte of data is not written.

Burst Mode

Burst read/write allows the controller to read/write multiple consecutive bytes from a device. It is initiated in the same manner as the byte read/write operation, but instead of terminating the read/write cycle after the first data byte is transferred, the controller can read/write to the whole register array. In burst write operation, after the receipt of each byte, the device responds with an acknowledge, and the address is internally incremented by one. When the address pointer reaches the end of the register address list, it goes back to the first register address. In burst read mode, the controller responds with an acknowledge, indicating it is waiting for additional data. The device continues to output data for each acknowledge received. The controller terminates the read operation by not responding with an acknowledge and issuing a STOP condition.

Data Transfer on I2C Serial Bus

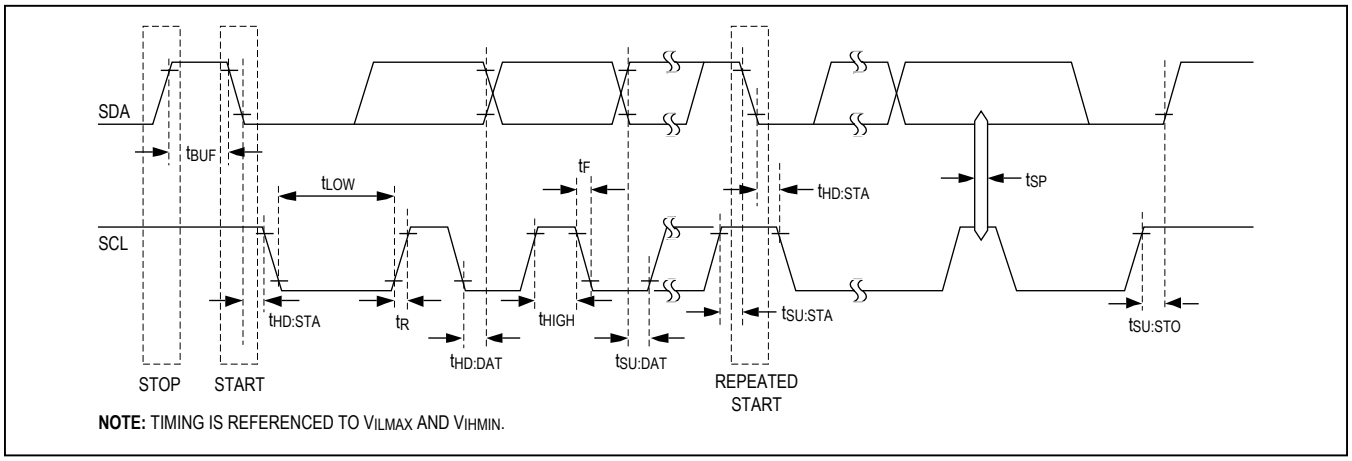


Figure 1. I2C Timing Diagram

RTC Startup Process

Use the following procedure to enable RTC and set time.

1) Exit software reset and enable oscillator (SWRSTN = 1 and OSCONZ = 0) on register Config_reg1(00h)
2) Write RTC time for registers 0x06-0x0C
3) Write Set_RTC=1 on register Config_reg2(01h)
4) Wait 10ms.
5) Write Set_RTC=0 on register Config_reg2(01h)

Oscillator Circuit

The MAX31341B/MAX31341C uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. The MAX31341B/MAX31341C includes integrated capacitive loading for a 6pF C_L crystal. See the *Electrical Characteristics* table for the external crystal parameters. After the oscillator is enabled, the startup time of the oscillator circuit is usually less than 1 second when using a crystal with the specified characteristics; however, an additional 4 seconds are needed for the chip to reach stable, low-current operation.

Clock Accuracy

When running from the internal oscillator, the accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error is added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 2 shows a typical PCB layout for isolation of the crystal and oscillator from noise. Refer to **Application Note 58: Crystal Considerations with Maxim Real-Time Clocks (RTCs)** for detailed information.

Minimizing the Clock Synchronization Delay

When external clock input is disabled (ECLK = 0), the countdown chain is driven by internal high-speed clock. The output of the countdown chain is the 1Hz clock that drives the RTC logic. By default, Clk_sync_reg (58h) = 0x02 and the countdown chain is reset whenever the Set_RTC transitions from 0 to 1. That means after Set_RTC becomes 1, RTC registers (06h – 0Ch) will transfer to internal RTC counter and the next RTC update will happen 1 second later with less than 10ms synchronization delay. If external clock (50Hz/60Hz/32kHz) is used, set Clk_sync_reg = 0x01 to minimize the synchronization delay to less than 100ms. If external 1Hz clock is used, set Clk_sync_reg = 0x00, the maximum synchronization delay will be 1 second.

Layout Example

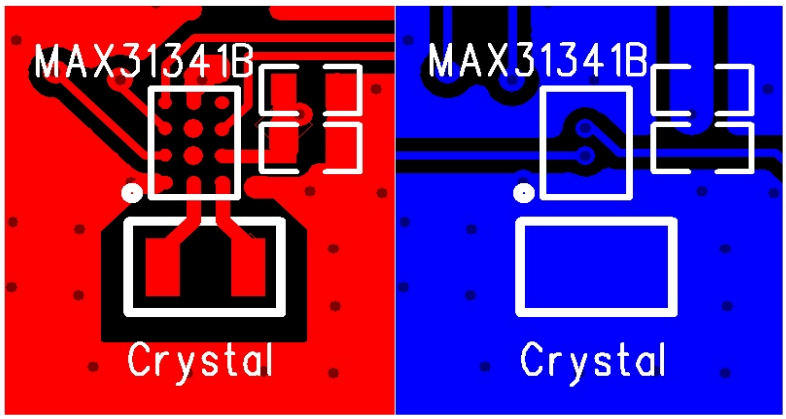


Figure 2. PCB Layout Example

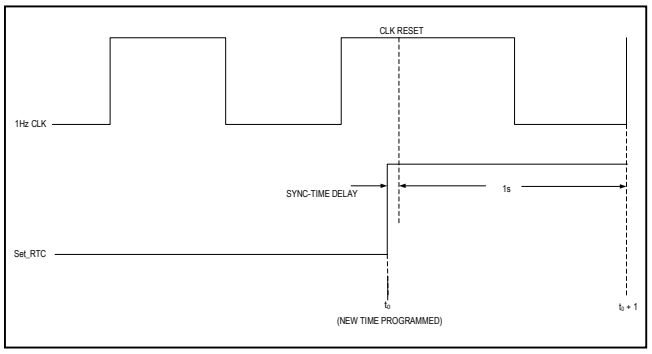


Figure 3. Clock Synchronization Delay

Comparator Mode

When Comparator Mode is selected, the comparator compares AIN voltage with the threshold that was configured in BREF bit field of Config_reg2 register. When AIN goes above or below (depending on AIP interrupt polarity bit) the threshold ANA_IF flag will be set, and interrupt will be asserted if ANA_IE bit in Int_en_reg register is 1. Refer to *Interrupt Modes* to configure the interrupt output pin.

Power Management

The MAX31341B/MAX31341C has a power management mode that monitors the supply voltage on V_{CC} and backup battery voltage connected to AIN and determines which source is used as the internal power supply. In power management mode, pin AIN should be connected to the backup battery. To enter Power Management/ Trickle Charger mode, set D_MODE in Pwr_mgmt_reg (56h) to 0x01. Refer to Table 1 for configuration details.

There is an ANA_IF interrupt flag status bit in the Int_ status_reg (05h) register that can be used as a power-fail flag. In power management mode, the ANA_IF interrupt flag is set when V_{CC} falls below the analog threshold voltage set through BREF in the Config_reg2 (01h) register (or when analog threshold voltage is adjusted to cross above V_{CC}). When operating in comparator mode, ANA_IF is set when it crosses the analog threshold voltage. The analog threshold voltage can be configured to detect a falling or rising edge trigger through the AIP bit in the Int_polarity_config (02h) register.

Trickle Charger

The trickler charger is for charging an external super capacitor or a rechargeable battery. The maximum charging current can be calculated as follows:

$$I_{MAX} = (V_{CC} – V_D – V_{BAT})/R$$

Where V_D is the diode voltage drop, V_{BAT} is the voltage of the battery being charged, and R is the resistance selected in the charging path.

As the battery charges, the battery voltage increases and the voltage across the charging path decreases. Therefore, the charging current also decreases.

Interrupts Status and Output

When an interrupt is asserted, a corresponding status bit in Int_status_reg (05h) becomes “1”, and an interrupt output transitions from High to Low. The time registers 0x06-0x0C will update 2ms after the interrupt is asserted. The interrupt status bit and output can be cleared by

Table 1. Power Management

D_MODE[1:0]	D_MAN_SEL	D_VBACK_SEL	MODE OF OPERATION	
00	x	x	**Comparator Mode**	
01	0	x	**Power Management Auto and Trickle Charger**	
			Supply Condition	**Active Supply**
			$V_{CC} < V_{TH}$, $V_{CC} < AIN$	AIN
			$V_{CC} < V_{TH}$, $V_{CC} > AIN$	V_{CC}
			$V_{CC} > V_{TH}$, $V_{CC} < AIN$	V_{CC}
			$V_{CC} > V_{TH}$, $V_{CC} > AIN$	V_{CC}
01	1	0	Power Management Manual and Trickle Charger Active Supply = V_{CC}	
01	1	1	Power Management Manual and Trickle Charger Active Supply = AIN, for AIN > V_{CC}	
10	x	x	Reserved (Do Not Use)	
11	x	x	Reserved (Do Not Use)	

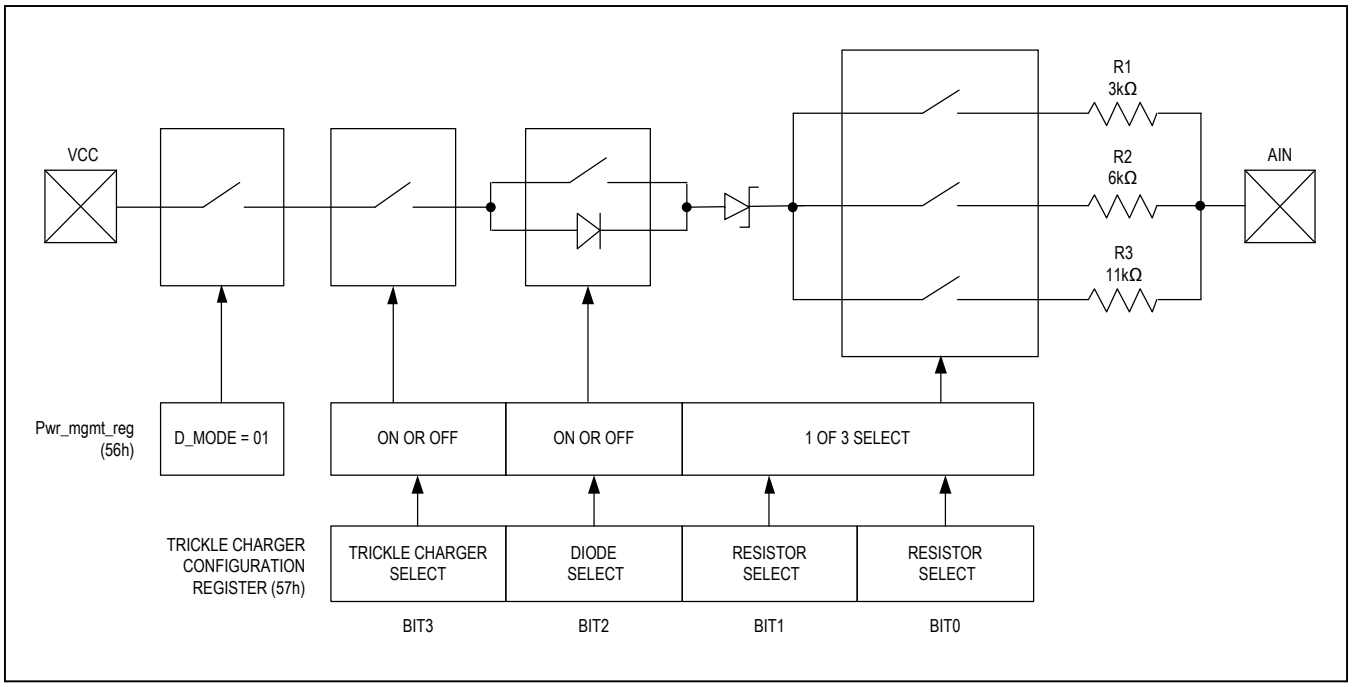


Figure 4. Trickle Charger Block Diagram

reading the Int_status_reg. Refer to Table 2 for interrupt configurations.

Data Retention Mode

The MAX31341B/MAX31341C features a Data Retention mode wherein the device shuts down its internal functional blocks (including the oscillator) except the I2C interface. The device consumes 5nA (typical) in this mode. It retains all the register and RAM contents, including the last valid date and time values. The device can resume counting from here when this mode is exited, and the oscillator is enabled again. User data can be preserved in the RAM in this mode as long as the backup supply is active.

Procedure to enter Data Retention mode:

1) Write DATA_RETEN = 1 in Config_reg2 (01h).
2) Write OSCONZ = 1 in Config_reg1 (00h).

Procedure to exit Data Retention mode:

1) Write DATA_RETEN = 0 in Config_reg2 (01h).
2) Write OSCONZ = 0 in Config_reg1 (00h).

Countdown Timer

The MAX31341B/MAX31341C features a countdown timer with a pause function. The timer can be configured by writing into registers Timer_config (03h) and Timer_init (15h). The Timer_init register should be loaded with the initial value from which the timer would start counting down. The Timer_config register allows these configuration options:

- Select the frequency of the timer using the TFS[1:0] field.
- Start/stop the timer using the TE (Timer Enable) bit.
- Enable/disable the timer repeat function using the TRPT bit. This function reloads and restarts the timer with the same init value once it counts down to zero. In repeat mode, the first timer interrupt indicates the timer has started counting.
- Pause/resume the countdown at any time when the timer is enabled using the TPAUSE bit (explained below).

The timer can be programmed to assert the $\overline{INTA}$ or $\overline{INTB}$ output (see Table 2) whenever it counts down to zero. This can be enabled/disabled using the TIE bit in register Int_en_reg (04h).

The TPAUSE bit is only valid when TE = 1. This bit must be reset to 0 whenever TE is reset to 0.

Table 3 highlights the steps to be used for various use cases involving TE and TPAUSE.

Table 2. Interrupt Modes

INTCN	ECLK	CLKIN/$\overline{INTA}$	CLKOUT/$\overline{INTB}$
0	0	$\overline{INTA}$: Alarm1, Alarm2, Timer, Analog interrupt (AIN), Digital interrupt (D1)	CLKOUT
0	1	CLKIN	CLKOUT
1	0	$\overline{INTA}$: Alarm1, Timer, Analog interrupt (AIN), Digital interrupt (D1)	$\overline{INTB}$: Alarm2
1	1	CLKIN	$\overline{INTB}$: Alarm1, Alarm2, Timer, Analog interrupt (AIN), Digital interrupt (D1)

Table 3. Countdown Timer Sequence

SEQUENCE	TE	TPAUSE	ACTION
Step1	0	0	Countdown timer is reset, and ready for next countdown operation. Timer_init can be programmed in this state.
Step2	1	0	Countdown timer starts counting down from the value programmed in Timer_init
Step3a (Optional)	1	1	Countdown timer is paused and is ready to start counting down when TPAUSE is programmed back to '0'. Contents of the countdown timer are preserved in this state.
Step3b If 3a is true	1	0	Countdown timer is brought out of pause state and starts counting down from the paused value.
	0	1	Not allowed

Typical use cases:

- Countdown timer without pause: Step 1 → Step 2 → Step 1, and so on.
- Countdown timer with pause: Step 1 → Step 2 → Step 3a → Step 3b → Step 1, and so on.

Register Map

ADDRESS	NAME	MSB							LSB
REGBLK									
0x00	Config_reg1[7:0]	ECLK	INTCN	CLKSEL[1:0]		OSCONZ	RS[1:0]		SWRSTN
0x01	Config_reg2[7:0]	–	DATA_RE-TEN	BREF[1:0]		I2C_TIME-OUT_EN	Rd_RTC	Set_RTC	–
0x02	Int_polarity_config[7:0]	–	AIP	EIP1	–	–	–	–	–
0x03	Timer_config[7:0]	–	–	TPAUSE	TE	–	TRPT	TFS[1:0]	
0x04	Int_en_reg[7:0]	–	DOSF	ANA_IE	EIE1	–	TIE	A2IE	A1IE
0x05	Int_status_reg[7:0]	LOS	OSF	ANA_IF	EIF1	–	TIF	A2F	A1F
0x06	Seconds[7:0]	–	sec_10[2:0]			seconds[3:0]			
0x07	Minutes[7:0]	–	min_10[2:0]			minutes[3:0]			
0x08	Hours[7:0]	–	Reserved	hr_10[1:0]		hour[3:0]			
0x09	Day[7:0]	–	–	–	–	–	day[2:0]		
0x0A	Date[7:0]	–	–	date_10[1:0]		date[3:0]			
0x0B	Month[7:0]	century	–	–	month_10	month[3:0]			
0x0C	Year[7:0]	year_10[3:0]				year[3:0]			
0x0D	Alm1_sec[7:0]	A1M1	sec_10[2:0]			seconds[3:0]			
0x0E	Alm1_min[7:0]	A1M2	min_10[2:0]			minutes[3:0]			

Register Map (continued)

ADDRESS	NAME	MSB						LSB
0x0F	Alm1_hrs[7:0]	A1M3	Reserved	hr_10[1:0]		hour[3:0]		
0x10	Alm1day_date[7:0]	A1M4	DY_DT	date_10[1:0]		day_date[3:0]		
0x11	Alm2_min[7:0]	A2M2	min_10[2:0]			minutes[3:0]		
0x12	Alm2_hrs[7:0]	A2M3	Reserved	hr_10[1:0]		hour[3:0]		
0x13	Alm2day_date[7:0]	A2M4	DY_DT	date_10[1:0]		day_date[3:0]		
0x14	Timer_Count[7:0]	Count[7:0]						
0x15	Timer_Init[7:0]	Count[7:0]						
0x16	Ram_Reg 0[7:0]	Data[7:0]						
0x17	Ram_Reg 1[7:0]	Data[7:0]						
0x18	Ram_Reg 2[7:0]	Data[7:0]						
0x19	Ram_Reg 3[7:0]	Data[7:0]						
0x1A	Ram_Reg 4[7:0]	Data[7:0]						
0x1B	Ram_Reg 5[7:0]	Data[7:0]						
0x1C	Ram_Reg 6[7:0]	Data[7:0]						
0x1D	Ram_Reg 7[7:0]	Data[7:0]						
0x1E	Ram_Reg 8[7:0]	Data[7:0]						
0x1F	Ram_Reg 9[7:0]	Data[7:0]						
0x20	Ram_Reg 10[7:0]	Data[7:0]						
0x21	Ram_Reg 11[7:0]	Data[7:0]						
0x22	Ram_Reg 12[7:0]	Data[7:0]						
0x23	Ram_Reg 13[7:0]	Data[7:0]						
0x24	Ram_Reg 14[7:0]	Data[7:0]						
0x25	Ram_Reg 15[7:0]	Data[7:0]						
0x26	Ram_Reg 16[7:0]	Data[7:0]						
0x27	Ram_Reg 17[7:0]	Data[7:0]						
0x28	Ram_Reg 18[7:0]	Data[7:0]						
0x29	Ram_Reg 19[7:0]	Data[7:0]						
0x2A	Ram_Reg 20[7:0]	Data[7:0]						
0x2B	Ram_Reg 21[7:0]	Data[7:0]						
0x2C	Ram_Reg 22[7:0]	Data[7:0]						
0x2D	Ram_Reg 23[7:0]	Data[7:0]						
0x2E	Ram_Reg 24[7:0]	Data[7:0]						
0x2F	Ram_Reg 25[7:0]	Data[7:0]						
0x30	Ram_Reg 26[7:0]	Data[7:0]						
0x31	Ram_Reg 27[7:0]	Data[7:0]						
0x32	Ram_Reg 28[7:0]	Data[7:0]						
0x33	Ram_Reg 29[7:0]	Data[7:0]						
0x34	Ram_Reg 30[7:0]	Data[7:0]						

Register Map (continued)

ADDRESS	NAME	MSB							LSB
0x35	Ram_Reg 31[7:0]	Data[7:0]							
0x36	Ram_Reg 32[7:0]	Data[7:0]							
0x37	Ram_Reg 33[7:0]	Data[7:0]							
0x38	Ram_Reg 34[7:0]	Data[7:0]							
0x39	Ram_Reg 35[7:0]	Data[7:0]							
0x3A	Ram_Reg 36[7:0]	Data[7:0]							
0x3B	Ram_Reg 37[7:0]	Data[7:0]							
0x3C	Ram_Reg 38[7:0]	Data[7:0]							
0x3D	Ram_Reg 39[7:0]	Data[7:0]							
0x3E	Ram_Reg 40[7:0]	Data[7:0]							
0x3F	Ram_Reg 41[7:0]	Data[7:0]							
0x40	Ram_Reg 42[7:0]	Data[7:0]							
0x41	Ram_Reg 43[7:0]	Data[7:0]							
0x42	Ram_Reg 44[7:0]	Data[7:0]							
0x43	Ram_Reg 45[7:0]	Data[7:0]							
0x44	Ram_Reg 46[7:0]	Data[7:0]							
0x45	Ram_Reg 47[7:0]	Data[7:0]							
0x46	Ram_Reg 48[7:0]	Data[7:0]							
0x47	Ram_Reg 49[7:0]	Data[7:0]							
0x48	Ram_Reg 50[7:0]	Data[7:0]							
0x49	Ram_Reg 51[7:0]	Data[7:0]							
0x4A	Ram_Reg 52[7:0]	Data[7:0]							
0x4B	Ram_Reg 53[7:0]	Data[7:0]							
0x4C	Ram_Reg 54[7:0]	Data[7:0]							
0x4D	Ram_Reg 55[7:0]	Data[7:0]							
0x4E	Ram_Reg 56[7:0]	Data[7:0]							
0x4F	Ram_Reg 57[7:0]	Data[7:0]							
0x50	Ram_Reg 59[7:0]	Data[7:0]							
0x51	Ram_Reg 58[7:0]	Data[7:0]							
0x52	Ram_Reg 60[7:0]	Data[7:0]							
0x53	Ram_Reg 61[7:0]	Data[7:0]							
0x54	Ram_Reg 62[7:0]	Data[7:0]							
0x55	Ram_Reg 63[7:0]	Data[7:0]							
0x56	Pwr_mgmt_reg[7:0]	–	–	–	–	D_ VBACK_ SEL	D_MAN_ SEL	D_MODE[1:0]	
0x57	Trickle_reg[7:0]	–	–	–	–	D_TRICKLE[3:0]			
0x58	Clock_sync_reg[7:0]	–	–	–	–	–	–	SYNC_DELAY[1:0]	
0x59	RevID_reg[7:0]	REVID[3:0]				–	–	–	–

Register Details

Config_reg1 (0x00)

Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	ECLK	INTCN	CLKSEL[1:0]		OSCONZ	RS[1:0]		SWRSTN
Reset	0x0	0x0	0x0		0x1	0x3		0x0
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ECLK	7	Enable external clock input	0x0: Disable the external clock 0x1: Enable the external clock
INTCN	6	Interupt control bit. Selects $\overline{\text{INTB}}$/CLKOUT pin output function	0x0: Output is square wave 0x1: Output is interrupt
CLKSEL	5:4	Selects the CLKIN frequency	0x0: 1Hz 0x1: 50Hz 0x2: 60Hz 0x3: 32.768kHz
OSCONZ	3	Oscillator is on when set to 0. Oscillator is off when set to 1.	0x0: Enable the oscillator 0x1: Disable the oscillator
RS	2:1	Square-wave output frequency selection on CLKOUT pin	0x0: 1Hz 0x1: 4.098kHz 0x2: 8.192kHz 0x3: 32.768kHz
SWRSTN	0	Software reset	0x0: Resets the digital block 0x1: Device is not on reset mode

Config_reg2 (0x1)

Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	DATA_RE-TEN	BREF[1:0]		I2C_TIME-OUT_EN	Rd_RTC	Set_RTC	–
Reset	–	0x0	0x0		0x1	0x1	0x0	–
Access Type	–	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
DATA_RE-TEN	6	Sets the device into data retention mode.	0x0: Normal operation mode 0x1: Data retention mode
BREF	5:4	BREF sets the analog comparator threshold voltage.	0x0: 1.3V 0x1: 1.7V 0x2: 2.0V 0x3: 2.2V
I2C_TIME-OUT_EN	3	I2C timeout Enable	0x0: Disables the I2C timeout 0x1: Enables the I2C timeout
Rd_RTC	2	Read RTC	0x0: Reads previous programmed RTC value in registers 06h-0Ch 0x1: Reads Current RTC value in registers 06h-0Ch
Set_RTC	1	Set RTC	0 to 1 transition loads RTC registers (06h - 0Ch) contents to countdown chain. See *Detailed Description*.

Int_polarity_config (0x2)

Interrupt Polarity Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	AIP	EIP1	–	–	–	–	–
Reset	–	0x0	0x0	–	–	–	–	–
Access Type	–	Write, Read	Write, Read	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
AIP	6	Analog interrupt polarity	0x0: Analog interrupt will trigger on falling edge of AIN input 0x1: Analog interrupt will trigger on rising edge of AIN input
EIP1	5	External interrupt polarity for D1	0x0: External interrupt will trigger on falling edge of D1 input 0x1: External interrupt will trigger on rising edge of D1 input

Timer_config (0x3)

Countdown Timer Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	TPAUSE	TE	–	TRPT	TFS[1:0]	
Reset	–	–	0x0	0x0	–	0X1	0x3	
Access Type	–	–	Write, Read	Write, Read	–	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TPAUSE	5	Timer Pause. This field is valid only when TE = 1. Reset TPAUSE when TE is reset to 0. See *Countdown Timer* section.	0x0: Resume timer countdown from paused state 0x1: Pause timer
TE	4	Timer enable	0x0: Timer is reset. New timer countdown value (Timer_Init) can be programmed in this state. Note: TPAUSE must be reset to 0 prior to setting TE to 1 0x1: Timer enabled countdown starts
TRPT	2	Timer repeat mode	0x0: Countdown timer will halt once it reaches zero 0x1: Countdown timer reloads the value from the Timer_init register upon reaching zero and continues counting.
TFS	1:0	Timer frequency selection	0x0: 1024Hz 0x1: 256Hz 0x2: 64Hz 0x3: 16Hz

Timer_config (0x3)

Countdown Timer Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	TPAUSE	TE	–	TRPT	TFS[1:0]	
Reset	–	–	0x0	0x0	–	0X1	0x3	
Access Type	–	–	Write, Read	Write, Read	–	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TPAUSE	5	Timer Pause. This field is valid only when TE = 1. Reset TPAUSE when TE is reset to 0. See *Countdown Timer* section.	0x0: Resume timer countdown from paused state 0x1: Pause timer
TE	4	Timer enable	0x0: Timer is reset. New timer countdown value (Timer_Init) can be programmed in this state. Note: In this state, reset TPAUSE to 0 0x1: Timer enabled countdown starts
TRPT	2	Timer repeat mode	0x0: Countdown timer will halt once it reaches zero 0x1: Countdown timer reloads the value from the Timer_init register upon reaching zero and continues counting.
TFS	1:0	Timer frequency selection	0x0: 1024Hz 0x1: 256Hz 0x2: 64Hz 0x3: 16Hz

Int_en_reg (0x4)

Interrupt Enable Register

BIT	7	6	5	4	3	2	1	0
Field	–	DOSF	ANA_IE	EIE1	–	TIE	A2IE	A1IE
Reset	–	0x0	0x0	0x0	–	0x0	0x0	0x0
Access Type	–	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DOSF	6	Disable Oscillator flag	0x0: OSF indicates oscillator status 0x1: Disables the oscillator flag (OSF= 0)
ANA_IE	5	Analog Interrupt enable	0x0: Disabled 0x1: Enabled
EIE1	4	External Interrupt enable for D1	0x0: Disabled 0x1: Enabled
TIE	2	Timer interrupt enable	0x0: Disabled 0x1: Enabled
A2IE	1	Alarm 2 interrupt enable	0x0: Disabled 0x1: Enabled
A1IE	0	Alarm1 interrupt enable	0x0: Disabled 0x1: Enabled

Int_status_reg (0x5)

Interrupt Status Register

BIT	7	6	5	4	3	2	1	0
Field	LOS	OSF	ANA_IF	EIF1	–	TIF	A2F	A1F
Reset	0x0	0x1	0x0	0x0	–	0x0	0x0	0X0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	–	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
LOS	7	Loss of signal. Valid only for external clock modes (ECLK = 1)	0x0: Oscillator clock frequency is within 0.8% of external clock frequency 0x1: Oscillator clock frequency differs more than 0.8% from the external clock frequency
OSF	6	Oscillator stop flag	0x0: Oscillator is running or when DOSF = 1 0x1: Oscillator has stopped
ANA_IF	5	Analog interrupt flag/power-fail flag	0x0: There is no external interrupt on AIN 0x1: There is/was an external interrupt on AIN
EIF1	4	External interrupt flag for D1	0x0: There is no external interrupt on D1 0x1: There is/was an external interrupt on D1
TIF	2	Timer interrupt flag	0x0: Countdown timer is not zero 0x1: Countdown timer reached to zero
A2F	1	Alarm2 flag	0x0: Alarm2 not triggered 0x1: Alarm2 triggered
A1F	0	Alarm1 flag	0x0: Alarm1 not triggered 0x1: Alarm1 triggered

Seconds (0x6)

Seconds Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	sec_10[2:0]			seconds[3:0]			
Reset	–	0x0			0x0			
Access Type	–	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION
sec_10	6:4	RTC seconds in multiples of 10
seconds	3:0	RTC seconds value

Minutes (0x7)

Minutes Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	min_10[2:0]			minutes[3:0]			
Reset	–	0x0			0x0			
Access Type	–	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION
min_10	6:4	RTC minutes in multiples of 10
minutes	3:0	RTC minutes value

Hours (0x8)

Hours Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	Reserved	hr_10[1:0]		hour[3:0]			
Reset	–	0x0		0x0	0x0			
Access Type	–	Write, Read		Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	6	User must enter 0	
hr_10	5:4	RTC hours in multiples of 10	
hour	3:0	RTC hours value	

Day (0x9)

Day Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	day[2:0]		
Reset	–	–	–	–	–	0x1		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION
day	2:0	RTC day of the week

Date (0xA)

Date Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	date_10[1:0]		date[3:0]			
Reset	–	–	0x0		0x1			
Access Type	–	–	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION
date_10	5:4	RTC date in multiples of 10
date	3:0	RTC date

Month (0xB)

Month Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	century	–	–	month_10	month[3:0]			
Reset	0x0	–	–	0x0	0x1			
Access Type	Write, Read	–	–	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
century	7	Century bit	0x0: Year is in current century 0x1: Year is in next century
month_10	4	RTC month in multiples of 10	
month	3:0	RTC months	

Year (0xC)

Year Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	year_10[3:0]				year[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
year_10	7:4	RTC year multiples of 10
year	3:0	RTC years

Alm1_sec (0xD)

Alarm 1 can be set by writing to registers 0Dh - 10h. See register map. The alarm can be programmed by the A1IE bit in Int_en_reg (04h) register to activate the $\overline{INTA}$/CLKIN output on an alarm match condition. A1M1, A1M2, A1M3, and A1M4 are mask bits. When all the mask bits of each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers match the corresponding values stored in the time-of-day/date alarm registers. The alarm can also be programmed to repeat every second, minute, hour, day, or date. Table 4 shows the possible settings. Configurations not listed in the table result in illogical operation. The DY_DT bit (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0-5 reflects the day of the week or the date of the month. If DY_DT is written to logic 0, the alarm is the result of a match with date of the month. If DY_DT is written to logic 1, the alarm is the result of a match with day of the week.

Table 4. Alarm 1 Settings

DY_DT	A1M4	A1M3	A1M2	A1M1	ALARM RATE
x	1	1	1	1	Once per sec
x	1	1	1	0	Sec match
x	1	1	0	0	Min and sec match
x	1	0	0	0	Hour, min, and sec match
0	0	0	0	0	Date and Time match
1	0	0	0	0	Day and Time match

BIT	7	6	5	4	3	2	1	0
Field	A1M1	sec_10[2:0]			seconds[3:0]			
Reset	0x0	0x0			0x0			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION
A1M1	7	Alarm1 mask bit for seconds
sec_10	6:4	Alarm1 seconds in multiples of 10
seconds	3:0	Alarm1 seconds

Alm1_min (0xE)

Alarm1 Minutes Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A1M2	min_10[2:0]			minutes[3:0]			
Reset	0x0	0x0			0x0			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION
A1M2	7	Alarm1 mask bit for minutes
min_10	6:4	Alarm1 minutes in multiples of 10
minutes	3:0	Alarm1 minutes

Alm1_hrs (0xF)

Alarm1 Hours Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A1M3	Reserved	hr_10[1:0]		hour[3:0]			
Reset	0x0	0x0		0x0	0x0			
Access Type	Write, Read	Write, Read		Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
A1M3	7	Alarm1 mask bit for hours	
Reserved	6	User must enter 0	
hr_10	5:4	Alarm1 hours in multiples of 10	
hour	3:0	Alarm1 hours	

Alm1day_date (0x10)

Alarm1 Day/Date Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A1M4	DY_DT	date_10[1:0]		day_date[3:0]			
Reset	0x0	0x0	0x0		0x0			
Access Type	Write, Read	Write, Read	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
A1M4	7	Alarm1 mask bit for day/date	
DY_DT	6	Alarm1 day/date match	0x0: Alarm when date match 0x1: Alarm when day match
date_10	5:4	Alarm1 date in multiples of 10	
day_date	3:0	Alarm1 day/date	

Alm2_min (0x11)

Alarm 2 can be set by writing to registers 11h - 13h. See the *Register Map*. The alarm can be programmed by the A2IE bit in Int_en_reg (04h) register to activate the $\overline{INTB}$/CLKIN output on an alarm match condition. Bit 7 of each of the time-of-day/ date alarm registers are mask bits. When all the mask bits of each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers match the corresponding values stored in the time-of-day/date alarm registers. The alarm can also be programmed to repeat every minute, hour, day, or date. Table 5 shows the possible settings. Configurations not listed in the table result in illogical operation. The DY_DT bit (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0-5 reflects the day of the week or the date of the month. If DY_DT is written to logic 0, the alarm is the result of a match with date of the month. If DY_DT is written to logic 1, the alarm is the result of a match with day of the week.

Table 5. Alarm 2 Settings

DY_DT	A2M4	A2M3	A2M1	ALARM RATE
x	1	1	1	Once per minute
x	1	1	0	Minute match
x	1	0	0	Hour and minute match
0	0	0	0	Date, hour, and minute match
1	0	0	0	Day, hour, and minute match

BIT	7	6	5	4	3	2	1	0
Field	A2M2	min_10[2:0]			minutes[3:0]			
Reset	0x0	0x0			0x0			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION
A2M2	7	Alarm2 mask bit for minutes
min_10	6:4	Alarm2 minutes in multiples of 10
minutes	3:0	Alarm2 minutes

Alm2_hrs (0x12)

Alarm2 Hours Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A2M3	Reserved	hr_10[1:0]		hour[3:0]			
Reset	0x0	0x0		0x0	0x0			
Access Type	Write, Read	Write, Read		Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
A2M3	7	Alarm2 mask bit for hours	
Reserved	6	User must enter 0	
hr_10	5:4	Alarm2 hours in multiples of 10	
hour	3:0	Alarm2 hours	

Alm2day_date (0x13)

Alarm2 Day/Date Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A2M4	DY_DT	date_10[1:0]		day_date[3:0]			
Reset	0x0	0x0	0x0		0x0			
Access Type	Write, Read	Write, Read	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
A2M4	7	Alarm2 mask bit for day/date	
DY_DT	6	Alarm2 day/date match	0x0: Alarm when date match 0x1: Alarm when day match
date_10	5:4	Alarm2 date in multiples of 10	
day_date	3:0	Alarm2 day/date	

Timer_Count (0x14)

Countdown Timer Value Register

BIT	7	6	5	4	3	2	1	0
Field	Count[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
Count	7:0	Count down timer current count value

Timer_Init (0x15)

Countdown Timer Initialization Register

BIT	7	6	5	4	3	2	1	0
Field	Count[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
Count	7:0	Count down timer initial value. The timer is loaded with the contents of this register when it reaches to zero in repeat mode

Ram_Reg (0x16, 0x17, 0x18, 0x19, 0x1A, 0x1B, 0x1C, 0x1D, 0x1E, 0x1F, 0x20, 0x21, 0x22, 0x23, 0x24, 0x25, 0x26, 0x27, 0x28, 0x29, 0x2A, 0x2B, 0x2C, 0x2D, 0x2E, 0x2F, 0x30, 0x31, 0x32, 0x33, 0x34, 0x35, 0x36, 0x37, 0x38, 0x39, 0x3A, 0x3B, 0x3C, 0x3D, 0x3E, 0x3F, 0x40, 0x41, 0x42, 0x43, 0x44, 0x45, 0x46, 0x47, 0x48, 0x49, 0x4A, 0x4B, 0x4C, 0x4D, 0x4E, 0x4F, 0x50, 0x51, 0x52, 0x53, 0x54, 0x55)

BIT	7	6	5	4	3	2	1	0
Field	Data[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
Data	7:0	RAM data byte. Power-on Reset value is random

Pwr_mgmt_reg (0x56)

Power Management Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	D_VBACK_SEL	D_MAN_SEL	D_MODE[1:0]	
Reset	–	–	–	–	0x0	0x0	0x0	
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
D_VBACK_SEL	3	When this bit is 0, and D_MAN_SEL is 1, V_{CC} is used as power supply. When this bit is 1, and D_MAN_SEL is 1, V_{BACKUP} is used as power supply.	0x0: Use V_{CC} as supply. 0x1: Use V_{BACKUP} as supply.
D_MAN_SEL	2	Default low. When this bit is low, the RTC determines which supply to use automatically. When this bit is high, user can manually select whether to use V_{CC} or V_{BACKUP} as supply via D_VBACK_SEL.	0x0: Device decides whether to use V_{CC} or V_{BACKUP} as supply. 0x1: User decides whether to use V_{CC} or V_{BACKUP} as supply by setting D_VBACK_SEL bit.
D_MODE	1:0	Sets the mode of the comparator to comparator mode or power management/trickle charger mode.	0x0: Comparator Mode 0x1: Power Management/Trickle Charger Mode 0x2: Reserved 0x3: Reserved

Trickle_reg (0x57)

Trickle Charger Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	D_TRICKLE[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
D_TRICKLE	3:0	Sets the charging path for trickle charger.	0x0: No Connect 0x1: No Connect 0x2: No Connect 0x3: No Connect 0x4: No Connect 0x5: No Connect 0x6: No Connect 0x7: No Connect 0x8: 3kΩ in series with a Schottky diode. 0x9: No Connect 0xA: 6kΩ in series with a Schottky diode. 0xB: 11kΩ in series with a Schottky diode. 0xC: 3kΩ in series with a diode in series with a Schottky diode. 0xD: No Connect 0xE: 6kΩ in series with a diode in series with a Schottky diode. 0xF: 11kΩ in series with a diode in series with a Schottky diode.

Clock_sync_reg (0x58)

Clock Synchronization Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	SYNC_DELAY[1:0]	
Reset	–	–	–	–	–	–	0b10	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SYNC_DELAY	1:0	Synchronization delay is the time it takes for the internal countdown chain to reset after the rising edge of Set_RTC. See the *Minimizing the Clock Synchronization Delay* section for further details. To minimize the delay, select the appropriate setting based on the clock configuration.	0x0: Synchronization delay setting for external 1Hz clock (ECLK = 1, CLKSEL = 0) mode. Delay is less than 1s. 0x1: Synchronization delay setting for external 50Hz/60Hz/32kHz clock (ECLK = 1, CLKSEL = 1/2/3) mode. Delay is less than 100ms. 0x2: Synchronization delay setting for internal oscillator mode (OSCONZ = 0, ECLK = 0). Delay is less than 10ms. 0x3: Reserved

RevID_reg (0x59)

Revision Identification Register

BIT	7	6	5	4	3	2	1	0
Field	REVID[3:0]				–	–	–	–
Reset	0x1				–	–	–	–
Access Type	Read Only				–	–	–	–

BITFIELD	BITS	DESCRIPTION
REVID	7:4	Revision ID

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX31341BEWC+T	-40°C to +85°C	12 WLP
MAX31341CETB+T	-40°C to +85°C	10 TDFN

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/19	Initial release	—
1	5/19	Updated *Layout Example*, Table 1, and *Countdown Timer* section	10–12
2	8/19	Updated *I²C Interface* section	9
3	1/20	Added MAX31341C part number to data sheet	1–30
4	3/20	Updated *Ordering Information*	29

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