



**THE DATASHEET OF  
A759KS106M2CAAE110**



# OPAx131 General-Purpose, FET-Input Operational Amplifiers

## 1 Features

- FET input:  $I_B = 50\text{pA}$  max
- Low offset voltage:  $750\mu\text{V}$  max
- Wide supply range:  $\pm 4.5\text{V}$  to  $\pm 18\text{V}$
- Slew rate:  $10\text{V}/\mu\text{s}$
- Wide bandwidth:  $4\text{MHz}$
- Excellent capacitive load drive
- Single, dual, quad versions

## 2 Applications

- [Data acquisition \(DAQ\)](#)
- [Flow transmitter](#)
- [Lab and field instrumentation](#)
- [Electrocardiogram \(ECG\)](#)

## 3 Description

The OPAx131 series of FET-input op amps provides high performance at low cost. The OPA131 single, OPA2131 dual, and OPA4131 quad versions in industry-standard pinouts allow cost-effective design options.

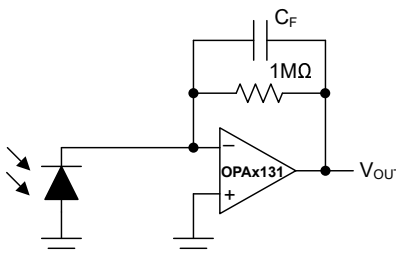
The OPAx131 series offers excellent general-purpose performance, including low offset voltage, drift, and good dynamic characteristics.

Single and dual versions are available in an 8-pin, SOIC, surface-mount package. The quad version is available in 14-pin and 16-pin, SOIC, surface-mount packages, and a 14-pin PDIP package.

### Device Information

| PART NUMBER | CHANNEL COUNT | PACKAGE <sup>(1)</sup> |
|-------------|---------------|------------------------|
| OPA131      | Single        | D (SOIC, 8)            |
| OPA2131     | Dual          | D (SOIC, 8)            |
| OPA4131     | Quad          | D (SOIC, 14)           |
|             |               | DW (SOIC, 16)          |
|             |               | N (PDIP, 14)           |

(1) For more information, see [Section 9](#).



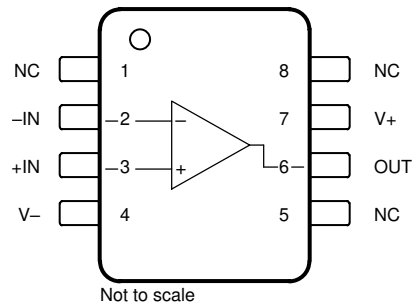
**Simplified Transimpedance Amplifier**



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## 4 Pin Configuration and Functions

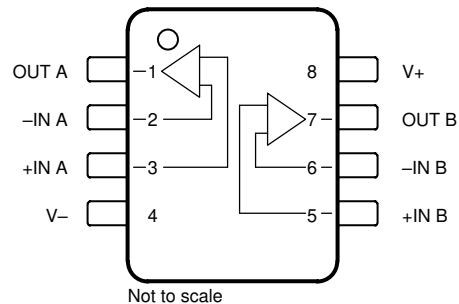


**Figure 4-1. OPA131 D Package, 8-Pin SOIC (Top View)**

**Table 4-1. Pin Functions: OPA131**

| PIN  |      | TYPE   | DESCRIPTION                              |
|------|------|--------|--|
| NAME | NO.  |        |  |
| +IN  | 3    | Input  | Noninverting input, channel A            |
| -IN  | 2    | Input  | Inverting input, channel A               |
| NC   | 1, 5 | —      | Do not connect these pins <sup>(1)</sup> |
| NC   | 8    | —      | No internal connection. Float this pin.  |
| OUT  | 6    | Output | Output                                   |
| V+   | 7    | Power  | Positive (highest) power supply          |
| V-   | 4    | Power  | Negative (lowest) power supply           |

(1) Existing layouts for the OPA131 D package before revision B of this data sheet do not need to be redesigned.



**Figure 4-2. OPA2131 D Package, 8-Pin SOIC (Top View)**

**Table 4-2. Pin Functions: OPA2131**

| PIN   |     | TYPE   | DESCRIPTION                     |
|-------|-----|--------|---------------------------------|
| NAME  | NO. |        |                                 |
| +IN A | 3   | Input  | Noninverting input, channel A   |
| +IN B | 5   | Input  | Noninverting input, channel B   |
| -IN A | 2   | Input  | Inverting input, channel A      |
| -IN B | 6   | Input  | Inverting input, channel B      |
| OUT A | 1   | Output | Output, channel A               |
| OUT B | 7   | Output | Output, channel B               |
| V+    | 8   | Power  | Positive (highest) power supply |
| V-    | 4   | Power  | Negative (lowest) power supply  |

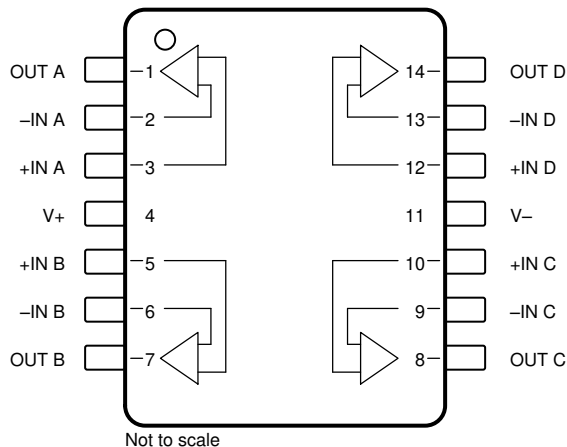
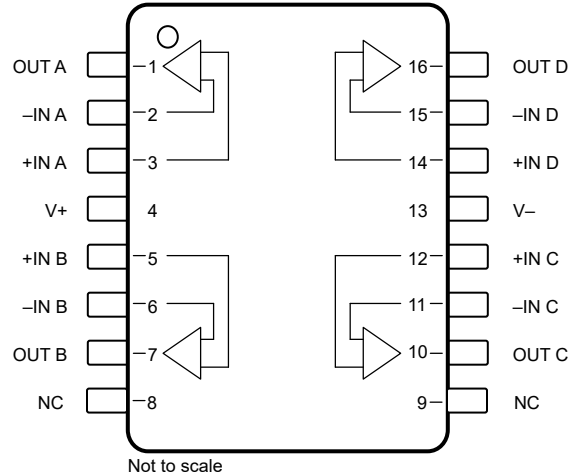


Figure 4-3. OPA4131 D Package, 14-Pin SOIC, and N Package, 14-Pin PDIP (Top View)

Table 4-3. Pin Functions: OPA4131 D and N packages

| PIN   |     | TYPE   | DESCRIPTION                     |
|-------|-----|--------|---------------------------------|
| NAME  | NO. |        |                                 |
| +IN A | 3   | Input  | Noninverting input, channel A   |
| +IN B | 5   | Input  | Noninverting input, channel B   |
| +IN C | 10  | Input  | Noninverting input, channel C   |
| +IN D | 12  | Input  | Noninverting input, channel D   |
| -IN A | 2   | Input  | Inverting input, channel A      |
| -IN B | 6   | Input  | Inverting input, channel B      |
| -IN C | 9   | Input  | Inverting input, channel C      |
| -IN D | 13  | Input  | Inverting input, channel D      |
| OUT A | 1   | Output | Output, channel A               |
| OUT B | 7   | Output | Output, channel B               |
| OUT C | 8   | Output | Output, channel C               |
| OUT D | 14  | Output | Output, channel D               |
| V+    | 4   | Power  | Positive (highest) power supply |
| V-    | 11  | Power  | Negative (lowest) power supply  |



**Figure 4-4. OPA4131 DW Package, 16-Pin SOIC (Top View)**

**Table 4-4. Pin Functions: OPA4131 DW Package**

| PIN   |      | TYPE   | DESCRIPTION                             |
|-------|------|--------|---|
| NAME  | NO.  |        |   |
| +IN A | 3    | Input  | Noninverting input, channel A           |
| +IN B | 5    | Input  | Noninverting input, channel B           |
| +IN C | 12   | Input  | Noninverting input, channel C           |
| +IN D | 14   | Input  | Noninverting input, channel D           |
| -IN A | 2    | Input  | Inverting input, channel A              |
| -IN B | 6    | Input  | Inverting input, channel B              |
| -IN C | 11   | Input  | Inverting input, channel C              |
| -IN D | 15   | Input  | Inverting input, channel D              |
| OUT A | 1    | Output | Output, channel A                       |
| OUT B | 7    | Output | Output, channel B                       |
| OUT C | 10   | Output | Output, channel C                       |
| OUT D | 16   | Output | Output, channel D                       |
| V+    | 4    | Power  | Positive (highest) power supply         |
| V-    | 13   | Power  | Negative (lowest) power supply          |
| NC    | 8, 9 | —      | No internal connection. Float this pin. |

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                     | MIN           | MAX        | UNIT |
|------------------|-------------------------------------|---------------|------------|------|
| V <sub>S</sub>   | Supply voltage, (V+) – (V–)         | Dual supply   | ±18        | V    |
|                  |                                     | Single supply | 36         |      |
|                  | Input voltage <sup>(2)</sup>        | (V–) – 0.5    | (V+) + 0.5 | V    |
|                  | Input current <sup>(2)</sup>        | ±10           |            | mA   |
| I <sub>SC</sub>  | Output short-circuit <sup>(3)</sup> | Continuous    |            |      |
| T <sub>A</sub>   | Operating temperature               | –55           | 125        | °C   |
| T <sub>J</sub>   | Junction temperature                |               |            | 150  |
| T <sub>stg</sub> | Storage temperature                 | –55           | 125        | °C   |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.
- (3) Short-circuit to ground, one amplifier per package.

### 5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                |                             | MIN           | NOM  | MAX | UNIT |   |
|----------------|-----------------------------|---------------|------|-----|------|---|
| V <sub>S</sub> | Supply voltage, (V+) – (V–) | Dual supply   | ±4.5 | ±15 | ±18  | V |
|                |                             | Single supply | 9    | 30  | 36   |   |
| T <sub>A</sub> | Ambient temperature         | –40           |      | +85 | °C   |   |

### 5.3 Thermal Information - OPA131

| THERMAL METRIC <sup>(1)</sup> |  | OPA131   |  | UNIT |
|-------------------------------|--|----------|--|------|
|                               |  | D (SOIC) |  |      |
|                               |  | 8 PINS   |  |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 150      |  | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 74       |  | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 62       |  | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 19.7     |  | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 54.8     |  | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | N/A      |  | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 5.4 Thermal Information - OPA2131

| THERMAL METRIC <sup>(1)</sup> |  | OPA2131  |  | UNIT |
|-------------------------------|--|----------|--|------|
|                               |  | D (SOIC) |  |      |
|                               |  | 8 PINS   |  |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 150      |  | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 52.3     |  | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 63.5     |  | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 10.7     |  | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 62.4     |  | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | N/A      |  | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 5.5 Thermal Information - OPA4131

| THERMAL METRIC <sup>(1)</sup> |  | OPA4131  |           |          | UNIT |
|-------------------------------|--|----------|-----------|----------|------|
|                               |  | D (SOIC) | DW (SOIC) | N (PDIP) |      |
|                               |  | 14 PINS  | 16 PINS   | 14 PINS  |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 110      | 110       | 80       | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 56       | N/A       | N/A      | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 53       | N/A       | N/A      | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 19       | N/A       | N/A      | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 46       | N/A       | N/A      | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | N/A      | N/A       | N/A      | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 5.6 Electrical Characteristics

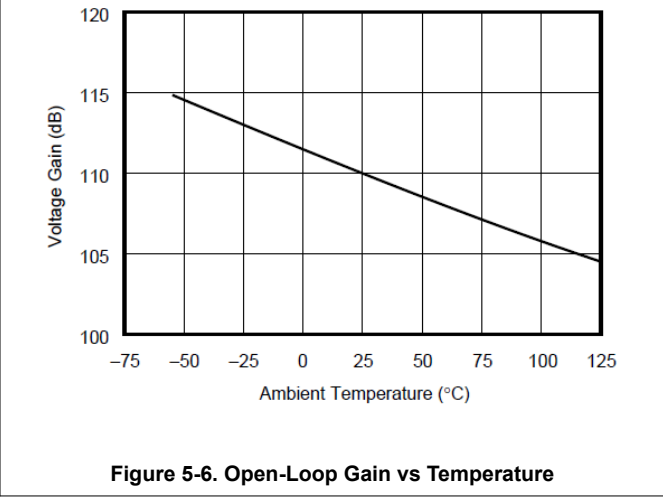
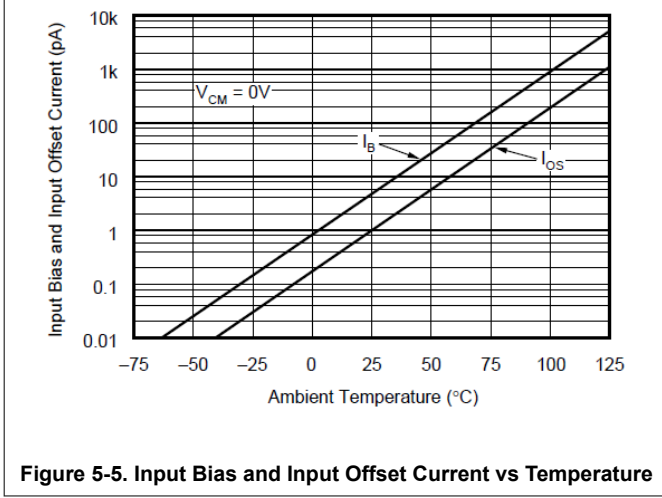
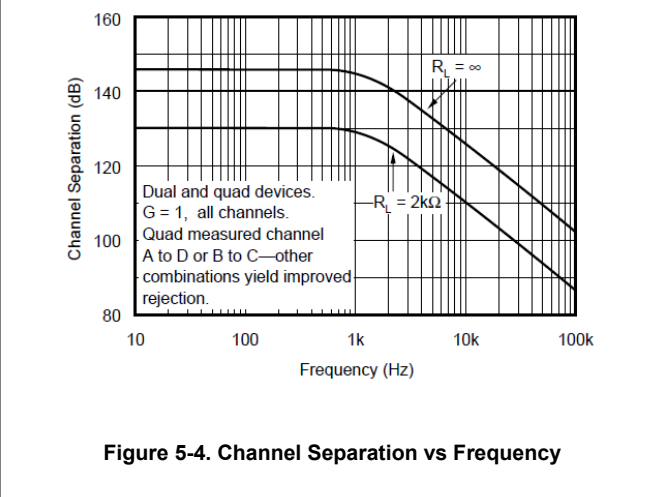
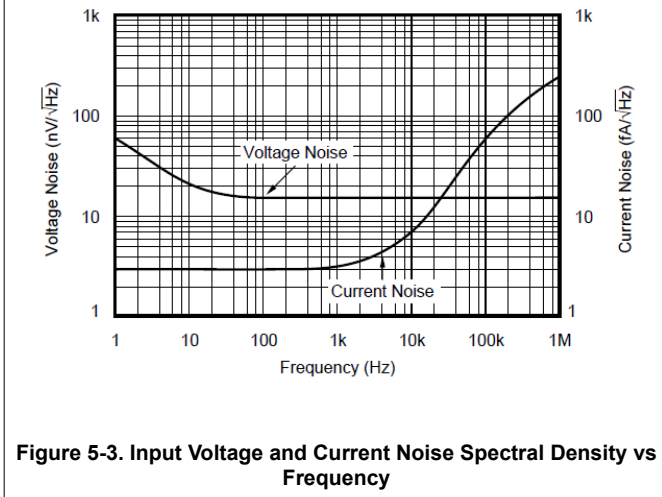
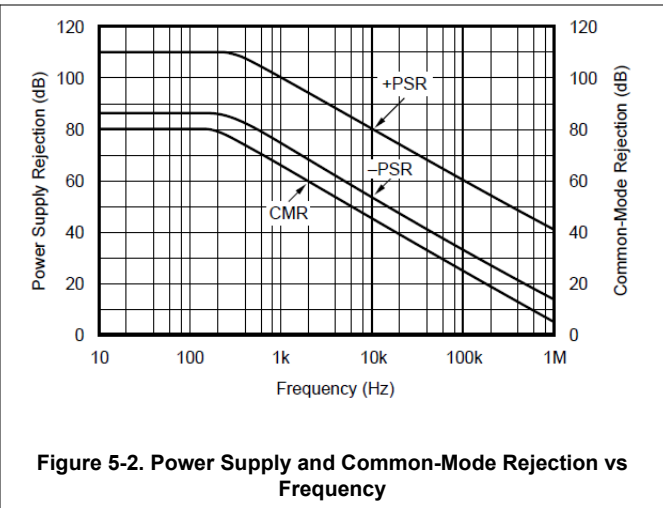
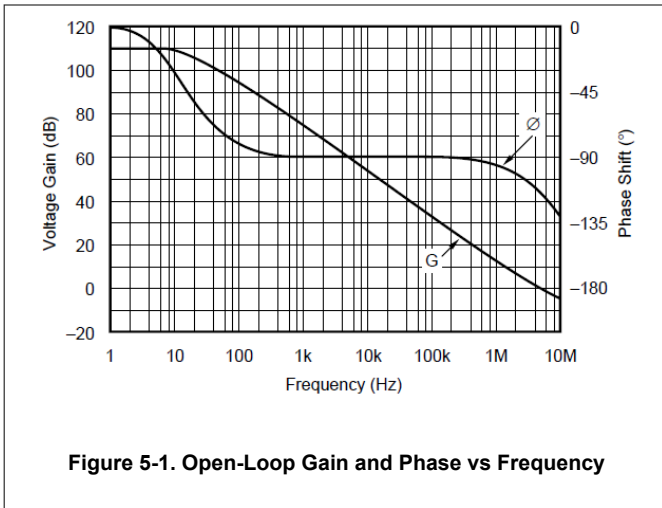
at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to midsupply, and  $V_{CM} = V_{OUT} = \text{midsupply}$  (unless otherwise noted)

| PARAMETER                 |                                      | TEST CONDITIONS                                   |                                  | MIN                         | TYP                     | MAX        | UNIT                         |
|---------------------------|--------------------------------------|---|----------------------------------|-----------------------------|-------------------------|------------|------------------------------|
| <b>OFFSET VOLTAGE</b>     |                                      |   |                                  |                             |                         |            |                              |
| $V_{OS}$                  | Input offset voltage                 | OPAx131UA   |                                  |                             | $\pm 0.2$               | $\pm 1$    | mV                           |
|                           |                                      | OPA2131U, OPA4131U                                |                                  |                             | $\pm 0.2$               | $\pm 1.5$  |                              |
|                           |                                      | OPA131U   |                                  |                             | $\pm 0.2$               | $\pm 0.75$ |                              |
| $dV_{OS}/dT$              | Input offset voltage drift           | $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$  |                                  |                             | $\pm 2$                 | $\pm 10$   | $\mu\text{V}/^\circ\text{C}$ |
| PSRR                      | Power-supply rejection ratio         | $9\text{V} \leq V_S \leq 36\text{V}$              | OPAx131UA,<br>OPA2131U, OPA4131U |                             | $\pm 50$                | $\pm 200$  | $\mu\text{V}/\text{V}$       |
|                           |                                      |   | OPA131U                          |                             | $\pm 50$                | $\pm 100$  |                              |
| <b>INPUT BIAS CURRENT</b> |                                      |   |                                  |                             |                         |            |                              |
| $I_B$                     | Input bias current <sup>(1)</sup>    |   |                                  |                             | $\pm 5$                 | $\pm 50$   | pA                           |
|                           |                                      | $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$  |                                  | See Typical Characteristics |                         |            |                              |
| $I_{OS}$                  | Input offset current <sup>(1)</sup>  |   |                                  |                             | $\pm 1$                 | $\pm 50$   | pA                           |
| <b>NOISE</b>              |                                      |   |                                  |                             |                         |            |                              |
| $e_n$                     | Input voltage noise density          | f = 10Hz  |                                  |                             | 21                      |            | nV/ $\sqrt{\text{Hz}}$       |
|                           |                                      | f = 100Hz   |                                  |                             | 16                      |            |                              |
|                           |                                      | f = 1kHz  |                                  |                             | 15                      |            |                              |
|                           |                                      | f = 10kHz   |                                  |                             | 15                      |            |                              |
| $I_n$                     | Input current noise density          | f = 1kHz  |                                  |                             | 3                       |            | fA/ $\sqrt{\text{Hz}}$       |
| <b>INPUT VOLTAGE</b>      |                                      |   |                                  |                             |                         |            |                              |
| $V_{CM}$                  | Common-mode voltage                  |   |                                  | (V-) + 3                    |                         | (V+) - 3.5 | V                            |
| CMRR                      | Common-mode rejection ratio          | $-12\text{V} \leq V_{CM} \leq 11.5\text{V}$       | OPAx131UA,<br>OPA2131U, OPA4131U | 70                          | 80                      |            | dB                           |
|                           |                                      |   | OPA131U                          | 80                          | 86                      |            |                              |
| <b>INPUT IMPEDANCE</b>    |                                      |   |                                  |                             |                         |            |                              |
|                           | Differential                         |   |                                  |                             | $10^{10} \parallel 5$   |            | $\Omega \parallel \text{pF}$ |
|                           | Common-mode                          | $-13\text{V} \leq V_{CM} \leq 11.5\text{V}$       |                                  |                             | $10^{12} \parallel 4.3$ |            |                              |
| <b>OPEN-LOOP GAIN</b>     |                                      |   |                                  |                             |                         |            |                              |
| $A_{OL}$                  | Open-loop voltage gain               | $-12\text{V} \leq V_O \leq 12\text{V}$            | OPAx131UA,<br>OPA2131U, OPA4131U | 94                          | 110                     |            | dB                           |
|                           |                                      |   | OPA131U                          | 100                         | 110                     |            |                              |
| <b>FREQUENCY RESPONSE</b> |                                      |   |                                  |                             |                         |            |                              |
| GBW                       | Gain bandwidth product               |   |                                  |                             | 4                       |            | MHz                          |
| SR                        | Slew rate                            |   |                                  |                             | 10                      |            | V/ $\mu\text{s}$             |
|                           | Settling time                        | 10V step, G = 1                                   | 0.1%                             |                             | 1.5                     |            | $\mu\text{s}$                |
|                           |                                      |   | 0.01%                            |                             | 2                       |            |                              |
| THD+N                     | Total harmonic distortion plus noise | f = 1kHz, G = 1, $V_O = 3.5\text{V}_{\text{rms}}$ |                                  |                             | 0.0008%                 |            |                              |
| <b>OUTPUT</b>             |                                      |   |                                  |                             |                         |            |                              |
| $V_O$                     | Voltage output                       | $R_L = 2\text{k}\Omega$                           | Positive                         | (V+) - 3                    | (V+) - 2.5              |            | V                            |
|                           |                                      |   | Negative                         | (V-) + 2.5                  | (V-) + 3                |            |                              |
| $I_{SC}$                  | Short-circuit current                |   |                                  |                             | $\pm 20$                |            | mA                           |
| <b>POWER SUPPLY</b>       |                                      |   |                                  |                             |                         |            |                              |
| $I_Q$                     | Quiescent current (per amplifier)    | $I_O = 0\text{mA}$                                | OPAx131UA                        |                             | $\pm 1.5$               | $\pm 1.75$ | mA                           |
|                           |                                      |   | OPAx131U                         |                             | $\pm 1.5$               | $\pm 2$    |                              |

(1) High-speed test at  $T_J = 25^\circ\text{C}$ .

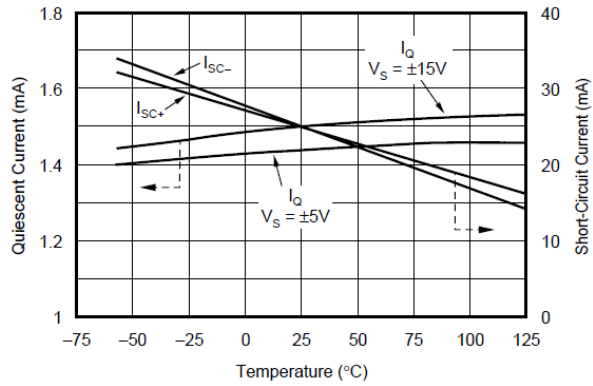
### 5.7 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to midsupply, and  $V_{CM} = V_{OUT} = \text{midsupply}$  (unless otherwise noted)

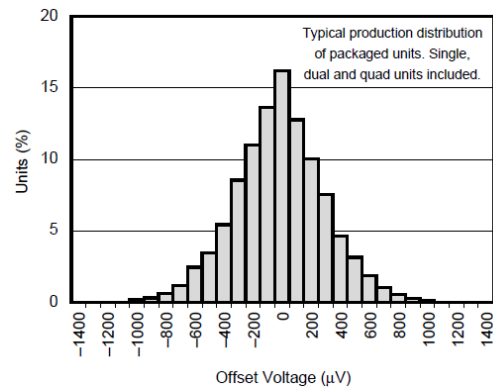


### 5.7 Typical Characteristics (continued)

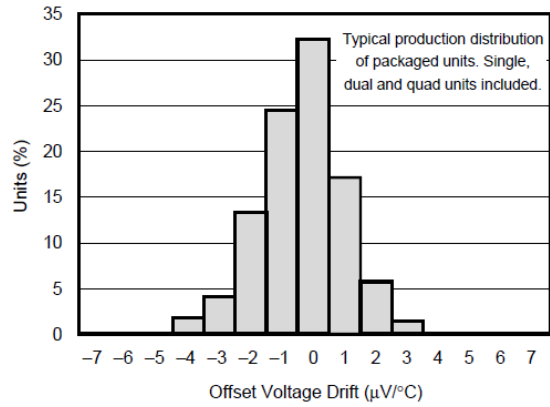
at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to midsupply, and  $V_{CM} = V_{OUT} = \text{midsupply}$  (unless otherwise noted)



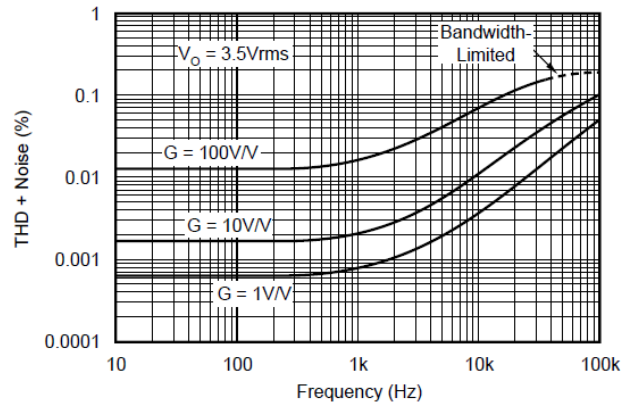
**Figure 5-7. Quiescent Current and Short-Circuit Current vs Temperature**



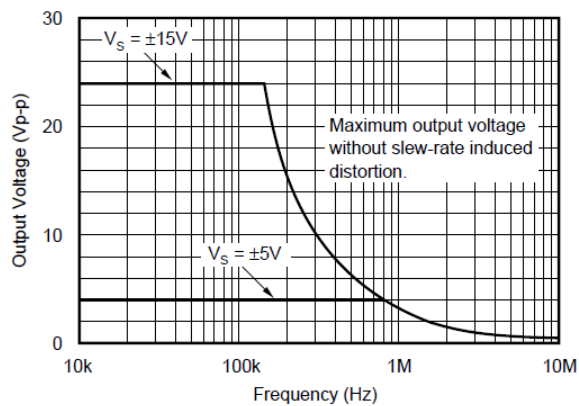
**Figure 5-8. Offset Voltage Production Distribution**



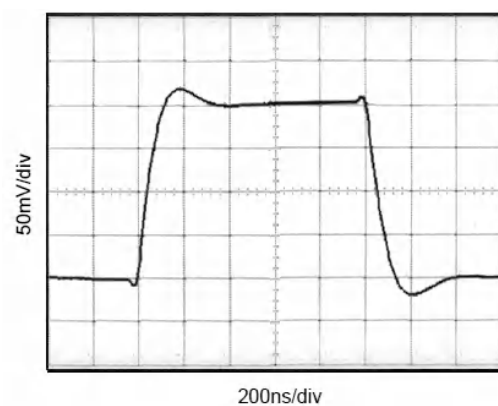
**Figure 5-9. Offset Voltage Drift Production Distribution**



**Figure 5-10. Total Harmonic Distortion + Noise vs Frequency**



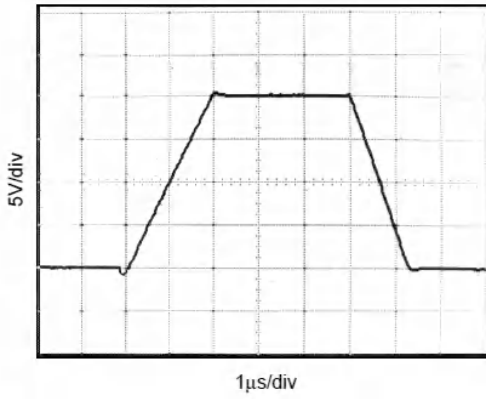
**Figure 5-11. Maximum Output Voltage vs Frequency**



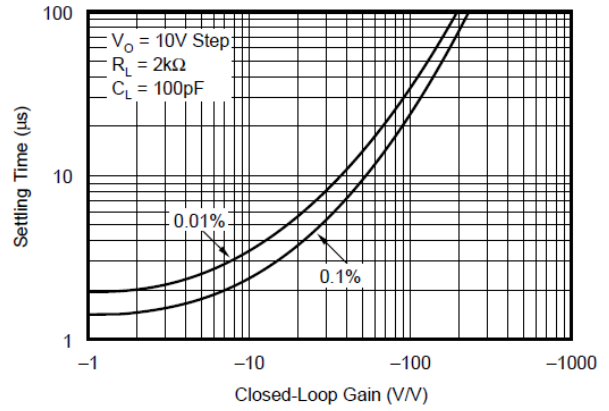
**Figure 5-12. Small-Signal Step Response  $G = 1$ ,  $C_L = 300\text{pF}$**

### 5.7 Typical Characteristics (continued)

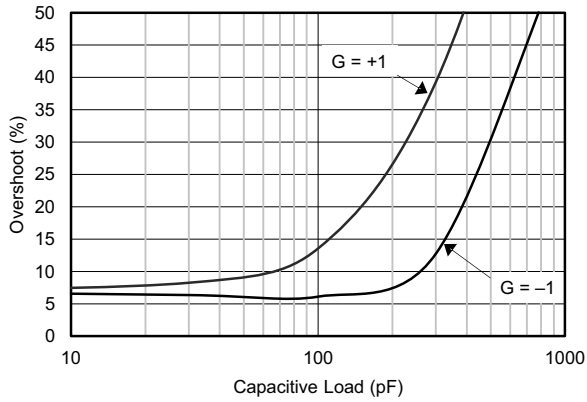
at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to midsupply, and  $V_{CM} = V_{OUT} = \text{midsupply}$  (unless otherwise noted)



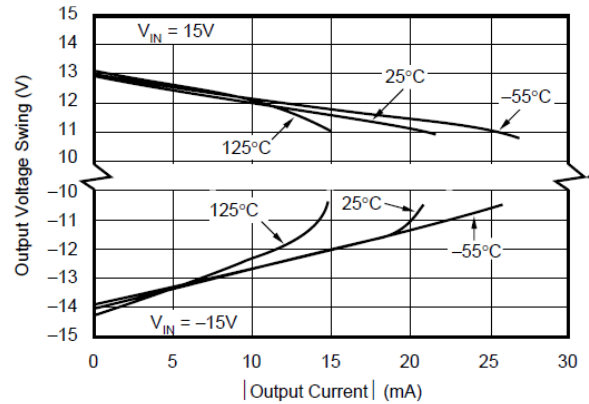
**Figure 5-13. Large-Signal Step Response  $G = 1$ ,  $C_L = 300\text{pF}$**



**Figure 5-14. Settling Time vs Closed-Loop Gain**



**Figure 5-15. Small-Signal Overshoot vs Load Capacitance**



**Figure 5-16. Output Voltage Swing vs Output Current**

## 6 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 6.1 Application Information

The OPAx131 series op amps are unity-gain stable and an excellent choice for a wide range of general-purpose applications. Bypass power-supply pins with 10nF ceramic capacitors or larger.

The OPAx131 series op amps are free from unexpected output phase-reversal common with FET op amps. Many FET-input op amps exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control-loop applications. All circuitry is completely independent in dual and quad versions, and normal behavior can be expected when one amplifier in a package is overdriven or short-circuited.

#### 6.1.1 Offset Voltage Trim

The offset voltage of the OPAx131 amplifiers is laser trimmed and usually requires no user adjustment. The OPAx131 provide less than  $\pm 1\text{mV}$  of input offset voltage and less than  $10\mu\text{V}/^\circ\text{C}$  of input offset voltage drift over the operating temperature range.

### 6.2 Typical Application

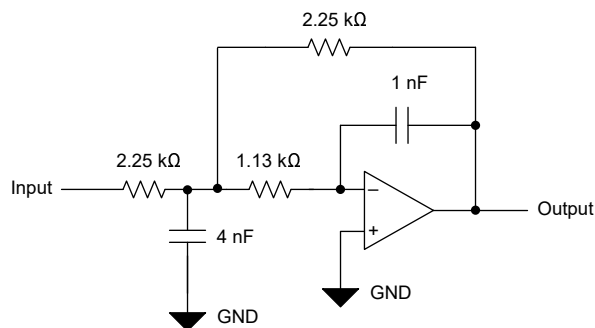


Figure 6-1. Second-Order Low-Pass Filter

#### 6.2.1 Input Bias Current

The input bias current is approximately 5pA at room temperature and increases with temperature (see also [Figure 5-5](#)). Input bias current also varies with common-mode voltage and power-supply voltage. This variation depends on the voltage between the negative power supply and the common-mode input voltage.

## 7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 7.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 7.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 7.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision A (December 2002) to Revision B (July 2024)</b>  | <b>Page</b> |
|---|-------------|
| • Updated the numbering format for tables, figures, and cross-references throughout the document.....   | 1           |
| • Added the <i>Device Information</i> table, and the <i>Applications, Pin Configuration and Functions, Specifications, Recommended Operating Conditions, Thermal Information, Application and Implementation, Typical Application, Device and Documentation Support, and Mechanical, Packaging, and Orderable Information</i> sections..... | 1           |
| • Updated <i>Description</i> .....  | 1           |
| • Deleted obsolete PDIP packages for OPA131 and OPA2131.....  | 3           |
| • Updated input voltage in <i>Absolute Maximum Ratings</i> .....  | 6           |
| • Added input current and related footnote to <i>Absolute Maximum Ratings</i> .....   | 6           |
| • Changed format of <i>Electrical Characteristics</i> to latest standard.....   | 8           |
| • Updated nominal conditions in the header of <i>Electrical Characteristics</i> .....   | 8           |
| • Deleted channel separation specification.....   | 8           |
| • Updated common-mode voltage MAX value.....  | 8           |
| • Updated common-mode rejection ratio and common-mode input impedance test conditions.....  | 8           |
| • Changed differential input impedance from 10 <sup>10</sup> Ω    1pF to 10 <sup>10</sup> Ω    5pF.....   | 8           |
| • Changed common-mode input impedance from 10 <sup>10</sup> Ω    3pF to 10 <sup>10</sup> Ω    4.3pF.....  | 8           |
| • Updated open loop voltage gain MIN and TYP values for R <sub>L</sub> = 10kΩ and R <sub>L</sub> = 2kΩ.....   | 8           |
| • Updated settling time test condition.....   | 8           |
| • Moved voltage output negative MIN values to MAX values.....   | 8           |

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|  |    |
|--|----|
| • Deleted note 1 from <i>Electrical Characteristics</i> .....  | 8  |
| • Updated Figure 5-15, <i>Small-Signal Overshoot vs Load Capacitance</i> .....                           | 9  |
| • Updated text in <i>Offset Voltage Trim</i> .....   | 12 |
| • Changed Figure 1, OPA130 Offset Voltage Trim Circuit, to Figure 6-1, Second-Order Low-Pass Filter..... | 12 |
| • Updated <i>Input Bias Current</i> description.....   | 12 |

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## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)   | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|---------------------------|-------------------------|
| OPA131U          | ACTIVE        | SOIC         | D               | 8    | 75          | RoHS & Green    | Call TI   NIPDAU                     | Level-3-260C-168 HR  | -55 to 125   | (O131U, OPA)<br>131U      | <a href="#">Samples</a> |
| OPA131UA         | ACTIVE        | SOIC         | D               | 8    | 75          | RoHS & Green    | Call TI   NIPDAU                     | Level-3-260C-168 HR  | -55 to 125   | (O131U, OPA)<br>131U<br>A | <a href="#">Samples</a> |
| OPA131UA/2K5     | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | Call TI   NIPDAU                     | Level-3-260C-168 HR  | -55 to 125   | (O131U, OPA)<br>131U<br>A | <a href="#">Samples</a> |
| OPA131UJ         | ACTIVE        | SOIC         | D               | 8    | 75          | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -55 to 125   | (O131UJ, OPA)<br>131UJ    | <a href="#">Samples</a> |
| OPA131UJ/2K5     | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -55 to 125   | (O131UJ, OPA)<br>131UJ    | <a href="#">Samples</a> |
| OPA2131UA        | ACTIVE        | SOIC         | D               | 8    | 75          | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -55 to 125   | OPA<br>2131UA             | <a href="#">Samples</a> |
| OPA2131UA/2K5    | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -55 to 125   | (2131UA, OPA)             | <a href="#">Samples</a> |
| OPA2131UJ        | ACTIVE        | SOIC         | D               | 8    | 75          | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  |              | (2131UJ, OPA)             | <a href="#">Samples</a> |
| OPA2131UJ/2K5    | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  |              | (2131UJ, OPA)             | <a href="#">Samples</a> |
| OPA4131NA        | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green    | NIPDAU-DCC                           | Level-3-260C-168 HR  | -40 to 85    | OPA4131NA                 | <a href="#">Samples</a> |
| OPA4131NJ        | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green    | NIPDAU-DCC                           | Level-3-260C-168 HR  | -40 to 85    | OPA4131NJ                 | <a href="#">Samples</a> |
| OPA4131PA        | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | -40 to 85    | OPA4131PA                 | <a href="#">Samples</a> |
| OPA4131PAG4      | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | -40 to 85    | OPA4131PA                 | <a href="#">Samples</a> |
| OPA4131PJ        | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | -40 to 85    | OPA4131PJ                 | <a href="#">Samples</a> |
| OPA4131UA        | ACTIVE        | SOIC         | DW              | 16   | 40          | RoHS & Green    | NIPDAU-DCC                           | Level-3-260C-168 HR  | -40 to 85    | OPA4131UA                 | <a href="#">Samples</a> |
| OPA4131UA/1K     | ACTIVE        | SOIC         | DW              | 16   | 1000        | RoHS & Green    | NIPDAU-DCC                           | Level-3-260C-168 HR  | -40 to 85    | OPA4131UA                 | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| OPA131UA/2K5  | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| OPA131UA/2K5  | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| OPA131UJ/2K5  | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| OPA131UJ/2K5  | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| OPA2131UA/2K5 | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| OPA2131UJ/2K5 | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| OPA4131UA/1K  | SOIC         | DW              | 16   | 1000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| OPA131UA/2K5  | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| OPA131UA/2K5  | SOIC         | D               | 8    | 2500 | 356.0       | 356.0      | 35.0        |
| OPA131UJ/2K5  | SOIC         | D               | 8    | 2500 | 356.0       | 356.0      | 35.0        |
| OPA131UJ/2K5  | SOIC         | D               | 8    | 2500 | 356.0       | 356.0      | 35.0        |
| OPA2131UA/2K5 | SOIC         | D               | 8    | 2500 | 356.0       | 356.0      | 35.0        |
| OPA2131UJ/2K5 | SOIC         | D               | 8    | 2500 | 356.0       | 356.0      | 35.0        |
| OPA4131UA/1K  | SOIC         | DW              | 16   | 1000 | 356.0       | 356.0      | 35.0        |

**TUBE**


\*All dimensions are nominal

| Device      | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| OPA131U     | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| OPA131U     | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| OPA131UA    | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| OPA131UA    | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| OPA131UJ    | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| OPA2131UA   | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| OPA2131UAE4 | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| OPA2131UAG4 | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| OPA2131UJ   | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| OPA4131NA   | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| OPA4131NJ   | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| OPA4131PA   | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| OPA4131PAG4 | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| OPA4131PJ   | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| OPA4131UA   | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |

## GENERIC PACKAGE VIEW

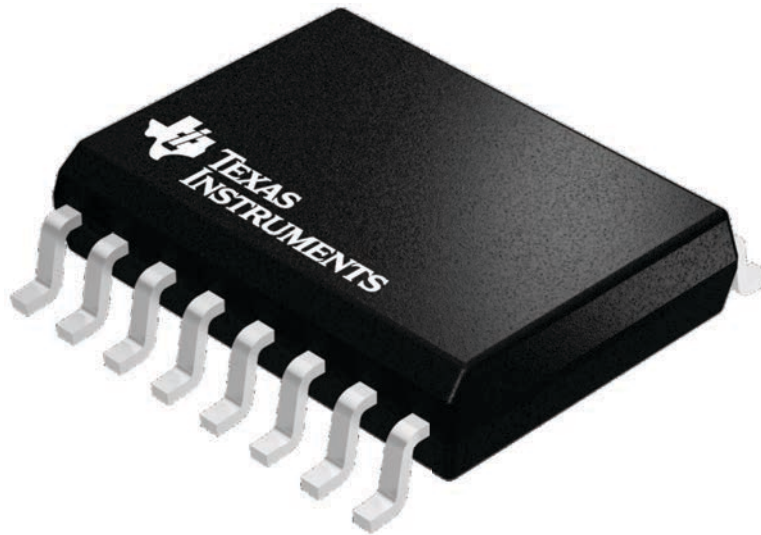
**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



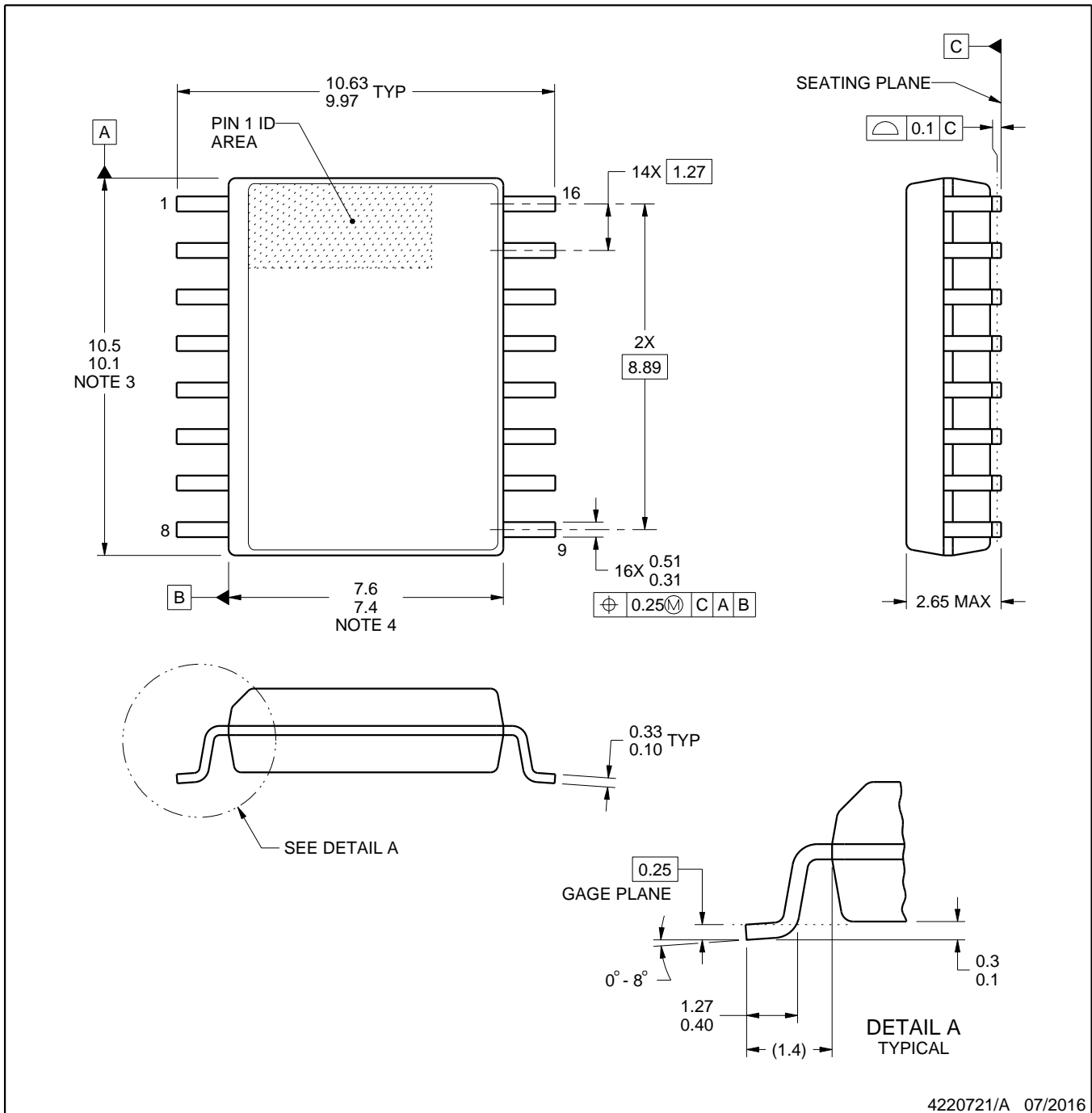
4224780/A



# DW0016A

# PACKAGE OUTLINE SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

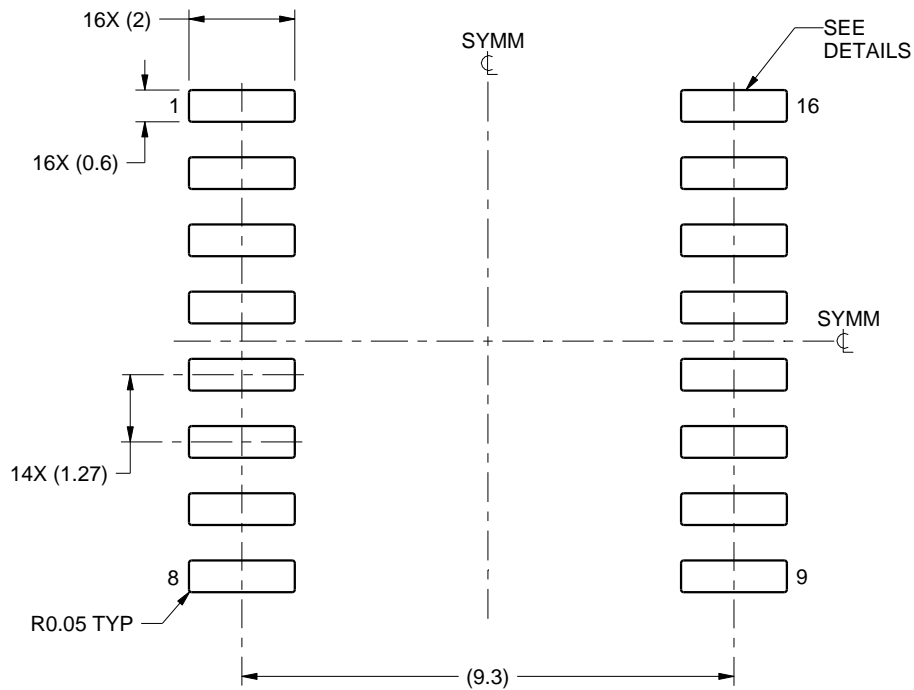
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

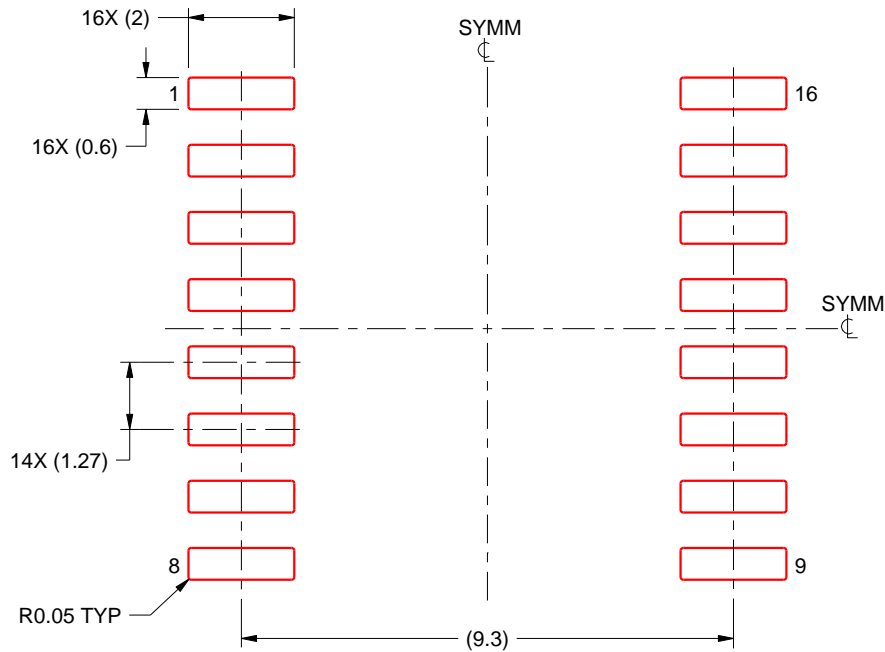
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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