WINSOURCE ELECTRONICS

THE DATASHEET OF

ADMV7410BCEZ

E-Band Low Noise Downconverter SiP, 71 GHz to 76 GHz

Data Sheet

ADMV7410

FEATURES

Conversion gain: 13 dB typical
Image rejection: 30 dBc typical
Noise figure: 5 dB typical
Input IP3: 1 dBm typical
Input IP2: 28 dBm typical
Input P1dB: −8 dBm typical
6× LO leakage at RFIN: <−55 dBm typical
I/Q amplitude imbalance: 0.2 dB typical
I/Q phase imbalance: 5° typical
Fully integrated, surface-mount, 34-terminal, 11 mm × 13 mm LGA_CAV package

APPLICATIONS

E-band communication systems
High capacity wireless backhauls
Test and measurement
Aerospace and defense

FUNCTIONAL BLOCK DIAGRAM

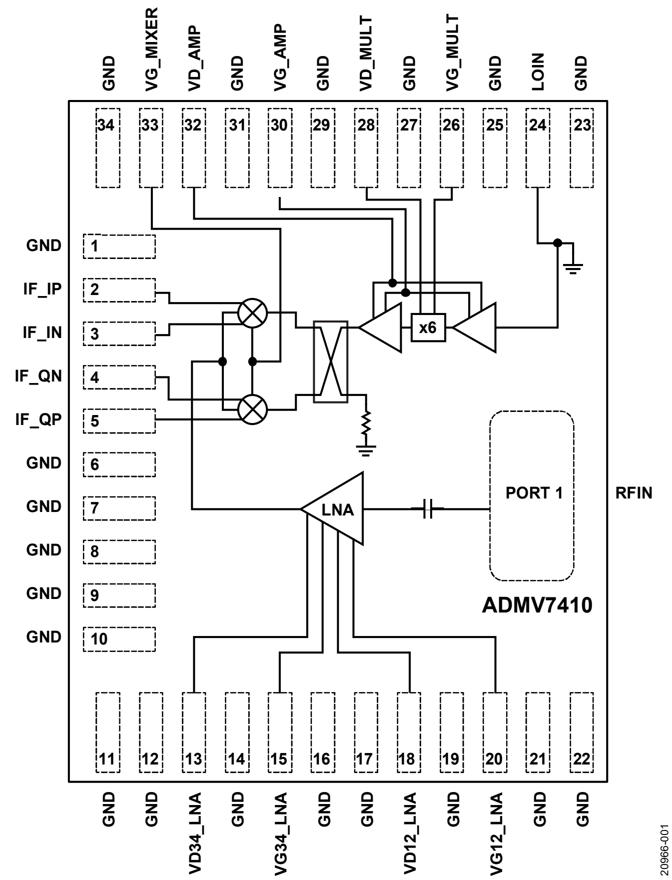

Figure 1.

GENERAL DESCRIPTION

The ADMV7410 is a fully integrated system in package (SiP) in phase/quadrature (I/Q) downconverter that operates between an intermediate frequency (IF) output range of dc and 2 GHz and a RF input range of 71 GHz and 76 GHz. The device provides a small signal conversion gain of 13 dB with 30 dBc of image rejection. The ADMV7410 uses a low noise amplifier followed by an image rejection mixer that is driven by a 6× local oscillator (LO) multiplier. Differential I and Q mixer outputs are provided for direct conversion applications. Alternatively, the outputs can be combined using an external 90° hybrid and two external 180° hybrids for single-ended applications.

The ADMV7410 comes in a fully integrated, surface-mount, 34-terminal, 11 mm × 13 mm, chip array small outline no lead cavity (LGA_CAV) package. The ADMV7410 operates over the −40°C to +85°C case temperature range.

Rev. B Document Feedback

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Technical Support **www.analog.com**

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REVISION HISTORY

10/2021—Rev. A to Rev. B

Updated Outline Dimensions ... 25

7/2019—Revision A: Initial Version

SPECIFICATIONS

T_A = −40°C to +85°C, IF = 1 GHz, LO power = 4 dBm, VD_AMP = +4 V, VG_MIXER = −1 V, VD_MULT = +1.5 V, VD12_LNA = +2 V, and VD34_LNA = +4 V, unless otherwise noted. Measurements performed as a downconverter with lower sideband selected and an external 90° hybrid followed by two external 180° hybrids at the IF ports, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit
OPERATING CONDITIONS					
Frequency Range					
RF		71		76	GHz
LO		11.5		13	GHz
IF Output		DC		2	GHz
LO Drive Level Range		0	4	8	dBm
PERFORMANCE					
Conversion Gain		7	13	20	dB
Gain Flatness			2		dB
Image Rejection		15	30		dBc
Input Power for 1 dB Compression (Input P1dB)		−13	−8		dBm
Input Third-Order Intercept (Input IP3)		−6	1		dBm
Input Second-Order Intercept (Input IP2)		15	28		dBm
6× LO Leakage at the RF Input Port (RFIN)			<−55	−50	dBm
I/Q Amplitude Imbalance			0.2	3	dB
I/Q Phase Imbalance		−10	5	10	Degrees
Noise Figure			5	8	dB
Return Loss					
RFIN			10		dB
LO Input Port (LOIN)			10		dB
Baseband Output Port[1]			10		dB
DIFFERENTIAL BASEBAND OUTPUT PORT IMPEDANCE			100		Ω
LOIN PORT IMPEDANCE			50		Ω
POWER SUPPLY					
DC Power Dissipation			1	1.25	W
Low Noise Amplifier Gate Voltage	VG12_LNA, VG34_LNA	−2		0	V
Low Noise Amplifier Drain Voltage					
First and Second Stage	VD12_LNA	1.9	2	2.1	V
Third and Fourth Stage	VD34_LNA	3.8	4	4.2	V
Multiplier Drain Voltage	VD_MULT	1.42	1.5	1.58	V
Multiplier Gate Voltage	VG_MULT	−2		0	V
Mixer Gate Voltage	VG_MIX	−2		0	V
Low Noise Amplifier Supply Current	I_{VD12_LNA} and I_{VD34_LNA}		66		mA
Amplifier Drain Current	I_{VD_AMP}		175		mA
Multiplier Drain Current	I_{VD_MULT}		80		mA

[1] Measurements taken without external hybrids at the IF ports.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VD_AMP	4.5 V
VD_MULT	3 V
VD12_LNA and VD34_LNA	4.5 V
VG_AMP	−3 V to +0.2 V
VG_MULT	−3 V to +0.2 V
VG12_LNA and VG34_LNA	−3 V to +0.2 V
LO Drive	10 dBm
Baseband Input (IF_IP, IF_IN, IF_QP, and IF_QN)	4 dBm
IF Source and Sink Current	3 mA
Nominal Junction Temperature (T_A = 85°C)	137°C
Maximum Junction Temperature (to Maintain 3 Million Hours Mean Time to Failure (MTTF))	175°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +150°C
Maximum Peak Reflow Temperature for Moisture Sensitivity Level 3 (MSL3)	260°C
Thermal Humidity Bias (THB)	JESD22-A101[1,2,3]
Thermal Humidity Storage (THS)	JESD22-A101[1,3]
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	250 V
Field Induced Charged Device Model (FICDM)	500 V

[1] Samples subject to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: bake for 24 hours at 125°C, unbiased soak for 192 hours at 30°C and 60% relative humidity (RH), and reflow of three passes through an oven with a peak temperature of 260°C.
[2] Results valid for 400 mW of nominal dc power dissipation for all active devices. Analog Devices, Inc., recommends that users perform their own THB test for all other bias conditions.
[3] Valid for package vent hole solder sealed or unsealed during test.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case (or die to package) thermal resistance.

Table 3. Thermal Resistance[1]

Package Type	θ_{JC}	Unit
CE-34-2	52.4	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P test board with 11 mm × 13 mm thermal vias. Refer to JEDEC standard JESD51-2 for additional information.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

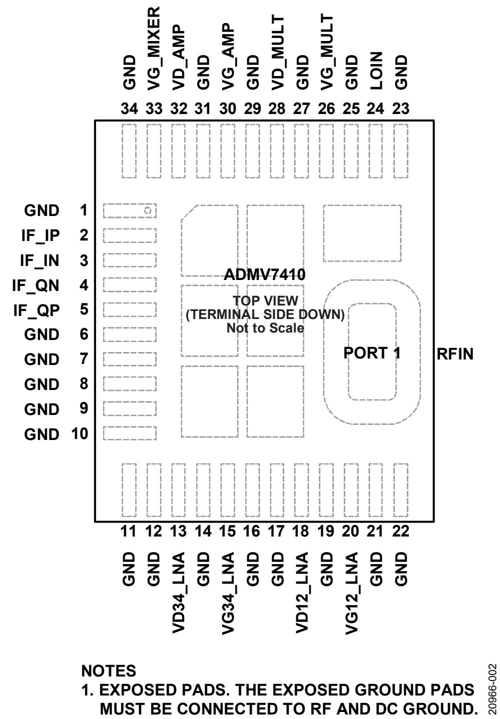


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 6 to 12, 14, 16, 17, 19, 21 to 23, 25, 27, 29, 31, 34	GND	Ground Connections. These pins must be connected to RF and dc ground.
2	IF_IP	Positive IF In Phase Output. This pin is dc-coupled. When operation to dc is not required, block this pin externally using a series capacitor with a value chosen to pass the necessary frequency range. For operation to dc, this pin must not source or sink more than 3 mA of current or device malfunction and device failure may result.
3	IF_IN	Negative IF In Phase Output. This pin is dc-coupled. When operation to dc is not required, block this pin externally using a series capacitor with a value chosen to pass the necessary frequency range. For operation to dc, this pin must not source or sink more than 3 mA of current or device malfunction and device failure may result.
4	IF_QN	Negative IF Quadrature Output. This pin is dc-coupled. When operation to dc is not required, block this pin externally using a series capacitor with a value chosen to pass the necessary frequency range. For operation to dc, this pin must not source or sink more than 3 mA of current or device malfunction and device failure may result.
5	IF_QP	Positive IF Quadrature Output. This pin is dc-coupled. When operation to dc is not required, block this pin externally using a series capacitor with a value chosen to pass the necessary frequency range. For operation to dc, this pin must not source or sink more than 3 mA of current or device malfunction and device failure may result.
13	VD34_LNA	Drain Voltage for the Third and Fourth Stage Low Noise Amplifier. See Figure 75 for the recommended external components.
15	VG34_LNA	Gate Voltage for the Third and Fourth Stage Low Noise Amplifier. See Figure 75 for the recommended external components.
18	VD12_LNA	Drain Voltage for the First and Second Stage Low Noise Amplifier. See Figure 75 for the recommended external components.
20	VG12_LNA	Gate Voltage for the First and Second Stage Low Noise Amplifier. See Figure 75 for the recommended external components.

Pin No.	Mnemonic	Description
24	LOIN	LO Input. This pin is dc-coupled and matched to 50 Ω.
26	VG_MULT	Gate Voltage for the LO Multiplier. See Figure 75 for the recommended external components.
28	VD_MULT	Drain Voltage for the LO Multiplier. See Figure 75 for the recommended external components.
30	VG_AMP	Gate Voltage for the LO Amplifier. See Figure 75 for the recommended external components.
32	VD_AMP	Drain Voltage for the LO Amplifier. See Figure 75 for the recommended external components.
33	VG_MIXER	Gate Voltage for the Field Effect Transistor (FET) Mixer. See Figure 75 for the recommended external components.
PORT 1	RFIN	WR-12 Waveguide Port. This port is ac-coupled and matched to the waveguide input impedance.
	EPAD	Exposed Pads. The exposed ground pads must be connected to RF and dc ground.

INTERFACE SCHEMATICS

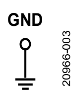


Figure 3. GND Interface Schematic

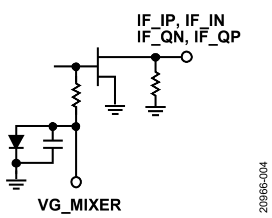


Figure 4. IF_IP, IF_IN, IF_QN, IF_QP, and VG_MIXER Interface Schematic

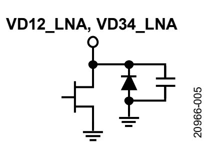


Figure 5. VD12_LNA and VD34_LNA Interface Schematic

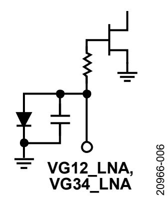


Figure 6. VG12_LNA and VG34_LNA Interface Schematic

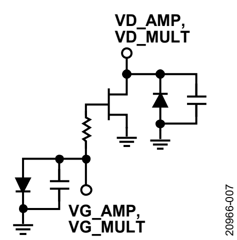


Figure 7. VG_MULT, VD_MULT, VG_AMP, and VD_AMP Interface Schematic

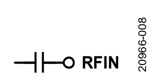


Figure 8. RFIN Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, IF = 1 GHz, RFIN = −20 dBm combined, LO power = +4 dBm, and lower sideband selected, unless otherwise noted.

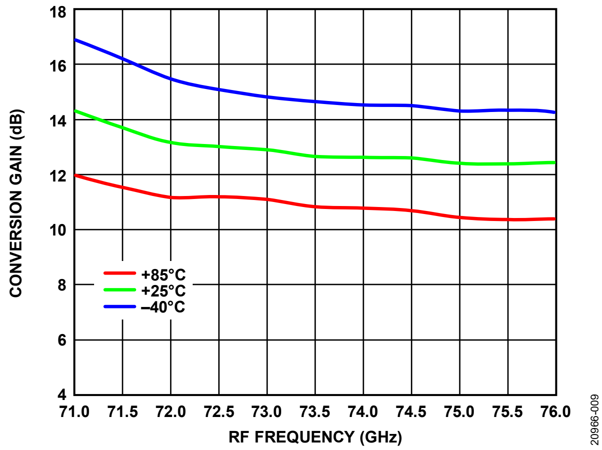


Figure 9. Conversion Gain vs. RF Frequency over Temperature

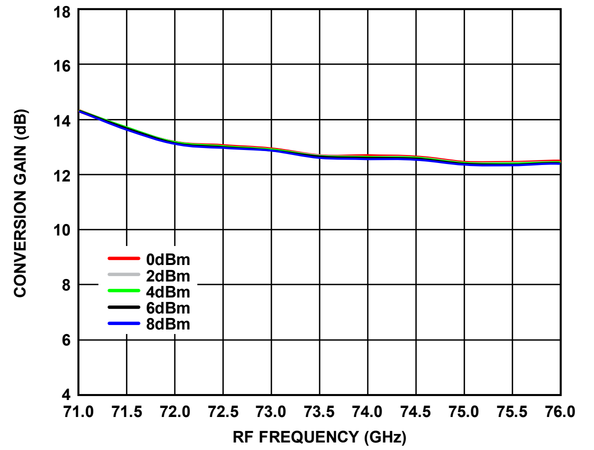


Figure 12. Conversion Gain vs. RF Frequency over LO Power

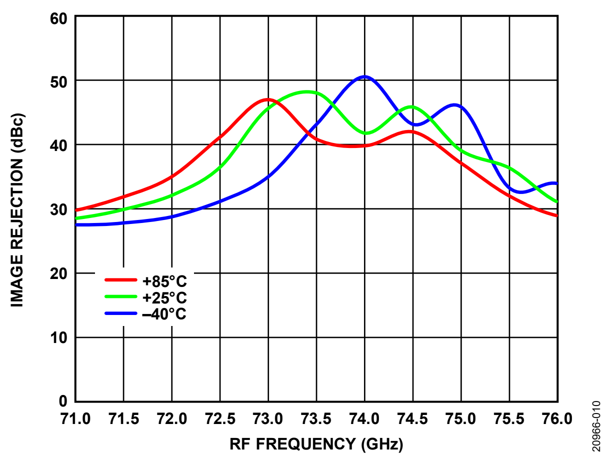


Figure 10. Image Rejection vs. RF Frequency over Temperature

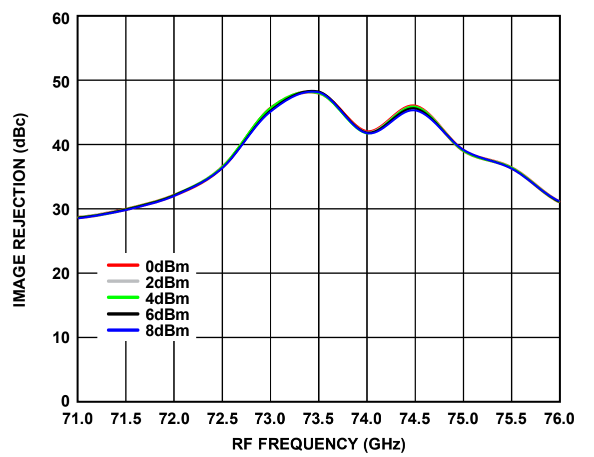


Figure 13. Image Rejection vs. RF Frequency over LO Power

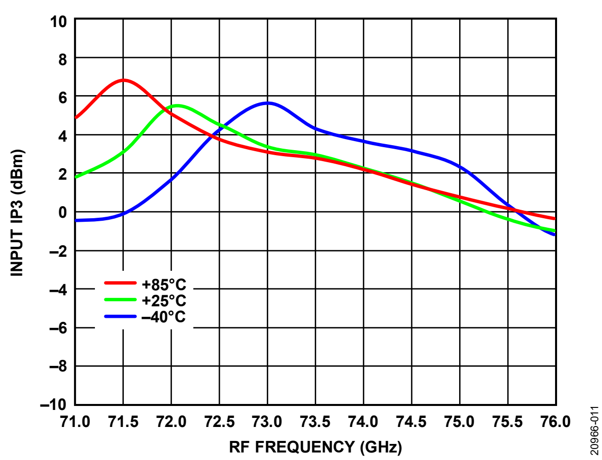


Figure 11. Input IP3 vs. RF Frequency over Temperature

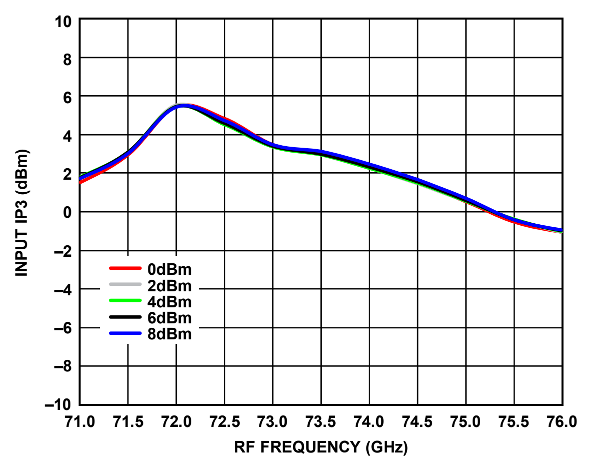


Figure 14. Input IP3 vs. RF Frequency over LO Power

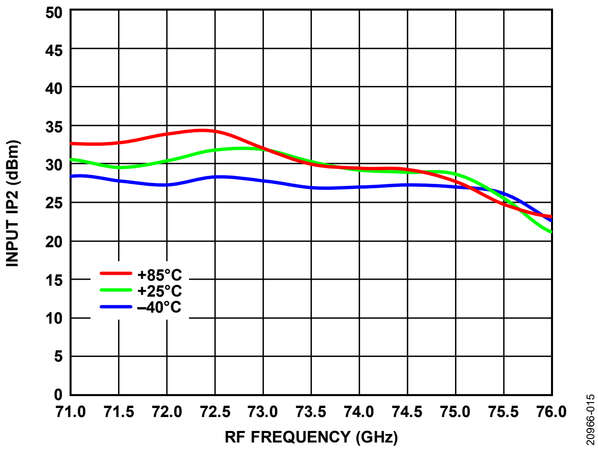


Figure 15. Input IP2 vs. RF Frequency over Temperature

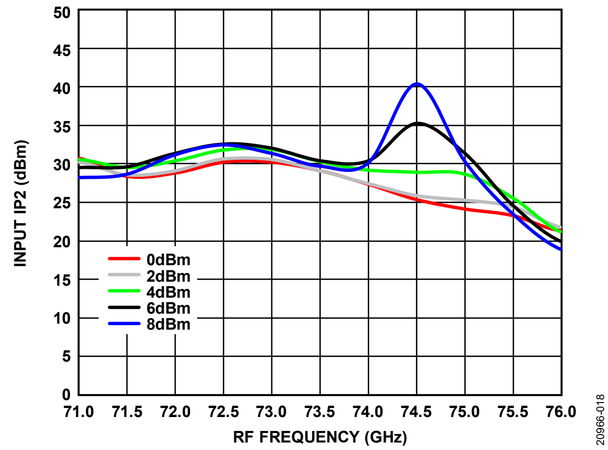


Figure 18. Input IP2 vs. RF Frequency over LO Power

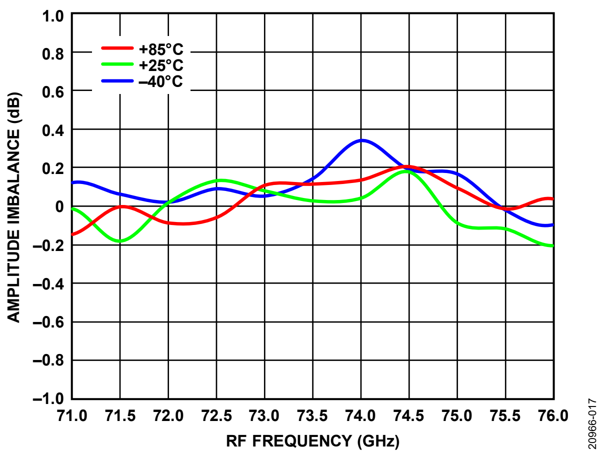


Figure 16. Amplitude Imbalance vs. RF Frequency over Temperature

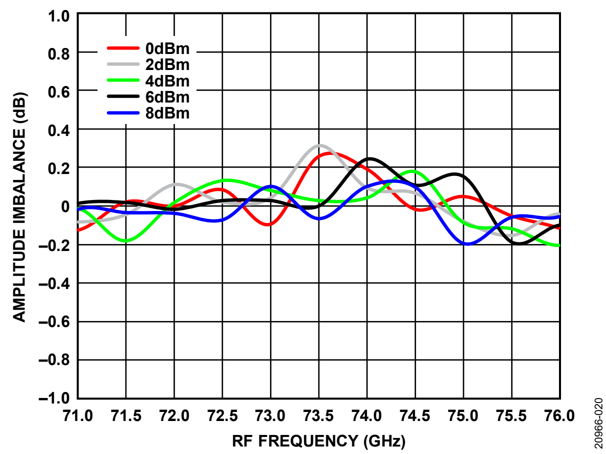


Figure 19. Amplitude Imbalance vs. RF Frequency over LO Power

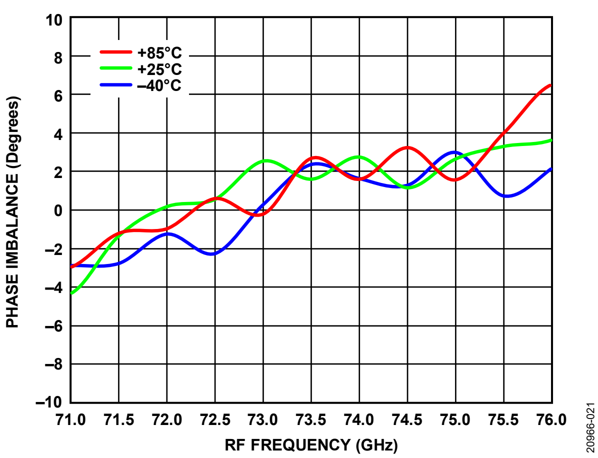


Figure 17. Phase Imbalance vs. RF Frequency over Temperature

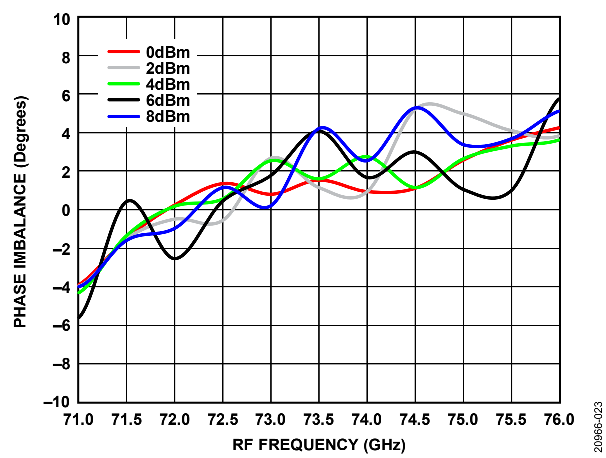


Figure 20. Phase Imbalance vs. RF Frequency over LO Power

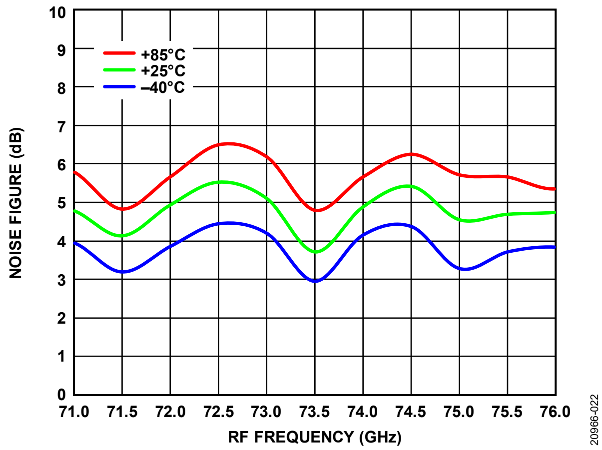


Figure 21. Noise Figure vs. RF Frequency over Temperature

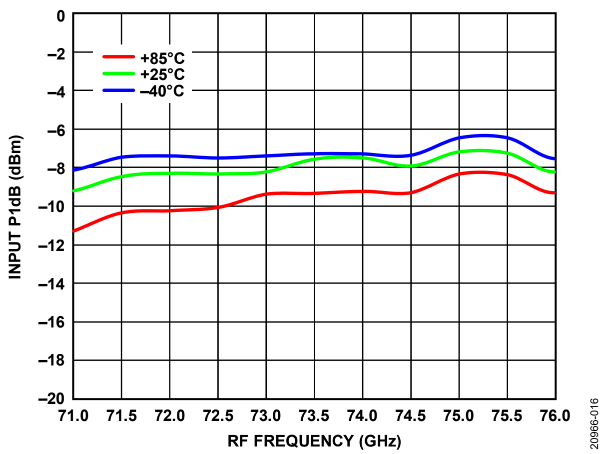


Figure 22. Input P1dB vs. RF Frequency over Temperature

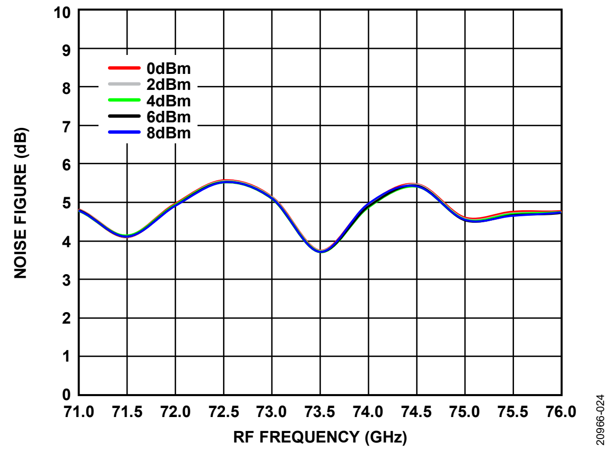


Figure 23. Noise Figure vs. RF Frequency over LO Power

T_A = 25°C, IF = 0.1 GHz, RFIN = −20 dBm combined, LO power = +4 dBm, and lower sideband selected, unless otherwise noted.

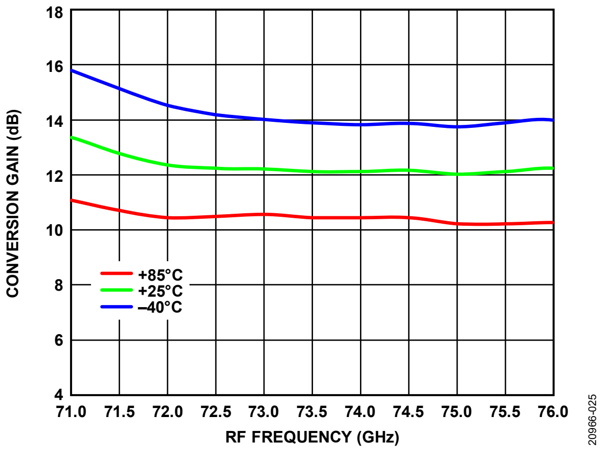


Figure 24. Conversion Gain vs. RF Frequency over Temperature

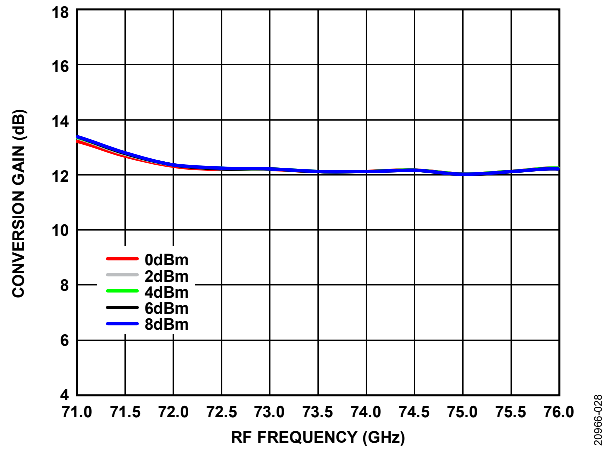


Figure 27. Conversion Gain vs. RF Frequency over LO Power

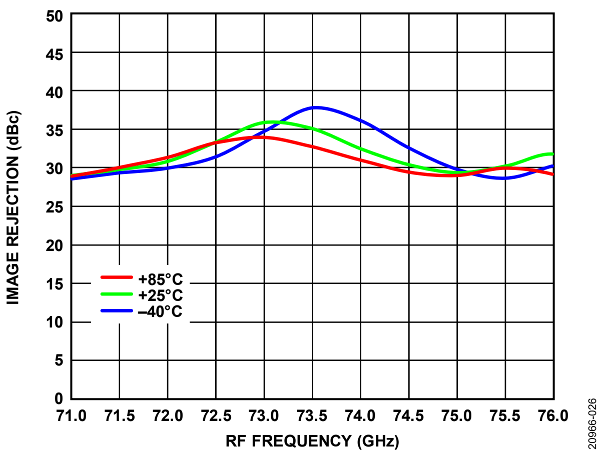


Figure 25. Image Rejection vs. RF Frequency over Temperature

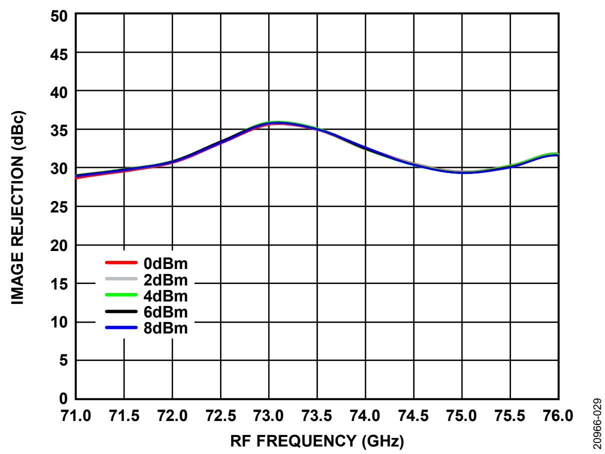


Figure 28. Image Rejection vs. RF Frequency over LO Power

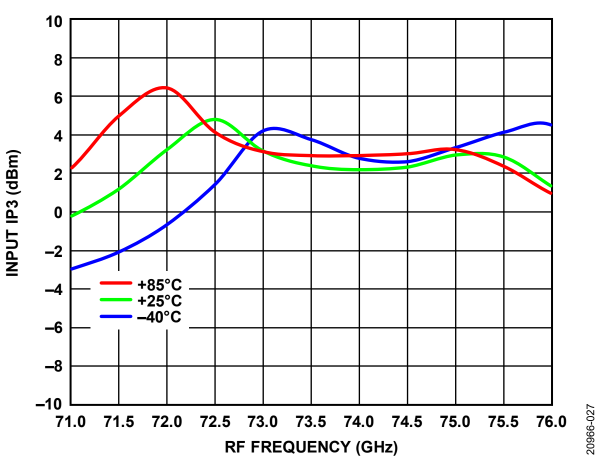


Figure 26. Input IP3 vs. RF Frequency over Temperature

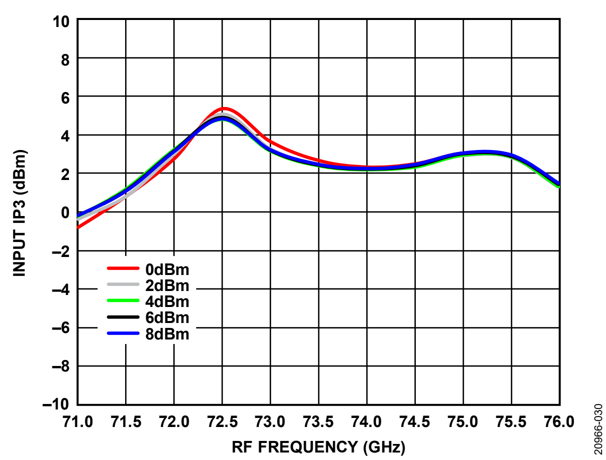


Figure 29. Input IP3 vs. RF Frequency over LO Power

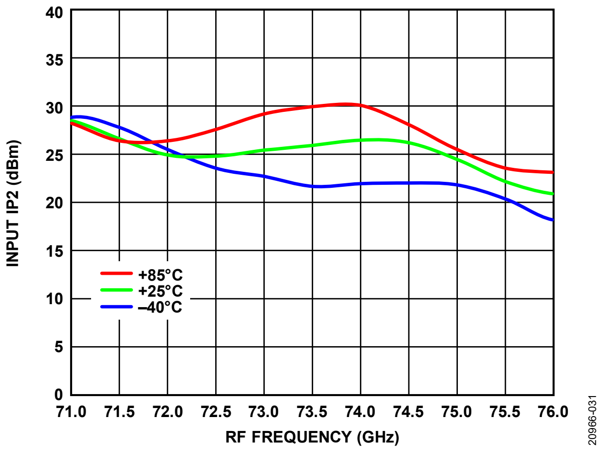


Figure 30. Input IP2 vs. RF Frequency over Temperature

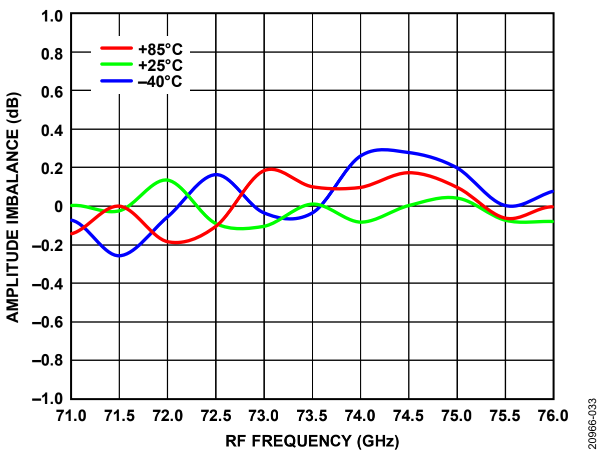


Figure 31. Amplitude Imbalance vs. RF Frequency over Temperature

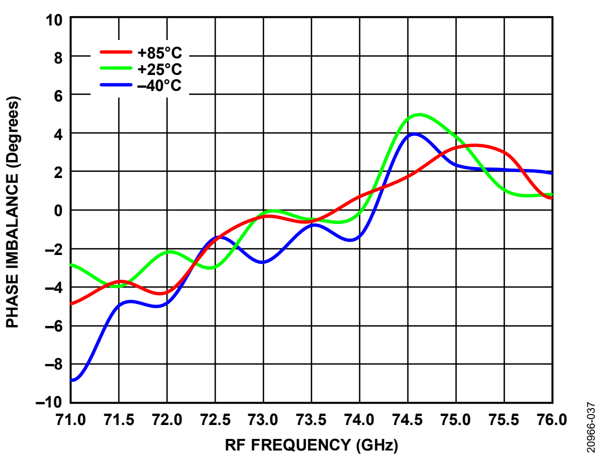


Figure 32. Phase Imbalance vs. RF Frequency over Temperature

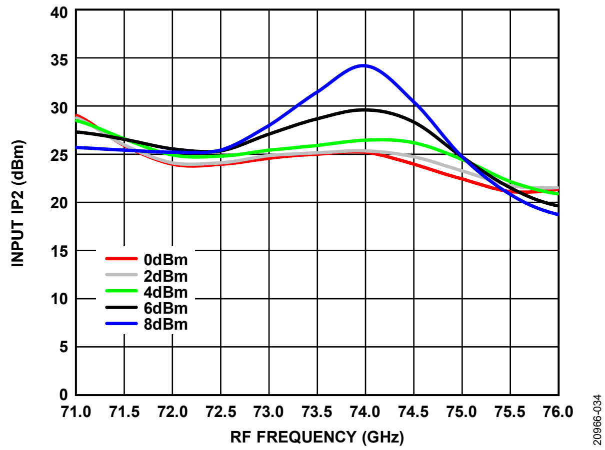


Figure 33. Input IP2 vs. RF Frequency over LO Power

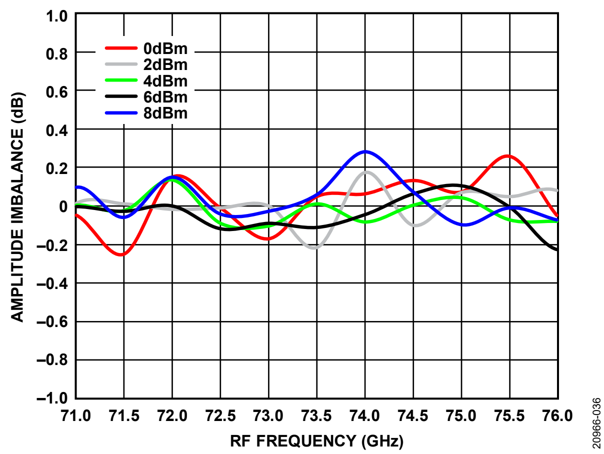


Figure 34. Amplitude Imbalance vs. RF Frequency over LO Power

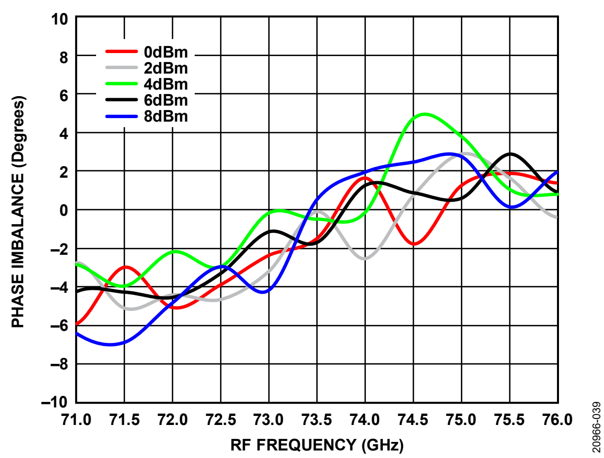


Figure 35. Phase Imbalance vs. RF Frequency over LO Power

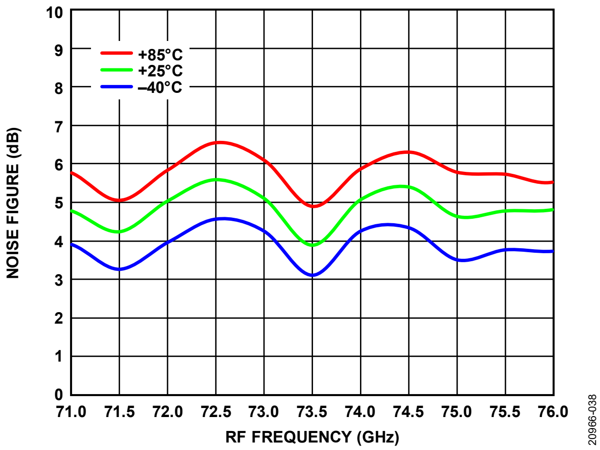


Figure 36. Noise Figure vs. RF Frequency over Temperature

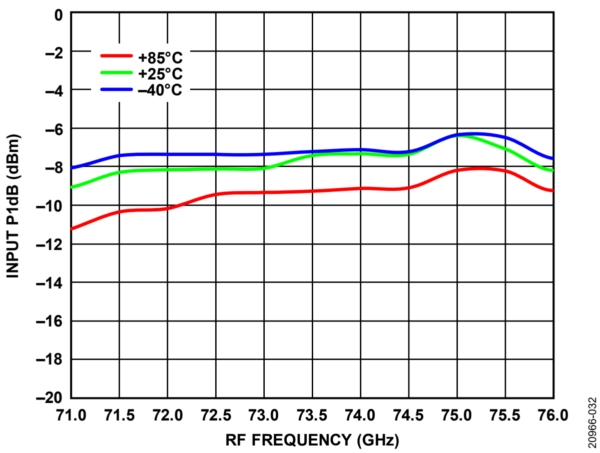


Figure 37. Input P1dB vs. RF Frequency over Temperature

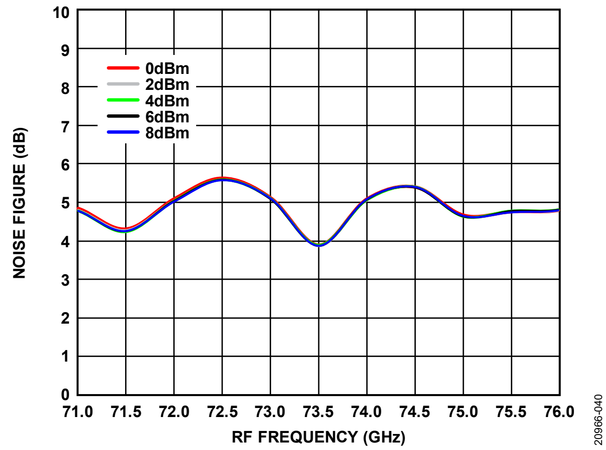


Figure 38. Noise Figure vs. RF Frequency over LO Power

T_A = 25°C, IF = 0.5 GHz, RFIN = −20 dBm combined, LO power = +4 dBm, and lower sideband selected, unless otherwise noted.

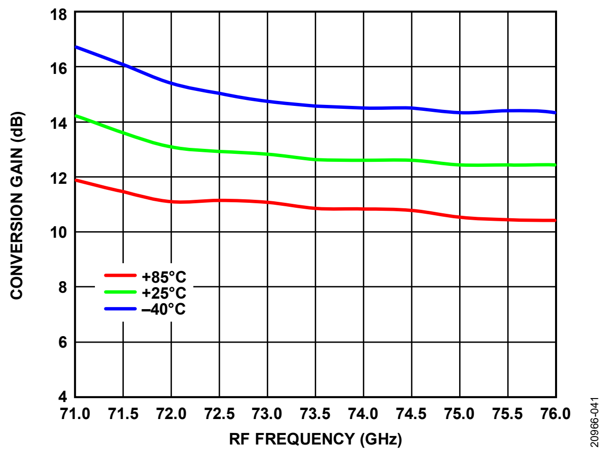


Figure 39. Conversion Gain vs. RF Frequency over Temperature

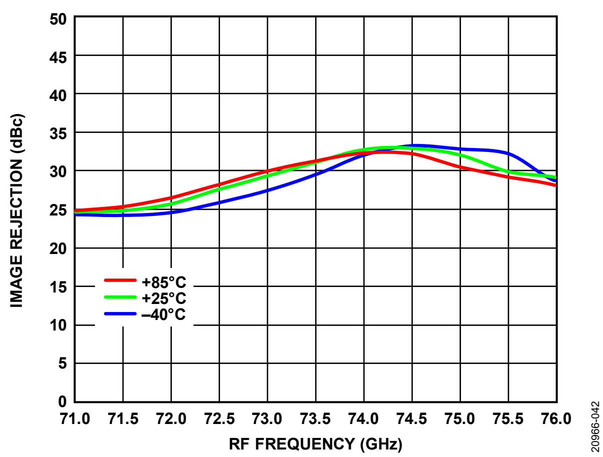


Figure 40. Image Rejection vs. RF Frequency over Temperature

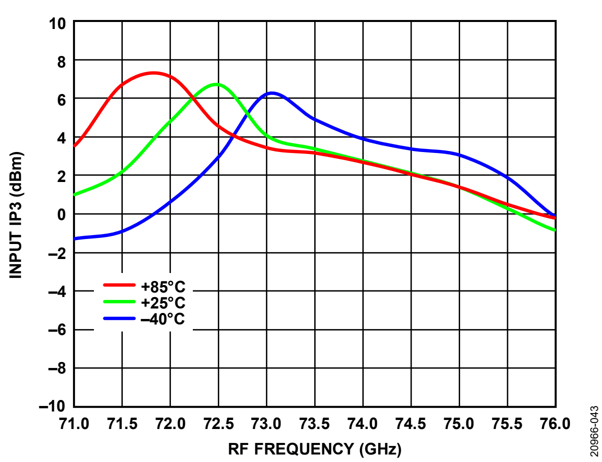


Figure 41. Input IP3 vs. RF Frequency over Temperature

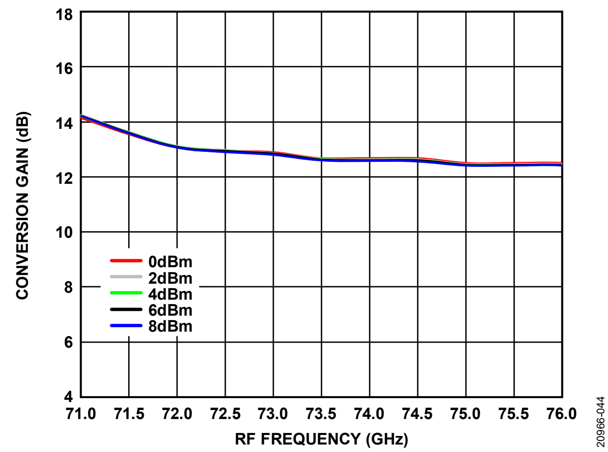


Figure 42. Conversion Gain vs. RF Frequency over LO Power

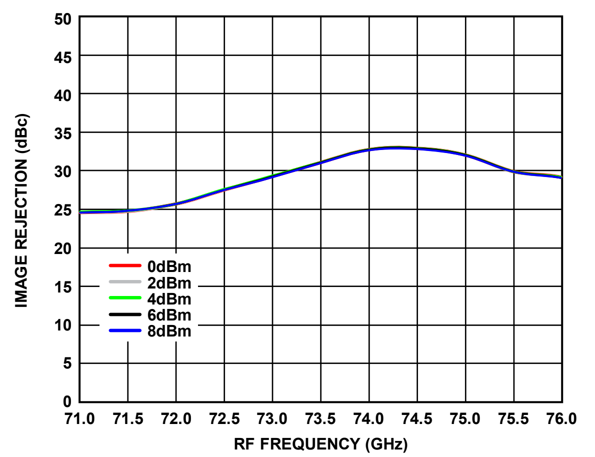


Figure 43. Image Rejection vs. RF Frequency over LO Power

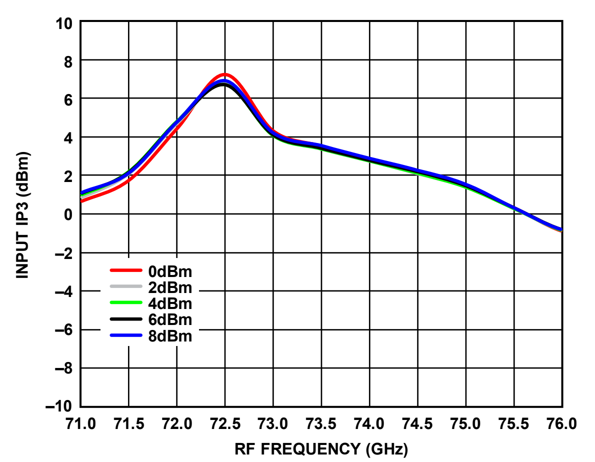


Figure 44. Input IP3 vs. RF Frequency over LO Power

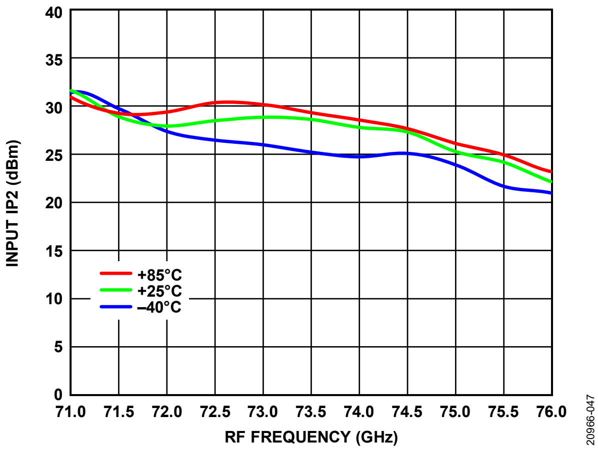


Figure 45. Input IP2 vs. RF Frequency over Temperature

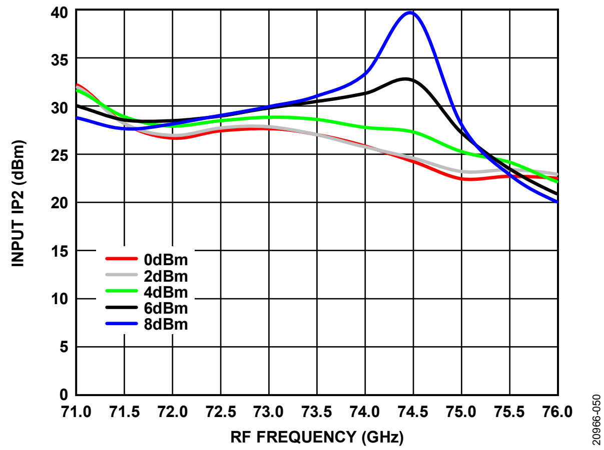


Figure 48. Input IP2 vs. RF Frequency over LO Power

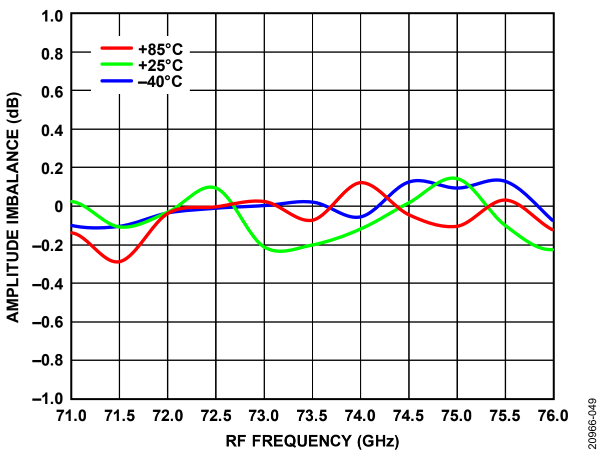


Figure 46. Amplitude Imbalance vs. RF Frequency over Temperature

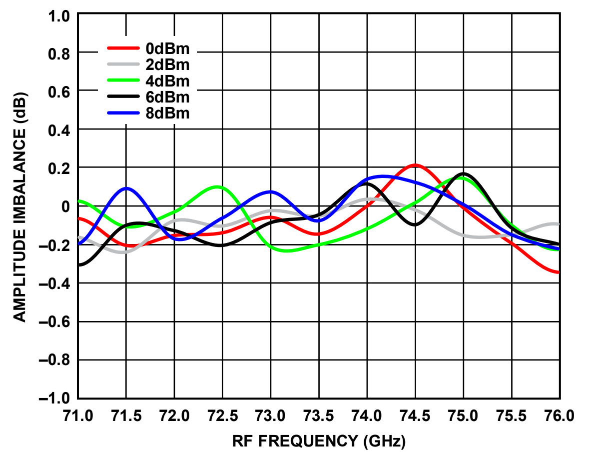


Figure 49. Amplitude Imbalance vs. RF Frequency over LO Power

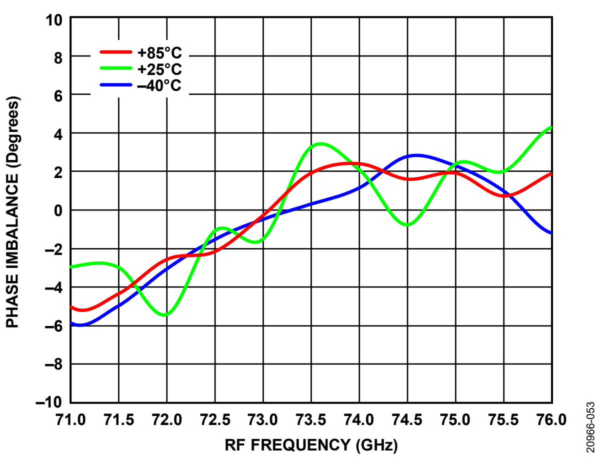


Figure 47. Phase Imbalance vs. RF Frequency over Temperature

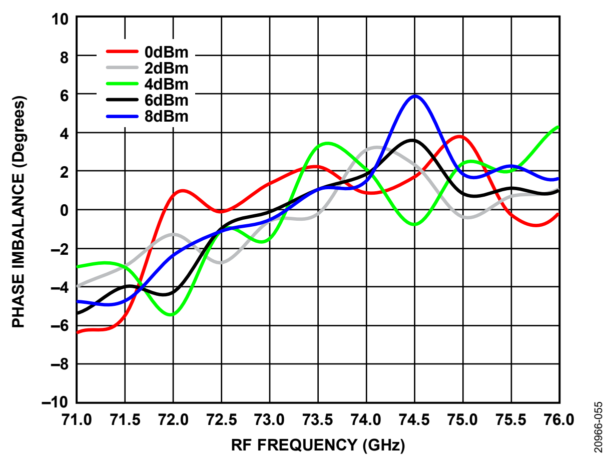


Figure 50. Phase Imbalance vs. RF Frequency over LO Power

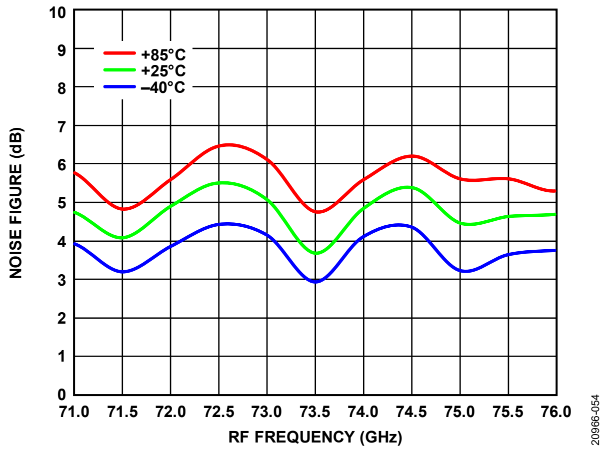


Figure 51. Noise Figure vs. RF Frequency over Temperature

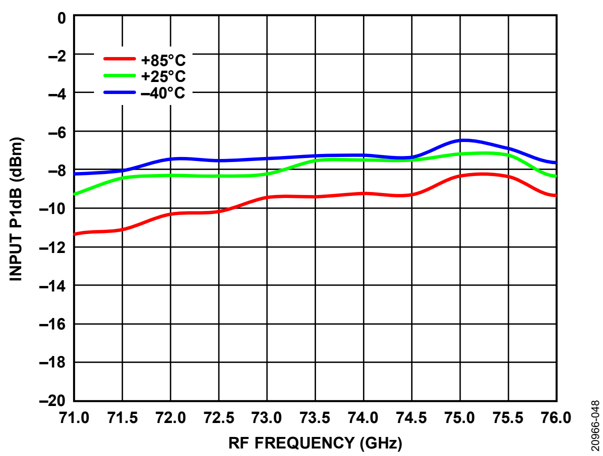


Figure 52. Input P1dB vs. RF Frequency over Temperature

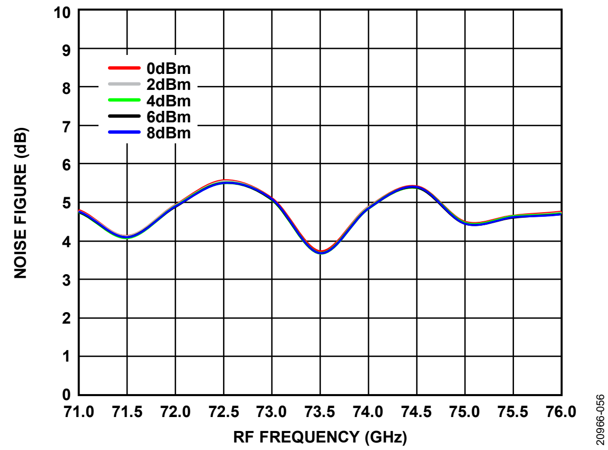


Figure 53. Noise Figure vs. RF Frequency over LO Power

T_A = 25°C, IF = 2 GHz, RFIN = −20 dBm combined, LO power = +4 dBm, and lower sideband selected, unless otherwise noted.

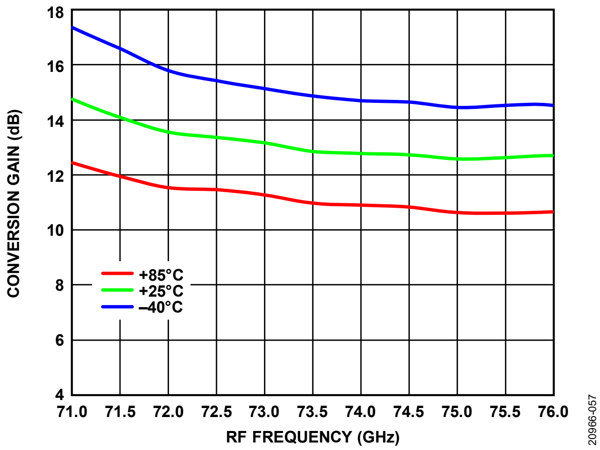


Figure 54. Conversion Gain vs. RF Frequency over Temperature

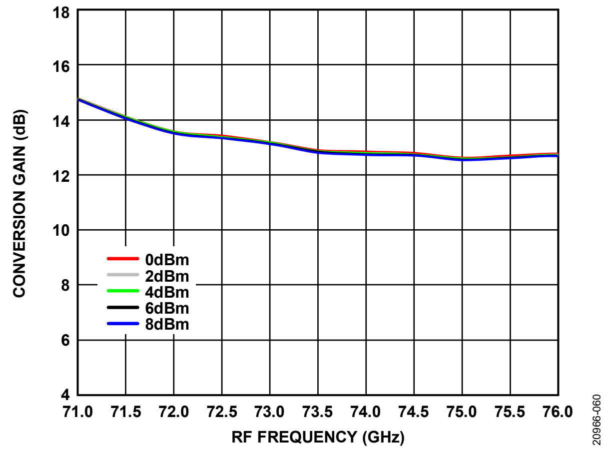


Figure 57. Conversion Gain vs. RF Frequency over LO Power

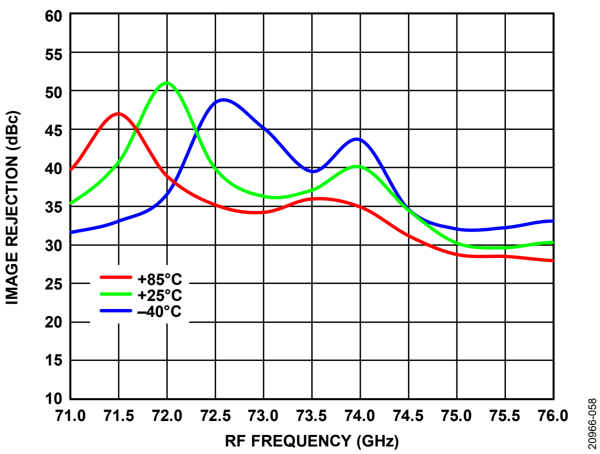


Figure 55. Image Rejection vs. RF Frequency over Temperature

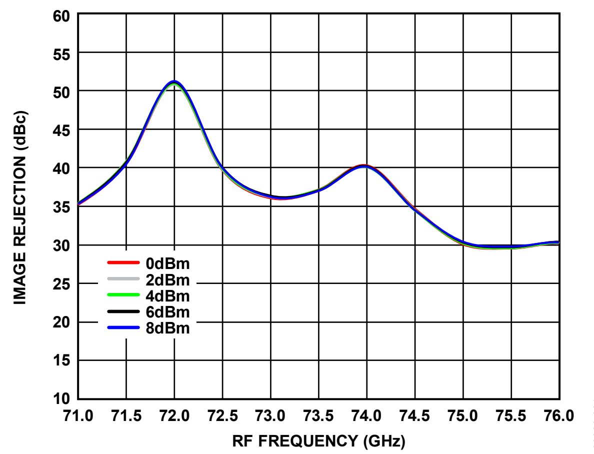


Figure 58. Image Rejection vs. RF Frequency over LO Power

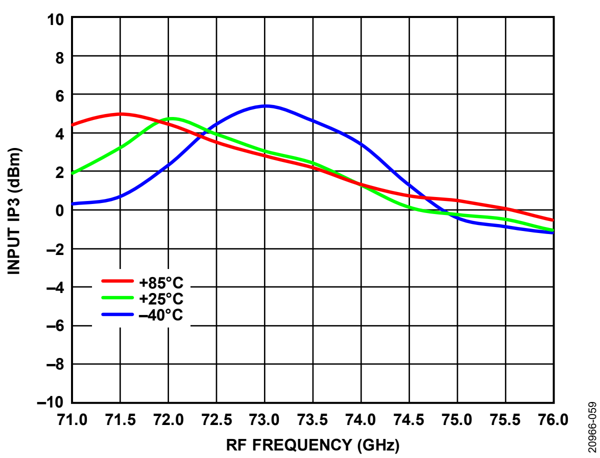


Figure 56. Input IP3 vs. RF Frequency over Temperature

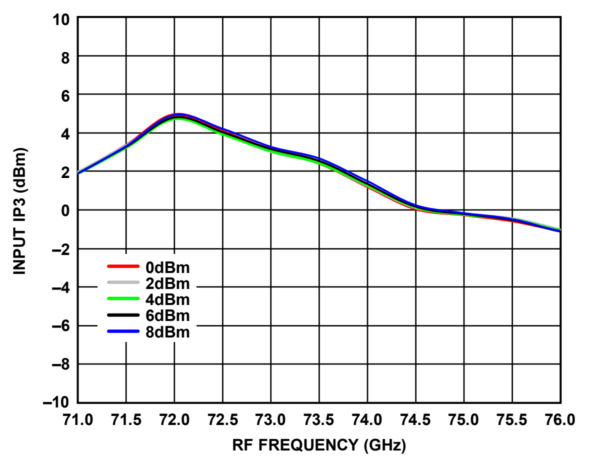


Figure 59. Input IP3 vs. RF Frequency over LO Power

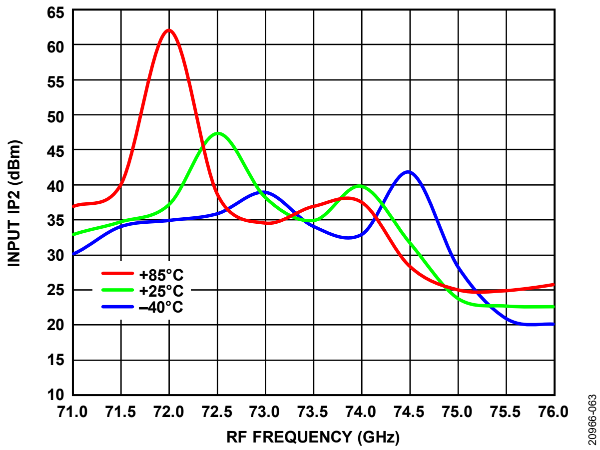


Figure 60. Input IP2 vs. RF Frequency over Temperature

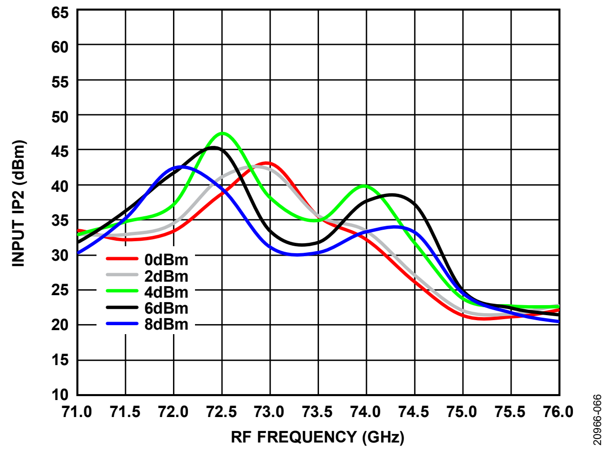


Figure 63. Input IP2 vs. RF Frequency over LO Power

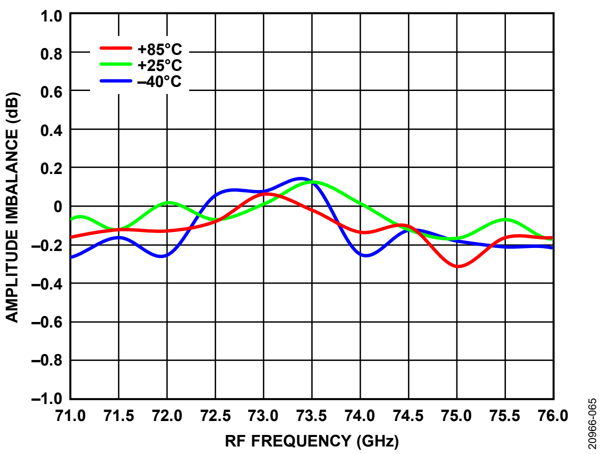


Figure 61. Amplitude Imbalance vs. RF Frequency over Temperature

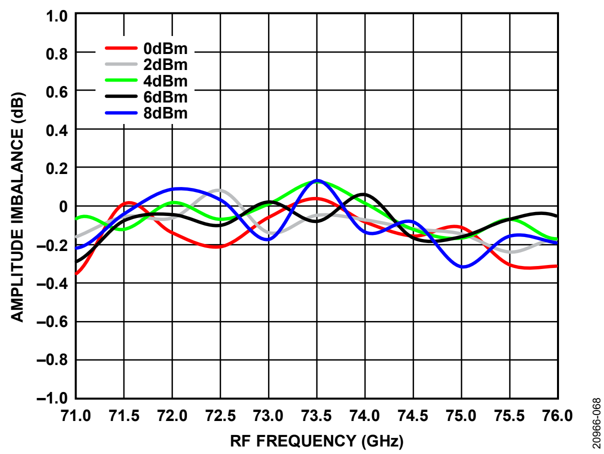


Figure 64. Amplitude Imbalance vs. RF Frequency over LO Power

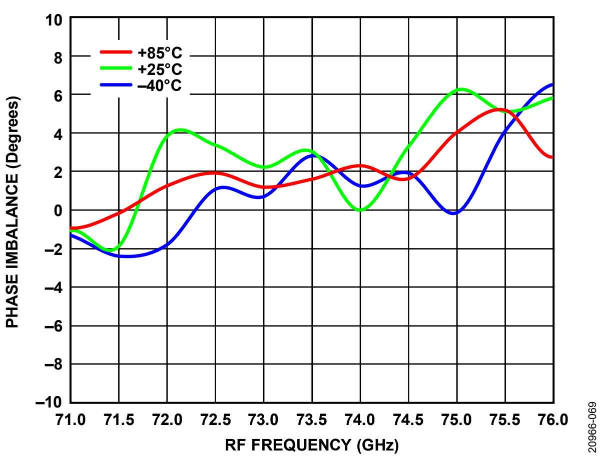


Figure 62. Phase Imbalance vs. RF Frequency over Temperature

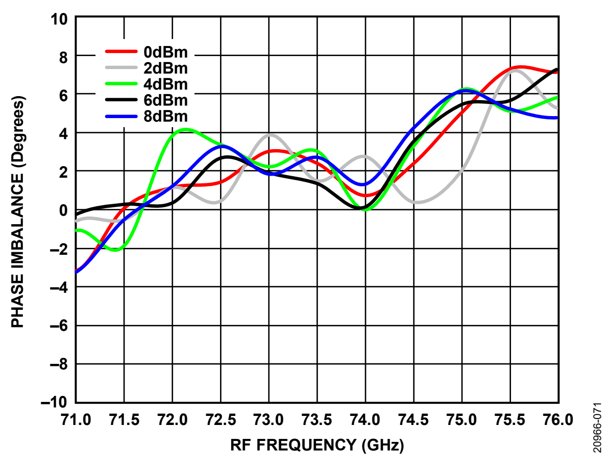


Figure 65. Phase Imbalance vs. RF Frequency over LO Power

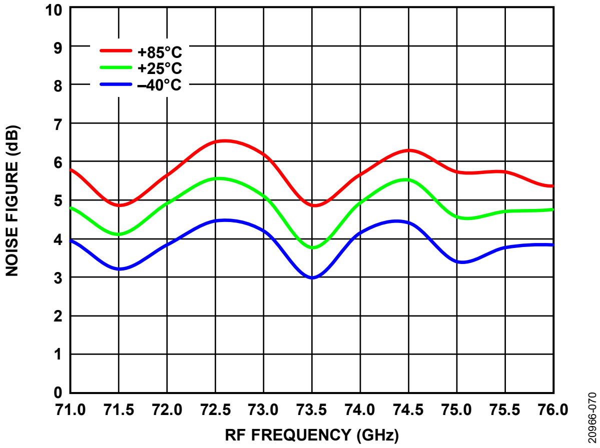


Figure 66. Noise Figure vs. RF Frequency over Temperature

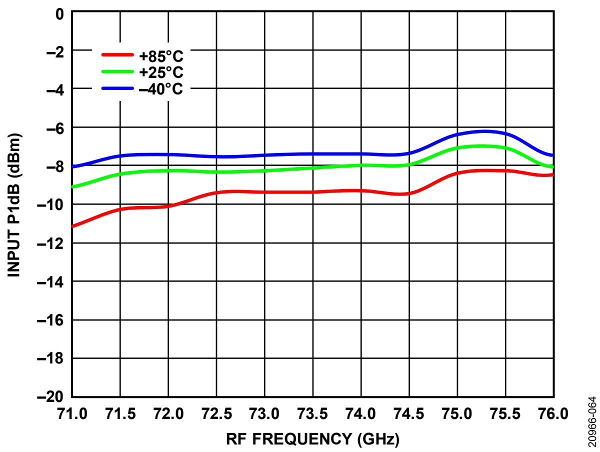


Figure 67. Input P1dB vs. RF Frequency over Temperature

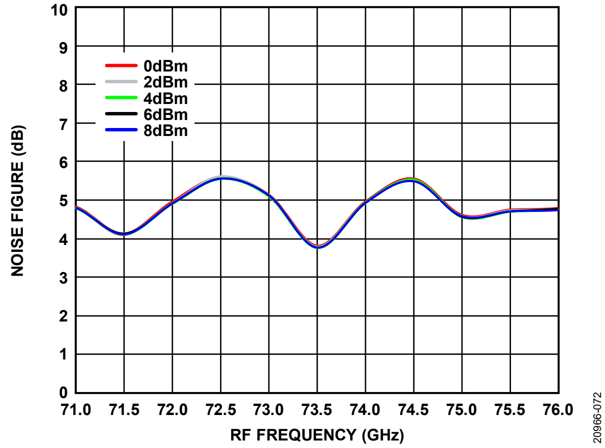


Figure 68. Noise Figure vs. RF Frequency over LO Power

RETURN LOSS AND 6× LO LEAKAGE

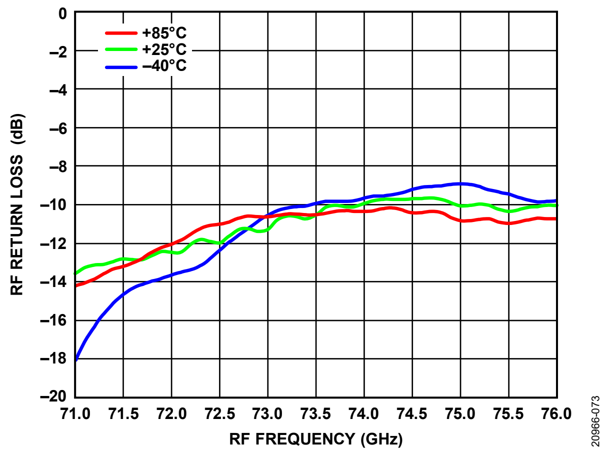


Figure 69. RF Return Loss vs. RF Frequency over Temperature LO Frequency = 11.8 GHz

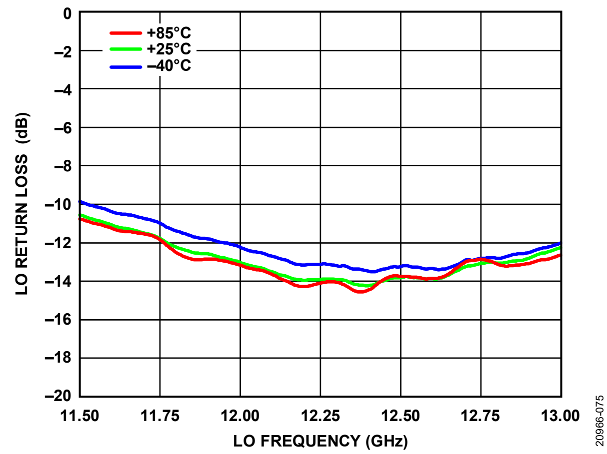


Figure 71. LO Return Loss vs. LO Frequency over Temperature

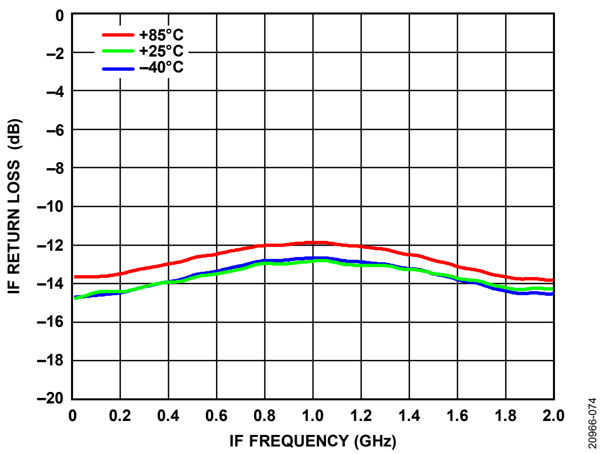


Figure 70. IF Return Loss vs. IF Frequency over Temperature LO Frequency = 11.8 GHz

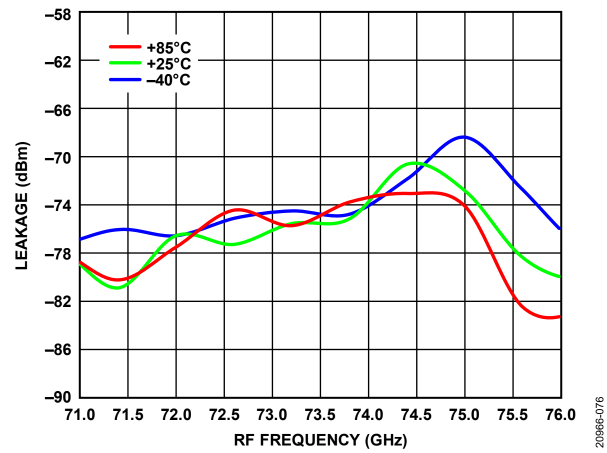


Figure 72. 6× LO Leakage at the RF Port over Temperature

SPURIOUS PERFORMANCE

T_A = 25°C, IF = 1 GHz, RFIN = −20 dBm, and LO input = +4 dBm, unless otherwise noted. Mixer spurious products are measured in dBc from the IF output power level single-ended for frequencies below 50 GHz, with all other IF ports terminated. Spur values are (M × RF) − (N × LO). N/A means not applicable.

M × N Spurious Outputs, RF = 71 GHz, LO = 12 GHz

		N × LO										
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**12**	**18**
M × RF	**0**	N/A	−35	−55	−56	−73	<−80	<−80	<−80	<−80	<−80	<−80
	1	<−80	<−80	−75	−66	−85	−34	0	−34	−67	<−80	<−80
	2	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	−74	−31	<−80
	3	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	−42
	4	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80
	5	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80

M × N Spurious Outputs, RF = 73.5 GHz, LO = 12.417 GHz

		N × LO										
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**12**	**18**
M × RF	**0**	N/A	−29	−84	−76	−69	<−80	<−80	<−80	<−80	<−80	<−80
	1	<−80	<−80	−73	−78	−82	−35	0	−37	−85	<−80	<−80
	2	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	−73	−34	<−80
	3	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	−96
	4	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80
	5	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80

M × N Spurious Outputs, RF = 76 GHz, LO = 12.833 GHz

		N × LO										
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**12**	**18**
M × RF	**0**	N/A	−34	−84	−74	<−80	<−80	<−80	<−80	<−80	<−80	<−80
	1	<−80	<−80	<−80	−74	−85	−91	0	−90	−83	<−80	<−80
	2	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	−65	−33	<−80
	3	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	−97
	4	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80
	5	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80	<−80

THEORY OF OPERATION

The ADMV7410 is a fully integrated SiP, I/Q low noise downconverter that consists of two functional blocks.

The RFIN port of the ADMV7410 is connected to the gallium arsenide (GaAs), low noise amplifier that consists of four stages of low noise amplification that feed into the second block.

The second block is a GaAs, I/Q downconverter with an integrated LO buffer and 6× multiplier. The 6× multiplier allows the use of a lower frequency range LO input signal, typically between 11.5 GHz and 13 GHz. The 6× multiplier is implemented using a cascade of 3× and 2× multipliers. The LO buffer amplifiers are included on chip to allow a typical LO drive level of 4 dBm for typical performance. The LO path feeds a quadrature splitter followed by on-chip baluns that drive the I and Q mixer cores. The mixer cores comprise singly balanced passive mixers. The RF input of the I and Q mixers are then driven through an on-chip Wilkinson power splitter, which is then fed by the first block of the ADMV7410.

APPLICATIONS INFORMATION

POWER-UP BIAS SEQUENCE

The ADMV7410 functional blocks use active multiple amplifier and multiplier stages that all use depletion mode pseudomorphic high electron mobility transistors (pHEMTs). To ensure transistor damage does not occur, use the following power-up bias sequence and do not apply RF power to the device on the LO or IF ports unless otherwise noted:

1. Apply a −2 V bias to VG_MULT, VG_AMP, VG12_LNA, and VG34_LNA.
2. Apply a −1 V bias to VG_MIXER.
3. Apply a 2 V bias to VD12_LNA.
4. Apply a 1.5 V bias to VD_MULT.
5. Apply a 4 V bias to VD_AMP and VD34_LNA.
6. Adjust VG_AMP between −2 V and 0 V to achieve a total I_{VD_AMP} current of 175 mA.
7. Adjust VG12_LNA between −2 V and 0 V to achieve a total I_{VD12_LNA} current of 22 mA.
8. Adjust VG34_LNA between −2 V and 0 V to achieve a total I_{VD34_LNA} current of 44 mA.
9. Apply a LO input signal on the LO port and adjust VG_MULT between −2 V and 0 V to achieve a total I_{VD_MULT} current of 80 mA.

POWER-DOWN SEQUENCE

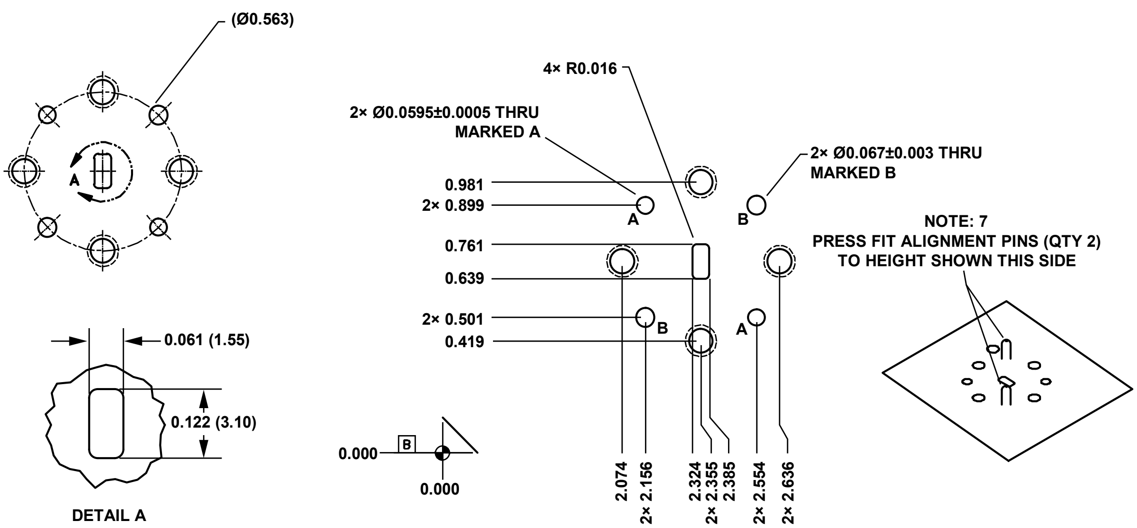
To power down the ADMV7410, take the following steps:

1. Apply a 0 V bias to VD_MULT, VD_AMP, VD12_LNA, and VD34_LNA.
2. Apply a 0 V bias to VG_MIXER.
3. Apply a 0 V bias to VG_MULT, VG_AMP, VG12_LNA, and VG34_LNA.

LAYOUT

Solder the exposed pad on the underside of the ADMV7410 to a low thermal and electrical impedance ground plane. This pad is typically soldered to an exposed opening in the solder mask. Connect these ground vias to all other ground layers to maximize heat dissipation from the device package.

Figure 73 illustrates the recommended mechanical layout on the interface plate used to interface to the WR-12 waveguide opening of the ADMV7410. The recommended PCB land pattern footprint is shown in Figure 74.

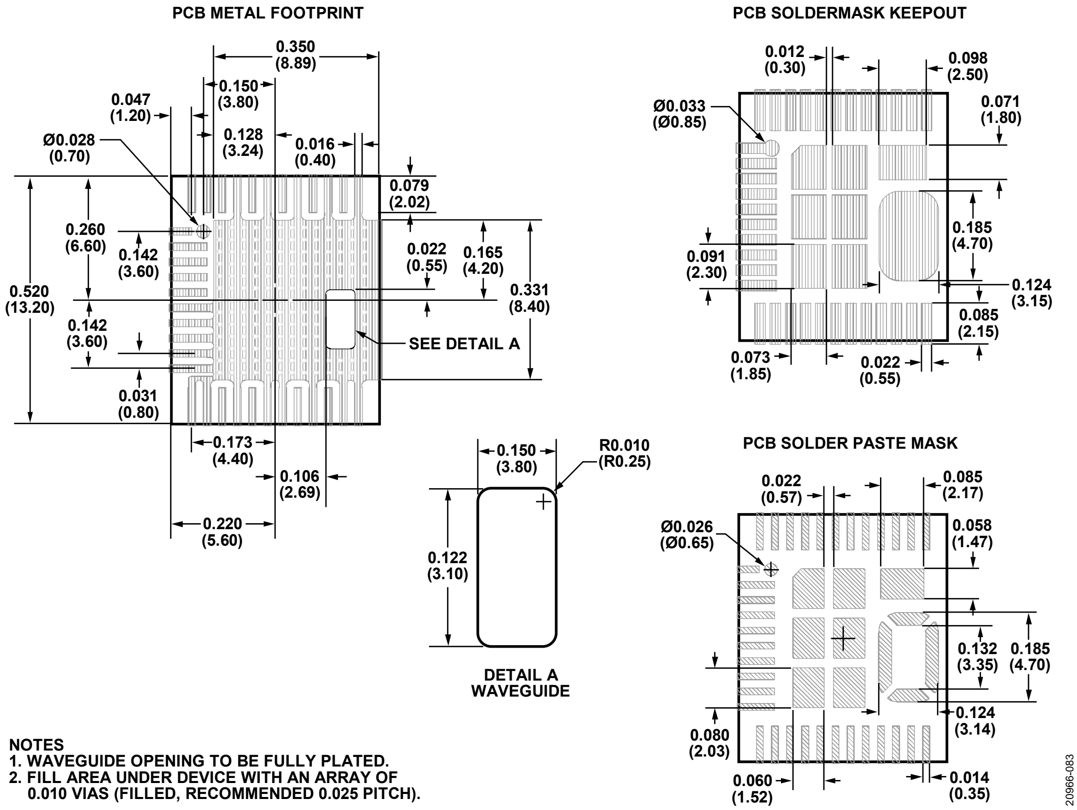


PART LIST				
ITEM	QTY	VENDOR	STOCK NUMBER	DESCRIPTION
1	2	VARIOUS	VARIOUS	PIN, ALIGNMENT, FLANGE, 0.0615 DIA

NOTES:
1. REMOVE BURRS AND BREAK SHARP EDGES.
2. ALL INTERNAL RADII ARE .090 UNLESS OTHERWISE NOTED.
3. SURFACE FINISH 32 RMS UNLESS OTHERWISE SPECIFIED.
4. DIMENSIONS APPLY AFTER PLATING.
5. MATERIAL: ALUMINUM 6061-T6 PER QQ-A-250/11.
6. FINISH: NONE.
7. INSTALL DOWEL PINS.
8. USE ELECTRONIC DATA FOR ALL GEOMETRY THAT IS NOT DIMENSIONED.

20966-082

Figure 73. Recommended Standard WR-12 Footprint



NOTES
1. WAVEGUIDE OPENING TO BE FULLY PLATED.
2. FILL AREA UNDER DEVICE WITH AN ARRAY OF 0.010 VIAS (FILLED, RECOMMENDED 0.025 PITCH).

Figure 74. PCB Land Pattern Footprint

TYPICAL APPLICATION CIRCUIT

Figure 75 shows the typical application circuit.

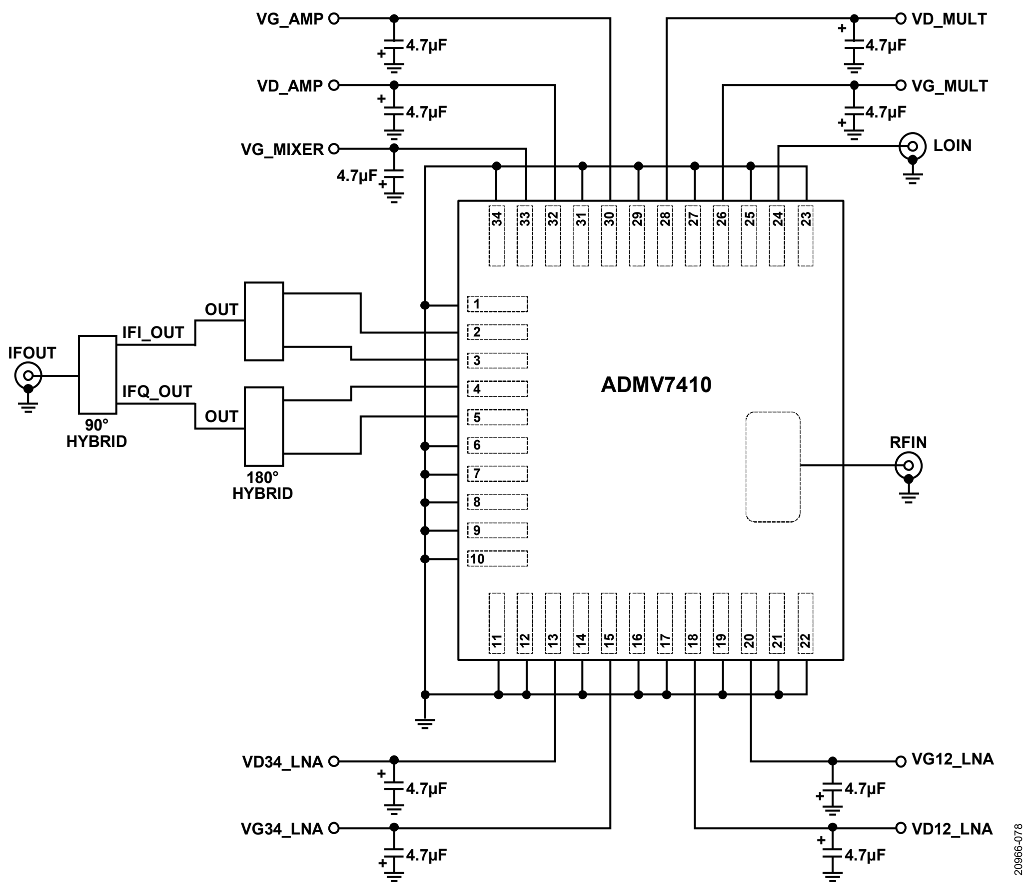


Figure 75. Typical Application Circuit

OUTLINE DIMENSIONS

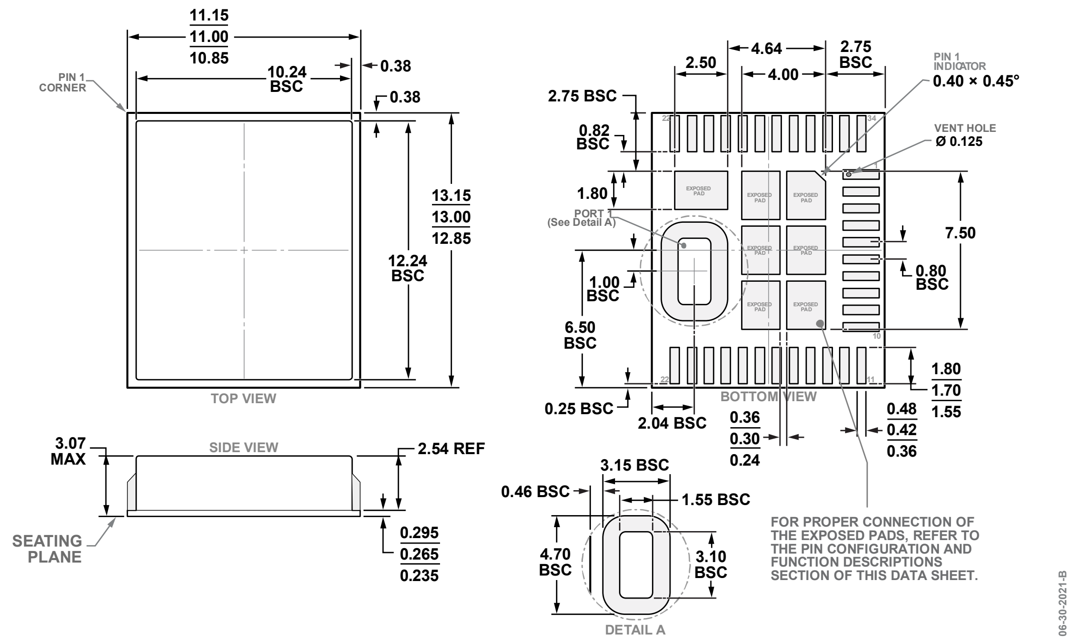


Figure 76. 34-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]
11.00 mm × 13.00 mm Body and 3.07 mm Maximum Package Height
(CE-34-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADMV7410BCEZ	−40°C to +85°C	34-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]	CE-34-2
ADMV7410-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.