WINSOURCE ELECTRONICS

THE DATASHEET OF

ADPA7005CHIP

GaAs, pHEMT, MMIC, 1 W Power Amplifier, 20 GHz to 44 GHz

FEATURES

- Output P1dB: 30.5 dBm typical at 22 GHz to 34 GHz
- P_{SAT}: 32 dBm typical at 22 GHz to 34 GHz
- Gain: 17 dB typical at 22 GHz to 34 GHz
- Output IP3: 41 dBm typical at 22 GHz to 34 GHz
- Supply voltage: 5 V at 1200 mA
- 50 Ω matched input/output
- Die size: 3.75 mm × 3.47 mm × 0.1 mm

APPLICATIONS

- Military and space
- Test instrumentation

FUNCTIONAL BLOCK DIAGRAM

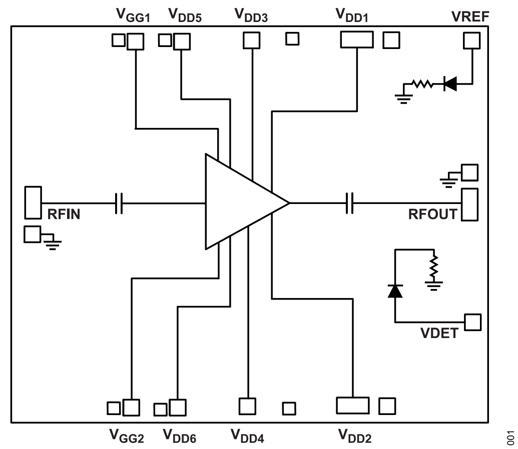

Figure 1.

GENERAL DESCRIPTION

The ADPA7005CHIP is a gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC), distributed power amplifier that operates from 20 GHz to 44 GHz. The amplifier provides 17 dB of small signal gain, 30.5 dBm output power for 1 dB compression (P1dB), and a typical output third-order intercept (IP3) of 41 dBm. The ADPA7005CHIP requires 1200 mA from a 5 V supply on the supply voltage (V_{DD}) and features inputs and outputs that are internally matched to 50 Ω, facilitating integration into multichip modules (MCMs). All data is taken with the chip connected via two 0.025 mm wire bonds that are at least 0.31 mm long.

TABLE OF CONTENTS

REVISION HISTORY

6/2023—Rev. 0 to Rev. A

2/2019—Revision 0: Initial Version

SPECIFICATIONS

20 GHZ TO 22 GHZ FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, and quiescent supply current (I_{DQ}) = 1200 mA for nominal operation, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		20		22	GHz	
GAIN			16.5		dB	
Gain Flatness			±0.7		dB	
Gain Variation Over Temperature			0.012		dB/°C	
NOISE FIGURE			9		dB	
RETURN LOSS						
Input			21		dB	
Output			24		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB		28.5		dBm	
Saturated Output Power	P_{SAT}		30		dBm	
Output Third-Order Intercept	IP3		38.5		dBm	Measurement taken at output power (P_{OUT}) per tone = 14 dBm
SUPPLY						
Current	I_{DQ}		1200		mA	Adjust the gate bias voltage (V_{GG1}) between −1.5 V up to 0 V to achieve the desired I_{DQ}
Voltage	V_{DD}	4	5		V	

22 GHZ TO 34 GHZ FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, and quiescent supply current (I_{DQ}) = 1200 mA for nominal operation, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		22		34	GHz	
GAIN		15	17		dB	
Gain Flatness			±0.6		dB	
Gain Variation Over Temperature			0.023		dB/°C	
NOISE FIGURE			7		dB	
RETURN LOSS						
Input			18		dB	
Output			20		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	28	30.5		dBm	
Saturated Output Power	P_{SAT}		32		dBm	
Output Third-Order Intercept	IP3		41		dBm	Measurement taken at output power (P_{OUT}) per tone = 14 dBm
SUPPLY						
Current	I_{DQ}		1200		mA	Adjust the gate bias voltage (V_{GG1}) between −1.5 V up to 0 V to achieve the desired I_{DQ}
Voltage	V_{DD}	4	5		V	

SPECIFICATIONS

34 GHZ TO 44 GHZ FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, and I_{DQ} = 1200 mA for nominal operation, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		34		44	GHz	
GAIN		11.5	14.5		dB	
Gain Flatness			±0.7		dB	
Gain Variation Over Temperature			0.024		dB/°C	
NOISE FIGURE			6		dB	
RETURN LOSS						
Input			15		dB	
Output			17		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	27	30		dBm	
Saturated Output Power	P_{SAT}		31		dBm	
Output Third-Order Intercept	IP3		40.5		dBm	Measurement taken at P_{OUT} per tone = 14 dBm
SUPPLY						
Current	I_{DQ}		1200		mA	Adjust V_{GG1} between −1.5 V up to 0 V to achieve the desired I_{DQ}
Voltage	V_{DD}	4	5		V	

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Drain Bias Voltage (V_{DDx})	6.0 V
V_{GG1}	−1.5 to 0 V
Radio Frequency Input Power (RFIN)	27 dBm
Continuous Power Dissipation (P_{DISS}), T = 85°C (Derate 149.2 mW/°C Above 85°C)	13.4 W
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +85°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	Class 1A (passed 250 V)

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to the carrier or substrate on which the die is mounted. Careful attention is needed with each material used in the thermal path below the IC. θ_{JC} is the channel to case thermal resistance, channel to bottom of die using die attach epoxy.

Table 5. Thermal Resistance

Package Type	θ_{JC}	Unit
C-12-3	6.7	°C/W

Table 6. Reliability Information

Parameter	Temperature (°C)
Maximum Channel Temperature	175°C
Nominal Channel Temperature (T = 85°C, V_{DD} = 5 V, I_{DQ} = 1200 mA)	125.2°C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

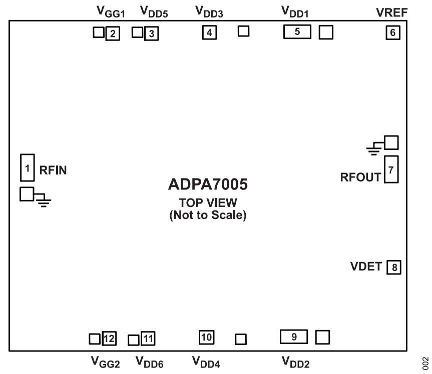

Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RFIN	RF Signal Input. This pad is ac-coupled and matched to 50 Ω.
2, 12	V_{GG1}, V_{GG2}	Amplifier Gate Control. External bypass capacitors of 4.7 µF, 0.01 µF, and 100 pF are required. ESD protection diodes are included and turn on below −1.5 V.
3, 4, 5, 9, 10, 11	V_{DD5}, V_{DD3}, V_{DD1}, V_{DD2}, V_{DD4}, V_{DD6}	Drain Bias for the amplifier. External bypass capacitors of 4.7 µF, 0.01 µF, and 100 pF are required.
6	VREF	Reference Diode. Use this pin in combination with VDET. The voltage provides temperature compensation to the VDET RF output power measurements.
7	RFOUT	RF Signal Output. This pad is ac-coupled and matched to 50 Ω.
8	VDET	Detector Diode Used for Measuring the RF Output Power. Detection via this pin requires the application of a dc bias voltage through an external series resistor. Used in combination with VREF, the difference voltage, VREF − VDET, is a temperature compensated dc voltage proportional to the RF output power.
Die Bottom	GND	Ground. The pads and die bottom must be connected to RF and dc ground.

INTERFACE SCHEMATICS

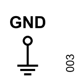

Figure 3. GND Interface Schematic

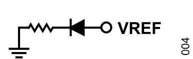

Figure 4. VREF Interface Schematic

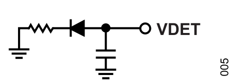

Figure 5. VDET Interface Schematic

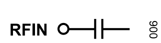

Figure 6. RFIN Interface Schematic

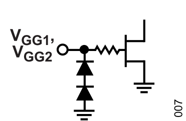

Figure 7. V_{GG1}, V_{GG2} Interface Schematic

Figure 8. RFOUT Interface Schematic

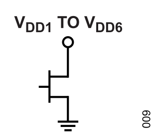

Figure 9. V_{DD1} to V_{DD6} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

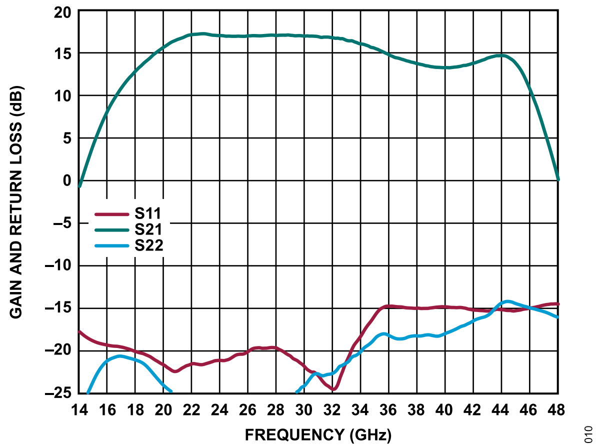

Figure 10. Gain and Return Loss vs. Frequency, V_{DD} = 5 V, I_{DQ} = 1200 mA

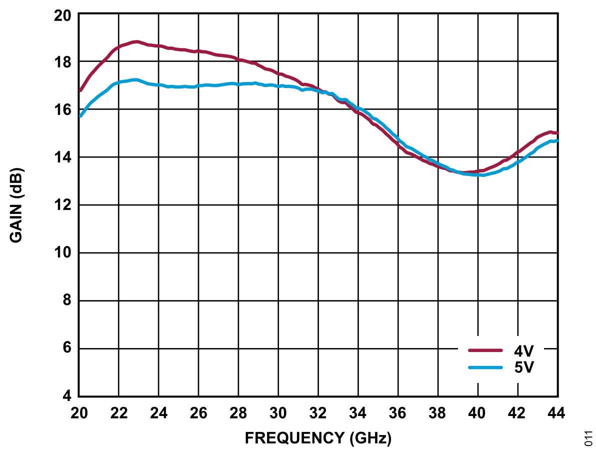

Figure 11. Gain vs. Frequency for Various V_{DD}, I_{DQ} = 1200 mA

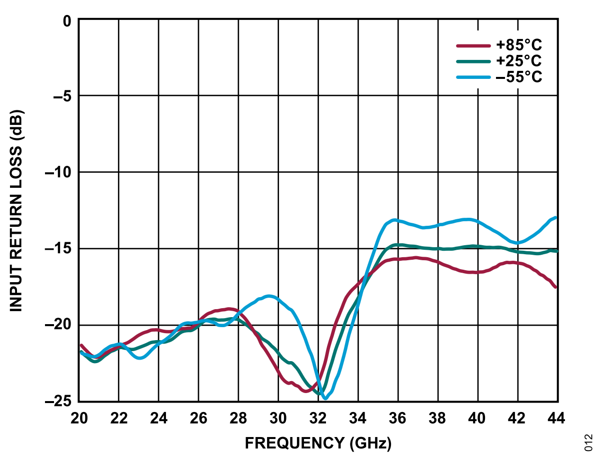

Figure 12. Input Return Loss vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1200 mA

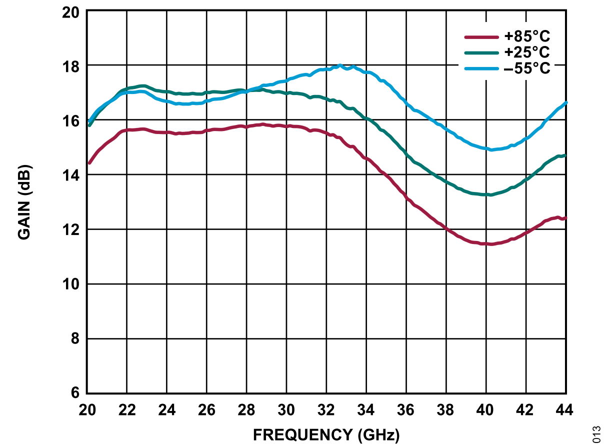

Figure 13. Gain vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1200 mA

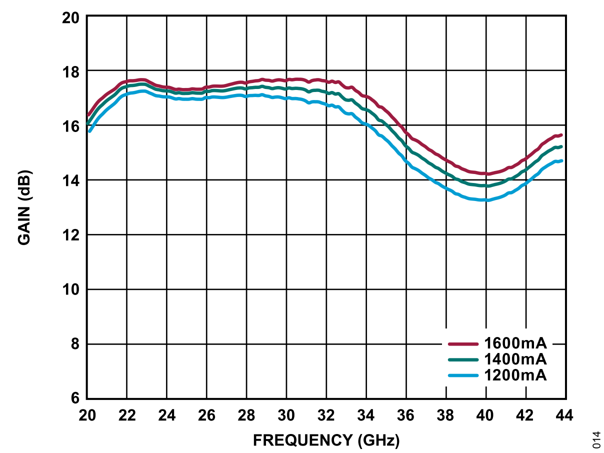

Figure 14. Gain vs. Frequency for Various I_{DQ}, V_{DD} = 5 V

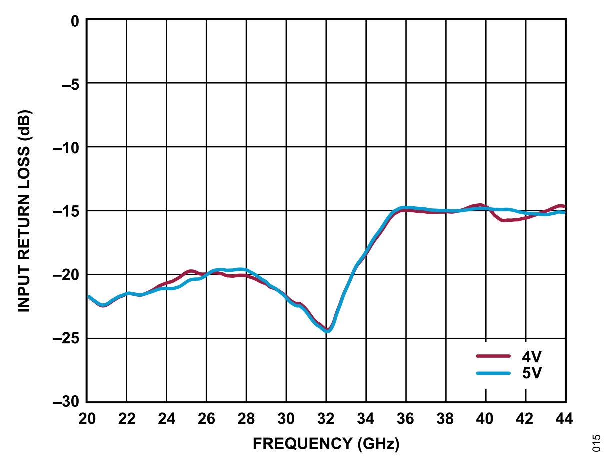

Figure 15. Input Return Loss vs. Frequency for Various V_{DD}, I_{DQ} = 1200 mA

TYPICAL PERFORMANCE CHARACTERISTICS

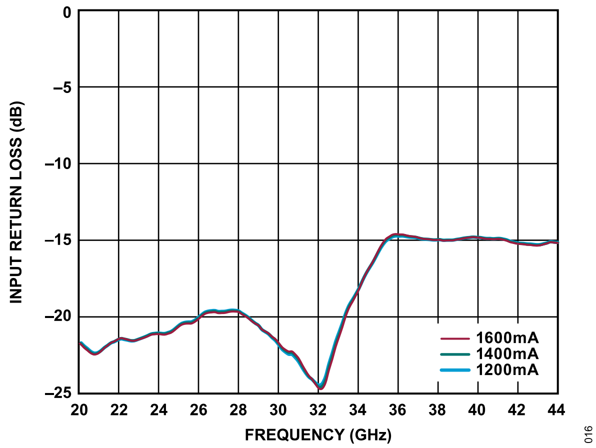

Figure 16. Input Return Loss vs. Frequency for Various I_{DQ}, V_{DD} = 5 V

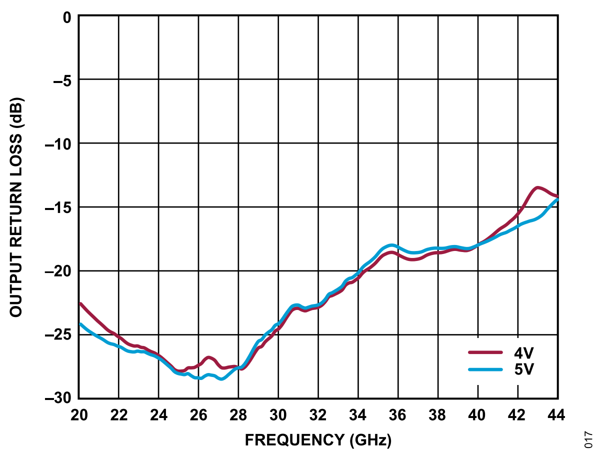

Figure 17. Output Return Loss vs. Frequency for Various V_{DD}, I_{DQ} = 1200 mA

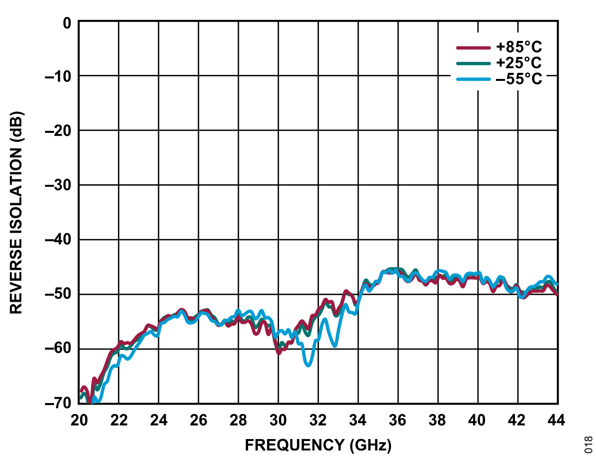

Figure 18. Reverse Isolation vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1200 mA

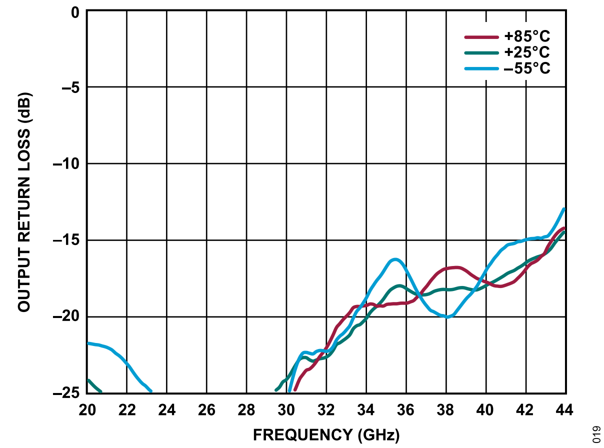

Figure 19. Output Return Loss vs. Frequency for Various Temperature, V_{DD} = 5 V, I_{DQ} = 1200 mA

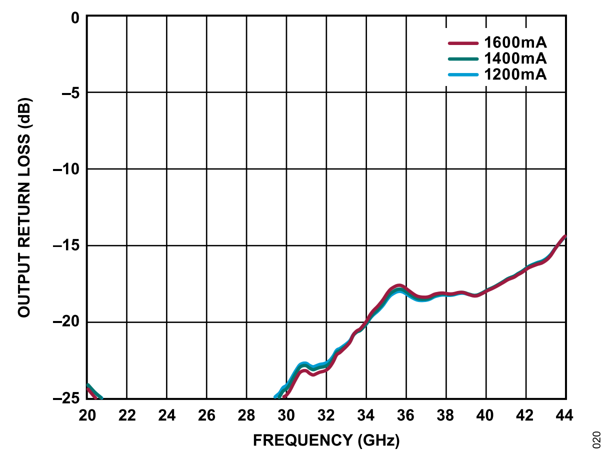

Figure 20. Output Return Loss vs. Frequency for Various I_{DQ}, V_{DD} = 5 V

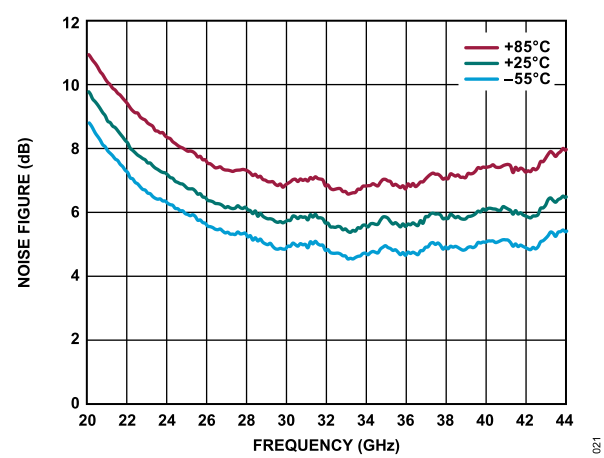

Figure 21. Noise Figure vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1200 mA

TYPICAL PERFORMANCE CHARACTERISTICS

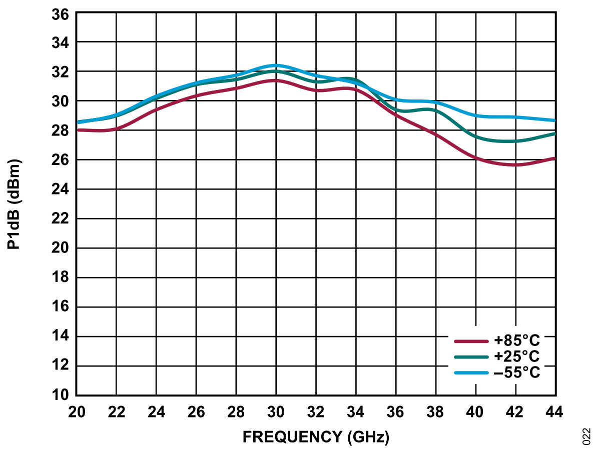

Figure 22. Output P1dB vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1200 mA

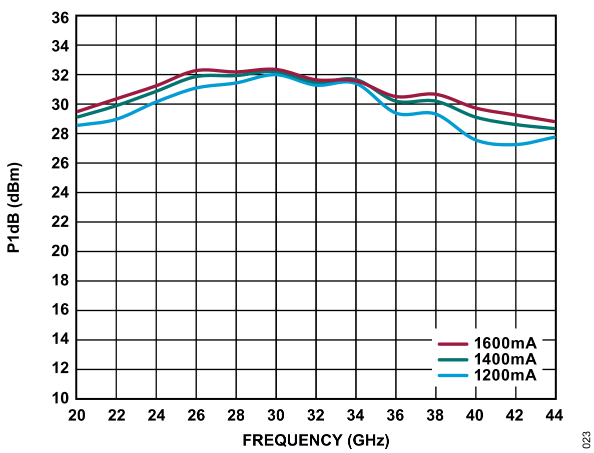

Figure 23. P1dB vs. Frequency for Various I_{DQ}, V_{DD} = 5 V

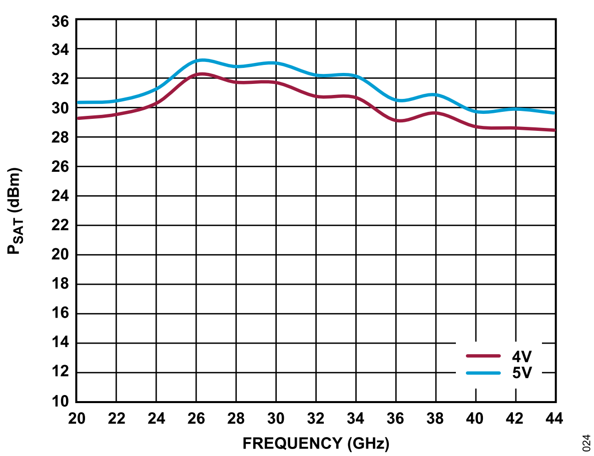

Figure 24. P_{SAT} vs. Frequency for Various V_{DD}, I_{DQ} = 1200 mA

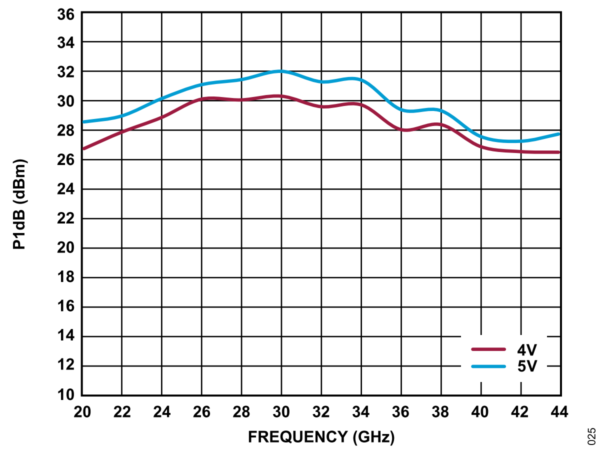

Figure 25. P1dB vs. Frequency for Various V_{DD}, I_{DQ} = 1200 mA

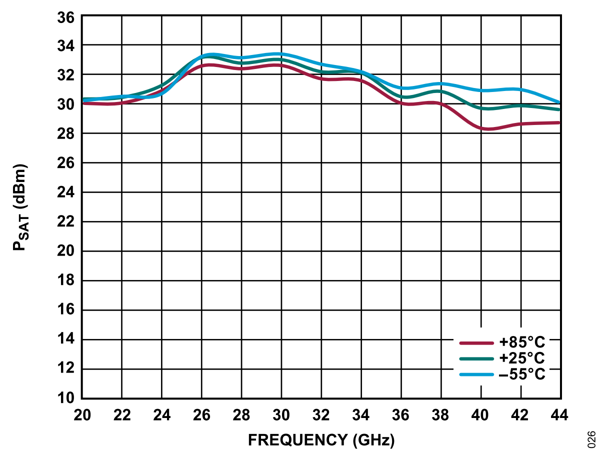

Figure 26. P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1200 mA

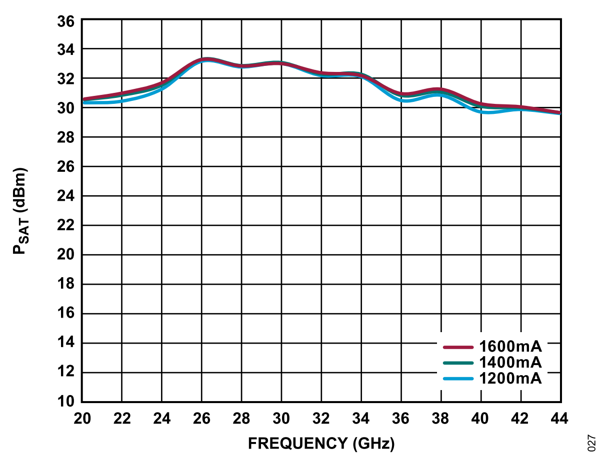

Figure 27. P_{SAT} vs. Frequency for Various I_{DQ}, V_{DD} = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

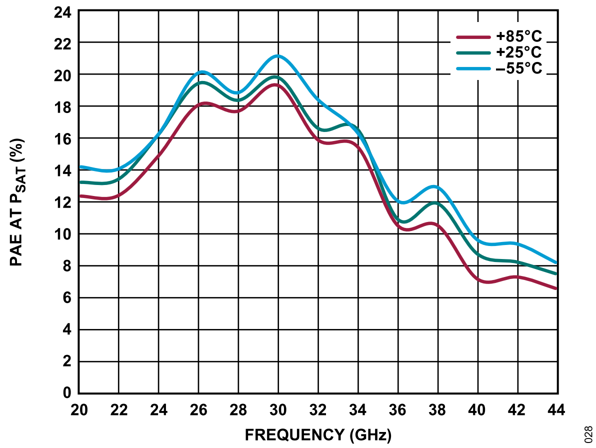

Figure 28. Power Added Efficiency (PAE) at P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1200 mA, PAE Measured at P_{SAT}

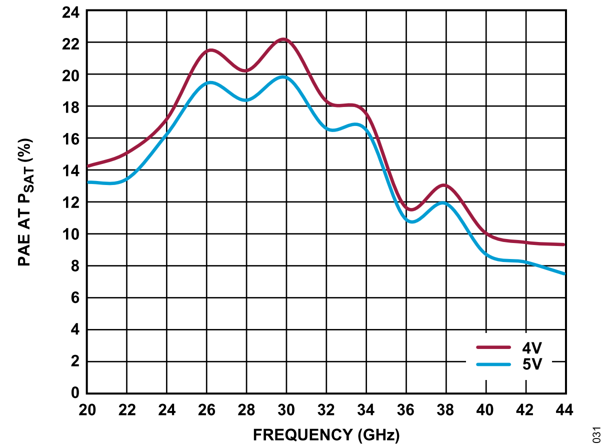

Figure 31. PAE at P_{SAT} vs. Frequency for Various V_{DD}, I_{DQ} = 1200 mA, PAE Measured at P_{SAT}

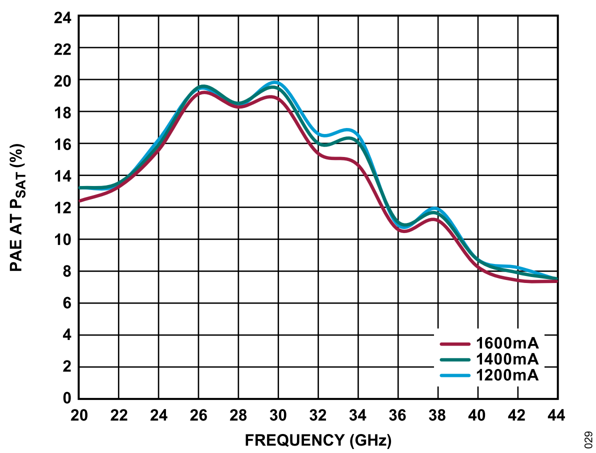

Figure 29. PAE at P_{SAT} vs. Frequency for Various I_{DQ}, V_{DD} = 5 V, I_{DQ} = 1200 mA, PAE Measured at P_{SAT}

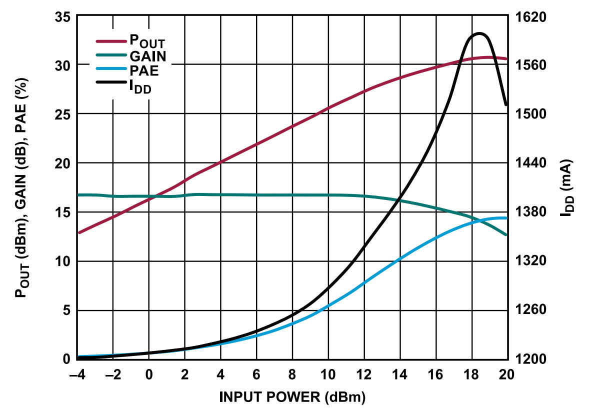

Figure 32. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 22 GHz, V_{DD} = 5 V, I_{DD} = 1200 mA

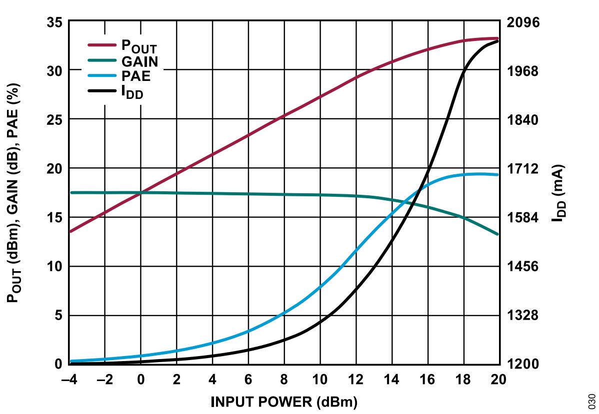

Figure 30. P_{OUT}, Gain, PAE, and Power PAE, Drain Current with RF Applied (I_{DD}) vs. Input Power, 26 GHz, V_{DD} = 5 V, I_{DD} = 1200 mA

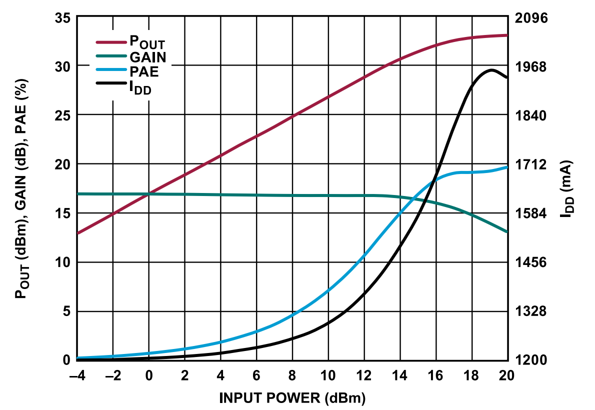

Figure 33. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 30 GHz, V_{DD} = 5 V, I_{DD} = 1200 mA

TYPICAL PERFORMANCE CHARACTERISTICS

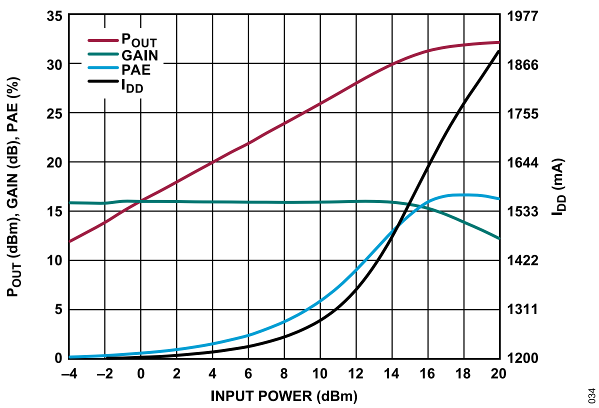

Figure 34. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 34 GHz, V_{DD} = 5 V, I_{DD} = 1200 mA

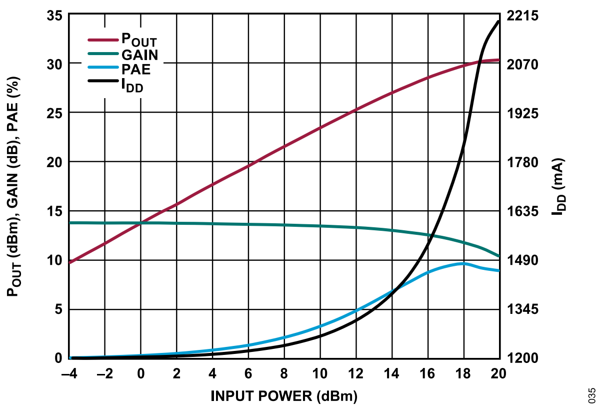

Figure 35. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 42 GHz, V_{DD} = 5 V, I_{DD} = 1200 mA

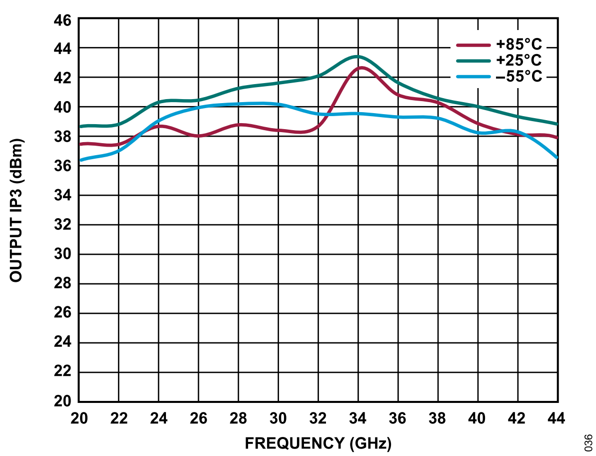

Figure 36. Output IP3 vs. Frequency for Various Temperatures, P_{OUT} per Tone = 14 dBm, V_{DD} = 5 V, I_{DQ} = 1200 mA

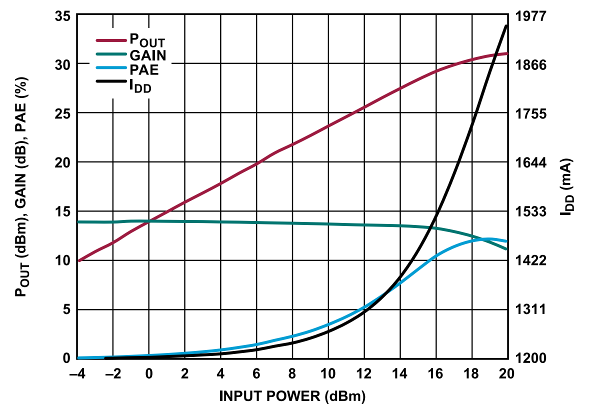

Figure 37. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 38 GHz, V_{DD} = 5 V, I_{DD} = 1200 mA

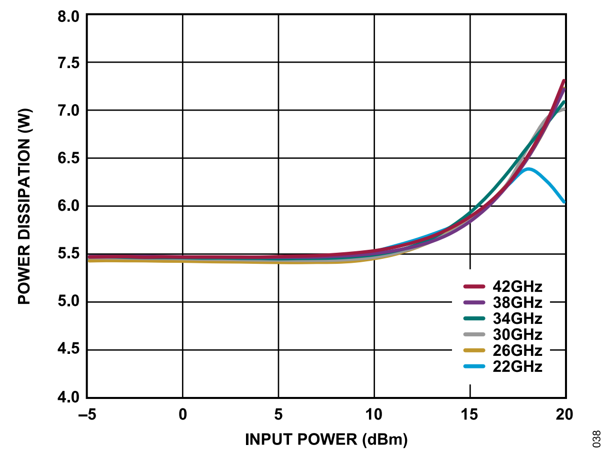

Figure 38. Power Dissipation vs. Input Power at T = 85°C, V_{DD} = 5 V, I_{DD} = 1200 mA

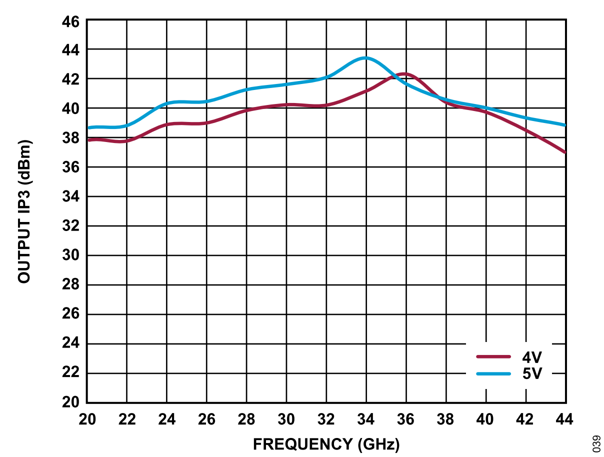

Figure 39. Output IP3 vs. Frequency for Various V_{DD}, P_{OUT} per Tone = 14 dBm, V_{DD} = 5 V, I_{DQ} = 1200 mA

TYPICAL PERFORMANCE CHARACTERISTICS

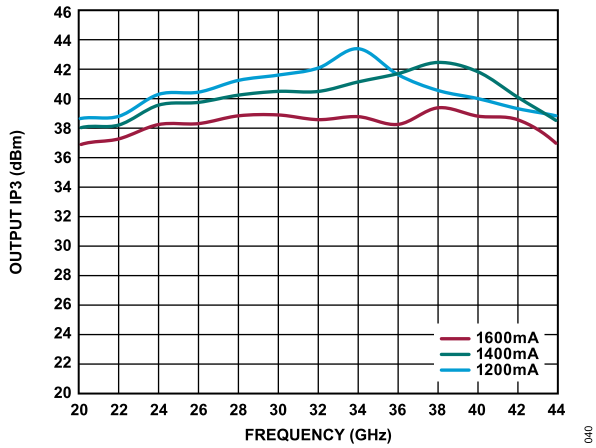

Figure 40. Output IP3 vs. Frequency for Various I_{DQ}, P_{OUT} per Tone = 14 dBm, V_{DD} = 5 V

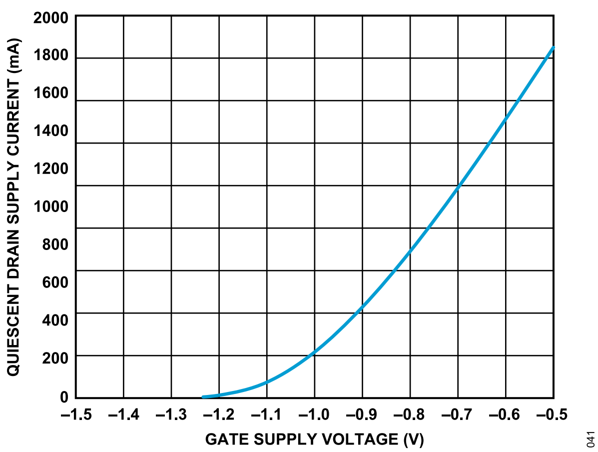

Figure 41. Quiescent Drain Supply Current vs. Gate Supply Voltage

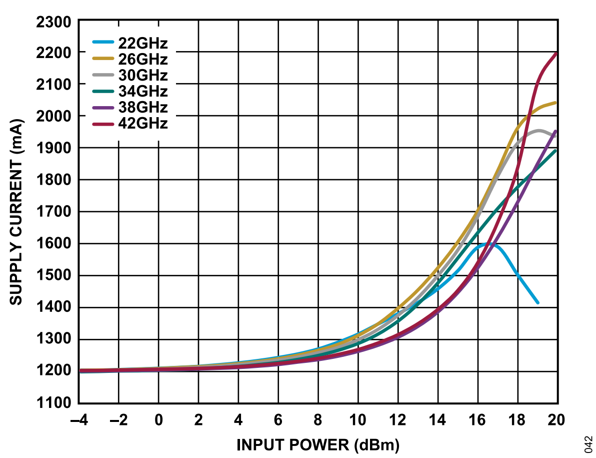

Figure 42. Supply Current I_{DD} vs. Input Power at Various Frequencies, V_{DD} = 5 V, I_{DD} = 1200 mA

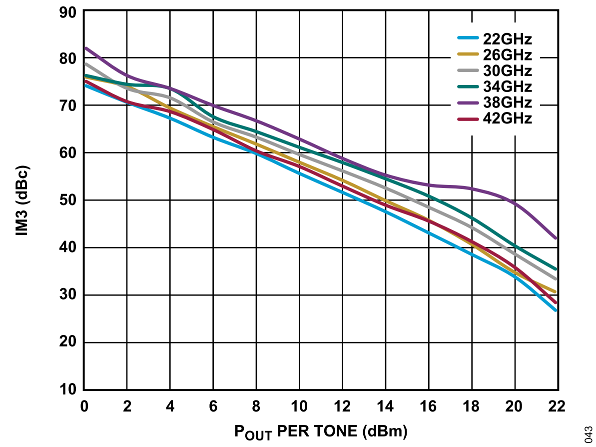

Figure 43. IM3 Distortion Relative to Carrier vs. P_{OUT} per Tone, V_{DD} = 5 V, I_{DQ} = 1200 mA

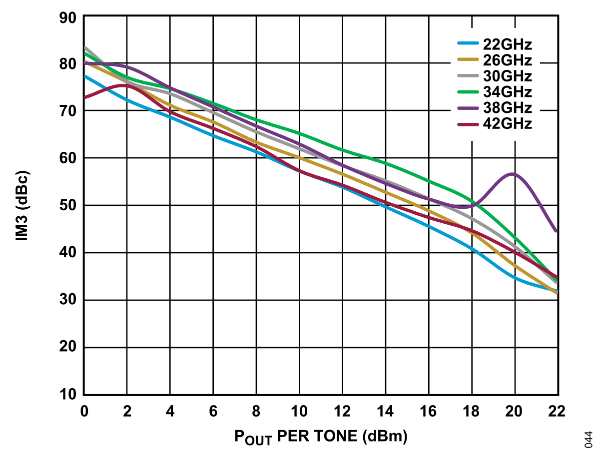

Figure 44. Third-Order Intermodulation (IM3) Distortion Relative to Carrier vs. P_{OUT} per Tone, V_{DD} = 4 V, I_{DQ} = 1200 mA

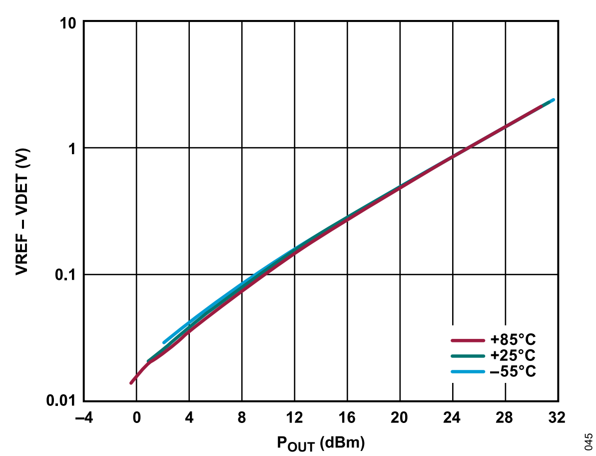

Figure 45. VREF – VDET vs. Output Power for Various Temperatures at 32 GHz

TYPICAL PERFORMANCE CHARACTERISTICS

CONSTANT I_{DD} OPERATION

Biased with HMC980LP4E active bias controller (see Figure 55), T_A = 25°C, V_{DD} = 5 V, and I_{DD} = 1600 mA for nominal operation, unless otherwise noted.

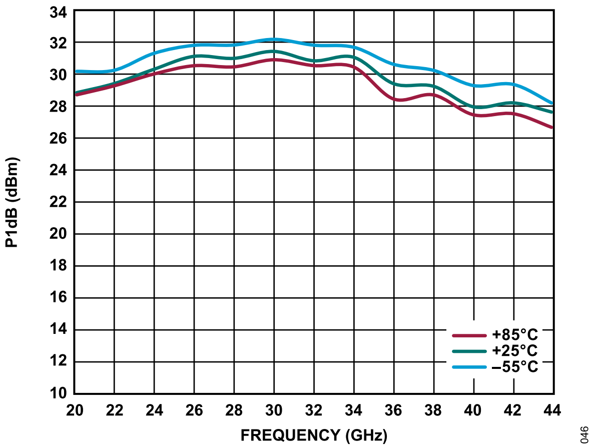

Figure 46. P1dB vs. Frequency for Various Temperatures, V_{DD} = 5 V, Data Measured with Constant I_{DD}

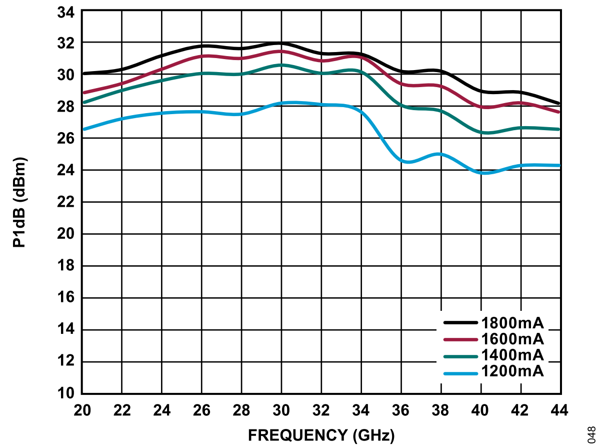

Figure 48. P1dB vs. Frequency for Various Drain Currents, V_{DD} = 5 V, Data Measured with Constant I_{DD}

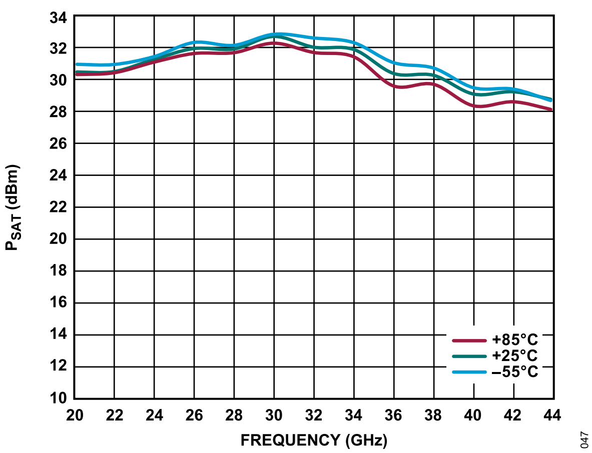

Figure 47. P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 5 V, Data Measured with Constant I_{DD}

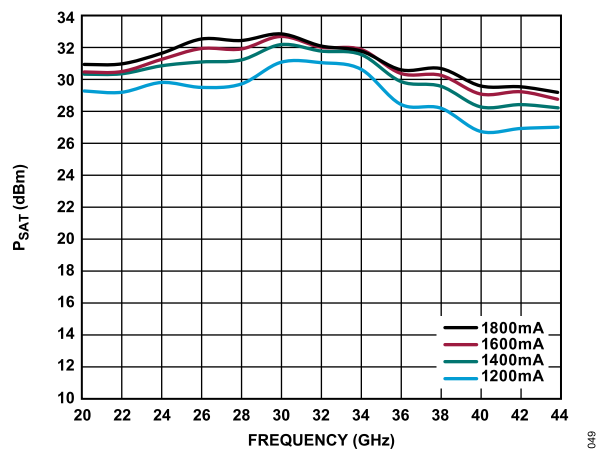

Figure 49. P_{SAT} vs. Frequency for Various Drain Currents, V_{DD} = 5 V, Data Measured with Constant I_{DD}

THEORY OF OPERATION

The architecture of the ADPA7005CHIP, a medium power amplifier, is shown in Figure 50. The ADPA7005CHIP uses two cascaded, three stage amplifiers operating in quadrature between six 90° hybrids.

The input signal is divided evenly into two, and then each signal is divided into two again. Each of these new paths is amplified through three independent gain stages. The amplified signals are then combined at the output. This balanced amplifier approach forms an amplifier with a combined gain of 15 dB and a P_{SAT} value of 32 dBm.

A portion of the RF output signal is directionally coupled to a diode for detection of the RF output power. When the diode is dc biased, the diode rectifies the RF power and makes the RF power available for measurement as a dc voltage at VDET. To allow temperature compensation of VDET, an identical and symmetrically located circuit, minus the coupled RF power, is available via VREF. Taking the difference of VREF − VDET provides a temperature compensated signal that is proportional to the RF output (see Figure 50).

The 90° hybrids ensure that the input and output return losses are greater than 15 dB. See the application circuits shown in Figure 63 and Figure 64 for further details on biasing the various blocks.

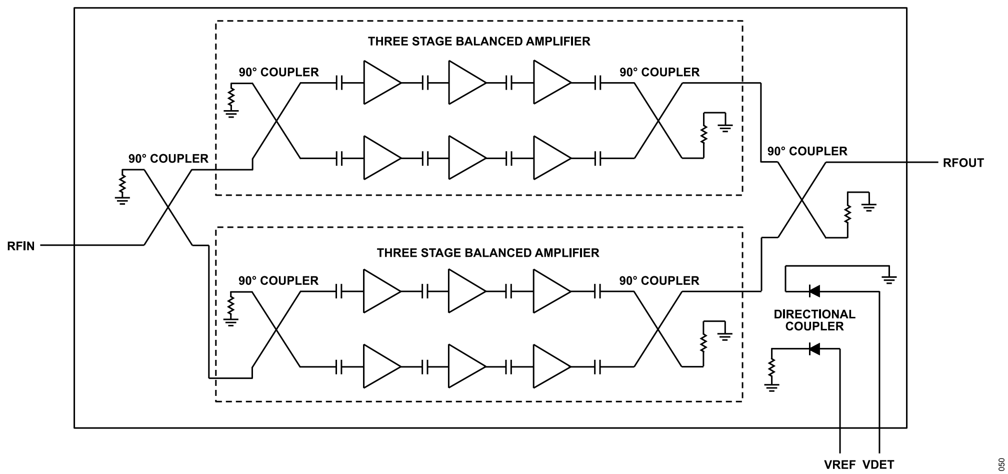

Figure 50. ADPA7005CHIP Architecture

APPLICATIONS INFORMATION

The ADPA7005CHIP is a GaAs, pHEMT, MMIC power amplifier. Capacitive bypassing is required for all V_{GGx} and V_{DDx} pins (see Figure 51). V_{GG1} is the gate bias pad for the top cascaded amplifiers. V_{GG2} is the gate bias pad for the bottom cascaded amplifiers. V_{DD1}, V_{DD3}, and V_{DD5} are drain bias pads for the top cascaded amplifiers. V_{DD2}, V_{DD4}, and V_{DD6} are drain bias pads for the bottom cascaded amplifiers.

All measurements for this device were taken using the typical application circuit (see Figure 63) and were configured as shown in the assembly diagram (Figure 64).

The following is the recommended bias sequence during power-up:

1. Connect GND to RF and dc ground.
2. Set all gate bias voltages, V_{GG1} and V_{GG2}, to −2 V.
3. Set all drain bias voltages, $V_{DDxx,}$ to 5 V.
4. Increase the gate bias voltage to achieve the quiescent supply current and set $I_{DQ,}$ = 1200 mA.
5. Apply the RF signal.

The following is the recommended bias sequence during power-down:

1. Turn off the RF signal.
2. Decrease the gate bias voltages, V_{GG1} and V_{GG2}, to −2 V to achieve an I_{DQ} = 0 mA (approximately).
3. Decrease all drain bias voltages to 0 V.
4. Increase the V_{GG1} and V_{GG2} gate bias voltage to 0 V.

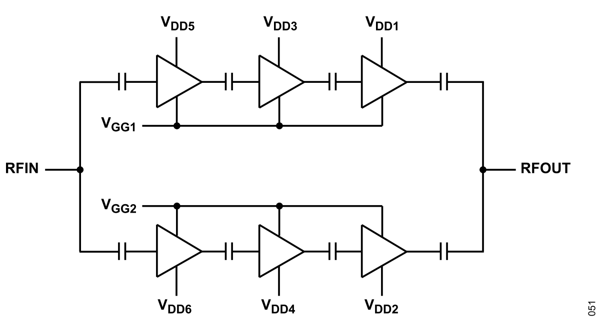

Figure 51. Simplified Block Diagram

Simplified bias pad connections to the dedicated gain stages and dependence and independence among pads are shown in Figure 51.

The V_{DD} = 5 V and I_{DD} = 1200 mA bias conditions are recommended to optimize overall performance. Unless otherwise noted, the data shown was taken using the recommended bias conditions. Operation of the ADPA7005CHIP at different bias conditions may provide performance that differs from what is shown in Figure 63 and Figure 64. Biasing the ADPA7005CHIP for higher drain current typically results in higher P1dB, output IP3, and gain at the expense of increased power consumption (see Table 8).

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GAAS MMICS

Attach the die directly to the ground plane with conductive epoxy (see the Handling Precautions section, the Mounting section, and the Wire Bonding section).

Microstrip, 50 Ω transmission lines on 0.127 mm thick alumina thin film substrates are recommended for bringing the RF to and from the chip. Raise the die 0.075 mm to ensure that the surface of the die is coplanar with the surface of the substrate.

Place the microstrip substrates as close to the die as possible to minimize ribbon bond length. Typical die to substrate spacing is 0.076 mm to 0.152 mm. To ensure wideband matching, a 15 fF capacitive stub is recommended on the PCB before the ribbon bond.

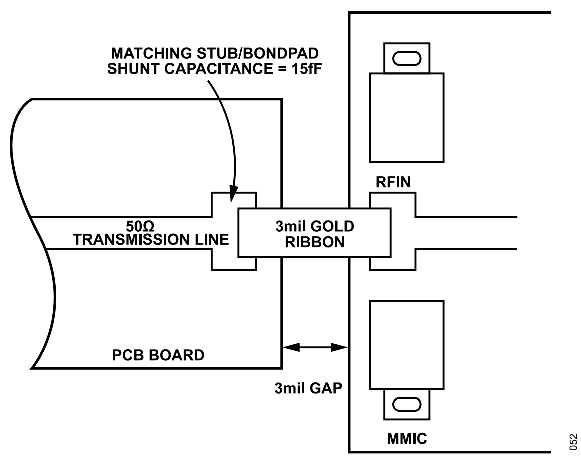

Figure 52. High Frequency Input Wideband Matching

Table 8. Power Selection Table

I_{DQ} (mA)[1, 2]	Gain (dB)	P1dB (dBm)	OIP3 (dBm)	P_{DISS} (W)	V_{GG} (V)
1200	17	32.0	42	6	−0.59
1400	17.4	32.3	40.2	7	−0.53
1600	17.7	32.5	38.4	8	−0.46

[1] Data taken at the following nominal bias conditions: V_{DD} = 5 V, T = 25°C.

[2] Adjust V_{GG1} and V_{GG2} from −2 V to 0 V to achieve the desired drain current.

APPLICATIONS INFORMATION

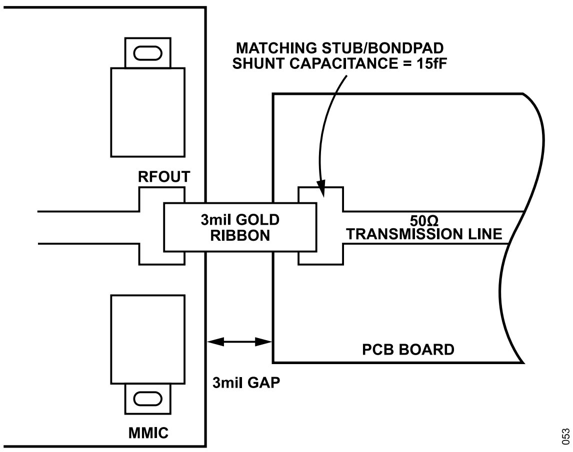

Figure 53. High Frequency Output Wideband Matching

Handling Precautions

To avoid permanent damage, follow these storage, cleanliness, static sensitivity, transient, and general handling precautions:

- Place all bare die in either waffle or gel-based ESD protective containers and then seal the die in an ESD protective bag for shipment. After the sealed ESD protective bag is opened, store all die in a dry nitrogen environment.
- Handle the chips in a clean environment. Do not attempt to clean the chip using liquid cleaning systems.
- Follow ESD precautions to protect against ESD strikes.
- While bias is applied, suppress instrument and bias supply transients. Use shielded signal and bias cables to minimize inductive pickup.
- Handle the chip along the edges with a vacuum collet or with a sharp pair of tweezers. The surface of the chip has fragile air bridges and must not be touched with a vacuum collet, tweezers, or fingers.

Mounting

Before the epoxy die is attached, apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after the chip is placed into position. Cure the epoxy per the schedule of the manufacturer.

Wire Bonding

RF bonds made with 3 mil × 0. 5 mil gold ribbon are recommended for the RF ports. These bonds must be thermosonically bonded with a force of 40 g to 60 g. Thermosonically bonded dc bonds of 0.025 mm diameter, are recommended. Create ball bonds with a force of 40 g to 50 g and wedge bonds with a force of 18 g to 22 g. Create all bonds with a nominal stage temperature of 150°C. Apply the minimum amount of ultrasonic energy (depending on the process and package being used) to achieve reliable bonds. Keep all bonds as short as possible, less than 0.31 mm.

Alternatively, short RF bonds that are ≤3 mm and made with two 1 mm wires can be used.

BIASING ADPA7005CHIP WITH THE HMC980LP4E

The HMC980LP4E is an active bias controller that is designed to meet the bias requirements for enhancement mode and depletion mode amplifiers such as the ADPA7005CHIP. The controller provides constant drain current biasing over temperature and part to part variation, and properly sequences gate and drain voltages to ensure the safe operation of the amplifier. The HMC980LP4E also offers self protection in the event of a short circuit, as well as an internal charge pump that generates the negative voltage needed on the gate of the ADPA7005CHIP, and the option to use an external negative voltage source. The HMC980LP4E is also available in die form as the HMC980-DIE.

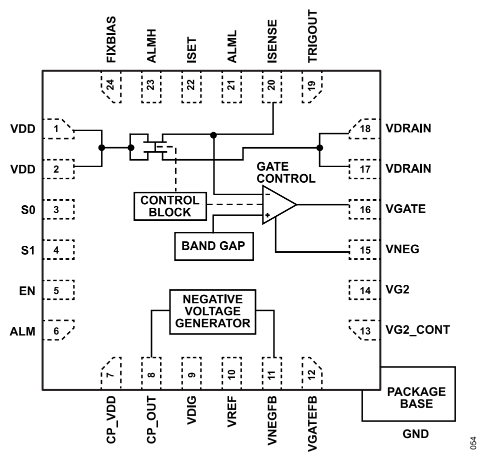

Figure 54. Functional Diagram of HMC980LP4E

APPLICATION CIRCUIT SETUP

Figure 55 displays the schematic of an application circuit using the HMC980LP4E to control the ADPA7005CHIP. When using an external negative supply for VNEG, refer to the schematic in Figure 56.

In the application circuit shown in Figure 55, the ADPA7005CHIP drain voltage and drain current are set by the following equations:

$$VDRAIN\ (5\ V) = V_{DD}\ (6.12\ V) - I_{DRAIN}\ (1600\ mA) \times 0.7\ \Omega \quad (1)$$

$$I_{DRAIN}\ (1600\ mA) = 150\ \Omega\ A \div R10\ (93.1\ \Omega) \quad (2)$$

where I_{DRAIN} is constant drain current.

LIMITING V_{GATE} FOR ADPA7005CHIP V_{GGX} ABSOLUTE MAXIMUM RATING REQUIREMENT

When using the HMC980LP4E to control the ADPA7005CHIP, the minimum voltages for VNEG and VGATE must be −1.5 V to keep these voltages within the absolute maximum rating limits for the V_{GGx} pads of the ADPA7005CHIP. To set the minimum voltages, set R15 and R16 to the values shown in Figure 55 and Figure 56. Please refer to the AN-1363 for more information and calculations for R15 and R16.

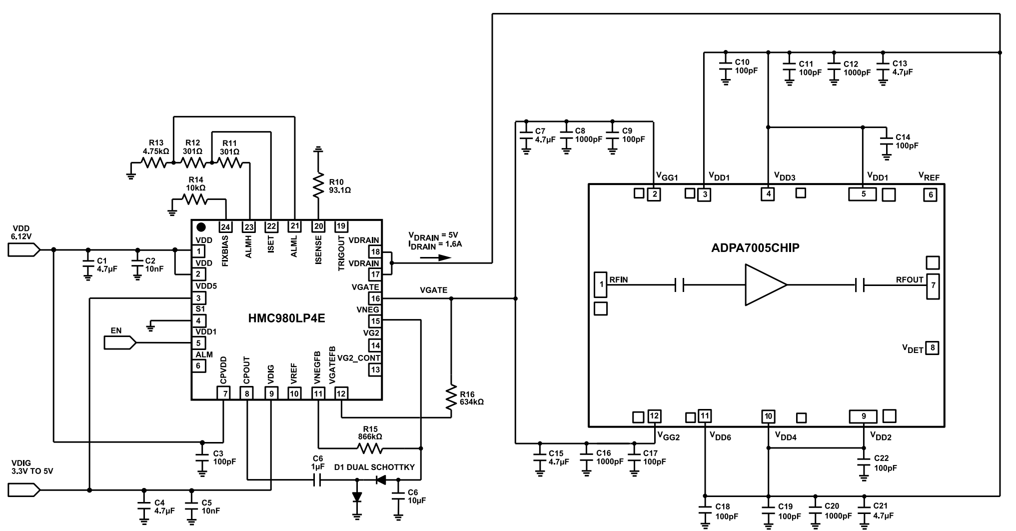

Figure 55. Application Circuit using HMC980LP4E with ADPA7005CHIP

BIASING ADPA7005CHIP WITH THE HMC980LP4E

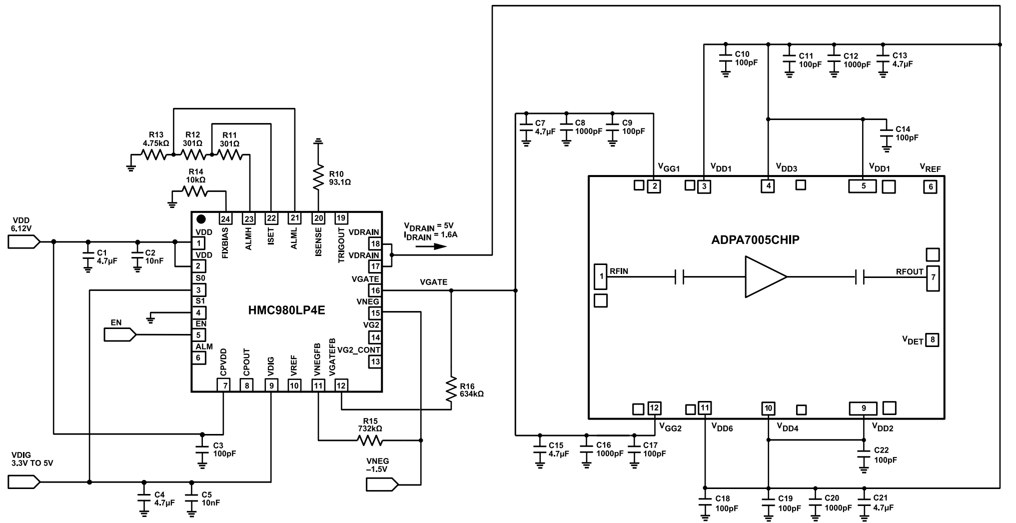

Figure 56. Application Circuit using HMC980LP4E with ADPA7005CHIP with External Negative Voltage Source

HMC980LP4E BIAS SEQUENCE

The dc supply sequencing in the Power-Up Sequence section and the Power-Down Sequence section is required to prevent damage to the HMC980LP4E when using it to control the ADPA7005CHIP.

Power-Up Sequence

The power-up sequence is as follows:

1. VDIG = 3.3 V
2. S0 = 3.3 V
3. VDD = 5.68 V
4. VNEG = −1.5 V (unnecessary if using internally generated voltage)
5. EN = 3.3 V (transition from 0 V to 3.3 V turns on VGATE and VDRAIN)

Power-Down Sequence

The power-down sequence is as follows:

1. EN = 0 V (transition from 3.3 V to 0 V turns off VDRAIN and VGATE)
2. VNEG = 0 V (unnecessary if using internally generated voltage)
3. VDD = 0 V
4. S0 = 0 V
5. VDIG = 0 V

After the HMC980LP4E bias control circuit is set up, toggle the bias to the ADPA7005CHIP on or off by applying 3.3 V or 0 V, respectively, to the EN pad. At EN = 3.3 V, VGATE drops to −1.5 V and VDRAIN turns on at 5 V. VGATE then rises until I_{DRAIN} = 800 mA, and the closed control loop regulates I_{DRAIN} at 1600 mA. When EN = 0 V, VGATE is set to −1.5 V, and VDRAIN is set to 0 V (see Figure 57 and Figure 58).

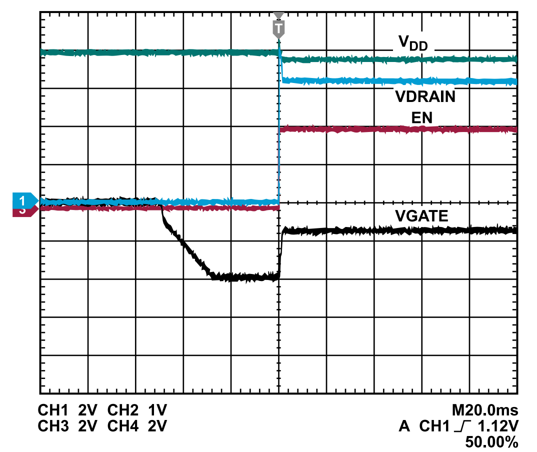

Figure 57. Turn On HMC980LP4E Outputs to ADPA7005CHIP

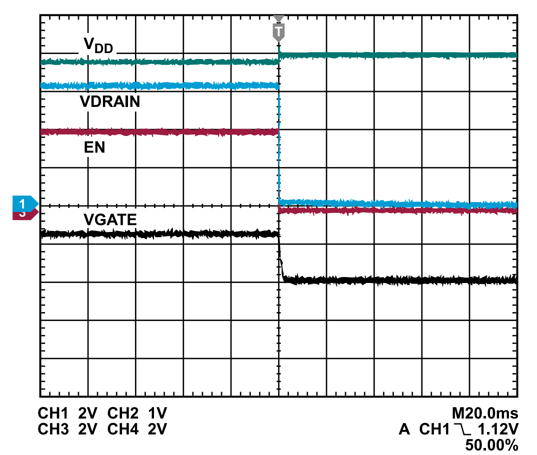

Figure 58. Turn Off HMC980LP4E Outputs to ADPA7005CHIP

BIASING ADPA7005CHIP WITH THE HMC980LP4E

CONSTANT DRAIN CURRENT BIASING VS. CONSTANT GATE VOLTAGE BIASING

The HMC980LP4E uses a closed-loop feedback to continuously adjust VGATE to maintain a constant gate current bias over dc supply variation, temperature, and part to part variation. In addition, constant drain current bias is the optimum method for reducing time in calibration procedures and for maintaining consistent performance over time. By comparing with a constant gate voltage bias where the current is driven to increase when RF power is applied, a slightly lower output P1dB is seen with a constant drain current bias. This output P1db is displayed in Figure 62, where the RF performance is slightly lower than constant gate voltage bias operation due to a lower drain current at the high input powers as the device reaches 1 dB compression.

The output P1dB performance for constant drain current bias can be increased towards constant gate voltage bias performance by increasing the set current towards the I_{DD} it would reach under RF drive in the constant gate voltage bias condition, as shown in Figure 62. The limit of increasing I_{DQ} under the constant current operation is set by the thermal limitations that can be found in the absolute maximum ratings table (see Table 4) from the amplifier data sheet with the maximum power dissipation specification. As the I_{DD} increase continues, the actual output P1dB does not continue to increase indefinitely, and the power dissipation increases. Thus, take the exchange between the power dissipation and output P1dB performance into consideration when using constant drain current biasing.

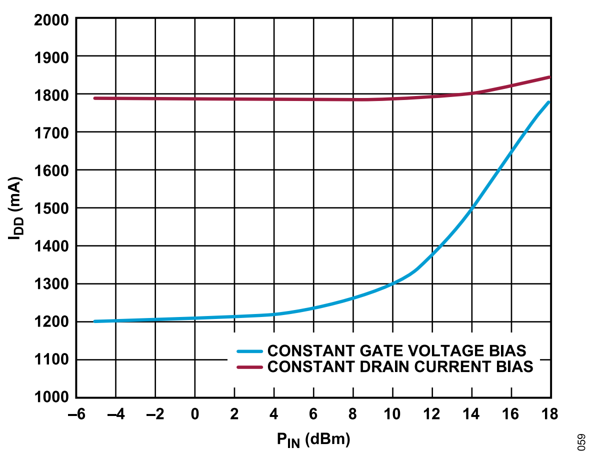

Figure 59. I_{DD} vs. RF Input Power (P_{IN}), V_{DD} = 5 V, Frequency = 32 GHz for Constant Drain Current Bias and Constant Gate Voltage Bias

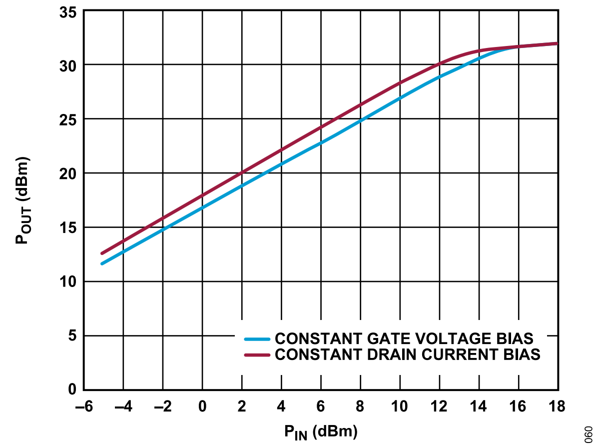

Figure 60. P_{OUT} vs. P_{IN}, V_{DD} = 5 V, Frequency = 32 GHz, Constant Drain Current Bias and Constant Gate Voltage Bias

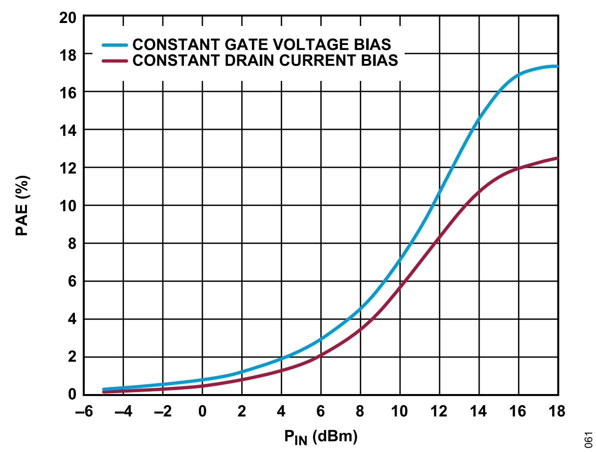

Figure 61. PAE vs. P_{IN}, V_{DD} = 5 V, Frequency = 32 GHz, Constant Drain Current Bias and Constant Gate Voltage Bias

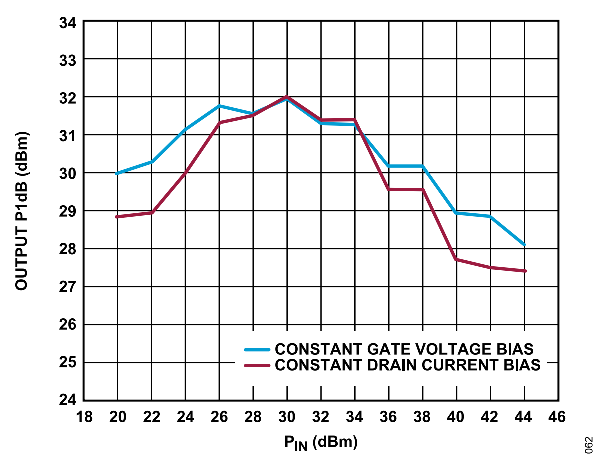

Figure 62. Output P1dB vs. P_{IN}, V_{DD} = 5 V, Frequency = 32 GHz, Constant Drain Current Bias and Constant Gate Voltage Bias

TYPICAL APPLICATION CIRCUIT

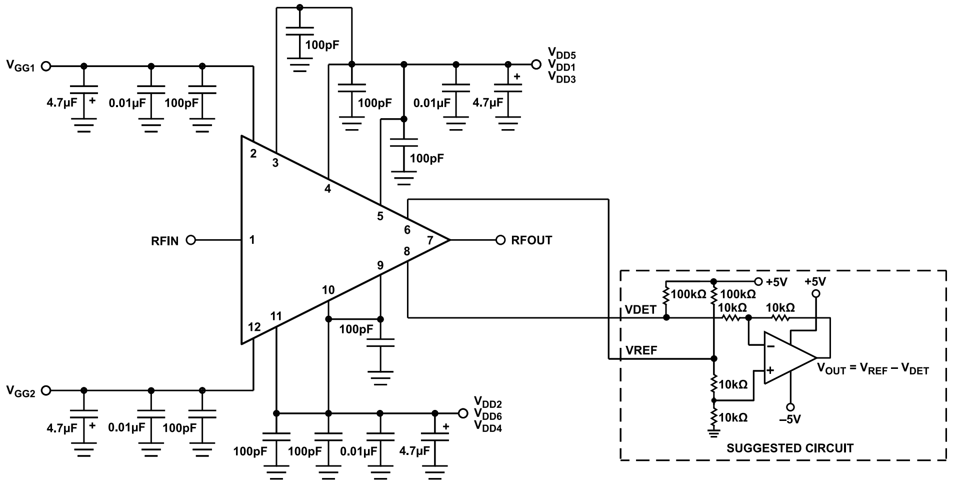

Figure 63. Typical Application Circuit Using the HMC980LP4E with the ADPA7005CHIP

ASSEMBLY DIAGRAM

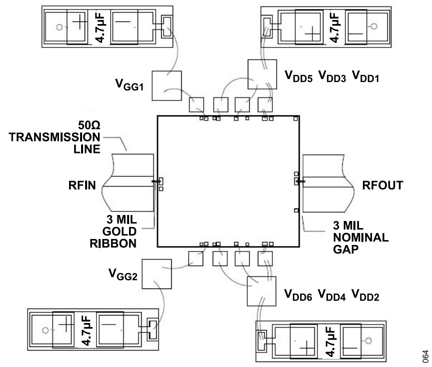

Figure 64. Assembly Diagram

OUTLINE DIMENSIONS

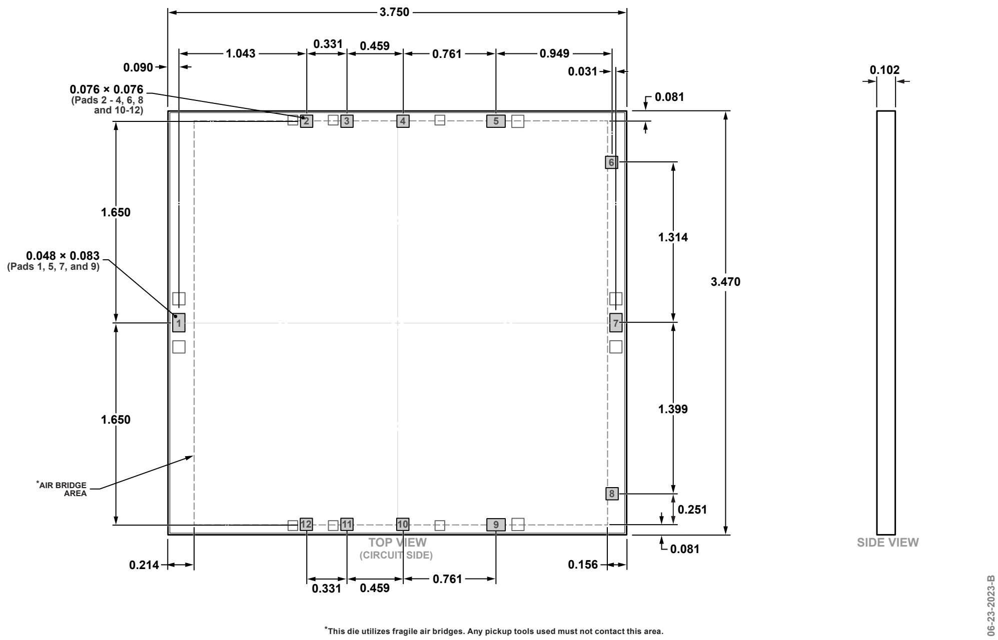

Figure 65. 12-Pad Bare Die [CHIP]
(C-12-3)
Dimensions shown in millimeters

Updated: June 20, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADPA7005CHIP	-55°C to +85°C	CHIPS OR DIE	C-12-3
ADPA7005C-KIT	-55°C to +85°C	CHIPS OR DIE	C-12-3

1 All models are RoHS compliant.