



**THE DATASHEET OF  
DLD101-7**

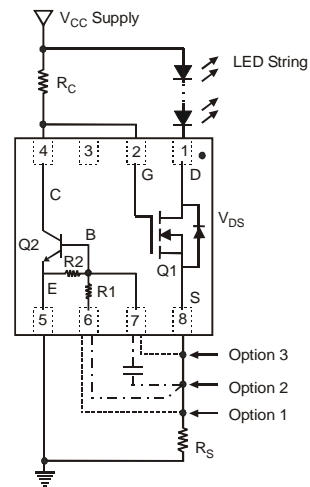
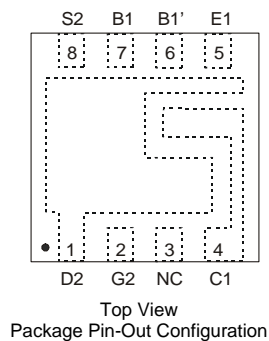
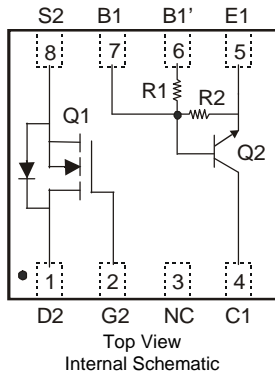


**Features**

- Primarily Designed for Driving LED/s for Illumination, Signage and Backlighting Applications
- Ideally Suited for Linear Mode Constant Current Applications
- $V_{BE}$  Referenced Current Sink Circuit
- Includes:
  - N-Channel Enhancement Mode MOSFET (Q1)
  - Base Accessible Pre-Biased Transistor (Q2)
- High Voltage Capable (50V)
- Small Form Factor Surface Mount Package
- High Dissipation Capability
- Low Thermal Resistance
- Lead Free By Design/RoHS Compliant (Note 1)**
- "Green" Device (Note 2)**
- Qualified to AEC-Q101 Standards for High Reliability**

**Mechanical Data**

- Case: DFN3030D-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish — NiPdAu over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Marking Information: See Page 7
- Ordering Information: See Page 7
- Weight: 0.0172 grams (approximate)



Typical Application Circuit for Linear Mode Current Sink LED Driver

**Maximum Ratings: (Q1)** @ $T_A = 25^\circ C$  unless otherwise specified

Characteristic	Symbol	Value	Unit
Drain Source Voltage	$V_{DSS}$	100	V
Gate-Source Voltage	$V_{GSS}$	$\pm 20$	V
Drain Current (Note 3)	$I_D$	1.0 0.8	A
		$T_A = 25^\circ C$ $T_A = 70^\circ C$	
Drain Current (Note 3)	$I_{DM}$	3.0	A
Body-Diode Continuous Current (Note 3)	$I_S$	1.0	A

**Maximum Ratings: (Q2)** @ $T_A = 25^\circ C$  unless otherwise specified

Characteristic	Symbol	Value	Unit
Supply Voltage	$V_{CC}$	50	V
Input Voltage	$V_{IN}$	-5 to +30	V
Output Current (DC)	$I_O$	100	mA

Notes: 1. No purposefully added lead.  
2. Diodes Inc.'s "Green" policy can be found on our website at [http://www.diodes.com/products/lead\\_free/index.php](http://www.diodes.com/products/lead_free/index.php).

**Thermal Characteristics – Total Device**

Characteristic	Symbol	Value	Unit
Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	0.7 (Note 3) 0.9 (Note 4) 1.4 (Note 5)	W
Thermal Resistance Junction to Ambient @ $T_A = 25^\circ\text{C}$	$R_{\theta JA}$	See Figure 1 (Notes 3, 4, & 5)	$^\circ\text{C/W}$
Thermal Resistance Junction to Case @ $T_A = 25^\circ\text{C}$	$R_{\theta JC}$	See Figure 2 (Notes 3, 4, & 5)	$^\circ\text{C/W}$
Operating and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$

Notes: 3. Part mounted on FR-4 substrate PC board, with minimum recommended pad layout (see page 6).  
 4. Part mounted on FR-4 substrate PC board, 2oz Copper with 6 mm<sup>2</sup> Cu Area, MOSFET element activated.  
 5. Part mounted on FR-4 substrate PC board, 2oz Copper with 35 mm<sup>2</sup> Cu Area, MOSFET element activated.

**Electrical Characteristics: (Q1) @ $T_A = 25^\circ\text{C}$  unless otherwise specified**

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 6)</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 60V, V_{GS} = 0V$
Gate-Source Leakage	$I_{GSS}$	—	—	$\pm 100$	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
<b>ON CHARACTERISTICS (Note 6)</b>						
Gate Threshold Voltage	$V_{GS(th)}$	2.0	—	4.1	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	—	0.85 0.99	$\Omega$	$V_{GS} = 10V, I_D = 1.5A$ $V_{GS} = 6V, I_D = 1A$
Forward Transconductance	$g_{fs}$	—	0.9	—	S	$V_{DS} = 15V, I_D = 1A$
Diode Forward Voltage	$V_{SD}$	—	0.89	1.1	V	$V_{GS} = 0V, I_S = 1.5A$
<b>DYNAMIC CHARACTERISTICS</b>						
Input Capacitance	$C_{iss}$	—	129	—	pF	$V_{DS} = 50V, V_{GS} = 0V$ $f = 1.0\text{MHz}$
Output Capacitance	$C_{oss}$	—	14	—	pF	
Reverse Transfer Capacitance	$C_{rss}$	—	8	—	pF	
<b>SWITCHING CHARACTERISTICS</b>						
Total Gate Charge	$Q_g$	—	3.4	—	nC	$V_{DS} = 50V, V_{GS} = 10V, I_D = 1A$
Gate-Source Charge	$Q_{gs}$	—	0.9	—		
Gate-Drain Charge	$Q_{gd}$	—	1	—		
Turn-On Delay Time	$t_{d(on)}$	—	7.9	—	ns	$V_{GS} = 50V, V_{DS} = 10V,$ $I_D = 1A, R_G \approx 6\Omega$
Rise Time	$t_r$	—	11.4	—		
Turn-Off Delay Time	$t_{d(off)}$	—	14.3	—		
Fall Time	$t_f$	—	9.6	—		

**Electrical Characteristics: (Q2) @ $T_A = 25^\circ\text{C}$  unless otherwise specified**

Characteristic (Note 6)	Symbol	Min	Typ	Max	Unit	Test Condition
Input Voltage	$V_{I(off)}$	0.4	-	-	V	$V_{CC} = 5V, I_O = 100\mu\text{A}$
	$V_{I(on)}$	-	-	1.5	V	$V_{CC} = 0.3V, I_O = 5\text{mA}$
Output Voltage	$V_{O(on)}$	-	0.05	0.3	V	$I_O/I_I = 5\text{mA}/0.25\text{mA}$
Output Current	$I_{O(off)}$	-	-	0.5	$\mu\text{A}$	$V_{CC} = 50V, V_I = 0V$
DC Current Gain	$G_1$	80	-	-	-	$V_O = 5V, I_O = 10\text{mA}$
Input Resistance	$R_1$	3.2	4.7	6.2	k $\Omega$	-
Resistance Ratio	$R_2/R_1$	8	10	12	-	-
Transition Frequency	$f_T$	-	260	-	MHz	$V_{CE} = 10V, I_E = 5\text{mA},$ $f = 100\text{MHz}$

Notes: 6. Short duration pulse test used to minimize self-heating effect.

**Thermal Characteristics**

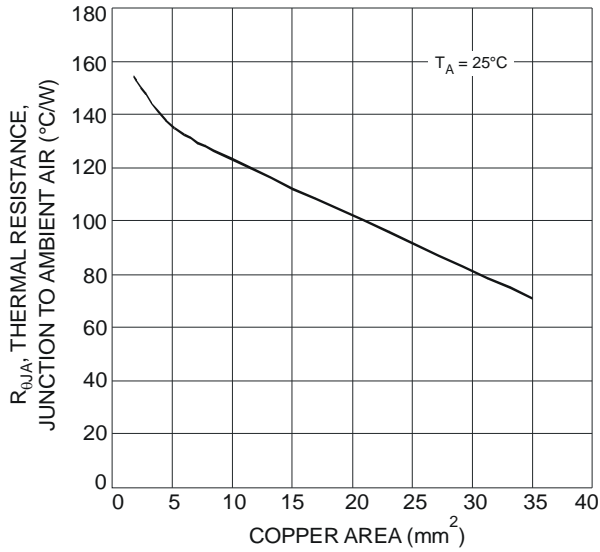


Fig. 1 Thermal Resistance, Junction to Ambient Air Characteristic

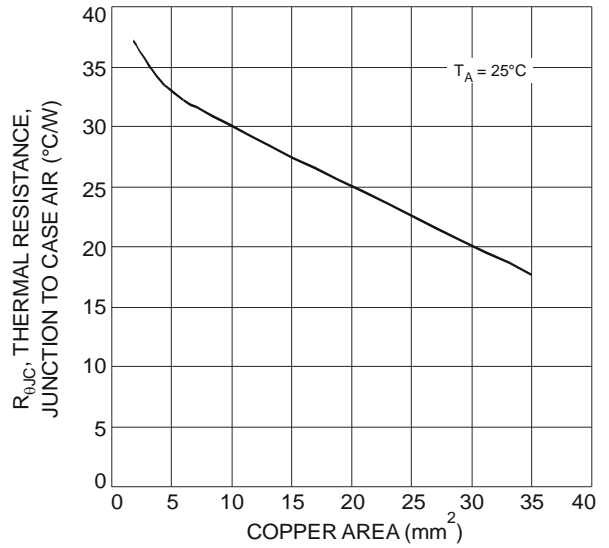


Fig. 2 Thermal Resistance, Junction to Case Air Characteristic

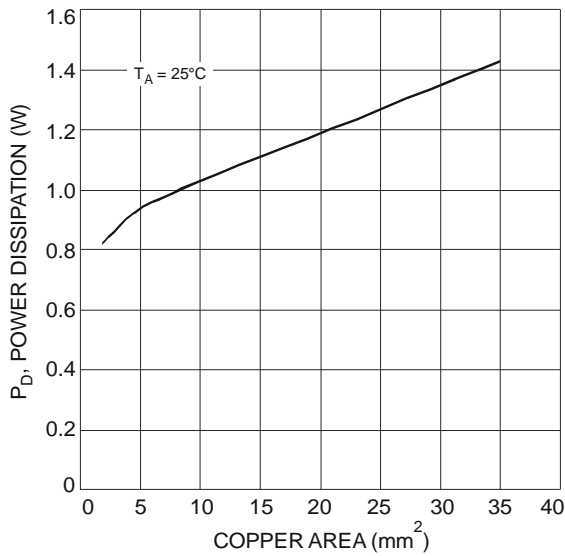


Fig. 3 Power Dissipation Characteristic

**Q1 Typical Performance Curves**

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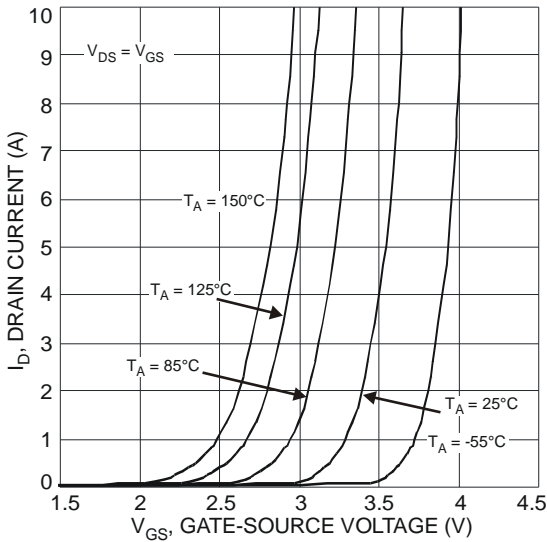


Fig. 4 Typical Transfer Characteristic

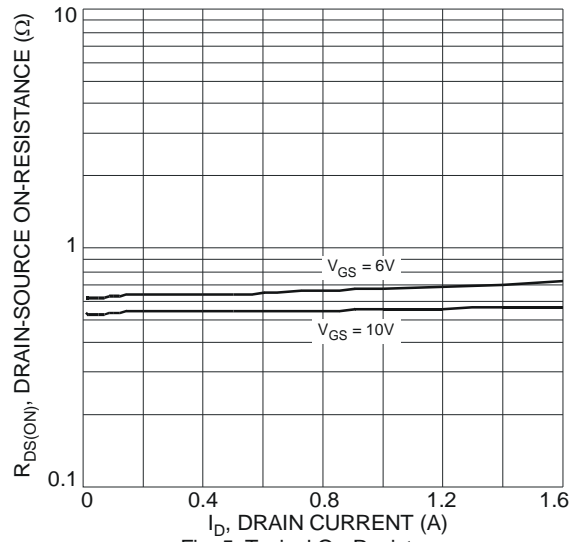


Fig. 5 Typical On-Resistance vs. Drain Current and Gate Voltage

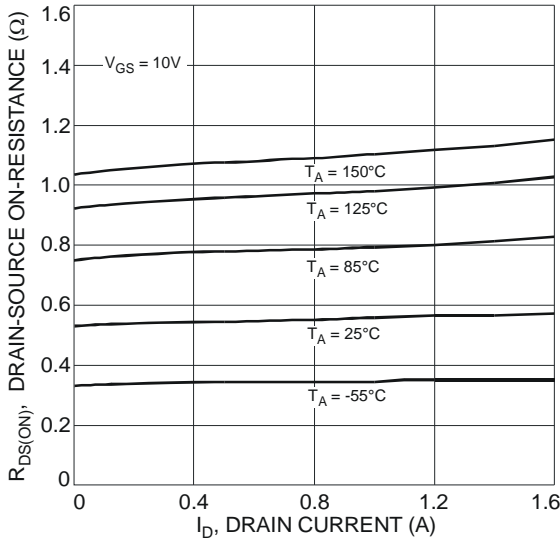


Fig. 6 Typical On-Resistance vs. Drain Current and Temperature

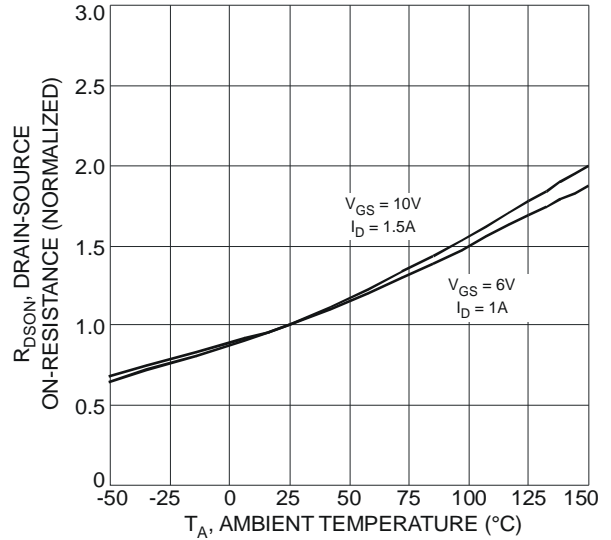


Fig. 7 On-Resistance Variation with Temperature

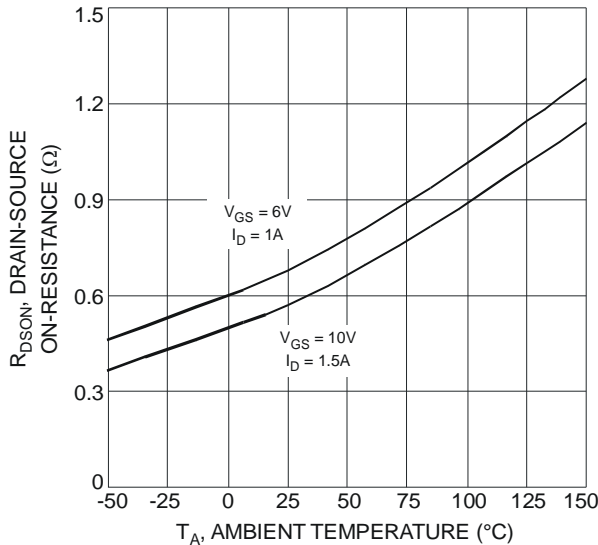


Fig. 8 On-Resistance Variation with Temperature

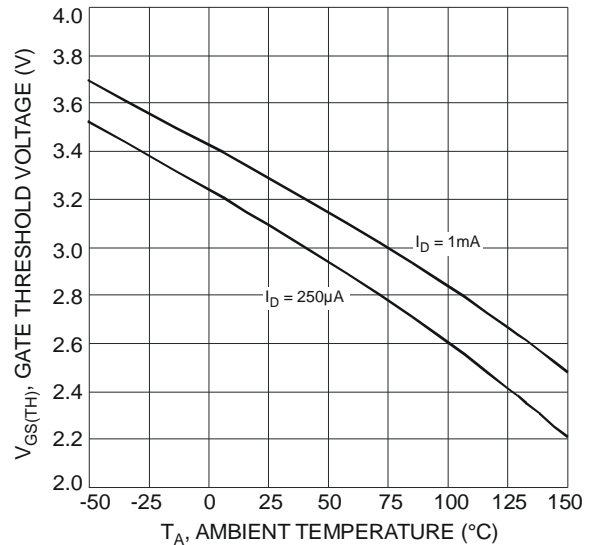


Fig. 9 Gate Threshold Variation vs. Ambient Temperature

**Q1 Typical Performance Curves - continued**

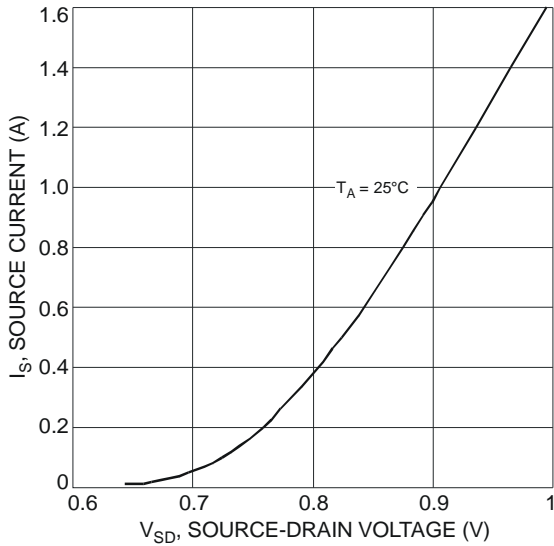


Fig. 10 Source-Drain Diode Forward Voltage vs. Current

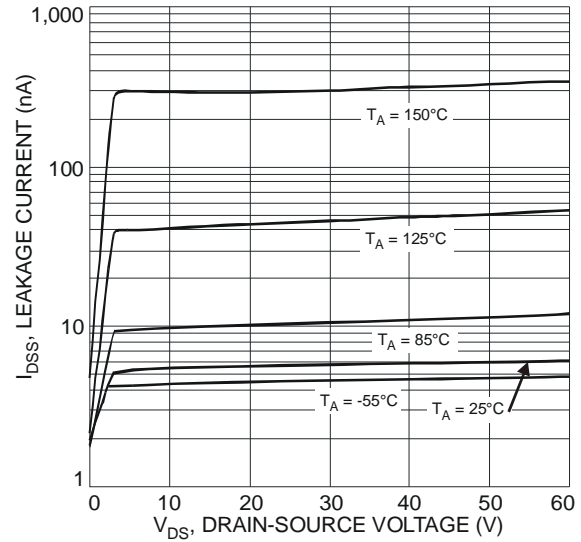


Fig. 11 Typical Leakage Current vs. Drain-Source Voltage

**Q2 Typical Performance Curves**

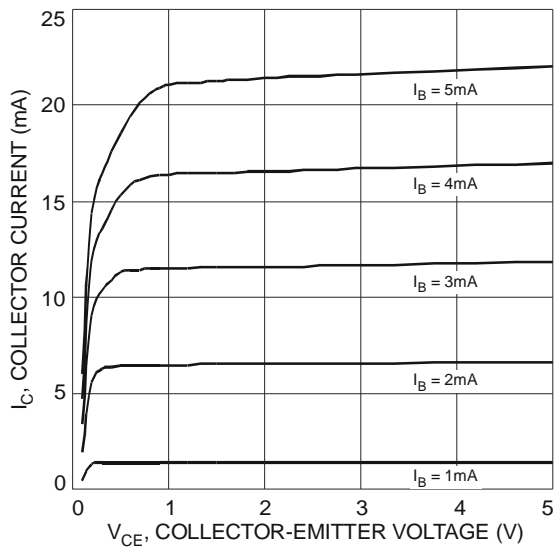


Fig. 12 Typical Collector Current vs. Collector-Emitter Voltage

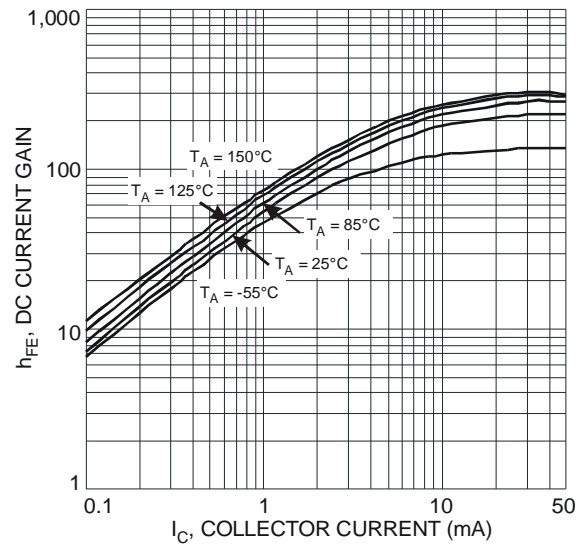


Fig. 13 Typical DC Current Gain vs. Collector Current

**Q2 Typical Performance Curves - continued**

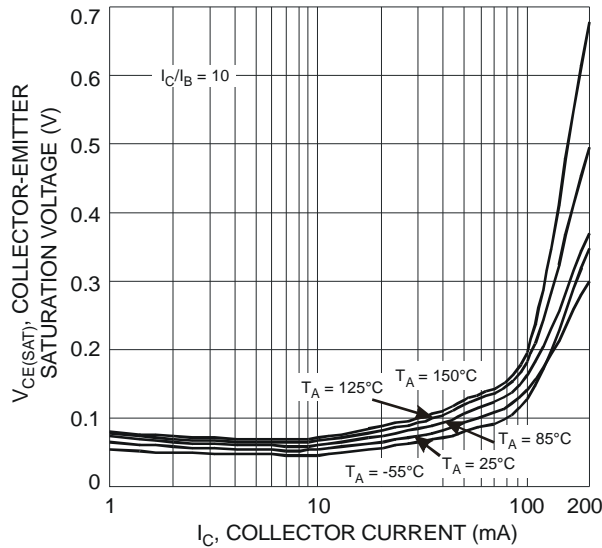


Fig. 14 Typical Collector-Emitter Saturation Voltage vs. Collector Current

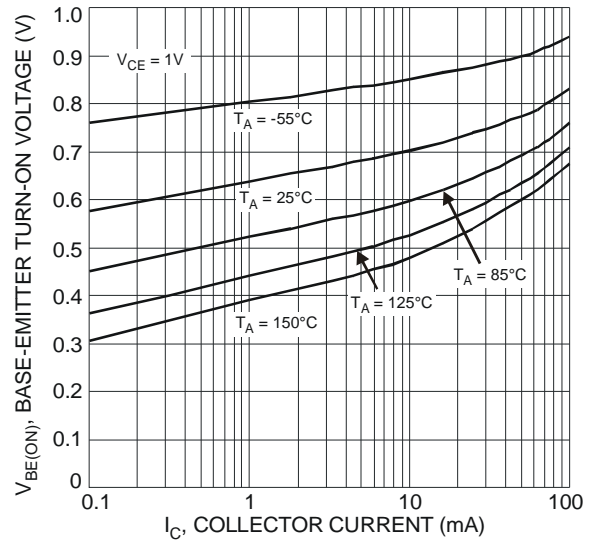


Fig. 15 Base-Emitter Turn-On Voltage vs. Collector Current

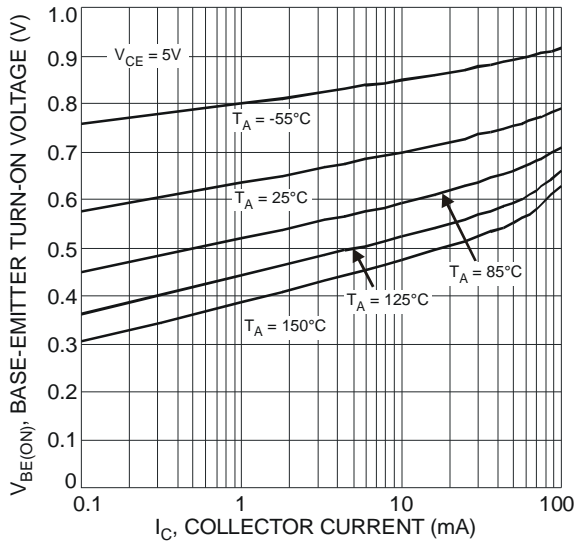
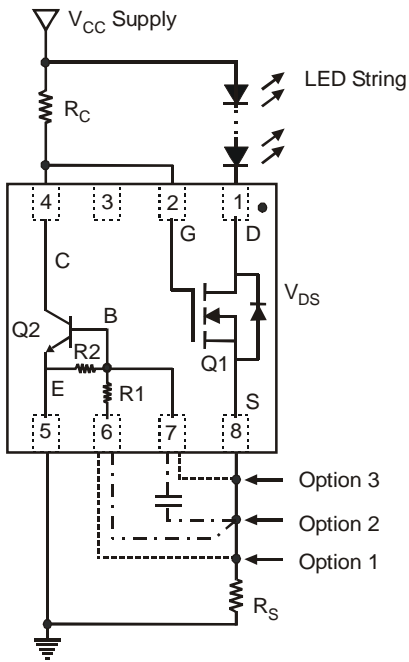


Fig. 16 Base-Emitter Turn-On Voltage vs. Collector Current

**Typical Application Circuit**



Option 3:  
 $I_{LED} \approx \frac{V_{BE}}{R_S}$

Options 1 & 2:  
 $I_{LED} \approx \frac{1.1 V_{BE}}{R_S}$

Option 2:  
 Capacitor is across R2 for better noise performance.

The DLD101 has been designed primarily for solid state lighting applications, to be used as a current sink circuit solution for LEDs. It features a N-channel MOSFET capable of 1A drive current and a pre-biased NPN transistor (which allows direct connection to the base, or via a series base resistor).

Figure 12 shows a typical application circuit diagram for driving an LED or string of LEDs. Note that the pre-biased transistor (Q2) has the option of bypassing the series base resistor by connecting directly to pin 7. The N-MOSFET (Q1) is configured as a  $V_{BE}$  referenced current sink and is biased on by  $R_C$ . The current passed through the LED string, MOSFET and source resistor, develops a voltage across  $R_S$  that provides a bias to the NPN transistor. Consideration of the expected linear mode power dissipation must be factored into the design, with respect to the DLD101's thermal resistance.

$V_{DS} = V_{CC} - V_F \text{ LED String} - V_{RS}$   
 $P_{Q1} = V_{DS} * I_{LED \text{ String}}$

PWM dimming functionality can be effected by either driving the NPN base via an additional resistor (thereby overriding the feedback from  $R_S$ ) or by pulling the gate of the MOSFET down by direct connection. The PWM control pulse stream can be provided by a micro-controller or simple 555 based circuitry.

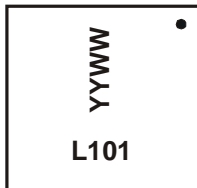
Fig. 12 Typical Application Circuit for Linear Mode Current Sink LED Driver

**Ordering Information** (Note 7)

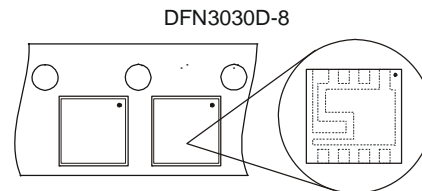
Part Number	Case	Packaging
DLD101-7	DFN3030D-8	3000/Tape & Reel

Notes: 7. For packaging details, go to our website at <http://www.diodes.com/datasheets/ap02007.pdf>.

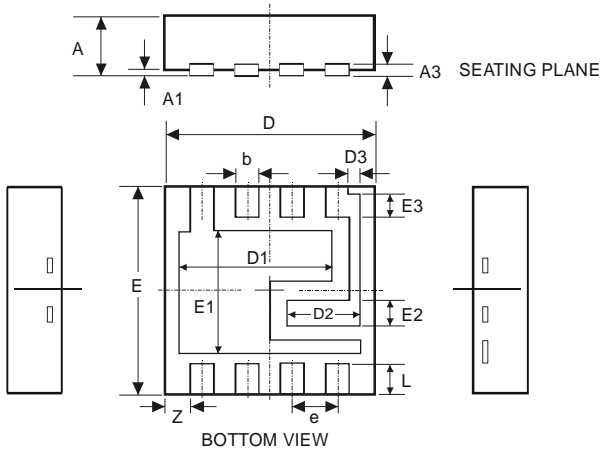
**Marking Information**



L101 = Product marking code  
 YYWW = Date code marking  
 YY = Last digit of year (ex: 10 for 2010)  
 WW = Week code (01 to 53)

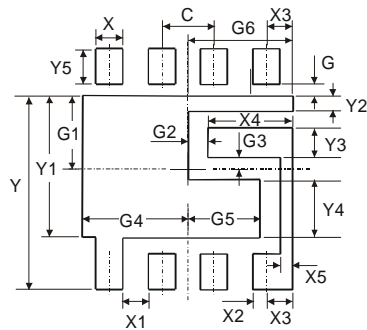


**Package Outline Dimensions**



DFN3030D-8							
Dim	Min	Max	Typ	Dim	Min	Max	Typ
A	0.570	0.630	0.600	e	-	-	0.650
A1	0	0.050	0.020	E	2.950	3.075	3.000
A3	-	-	0.150	E1	1.800	2.000	1.900
b	0.290	0.390	0.340	E2	0.290	0.490	0.390
D	2.950	3.075	3.000	E3	0.175	0.375	0.275
D1	2.175	2.375	2.275	L	0.300	0.40	0.350
D2	0.980	1.180	1.080	Z	-	-	0.355
D3	0.105	0.305	0.205				
All Dimensions in mm							

**Suggested Pad Layout**



Dimensions	Value (in mm)	Dimensions	Value (in mm)
C	0.650	X2	0.220
G	0.150	X3	0.375
G1	0.950	X4	1.080
G2	0.270	X5	0.150
G3	0.135	Y	2.600
G4	1.350	Y1	1.900
G5	0.925	Y2	0.150
G6	1.350	Y3	0.390
X	0.440	Y4	0.815
X1	0.210	Y5	0.550

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