THE DATASHEET OF

SI8941AD-IS4R

DATA SHEET

Si8941/Si8946/Si8947 Isolated Delta-Sigma Modulator for Current Shunt Measurement

Applications

- Industrial, HEV and renewable energy inverters
- AC, brushless, and DC motor controls and drives
- Variable speed motor control in consumer white goods
- Isolated switch mode and UPS power supplies
- Automotive on-board chargers, battery management systems, and charging stations

Features

- Low voltage differential input
  - ±62.5 mV and ±250 mV options
- Modulator clock options
  - External clock up to 25 MHz (Si8941)
  - 10 MHz internal clock (Si8946)
  - 20 MHz internal clock (Si8947)
- Typical input offset: ±50 µV
- Typical gain error: ±0.05%
- Excellent drift specifications
  - ±0.5 µV/°C typical offset drift
  - ±4 ppm/°C typical gain drift
- Typical 14-bit (ENOB) precision
- High common-mode transient immunity: 75 kV/µs
- Typical SNR: 90 dB
- Typical THD: –97 dB
- Automotive-grade OPNs available
  - AEC-Q100 qualification
  - AIAG-compliant PPAP documentation support
  - IMDS and CAMDS listing support
- Compact packages
  - 8-pin wide body stretched SOIC
  - 8-pin narrow body SOIC
- –40 to 125 °C

Safety Approvals

- UL 1577 recognized
  - Up to 5000 kV_{RMS} for 1 minute
- CSA certification conformity
  - 62368-1 (reinforced insulation)
- VDE certification conformity (Pending)
  - 60747-17 (reinforced insulation)
- CQC certification approval
  - GB4943.1

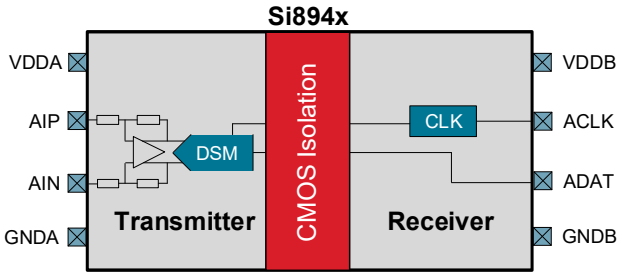


Figure 1. Si894x Block Diagram

Description

The Si8941/46/47 are galvanically isolated delta-sigma modulators which output a digital signal proportional to the voltage level at the input. The low-voltage differential input is ideal for measuring voltage across a current shunt resistor or for any place where a sensor must be isolated from the control system. Low noise, low error, and high precision ensure an accurate measurement of system current.

The output of the Si8941/46/47 comes from a second order delta-sigma modulator. The modulator can be clocked either from an on-board oscillator (Si8946/47) or from an external clock (Si8941). The output is typically digitally filtered by an MCU or FPGA in the system.

The Si8941/46/47 isolated delta-sigma modulator utilizes Skyworks proprietary isolation technology. It supports up to 5.0 kV_{RMS} withstand voltage per UL1577. This technology enables higher performance, reduced variation with temperature and age, tighter part-to-part matching, and longer lifetimes compared to other isolation technologies.

Automotive Grade is available for certain part numbers. These products are built using automotive-specific flows at all steps in the manufacturing process to ensure the robustness and low defectivity required for automotive applications.

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

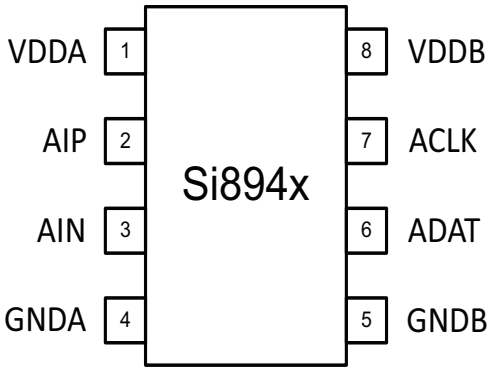


Figure 2. Si894x Pinout (Top View)

Table 1. Si894x Pin Descriptions

Name	Pin Number	Description
VDDA	1	Input side power supply
AIP	2	Analog input high
AIN	3	Analog input low
GNDA	4	Input side ground
GNDB	5	Output side ground
ADAT	6	Delta-Sigma modulator data output
ACLK	7	Delta-Sigma modulator clock (input on Si8941, output on Si8946/47)
VDDB	8	Output side power supply

1. Technical Description

The input to the Si8941/46/47 is designed for low-voltage, differential signals. This is ideal for connection to low-resistance current shunt measurement resistors. The Si8941A/46A/47A has a specified full scale input range of ±62.5 mV, and the Si8941B/46B/47B has a specified full scale input range of ±250 mV. This allows the user to choose low-ohmic resistance value sense resistors to minimize system power loss.

The analog input stage of the Si8941/46/47 is a fully differential amplifier feeding the input of a second-order, delta-sigma modulator that digitizes the input signal into a 1-bit output stream. The isolated data output ADAT pin of the converter provides a stream of digital ones and zeros that is synchronous to the ACLK pin.

The Si8946/47 clock is generated internally while the Si8941 clock is provided externally. The time average of this serial bit-stream output is proportional to the analog input voltage.

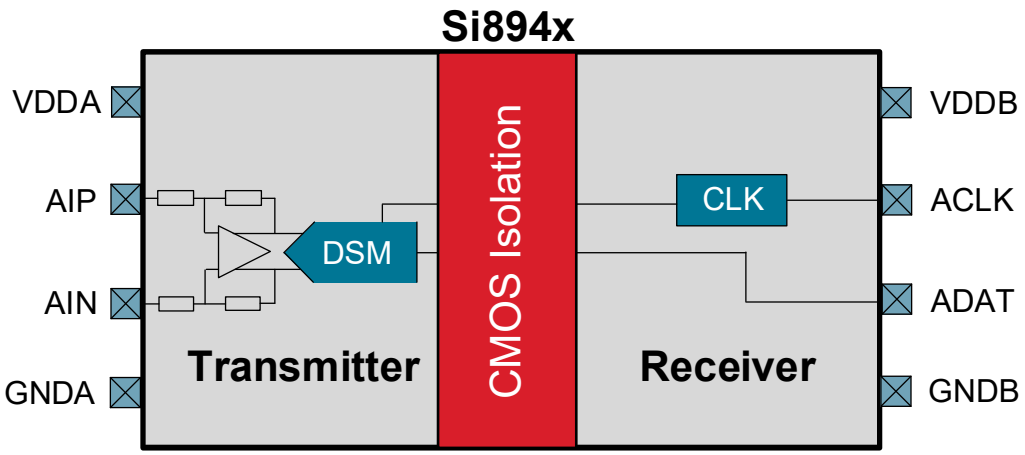


Figure 3. Si8941/Si8946/Si8947 Functional Block Diagram

1.1. Fail-Safe and Low-Power Modes

The Si8941/46/47 implements a fail-safe output when the high voltage-side supply voltage VDDA goes away. The fail-safe output is a steady state logic 0 on ADAT for the externally clocked Si8941. The fail-safe output is a steady state logic 1 on ADAT for the internally clocked Si8946/47.

The clock output ACLK of the Si8946/47 will stop after 256 cycles with a steady state logic 1. When the supply comes back, the clock will be turned back on and the normal DSM data stream will be output in approximately 250 µs. To differentiate from the failsafe output, a maximum nominal input signal will generate a single 1 every 128 bits at ADAT.

In addition to the fail-safe output, when a loss of VDDA supply occurs, the part will automatically move into a lower power mode that reduces IDDB current to approximately 1 mA. Similarly, a loss of VDDB supply will reduce IDDA current to approximately 1 mA. When the supply voltage is returned, normal operation begins in approximately 250 µs.

1.2. Modulator

The output of the Si8941/46/47 comes from a second order delta-sigma modulator, see Figure 3. The modulator provides 1-bit data stream whose average represents the input analog voltage. Zero volts across the inputs is represented at the output by a pulse train that has 50% ones density.

Positive specified linear full-scale at the input (e.g., +250 mV for the Si8941B/46B/47B and +62.5 mV for the Si8941A/46A/47A) produces an output datastream that has 89.06% ones density, and negative specified full scale gives an output that has 10.94% ones density. Table xx shows the values for other input levels and for both full-scale input options of the device.

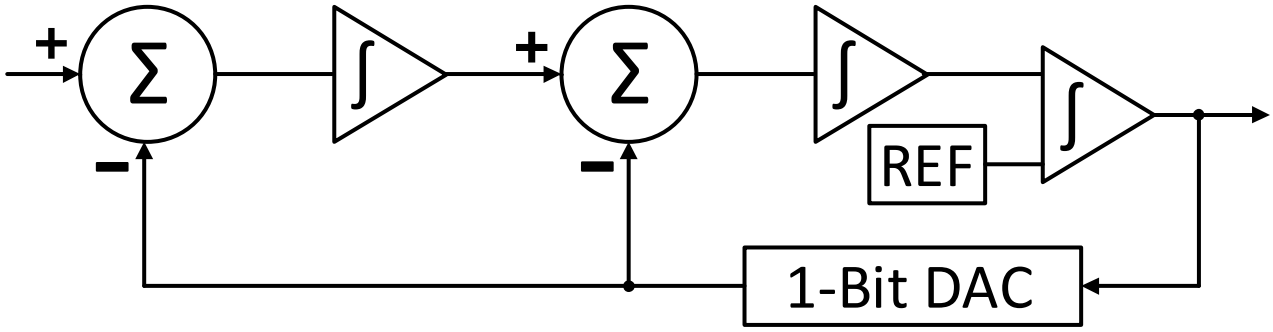


Figure 4. Typical Second Order Delta-Sigma Modulator Block Diagram

Table 2. Modulator Output

Differential Input		Bitstream % Ones
Si8941A/46A/47A	Si8941B/46B/47B	
+62.5 mV	+250 mV	89.06%
+31.25 mV	+125 mV	69.53%
0 mV	0 mV	50%
-31.25 mV	-125 mV	30.47%
-62.5 mV	-250 mV	10.94%

2. Current Sense Application

In the driver circuit presented below, the Si8941/46/47 is used to amplify the voltage across the sense resistor, RSENSE, where it is oversampled and converted into a 1-bit bitstream, then transmitted across the isolation barrier to be processed by the system controller/FPGA. Placing the sense resistor before the load is known as high-side sensing and isolation is needed because the voltage of RSENSE with respect to ground will swing between 0 V and the high voltage rail connected to the drain of Q1.

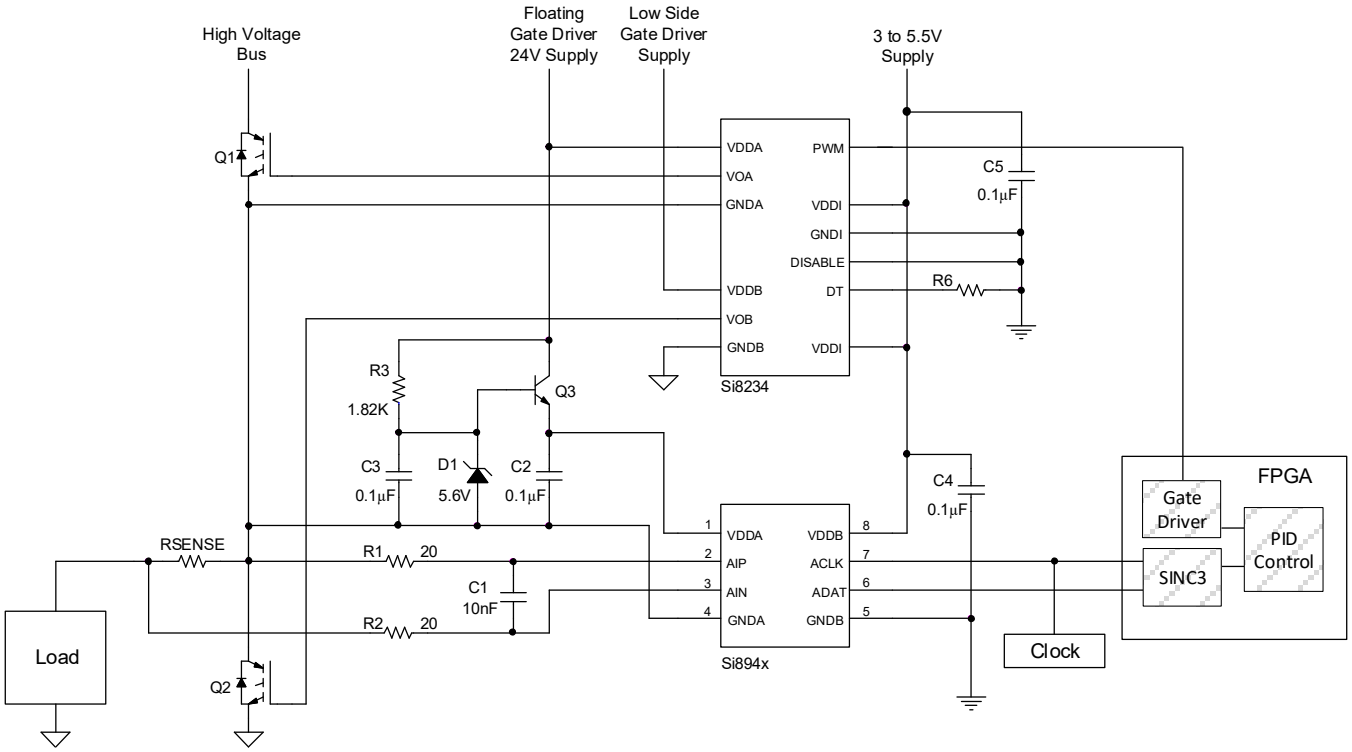


Figure 5. Current Sense Application

The load in this application can be a motor winding or a similar inductive winding. In a three-phase motor drive application, this circuit would be repeated three times, one for each phase. RSENSE should be a small value resistor to reduce power loss. However, an excessively low resistance will reduce the signal-to-noise ratio of the measurement.

Si8941/46/47 offers two specified linear full-scale input options, ±62.5 mV (Si8941A/46A/47A) and ±250 mV (Si8941B/46B/47B), for optimizing the value of RSENSE. Further product ordering options include whether the CLK pin is an input (Si8941) or an output (Si8946/47).

AIP and AIN connections to the RSENSE resistor should be made as close as possible to each end of the RSENSE resistor as trace resistance will add error to the measurement. The input to the Si8941/46/47 is differential, and the PCB traces back to the input pins should run in parallel. This ensures that any large noise transients that occur on the high-voltage side are coupled equally to the AIP and AIN pins and will be rejected by the Si8941/46/47 as a common-mode signal.

The Si8941/46/47 has intrinsic low-pass filtering at approximately 800 kHz. If further input filtering is required, a passive, differential RC low-pass filter can be placed between RSENSE and the input pins. Values of R1 = R2 = 20 Ω and C1 = 10 nF provides a cutoff at approximately 400 kHz. For the lowest gain error, R1 and R2 should always be less than 33 Ω to keep the source impedance sufficiently low compared to the Si8941/46/47 input impedance.

The common-mode voltage of AIN and AIP must be greater than –0.2 V but less than 1 V with respect to GNDA. To meet this requirement, route a trace from the GNDA pin of the Si8941/46/47 to one side of the RSENSE resistor. In this circuit, GNDA, RSENSE, the source of Q1, and the drain of Q2 are connected. The ground of the gate driver (one half of the Skyworks Si8234 in this example) is also commonly connected to the same node.

The Q1 gate driver has a floating supply of 24 V. Since the input and output of the Si8941/46/47 are galvanically isolated from each other, separate power supplies are necessary on each side. Q3, R3, C3, and D1 make a regulator circuit for powering the input side of the Si8941/46/47 from this floating supply. D1 establishes a voltage of 5.6 V at the base of Q3. R3 is selected to provide a Zener current of 10 mA for D1. C3 provides filtering at the base of Q3, and the emitter output of Q3 provides approximately 5 V to VDDA. C2 is a bypass capacitor for the supply and should be placed at the VDDA pin with its return trace connecting to the GNDA connection at RSENSE.

C4, the local bypass capacitor for the B-side of Si8941/46/47, should be placed close to the VDDB supply pin with its return close to GNDB. The output signal typically goes directly to a digital filter for additional processing. The digital filter may be implemented by a dedicated FPGA in the system or may be a peripheral in the main system controller.

The Si8941 expects an external clock to provide the clock signal for the modulator. That external clock can be provided by the same device that implements the digital filtering or another device that syncs both the modulator and the digital filter. The Si8946/47 generates an internal clock to the digital filter.

3. Electrical and Mechanical Specifications

The absolute maximum ratings of the Si8941/Si8946/Si8947 are provided below, followed by electrical specifications, performance graphs, and mechanical specifications.

Table 3. Si8941/Si8946/Si8947 Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Storage temperature	T_{STG}	–65	150	°C
Ambient temperature under bias	T_A	–40	125	°C
Junction temperature	T_J		150	°C
Supply voltage	VDDA, VDDB	–0.5	6.0	V
Input voltage respect to GNDA	V_{IN}	–0.5	VDDA + 0.5	V
Output sink or source current	I_O		5	mA
Total power dissipation	P_T		212	mW
Lead solder temperature (10 s)			260	°C
Human Body Model ESD rating		6000		V
Charged Device Model ESD rating		2000		V

1. Exposure to maximum rating conditions for extended periods may reduce device reliability. Exceeding any of the limits listed here may result in permanent damage to the device.

ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.

Table 4. Si8941/Si8946/Si8947 Electrical Specifications[1]

T_A = –40 to +125 °C, A_{IN} = GNDA, SINC3 filter with 256 oversampling ratio and 20 MHz clock; typical specs at 25 °C with VDDA = V_{DDB} = 5 V unless specified differently under Test Condition

Parameter		Symbol	Test Condition	Min	Typ	Max	Units
Input side supply voltage		VDDA		3.0		5.5	V
Input supply current	Si8941	IDDA	VDDA = 3.3 V		6.9	8.2	mA
	Si8946	IDDA	VDDA = 3.3 V		6.7	8.1	mA
	Si8947	IDDA	VDDA = 3.3 V		6.6	8.8	mA
Output side supply voltage		VDDB		3.0		5.5	V
Output supply current	Si8941	IDDB	V_{DDB} = 3.3 V		4	4.8	mA
	Si8946	IDDB	V_{DDB} = 3.3 V		3.5	6.6	mA
	Si8947	IDDB	V_{DDB} = 3.3 V		7.2	9.7	mA
Amplifier Input							
Specified linear input range	Si8941A/46A/47A	$V_{AIP} – V_{AIN}$		–62.5		62.5	mV
	Si8941B/46B/47B			–250		250	mV
Maximum input voltage before clipping	Si8941A/46A/47A	$V_{AIP} – V_{AIN}$			±80		mV
	Si8941B/46B/47B				±320		mV
Common-mode operating range		V_{CM}	AIN ≠ GNDA	–0.2		1	V
Input offset		V_{OS}	T_A = 25 °C, $A_{IP} = A_{IN}$ = 0	–0.18	±0.05	0.18	mV
Input offset drift		V_{OST}		–2	±0.5	2	µV/°C
Gain error		E_G	T_A = 25 °C	–0.18	±0.05	0.18	%
Gain error drift		E_{GT}		–25	–4	25	ppm/°C
Differential input impedance	Si8941A/46A/47A	R_{IN}			6.3		kΩ
	Si8941B/46B/47B				21.4		kΩ
Differential input impedance drift		R_{INT}			850		ppm/°C
Dynamic Characteristics							
SNR	Si8941A/46A/47A	SNR	F_{IN} = 5 kHz BW = 40 kHz (Si8941/47) BW = 20 kHz (Si8946)	80	86		dB
	Si8941B/46B/47B			84	90		dB
Nonlinearity	Si8941A/46A/47A		T_A = 25 °C	–0.008	0.002	0.008	%
	Si8941B/46B/47B			–0.004	0.001	0.004	%
Nonlinearity drift	Si8941/46/47		T_A = 25 °C	–0.6		0.6	ppm/°C
Total Harmonic distortion	Si8941A/46A/47A	THD	F_{IN} = 5 kHz BW = 40 kHz (Si8941/47) BW = 20 kHz (Si8946)		–95	–81	dB
	Si8941B/46B/47B	THD	F_{IN} = 5 kHz BW = 40 kHz (Si8941/47) BW = 20 kHz (Si8946)		–97	–81	dB
Power-supply rejection ratio		PSRR	VDDA at DC		–100		dB
			VDDA at 100 mV and 10 kHz ripple		–100		dB
			V_{DDB} at DC		–100		dB
			V_{DDB} at 100 mV and 10 kHz ripple		–100		dB
Common-mode transient immunity		CMTI		50	75		kV/µs
Digital							
Logic high input threshold (Si8941)		V_{IH}		85% of V_{DDB}			V
Logic low input threshold (Si8941)		V_{IL}				15% of V_{DDB}	V
Input hysteresis		V_{IHYST}			120		mV
Output load capacitance		C_{LOAD}			15		pF

Table 4. Si8941/Si8946/Si8947 Electrical Specifications[1] (Continued)

T_A = –40 to +125 °C, A_{IN} = GNDA, SINC3 filter with 256 oversampling ratio and 20 MHz clock; typical specs at 25 °C with VDDA = V_{DDB} = 5 V unless specified differently under Test Condition

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
External Clock (Si8941)						
Clock frequency	FCLKIN		5		25	MHz
Duty cycle	FDUTY		45	50	55	%
Delay to data valid	TDELAY				23	ns
Data hold time	THOLD		6			ns
Internal Clock (Si8946)						
Clock frequency	FCLKOUT	T_A = 25 °C	9.9	10	10.1	MHz
		T_A = –40 °C to 125 °C	9.8	10	10.2	MHz
Duty cycle	FDUTY		45	50	55	%
Delay to data valid	TDELAY				60	ns
Data hold time	THOLD		40			ns
Internal Clock (Si8947)						
Clock frequency	FCLKOUT	T_A = 25 °C	19.8	20	20.2	MHz
		T_A = –40 °C to 125 °C	19.6	20	20.4	MHz
Duty cycle	FDUTY		45	50	55	%
Delay to data valid	TDELAY				30	ns
Data hold time	THOLD		20			ns

1. Performance is guaranteed only under the conditions listed in this Table and is not guaranteed over the full operating or storage temperature ranges. Operation at elevated temperatures may reduce reliability of the device.

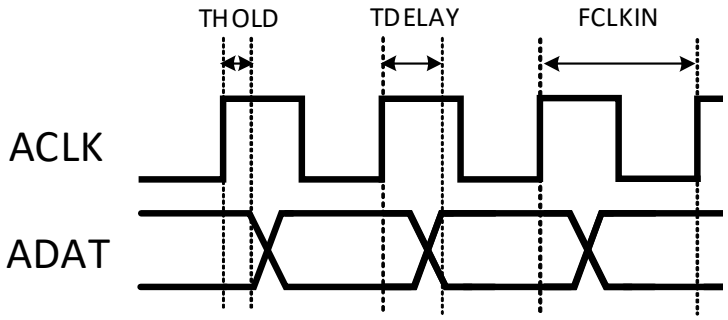


Figure 6. Si8941 Clock Input

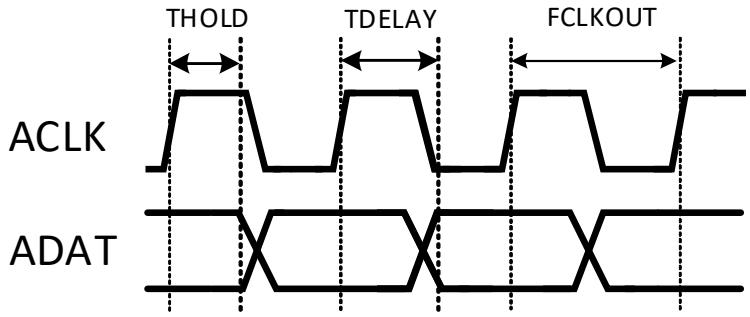


Figure 7. Si8946/47 Clock Output

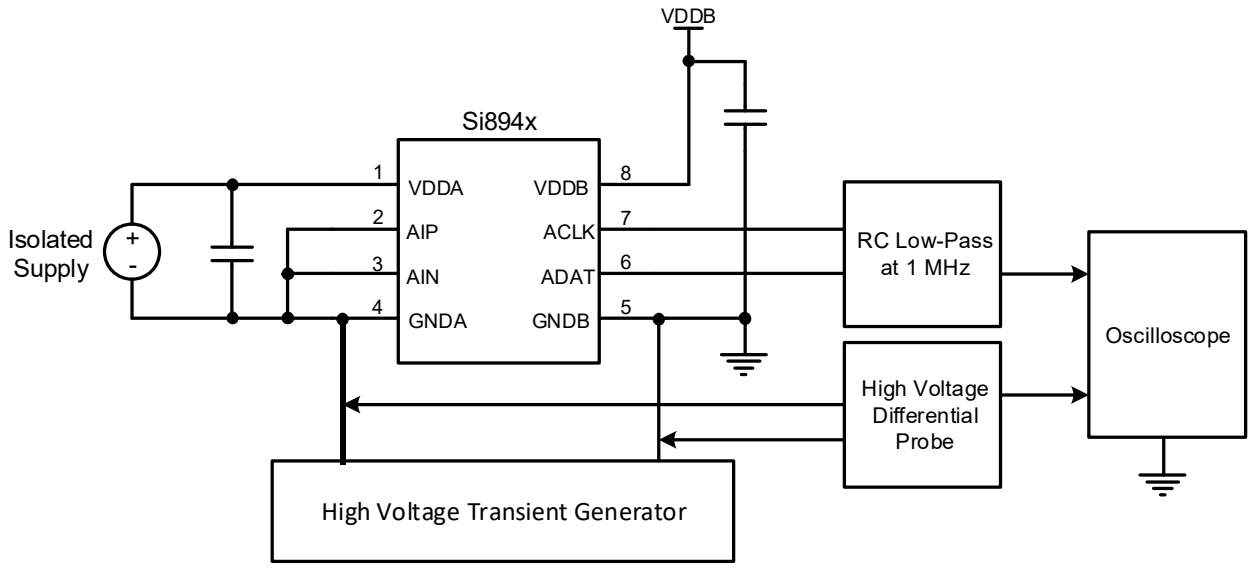


Figure 8. Common-Mode Transient Immunity Characterization Circuit

4. Typical Performance Characteristics

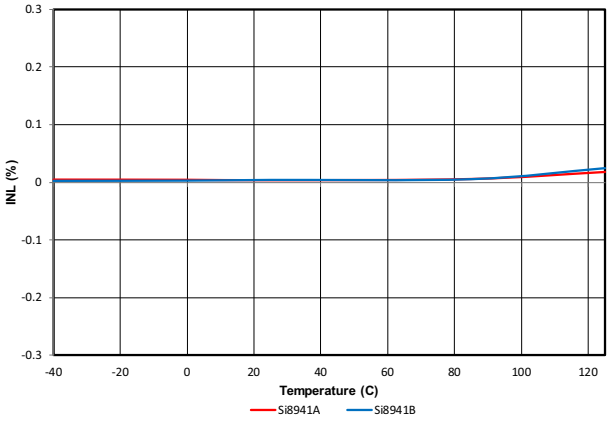


Figure 9. Si8941 Nonlinearity (%) vs. Temperature (°C)

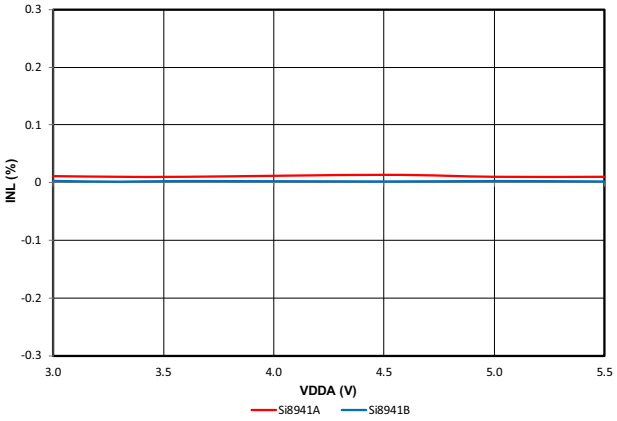


Figure 10. Si8941 Nonlinearity (%) vs. VDDA Supply (V)

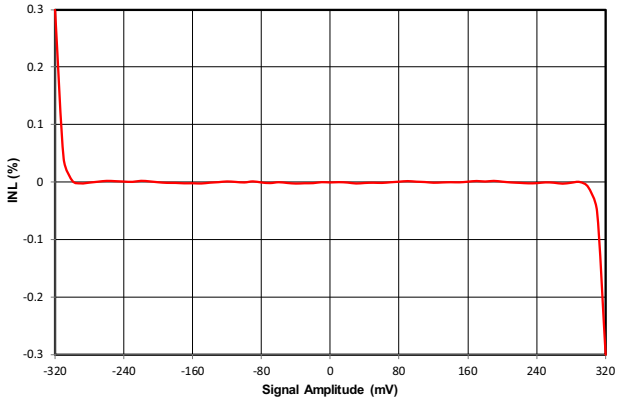


Figure 11. Si8941B Nonlinearity (%) vs. Input Signal Amplitude (mV)

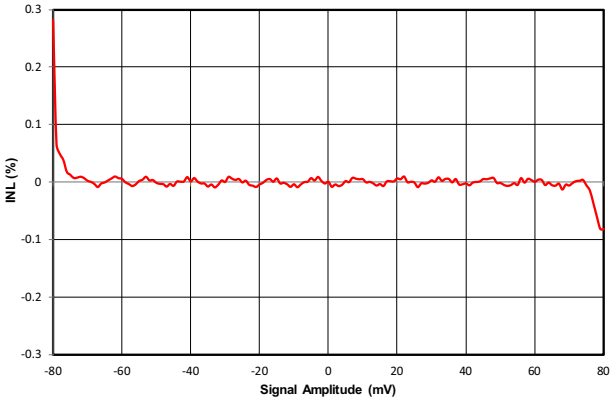


Figure 12. Si8941A Nonlinearity (%) vs. Input Signal Amplitude (mV)

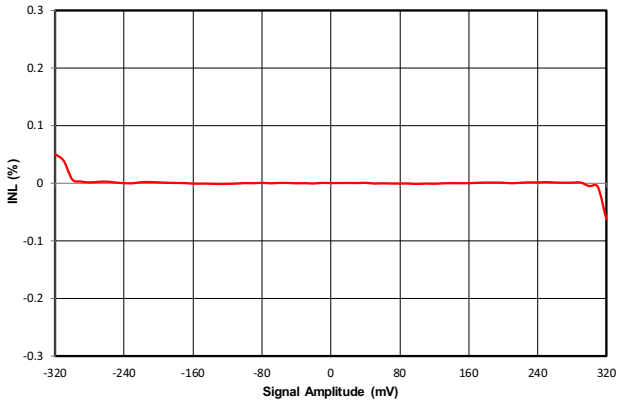


Figure 13. Si8946B Nonlinearity (%) vs. Input Signal Amplitude (mV)

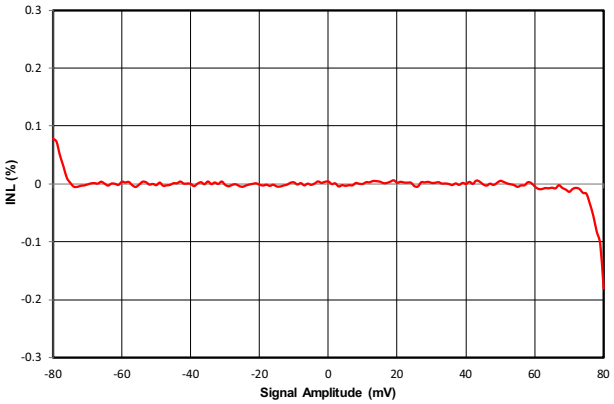


Figure 14. Si8946A Nonlinearity (%) vs. Input Signal Amplitude (mV)

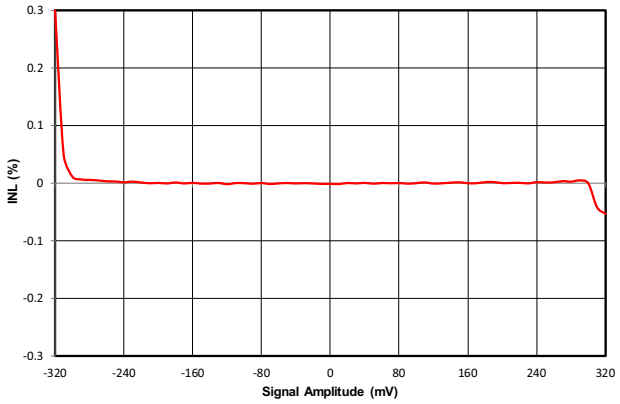


Figure 15. Si8947B Nonlinearity (%) vs. Input Signal Amplitude (mV)

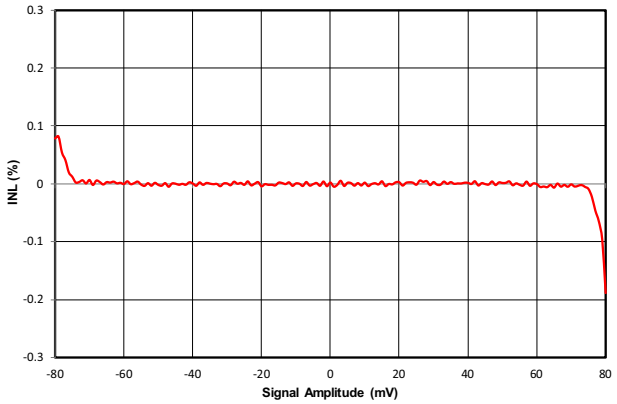


Figure 16. Si8947A Nonlinearity (%) vs. Input Signal Amplitude (mV)

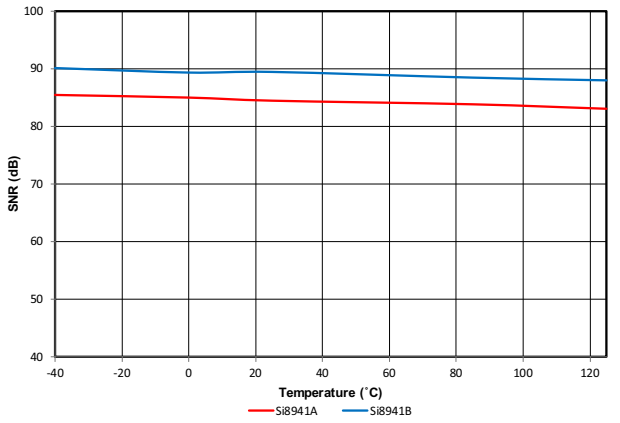


Figure 17. Si8941 Signal-to-Noise Ratio (dB) vs. Temperature (°C)

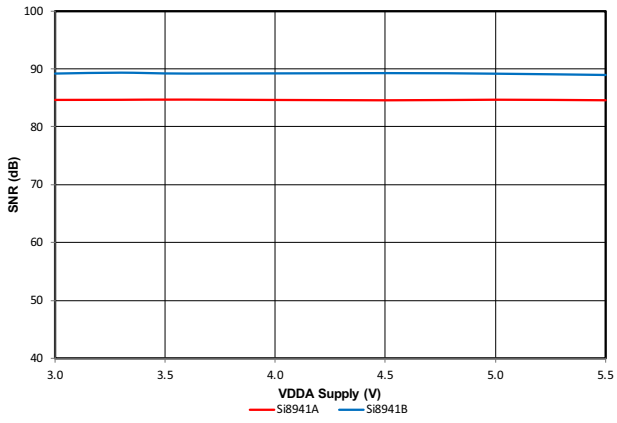


Figure 18. Si8941 Signal-to-Noise Ratio (dB) vs. VDDA Supply (V)

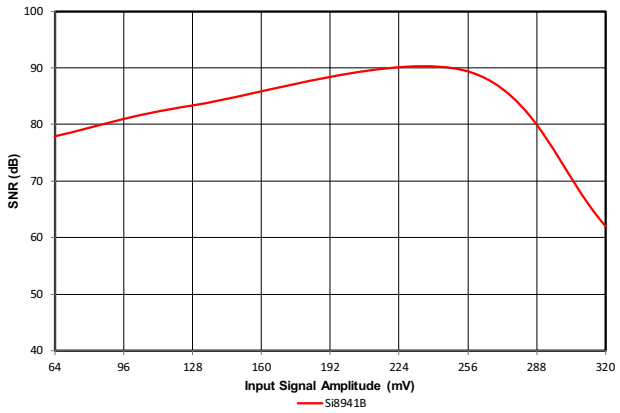


Figure 19. Si8941B Signal-to-Noise Ratio (dB) vs. Input Signal Amplitude (mV)

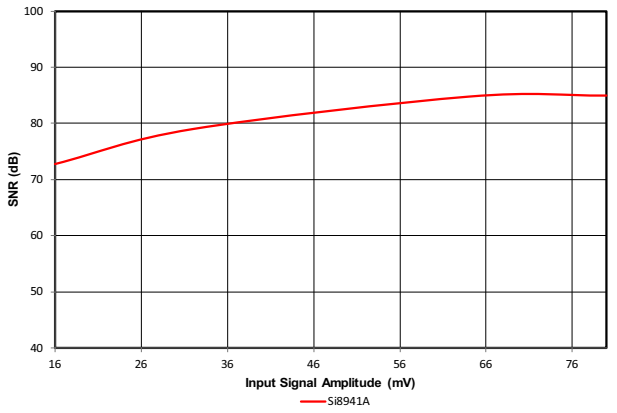


Figure 20. Si8941A Signal-to-Noise Ratio (dB) vs. Input Signal Amplitude (mV)

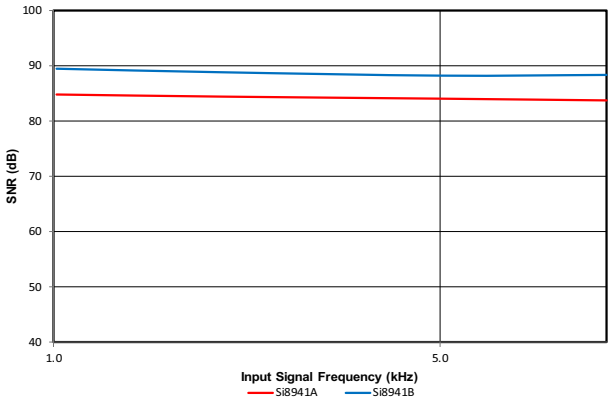


Figure 21. Si8941 Signal-to-Noise Ratio (dB) vs. Input Signal Frequency (kHz)

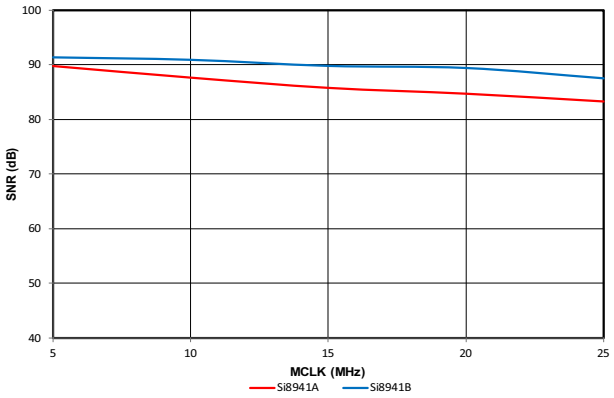


Figure 22. Si8941 Signal-to-Noise Ratio (dB) vs. MCLK (MHz)

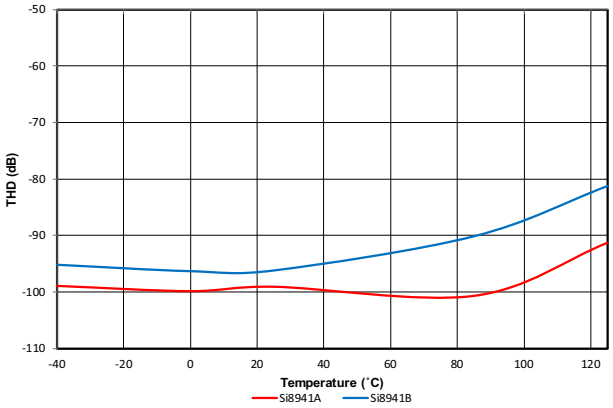


Figure 23. Si8941 Total Harmonic Distortion (dB) vs. Temperature (°C)

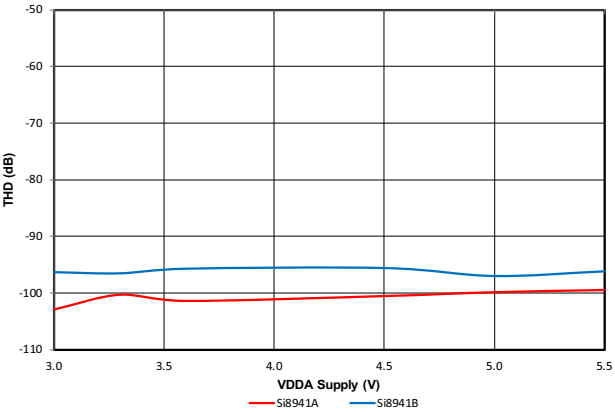


Figure 24. Si8941 Total Harmonic Distortion (dB) vs. VDDA Supply (V)

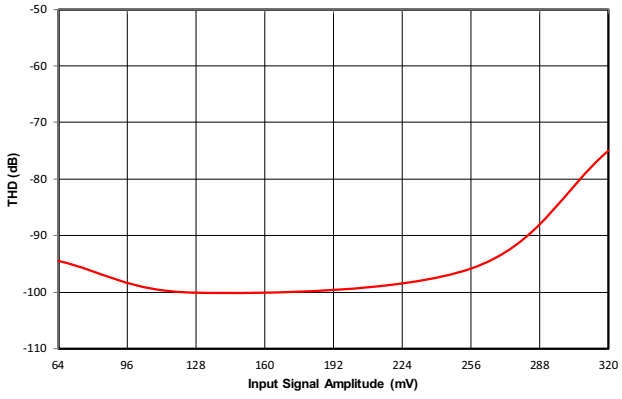


Figure 25. Si8941B Total Harmonic Distortion (dB) vs. Input Signal Amplitude (mV)

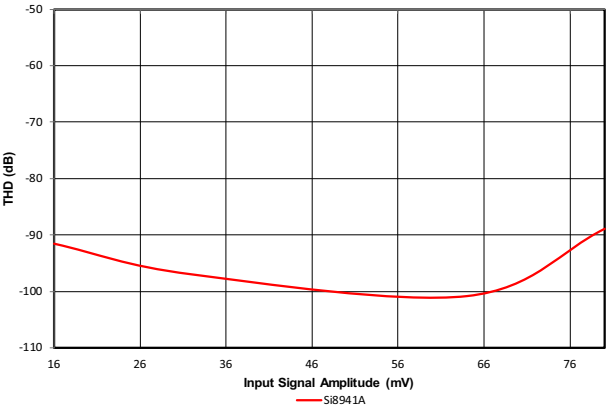


Figure 26. Si8941A Total Harmonic Distortion (dB) vs. Input Signal Amplitude (mV)

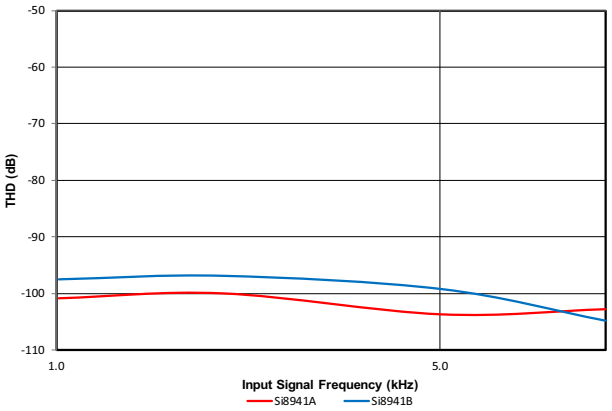


Figure 27. Si8941 Total Harmonic Distortion (dB) vs. Input Signal Frequency (kHz)

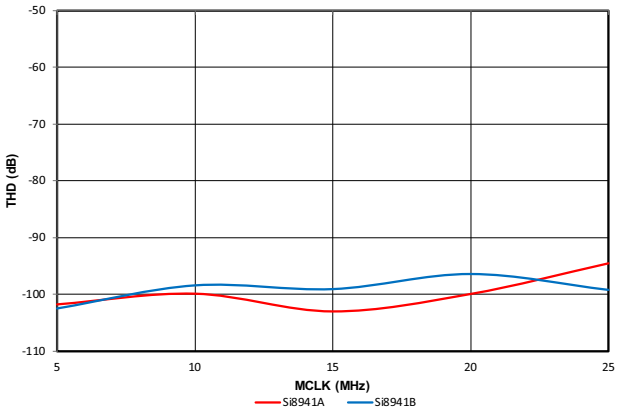


Figure 28. Si8941 Total Harmonic Distortion (dB) vs. MCLK (MHz)

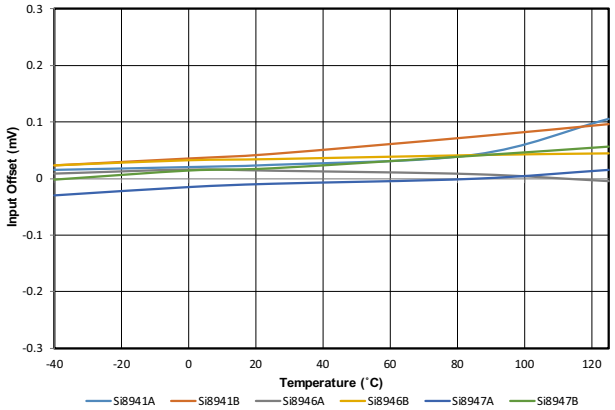


Figure 29. Input Offset (mV) vs. Temperature (°C)

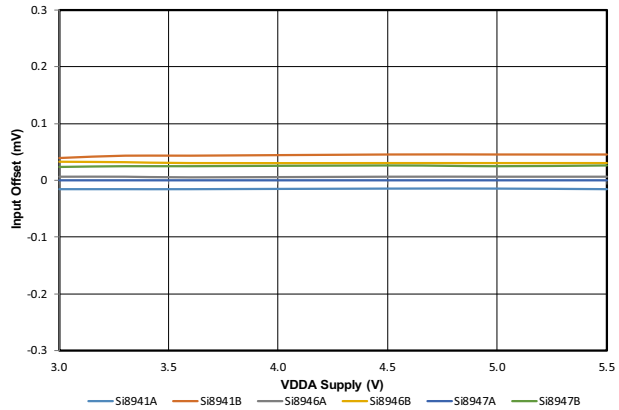


Figure 30. Input Offset (mV) vs. VDDA Supply (V)

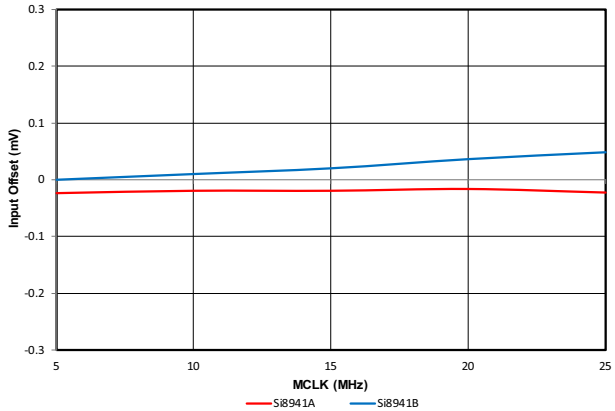


Figure 31. Si8941 Input Offset (mV) vs. MCLK (MHz)

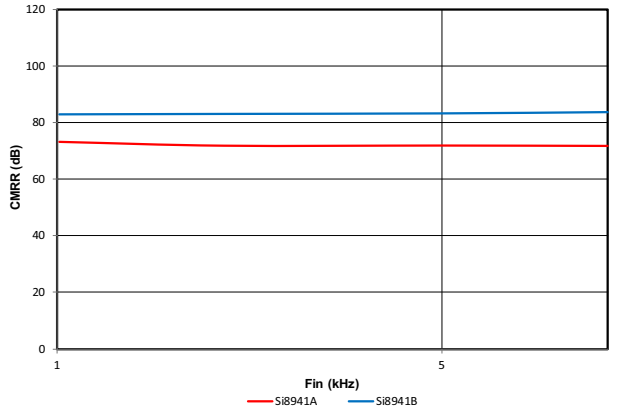


Figure 32. Si8941 Common-Mode Rejection Ratio (dB) vs. Input Signal Frequency (kHz)

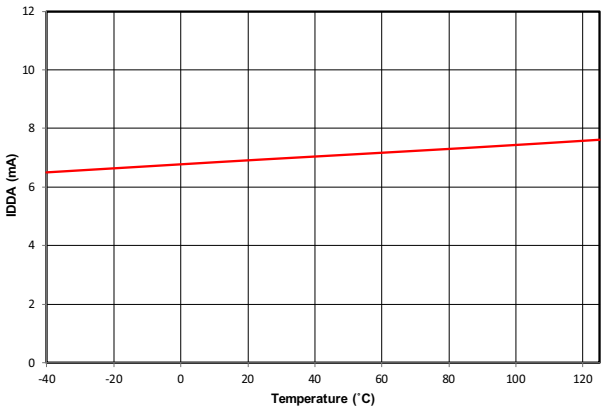


Figure 33. IDDA (mA) vs. Temperature (°C)

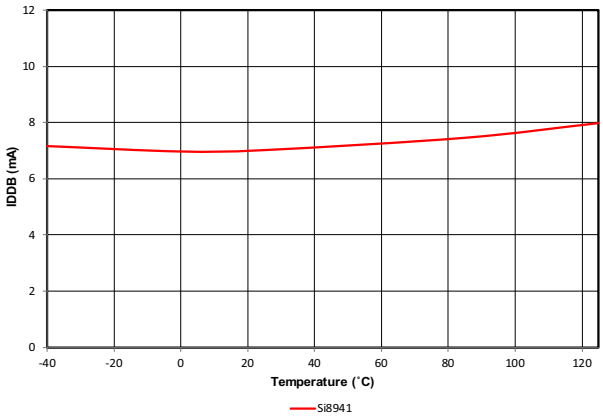


Figure 34. Si8941 IDDB (mA) vs. Temperature (°C)

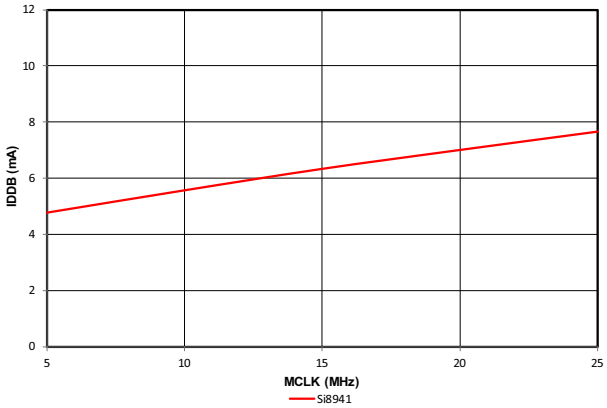


Figure 35. Si8941 IDDB (mA) vs. MCLK (MHz)

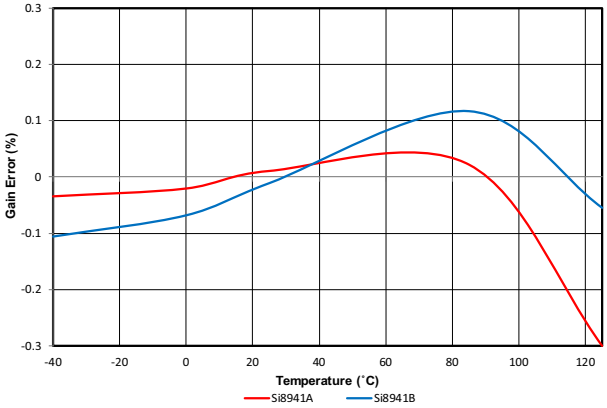


Figure 36. Si8941 Gain Error (%) vs. Temperature (°C)

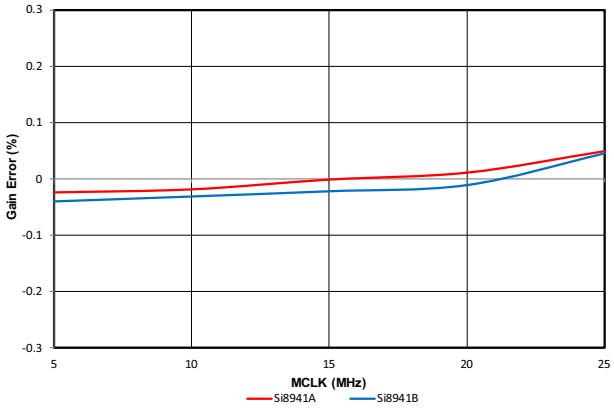


Figure 37. Si8941 Gain Error (%) vs. MCLK (MHz)

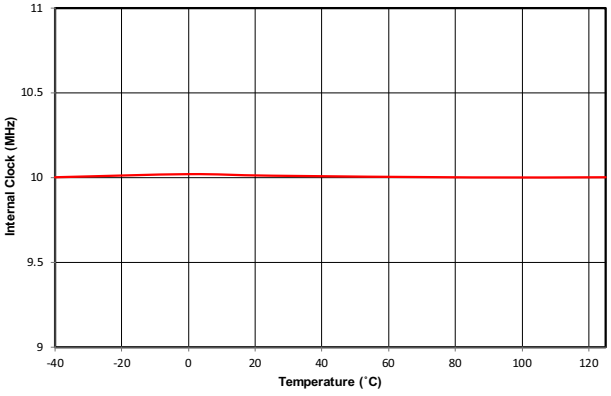


Figure 38. Si8946 Internal Clock Frequency (MHz) vs. Temperature (°C)

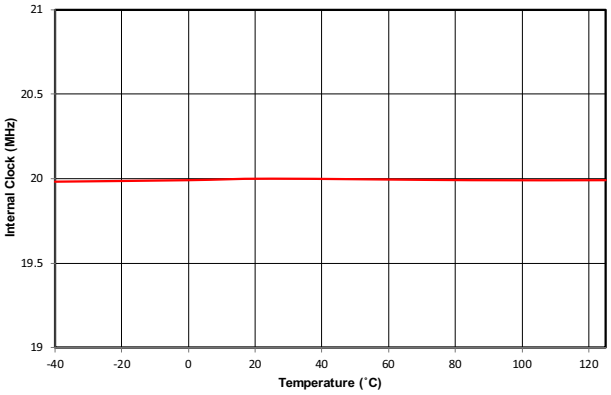


Figure 39. Si8947 Internal Clock Frequency (MHz) vs. Temperature (°C)

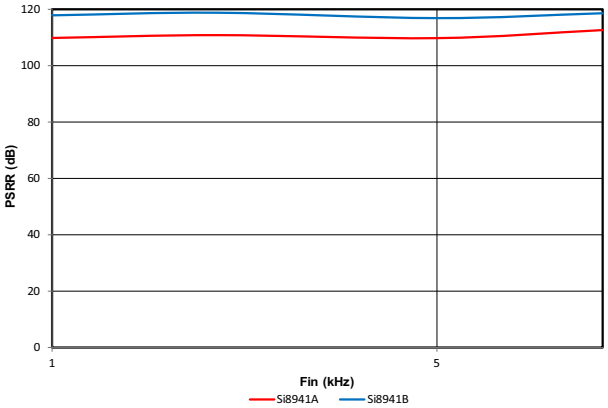


Figure 40. Si8941 Power Supply Rejection Ratio (dB) vs. Input Signal Frequency (kHz)

5. Safety Certifications and Specifications

Table 5. Regulatory Information[1]

CSA
The Si8941/Si8946/Si8947 is certified under CSA. For more details, see Master Contract File 232873.
62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
VDE
The Si8941/Si8946/Si8947 is certified under VDE. For more details, see File 5028467.
60747-17: Up to 2121 V_{peak} for reinforced insulation working voltage.
UL
The Si8941/Si8946/Si8947 is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} V_{ISO} isolation voltage for basic protection.
CQC
The Si8941/Si8946/Si8947 is certified under GB4943.1.
Rated up to 250 V_{RMS} reinforced insulation working voltage at 5000 meters tropical climate.

1. For more information, see Section 15. Ordering Information

Table 6. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			WB Stretched SOIC-8	NB SOIC-8	
Nominal external air gap (clearance)	CLR		8.0	4.0	mm
Nominal external tracking (creepage)	CRP		8.0	4.0	mm
Minimum internal gap (internal clearance)	DTI		0.036	0.036	mm
Tracking resistance	PTI or CTI	IEC60112	600	600	V_{RMS}
Erosion depth	ED		0.04	0.04	mm
Resistance (input-output)[1]	R_{IO}	Test voltage = 500 V, 25 °C	10^{12}	10^{12}	Ω
Capacitance (input-output)[1]	C_{IO}	f = 1 MHz	1	1	pF

1. To determine resistance and capacitance, the Si8941/Si8946/Si8947 is converted into a two-terminal device. Pins 1 to 4 are shorted together to form the first terminal, and pins 5 to 8 are shorted together to form the second terminal. The parameters are then measured between these two terminals.

Table 7. IEC 60664-1 Ratings

Parameter	Test Conditions	Specification	
		WB Stretched SOIC-8	NB SOIC-8
Material group		I	I
Overvoltage category	Rated mains voltage ≤150 V_{RMS}	I-IV	I-IV
	Rated mains voltage ≤300 V_{RMS}	I-IV	I-III
	Rated mains voltage ≤600 V_{RMS}	I-IV	I-II
	Rated mains voltage ≤1000 V_{RMS}	I-III	I

Table 8. IEC 60747-17 Insulation Characteristics[1]

Parameter	Symbol	Test Condition	Characteristic		Unit
			WB Stretched SOIC-8	NB SOIC-8	
Maximum working isolation voltage	V_{IOWM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	1500	445	V_{RMS}
Maximum repetitive isolation voltage	V_{IORM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	2121	630	V_{peak}
Apparent charge	q_{pd}	Method b: At routine test (100% production) and preconditioning (type test); V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 x V_{IORM}, t_m = 1 s (method b1) or $V_{pd(m)}$ = V_{ini}, t_m = t_{ini} (method b2)	≤5	≤5	pC
Maximum transient isolation voltage	V_{IOTM}	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	7070	3535	V_{peak}
Maximum surge isolation voltage	V_{IOSM}	Tested in oil with 1.3 x V_{IMP} or 10 kV minimum and 1.2 µs/50 µs profile	10400	10400	V_{peak}
Maximum impulse voltage	V_{IMP}	Tested in air with 1.2 µs/50 µs profile	8000	5000	V_{peak}
Isolation resistance	R_{IO_S}	T_{AMB} = T_S, V_{IO} = 500 V	$>10^9$	$>10^9$	Ω
Pollution degree			2	2	
Climatic category			40/125/21	40/125/21	

1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 9. UL 1577 Insulation Characteristics

Parameter	Symbol	Test Condition	Characteristic		Unit
			WB Stretched SOIC-8	NB SOIC-8	
Maximum withstanding isolation voltage	V_{ISO}	V_{TEST} = V_{ISO}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{ISO}, t = 1 s (100% production)	5000	2500	V_{RMS}

Table 10. IEC 60747-17 Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Characteristic	Unit
Safety temperature	T_S		150	°C
Safety input, output or supply current (WB stretched SOIC-8)	I_S	θ_{JA} = 90 °C/W V_{DD} = 5.5 V T_J = 150 °C T_A = 25 °C	253	mA
		θ_{JA} = 90 °C/W V_{DD} = 3.6 V T_J = 150 °C T_A = 25 °C	386	mA
Safety input, output or supply current (NB SOIC-8)	I_S	θ_{JA} = 112 °C/W V_{DD} = 5.5 V T_J = 150 °C T_A = 25 °C	203	mA
		θ_{JA} = 112 °C/W V_{DD} = 3.6 V T_J = 150 °C T_A = 25 °C	310	mA
Safety input, output or total power (WB stretched SOIC-8)	P_S	θ_{JA} = 90 °C/W T_J = 150 °C T_A = 25 °C	1389	mW
Safety input, output or total power (NB SOIC-8)	P_S	θ_{JA} = 112 °C/W T_J = 150 °C T_A = 25 °C	1116	mW

1. Maximum value allowed in the event of a failure. Refer to the derating curves Figure 41, "WB Stretched SOIC-8 Thermal Derating Curve (Dependence of Safety Limiting Current)," on page 19 and Figure 42, "NB SOIC-8 Thermal Derating Curve (Dependence of Safety Limiting Current)," on page 20.

Table 11. Thermal Characteristics

Parameter	Symbol	WB Stretched SOIC-8	NB SOIC-8	Unit
IC Junction-to-air thermal resistance	θ_{JA}	90	112	°C/W

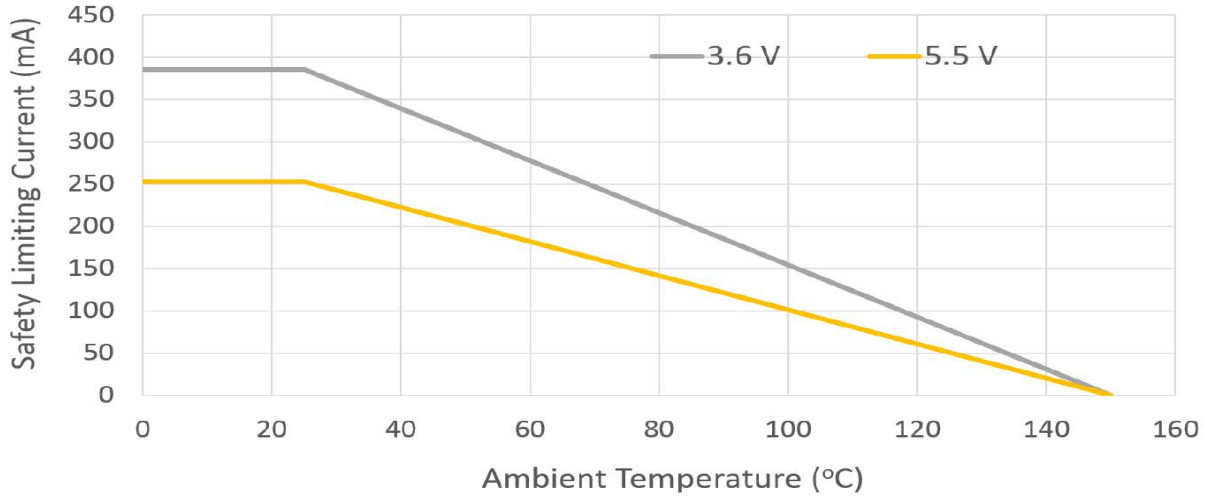


Figure 41. WB Stretched SOIC-8 Thermal Derating Curve (Dependence of Safety Limiting Current)

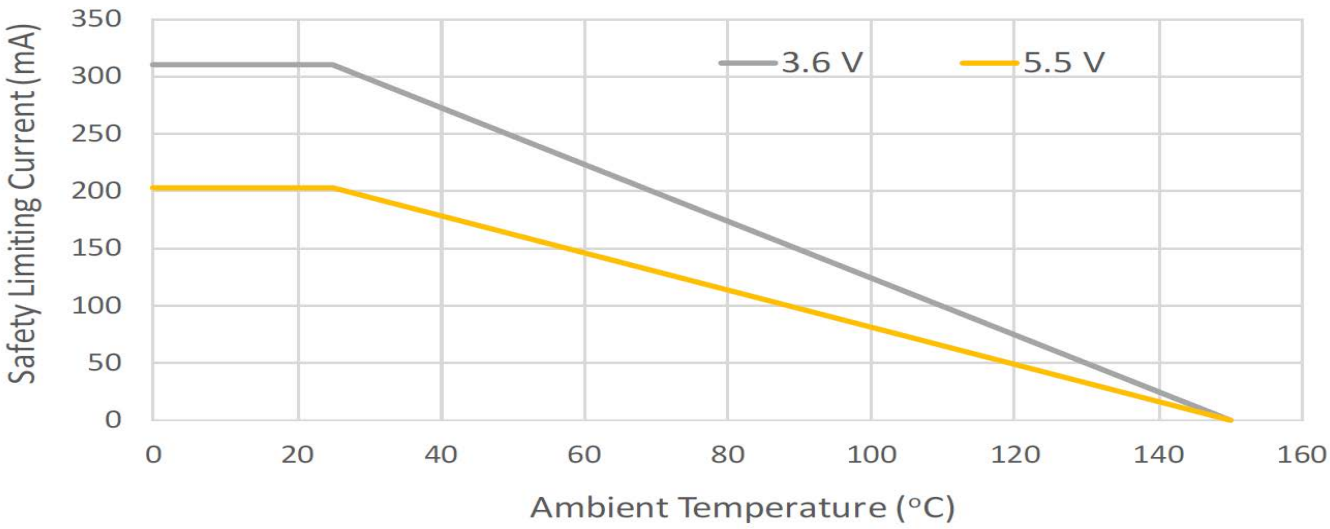


Figure 42. NB SOIC-8 Thermal Derating Curve (Dependence of Safety Limiting Current)

6. Package Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The Si8941AD-IS4, Si8941BD-IS4, Si8946AD-IS4, Si8946BD-IS4, Si8947AD-IS4, Si8947BD-IS4, Si8941AD-AS4, Si8941BD-AS4, Si8946AD-AS4, Si8946BD-AS4, Si8947AD-AS4, and Si8947BD-AS4 are rated to Moisture Sensitivity Level 2A (MSL2A) at 260°C.

The Si8941AB-IS, Si8941BB-IS, Si8946AB-IS, Si8946BB-IS, Si8947AB-IS, Si8947BB-IS, Si8941AB-AS, Si8941BB-AS, Si8946AB-AS, Si8946BB-AS, Si8947AB-AS, Si8947BB-AS are rated to MSL 2 at 260°C.

They can be used for lead or lead-free soldering. For additional information, refer to Skyworks Application Note, “PCB Design and SMT Assembly/Rework Guidelines,” Document Number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Refer to Standard SMT Reflow Profiles: JEDEC Standard J-STD-020.

7. Package Outline: 8-Pin Wide Body Stretched SOIC

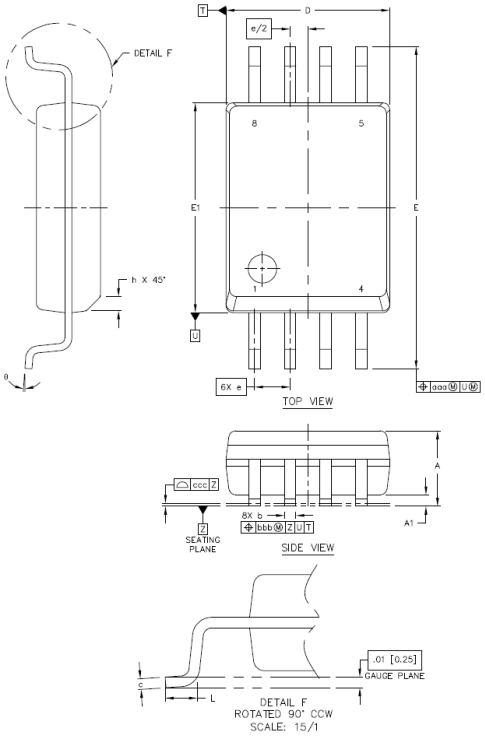


Figure 43. 8-Pin Wide Body Stretched SOIC Package

Table 12. 8-Pin Wide Body Stretched SOIC Package Dimensions

Dimension	Millimeters		Notes
	Min	Max	
A	2.49	2.79	Dimensioning and tolerancing per ANSI Y14.5M-1994. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.
A1	0.36	0.46	
b	0.30	0.51	
c	0.20	0.33	
D	5.74	5.94	
E	11.25	11.76	
E1	7.39	7.59	
e	1.27 BSC		
L	0.51	1.02	
h	0.25	0.76	
θ	0°	8°	
aaa		0.25	
bbb		0.25	
ccc		0.10	

8. Package Outline: 8-Pin Narrow Body SOIC

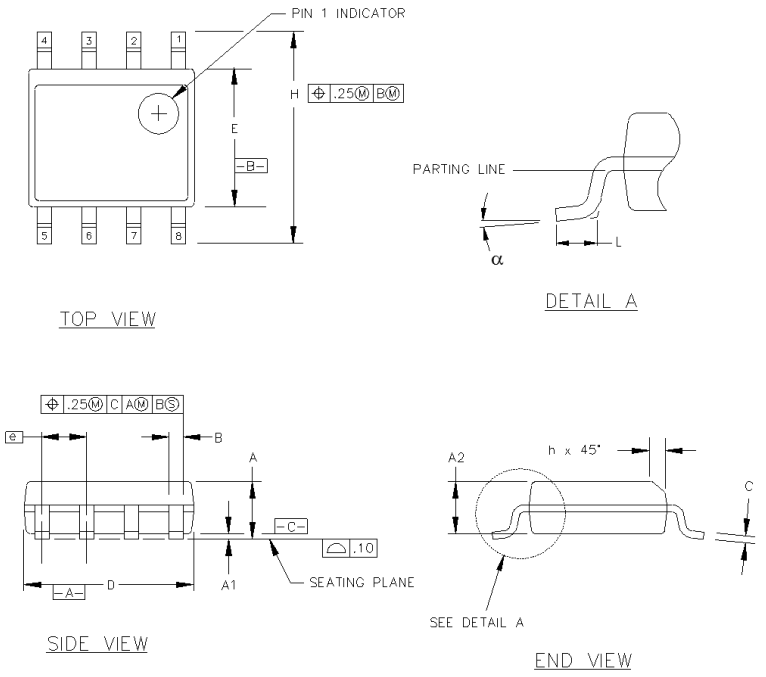


Figure 44. 8-Pin Narrow Body SOIC Package

Table 13. 8-Pin Narrow Body SOIC Package Dimensions

Dimension	Millimeters		Notes
	Min	Max	
A	1.35	1.75	Dimensioning and tolerancing per ANSI Y14.5M-1982. This drawing conforms to JEDEC Outline MS-012. Recommended card reflow profile is per the JEDEC/IPC J-STD-020B specification for small body components.
A1	0.10	0.25	
A2	1.40 REF	1.55 REF	
B	0.33	0.51	
C	0.19	0.25	
D	4.80	5.00	
E	3.80	4.00	
e	1.27 BSC		
H	5.80	6.20	
h	0.25	0.50	
L	0.40	1.27	
α	0°	8°	

9. Land Pattern: 8-Pin Wide Body Stretched SOIC

General Guidelines

1. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a fabrication allowance of 0.05 mm.
2. This land pattern design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD).
2. Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.

Card Assembly

1. A No-clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

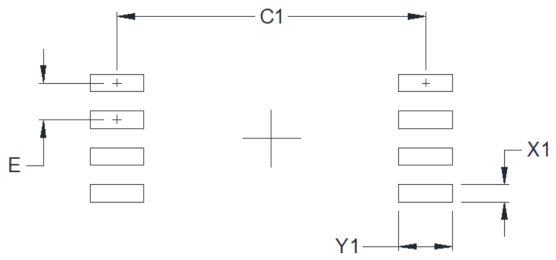


Figure 45. 8-Pin Wide Body Stretched SOIC Land Pattern

Table 14. 8-Pin Wide Body Stretched SOIC Land Pattern Dimensions[1]

Dimension	(mm)
C1	10.60
E	1.27
X1	0.60
Y1	1.85

1. See General Guidelines

10. Land Pattern: 8-Pin Narrow Body SOIC

General Guidelines

1. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.
2. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).

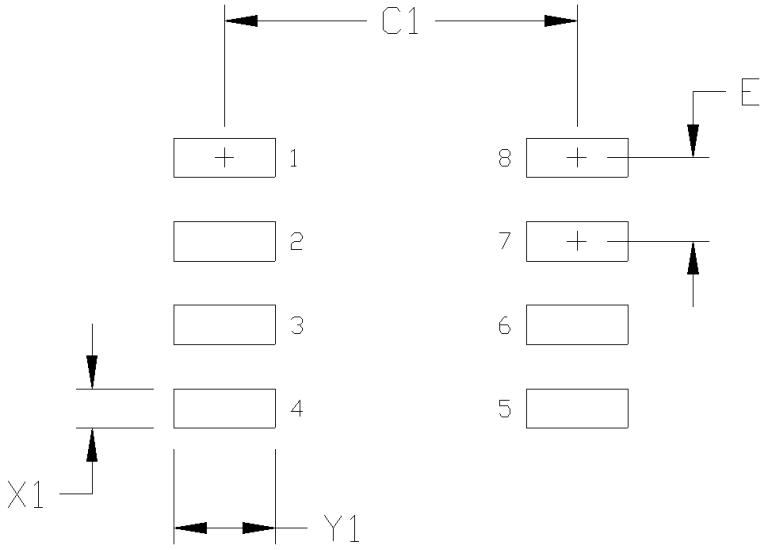


Figure 46. 8-Pin Narrow Body SOIC Land Pattern

Table 15. 8-Pin Narrow Body SOIC Land Pattern Dimensions[1]

Dimension	mm
C1	5.40
E	1.27
X1	0.60
Y1	1.55

1. See General Guidelines

11. Top Marking: 8-Pin Wide Body Stretched SOIC

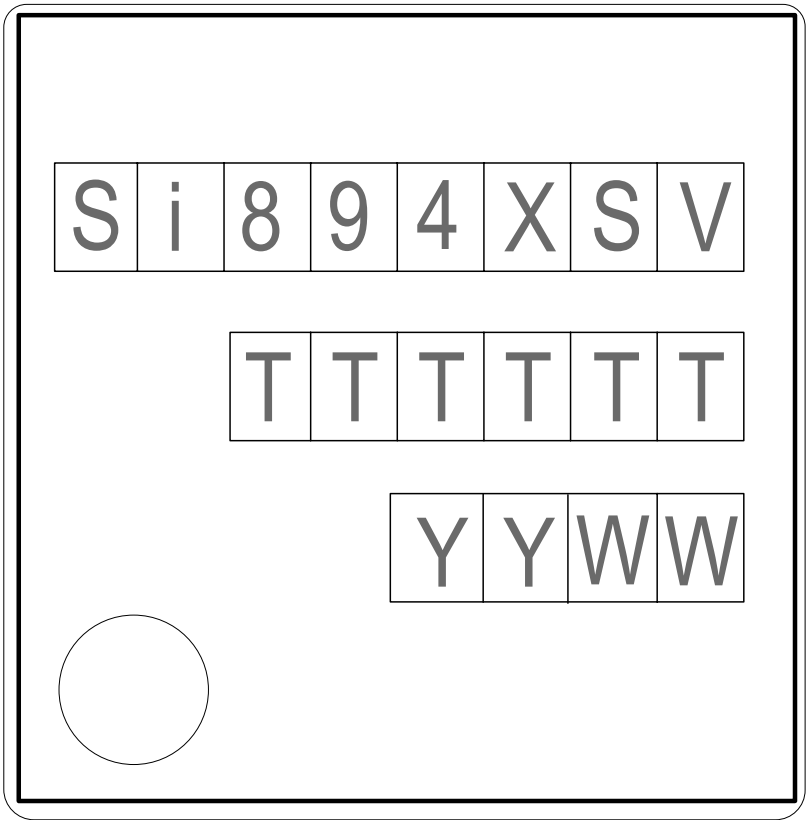


Figure 47. Si894x Typical Package Marking, 8-Pin Wide Body Stretched SOIC

Table 16: 8-Pin Wide Body Stretched SOIC Top Marking Explanation

Line 1	Part Number	Si8941 or Si8946 or Si8947 Delta-Sigma Modulators X = Clock Source/Speed 1 = External (Si8941) 6 = Internal 10 MHz (Si8946) 7 = Internal 20 MHz (Si8947) S = Input range: A = ±62.5 mV B = ±250 mV V = Insulation rating: D = 5.0 kV_{RMS}
Line 2	TTTTTT	Manufacturing code
Line 3	YY = Year WW = Work Week Circle = 43 mils diameter left justified	Year and work week

12. Top Marking: 8-Pin Narrow Body SOIC

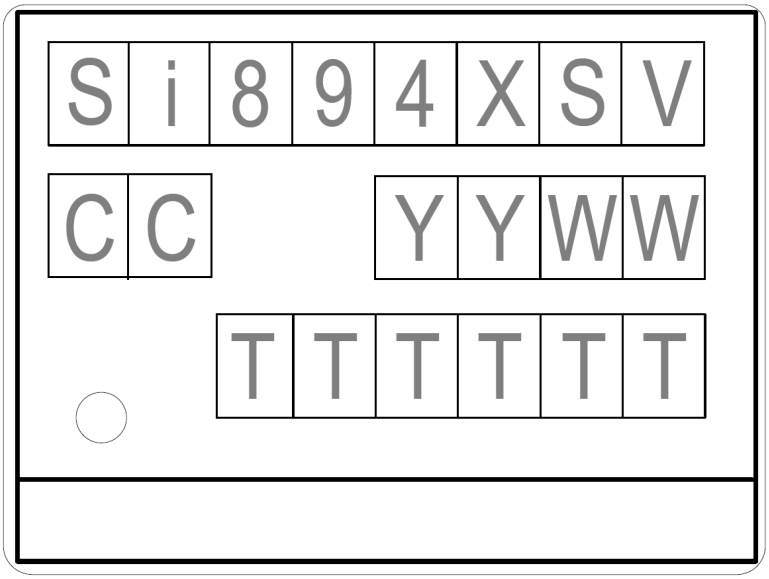
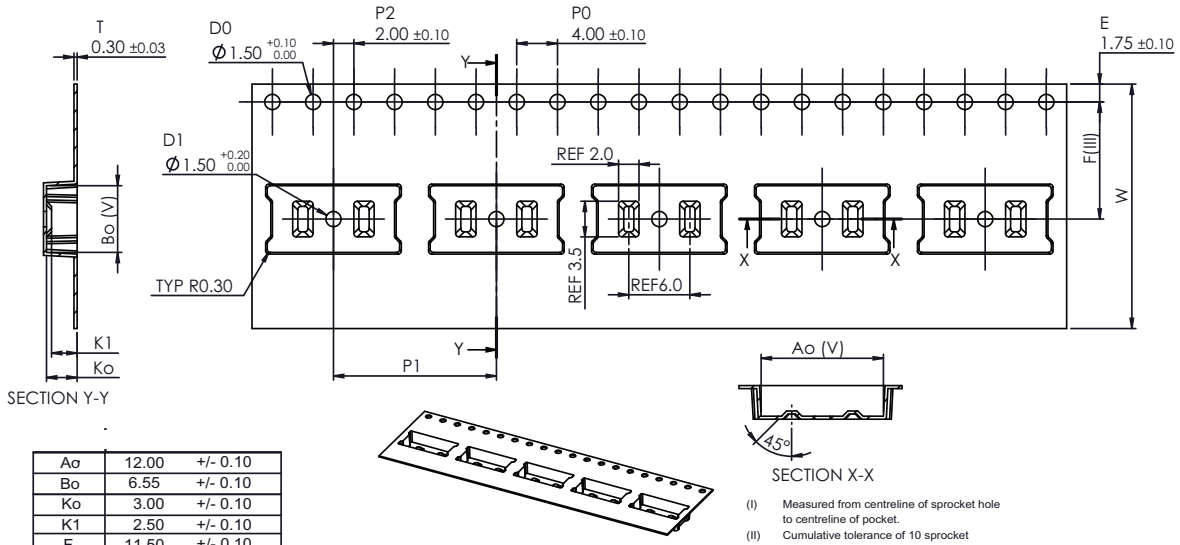


Figure 48. Si894x Typical Package Marking, 8-Pin Narrow Body SOIC

Table 17. 8-Pin Narrow Body SOIC Top Marking Explanation

Line 1	Part Number	Si8941 or Si8946 or Si8947 Delta-Sigma Modulators X = Clock Source/Speed 1 = External (Si8941) 6 = Internal 10 MHz (Si8946) 7 = Internal 20 MHz (Si8947) S = Input range: A = ±62.5 mV B = ±250 mV V = Insulation rating B = 2.5 kV_{RMS}
Line 2	CC = Country of origin ISO code abbreviation	
	YY = Year WW = Work Week	Year and work week
Line 3	Circle = 19.7 mils diameter left justified	Manufacturing code

13. Tape and Reel Information, Wide Body



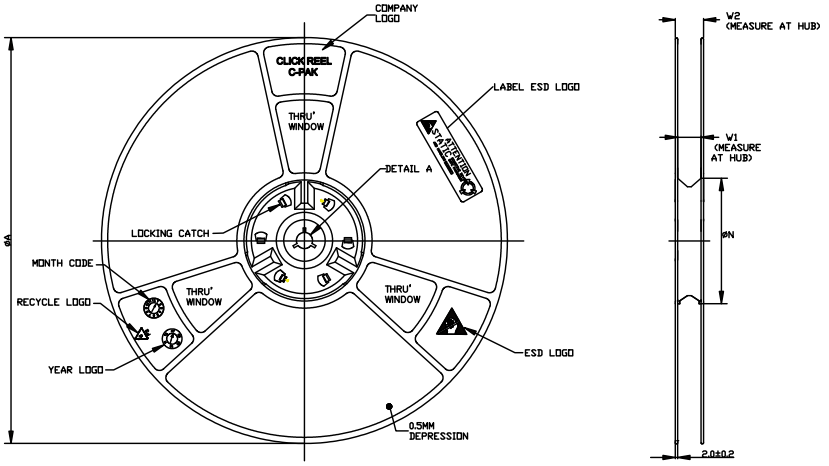
Aσ	12.00	+/- 0.10
Bo	6.55	+/- 0.10
Ko	3.00	+/- 0.10
K1	2.50	+/- 0.10
F	11.50	+/- 0.10
P1	16.00	+/- 0.10
W	24.15	+/- 0.10

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Dimension is determined by C value for pocekt base with typical radius 0.2

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

206440-039a

Figure 49. Wide Body Carrier Tape Information

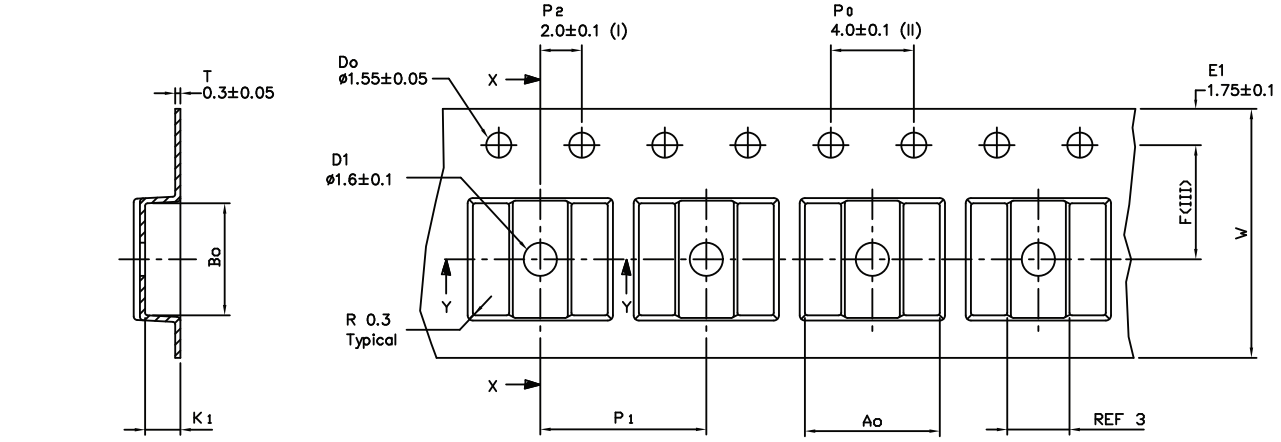


CARRIER TAPE WIDTH
24.15 MM ±0.10 MM

206440-040a

Figure 50. Wide Body Reel Information

14. Tape and Reel Information, Narrow Body



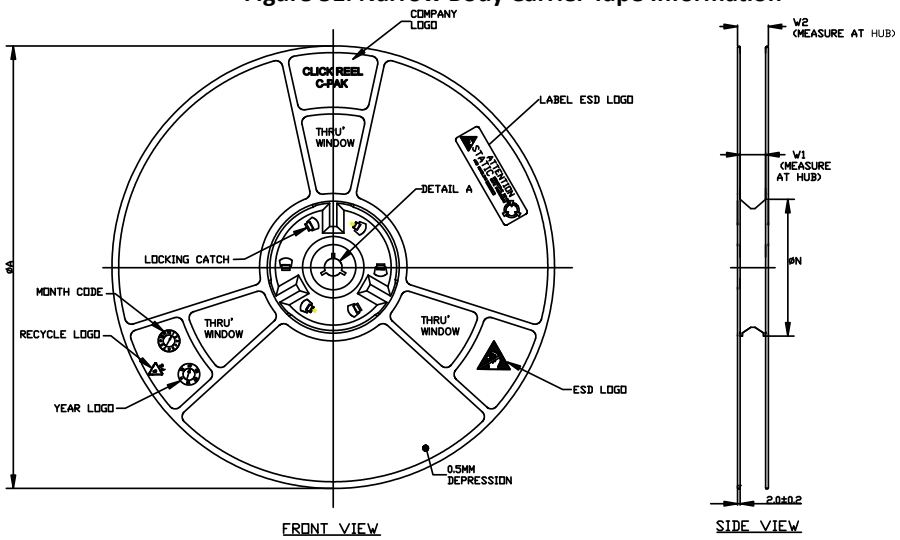
Ao	6.50 +/− 0.1
Bo	5.40 +/− 0.1
Ko	2.00 +/− 0.1
K1	1.70 +/− 0.1
F	5.50 +/− 0.1
P1	8.00 +/− 0.1
W	12.00 +0.3/−0.0

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

206440-044a

Figure 51. Narrow Body Carrier Tape Information



CARRIER TAPE WIDTH
12.00 MM +0.3 -0.0 MM

206440-045

Figure 52. Narrow Body Reel Information

15. Ordering Information

Industrial and Automotive Grade Ordering Part Numbers (OPNs)

Industrial-grade devices (part numbers with an "-I" in their suffix) are built using well-controlled, high-quality manufacturing flows to ensure robustness and reliability. Qualifications are compliant with JEDEC, and defect reduction methodologies are used throughout definition, design, evaluation, qualification, and mass production steps.

Automotive-grade devices (part numbers with an "-A" in their suffix) are built using automotive-specific flows at all steps in the manufacturing process to ensure robustness and low defectivity. These devices are supported with AIAG-compliant Production Part Approval Process (PPAP) documentation, and feature International Material Data System (IMDS) and China Automotive Material Data System (CAMDS) listings. Qualifications are compliant with AEC-Q100, and a zero-defect methodology is maintained throughout definition, design, evaluation, qualification, and mass production steps.

Ordering Part Number[1, 2, 3]	Automotive Ordering Part Number[1, 2, 3, 4, 5]	Ordering Options			
		Specified Input Range	Isolation Rating	Clock	Package Type
Si8941AD-IS4	Si8941AD-AS4	±62.5 mV	5.0 kV_{RMS}	Input	WB stretched SOIC-8
Si8941BD-IS4	Si8941BD-AS4	±250 mV	5.0 kV_{RMS}	Input	WB stretched SOIC-8
Si8946AD-IS4	SI8946AD-AS4	±62.5 mV	5.0 kV_{RMS}	10 MHz output	WB stretched SOIC-8
Si8946BD-IS4	SI8946BD-AS4	±250 mV	5.0 kV_{RMS}	10 MHz output	WB stretched SOIC-8
Si8947AD-IS4	SI8947AD-AS4	±62.5 mV	5.0 kV_{RMS}	20 MHz output	WB stretched SOIC-8
Si8947BD-IS4	SI8947BD-AS4	±250 mV	5.0 kV_{RMS}	20 MHz output	WB stretched SOIC-8
Si8941AB-IS	Si8941AB-AS	±62.5 mV	2.5 kV_{RMS}	Input	NB SOIC-8
Si8941BB-IS	Si8941BB-AS	±250 mV	2.5 kV_{RMS}	Input	NB SOIC-8
Si8946AB-IS	SI8946AB-AS	±62.5 mV	2.5 kV_{RMS}	10 MHz output	NB SOIC-8
Si8946BB-IS	SI8946BB-AS	±250 mV	2.5 kV_{RMS}	10 MHz output	NB SOIC-8
Si8947AB-IS	SI8947AB-AS	±62.5 mV	2.5 kV_{RMS}	20 MHz output	NB SOIC-8
Si8947BB-IS	SI8947BB-AS	±250 mV	2.5 kV_{RMS}	20 MHz output	NB SOIC-8

1. All packages are RoHS-compliant.
2. "Si" and "SI" are used interchangeably.
3. An "R" at the end of the part number denotes tape and reel packaging option.
4. Automotive-grade devices ("-A" suffix) are identical in construction materials, topside marking, and electrical parameters to their Industrial Grade ("-I suffix") version counterparts. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.
5. In the top markings of each device, the Manufacturing Code represented by "TTTTTT" contains as its first character a letter in the range N through Z to indicate Automotive Grade.

Revision History

Revision B

October 2, 2023

Re-formatted to new standards. Added new text for Automotive Grade products, AEC-Q100 qualification, updated regulatory information, updated absolute maximum note 1, removed not needed IDD minimum specs, added tape and reel information, and added MSL ratings.

Revision 206439A

December, 2022

• Updated decimal-based revision number to alphanumeric code.

Revision 0.8

September, 2022

• Updated Safety Approvals on front page.

• Updated minimum supply currents in Electrical Specifications.

• Updated Regulatory Information.

Revision 0.7

April, 2021

• Updated Applications and Key Features on front page.

• Updated Electrical Specifications after full characterization.

• Added Automotive OPNs to Ordering Guide.

• Updated Insulation and Safety-Related Specifications table.

• Numerous clarifications throughout.

Revision 0.5

March, 2019

• Updated specifications.

• Added narrow body SOIC package.

• Added timing diagram.

Revision 0.1

January, 2018

• Initial release.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View SI8941AD-IS4R on WIN SOURCE
- Skyworks Solutions Inc. Information

Optimize Your Supply Chain with WIN SOURCE Solutions

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- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management