THE DATASHEET OF

SI86S660BC-IS1

DATA SHEET

Si86S6xx/Lxx/Mxx/Qxx/Sxx: Multi-Channel Digital Isolators

Industrial Applications

- Industrial automation systems
- Medical electronics
- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control
- Power inverters
- Communications systems

Automotive Applications

- Onboard chargers
- Battery management systems
- Charging stations
- Traction inverters
- Hybrid electric vehicles
- Battery electric vehicles

Key Features

- High-speed operation: DC to 150 Mbps
- No start-up initialization required
- Wide supply voltage: 2.25 to 5.5 V
- Up to 6000 V_{RMS} isolation
- Reinforced IEC 60747-17 rating
- High electromagnetic immunity
- Low power and sleep mode options
- Tri-state outputs with enable
- Schmitt trigger + CMOS threshold inputs
- Selectable fail-safe mode: Default high- or low-output (ordering option)
- Precise timing (typical)
  - 10 ns propagation delay
  - 3.5 ns pulse width distortion
- Transient Immunity of 100 kV/µs (min)
- AEC-Q100 qualification
- Wide temperature range: –40 to 125 °C
- RoHS-compliant packages
  - WB SOIC-16
  - NB SOIC-16
  - QSOP-16
- Automotive-grade ordering part numbers (OPNs) available
  - AIAG compliant PPAP documentation support
  - IMDS and CAMDS listing support

Safety Regulatory Approvals (Pending)

- UL 1577 recognized
  - Up to 6000 V_{RMS} for 1 minute.
- CSA certification conformity
  - 62368-1, 60601-1 (reinforced insulation)
- VDE certification conformity
  - 60747-17 (reinforced insulation)
- CQC certification approval
  - GB4943.1

Description

Skyworks' family of robust, high-speed, low-power, multi-channel digital isolators are CMOS devices offering substantial data rate, propagation delay, power, size, reliability, and external BOM advantages over legacy isolation technologies. All have CMOS thresholds and Schmitt trigger inputs for high noise immunity and only require VDD bypass capacitors. Data rates up to 150 Mbps are supported, and all devices achieve typical propagation delays of 10 ns. This family includes SPI and QSPI capabilities with direction control pin options. Enable inputs provide a single point control for enabling and disabling outputs. Low power operating modes are provided to optimize power savings.

A sleep mode option is included to help conserve power by shutting down active circuits by external pin control. Options include a choice of isolation ratings (3.75 and 6.0 kV_{RMS}). A fail-safe operating mode controls the default output state during power loss. All products are safety certified by UL, CSA, VDE, and CQC. Products in wide-body packages support voltages of 6.0 kV_{RMS} with one minute withstand capability per UL 1577. Automotive Grade is available. These products are built using automotive specific flows at all steps in the manufacturing process to ensure the robustness and low defectivity required for automotive applications.

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

1. Pin Descriptions

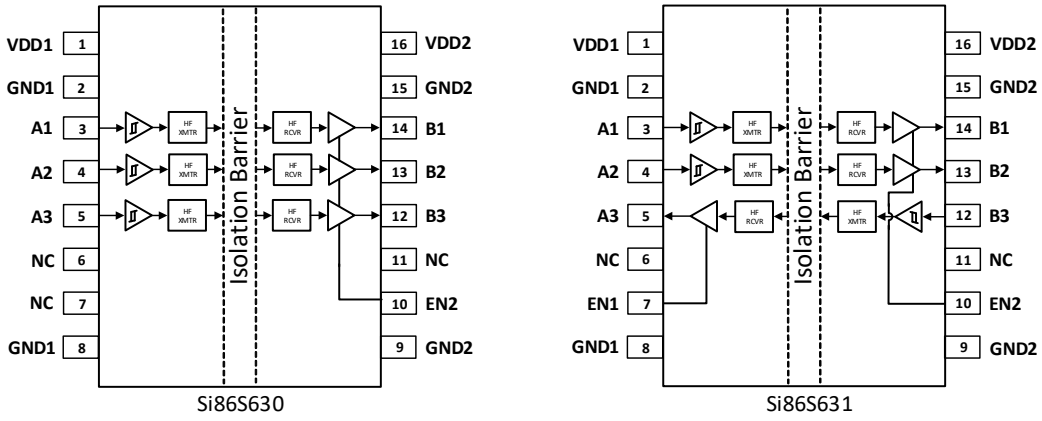

Figure 1. Si86S63x Pinouts

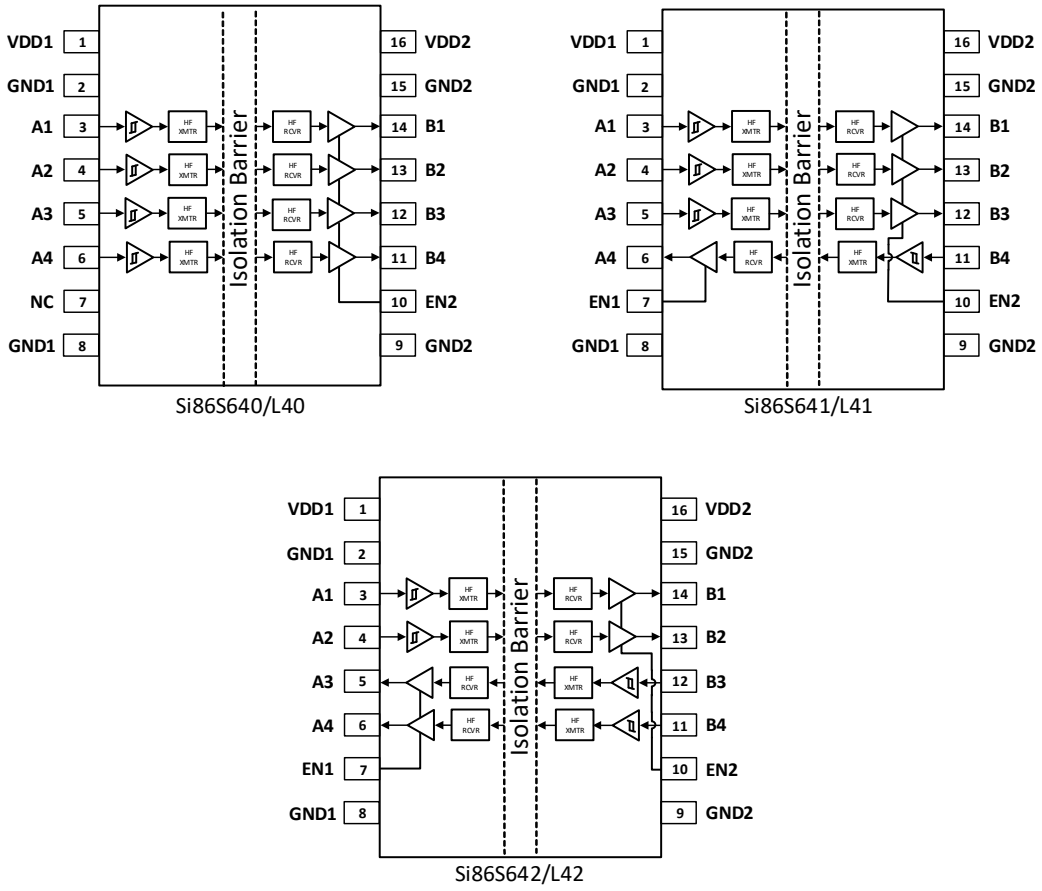

Figure 2. Si86S64x/L4x Pinouts

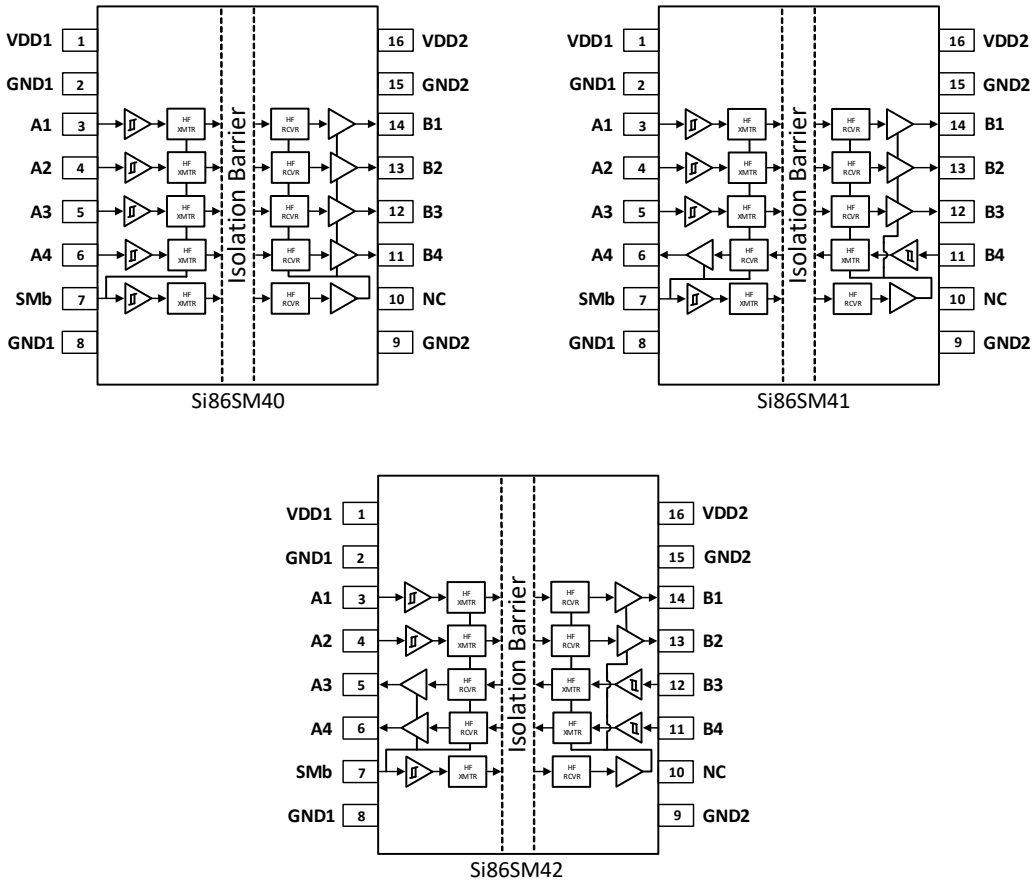

Figure 3. Si86SM4x Pinouts

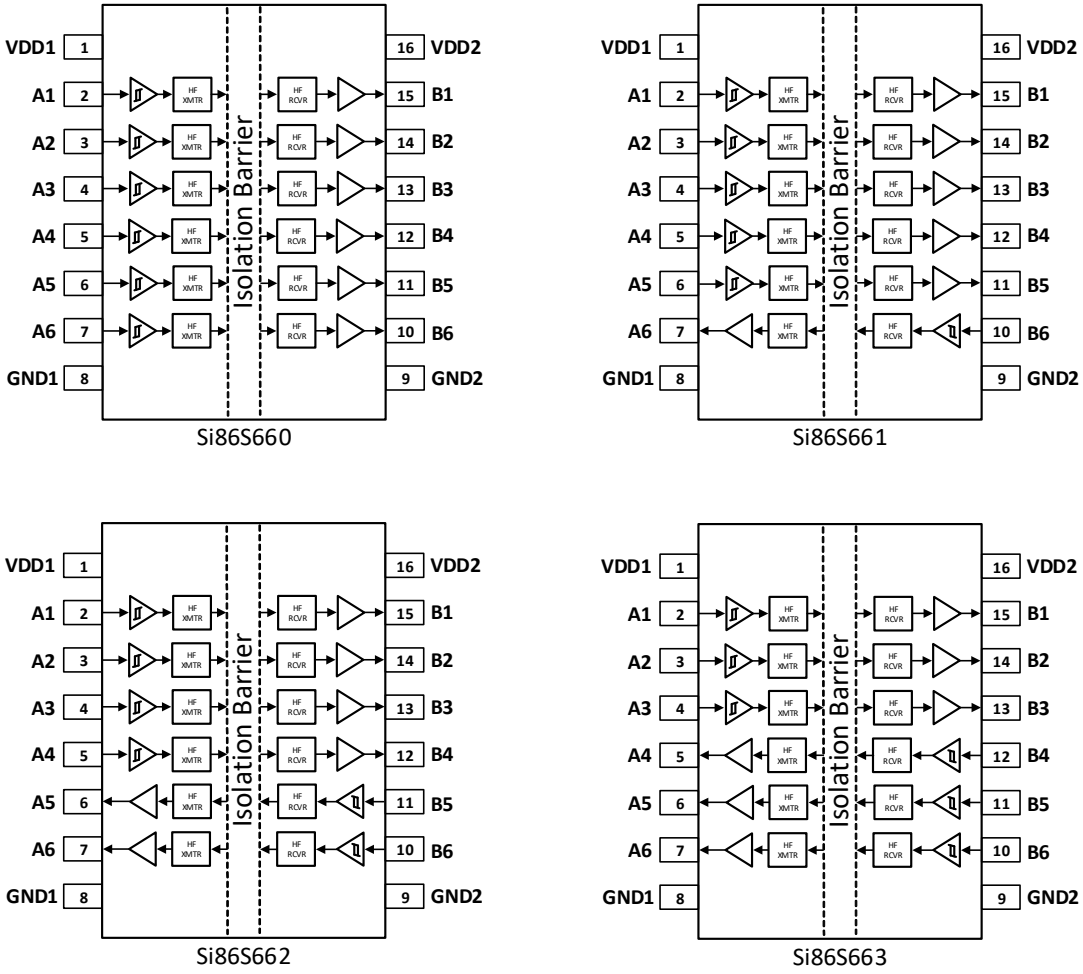

Figure 4. Si86S66x Pinouts

Table 1. Si86S6x/Lx/Mx Pin Descriptions

Name	Type	Description
VDD1	Supply	Side A power supply
GND1	Ground	Side A ground
A1 to A6	Digital I/O	Side A digital I/O
EN1/EN2	Digital input	Side A/B active high output enable
SMb	Digital input	Sleep mode active low for OPNs Si86SMx
NC	—	Not connected
GND2	Ground	Side B ground
B1 to B6	Digital I/O	Side B digital I/O
VDD2	Supply	Side B power supply

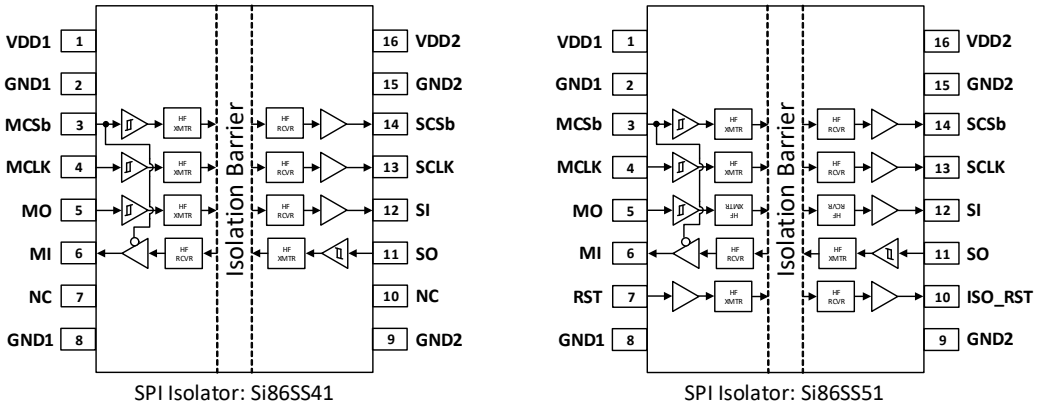

Figure 5. Si86SS41/51 Pinouts

Table 2. Si86SS41/51 Pinout Description

Name	Type	Description
VDD1	Supply	Main side (Side A) power supply pin
GND1	Ground	Main side supply ground pin
MCSb	Digital input	Main side SPI bus chip select, active low input pin
MCLK	Digital input	Main side SPI CLK input pin
MO	Digital input	Main side input pin
MI	Digital output	Main side output pin
NC (Si86SS41)	—	Not connected
RST (Si86SS51)	Digital input	Reset
ISO_RST (Si86SS51)	Digital output	Isolated reset
GND2	Ground	Secondary side supply ground pin
SI	Digital output	Secondary side output pin
SO	Digital input	Secondary side input pin
SCLK	Digital output	Secondary side SPI CLK isolated output pin
SCSb	Digital output	Secondary side SPI bus chip select, isolated output pin
VDD2	Supply	Secondary side power supply pin

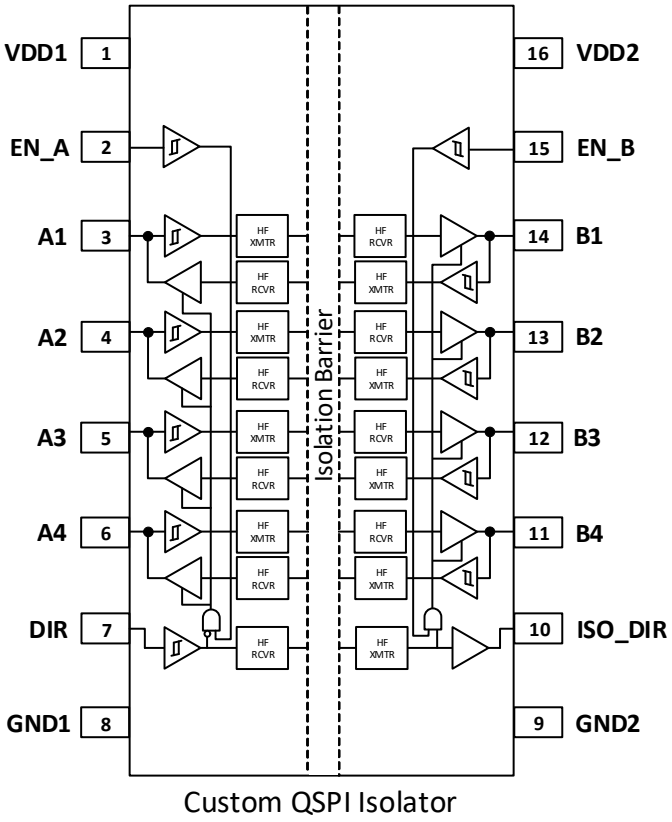

Figure 6. Si86SQ44 Pinout

Table 3. Si86SQ44 Pinout Description

Name	Type	Description
VDD1	Supply	Main side (Side A) power supply pin
EN_A	Digital input	Output enable for side A
Ax	Digital I/O	I/O pins for side A
DIR	Digital input	Input pin, sets channel direction for all channels
GND1	Ground	Main side (Side A) supply ground
GND2	Ground	Secondary side (Side B) supply ground
ISO_DIR	Digital output	Isolated DIR signal output
Bx	Digital I/O	I/O pins for side B
EN_B	Digital input	Output enable for side B
VDD2	Supply	Secondary side (Side B) power supply pin

2. Functional Description

2.1. Theory of Operation

The operation of an Si86Sx channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si86Sx channel is shown in Figure 7.

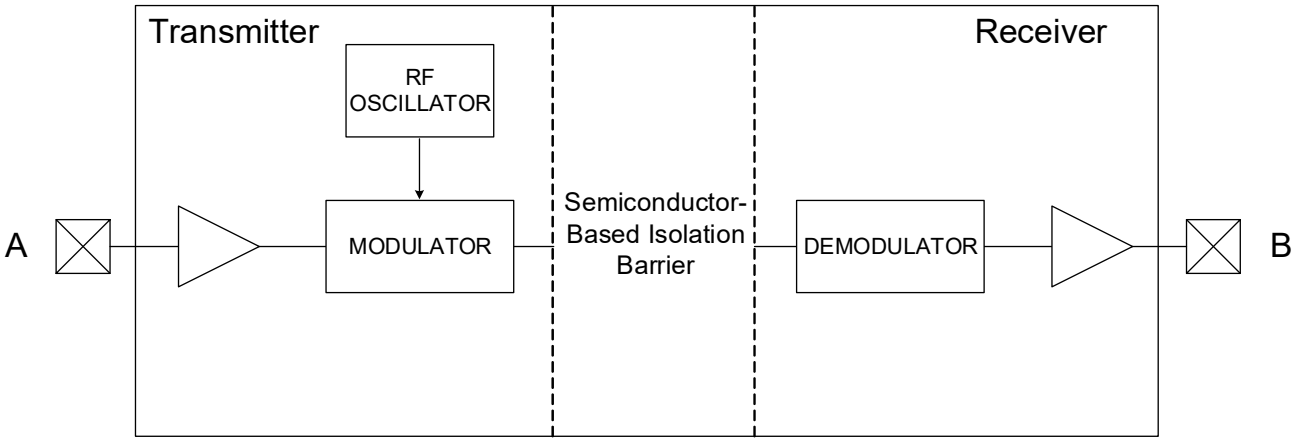

Figure 7. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and improved immunity to magnetic fields. See the following figure for more details.

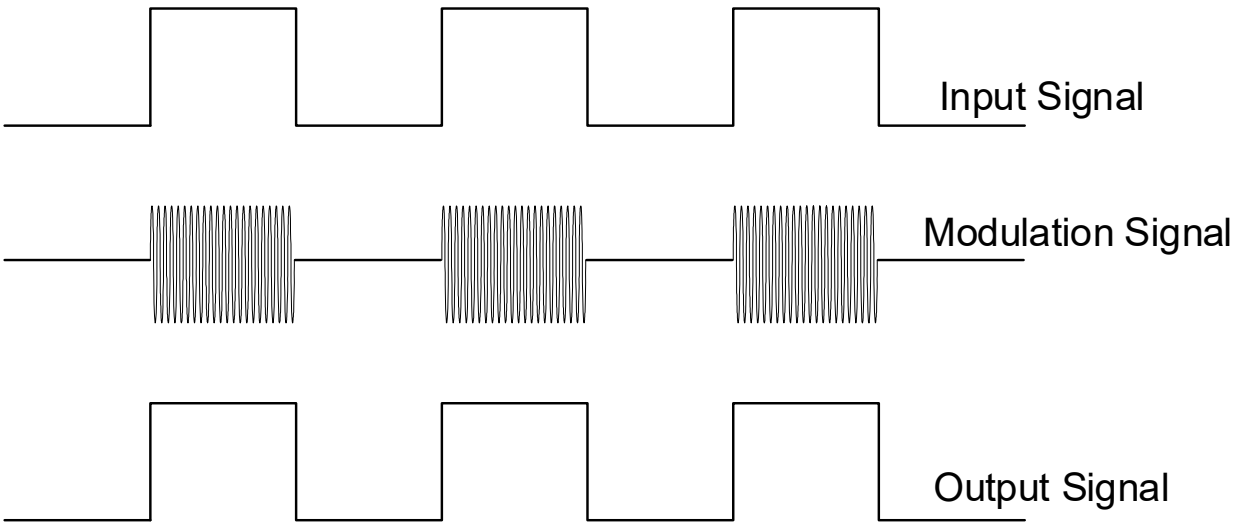

Figure 8. Modulation Scheme

3. Device Operation and System Overview

Device behavior during start-up, normal operation, and shutdown is shown in Figure 9, "Device Behavior during Startup," on page 10, where UVLO+ and UVLO– are the respective positive-going and negative-going thresholds. Refer to the following tables to determine outputs when power supply (VDD) is not present and for logic conditions when enable pins are used.

Table 4. Si86S6x/Lx/Mx Logic Operation

VI Input[1,2,3]	EN/SMb[3]	VDDI State[1,4,5,6]	VDDO State[1,4,5,6]	VO Output[1,2]	Comments
H	H or open	P	P	H	Normal operation
L	H or open	P	P	L	
X	L	P	P	Hi-Z	
X	X	UP	P	L[6]	Default low options
				H[6]	Default high options
X	X	P	UP	UD[7]	Upon transition of VDDO from unpowered to powered, V_O returns to correct state.

1. V_I and V_O are the input and output terminals of any one channel. VDDI and VDDO are the power supplies on the input and output sides respectively.
2. X = Not Applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance; UD = Undetermined.
3. EN1/EN2 enable pins control the state of all outputs on the same side as the pin as stated in table above. For options with sleep mode 1, EN1/EN2 enable pins also turn off circuits on that side, allowing for a low power mode. The SMb pin controls the state of all outputs on the device, including ones on the isolated side, as well as allowing the device to be in low power mode as described in "2.1. Theory of Operation" on page 7.
4. "Powered" state (P) is defined as 2.25 V < VDD < 5.5 V.
5. "Unpowered" state (UP) is defined as VDD < 2.25 V.
6. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
7. UD = Undetermined. Refer to Figure 9, "Device Behavior during Startup," on page 10, the start-up time from unpowered state, below 1.7 V (RSTB) threshold to powered state, is 0.3 ms. If VDDO only dips below 2.1 V (VDDOK level in Figure 3.1) but stays above RSTB level, the start-up time is 1 µs.

Table 5. Si86SS Logic Operation

VI Input[1,2]	VDDI State	VDDO State[1,3,4]	VO Output[1,2]	Comments
H	P	P	H	Normal operation
L	P	P	L	
X	UP	P	L	Default low options
			H	Default high options
X	P	UP	UD[5]	Upon transition of VDDO from unpowered to powered, V_O returns to correct state.

1. V_I and V_O are the input and output terminals of any one channel. VDDI and VDDO are the power supplies on the input and output sides respectively.
2. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance.
3. "Powered" state (P) is defined as 2.25 V < VDD < 5.5 V.
4. "Unpowered" state (UP) is defined as VDD <2.25 V.
5. UD = Undetermined. Refer to Figure 9, "Device Behavior during Startup," on page 10, the start-up time from unpowered state, below 1.7 V (RSTB) threshold to powered state, is 0.3 ms. If VDDO only dips below 2.1 V (VDDOK level in Figure 3.1) but stays above RSTB level, the start-up time is 1 µs.

Table 6. Si86SQx Logic Operation

Ax[1]	Bx[1]	DIR[1]	ISO_DIR[1]	EN_A[1]	EN_B[1]	VDD1 State[2,3]	VDD2 State[2,3]	Notes
X	Hi-Z	H	H	X	L	P	P	Direction is set as input = A; output = B
L	L	H	H	X	H	P	P	Direction is set as input = A; output = B
H	H	H	H	X	H	P	P	Direction is set as input = A; output = B
Hi-Z	X	L	L	L	X	P	P	Direction is set as input = B; output = A
L	L	L	L	H	X	P	P	Direction is set as input = B; output = A
H	H	L	L	H	X	P	P	Direction is set as input = B; output = A
UD	X	X	L	X	X	UP	P	Direction is not set properly if any supply is UP[4]
X	UD	X	UD	X	X	P	UP	Direction is not set properly if any supply is UP[4]

1. X = Not Applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance; UD = Undetermined.
2. "Powered" state (P) is defined as 2.25 V < VDD < 5.5 V.
3. "Unpowered" state (UP) is defined as VDD <2.25 V.
4. 100 kΩ weak pulldown on I/O when the VDD is UP.

3.1. Device Startup, UVLO, and Reset Functionality

Outputs are held low during powerup until VDD is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs. The start-up time of the device is estimated to be 0.3 ms due to the device initialization time. During this time, the outputs will have a 100 kΩ pulldown resistor that will pull the outputs low. After stabilization, the outputs will transition to the default output state indicated by the particular product option.

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. Side A and Side B each have their own undervoltage lockout monitors. Each side can enter or exit UVLO independently. For example, referring to the figure below, Side A unconditionally enters UVLO when VDD1 falls below VDD1(UVLO–) and exits UVLO when VDD1 rises above VDD1(UVLO+). Side B operates the same as Side A with respect to its VDD2 supply.

Along with UVLO, each side has its own self biased circuitry that can detect supply going low enough and issue a complete reset of the part. This is done to avoid loss of device configuration for the particular product option. Referring to the figure below, Side A goes into reset as soon as VDD1 goes below RSTB– (~1.7 V) and comes out of reset when VDD1 goes above RSTB+. When the supply voltage is above RSTB+ the device configuration is reloaded. Side B operates the same as Side A with respect to its VDD2 supply.

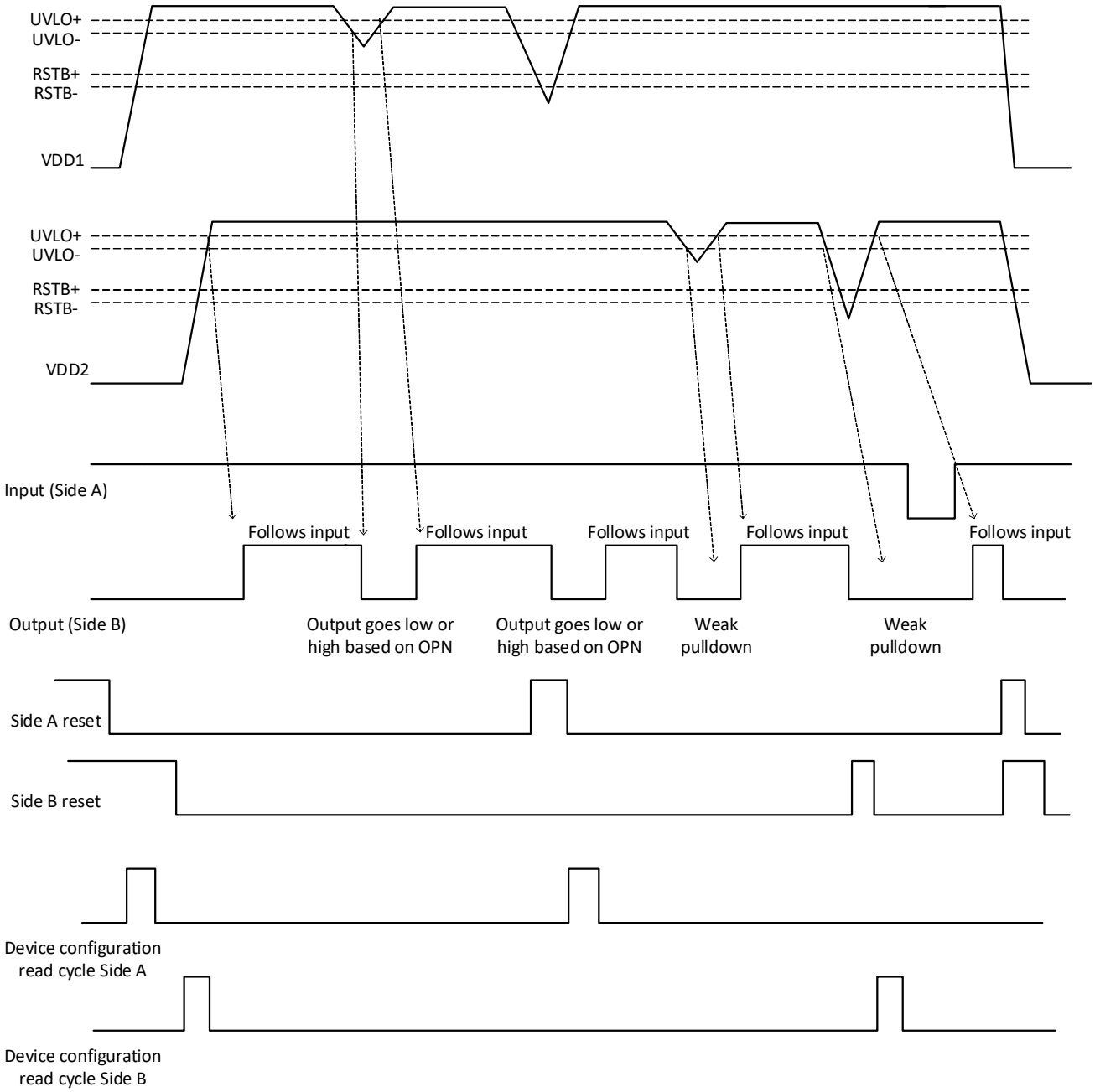

Figure 9. Device Behavior during Startup

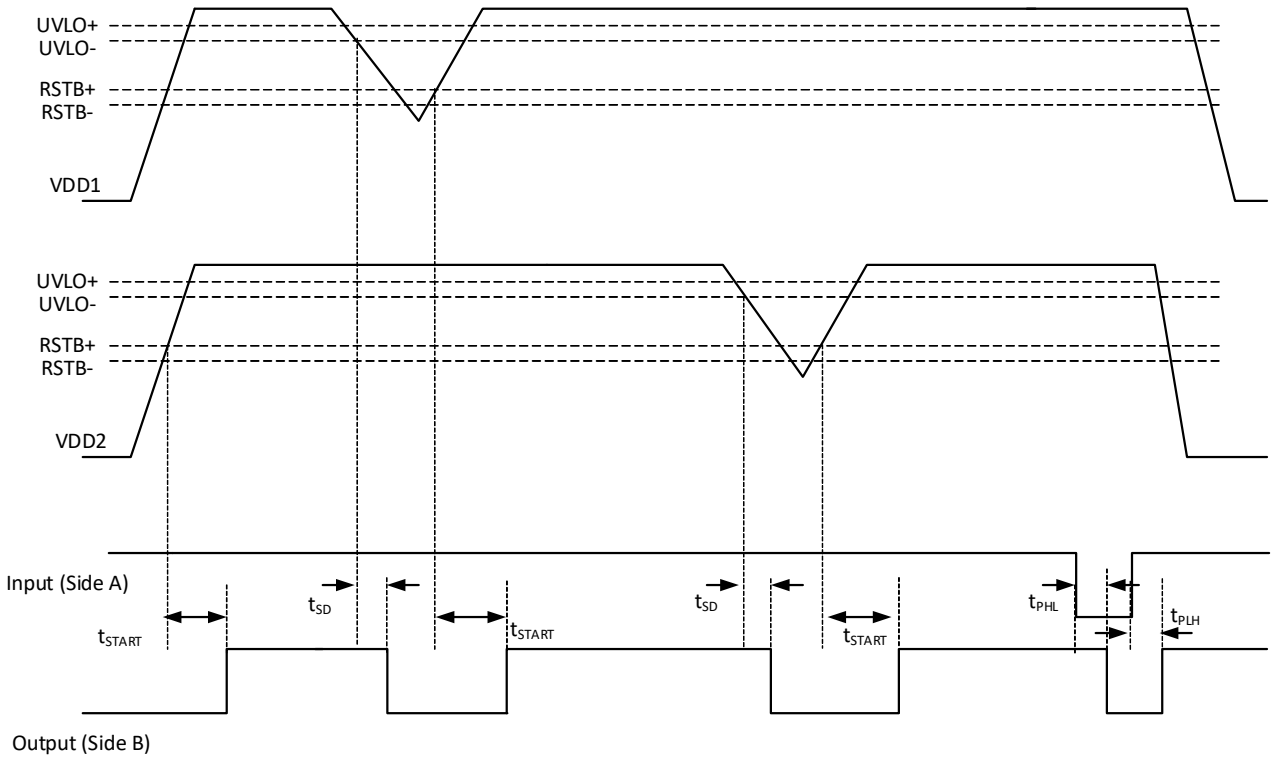

Figure 10. Device Behavior during Normal Operation

3.2. Layout Considerations

To ensure safety in the end-user application, high-voltage circuits (i.e., circuits with >30 VAC) must be physically separated from the safety extra-low-voltage circuits (SELV is a circuit with <30 VAC) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 14, “Insulation and Safety-Related Specifications,” on page 34 and Table 16, “IEC 60747-17 Insulation Characteristics for Si86Sx,” on page 35 detail the working voltage and creepage/clearance capabilities of the Si86Sx and detail the component standards (UL1577, IEC 60747-17), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (61010-1, 62368-1, 60601-1, etc.) requirements before starting any design that uses a digital isolator.

3.2.1. Supply Bypass

The Si86Sx family requires 0.1 and 10 µF bypass capacitors between VDD1 and GND1 and VDD2 and GND2. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, the user may also include resistors (50 to 300 Ω) in series with the inputs and outputs if the system is excessively noisy.

3.2.2. Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled-impedance PCB traces.

3.3. Fail-Safe Operating Mode

Si86Sx devices feature a selectable (by ordering option) mode whereby the default output state (when the input supply is unpowered) can either be a logic high or logic low when the output supply is powered.
See Table 4, “Si86S6x/Lx/Mx Logic Operation,” on page 8 and “11. Ordering Information” on page 49 for more information.

3.4. Device Features and System Overview

3.4.1. Low-Power Mode Operation

The Si86SLx devices are optimized for lower-power operation compared to the Si86S6x options. Typically, they consume 0.25 mA per channel less current in quiescent mode. The pinouts are no different than the Si86S6x options. This mode is always turned on for these devices. The architecture is tuned in favor of power savings rather than higher performance in terms of timing specifications. Refer to “4. Electrical Specifications” on page 18 for details on Low Power mode timing specifications.

3.4.2. Sleep Mode Operation

This new feature is very useful for power savings without compromising on performance. Instead of trading off data rate or CMTI performance for power savings, these options provide an SMb pin that can be used to put the device in sleep mode when not in operation. For example, the Si86SM42 is a four-channel device with two forward channels and two reverse channels. The left, “A”, side of the device has an SMb pin which when driven high (or left unconnected) enables the device but when driven low puts the device into sleep mode with 750 µA per side. In this mode, one isolation channel is always active to read the status of the SMb pin and to restart the device when SMb is driven high or left open.

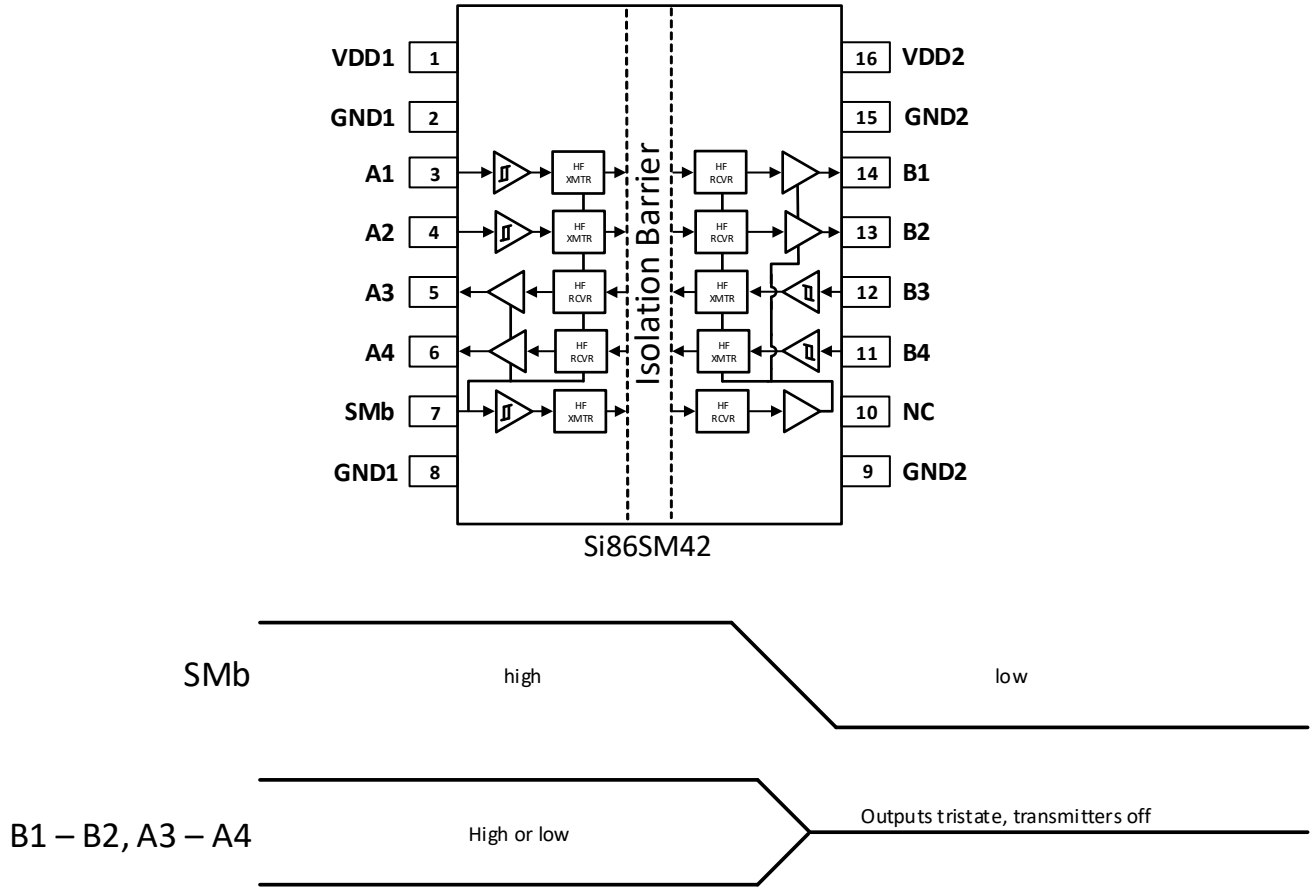

Figure 11. Sleep Mode Operation

3.4.3. SPI Operation for Si86SSx

The Si86SSx are SPI compatible devices. The non-isolated or main (controller) side input pins are MCSb (main side SPI chip select), MCLK (main side SPI clock), and MO (main side SPI MOSI). The non-isolated or main side output pin is MI (main side SPI MISO). The isolated or secondary (peripheral) side output pin is SCSb (secondary side SPI chip select), SCLK (secondary side SPI clock), and SI (secondary side SPI MOSI). The isolated or secondary side input pin is SO (secondary side SPI MISO). The Si86SS51 has an extra isolated digital channel that can be used for signals like Interrupt or Reset. For details, refer to "AN1359: Design Considerations for the Si86Sx Family".

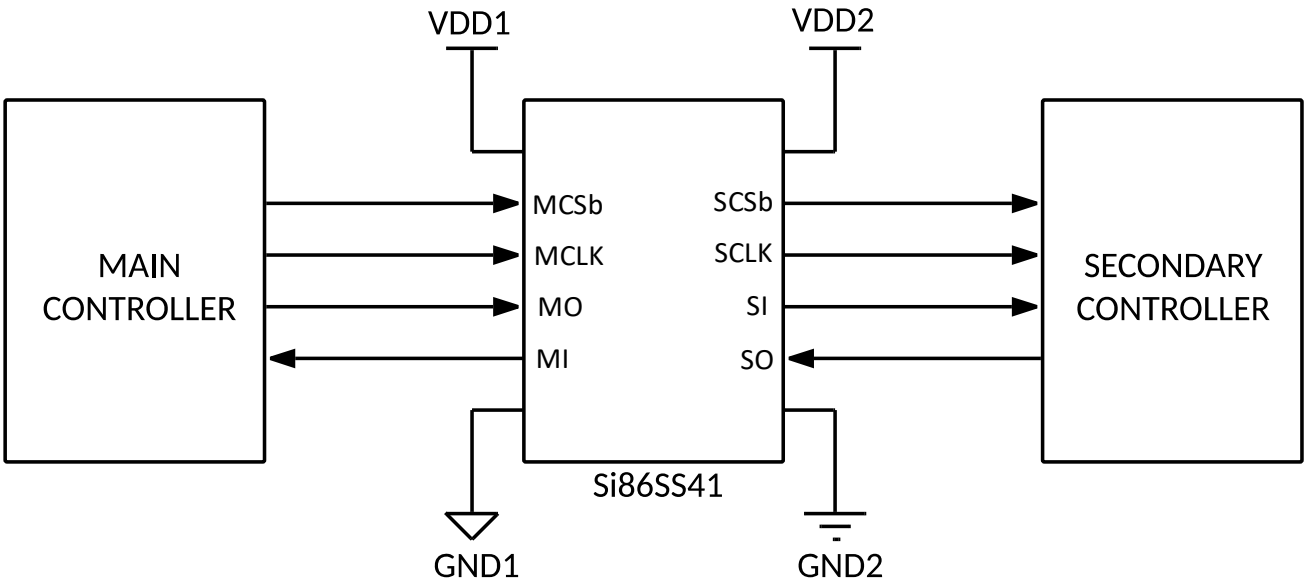

Figure 12. Basic SPI

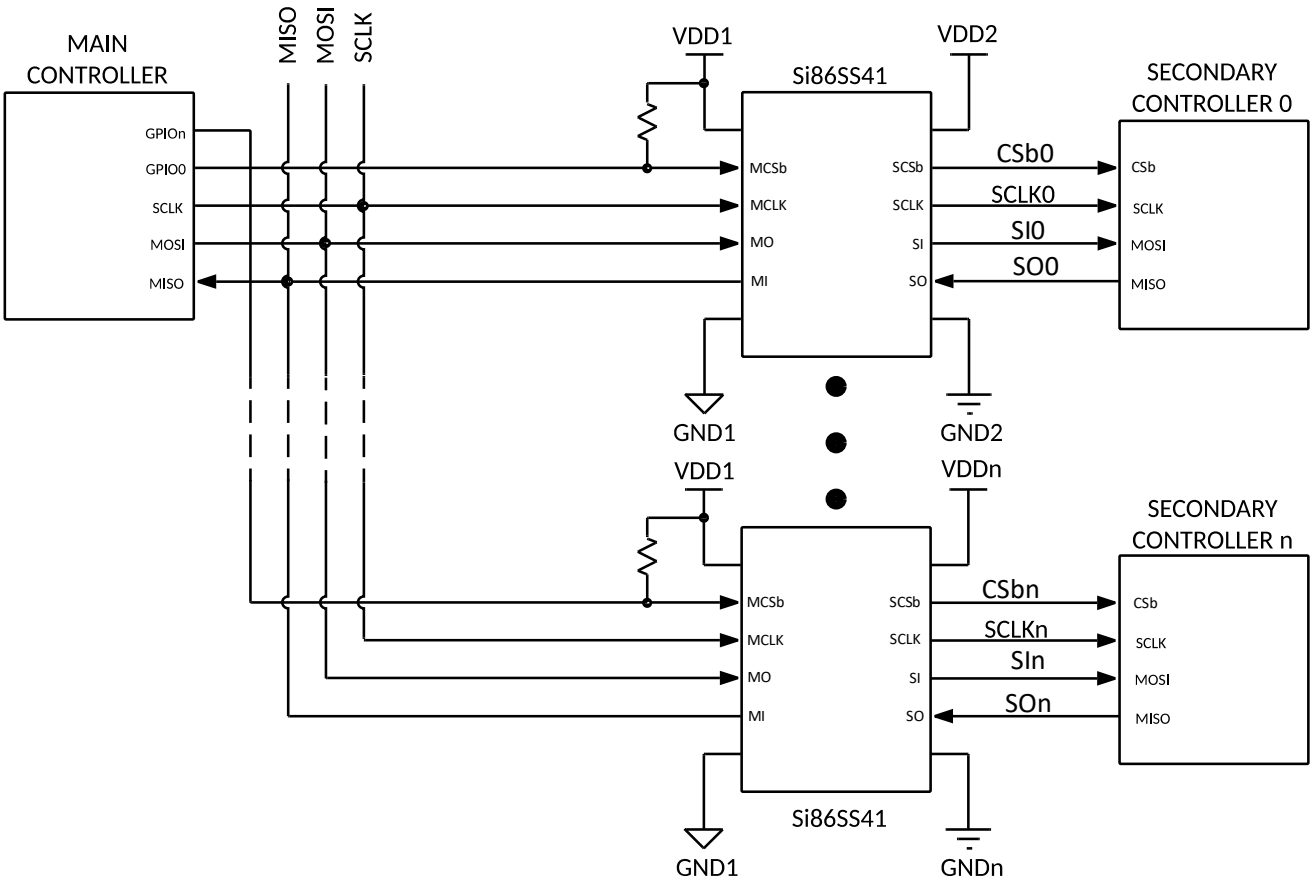

Figure 13. SPI Arrangement with Buffered MI

3.4.4. Custom QSPI Implementation Mode

The Si86SQ44 is a five-channel device with four reversible channels and one forward direction channel (DIR_IN). The DIR_IN pin when driven high configures the device for signal flow from Side A to Side B. The DIR_OUT pin provides an isolated copy of the DIR_IN state. The DIR_IN pin when driven low configures the device for signal flow from B to A. Each side of the device also has an enable pin (EN_A, EN_B), which when driven high enables the transmitter and receiver circuits, and when driven low configures the outputs as tristate. A 10 kΩ pull up resistor to the corresponding VDD is recommended for each enable pin.

The direction control feature of the Si86SQ44 can be useful in implementing a bidirectional (reversible) isolated bus.

Quad SPI is commonly used for faster data transfer from low pin count external memory. It is similar to SPI, but it has four data lines instead of two (MOSI and MISO), and the data lines operates in half-duplex mode with all four lines either reading or writing four bits of data on the same clock edge. Because QSPI operates in half-duplex, the Si86SQ44 can be used for the data lines as it provides direction control of four isolated channels.

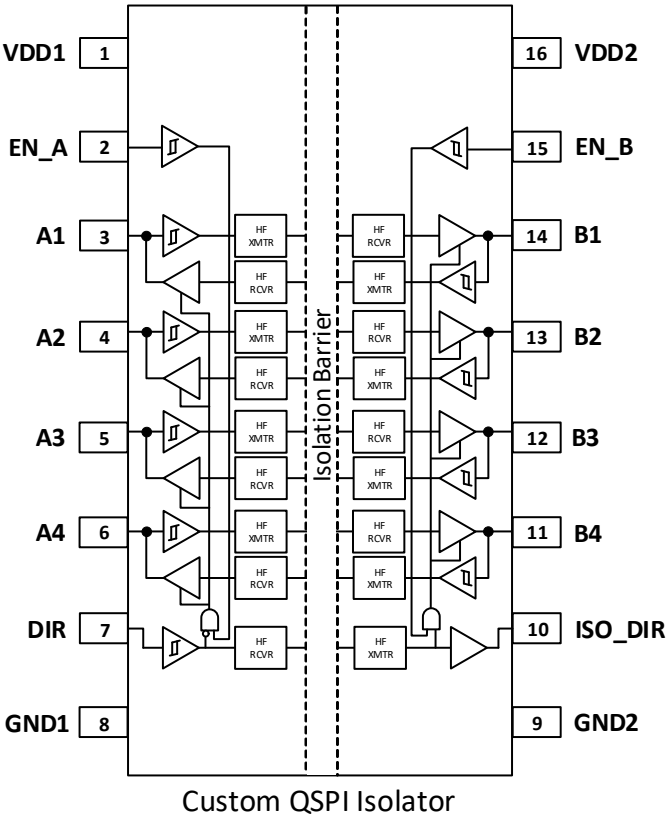

Figure 14. Si86SQ44 Configuration

3.4.5. Input Noise Filters with Deglitch Times of 36 ns

The Si86S64x (4-channel) family is orderable with input deglitch filters which have delay times of 36 ns. These filters remove undesirable noise pulses (glitches) from the input signal so that the isolator only produces an output for a valid input. Any input pulse which lasts less than the deglitch time will not be passed by the filter. Any other input pulse will be passed by the filter and delayed by the filter delay time. See Figure 15 below. The figure shows a positive noise pulse, but negative pulses will also be filtered out.

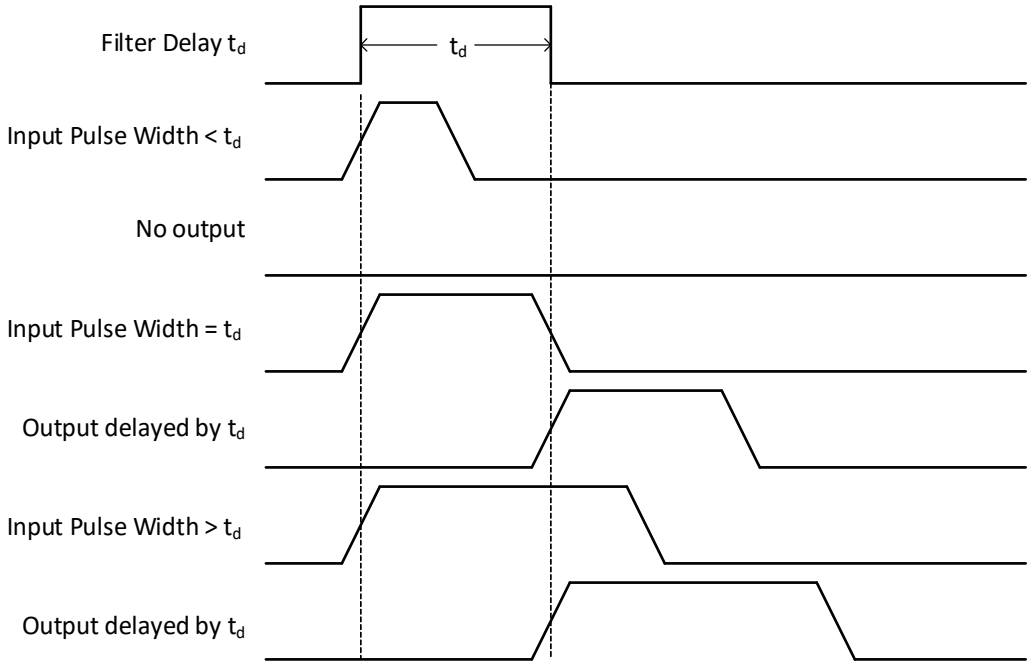

Figure 15. Input Noise Filter Functionality

4. Electrical Specifications

Table 7. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Storage temperature	T_{STG}	–65	150	°C
Operating temperature	T_A	–40	125	°C
Junction temperature	T_J	—	150	°C
Supply voltage	VDD1, VDD2	–0.5	7.0	V
Supply voltage ramp-up	VDD1, VDD2	—	1	V/µs
Input voltage	V_I	–0.5	VDD + 0.5	V
Output voltage	V_O	–0.5	VDD + 0.5	V
Output current drive channel	I_O	–10	+10	mA
ESD	HBM	—	8	kV
ESD	CDM	—	2	kV
ESD	IEC 61000-4-2 contact discharge[2]	—	8000	V
Lead solder temperature (10 s)		—	260	°C

1. Exposure to maximum rating conditions for extended periods may reduce device reliability. Exceeding any of the limits listed here may result in permanent damage to the device.
2. Test is performed across the isolation barrier with device in two-terminal configuration, with pins on each side shorted together. Tested per IEC 61000-4-2 contact discharge.

ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.

Table 8. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Junction operating temperature	T_J	—	—	150	°C
Ambient operating temperature[1]	T_A	–40	25	125	°C
Supply voltage	VDD1, VDD2	2.25	—	5.5	V

1. The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage. The maximum junction temperature is a limitation, and the maximum ambient temperature for any given condition can be calculated as shown in 6.1. Estimating Maximum Ambient Temperature .

Table 9. Electrical Characteristics (General)

T_A = –40 to 125 °C; VDD1, VDD2 as specified in Table 8 above.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD undervoltage threshold	VDD_{UV+}	VDD1, VDD2 rising	2.10	2.18	2.25	V
VDD undervoltage threshold	$VDD_{UV–}$	VDD1, VDD2 falling	1.98	2.05	2.12	V
VDD undervoltage hysteresis	VDD_{HYS}		105	131	160	mV
Input hysteresis	V_{HYS}		0.15 x VDDx	—	—	V
High level input voltage	V_{IH}		0.7 x VDDx	—	—	V
Low level input voltage	V_{IL}		—	—	0.3 x VDDx	V
High level output voltage	V_{OH}	I_{OH} = –4 mA	VDD1, VDD2–0.4	—	—	V
Low level output voltage	V_{OL}	I_{OL} = 4 mA	—	—	0.4	V
Output impedance	Z_O		—	50	—	Ω

Table 10. Electrical Characteristics (VDD = 5.0 V)

VDD1 = 5.0 V ±10%, VDD2 = 5.0 V ±10%, T_A = –40 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S630Bx, Ex						
IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	—	0.70 2.19 2.47 2.29	0.85 2.76 3.03 2.83	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	1.58 2.26	1.93 2.82	mA
Si86S631Bx, Ex						
IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	—	1.28 1.84 2.54 2.25	1.56 2.27 3.00 3.02	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	1.92 2.20	2.29 2.66	mA
Si86S640Bx, Ex						
IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	—	0.84 2.83 3.24 2.96	1.02 3.56 3.95 3.64	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.04 2.93	2.48 3.65	mA
Si86S641Bx, Ex						
IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	—	1.32 2.29 3.17 3.00	1.68 2.96 4.04 3.79	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.26 2.66	2.87 3.40	mA

Table 10. Electrical Characteristics (VDD = 5.0 V) (Continued)

VDD1 = 5.0 V ±10%, VDD2 = 5.0 V ±10%, T_A = –40 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86SW41Bx						
IDD1 IDD2 IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex) All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	1.35 2.31 3.53 3.18 2.45 2.76	1.81 3.06 4.31 3.96 3.07 3.55	mA
Si86S642Bx, Ex						
IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	—	1.86 1.89 3.12 3.12	2.41 2.44 3.97 3.97	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.53 2.55	3.23 3.26	mA
Si86S640Fx, Hx						
IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	—	1.08 3.05 3.53 3.18	1.23 3.81 4.13 3.89	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.31 3.15	2.67 3.91	mA
Si86S641Fx, Hx						
IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	—	1.55 2.52 3.42 3.32	1.87 3.14 4.11 3.94	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.51 2.90	3.01 3.56	mA
Si86S642Fx, Hx						
IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex)	—	2.12 2.14 3.41 3.42	2.57 2.60 4.07 4.09	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.80 2.81	3.36 3.37	mA
Si86SL40Bx, Ex						
IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex)	—	0.79 2.07 2.89 2.13	0.96 2.63 3.54 2.67	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	1.85 2.14	2.24 2.71	mA
Si86SL41Bx, Ex						
IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex)	—	1.07 1.69 2.63 2.25	1.35 2.18 3.25 2.83	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	1.87 1.99	2.31 2.53	mA
Si86SL42Bx, Ex						
IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	—	1.46 1.48 2.54 2.56	1.85 1.86 3.15 3.17	mA

Table 10. Electrical Characteristics (VDD = 5.0 V) (Continued)

VDD1 = 5.0 V ±10%, VDD2 = 5.0 V ±10%, T_A = –40 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.04 2.04	2.54 2.53	mA
Si86SM40Bx, Ex IDD1 IDD2 IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex) SMb = 0 (sleep mode) SMb = 0 (sleep mode)	—	1.51 3.50 3.95 3.63 0.78 1.19	1.85 4.47 4.89 4.57 0.95 1.68	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.73 3.59	3.36 4.56	mA
Si86SM41Bx, Ex IDD1 IDD2 IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex) SMb = 0 (sleep mode) SMb = 0 (sleep mode)	—	2.07 2.93 3.91 3.64 0.77 1.20	2.62 3.73 4.92 4.53 0.97 1.53	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	3.01 3.30	3.78 4.16	mA
Si86SM42Bx, Ex IDD1 IDD2 IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex) SMb = 0 (sleep mode) SMb = 0 (sleep mode)	—	2.62 2.52 3.89 3.78 0.77 1.20	3.36 3.23 4.92 4.77 0.98 1.54	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	3.29 3.17	4.18 4.02	mA
Si86SS41Bx, Ex IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	—	1.37 2.43 3.12 3.13	1.76 3.15 4.01 3.95	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.26 2.80	2.88 3.58	mA
Si86SS51Bx, Ex IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	— — — —	1.52 2.99 3.89 3.72	1.89 3.84 4.73 4.65	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.58 3.40	3.13 4.30	mA
Si86SQ44Bx, Ex IDD1 IDD2 IDD1 IDD2 IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex), DIR = 1 VI = 0(Bx), 1(Ex), DIR = 1 VI = 1(Bx), 0(Ex), DIR = 1 VI = 1(Bx), 0(Ex), DIR = 1 VI = 0(Bx), 1(Ex), DIR = 0 VI = 0(Bx), 1(Ex), DIR = 0 VI = 1(Bx), 0(Ex), DIR = 0 VI = 1(Bx), 0(Ex), DIR = 0	—	3.82 3.47 6.87 3.60 3.05 3.76 3.19 6.81	4.85 4.45 8.51 4.51 3.91 4.83 3.99 8.48	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs; DIR = 1.	—	5.51 3.55	6.84 4.49	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs; DIR = 0.	—	2.40 3.89	3.18 4.97	mA

Table 10. Electrical Characteristics (VDD = 5.0 V) (Continued)

VDD1 = 5.0 V ±10%, VDD2 = 5.0 V ±10%, T_A = –40 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S660Bx, Ex IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	—	0.96 4.05 4.55 4.24	1.16 5.09 5.56 5.23	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.75 4.21	3.33 5.35	mA
Si86S661Bx, Ex IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	—	1.53 3.51 4.61 4.28	1.87 4.47 5.52 5.31	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	3.09 3.93	3.70 4.93	mA
Si86S662Bx, Ex IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	—	1.99 2.93 4.47 4.27	2.38 3.66 5.24 5.13	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	3.25 3.62	3.83 4.41	mA
Si86SW62Bx IDD1 IDD2 IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex) All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.04 2.95 4.98 4.52 3.53 3.76	2.56 3.78 5.59 5.36 4.10 4.60	mA
Si86S663Bx, Ex IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	—	2.59 2.59 4.55 4.55	3.40 3.40 5.79 5.79	mA
IDD IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	3.56 3.56	4.53 4.53	mA
Timing Characteristics						
Data rate Si86SxxxB/Ex			—	—	150	Mbps
Data Rate Si86SxxxF/Hx			—	—	10	Mbps
Pulse width Si86SxxxB/Ex		Minimum pulse width guaranteed to be transmitted to output.	6.7	—	—	ns
Pulse width Si86SxxxF/Hx		Minimum pulse width guaranteed to be transmitted to output.	100	—	—	ns
Propagation delay (Si86SxxxB/Ex)	t_{PHL}, t_{PLH}	See Figure 17, “Propagation Delay Timing,” on page 32.	6.5	9	14	ns
Pulse width distortion (Si86SxxxB/Ex) $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 17, “Propagation Delay Timing,” on page 32.	—	—	3	ns
Pulse width distortion (Si86SWx) $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 17, “Propagation Delay Timing,” on page 32.	—	—	3	ns
Propagation delay skew (Si86SxxxB/Ex)	$t_{PSK(P-P)}$[1]		—	2.0	4.5	ns
Channel-channel skew (Si86SxxxB/Ex)	t_{PSK}		—	0.8	2	ns
Propagation delay (Si86SxxxF/Hx)	t_{PHL}, t_{PLH}	See Figure 17, “Propagation Delay Timing,” on page 32.	31.5	36	42	ns

Table 10. Electrical Characteristics (VDD = 5.0 V) (Continued)

VDD1 = 5.0 V ±10%, VDD2 = 5.0 V ±10%, T_A = –40 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Pulse width distortion (Si86SxxxF/Hx) $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 17, "Propagation Delay Timing," on page 32.	—	—	3	ns
Propagation delay skew (Si86SxxxF/Hx)	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-channel skew (Si86SxxxF/Hx)	t_{PSK}		—	1.5	4	ns
Propagation delay skew (Si86SLx, low power mode)	t_{PHL}, t_{PLH}	See Figure 17, "Propagation Delay Timing," on page 32.	7.0	11.5	19.5	ns
Pulse width distortion (Si86SLx, low power mode) $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 17, "Propagation Delay Timing," on page 32.	—	—	7	ns
Propagation delay skew (Si86SLx, low power mode)	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-channel skew (Si86SLx, low power mode)	t_{PSK}		—	1.5	7	ns
Direction transition delay (Si86SQx)	t_{DIR}		36	55	80	ns
Output rise time	t_r	C_L = 15 pF See Figure 17, "Propagation Delay Timing," on page 32.	—	2.5	—	ns
Output fall time	t_f	C_L = 15 pF See Figure 17, "Propagation Delay Timing," on page 32.	—	2.5	—	ns
Peak eye diagram jitter	$t_{JIT(PK)}$		—	350	—	ps
Common mode transient immunity Si86SxxxB/Ex Si86SxxxF/Hx	CMTI	See Figure 19, "Common-Mode Transient Immunity Test Circuit," on page 33 . VI = VDD or 0 V VCM = ±1500 V	 100 150	 — —	 — —	kV/µs
Enable to data valid	t_{en1}	See Figure 16, "ENABLE Timing Diagram," on page 32.	—	12	20	ns
SMb to sleep mode delay (Si86SMx)	t_{SM}	See Figure 18, "SMb Timing," on page 33.	—	14	23	ns
Enable to data tri-state	t_{en2}	See Figure 16, "ENABLE Timing Diagram," on page 32.	—	11	17	ns
SMb to wake-up from sleep mode	t_{WU}	See Figure 18, "SMb Timing," on page 33.	—	700	1800	ns
Input power loss to valid default output	t_{SD}	See Figure 10, "Device Behavior during Normal Operation," on page 11.	—	8.0	12	ns
Start-up time[2]	t_{START}	See Figure 10, "Device Behavior during Normal Operation," on page 11.	—	—	300	µs
Input leakage current	I_L		–9	—	+9	µA
EN, SMb, MCSb, DIR input current	I_{ENH}, I_{ENL}	$V_{ENx} = V_{IH}$ or V_{IL}	—	—	90	µA

1. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
2. Start-up time is the time period from the application of power to the appearance of valid data at the output. The device initialization time is included in the t_{START} specification above.

Table 11. Electrical Characteristics (VDD = 3.3 V)

VDD1 = 3.3 V ±10%, VDD2 = 3.3 V ±10%, T_A = –40 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S630Bx, Ex IDD1 IDD2 IDD1 IDD2		 VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	 — 	 0.66 2.16 2.43 2.25	 0.81 2.72 2.98 2.78	 mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	1.54 2.21	1.87 2.76	mA
Si86S631Bx, Ex IDD1 IDD2 IDD1 IDD2		 VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	 — 	 1.25 1.8 2.5 2.48	 1.51 2.22 2.95 2.97	 mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	1.88 2.15	2.23 2.6	mA
Si86S640Bx, Ex IDD1 IDD2 IDD1 IDD2		 VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	 — 	 0.81 2.8 3.2 2.92	 0.97 3.51 3.89 3.64	 mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2 2.88	2.4 3.57	mA
Si86S641Bx, Ex IDD1 IDD2 IDD1 IDD2		 VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	 — 	 1.28 2.26 3.13 2.96	 1.64 2.91 3.97 3.73	 mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.22 2.61	2.8 3.33	mA
Si86SW41Bx IDD1 IDD2 IDD1 IDD2 IDD1 IDD2		 VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex) All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	 — 	 1.30 2.27 3.47 3.11 2.39 2.69	 1.75 3.01 4.23 3.89 2.99 3.44	 mA
Si86S642Bx, Ex IDD1 IDD2 IDD1 IDD2		 VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	 — 	 1.83 1.85 3.08 3.08	 2.37 2.39 3.91 3.91	 mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.48 2.5	3.15 3.19	mA
Si86S640Fx, Hx IDD1 IDD2 IDD1 IDD2		 VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	 — 	 1.04 3.01 3.49 3.14	 1.18 3.76 4.06 3.85	 mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.26 3.1	2.61 3.83	mA
Si86S641Fx, Hx IDD1 IDD2 IDD1 IDD2		 VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	 — 	 1.51 2.49 3.38 3.19	 1.83 3.09 4.05 3.88	 mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.46 2.85	2.94 3.5	mA

Table 11. Electrical Characteristics (VDD = 3.3 V) (Continued)

VDD1 = 3.3 V ±10%, VDD2 = 3.3 V ±10%, T_A = –40 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S642Fx, Hx						
IDD1		VI = 0(Bx), 1(Ex)		2.09	2.52	
IDD2		VI = 0(Bx), 1(Ex)	—	2.11	2.55	mA
IDD1		VI = 1(Bx), 0(Ex)		3.37	4.02	
IDD2		VI = 1(Bx), 0(Ex)		3.38	4.03	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.75	3.29	mA
IDD2				2.76	3.3	
Si86SL40Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		0.76	0.91	
IDD2		VI = 0(Bx), 1(Ex)	—	2.04	2.59	mA
IDD1		VI = 1(Bx), 0(Ex)		2.85	3.47	
IDD2		VI = 1(Bx), 0(Ex)		2.09	2.62	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	1.8	2.17	mA
IDD2				2.08	2.63	
Si86SL41Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.04	1.3	
IDD2		VI = 0(Bx), 1(Ex)	—	1.65	2.13	mA
IDD1		VI = 1(Bx), 0(Ex)		2.59	3.2	
IDD2		VI = 1(Bx), 0(Ex)		2.21	2.78	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	1.82	2.25	mA
IDD2				1.94	2.46	
Si86SL42Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.43	1.81	
IDD2		VI = 0(Bx), 1(Ex)	—	1.44	1.82	mA
IDD1		VI = 1(Bx), 0(Ex)		2.5	3.08	
IDD2		VI = 1(Bx), 0(Ex)		2.52	3.11	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	1.99	2.47	mA
IDD2				1.99	2.47	
Si86SM40Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.48	1.81	
IDD2		VI = 0(Bx), 1(Ex)		3.46	4.41	
IDD1		VI = 1(Bx), 0(Ex)	—	3.91	4.81	mA
IDD2		VI = 1(Bx), 0(Ex)		3.59	4.5	
IDD1		SMb = 0 (sleep mode)		0.73	0.88	
IDD2		SMb = 0 (sleep mode)		1.15	1.61	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.69	3.29	mA
IDD2				3.54	4.48	
Si86SM41Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		2.03	2.57	
IDD2		VI = 0(Bx), 1(Ex)		2.9	3.68	
IDD1		VI = 1(Bx), 0(Ex)	—	3.86	4.85	mA
IDD2		VI = 1(Bx), 0(Ex)		3.6	3.68	
IDD1		SMb = 0 (sleep mode)		0.72	0.90	
IDD2		SMb = 0 (sleep mode)		1.17	1.47	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.96	3.71	mA
IDD2				3.25	4.08	
Si86SM42Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		2.58	3.31	
IDD2		VI = 0(Bx), 1(Ex)		2.49	3.19	
IDD1		VI = 1(Bx), 0(Ex)	—	3.85	4.85	mA
IDD2		VI = 1(Bx), 0(Ex)		3.74	4.71	
IDD1		SMb = 0 (sleep mode)		0.72	0.91	
IDD2		SMb = 0 (sleep mode)		1.16	1.49	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	3.23	4.09	mA
IDD2				3.12	3.95	
Si86SS41Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.31	1.69	
IDD2		VI = 0(Bx), 1(Ex)	—	3.09	3.1	mA
IDD1		VI = 1(Bx), 0(Ex)		3.08	3.95	
IDD2		VI = 1(Bx), 0(Ex)		3.09	3.9	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.22	2.81	mA
IDD2				2.75	3.51	

Table 11. Electrical Characteristics (VDD = 3.3 V) (Continued)

VDD1 = 3.3 V ±10%, VDD2 = 3.3 V ±10%, T_A = –40 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86SS51Bx, Ex IDD1 IDD2 IDD1 IDD2		V_I = 0(Bx), 1(Ex) V_I = 0(Bx), 1(Ex) V_I = 1(Bx), 0(Ex) V_I = 1(Bx), 0(Ex)	—	1.47 2.96 3.85 3.68	1.81 3.79 4.67 4.59	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.57 3.35	3.12 4.22	mA
Si86SQ44Bx, Ex IDD1 IDD2 IDD1 IDD2 IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex), DIR = 1 VI = 0(Bx), 1(Ex), DIR = 1 VI = 1(Bx), 0(Ex), DIR = 1 VI = 1(Bx), 0(Ex), DIR = 1 VI = 0(Bx), 1(Ex), DIR = 0 VI = 0(Bx), 1(Ex), DIR = 0 VI = 1(Bx), 0(Ex), DIR = 0 VI = 1(Bx), 0(Ex), DIR = 0	—	3.78 3.44 6.81 3.57 3.00 3.72 3.13 6.75	4.08 4.41 8.42 4.47 3.84 4.78 3.92 7.46	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs; DIR = 1.	—	5.41 3.51	6.71 4.44	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs; DIR = 0.	—	2.57 3.82	3.36 4.88	mA
Si86S660Bx, Ex IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	—	0.93 4.01 4.5 4.2	1.11 5.03 5.48 5.18	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.71 4.14	3.27 5.14	mA
Si86S661Bx, Ex IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	—	1.50 3.48 4.56 4.24	1.82 4.42 5.44 5.25	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	3.04 3.87	3.62 4.85	mA
Si86S662Bx, Ex IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	—	1.95 2.89 4.42 4.23	2.34 3.61 5.17 5.07	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	3.20 3.57	3.75 4.35	mA
Si86SW62Bx IDD1 IDD2 IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex) All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	1.98 2.90 4.90 4.45 3.45 3.68	2.50 3.73 5.51 5.29 4.00 4.50	mA
Si86S663Bx, Ex IDD1 IDD2 IDD1 IDD2		VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	—	2.53 2.53 4.47 4.47	3.35 3.35 5.71 5.71	mA
IDD1 IDD2		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	3.49 3.49	4.48 4.48	mA
Timing Characteristics						
Data rate Si86SxxxB/Ex			—	—	150	Mbps
Data rate Si86SxxxF/Hx			—	—	10	Mbps
Pulse width Si86SxxxB/Ex		Minimum pulse width guaranteed to be transmitted to output.	6.7	—	—	ns

Table 11. Electrical Characteristics (VDD = 3.3 V) (Continued)

VDD1 = 3.3 V ±10%, VDD2 = 3.3 V ±10%, T_A = –40 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Pulse width Si86SxxxF/Hx		Minimum pulse width guaranteed to be transmitted to output.	100	—	—	ns
Propagation delay (Si86SxxxB/Ex)	t_{PHL}, t_{PLH}	See Figure 17, “Propagation Delay Timing,” on page 32.	6	9	15	ns
Pulse width distortion (Si86SxxxB/Ex) $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 17, “Propagation Delay Timing,” on page 32.	—	—	3	ns
Pulse width distortion (Si86SWx) $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 17, “Propagation Delay Timing,” on page 32.	—	—	3.5	ns
Propagation delay skew (Si86SxxxB/Ex)	$t_{PSK(P-P)}$[1]		—	2.0	4.5	ns
Channel-channel skew (Si86SxxxB/Ex)	t_{PSK}		—	0.9	3	ns
Propagation delay (Si86SxxxF/Hx)	t_{PHL}, t_{PLH}	See Figure 17, “Propagation Delay Timing,” on page 32.	31	36	42	ns
Pulse width distortion (Si86SxxxF/Hx) $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 17, “Propagation Delay Timing,” on page 32.	—	—	3	ns
Propagation delay skew (Si86SxxxF/Hx)	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-channel skew (Si86SxxxF/Hx)	t_{PSK}		—	1.5	3.5	ns
Propagation delay (Si86SLx low-power mode)	t_{PHL}, t_{PLH}	See Figure 17, “Propagation Delay Timing,” on page 32.	7	12	20	ns
Pulse width distortion (Si86SLx, low-power mode) $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 17, “Propagation Delay Timing,” on page 32.	—	—	7	ns
Propagation delay skew (Si86SLx, low-power mode)	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-channel skew (Si86SLx, low-power mode)	t_{PSK}		—	1.5	5.5	ns
Direction transition Delay (Si86SQx)	t_{DIR}		37	57	83	ns
Output rise time	t_r	C_L = 15 pF See Figure 17, “Propagation Delay Timing,” on page 32.	—	2.5	—	ns
Output fall time	t_f	C_L = 15 pF See Figure 17, “Propagation Delay Timing,” on page 32.	—	2.5	—	ns
Peak eye diagram jitter	$t_{JIT(PK)}$		—	350	—	ps
Common mode transient immunity Si86SxxxB/Ex Si86SxxxF/Hx	CMTI	See Figure 19, “Common-Mode Transient Immunity Test Circuit,” on page 33 VI = VDD or 0 V VCM = ±1500 V	 100 150	 — —	 — —	kV/µs
Enable to data valid	t_{en1}	See Figure 16, “ENABLE Timing Diagram,” on page 32	—	17	27	ns
SMb to sleep mode delay (Si86SMx)	t_{SM}	See Figure 18, “SMb Timing,” on page 33	—	15	25	ns
Enable to data tri-state	t_{en2}	See Figure 16, “ENABLE Timing Diagram,” on page 32	—	12	19	ns
SMb to wake-up from sleep mode	t_{WU}	See Figure 18, “SMb Timing,” on page 33	—	1100	1900	ns
Input power loss to valid default output	t_{SD}	See Figure 10, “Device Behavior during Normal Operation,” on page 11.	—	8.0	12	ns
Start-up time[2]	t_{START}	See Figure 10, “Device Behavior during Normal Operation,” on page 11.	—	—	300	µs
Input leakage current	I_L		–7	—	+7	µA
EN, SMb, MCSb, DIR input current	I_{ENH}, I_{ENL}	VENx = V_{IH} or V_{IL}	—	—	60	µA

1. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
2. Start-up time is the time period from the application of power to the appearance of valid data at the output. The device initialization time is included in the t_{START} specification above.

Table 12. Electrical Characteristics (VDD = 2.5 V)

VDD1 = 2.5 V ±10%, VDD2 = 2.5 V ±10%, T_A = –40 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S630Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		0.64	0.79	
IDD2		VI = 0(Bx), 1(Ex)	—	2.14	2.7	mA
IDD1		VI = 1(Bx), 0(Ex)		2.41	2.96	
IDD2		VI = 1(Bx), 0(Ex)		2.23	2.76	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	1.52	1.85	mA
IDD2				2.19	2.74	
Si86S631Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.23	1.5	
IDD2		VI = 0(Bx), 1(Ex)	—	1.78	2.19	mA
IDD1		VI = 1(Bx), 0(Ex)		2.48	2.93	
IDD2		VI = 1(Bx), 0(Ex)		2.46	2.95	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	1.85	2.21	mA
IDD2				2.13	2.58	
Si86S640Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		0.79	0.96	
IDD2		VI = 0(Bx), 1(Ex)	—	2.77	3.49	mA
IDD1		VI = 1(Bx), 0(Ex)		3.17	3.86	
IDD2		VI = 1(Bx), 0(Ex)		2.9	3.58	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	1.97	2.38	mA
IDD2				2.85	3.54	
Si86S641Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.27	1.62	
IDD2		VI = 0(Bx), 1(Ex)	—	2.23	2.89	mA
IDD1		VI = 1(Bx), 0(Ex)		3.1	3.95	
IDD2		VI = 1(Bx), 0(Ex)		2.93	3.72	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.19	2.77	mA
IDD2				2.59	3.3	
Si86SW41Bx						
IDD1		VI = 0(Bx), 1(Ex)		1.28	1.72	
IDD2		VI = 0(Bx), 1(Ex)		2.08	2.97	
IDD1		VI = 1(Bx), 0(Ex)	—	3.41	4.19	mA
IDD2		VI = 1(Bx), 0(Ex)		3.06	3.86	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.		2.34	2.92	
IDD2				2.66	3.39	
Si86S642Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.81	2.35	
IDD2		VI = 0(Bx), 1(Ex)	—	1.83	2.37	mA
IDD1		VI = 1(Bx), 0(Ex)		3.06	3.88	
IDD2		VI = 1(Bx), 0(Ex)		3.06	3.88	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.45	3.12	mA
IDD2				2.45	3.12	
Si86S640Fx, Hx						
IDD1		VI = 0(Bx), 1(Ex)		1.02	1.17	
IDD2		VI = 0(Bx), 1(Ex)	—	2.99	3.74	mA
IDD1		VI = 1(Bx), 0(Ex)		3.46	4.03	
IDD2		VI = 1(Bx), 0(Ex)		3.12	3.82	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.24	2.58	mA
IDD2				3.07	3.8	
Si86S641Fx, Hx						
IDD1		VI = 0(Bx), 1(Ex)		1.49	1.81	
IDD2		VI = 0(Bx), 1(Ex)	—	2.46	3.07	mA
IDD1		VI = 1(Bx), 0(Ex)		3.36	4.03	
IDD2		VI = 1(Bx), 0(Ex)		3.16	3.86	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.44	2.92	mA
IDD2				2.82	3.48	

Table 12. Electrical Characteristics (VDD = 2.5 V) (Continued)

VDD1 = 2.5 V ±10%, VDD2 = 2.5 V ±10%, T_A = –40 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S642Fx, Hx						
IDD1		VI = 0(Bx), 1(Ex)		2.07	2.51	
IDD2		VI = 0(Bx), 1(Ex)	—	2.09	2.53	mA
IDD1		VI = 1(Bx), 0(Ex)		3.35	3.99	
IDD2		VI = 1(Bx), 0(Ex)		3.35	4.01	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.72	3.26	mA
IDD2				2.73	3.27	
Si86SL40Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		0.74	0.89	
IDD2		VI = 0(Bx), 1(Ex)	—	2.02	2.57	mA
IDD1		VI = 1(Bx), 0(Ex)		2.83	3.45	
IDD2		VI = 1(Bx), 0(Ex)		2.08	2.6	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	1.78	2.15	mA
IDD2				2.06	2.6	
Si86SL41Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.02	1.29	
IDD2		VI = 0(Bx), 1(Ex)	—	1.63	2.11	mA
IDD1		VI = 1(Bx), 0(Ex)		2.57	3.17	
IDD2		VI = 1(Bx), 0(Ex)		2.19	2.76	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	1.8	2.22	mA
IDD2				1.92	2.44	
Si86SL42Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.41	1.79	
IDD2		VI = 0(Bx), 1(Ex)	—	1.42	1.8	mA
IDD1		VI = 1(Bx), 0(Ex)		2.48	3.07	
IDD2		VI = 1(Bx), 0(Ex)		2.49	3.08	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	1.96	2.44	mA
IDD2				1.97	2.44	
Si86SM40Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.45	1.78	
IDD2		VI = 0(Bx), 1(Ex)		3.44	4.38	
IDD1		VI = 1(Bx), 0(Ex)	—	3.87	4.78	mA
IDD2		VI = 1(Bx), 0(Ex)		3.57	4.47	
IDD1		SMb = 0 (sleep mode)		0.70	0.86	
IDD2		SMb = 0 (sleep mode)		1.14	1.58	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.66	3.26	mA
IDD2				3.51	4.44	
Si86SM41Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		2.01	2.55	
IDD2		VI = 0(Bx), 1(Ex)		2.87	3.66	
IDD1		VI = 1(Bx), 0(Ex)	—	3.84	4.82	mA
IDD2		VI = 1(Bx), 0(Ex)		3.57	4.45	
IDD1		SMb = 0 (sleep mode)		0.69	0.88	
IDD2		SMb = 0 (sleep mode)		1.15	1.46	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.93	3.67	mA
IDD2				3.23	4.06	
Si86SM42Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		2.56	3.29	
IDD2		VI = 0(Bx), 1(Ex)		2.47	3.16	
IDD1		VI = 1(Bx), 0(Ex)	—	3.82	4.83	mA
IDD2		VI = 1(Bx), 0(Ex)		3.72	4.68	
IDD1		SMb = 0 (sleep mode)		0.69	0.88	
IDD2		SMb = 0 (sleep mode)		1.15	1.48	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	3.2	4.06	mA
IDD2				3.1	3.92	
Si86SS41Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.29	1.66	
IDD2		VI = 0(Bx), 1(Ex)	—	2.38	3.08	mA
IDD1		VI = 1(Bx), 0(Ex)		3.06	3.93	
IDD2		VI = 1(Bx), 0(Ex)		3.07	3.88	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.21	2.79	mA
IDD2				2.73	3.48	

Table 12. Electrical Characteristics (VDD = 2.5 V) (Continued)

VDD1 = 2.5 V ±10%, VDD2 = 2.5 V ±10%, T_A = –40 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86SS51Bx, Ex						
IDD1		V_I = 0(Bx), 1(Ex)	—	1.44	1.78	mA
IDD2		V_I = 0(Bx), 1(Ex)		2.94	3.77	
IDD1		V_I = 1(Bx), 0(Ex)		3.82	4.64	
IDD2		V_I = 1(Bx), 0(Ex)		3.66	4.57	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.56	3.11	mA
IDD2				3.32	4.19	
Si86SQ44Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex), DIR = 1	—	3.76	4.77	mA
IDD2		VI = 0(Bx), 1(Ex), DIR = 1		3.42	4.39	
IDD1		VI = 1(Bx), 0(Ex), DIR = 1		6.75	8.36	
IDD2		VI = 1(Bx), 0(Ex), DIR = 1		3.55	4.45	
IDD1		VI = 0(Bx), 1(Ex), DIR = 0		2.97	3.81	
IDD2		VI = 0(Bx), 1(Ex), DIR = 0		3.70	4.76	
IDD1		VI = 1(Bx), 0(Ex), DIR = 0		3.10	3.88	
IDD2		VI = 1(Bx), 0(Ex), DIR = 0		6.70	8.33	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs; DIR = 1.	—	5.34	6.63	mA
IDD2				3.49	4.42	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs; DIR = 0.	—	2.64	3.45	mA
IDD2				3.77	4.83	
Si86S660Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)	—	0.91	1.10	mA
IDD2		VI = 0(Bx), 1(Ex)		3.99	5.01	
IDD1		VI = 1(Bx), 0(Ex)		4.46	5.45	
IDD2		VI = 1(Bx), 0(Ex)		4.18	5.16	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	2.68	3.23	mA
IDD2				4.1	5.1	
Si86S661Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)	—	1.48	1.80	mA
IDD2		VI = 0(Bx), 1(Ex)		3.46	4.40	
IDD1		VI = 1(Bx), 0(Ex)		4.53	5.41	
IDD2		VI = 1(Bx), 0(Ex)		4.22	5.23	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	3.00	3.59	mA
IDD2				3.84	4.82	
Si86S662Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)	—	1.93	2.32	mA
IDD2		VI = 0(Bx), 1(Ex)		2.88	3.59	
IDD1		VI = 1(Bx), 0(Ex)		4.39	5.14	
IDD2		VI = 1(Bx), 0(Ex)		4.21	5.05	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	3.17	3.73	mA
IDD2				3.54	4.32	
Si86SW62Bx						
IDD1		VI = 0(Bx), 1(Ex)	—	1.94	2.46	mA
IDD2		VI = 0(Bx), 1(Ex)		2.68	3.69	
IDD1		VI = 1(Bx), 0(Ex)		4.83	5.45	
IDD2		VI = 1(Bx), 0(Ex)		4.40	5.24	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.		3.38	3.93	
IDD2				3.63	4.44	
Si86S663Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)	—	2.5	3.31	mA
IDD2		VI = 0(Bx), 1(Ex)		2.5	3.31	
IDD1		VI = 1(Bx), 0(Ex)		4.42	5.66	
IDD2		VI = 1(Bx), 0(Ex)		4.42	5.66	
IDD1		All Inputs = 500 kHz square wave; C_L = 15 pF on all outputs.	—	3.47	4.42	mA
IDD2				3.46	4.42	
Timing characteristics						
Data rate Si86SxxxB/Ex			—	—	150	Mbps
Data rate Si86SxxxF/Hx			—	—	10	Mbps
Pulse width Si86SxxxB/Ex		Minimum pulse width guaranteed to be transmitted to output.	6.7	—	—	ns
Pulse width Si86SxxxF/Hx		Minimum pulse width guaranteed to be transmitted to output.	100	—	—	ns

Table 12. Electrical Characteristics (VDD = 2.5 V) (Continued)

VDD1 = 2.5 V ±10%, VDD2 = 2.5 V ±10%, T_A = –40 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Propagation delay (Si86SxxxB/Ex)	t_{PHL}, t_{PLH}	See Figure 17, “Propagation Delay Timing,” on page 32.	8	11	18	ns
Pulse width distortion (Si86SxxxB/Ex) $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 17, “Propagation Delay Timing,” on page 32.	—	—	3	ns
Pulse width distortion (Si86SWx) $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 17, “Propagation Delay Timing,” on page 32.	—	—	3.5	ns
Propagation delay skew (Si86SxxxB/Ex)	$t_{PSK(P-P)}$[1]		—	2.0	4.5	ns
Channel-channel skew (Si86SxxxB/Ex)	t_{PSK}		—	1.1	3	ns
Propagation delay (Si86SxxxF/Hx)	t_{PHL}, t_{PLH}	See Figure 17, “Propagation Delay Timing,” on page 32.	33	39	45	ns
Pulse width distortion (Si86SxxxF/Hx) $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 17, “Propagation Delay Timing,” on page 32.	—	—	3	ns
Propagation delay skew (Si86SxxxF/Hx)	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-channel skew (Si86SxxxF/Hx)	t_{PSK}		—	1.7	3	ns
Propagation delay (Si86SLx, low-power mode)	t_{PHL}, t_{PLH}	See Figure 17, “Propagation Delay Timing,” on page 32.	9	14	23	ns
Pulse width distortion (Si86SLx, low-power mode) $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 17, “Propagation Delay Timing,” on page 32.	—	—	7	ns
Propagation delay skew (Si86SLx, low-power mode)	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-channel skew (Si86SLx, low-power mode)	t_{PSK}		—	1.6	6	ns
Direction transition delay (Si86SQx)	t_{DIR}	.	40	64	95	ns
Output rise time	t_r	C_L = 15 pF See Figure 17, “Propagation Delay Timing,” on page 32.	—	2.5	—	ns
Output fall time	t_f	C_L = 15 pF See Figure 17, “Propagation Delay Timing,” on page 32.	—	2.5	—	ns
Peak eye diagram jitter	$t_{JIT(PK)}$		—	350	—	ps
Common mode transient immunity Si86SxxxB/Ex Si86SxxxF/Hx	CMTI	See Figure 19, “Common-Mode Transient Immunity Test Circuit,” on page 33 VI = VDD or 0 V VCM = ±1500 V	 100 150	 — —	 — —	kV/µs
Enable to data valid	t_{en1}	See Figure 16, “ENABLE Timing Diagram,” on page 32	—	29	44	ns
SMb to sleep mode delay (Si86SMx)	t_{SM}	See Figure 18, “SMb Timing,” on page 33	—	19	30	ns
Enable to data tri-state	t_{en2}	See Figure 16, “ENABLE Timing Diagram,” on page 32	—	16	27	ns
SMb to wake-up from sleep mode	t_{WU}	See Figure 18, “SMb Timing,” on page 33	—	1400	2100	ns
Input power loss to valid default output	t_{SD}	See Figure 10, “Device Behavior during Normal Operation,” on page 11.	—	8.0	12	ns

Table 12. Electrical Characteristics (VDD = 2.5 V) (Continued)

VDD1 = 2.5 V ±10%, VDD2 = 2.5 V ±10%, T_A = –40 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Start-up time[2]	t_{START}	See Figure 10, "Device Behavior during Normal Operation," on page 11.	—	—	300	µs
Input leakage current	I_L		–7	—	+7	µA
EN, SMb, MCSb, DIR input current	I_{ENH}, I_{ENL}	VENx = V_{IH} or V_{IL}	—	—	45	µA

1. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
2. Start-up time is the time period from the application of power to the appearance of valid data at the output. The OTP initialization time is included in the t_{START} specification above.

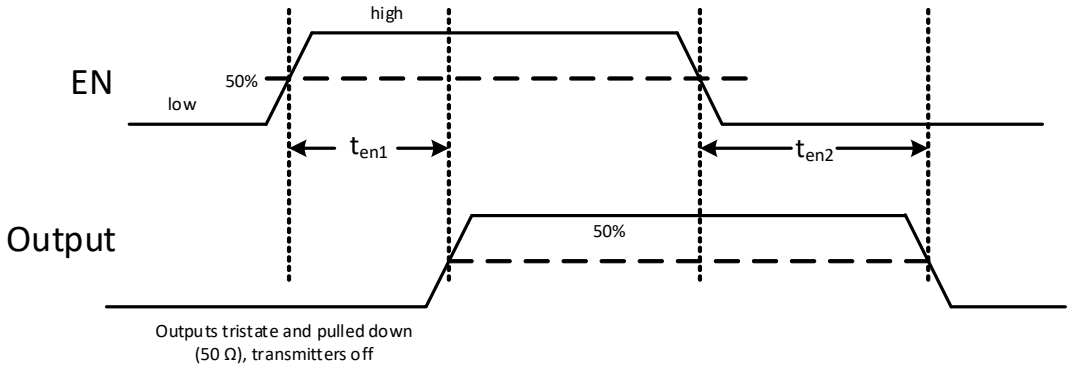

Figure 16. ENABLE Timing Diagram

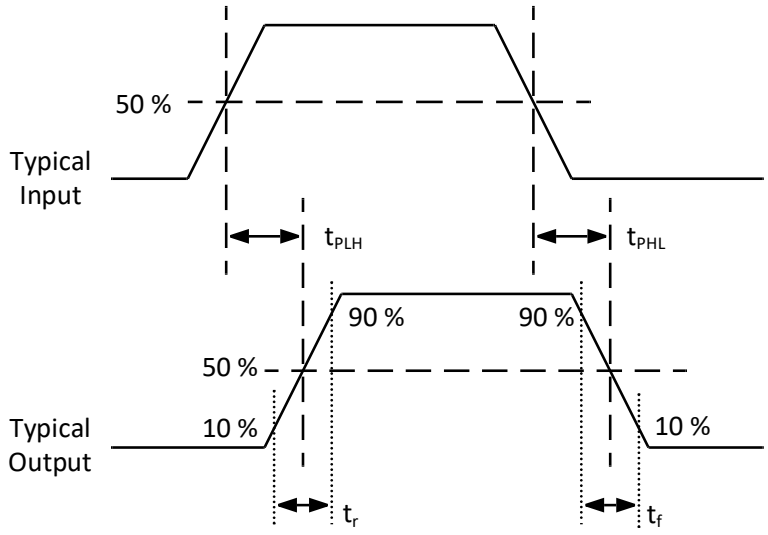

Figure 17. Propagation Delay Timing

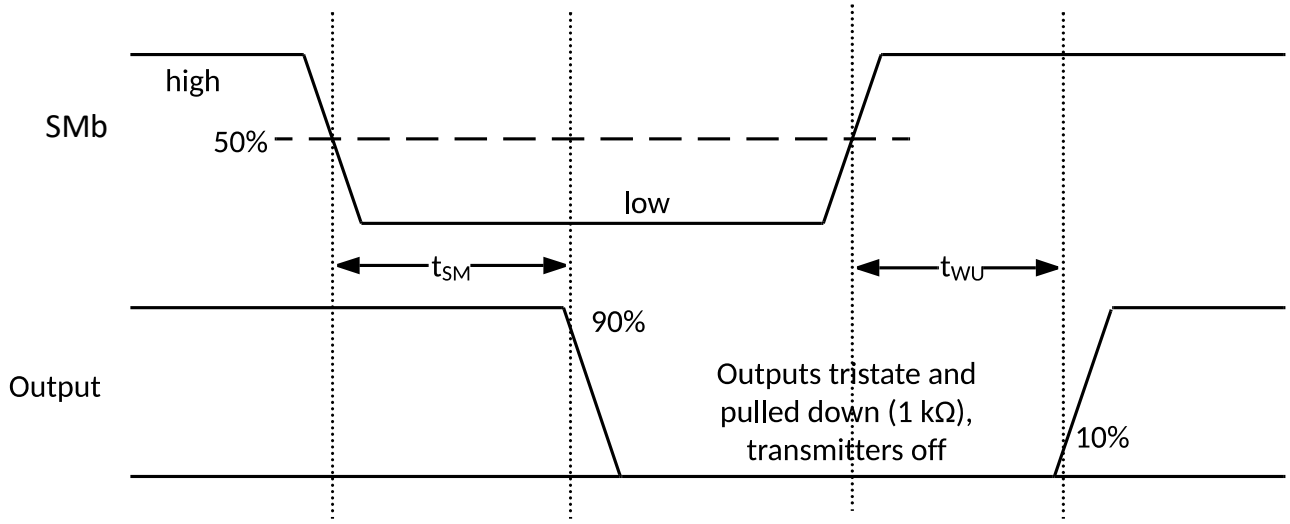

Figure 18. SMb Timing

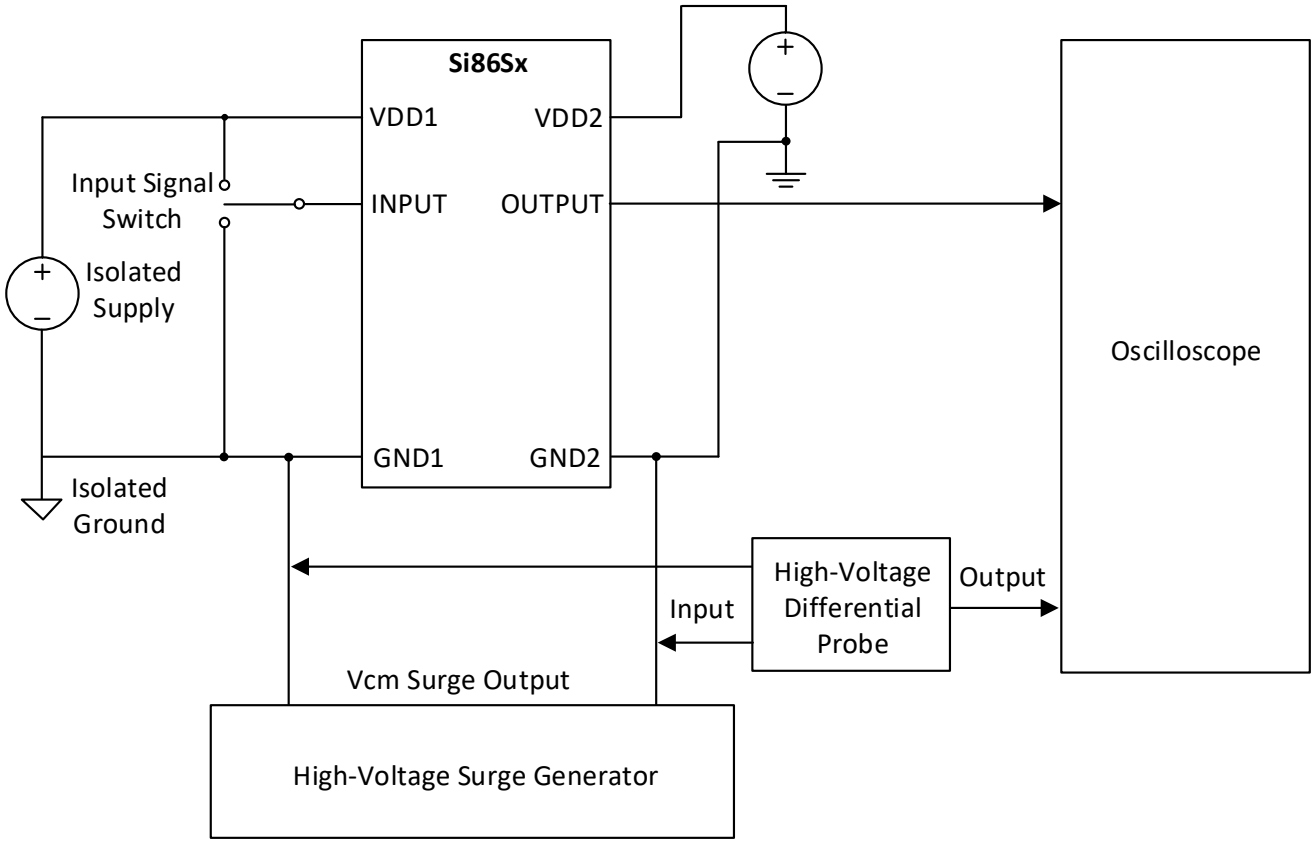

Figure 19. Common-Mode Transient Immunity Test Circuit

5. Safety Certifications and Specifications

Table 13. Regulatory Information (Pending)[1]

CSA
The Si86Sx is certified under CSA. For more details, see master contract number 232873.
62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
60601-1: Up to 250 V_{RMS} working voltage and two means of patient protection (MOPP).
VDE
The Si86Sx is certified under VDE. For more details, see file 5028467.
60747-17: Up to 2121 Vpeak for reinforced insulation working voltage.
UL
The Si86Sx is certified under UL1577 component recognition program. For more details, see file E257455.
Rated up to 6.0 kV_{RMS} V_{ISO} isolation voltage for basic protection.
CQC
The Si86Sx is certified under GB4943.1.
Rated up to 250 V_{RMS} reinforced insulation working voltage at 5000 meters tropical climate.

1. For details, see "11. Ordering Information" on page 49.

Table 14. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value			Unit
			WB SOIC-16	NB SOIC-16	QSOP-16	
Nominal external air gap (clearance)	CLR		8.0	3.9	3.6	mm
Nominal external tracking (creepage)	CRP		8.0	3.9	3.6	mm
Minimum internal gap (internal clearance)	DTI		0.036	0.036	0.036	mm
Tracking resistance	CTI or PTI	IEC60112	600	600	600	V_{RMS}
Erosion depth	ED		0.019	0.019	0.031	mm
Resistance (input-output)[1]	R_{IO}	Test voltage = 500 V at 25 °C	10^{12}	10^{12}	10^{12}	Ω
Capacitance (input-output)[1]	C_{IO}	f = 1 MHz	2.0	2.0	2.0	pF
Input capacitance[2]	C_I		4.0	4.0	4.0	pF

1. To determine resistance and capacitance, the Si86Sx is converted into a 2-terminal device. Pins on Side A are shorted together to form the first terminal and pins on Side B are shorted together to form the second terminal. The parameters are then measured between these two terminals.
2. Measured from input pin to ground.

Table 15. IEC 60664-1 Ratings

Parameter	Test Conditions	Specification		
		WB SOIC-16	NB SOIC-16	QSOP-16
Material group		I	I	I
Overvoltage category	Rated mains voltage ≤150 V_{RMS}	I-IV	I-IV	I-IV
	Rated mains voltage ≤300 V_{RMS}	I-IV	I-III	I-III
	Rated mains voltage ≤600 V_{RMS}	I-IV	I-II	I-II
	Rated mains voltage ≤1000 V_{RMS}	I-III	I	I

Table 16. IEC 60747-17 Insulation Characteristics for Si86Sx[1]

Parameter	Symbol	Test Condition	Characteristic			Unit
			WB SOIC-16	NB SOIC-16	QSOP-16	
Maximum working isolation voltage	V_{IOWM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	1500	445	445	V_{RMS}
Maximum repetitive isolation voltage	V_{IORM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	2121	630	630	V_{peak}
Apparent charge	q_{pd}	Method b: At routine test (100% production) and preconditioning (type test); V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 x V_{IORM}, t_m = 1 s (method b1) or $V_{pd(m)}$ = V_{ini}, t_m = t_{ini} (method b2)	≤5	≤5	≤5	pC
Maximum transient isolation voltage	V_{IOTM}	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	8484	5302	3535	V_{peak}
Maximum surge isolation voltage	V_{IOSM}	Tested in oil with 1.3 x V_{IMP} or 10 kV minimum and 1.2 µs/50 µs profile	10400	10400	10400	V_{peak}
Maximum impulse voltage	V_{IMP}	Tested in air with 1.2 µs/50 µs profile	8000	5000	5000	V_{peak}
Isolation resistance	R_{IO_S}	T_{AMB} = T_S, V_{IO} = 500 V	$>10^9$	$>10^9$	$>10^9$	Ω
Pollution degree			2	2	2	
Climatic category			40/125/21	40/125/21	40/125/21	

1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 17. UL 1577 Insulation Characteristics

Parameter	Symbol	Test Condition	Characteristic			Unit
			WB SOIC-16	NB SOIC-16	QSOP-16	
Maximum withstanding isolation voltage	V_{ISO}	V_{TEST} = V_{ISO}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{ISO}, t = 1 s (100% production)	6000	3750	2500	V_{RMS}

Table 18. IEC 60747-17 Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Max			Unit
			WB SOIC-16	NB SOIC-16	QSOP-16	
Safety temperature	T_S		150	150	150	°C
Safety input, output, or supply current	I_S	Refer to θ_{JA} in Table 19, V_{DD} = 5.5 V, T_J = 150 °C, T_A = 25 °C	345	339	311	mA
Safety input, output, or total power	P_S		1894	1865	1712	mW

1. Maximum value allowed in the event of a failure; also see the thermal derating curves in Figure 20, Figure 21, and Figure 22.

Table 19. Thermal Characteristics

Parameter	Symbol	WB SOIC-16	NB SOIC-16	QSOP-16	Unit
IC junction-to-air thermal resistance	θ_{JA}	66	67	73	°C/W
IC junction-to-board thermal resistance	θ_{JB}	35	30	43	
IC junction-to-case thermal resistance	θ_{JC}	24	20	31	
Thermal characterization parameter to report the difference between junction temperature and the temperature of the board measured at the top surface of the board.	Ψ_{JB}	33	29	43	

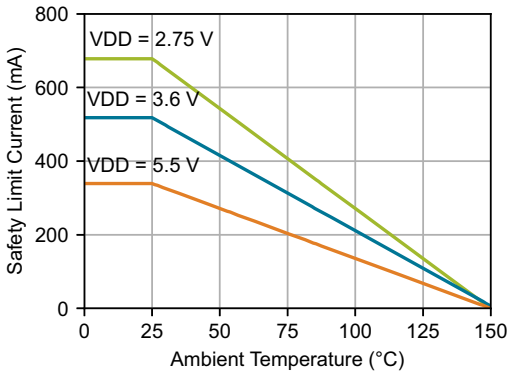

Figure 20. (NB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Current

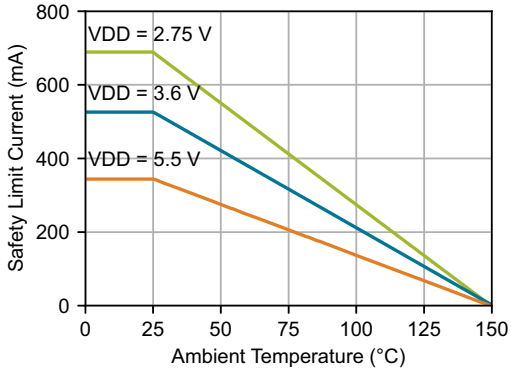

Figure 21. (WB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Current

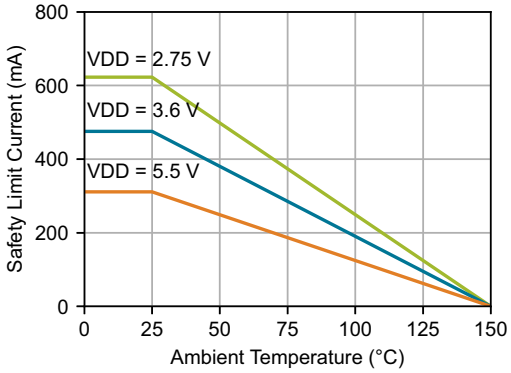

Figure 22. (QSOP-16) Thermal Derating Curve, Dependence of Safety Limiting Current

6. Typical Performance Characteristics

The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to Electrical Characteristics tables for actual specification limits. All typical characteristics data is valid for nominal VDD and ambient temperature of 25 °C. For typical IDD, please refer to the Isolator Power Consumption Calculator provided on the Skyworks web site.

6.1. Estimating Maximum Ambient Temperature

$T_{A(max)} = T_{Jmax} – P \times \theta_{JA}$. θ_{JA} values are specified in Table 19, “Thermal Characteristics,” on page 36.

P = total power dissipated by package in W. Values for any OPN and operating condition can be obtained using the Skyworks Isolator Power Consumption Calculator.

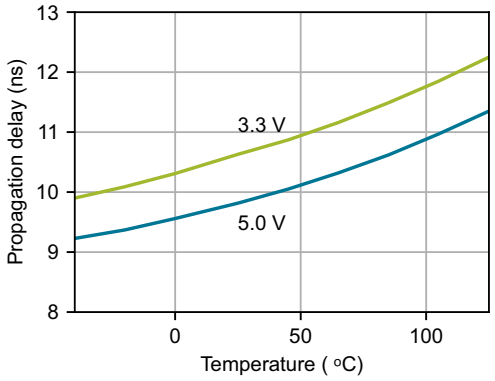

Figure 23. Si86S6x Propagation Delay vs. Temperature

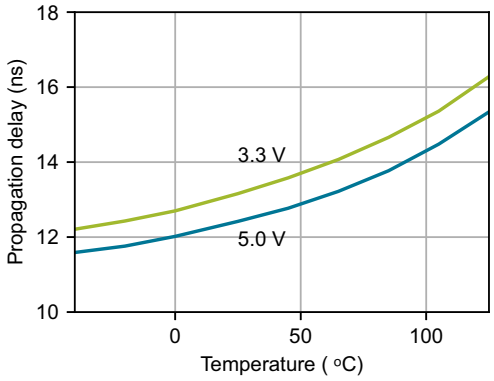

Figure 24. Si86SLx Propagation Delay vs. Temperature

7. Package Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The Si86S6x are rated to Moisture Sensitivity Level 2 (MSL2) at 260 °C for all packages except WB SOIC-16, which is rated to Moisture Sensitivity Level 2A (MSL2A) at 260 °C.

They can be used for lead or lead-free soldering. For additional information, refer to Skyworks Application Note, “PCB Design and SMT Assembly/Rework Guidelines,” Document Number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Refer to Standard SMT Reflow Profiles: JEDEC Standard J-STD-020.

8. Package Outline

8.1. Package Outline (WB SOIC-16)

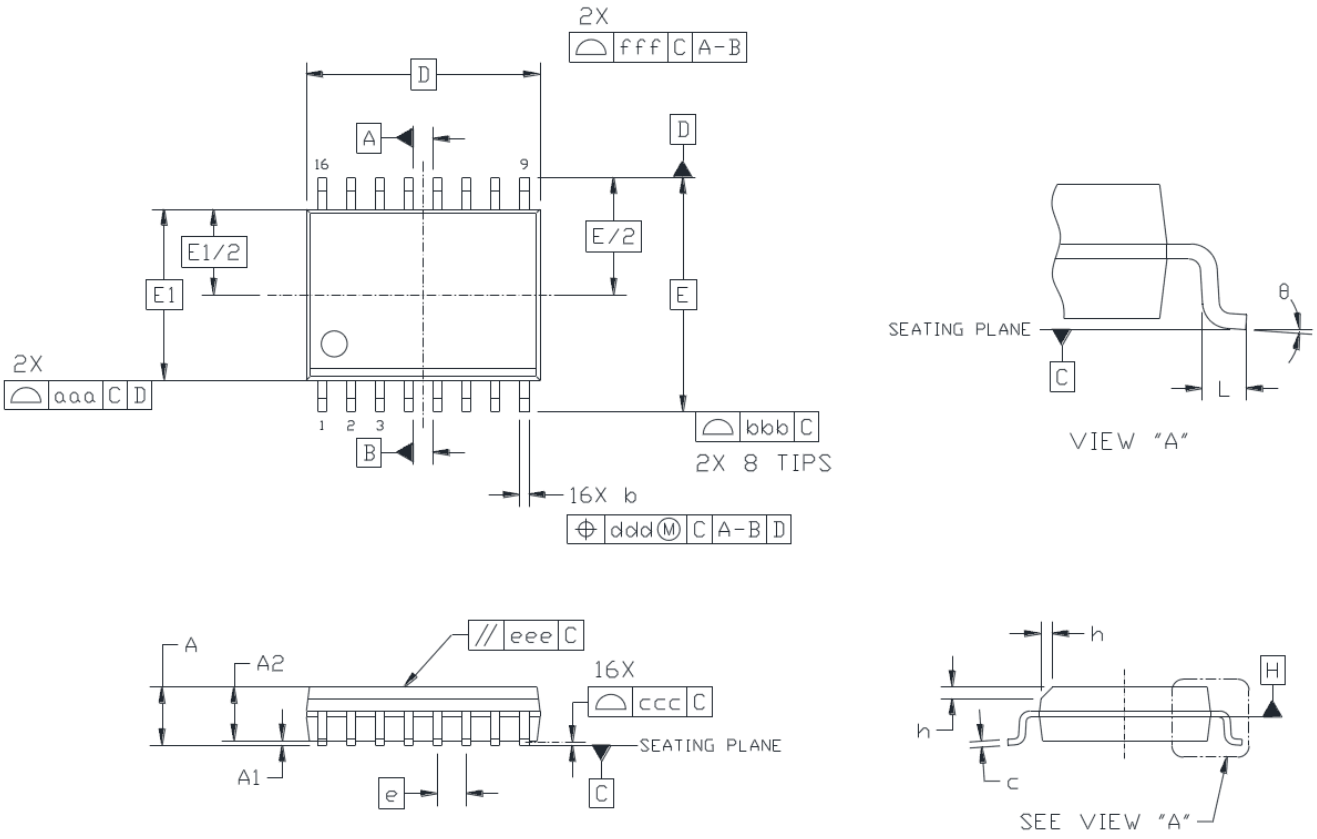

Figure 25. WB SOIC-16 Package

Table 20. WB SOIC-16 Package Diagram Dimensions [1, 2, 3, 4,]

Dimension	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	10.30 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
θ	0°	8°
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020 specification for small body, lead-free components.

8.2. Package Outline (NB SOIC-16)

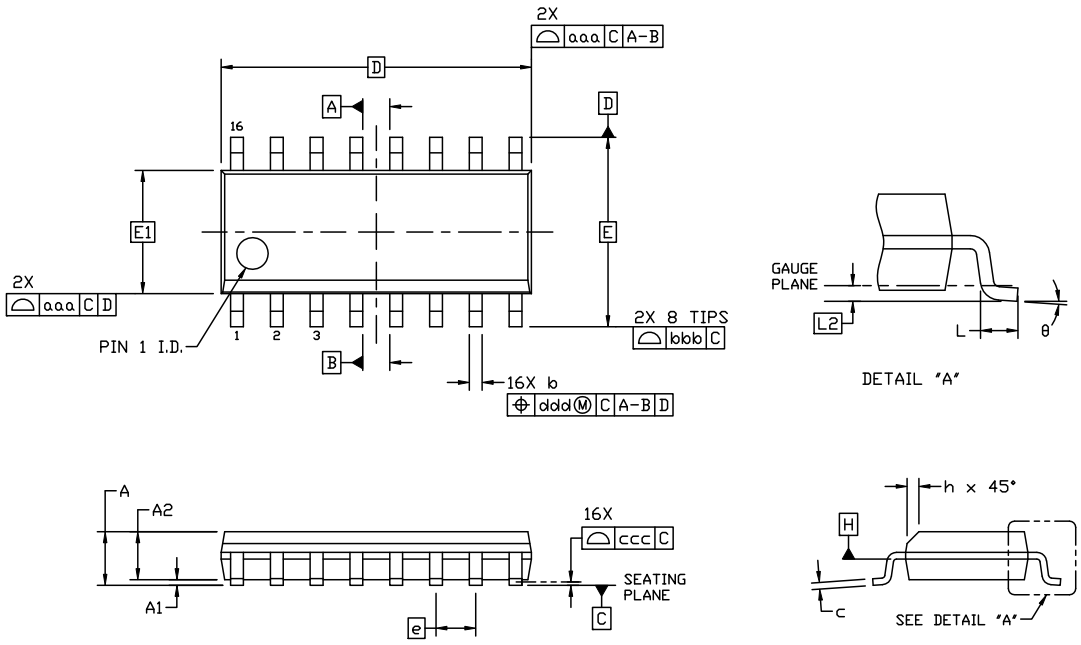

Figure 26. NB SOIC-16 Package

Table 21. NB SOIC-16 Package Diagram Dimensions [1,2,3,4]

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.17	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC solid state outline MS-012, variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.

8.3. Package Outline (QSOP-16)

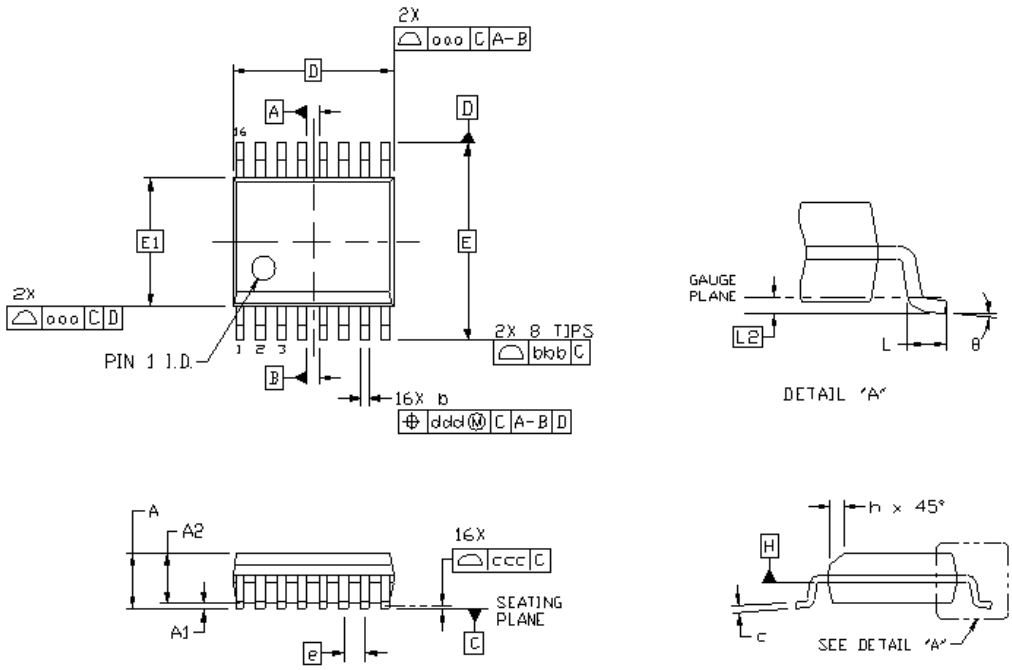

Figure 27. QSOP-16 Package

Table 22. QSOP-16 Package Diagram Dimensions[1,2,3,4]

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.20	0.30
c	0.17	0.25
D	4.89 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	0.635 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC solid state outline MO-137, variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.

9. Land Pattern

9.1. Land Pattern (WB SOIC-16)

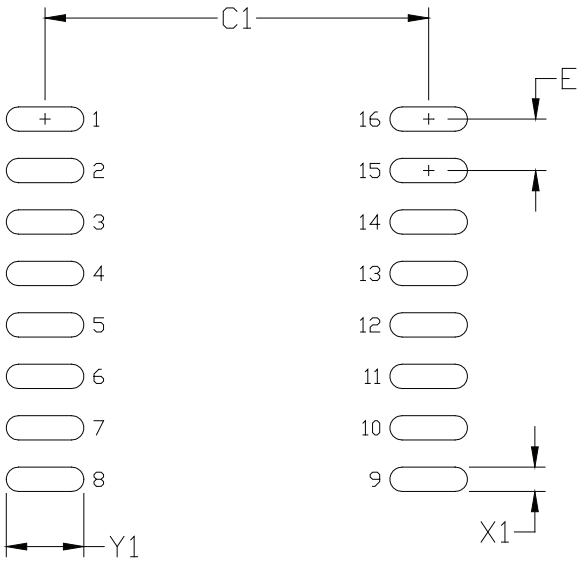

Figure 28. WB SOIC-16 PCB Land Pattern

Table 23. WB SOIC-16 Land Pattern Dimensions[1,2]

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.80
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.60

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

9.2. Land Pattern (NB SOIC-16)

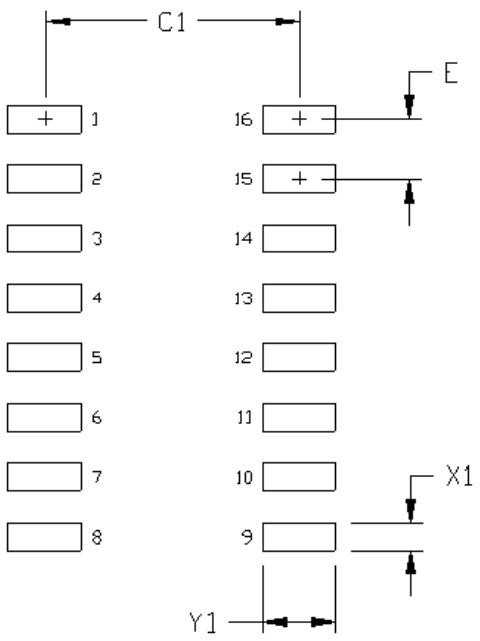

Figure 29. NB SOIC-16 PCB Land Pattern

Table 24. NB SOIC-16 Land Pattern Dimensions[1,2]

Dimension	Feature	(mm)
C1	Pad column spacing	5.40
E	Pad row pitch	1.27
X1	Pad width	0.60
Y1	Pad length	1.55

1. This land pattern design is based on IPC-7351 pattern SOIC127P600X165-16N for density level B (median land protrusion).
2. All feature sizes shown are at maximum material condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

9.3. Land Pattern (QSOP-16)

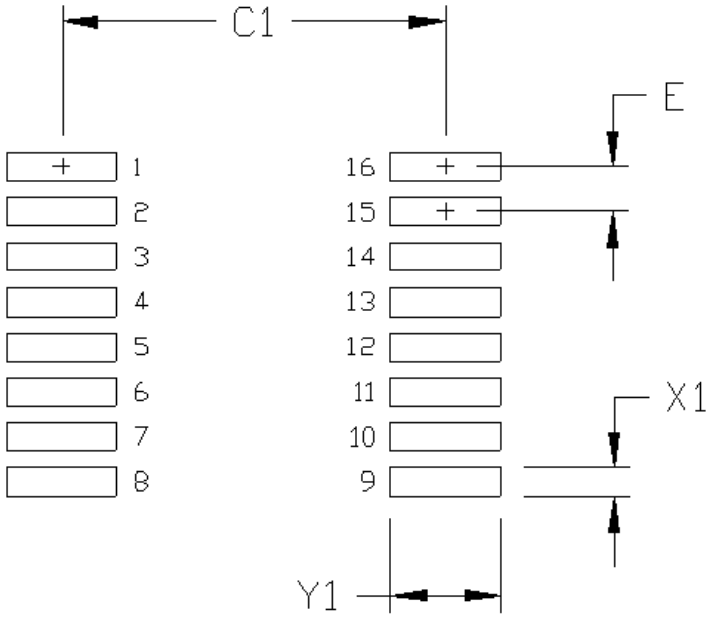

Figure 30. QSOP-16 PCB Land Pattern

Table 25. QSOP-16 Land Pattern Dimensions[1,2]

Dimension	Feature	(mm)
C1	Pad column spacing	5.40
E	Pad row pitch	0.635
X1	Pad width	0.40
Y1	Pad length	1.55

1. This land pattern design is based on IPC-7351 pattern SOP63P602X173-16N for density level B (median land protrusion).
2. All feature sizes shown are at maximum material condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

10. Top Marking

10.1. Top Marking (WB SOIC-16)

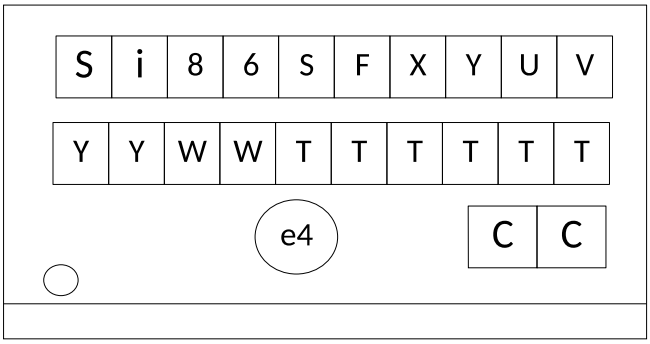

Figure 31. WB SOIC-16 Top Marking

Table 26. WB SOIC-16 Top Marking Explanation[1]

Line 1 Marking:	Base part number ordering options (See 11. Ordering Information for more information)	Si86S = Isolator product series F = product family 6 = Industry standard footprint L = Low power mode M = Sleep mode S = SPI compatible Q = Custom QSPI implementation X = Total # of channels Y = Total # of reverse channels (right to left) U = Default and deglitch option B = Output default low, no deglitch E = Output default high, no deglitch F = Output default low, 36 ns deglitch H = Output default high, 36 ns deglitch V = Isolation rating E = 6.0 kV_{RMS}
Line 2 Marking:	YY	Year of manufacturing at assembly house
	WW	Work week of manufacturing at assembly house
	TTTTTT	Manufacturing code from assembly house
Line 3 Marking:	Circle = 1.5 mm Diameter (Center Justified)	“e4” Pb-Free Symbol
	CC	Country of origin ISO code abbreviation

1. Automotive-grade part numbers are indicated on the shipping label.

10.2. Top Marking (NB SOIC-16)

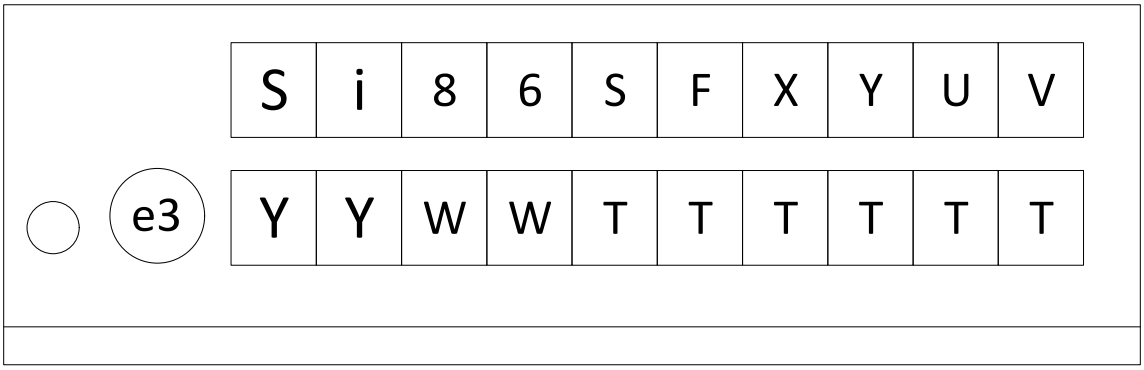

Figure 32. NB SOIC-16 Top Marking

Table 27. NB SOIC-16 Top Marking Explanation[1]

Line 1 Marking:	Base part number ordering options (See 1. Ordering Guide for more information)	Si86S = Isolator product series F = product family 6 = Industry standard footprint L = Low power mode M = Sleep mode S = SPI compatible Q = Custom QSPI implementation W = Wi-Fi bands 1.8 and 5.0 GHz plus DECT band compatible X = Total # of channels Y = Total # of reverse channels (right to left) U = Default and deglitch option B = Output default low, no deglitch E = Output default high, no deglitch F = Output default low, 36 ns deglitch H = Output default high, 36 ns deglitch V = Isolation rating C = 3.75 kV_{RMS}
Line 2 Marking:	YY	Year of manufacturing at assembly house
	WW	Work week of manufacturing at assembly house
	TTTTTT	Manufacturing code from assembly house
	Circle = 1.3 mm diameter	“e3” Pb-free symbol

1. Automotive-grade part numbers are indicated on the shipping label.

10.3. Top Marking (QSOP-16)

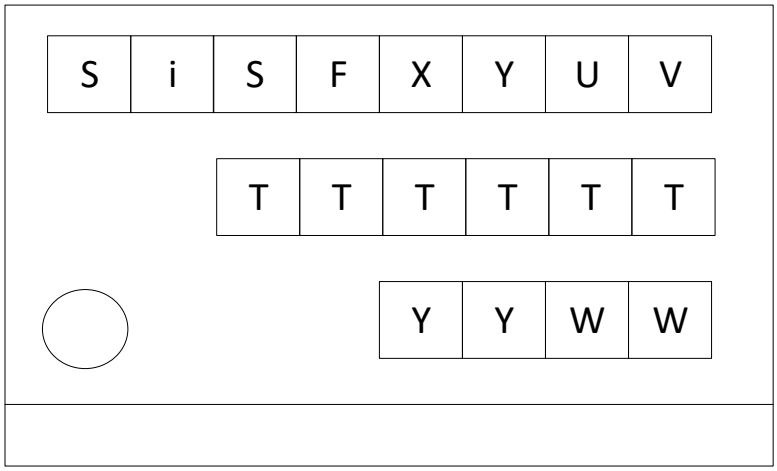

Figure 33. QSOP-16 Top Marking

Table 28. QSOP-16 Top Marking Explanation[1]

Line 1 Marking:	Base part number ordering options (See 11. Ordering Information for more information)	SiS = Si86S Isolator product series F = product family 6 = Industry standard footprint L = Low power mode M = Sleep mode S = SPI compatible Q = Custom QSPI implementation X = Total # of channels Y = Total # of reverse channels (right to left) U = Default and deglitch option B = Output default low, no deglitch E = Output default high, no deglitch F = Output default low, 36 ns deglitch H = Output default high, 36 ns deglitch V = Isolation rating B = 2.5 kV_{RMS}
Line 2 Marking:	TTTTTT	Manufacturing code from assembly house
Line 3 Marking:	YY	Year of manufacturing at assembly house
	WW	Work week of manufacturing at assembly house

1. Automotive-grade part numbers are indicated on the shipping label.

11. Ordering Information

Industrial and Automotive Grade OPNs

Industrial-grade devices (part numbers having an “-I” in their suffix) are built using well-controlled, high-quality manufacturing flows to ensure robustness and reliability. Qualifications are compliant with JEDEC, and defect reduction methodologies are used throughout definition, design, evaluation, qualification, and mass production steps.

Automotive-grade devices (part numbers having an “-A” in their suffix) are built using automotive-specific flows and additional statistical process controls at all steps in the manufacturing process to ensure robustness and low defectivity. These devices are supported with AIAG-compliant Production Part Approval Process (PPAP) documentation, and feature International Material Data System (IMDS) and China Automotive Material Data System (CAMDS) listings. Qualifications are compliant with AEC-Q100, and a zero-defect methodology is maintained throughout definition, design, evaluation, qualification, and mass production steps. Automotive-grade devices (with an “-A” suffix) are identical in construction materials, topside marking, and electrical parameters to their Industrial-Grade (with an “-I” suffix) version counterparts.

Table 29. Ordering Guide for 3-Channel Digital Isolators[1,2,3,4,5]

Ordering Part Numbers (OPNs)	Automotive OPNs[6]	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Deglitch Filter Delay (ns)	Default Output State	Isolation Rating (kV_{RMS})	Package
Si86S630BC-IS1	Si86S630BC-AS1	3	0	0	Low	3.75	NB SOIC-16
Si86S630BE-IS2	Si86S630BE-AS2	3	0	0	Low	6.0	WB SOIC-16
Si86S630EC-IS1	Si86S630EC-AS1	3	0	0	High	3.75	NB SOIC-16
Si86S630EE-IS2	Si86S630EE-AS2	3	0	0	High	6.0	WB SOIC-16
Si86S631BC-IS1	Si86S631BC-AS1	2	1	0	Low	3.75	NB SOIC-16
Si86S631BE-IS2	Si86S631BE-AS2	2	1	0	Low	6.0	WB SOIC-16
Si86S631EC-IS1	Si86S631EC-AS1	2	1	0	High	3.75	NB SOIC-16
Si86S631EE-IS2	Si86S631EE-AS2	2	1	0	High	6.0	WB SOIC-16

1. Refer to 10. Top Marking for the product decoder.
2. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
3. “Si” and “SI” are used interchangeably.
4. An “R” at the end of the part number denotes tape and reel packaging option.
5. Temperature range is –40 to 125 °C.
6. In the top markings of each device, the manufacturing code represented by “TTTTTT” contains, as its first character, a letter in the range N through Z to indicate automotive-grade.

Table 30. Ordering Guide for 4-Channel Digital Isolators[1,2,3,4]

Ordering Part Numbers (OPNs)	Automotive OPNs[5,6]	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Deglitch Filter Delay (ns)	Default Output State	Isolation Rating (kV_{RMS})	Package
Si86S640BC-IS1	Si86S640BC-AS1	4	0	0	Low	3.75	NB SOIC-16
Si86S640BB-IU	Si86S640BB-AU	4	0	0	Low	2.5	QSOP-16
Si86S640BE-IS2	Si86S640BE-AS2	4	0	0	Low	6.0	WB SOIC-16
Si86S640EC-IS1	Si86S640EC-AS1	4	0	0	High	3.75	NB SOIC-16
Si86S640EB-IU	Si86S640EB-AU	4	0	0	High	2.5	QSOP-16
Si86S640EE-IS2	Si86S640EE-AS2	4	0	0	High	6.0	WB SOIC-16
Si86S641BC-IS1	Si86S641BC-AS1	3	1	0	Low	3.75	NB SOIC-16
Si86S641BB-IU	Si86S641BB-AU	3	1	0	Low	2.5	QSOP-16
Si86S641BE-IS2	Si86S641BE-AS2	3	1	0	Low	6.0	WB SOIC-16
Si86S641EC-IS1	Si86S641EC-AS1	3	1	0	High	3.75	NB SOIC-16
Si86S641EB-IU	Si86S641EB-AU	3	1	0	High	2.5	QSOP-16
Si86S641EE-IS2	Si86S641EE-AS2	3	1	0	High	6.0	WB SOIC-16
Si86SW41BC-IS1	Si86SW41BC-AS1	3	1	0	Low	3.75	NB SOIC-16
Si86S642BC-IS1	Si86S642BC-AS1	2	2	0	Low	3.75	NB SOIC-16
Si86S642BB-IU	Si86S642BB-AU	2	2	0	Low	2.5	QSOP-16
Si86S642BE-IS2	Si86S642BE-AS2	2	2	0	Low	6.0	WB SOIC-16
Si86S642EC-IS1	Si86S642EC-AS1	2	2	0	High	3.75	NB SOIC-16
Si86S642EB-IU	Si86S642EB-AU	2	2	0	High	2.5	QSOP-16
Si86S642EE-IS2	Si86S642EE-AS2	2	2	0	High	6.0	WB SOIC-16
Si86S640FC-IS1	Si86S640FC-AS1	4	0	36	Low	3.75	NB SOIC-16
Si86S640FE-IS2	Si86S640FE-AS2	4	0	36	Low	6.0	WB SOIC-16
Si86S640HC-IS1	Si86S640HC-AS1	4	0	36	High	3.75	NB SOIC-16
Si86S640HE-IS2	Si86S640HE-AS2	4	0	36	High	6.0	WB SOIC-16
Si86S641FC-IS1	Si86S641FC-AS1	3	1	36	Low	3.75	NB SOIC-16
Si86S641FE-IS2	Si86S641FE-AS2	3	1	36	Low	6.0	WB SOIC-16
Si86S641HC-IS1	Si86S641HC-AS1	3	1	36	High	3.75	NB SOIC-16
Si86S641HE-IS2	Si86S641HE-AS2	3	1	36	High	6.0	WB SOIC-16
Si86S642FC-IS1	Si86S642FC-AS1	2	2	36	Low	3.75	NB SOIC-16
Si86S642FE-IS2	Si86S642FE-AS2	2	2	36	Low	6.0	WB SOIC-16
Si86S642HC-IS1	Si86S642HC-AS1	2	2	36	High	3.75	NB SOIC-16
Si86S642HE-IS2	Si86S642HE-AS2	2	2	36	High	6.0	WB SOIC-16
Low-Power Mode							
Si86SL40BC-IS1	Si86SL40BC-AS1	4	0	0	Low	3.75	NB SOIC-16
Si86SL40BE-IS2	Si86SL40BE-AS2	4	0	0	Low	6.0	WB SOIC-16
Si86SL40EC-IS1	Si86SL40EC-AS1	4	0	0	High	3.75	NB SOIC-16
Si86SL40EE-IS2	Si86SL40EE-AS2	4	0	0	High	6.0	WB SOIC-16
Si86SL41BC-IS1	Si86SL41BC-AS1	3	1	0	Low	3.75	NB SOIC-16
Si86SL41BE-IS2	Si86SL41BE-AS2	3	1	0	Low	6.0	WB SOIC-16
Si86SL41EC-IS1	Si86SL41EC-AS1	3	1	0	High	3.75	NB SOIC-16
Si86SL41EE-IS2	Si86SL41EE-AS2	3	1	0	High	6.0	WB SOIC-16
Si86SL42BC-IS1	Si86SL42BC-AS1	2	2	0	Low	3.75	NB SOIC-16
Si86SL42BE-IS2	Si86SL42BE-AS2	2	2	0	Low	6.0	WB SOIC-16
Si86SL42EC-IS1	Si86SL42EC-AS1	2	2	0	High	3.75	NB SOIC-16
Si86SL42EE-IS2	Si86SL42EE-AS2	2	2	0	High	6.0	WB SOIC-16

Table 30. Ordering Guide for 4-Channel Digital Isolators[1,2,3,4]

Ordering Part Numbers (OPNs)	Automotive OPNs[5,6]	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Deglitch Filter Delay (ns)	Default Output State	Isolation Rating (kV_{RMS})	Package
Sleep Mode							
Si86SM40BC-IS1	Si86SM40BC-AS1	4	0	0	Low	3.75	NB SOIC-16
Si86SM40BE-IS2	Si86SM40BE-AS2	4	0	0	Low	6.0	WB SOIC-16
Si86SM40EC-IS1	Si86SM40EC-AS1	4	0	0	High	3.75	NB SOIC-16
Si86SM40EE-IS2	Si86SM40EE-AS2	4	0	0	High	6.0	WB SOIC-16
Si86SM41BC-IS1	Si86SM41BC-AS1	3	1	0	Low	3.75	NB SOIC-16
Si86SM41BE-IS2	Si86SM41BE-AS2	3	1	0	Low	6.0	WB SOIC-16
Si86SM41EC-IS1	Si86SM41EC-AS1	3	1	0	High	3.75	NB SOIC-16
Si86SM41EE-IS2	Si86SM41EE-AS2	3	1	0	High	6.0	WB SOIC-16
Si86SM42BC-IS1	Si86SM42BC-AS1	2	2	0	Low	3.75	NB SOIC-16
Si86SM42BE-IS2	Si86SM42BE-AS2	2	2	0	Low	6.0	WB SOIC-16
Si86SM42EC-IS1	Si86SM42EC-AS1	2	2	0	High	3.75	NB SOIC-16
Si86SM42EE-IS2	Si86SM42EE-AS2	2	2	0	High	6.0	WB SOIC-16
SPI Mode							
Si86SS41BC-IS1	Si86SS41BC-AS1	3	1	0	Low	3.75	NB SOIC-16
Si86SS41BE-IS2	Si86SS41BE-AS2	3	1	0	Low	6.0	WB SOIC-16
Si86SS41EC-IS1	Si86SS41EC-AS1	3	1	0	High	3.75	NB SOIC-16
Si86SS41EE-IS2	Si86SS41EE-AS2	3	1	0	High	6.0	WB SOIC-16
Si86SS51BC-IS1	Si86SS51BC-AS1	4	1	0	Low	3.75	NB SOIC-16
Si86SS51BE-IS2	Si86SS51BE-AS2	4	1	0	Low	6.0	WB SOIC-16
Si86SS51EC-IS1	Si86SS51EC-AS1	4	1	0	High	3.75	NB SOIC-16
Si86SS51EE-IS2	Si86SS51EE-AS2	4	1	0	High	6.0	WB SOIC-16
Custom QSPI Implementation Mode							
Si86SQ44BB-IU	Si86SQ44BB-AU	4	0	0	Low	2.5	QSOP-16
Si86SQ44BE-IS2	Si86SQ44BE-AS2	4	0	0	Low	6.0	WB SOIC-16
Si86SQ44EB-IU	Si86SQ44EB-AU	4	0	0	High	2.5	QSOP-16
Si86SQ44EE-IS2	Si86SQ44EE-AS2	4	0	0	High	6.0	WB SOIC-16

1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
2. “Si” and “SI” are used interchangeably.
3. An “R” at the end of the part number denotes tape and reel packaging option.
4. Temperature range is –40 to 125 °C.
5. Automotive-grade devices (with an “–A” suffix) are identical in construction materials, topside marking, and electrical parameters to their industrial-grade (with an “–I” suffix) version counterparts. automotive-grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The automotive-grade part number is included on shipping labels.
6. In the top markings of each device, the manufacturing code represented by “TTTTTT” contains, as its first character, a letter in the range N through Z to indicate automotive-grade.

Table 31. Ordering Guide for 6-Channel Digital Isolators[1,2,3,4]

Ordering Part Numbers (OPNs)	Automotive OPNs[5,6]	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Deglitch Filter Delay (ns)	Default Output State	Isolation Rating (kV_{RMS})	Package
Si86S660BC-IS1	Si86S660BC-AS1	6	0	0	Low	3.75	NB SOIC-16
Si86S660BB-IU	Si86S660BB-AU	6	0	0	Low	2.5	QSOP-16
Si86S660BE-IS2	Si86S660BE-AS2	6	0	0	Low	6.0	WB SOIC-16
Si86S660EC-IS1	Si86S660EC-AS1	6	0	0	High	3.75	NB SOIC-16
Si86S660EB-IU	Si86S660EB-AU	6	0	0	High	2.5	QSOP-16
Si86S660EE-IS2	Si86S660EE-AS2	6	0	0	High	6.0	WB SOIC-16
Si86S661BC-IS1	Si86S661BC-AS1	5	1	0	Low	3.75	NB SOIC-16
Si86S661BB-IU	Si86S661BB-AU	5	1	0	Low	2.5	QSOP-16
Si86S661BE-IS2	Si86S661BE-AS2	5	1	0	Low	6	WB SOIC-16
Si86S661EC-IS1	Si86S661EC-AS1	5	1	0	High	3.75	NB SOIC-16
Si86S661EB-IU	Si86S661EB-AU	5	1	0	High	2.5	QSOP-16
Si86S661EE-IS2	Si86S661EE-AS2	5	1	0	High	6	WB SOIC-16
Si86SW62BC-IS1	Si86SW62BC-AS1	4	2	0	Low	3.75	NB SOIC-16
Si86S662BC-IS1	Si86S662BC-AS1	4	2	0	Low	3.75	NB SOIC-16
Si86S662BB-IU	Si86S662BB-AU	4	2	0	Low	2.5	QSOP-16
Si86S662BE-IS2	Si86S662BE-AS2	4	2	0	Low	6	WB SOIC-16
Si86S662EC-IS1	Si86S662EC-AS1	4	2	0	High	3.75	NB SOIC-16
Si86S662EB-IU	Si86S662EB-AU	4	2	0	High	2.5	QSOP-16
Si86S662EE-IS2	Si86S662EE-AS2	4	2	0	High	6	WB SOIC-16
Si86S663BC-IS1	Si86S663BC-AS1	3	3	0	Low	3.75	NB SOIC-16
Si86S663BB-IU	Si86S663BB-AU	3	3	0	Low	2.5	QSOP-16
Si86S663BE-IS2	Si86S663BE-AS2	3	3	0	Low	6.0	WB SOIC-16
Si86S663EC-IS1	Si86S663EC-AS1	3	3	0	High	3.75	NB SOIC-16
Si86S663EB-IU	Si86S663EB-AU	3	3	0	High	2.5	QSOP-16
Si86S663EE-IS2	Si86S663EE-AS2	3	3	0	High	6.0	WB SOIC-16

1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
2. “Si” and “SI” are used interchangeably.
3. An “R” at the end of the part number denotes tape and reel packaging option.
4. Temperature range is –40 to 125 °C.
5. Automotive-grade devices (with an “–A” suffix) are identical in construction materials, topside marking, and electrical parameters to their industrial-grade (with an “–I” suffix) version counterparts. Automotive-grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The automotive-grade part number is included on shipping labels.
6. In the top markings of each device, the manufacturing code represented by “TTTTTT” contains, as its first character, a letter in the range N through Z to indicate automotive-grade.

12. Revision History

Revision	Date	Description
B	August, 2023	Corrected max PWD specifications in: "4. Electrical Specifications" on page 18. Corrections and clarifications made in: Table 13, "Regulatory Information (Pending)," on page 34, Table 15, "IEC 60664-1 Ratings," on page 35, Table 16, "IEC 60747-17 Insulation Characteristics for Si86Sx," on page 35, and Table 17, "UL 1577 Insulation Characteristics," on page 35. Corrections and clarifications made in: "6. Typical Performance Characteristics" on page 37. Formatting and typo corrections made for Si86SW62BC-IS1 line item in: "11. Ordering Information" on page 49. Updated "9.1. Land Pattern (WB SOIC-16)" on page 43.
A	April, 2023	Production release.
0.5	August, 2022	Preview version.

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