



**THE DATASHEET OF
TMD5ADP1460**



JTAG Emulation Adapter Board Kit 14e-60t

Quick Start Guide

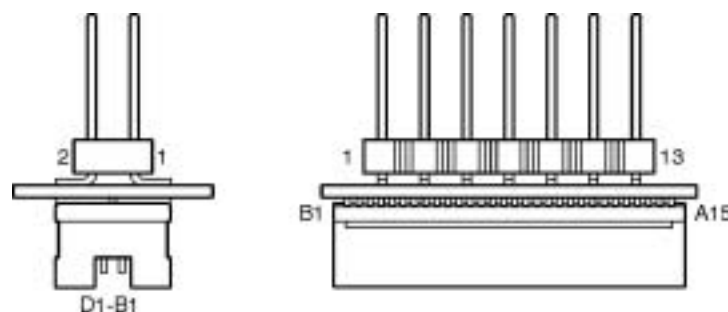


Figure 1. JTAG Emulation Adapter Board

Overview

The 14e-60t JTAG Emulation Adapter Board is designed to allow targets containing Texas Instruments' 60-pin Next Generation Emulation Interface to be used with traditional fielded 14-pin emulation hardware (e.g. XDS510 and XDS560). See 60-Pin Emulation Header Technical Reference SPRU655A for more information.

Compatibility

This adapter is designed to be backwards compatible with traditional 14-pin emulators and to support common JTAG functions: TMS, TRST/, TDI, TVD, TDO, TCKRTN, TCK, EMU0 and EMU1.

Mechanical Considerations

The new 14-pin emulator to 60-pin target adapter board was designed using quality components and an FR-4 base-laminate material suitable of supporting most legacy board designs and speeds. Board thickness was maintained at 0.0625" (customary for current designs). The connectors chosen were based on performance and life-cycle count. The adapter board was designed for a character impedance of approximately 50 ohm to reduce the mismatch with typical target boards.

WARNING:

Please consult page 2 of this Quick Start Guide regarding installation of the 14e-60t adapter. The 60-pin interface is not keyed and needs to be correctly oriented for proper emulator operation.

The following tables are provided for your assistance. Table 1 specifies the pinout of the 14-pin (top) emulator connector. Table 2 specifies the pinout of the 60-pin (bottom) target connector.

Pin	Name	Pin	Name
1	TMS	2	TRST/
3	TDI	4	TDIS
5	TVD	6	KEY
7	TDO	8	GND
9	TCKRTN	10	GND
6	TCLK	12	GND
13	EMU0	14	EMU1

Table 1. 14-Pin JTAG Header Pinout

Table 2. 60-Pin Header Pinout (14e-60t Adapter only)

Pin	A	B	C	D
1	GND	N/C	N/C	N/C
2	GND	TMS	N/C	GND
3	GND	N/C	TRST/	GND
4	GND	TDI	N/C	GND
5	GND	N/C	N/C	GND
6	GND	N/C	N/C	GND
7	GND	TDO	N/C	GND
8	N/C	TVD	TCLKRTN	GND
9	GND	N/C	N/C	GND
10	GND	N/C	N/C	GND
11	GND	N/C	N/C	GND
12	GND	TCLK	N/C	GND
13	GND	N/C	N/C	GND
14	GND	EMU0	EMU1	GND
15	N/C	N/C	N/C	GND

Key Notes / Concerns

Orientation

The 14e-60t adapter is designed with a keyed pin for the classic 14-pin emulator header only (located on pin 6). Use caution when inserting the 60-pin interface to the target-interface board. If the 60-pin interface is installed 180° incorrectly, damage can occur to the target, adapter, and emulator. The adapter has specific markings (silk screen) intended to assist you in proper installation. Be sure to align the adapter so that the silk screen is oriented correctly. Two specific markings are available for your assistance, DSP and Cable Entry. Figure 2 illustrates the top view of the adapter and respective silk screen markings.

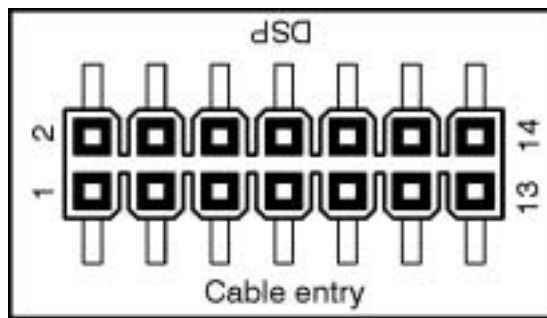


Figure 2. 60-Pin Connector Silk Screen Markings

CAUTION:

Texas Instruments Incorporated does not warrant this product, your emulation tool(s), or target if your adapter is installed incorrectly or the actual target connector is incorrectly connected electrically. Pay close attention to orientation and pin out.

Performance

Functionality and performance should always be a consideration when designing and using an adapter. For any critical signals, it is recommended that simulation and modeling be performed. The use of an adapter induces additional node lengths that may increase signal reflections or crosstalk.

This 60-pin test adapter is not intended to be hot pluggable, damage can occur! TVD, pin 5 on your current JTAG header, is intended to provide a Target Voltage Detect to the emulation system. Proper configuration of this pin is mandatory. The use of any adapter, alternate interface or incorrect connection to this new header may dramatically affect the performance of your system. Texas Instruments' next generation emulation header requires the correct pin out of all target board signals per Table 2. Consequently, all emulator pod signals should be wired in accordance with Table 1.

It is strongly recommended that the target interface board be impedance matched and that the printed circuit board traces have a co-planarity suitable for the trace width and pitch. Choice of trace widths and spacing should conform to good engineering practices and be made compatible with current manufacturing technologies (4/4, 4/3, or 3/3).

Basic JTAG functionality utilizing this adapter should result in no apparent performance degradation. The additional advanced features supported on the new 60-pin interface connector and Next Generation Emulator are not supported when using this adapter.

Damage

As with any component, damage can occur if the adapter is mishandled, misused or forced into place. Should your adapter become damaged for any reason, Texas Instruments recommends the purchase of a new adapter. Damaged adapters should be discarded to prevent future use.

Upgrades

Upgrades to Texas Instruments' emulation adapters are not planned. These adapters are provided for a limited time until a sufficient amount of proper tools are available to interface with the new emulation connector.

Disclaimers

Read the following for important information to be aware of:

- Successful use of Texas Instruments next generation emulation interface for HS-RTDX and trace capture requires the use of good engineering design practices when developing target interface boards.
- Connector choice is extremely important, excessive insertion and removal forces will reduce the

life of your interface. Follow the connector manufacturer's specifications for pad placement, layout and processing. Failure to do so may result in the shorting of connections, poor processing and potential damage to your target or emulator / pod assembly.

- Texas Instruments is not responsible for co-planarity problems in manufacturing where connector assembly is concerned. Choose your printed circuit board plating material wisely.
- Target board impedance mismatch and the results of such a mismatch can be detrimental to the performance of the emulation platform, amongst other potential problems.
- Excessive capacitance loading due to long trace lengths, added vias, connectors or test points causes reduced performance and less than adequate results. Minimize the capacitive loading on every trace to and from the header.

Texas Instruments has taken into account a reasonable amount of skew for its new emulation interface and supporting new hardware. Excessive signal skew may cause undesirable results. This is a costly correction and usually requires the respin of a target board. Spend the appropriate amount of time up front to validate your design.

Logic (Schematic) Details

Figure 3 represents the logic design and pinout for the 14-pin target to 60-pin emulator adapter.

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