THE DATASHEET OF

A3938SLDTR

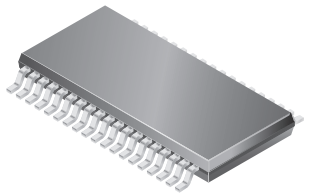
A3938

Three-Phase Power MOSFET Controller

FEATURES AND BENEFITS

- Drives a wide range of N-channel MOSFETs
- Low-side synchronous rectification
- Power MOSFET protection
- Adjustable dead time for cross-conduction protection
- Selectable coast or dynamic brake on power-down or RESET input
- Fast/slow current decay modes
- Internal PWM current control
- Motor lead short-to-ground protection
- Internal 5 V regulator
- Fault diagnostic output
- Thermal shutdown
- Undervoltage protection

Package 38-pin TSSOP (suffix LD):



Not to scale

DESCRIPTION

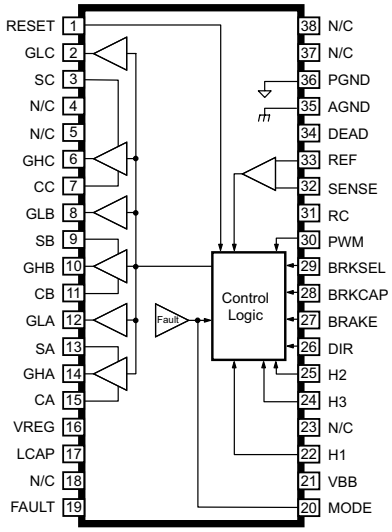
The A3938 is a three-phase, brushless DC motor controller. It has a high-current gate drive capability that allows driving of a wide range of power MOSFETs and can support motor supply voltages to 50 V. The A3938 integrates a bootstrapped high-side driver to minimize the external component count required to drive N-channel MOSFET drivers.

Internal fixed off-time, PWM current-control circuitry can be used to regulate the maximum load current to a desired value. The peak load current limit is set by the user's selection of an input reference voltage and external sensing resistor. A user-selected external RC timing network sets the fixed off-time pulse duration. For added flexibility, the PWM input can provide speed/torque control where the internal current control circuit sets a limit on the maximum current.

The A3938 includes a synchronous rectification feature. This shorts out the current path through the power MOSFET reverse body diodes during PWM off-cycle current decay. This can minimize power dissipation in the MOSFETs, eliminate the need for external power clamp diodes, and potentially allow a more economical choice for the MOSFET drivers.

The A3938 provides commutation logic for Hall sensors configured for 120-degree spacing. The H-all input pins are pulled-up to an internally-generated 5 V reference. Power MOSFET protection features include: bootstrap capacitor charging current monitor, regulator undervoltage monitor, motor lead short-to-ground, and thermal shutdown.

The LD package is lead (Pb) free, with 100% matte tin plated leadframe.



SELECTION GUIDE

Part Number	Packing
A3938SLDTR-T	4000 per reel

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	V_{BB}		50	V
VREG Pin, Transient	V_{REG}		15	V
Logic Input Voltage Range	V_{IN}		–0.3 to V_{LCAP} + 0.3	V
Sense Voltage Range	V_{SENSE}		–5 to 1.5	V
Output Voltage Range				V
SA, SB, SC Pins			–5 to 50	V
GHA, GHB, GHC Pins			–5 to V_{BB} + 17	V
CA, CB, CC Pins			V_{Sx} + 17	V
Operating Ambient Temperature	T_A	Range S	–20 to 85	°C
Junction Temperature	T_J		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions

Characteristic	Symbol	Test Conditions	Min.	Units
Package Thermal Resistance	$R_{\theta JA}$	LD package, 4 layer PCB based on JEDEC standard	51	°C/W

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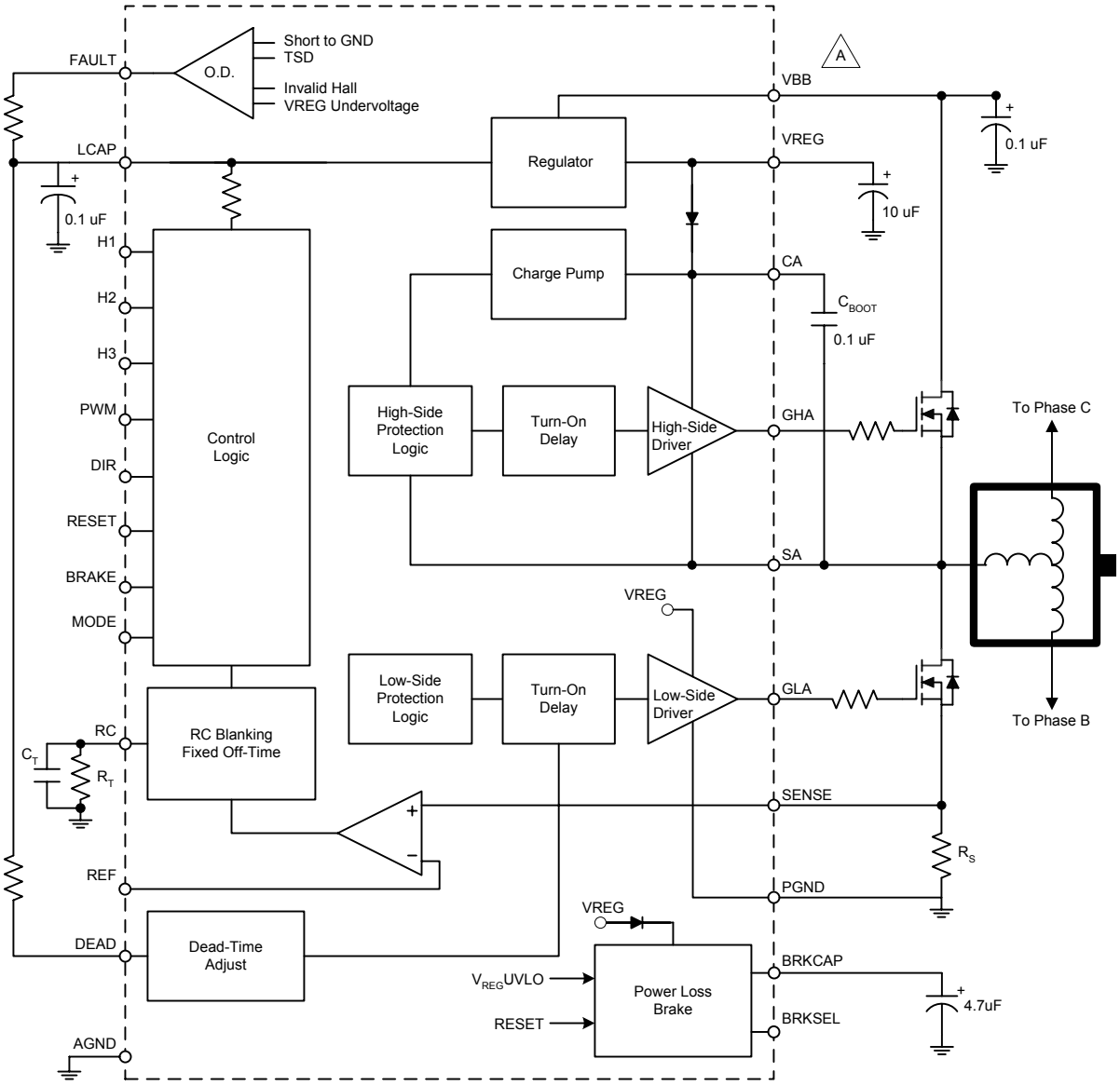
FUNCTIONAL BLOCK DIAGRAM

(This diagram shows only one of the three outputs)



A For 12 V applications, VBB must be shorted to VREG. For this condition, the absolute maximum rating of 15 V on VREG must be maintained to prevent damage to the A3938.

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ELECTRICAL CHARACTERISTICS [1][2] Unless otherwise noted: T_A = 25°C, V_{BB} = 18 V to 50 V, C_{LCAP} = 0.1 µF, C_{BOOT} = 0.1 µF, C_{VREG} = 10 µF, PWM = 22.5 kHz, square wave, two phases active

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Units
Quiescent Current	I_{VBB}	RESET = 1, Coast mode, stopped	–	–	8.0	mA
LCAP Regulator	V_{LCAP}	I_{lcap} = –3.0 mA	4.75	5	5.25	V
VREG = VBB Supply Voltage Range	V_{REG}	VREG = VBB, observe maximum rating = 15 V	10.8	–	13.2	V
VREG Output Voltage	V_{REG}	V_{BB} = 13.2 V to 18 V, I_{vreg} = –10 mA	–	V_{BB} – 2.5	–	V
		V_{BB} = 18 V to 50 V, I_{vreg} = –10 mA	12.4	13	13.6	V
VREG Load Regulation	$V_{REGLOAD}$	I_{vreg} = –1 mA to –30 mA, Coast mode	–	25	–	mV
VREG Line Regulation	V_{REGLIN}	I_{vreg} = –10 mA, Coast mode	–	40	–	mV
CONTROL LOGIC						
Logic Input Voltage	$V_{IN(1)}$	Minimum high level for logical 1	2.0	–	–	V
	$V_{IN(0)}$	Maximum low level for logical 0	–	–	0.8	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = 2.0 V	–30	–	–90	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	–50	–	–130	µA
GATE DRIVE						
Low-Side Drive, Output High	V_{HGL}	I_{gx} = 0	V_{REG} – 0.8	V_{REG} – 0.5	–	V
High-Side Drive, Output High	V_{HGH}	I_{gx} = 0	10.4	11.6	12.8	V
Pull-Up Switch Resistance	$R_{DS(ON)}$	I_{gx} = –50 mA	–	14	–	Ω
Pull-Down Switch Resistance	$R_{DS(ON)}$	I_{gx} = 50 mA	–	4	–	Ω
Low-Side Switching, 10/90 Rise Time	t_{rGL}	C_{load} = 3300 pF	–	120	–	ns
Low-Side Switching, 10/90 Fall Time	t_{fGL}	C_{load} = 3300 pF	–	60	–	ns
High-Side Switching, 10/90 Rise Time	t_{rGH}	C_{load} = 3300 pF	–	120	–	ns
High-Side Switching, 10/90 Fall Time	t_{fGH}	C_{load} = 3300 pF	–	60	–	ns
Propagation Delay; GHx,GLx Rising	t_{pr}	PWM to gate drive out, C_{load} = 3300 pF	–	220	–	ns
Propagation Delay; GHx,GLx Falling	t_{pf}	PWM to gate drive out, C_{load} = 3300 pF	–	110	–	ns
Dead Time, Maximum	t_{DEAD}	V_{dead} = 0, GHx to GLx, C_{load} = 0	3.5	5.6	7.6	µs
Dead Time, Minimum	t_{DEAD}	I_{DEAD} = 780 µA, GLx to GHx, C_{load} = 0	50	100	150	ns

Continued on next page...

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ELECTRICAL CHARACTERISTICS [1][2] *(continued)* Unless otherwise noted: T_A = 25°C, V_{BB} = 18 V to 50 V, C_{LCAP} = 0.1 µF, C_{BOOT} = 0.1 µF, C_{VREG} = 10 µF, PWM = 22.5 kHz, square wave, two phases active

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Units
BOOTSTRAP CAPACITOR						
Bootstrap Capacitor Voltage	V_{CX}	I_{cx} = 0, V_{sx} = 0, V_{reg} = 13 V	10.4	11.6	12.8	V
Bootstrap R_{OUT}	R_{CX}	I_{cx} = –50 mA	–	9	12	Ω
Charge Current (Source)	I_{CX}		100	–	–	mA
CURRENT LIMIT CIRCUITRY						
Input Offset Voltage	V_{IO}	0 V < V_{cmr} < 1.5 V	–	–	± 5	mV
Input Current, Sense pin	I_B	0 V < V_{cm}, V_{diff} < 1.5 V	–	–25	–	µA
Input Current, Reference pin	I_B	0 V < V_{cm}, V_{diff} < 1.5 V	–	0	–	µA
Blank Time	t_{BLANK}	R = 56 kΩ, C = 470 pF	–	0.91	–	µs
RC Charge Current	I_{RC}		–0.9	–1	–1.1	mA
RC Voltage Threshold	V_{RCL}		1.0	1.1	1.2	V
	V_{RCH}		2.7	3.0	3.3	V
PROTECTION CIRCUITRY						
Bootstrap Charge Threshold	I_{cx}	GHx turns on, and GLx turns off, at I_{cx}	–	–9	–	mA
Short to Ground, Drain-Source Monitor	V_{dsh}	V_{BB} – V_{SX}, high side on	1.3	2.0	2.7	V
VREG Undervoltage Threshold	V_{UVLO}	V_{REG} increasing	9.2	9.7	10.2	V
		V_{REG} decreasing	8.6	9.1	9.6	V
Fault Output Voltage	V_{OUT}	I_{OL} = 1 mA	–	–	0.5	V
Brake Capacitor Supply Current	I_{BRAKE}	V_{BB} = 8 V, BRKSEL = 1	–	30	–	µA
Low Side Gate Voltage	V_{GLBH}	V_{BB} = 0, BRKCAP = 8 V	–	6.6	–	V
Thermal Shutdown Temperature	T_J		–	165	–	°C
Thermal Shutdown Hysteresis	ΔT_J		–	10	–	°C

[1] Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.

[2] Negative current is defined as conventional current coming out of (sourced from) the specified device terminal.

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PIN DESCRIPTIONS

RESET. A logic input that enables the device. Has internal 50 kΩ pull-up to LCAP. Setting RESET to 1 coasts or brakes the motor, depending on the state of the BRKSEL pin. Setting RESET to 0 enables the gate drive to follow commutation logic. Setting RESET to 1 overrides the BRAKE pin.

GLA/GLB/GLC. Low-side gate drive outputs for external MOSFET drivers. External series gate resistors can be used to control slew rate seen at the power driver gate, thereby controlling the *di*/*dt* and *dv*/*dt* of Sx outputs.

SA/SB/SC. Directly connected to the motor terminals, these pins sense the voltages switched across the load. The pins are also connected to the negative side of the bootstrap capacitors and the negative supply connections for the floating high-side drivers.

GHA/GHB/GHC. High-side gate drive outputs for N-channel MOSFET drivers. External series gate resistors can be used to control slew rate seen at the power driver gate, thereby controlling the *di*/*dt* and *dv*/*dt* of Sx outputs.

CA/CB/CC. High-side connections for bootstrap capacitors, providing positive supply for high-side gate drivers. The bootstrap capacitors are charged to approximately VREG when the output Sx terminals go low. When the outputs swing high, the voltages on these pins rise with the outputs to provide the boosted gate voltages needed for the N-channel power MOSFETs.

MODE. Logic input to set current-decay mode. In response to a PWM Off command, Slow Decay mode (MODE = 1) switches off the high-side FET, and Fast Decay mode (MODE = 0) switches off the high-side and low-side FETs. Has an internal 50 kΩ pull-up to LCAP.

H1/H2/H3. Hall sensor inputs with internal, 50 kΩ pull-ups to LCAP. Configured for 120-degree electrical spacing.

DIR. Logic input to reverse rotation (see the table Commutation Truth Table, on the next page). Has internal, 50 kΩ pull-up to LCAP.

FAULT. Open-drain output to indicate fault condition. Will be pulled high (usually by 5.1 kΩ external pull-up) for any of the following fault conditions:

- Invalid Hall sensor input code (coasts the motor).
- Undervoltage condition detected at VREG (coasts or brakes the motor depending on stored setting for BRKSEL).
- Thermal shutdown (coasts the motor).
- Motor lead (SA/SB/SC) connected to ground (turns off only the high-side power MOSFETs).

Only the "short-to-ground" fault is latched, but it is cleared at each commutation. If the motor has stalled due to a short-to-ground being detected, toggling the RESET pin or repeating a power-up sequence clears the fault.

BRAKE. Logic input for braking function. Setting BRAKE to 1 turns on low-side MOSFETs, and turns off the high-side MOSFETs. This effectively shorts the BEMF in the windings and brakes the motor. Internal 50 kΩ pull-up to LCAP. Setting RESET to 1 overrides this BRAKE pin. See also BRKSEL.

BRKCAP. This pin is for connection of the reservoir capacitor used to provide the positive power supply for the sink drive outputs for a power-down condition. This allows predictable braking, if desired. Using a 4.7 µF capacitor will provide 6.5 V gate drive for 300 ms. If the power-down braking option is not needed (i.e., BRKSEL = 0), then this pin should be tied to VREG.

BRKSEL. Logic input to enable/disable braking upon power-down condition or RESET = 1. Internal 50 kΩ pull-up to LCAP. Setting BRKSEL to 0 enables Coast mode. Setting BRKSEL to 1 enables Brake mode.

PWM. Speed control input. Setting PWM to 1 turns on MOSFETs selected by Hall input logic. Setting PWM to 0 turns off the selected MOSFETs. Keep the PWM input held high to utilize internal current control circuitry. Internal 50 kΩ pull-up to LCAP.

RC. Analog input. Connection for R_T and C_T to set the fixed off-time. C_T also sets the BLANK time (see the section Application Information). It is recommended that the fixed off-time should not be less than 10 µs. The resistor should be in the range between 10 kΩ and 500 kΩ.

VREG. Regulated 13 V supply for the low-side gate drive and the bootstrap capacitor charge circuit. As a regulator, use a 10 µF decoupling/storage capacitor (ESR < 1 Ω) from this pin to AGND, as close to the device pins as possible.
Note: For 12 V applications, the VREG pin should be shorted to VBB.

VBB. Motor power supply connection for the A3938 and for power MOSFETs. It is good practice to connect a decoupling capacitor from this pin to AGND, as close to the device pins as possible.

REF. Analog input to current limit comparator. Voltage applied here sets the peak load current according to the following equation:

$$I_{TRIP} = V_{REF} / R_{SENSE}$$

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LCAP. 5 V reference to power internal logic and provide low current for DEAD pin and FAULT pin. Connection for 0.1 µF external capacitor for decoupling.

DEAD. Analog input. A resistor between DEAD and LCAP is selected to adjust turn-off time to turn-on time. This delay is needed to prevent cross-conduction in the external power MOSFETs. See the section Application Information for details on setting dead time.

SENSE. Analog input to the current limit comparator. Voltage representing load current appears on this pin. Voltage transients that are seen at this pin when the drivers turn on are ignored for period of time, t_{BLANK}.

AGND. Analog reference ground.

PGND. Return for low-side gate drivers. This should be connected to the PCB power ground.

Commutation Truth Table

H1	H2	H3	DIR	GLA	GLB	GLC	GHA	GHB	GHC	SA	SB	SC
1	0	1	1	0	0	1	1	0	0	HI	Z	LO
1	0	0	1	0	0	1	0	1	0	Z	HI	LO
1	1	0	1	1	0	0	0	1	0	LO	HI	Z
0	1	0	1	1	0	0	0	0	1	LO	Z	HI
0	1	1	1	0	1	0	0	0	1	Z	LO	HI
0	0	1	1	0	1	0	1	0	0	HI	LO	Z
1	0	1	0	1	0	0	0	0	1	LO	Z	HI
1	0	0	0	0	1	0	0	0	1	Z	LO	HI
1	1	0	0	0	1	0	1	0	0	HI	LO	Z
0	1	0	0	0	0	1	1	0	0	HI	Z	LO
0	1	1	0	0	0	1	0	1	0	Z	HI	LO
0	0	1	0	1	0	0	0	1	0	LO	HI	Z

Input Logic

MODE	PWM	RESET	Quadrant	Mode of Operation**
0*	0	0	Fast decay	PWM chop – current decay with opposite of selected low-side drivers ON.
0*	1	0	Fast Decay	Selected drivers ON. If current limiting, opposite of selected low-side drivers ON.
1	0	0	Slow decay	PWM chop – current decay with both low-side drivers ON.
1	1	0	Slow Decay	Selected drivers ON. If current limiting, both low-side drivers ON.
X	X	1	X	All high-side drivers OFF, low-sides see BRKSEL stored. Clears storable faults.

* Low-side, only, Synchronous Rectification mode.

**See Commutation Truth Table for meaning of “both” and "selected."

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APPLICATION INFORMATION

Synchronous Rectification. To reduce power consumption in the external MOSFETs, during the load current recirculation PWM-off cycle, the A3938 control logic turns on the appropriate low-side driver only. The reverse body diode of the power MOSFET conducts only during the dead time required at each PWM transition, as usual. However, unlike full synchronous rectification, the opposite high-side FET's body diode (not the R_{DSON}) will carry the re-circulating current, be self-extinguishing, and not force the motor to reverse direction.

Dead Time. To prevent cross-conduction, it is required to have a delay between a high-side or low-side turn-off, and the next turn-on event. The potential for cross-conduction occurs with synchronous rectification, direction changes, PWM, or after a bootstrap capacitor charging cycle. This dead-time is set via a resistor from the DEAD pin to LCAP and can be varied from 100 ns to 5.5 µs.

For a nominal case, given:

• 25°C ambient temperature, and

• 5.6 kΩ < R_{dead} < 470 kΩ,

$$t_{dead\ (nom,ns)} = 37 + [(11.9 \times 10^{-3}) \times (R_{dead} + 500)]$$

For predicting worst-case overvoltage and temperature extremes, use the following equations:

$$t_{dead\ (min,ns)} = 10 + [(6.55 \times 10^{-3}) \times (R_{dead} + 350)]$$

$$t_{dead\ (max,ns)} = 63 + [(17.2 \times 10^{-3}) \times (R_{dead} + 650)]$$

For nominal comparison with I_{dead} currents, also at 25°C ambient temperature:

$$I_{dead} = (V_{lcap} - V_{be}) / (R_{dead} + R_{int})$$

where V_{lcap} = 5 V, V_{be} = 0.7 V, and R_{int} = 500 Ω.

Rather than use R_{dead} values near 470 kΩ, set V_{dead} = 0 V, which activates an internal (I_{dead} = 10 µA) current source.

The choice of power MOSFET and external gate resistance determines the selection of the dead-time resistor. The dead time should be made long enough to cover the variation of the MOSFET capacitance and gate resistor tolerances (both external and internal to the A3938).

Decoupling. The internal reference VREG supplies current for the gate drive circuit. As the gates are driven high, they will require current from an external decoupling capacitor to support the transients. This capacitor should be placed as close as possible to the VREG pin. The value of the capacitor should be at least 20 times larger than the bootstrap capacitor. Additionally, a 1 nF (or larger) ceramic monolithic capacitor should be connected between LCAP and AGND, as close to the device pins as possible.

Protection Circuitry. The A3938 has several protection features:

• **Bootstrap Monitor**. The bootstrap capacitor is charged whenever a sink-side MOSFET is on, an Sx output goes low, or load current recirculates. This happens constantly during normal operation.

Note: The high side will not be allowed to turn on before the charging has decayed to less than approximately 9 mA.

• **Undervoltage**. VREG supplies the low-side gate driver and the bootstrap charge current. It is critical to ensure that the voltages are at a proper level before enabling any of the outputs. The undervoltage circuit is active during power-up and signals a fault, and also coasts or brakes (depending on the stored BRKSEL setting) the motor during that time period, until VREG is greater than approximately 10 V. On powering down, a fault is signaled and the motor is coasted or braked, depending on the stored setting for BRKSEL.

• **Hall Invalid**. Illegal codes for the Hall sensor inputs (0,0,0 or 1,1,1) force a fault and coast the motor. Noisy Hall lines may cause Hall code errors, and therefore faults. Additional external pull-up loading and filtering may be required in some systems.

Hint: Use dividers to the VREG terminal, than to the LCAP terminal, because the VREG terminal has more current capability.

• **Thermal Shutdown**. Junction temperatures greater than 165°C cause the A3938 to signal a fault and coast the motor.

• **Motor Lead**. The A3938 signals a fault if the motor lead is shorted to ground. A short-to-ground is assumed after a high-side is turned on and greater than 2 V is measured between the drain (VBB) and source (Sx) of the high-side power MOSFET. This fault is cleared at the beginning of each commutation. If a stalled motor results from a fault, the fault can only be cleared by toggling the RESET pin or by a power-up sequence.

Current Regulation. Load current can be regulated by an internal fixed off-time, PWM-control circuit. When the outputs of the MOSFETs are turned on, current increases in the motor winding until it reaches a value given by:

$$I_{TRIP} = V_{REF} / R_{SENSE}$$

At the trip point, the sense comparator resets the source enable latch, turning off the source driver. At this point, load

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inductance causes the current to recirculate for the fixed off-time period. The current path during recirculation is determined by the configuration of the MODE and SR input pins. The fixed off-time is determined by an external resistor, R_T, and capacitor, C_T, connected in parallel from the RC terminal to AGND. The fixed off-time is approximated by:

$$t_{OFF} = R_T \times C_T$$

t_{OFF} should be in the range between 10 µs and 50 µs. Larger values for t_{OFF} could result in audible noise problems. For proper circuit operation, 10 kΩ < R_T < 500 kΩ.

Torque control can be implemented by varying the REF input voltage as long as the PWM input stays high. If direct control of the torque/current is desired by PWM input, a voltage can be applied to the REF pin to set an absolute maximum current limit.

PWM Blank. The capacitor C_T also serves as the means to set the BLANK time duration. At the end of a PWM off-cycle, a high-side gate selected by the commutation logic turns on. At this time, large current transients can occur during the reverse recovery time, t_{rr}, of the intrinsic body diodes of the power MOSFETs. To prevent false tripping of the sense comparator, the BLANK function disables the comparator for a time period defined by:

$$t_{BLANK} = 1.9 \times C_T / (1 \times 10^{-3} - [2 / R_T])$$

The user must ensure that C_T is large enough to cover the current spike duration.

Braking. The A3938 dynamically brakes the motor by forcing all low-side power MOSFETs on, and all high-side power MOSFETs off. This effectively short-circuits the BEMF and brakes the motor. During braking, the load current can be approximated by:

$$I_{BRAKEPEAK} = V_{BEMF} / R_{LOAD}$$

As the current does not flow through the sense resistor during a dynamic brake, care should be taken to ensure that the maximum ratings of the power MOSFETs are not exceeded. Note: On its rising edge, a RESET setting of 1 overrides the BRAKE input pin and latches the condition selected by the BRKSEL pin.

Power Loss Brake. The BRKCAP and BRKSEL pins provide a power-down braking option. A Power-Loss Brake Trigger Event, which is either an undervoltage on VREG or a RESET = 1 rising edge, is sensed by the A3938, which then dynamically brakes or coasts (depending on the stored BRKSEL setting) the motor. The reservoir capacitor on the BRKCAP pin provides the positive voltage that forces the low-side gates of the power MOSFETs high, keeping them on, even after supply voltage is lost. A stored setting of BRKSEL = 1 brakes the motor, but a stored setting of BRKSEL = 0 coasts it. The combined effect of these settings is shown in the table Brake Control.

Brake Control

BRAKE	BRKSEL	Before Power Loss Brake Trigger Event	After Power Loss Brake Trigger Event
0	0	Normal run mode	Coast mode – All gate drive outputs OFF
0	1	Normal run mode	Brake mode – All low-side gate drivers ON
1	0	Brake mode – All low-side gate drivers ON	Coast mode – All gate drive outputs OFF
1	1	Brake mode – All low-side gate drivers ON	Brake mode – All low-side gate drivers ON

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Terminal List

Name	Description	Number
PGND	Low-Side Gate Drive Return	36
RESET	Control Input	1
GLC	Low-Side Gate Drive Output, Phase C	2
SC	Motor Connection, Phase C	3
GHC	High-Side Gate Drive Output, Phase C	6
CC	Bootstrap Capacitor, Phase C	7
GLB	Low-Side Gate Drive Output, Phase B	8
SB	Motor Connection, Phase B	9
GHB	High-Side Gate Drive Output, Phase B	10
CB	Bootstrap Capacitor, Phase B	11
GLA	Low-Side Gate Drive Output, Phase A	12
SA	Motor Connection, Phase A	13
GHA	High-Side Gate Drive Output, Phase A	14
CA	Bootstrap Capacitor, Phase A	15
VREG	Gate Drive Supply	16
LCAP	5 V Output	17
FAULT	Diagnostic Output	19
MODE	Control Input	20
VBB	Load Supply	21
H1	Hall Control Input	22
H3	Hall Control Input	24
H2	Hall Control Input	25
DIR	Control Input	26
BRAKE	Control Input	27
BRKCAP	Power Loss Brake Reservoir Capacitor	28
BRKSEL	Control Input	29
PWM	Control Input	30
RC	Connection for Fixed Off-Time R and C	31
SENSE	Sense Resistor	32
REF	Current Limit Adjust	33
DEAD	Dead Time Adjust	34
AGND	Ground	35
N/C	Not Connected	4, 5, 18, 23, 37, 38

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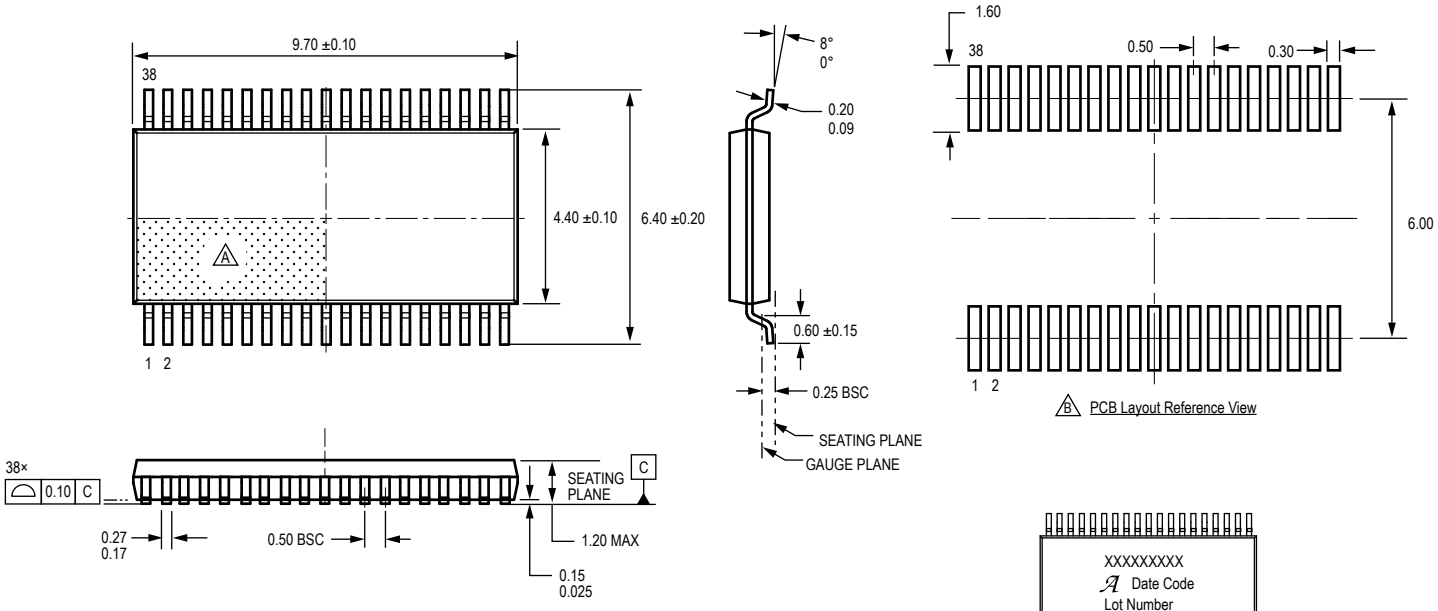
LD Package, 38-pin TSSOP

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000381, Rev. 1 and JEDEC MO-153 BD-1)
Dimensions in millimeters
NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Reference pad layout (reference IPC SOP50P640X110-38M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

C Standard Branding Reference

Lines 1, 2, 3 = Maximum 13 characters per line.

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

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Revision History

Number	Date	Description
1	April 10, 2019	Minor editorial updates
2	April 22, 2022	Updated package drawing (page 11) and minor editorial updates
3	May 25, 2023	Updated package branding (page 11)

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