THE DATASHEET OF

NCV7748D2R2G

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NCV7748

Automotive LIN Low-Side Relay Driver

The NCV7748 is an automotive eight channel low−side driver providing drive capability up to 0.75 A per channel. Output control is via a LIN bus with optimized LIN command set allowing high flexibility while still maintaining compliance to SAE J2602 LIN specification.

Each output driver includes an output clamp for inductive loads.

All output drivers have overcurrent detection implemented. Selected low side drivers (OUT4,8) offer additional reporting of faults for open load (or short to ground) and individual over temperature conditions which allows connection to a wiring harness outside of the module.

The NCV7748 is available in an SOIC14 package.

Features

OUTPUT DRIVERS

- Low−side Drivers, 8 Channels
  - OUT4 & OUT8 0.75 A, RDSon 0.8 Ω (typ), 1.6 Ω (max)
  - OUT1−3 & OUT5−7 0.6 A, RDSon 1.5 Ω (typ), 3.0 Ω (max)
- Low Quiescent Current in Sleep Mode
- Fault Reporting
- Global Over Temperature Detection and Shutdown
- Power−on Reset and Undervoltage Detection

LIN−Bus INTERFACE

- Integrated LIN Physical Layer Compliant to SAE J2602/LIN2.x
- Integrated State Machine for SAE J2602 Compliant LIN Protocol Handling and the LIN Message Decoding
- Virtual LIN Node Concept to Drive up to 32 Relays using One LIN Node Address with up to Four Slaves Devices
- Device Node Address (NAD) Selectable by External Resistor
- LIN Bus Short−circuit Protection to Supply and Ground
- Automatic Bit Rate Synchronization
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Power Distribution Box (PDB); Power Distribution Center (PDC)
- Body Junction Box (BJB); Engine Junction Box (EJB)
- Rear Junction Box (RJB); Body Electrical Center (BEC)
- Interior Electrical Center (IEC); Rear Electrical Center (REC)
- Underhood Electrical Center (UEC); Junction Box (JB)

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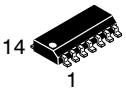
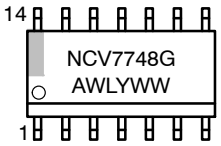


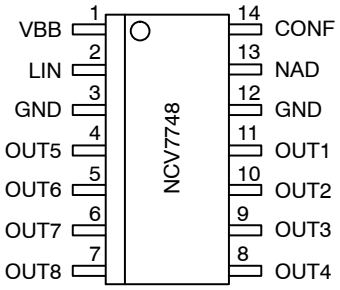
SOIC−14
D2 SUFFIX
CASE 751A

MARKING DIAGRAM



NCV7748 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

PIN CONNECTIONS



(Top Views)

ORDERING INFORMATION

See detailed ordering and shipping information on page 29 of this data sheet.

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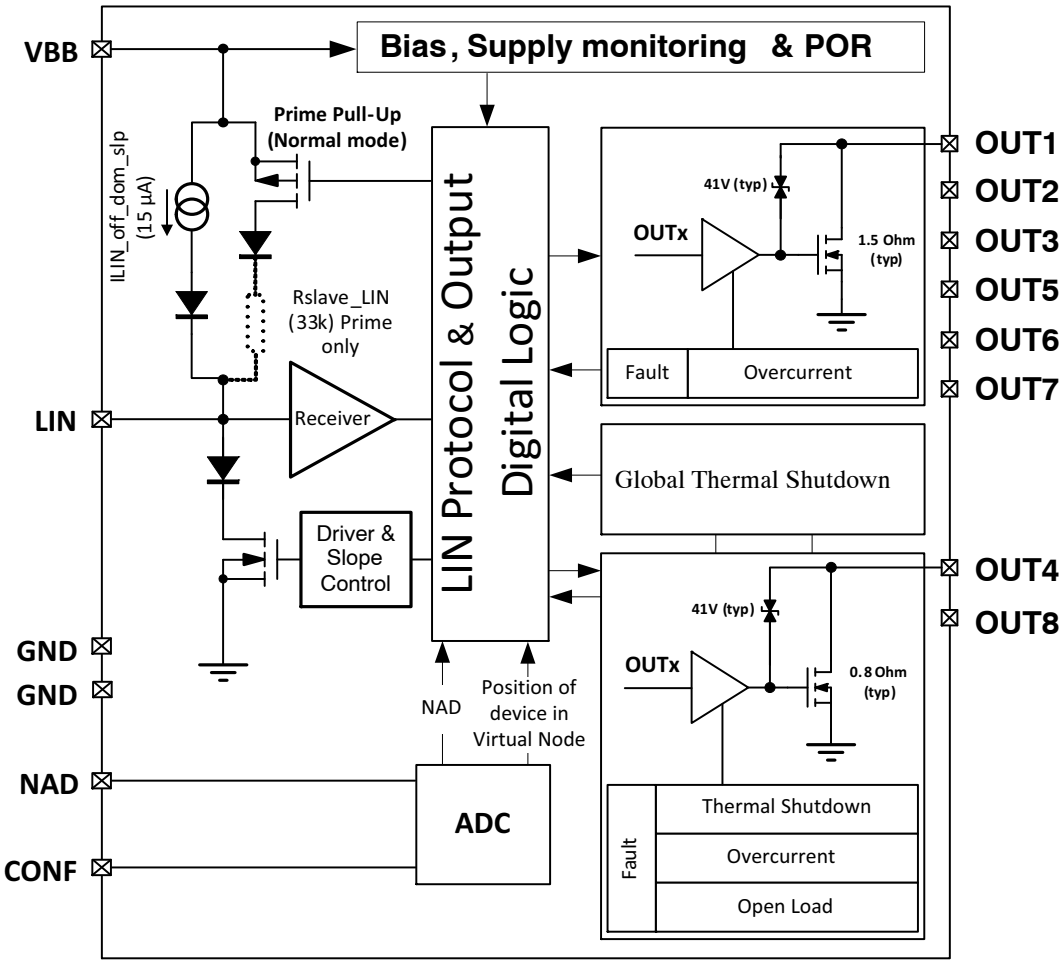


Figure 1. Block Diagram

Table 1. PIN FUNCTION DESCRIPTION, NCV7748

Pin No.	Pin Name	Pin Type	Description
1	VBB	Battery supply input	Battery connection
2	LIN	LIN bus interface	LIN bus pin, low in dominant state
3	GND (Note 1)	Ground	Ground connection
4	OUT5	LS driver	Channel 5 Low−side drive output, Ron = 1.5 Ω (typ)
5	OUT6	LS driver	Channel 6 Low−side drive output, Ron = 1.5 Ω (typ)
6	OUT7	LS driver	Channel 7 Low−side drive output, Ron = 1.5 Ω (typ)
7	OUT8	LS driver	Channel 8 Low−side drive output, Ron = 0.8 Ω (typ)
8	OUT4	LS driver	Channel 4 Low−side drive output, Ron = 0.8 Ω (typ)
9	OUT3	LS driver	Channel 3 Low−side drive output, Ron = 1.5 Ω (typ)
10	OUT2	LS driver	Channel 2 Low−side drive output, Ron = 1.5 Ω (typ)
11	OUT1	LS driver	Channel 1 Low−side drive output, Ron = 1.5 Ω (typ)
12	GND (Note 1)	Ground	Ground connection
13	NAD	LV analog input/output	Node Addressing via external resistor (NAD selection)
14	CONF	LV analog input/output	Defines virtual node configuration position via external resistor

NOTE: (LV = Low Voltage)

1. Pins 3 and 12 must be shorted externally.

Table 2. EXTERNAL COMPONENTS SPECIFICATION (See Figure 2)

Component	Function	Value	Unit	Tolerance
C_{VBB}	Decoupling capacitor on battery line, ceramic (X7R)	100	nF	20%
C_{Bulk}	Bulk capacitor (energy storage)	Depends on minimum battery voltage profile requirements		
R_{NAD}	Resistor for defining NAD of device	475 (Note 2)	Ω	1% (Note 5)
R_{CONF1}	Resistor for defining device's position in virtual node	10.0 (Note 3)	kΩ	1% (Note 5)
R_{CONF2}	Resistor for defining device's position in virtual node	1.00 (Note 4)	kΩ	1% (Note 5)
D1 − D2	Power supply diode for relays and NCV7748	e.g. MRA4003T3G		
D_{ESD}	Optional LIN ESD protection diode	e.g. NUP1105LT1G or MMBZ27x		

2. Node Address = 0x60
3. Position of device in the virtual node = A′
4. Position of device in the virtual node = B
5. This tolerance is required for every value of used resistors on NAD and CONF pins selected according to Table 6 and Table 7. The initial 1% tolerance of resistors must not get worse than 3% over the application life time.

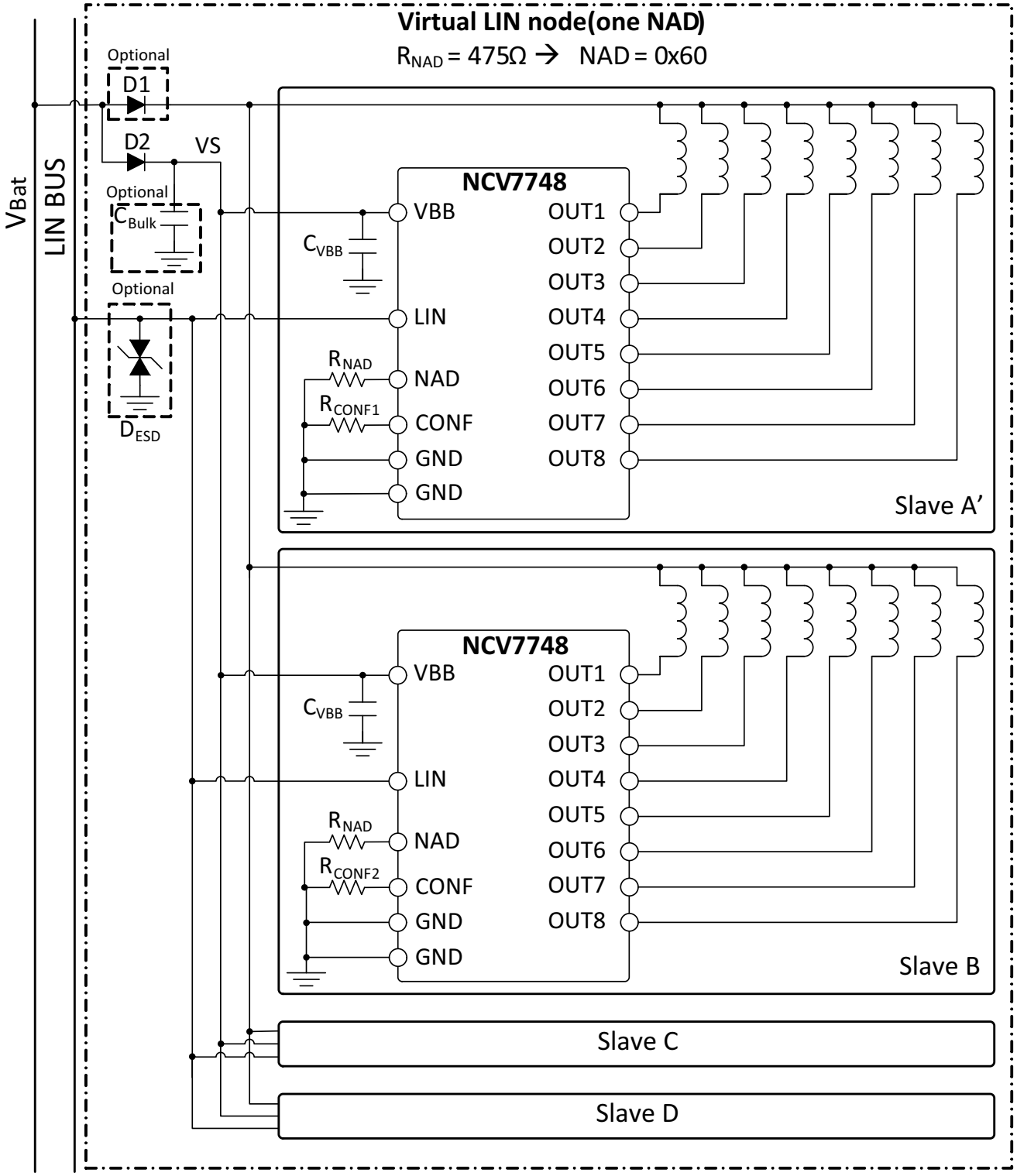


Figure 2. Application Diagram

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
Vmax_VBB	Power supply voltage	−0.3	+40	V
Vmax_LIN	DC voltage on LIN pin	−40	+40	V
Vmax_OUTx	OUT pins voltage range DC (voltage internally limited during flyback)	−0.3	38	V
Vmax_OUTx_peak	OUT pins peak voltage range Internally limited. Applies to VBB range from 0 V to Vmax_VBB (powered and unpowered modes)		45	V
Imax_OUT4,8	Maximum OUT4,8 pin current	−0.2	1.3	A
Imax_OUT1−3,5−7	Maximum OUT1−3, 5−7 pin current	−0.2	1.2	A
Clmp_sing Clmp_rep	Clamping energy Maximum (single pulse) OUT1−3, 5−7 (IOUT = 300 mA, T_A = 150°C) OUT4,8 (IOUT = 400 mA, T_A = 150°C) Repetitive (multiple) 2M pulses, VBB = 15 V, 63 Ω, 390 mH, T_A = 25°C	 − −	 40 65	mJ
Vmax_CONF	CONF pin DC maximum voltage	−0.3	3.6	V
Vmax_NAD	NAD pin DC maximum voltage	−0.3	3.6	V
RSC_level	AEC Q100−012 Short Circuit Reliability Characterization	Grade A (minimum of 1 million of cycles)		
ESD Human Body Model (100 pF, 1500 Ω)	All pins	−2	+2	kV
	Pin LIN to GND	−6	+6	
ESD following IEC 61000−4−2 (150 pF, 330 Ω)	Valid for pins VBB to GND and LIN to GND VBB pin with reverse−protection and filtering capacitor	−6	+6	kV
Tj_mr	Junction temperature	−40	+150	°C
Tstg	Storage Temperature Range	−55	+150	°C
MSL	Moisture Sensitivity Level (max. 260°C processing)	3		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
Rth_ja_1	Thermal Resistance, Junction−to−Ambient (1S0P) (Note 6)	88	°C/W
Rth_jc_1	Thermal Resistance, Junction−to−Case (1S0P) (Note 6)	30	
Rtj_jl_1	Thermal Resistance, Junction−to−Lead (1S0P) (Note 6)	61	
Rth_ja_2	Thermal Resistance, Junction−to−Ambient (2S2P) (Note 7)	62	
Rth_jc_2	Thermal Resistance, Junction−to−Case (2S2P) (Note 7)	30	
Rth_jl_2	Thermal Resistance, Junction−to−Lead (2S2P) (Note 7)	52	

6. Based on JESD51−3, 1.2 mm thick FR4, 1S0P PCB with 2 oz. copper to 645 mm^2 spreader. Thermal Information is based on dissipating 125 mW on OUT1−3, 5−7 low−side drivers and 625 mW on OUT4 & 8 low−de drivers.
7. Based on JESD51−7, 1.2 mm thick FR4, 2S2P PCB with 2 oz. copper. Thermal Information is based on dissipating 125 mW on all eight output drivers.

Table 5. ELECTRICAL CHARACTERISTICS 6 V ≤ V_{BB} ≤ 18 V, −40°C ≤ Tj ≤ 150°C; unless otherwise specified; $R_{L(LIN-VBB)}$ = 500 Ω, unless otherwise specified. Typical values are given at $V(V_{BB})$ = 12 V and T_J = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBB SUPPLY						
VBB	Supply Voltage	Functional (Note 8)	4	–	38	V
		Parameter specification	6	–	18	
VBB_PORH	VBB POR threshold	VBB rising	3.2	–	4	V
VBB_PORL	VBB POR threshold	VBB falling	3	–	3.7	V
VBB_UV_H	UV−threshold voltage high level	VBB rising (Note 8)	4	–	5	V
VBB_UV_L	UV−threshold voltage low level	VBB falling (Note 8)	3.8	–	4.7	V

8. Below 5 V on VBB in normal mode, the LIN bus will either stay recessive or comply with the voltage level specifications and transition time specifications as required by SAE J2602. It is ensured by the battery monitoring circuit (VBB_UV). Between VBB_UV and VBB_POR levels, OUTx pins status remains as commanded before undervoltage event. Above 18 V on VBB, LIN communication is operational (LIN pin toggling) but parameters are not guaranteed.

I_VBB_norm	VBB consumption in Normal mode	Normal mode, bus communication off, VLIN = VBB	–	–	5	mA
I_VBB_norm_c	VBB consumption in Normal mode, LIN active	Normal mode, bus communication on, VLIN = Low, No Load	–	–	10	mA
I_VBB_sleep	VBB consumption in Sleep mode	Sleep mode	–	–	50	μA
I_ VBB _sleep_i	VBB consumption in Sleep mode	VBB = 12.8V; VLIN = VBB ; Tj = 25°C Guaranteed by design and prototype evaluations, not tested in production	–	–	20	μA
OUT DRIVERS						
Ron_OUT1−3,5−7	On−resistance to ground OUT1−3 and OUT5−7	I(OUTx) = 90 mA	–	1.5	3	Ω
Ron_OUT4,8	On−resistance to ground OUT4 and OUT8	I(OUTx) = 340 mA	–	0.8	1.6	Ω
I_det_OUT4,8	Overcurrent Detection Current OUT4 and OUT8	OUTx = VBB	0.75	–	1.3	A
I_det_OUT1−3,5−7	Overcurrent Detection Current OUT1−3, OUT5−7	OUTx = VBB	0.6	–	1.2	A
Ileak_OUT1−8_r	Output leakage current in sleep mode (Note 9)	OUTx = VBB = 13.5 V, Tj = 25°C Guaranteed by design and prototype evaluations, not tested in production	–	–	1	μA
Ileak_OUT1−8	Output leakage current in sleep mode (Note 9)	OUTx = VBB = 13.5 V	–	–	5	μA
Vclmp_OUT1−3,5−7	Output clamp voltage	I(OUTx) = 90 mA	36	–	45	V
Vclmp_OUT4,8	Output clamp voltage	I(OUTx) = 340 mA	36	–	45	V
V_diode _OUT1−3,5−7	Output Body Diode Voltage	I(OUTx) = −90 mA	–	–	1.1	V
V_diode _OUT4,8	Output Body Diode Voltage	I(OUTx) = −340 mA	–	–	1.1	V
V_th_open	Open Load Detection Threshold Voltage (OUT4, OUT8)		1	–	2.5	V
I_th_open	Open Load Diagnostic Sink Current (OUT4, OUT8)	1 V < OUTx < 13.5 V, Normal mode, drivers commanded OFF	50	100	140	μA

9. In normal mode I_th_open load diagnostic current is flowing and does not allow a leakage current measurement.

MODE TRANSITIONS AND TIMEOUTS						
T_init	Sleep transition time after LIN wake−up detected (Duration of INIT mode)	See Figure 5	–	–	10	ms
T_go_to_sleep	Time to go to sleep	No communication on LIN and/or undervoltage	4	–	10	s
T_go_to_sleep_i	Time to go to sleep after LIN frame received	10.417 kbps or 19.2 kbps frame received	4	–	5	s

Table 5. ELECTRICAL CHARACTERISTICS 6 V ≤ V_{BB} ≤ 18 V, −40°C ≤ Tj ≤ 150°C; unless otherwise specified; $R_{L(LIN-VBB)}$ = 500 Ω, unless otherwise specified. Typical values are given at $V(V_{BB})$ = 12 V and T_J = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
MODE TRANSITIONS AND TIMEOUTS						
T_OC_del	Overcurrent Shut−Down Delay Time on OUTx pins	OUTx shorted to VBB	3	15	50	μs
T_OL_det	Open Load Detection Time OUT4, OUT8		30	115	200	μs
THERMAL PROTECTION						
T_{jsd}	Global Thermal shut−down level	Guaranteed by design and prototype evaluations, not tested in production	150	175	190	°C
$T_{jsd_hys_global}$	Thermal shut−down hysteresis	Guaranteed by design and prototype evaluations, not tested in production	–	20	–	°C
$T_{jsd_OUT4,8}$	Thermal shut−down level on OUT4 and OUT8	Guaranteed by design and prototype evaluations, not tested in production	150	175	190	°C
$T_{jsd_hys_O4,8}$	Thermal shut−down hysteresis	Guaranteed by design and prototype evaluations, not tested in production	–	20	–	°C
LIN TRANSMITTER DC CHARACTERISTICS						
VLin_dom_LoSup	LIN dominant output voltage	Bus driven dominant; VBB = 7.3 V	–	–	1.2	V
VLin_dom_HiSup	LIN dominant output voltage	Bus driven dominant; VBB = 18 V	–	–	2	V
VLin_rec	LIN recessive output voltage	Bus left recessive; I(LIN) = 0 mA	VBB − 1.5	–	VBB	V
ILIN_lim	Short circuit current limitation	V(LIN) = VBB = 18 V	40	–	200	mA
Rslave_LIN	Internal pull−up resistance	Activated on prime LIN node only (See functional description)	20	33	47	kΩ
LIN RECEIVER DC CHARACTERISTICS						
Vbus_dom_LIN	Bus voltage for dominant state		–	–	0.4 x VBB	V
Vbus_rec_LIN	Bus voltage for recessive state		0.6 x VBB	–	–	V
Vrec_dom_LIN	Receiver threshold	LIN bus recessive −> dominant	0.4 x VBB	–	0.5 x VBB	V
Vrec_rec_LIN	Receiver threshold	LIN bus dominant −> recessive	0.5 x VBB	–	0.6 x VBB	V
Vrec_cnt_LIN	Receiver center voltage	(Vrec_dom_LIN + Vrec_rec_LIN) / 2	0.475 x VBB	–	0.525 x VBB	V
Vrec_hys_LIN	Receiver hysteresis	(Vrec_rec_LIN − Vrec_dom_LIN)	0.05 x VBB	–	0.175 x VBB	V
ILIN_off_dom	LIN output current, bus in dominant state	Normal mode, driver off; VBB = 12 V; V(LIN) = 0 V	−1	–	–	mA
ILIN_off_dom_slp	LIN output current, bus in dominant state	Sleep mode, driver off; VBB = 12 V; V(LIN) = 0 V	−20	−15	−2	μA
ILIN_off_rec	LIN output current, bus in recessive state	Driver off; VBB = 12 V	–	–	2	μA
ILIN_no_GND	Communication not affected	VBB = GND = 12 V; 0 < V(LIN) < 18 V	−1	–	1	mA
ILIN_no_VBB	LIN bus remains operational	VBB = GND = 0 V; 0 < V(LIN) < 18 V	–	–	5	μA

Table 5. ELECTRICAL CHARACTERISTICS 6 V ≤ V_{BB} ≤ 18 V, −40°C ≤ Tj ≤ 150°C; unless otherwise specified; $R_{L(LIN-VBB)}$ = 500 Ω, unless otherwise specified. Typical values are given at $V(V_{BB})$ = 12 V and T_J = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LIN TRANSMITTER DYNAMIC CHARACTERISTICS (The following bus loads are considered: BL1 = 1 kΩ / 1 nF; BL2 = 660 Ω / 6.8 nF; BL3 = 500 Ω / 10 nF)(Resistor = Vbat to LIN, Capacitor = LIN to GND)						
D1	Duty Cycle 1 = $t_{BUS_rec(min)}$ / (2 x TBit) (see Figure 3)	$TH_{Rec(max)}$ = 0.744 x VBB, $TH_{Dom(max)}$ = 0.581 x VBB, Tbit = 50 μs, VBB = 7 V to 18 V, BL1, BL2, BL3	0.396		0.5	
D2	Duty Cycle 2 = $t_{BUS_rec(max)}$ / (2 x TBit) (see Figure 3)	$TH_{Rec(min)}$ = 0.422 x VBB, $TH_{Dom(min)}$ = 0.284 x VBB, Tbit = 50 μs, VBB = 7.6 V to 18 V, BL1, BL2, BL3	0.5		0.581	
D3	Duty Cycle 3 = $t_{BUS_rec(min)}$ / (2 x TBit) (see Figure 3)	$TH_{Rec(max)}$ = 0.788 x VBB, $TH_{Dom(max)}$ = 0.616 x VBB, Tbit = 96 μs, VBB = 7 V to 18 V BL1, BL2, BL3	0.417		0.5	
D4	Duty Cycle 4 = $t_{BUS_rec(max)}$ / (2 x TBit) (see Figure 3)	$TH_{Rec(min)}$ = 0.389 x VBB, $TH_{Dom(min)}$ = 0.251 x VBB, Tbit = 96 μs VBB = 7.6 V to 18 V, BL1, BL2, BL3	0.5		0.59	
T_fall_LIN	LIN falling edge (see Figure 4) BL1,BL2	VBB = 12 V; BL1, BL2 40% to 60% measurements extrapolated to 0% to 100%			22.5	μs
T_rise_LIN	LIN rising edge (see Figure 4) BL1,BL2	VBB = 12 V; BL1, BL2 40% to 60% measurements extrapolated to 0% to 100%			22.5	μs
T_sym_LIN	LIN slope symmetry BL1,BL2	Normal mode VBB = 12 V; BL1, BL2	−6	0	6	μs
T_fall_LIN_L3	LIN falling edge (see Figure 4) BL3	VBB = 12 V; BL3 40% to 60% measurements extrapolated to 0% to 100%			27	μs
T_rise_LIN_L3	LIN rising edge (see Figure 4) BL3	VBB = 12 V; BL3 40% to 60% measurements extrapolated to 0% to 100%			27	μs
T_sym_LIN_L3	LIN slope symmetry BL3	Normal mode; VBB = 12 V; BL3	−6	0	6	μs
C_LIN	Capacitance of the LIN pin	Guaranteed by design; not tested in production		20	30	pF
LIN RECEIVER DYNAMIC CHARACTERISTICS						
T_LIN_wake	Dominant duration for wakeup		30	90	150	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

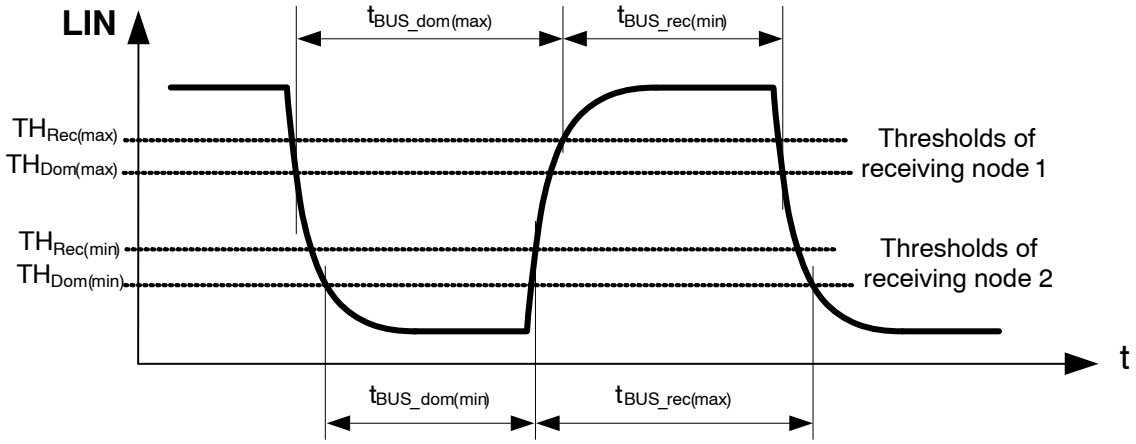


Figure 3. LIN Dynamic Characteristics – Duty Cycles

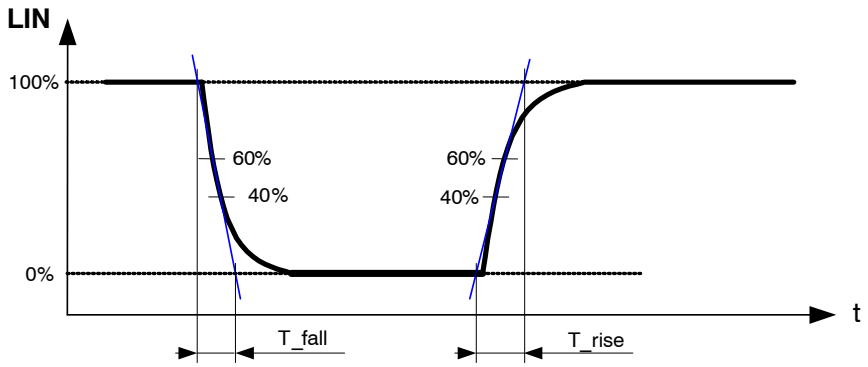


Figure 4. LIN Dynamic Characteristics – Transmitter Slope

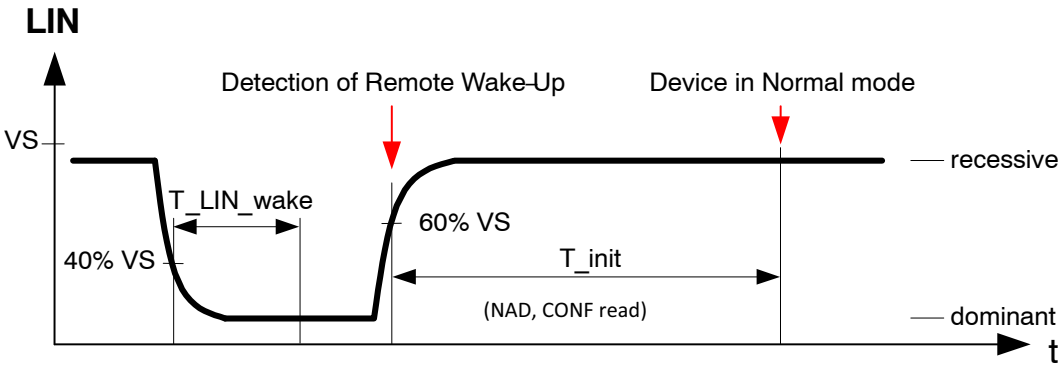


Figure 5. LIN Wake Up and Normal Mode Transition

Functional Description

The NCV7748 is an automotive eight channel low−side driver providing drive capability up to 0.75 A or 0.6 A per channel depending on channel selection. Output control is via a LIN bus with an optimized LIN command set allowing high flexibility while still maintaining compliance to the SAE J2602 LIN specification. Use of a virtual LIN node concept allows driving up to 32 channels with one LIN command.

Each output driver includes an output clamp for inductive loads.

All output drivers have overcurrent detection implemented. Select low side driver(s) offer additional fault reporting of open load (or short to ground) and local over temperature conditions which allows connection to a wiring harness outside of the module.

Operating Modes

The NCV7748 integrated circuit has **two BASIC modes** of operation:

1. **Normal mode** Fully functional.
2. **Sleep mode** Low quiescent current. Device is inactive waiting for LIN bus wake up.

The principal operating modes of the NCV7748 are shown in Figure 7.

There are also additional transition modes of operation: Un−powered, INIT, Reset and Undervoltage mode. Global thermal shutdown mode is shown in Figure 8. Within normal mode as shown in Figure 10, the device can transition into overcurrent mode (driver 1 to 3 and 5 to 7) or as shown in Figure 9 overcurrent/local thermal shutdown mode on drivers four and eight.

Un−Powered and INIT Mode

The device is held in power−on reset when VBB is below the *VBB_POR* level. All outputs are in HiZ state and LIN is disabled. Note: While LIN is disabled the weak pull up is activated (See ILIN_off_dom_slp parameter)

As soon as the VBB main supply exceeds the power−on reset level, the device enters the INIT Mode and begins an initialization sequence. ERR.0 bit is set high after the power−on reset. (See Table 15)

All the registers are set to their default values.

The device is reading the configuration resistors on the NAD and CONF pins. (Details of the device configuration based on NAD and CONF pins are in the Supported LIN commands chapter)

If the NAD and CONF pins are successfully read, the device enters normal mode. Otherwise (e.g. NAD, CONF pins shorted to ground, open or short between these pins) the device will enter Sleep mode. LIN is disabled during INIT mode and all OUTx outputs are in HiZ state.

The device stays in the INIT mode for a maximum time of *T_init*.

Sleep Mode

Sleep mode is entered from Normal mode or Undervoltage mode if there is no activity on the bus for longer time than limited by the *T_go_to_sleep* parameter. No activity is defined as no transition from recessive to dominant.

Another way to enter the Sleep mode from the Normal mode is successful reception of the Go to sleep command. (See Supported LIN commands chapter).

In Sleep Mode all outputs are off, the device is in Wake−up mode and there is no change in the state of the ERR bits.

If a valid LIN wake−up (See *T_LIN_wake*) is detected, the Sleep mode transitions to INIT mode.

Internal LIN Transceiver Modes

Within the NCV7748, the LIN transceiver has three internal modes of operation, normal active mode (On), Disabled mode (OFF), and within the NCV7748 sleep mode the LIN transceiver is powered down waiting to be woken up and is said to be in Wake−Up Mode.

LIN is active (On) during Normal Mode.

LIN is disabled (Off) during Un−Powered mode, Reset, and INIT mode.

In Sleep Mode, the internal LIN transceiver is in Wake−Up Mode waiting for a dominant signal (low) with a minimum continuous duration of T_LIN_wake. A remote wake−up occurs after T_LIN_wake and the return of LIN to a high (60% VS) (Figure 5).

When a LIN Wake−Up occurs, the device enters the INIT mode.

Reset Mode

After a successful reception of a broadcast or targeted reset frame, the device enters Reset mode.

All registers are set to their default values and ERR.0 bit is set to high.

Normal Mode

Normal mode is entered after a successful transition through the INIT mode.

The internal LIN transceiver is active and drivers are set as defined by LIN commands. (Details are in Supported LIN commands chapter.)

Open Load Detection

Open Load Detection is achieved for drivers OUT4 and OUT8 with the Open Load Detection Threshold Voltage reference voltage (*V_th_open*) and its corresponding Open Load Diagnostic Sink Current (*I_th_open*) (when the output driver [OUT4 or OUT8] is off) in both normal mode and after power up. The output driver maintains its functionality with and without the output status bit set (i.e. it can turn on and off).

During normal operation, the open circuit impedance (Roc) is zero ohms (Figure 6). This sets the voltage on OUT4 or OUT8 to VS volts. As long as VS is above V_th_open no open circuit fault will be recognized. The voltage appearing on OUT4 or OUT8 is a result of VS and the voltage drop across Roc realized by the current flow created by I_th_open.

The NCV7748 voltage level trip points are referenced to ground. The threshold range is between 1.0 V and 2.5 V.

With a nominal battery voltage (VS) of 14 V, the resultant worst case thresholds of detection are as follows.

$$\frac{(\text{VS} - \text{OpenLoadDetectionThresholdvoltage})}{\text{OpenLoadDiagnosticSinkCurrent}} = \text{OpenLoad Impedance}$$

$$\frac{(14\ \text{V} - 2.5\ \text{V})}{140\ \mu\text{A}} = 82.1\ \text{K}\Omega$$

$$\frac{(14\ \text{V} - 1.0\ \text{V})}{50\ \mu\text{A}} = 260\ \text{K}\Omega$$

The maximum impedance detection threshold is 260 KΩ, but may not be detected until the minimum impedance of 82.1 KΩ.

Note – Electrical parameter magnitudes in the Open Load Detection diagram are shown as typical values.

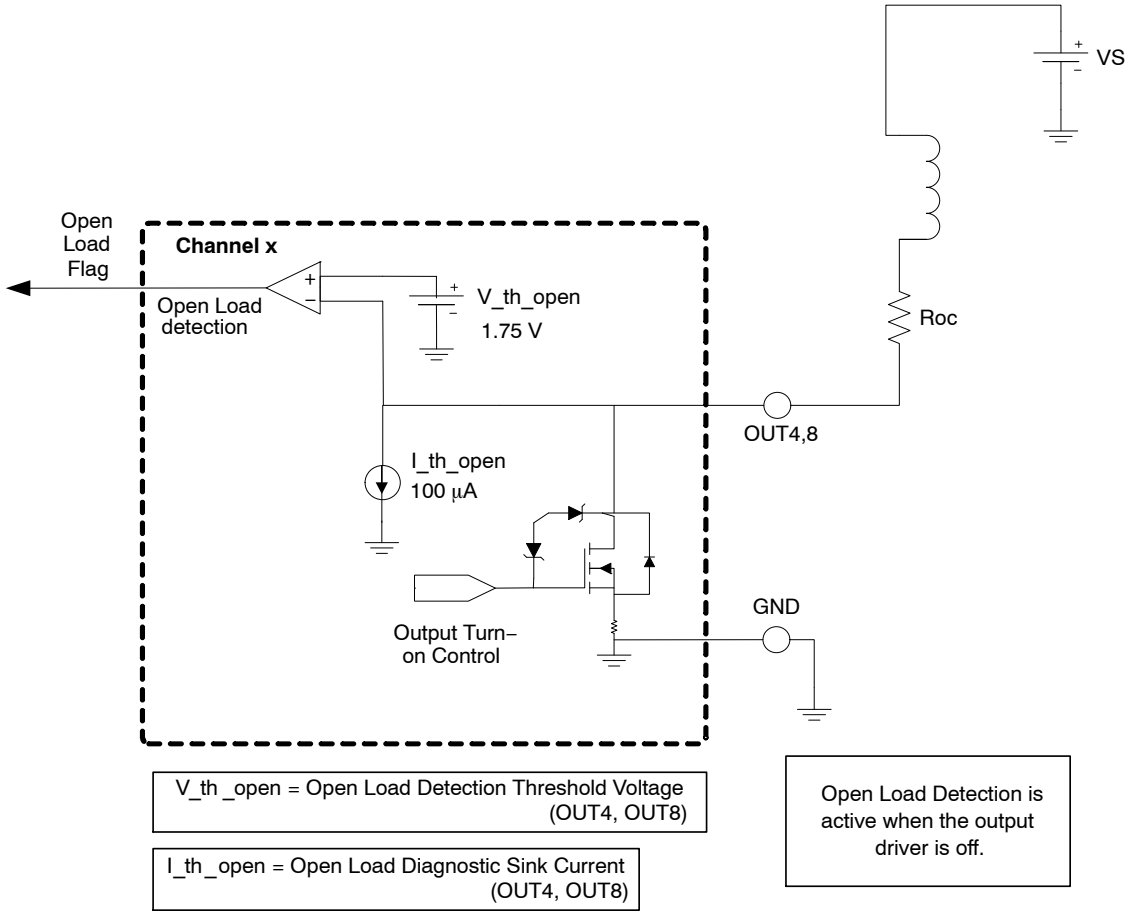


Figure 6. Open Load Detection

Dual Reporting APPINFO 01000b

Both **Local Thermal Shutdown** and **Overcurrent Detection** are reported in the APPINFO register (01000b) as an OR'd bit. Either or both of these conditions will be reported as a "1". (See Table 17)

Local Thermal Shutdown

Output 4 and 8 have local thermal shutdown sensors protecting the drivers. If OUT4/8 thermal shutdown threshold (*Tjsd_OUT4,8)* is reached, the corresponding driver is latched off and fault flags are set. The local thermal shutdown on OUT4 and OUT8 is latched in the OUT Status readout register (See Table 16) as well as in the APPINFO register. (See Table 17, APPINFO.3 bit).

The only way to leave the overcurrent / local thermal shutdown state and at the same time clear out the output status and APPINFO register is to command OFF the affected driver.

The overcurrent /local thermal shutdown info in the APPINFO register is only kept high if Global thermal shutdown is not activated. Global thermal shutdown has higher priority and masks APPINFO.3 to low as long as Global thermal shutdown is active. This is to avoid having both APPINFO.2 and APPINFO.3 bits high at the same time as this combination is reserved in some systems for ECU fault diagnostics.

Overcurrent Detection

All eight drivers have overcurrent detection implemented. Drivers are latched off if the load current exceeds *I_det_OUTx* level for the time longer than *T_OC_del* (see Figures 9 and 10).

The overcurrent status on OUT4 and OUT8 is latched in the OUT Status readout register (See Table 16) as well as in the APPINFO register. (See Table 17, APPINFO.3 bit). On OUT1−3 and OUT5−7 the overcurrent status is latched in the OUT status register but not in the APPINFO register.

The only way to leave the overcurrent / local thermal shutdown state and at the same time clear out the output status and APPINFO register is to command OFF the affected driver.

The overcurrent / local thermal shutdown info in the APPINFO register is only kept high if Global thermal shutdown is not activated. Global thermal shutdown has higher priority and masks APPINFO.3 to low as long as Global thermal shutdown is active. This is to avoid having both APPINFO.2 and APPINFO.3 bits high at the same time as this combination is reserved in some systems for ECU fault diagnostics.

Global Thermal Shutdown Mode

The device junction temperature is monitored in order to avoid permanent degradation or damage of the chip. Junction temperature exceeding the Shutdown level T_{J_SD} puts the chip into Thermal Shutdown mode. (See Figure 8)

In Global thermal Shutdown mode, all OUTx drivers are deactivated, LIN transceiver remains active. APPINFO.2 bit is set high and APPINFO.3 as mentioned above is masked to low (00100b). The mode is automatically exited if the junction cools down below the T_{J_SD} minus hysteresis $T_{jsd_hys_global}$ threshold. APPINFO.2 is not latched and is cleared when mode is exited.

Undervoltage Mode

If the voltage on the battery pin VBB goes below *VBB_UV_L,* the device enters Undervoltage mode. LIN is disabled (both transmitter and receiver) but drivers' status remains unchanged.

The device returns to Normal mode if the battery voltage goes above *VBB_UV_H* level. Un−powered mode is entered if VBB voltage drops below *VBB_POR_L* level.

As LIN timeout counter is running during the Undervoltage mode as well, the device is suspended to the Sleep mode when the timeout of *T_go_to_sleep* elapses.

Error Field (ERR [2:0]) & APPINFO (J2602 STATUS BYTE)

The NCV7748 uses a 3 bit error field (ERR[2:0]) as specified in SAE J2602 for LIN Protocol Error reporting and is reported in response to the GET STATUS COMMAND and the GET NODE ID COMMAND. Errors are reported and cleared in response to these commands in a serial prioritized sequence. The 8 Error states are reported from highest priority (7) to lowest priority (0) which is No Error. Each command clears just one error as they are reported until all errors are clear.

Error State Definitions

(See Table 15)

No Error – No detected fault.

Reset – VBB POR, Targeted reset (from normal mode), Broadcast reset (from normal mode)

Data Error – A TxD Bit Error shall be detected when the bit or byte value that is received is different from the bit or byte value that is transmitted.

Data Checksum – A Checksum Error shall be detected if the sum of all values and subtract 255 every time the sum is greater or equal to 256 over all received data bytes and the protected identifier (when using enhanced checksum) and the received checksum byte field does not result in $FF.

Byte Field Framing Error – The receiver shall detect a Byte Field Framing Error if the ninth bit after a valid start bit is dominant (low).

ID Parity Error – The receiver shall detect an ID Parity Error if the received ID parity (bits 6 & 7) does not match the ID parity calculated from P0 = ID0 ⊕ ID1 ⊕ ID2 ⊕ ID4 (1), P1 = ¬ (ID1 ⊕ ID3 ⊕ ID4 ⊕ ID5).

APPINFO [4:0]

The NCV7748 uses a 5 bit application specific field as specified in SAE J2602 for reporting the APPINFO register (reference Table 17) and is reported in response to the GET STATUS COMMAND and the GET NODE ID COMMAND. Global Thermal Shutdown is prioritized to report ahead of OUT4, OUT8 Thermal Shutdown or OUT4, OUT8 Overcurrent. All thermal shutdown and overcurrent faults must be cleared by commanding off the affected driver before they can be turned back on. Commanding off the affected driver will also clear APPINFO.

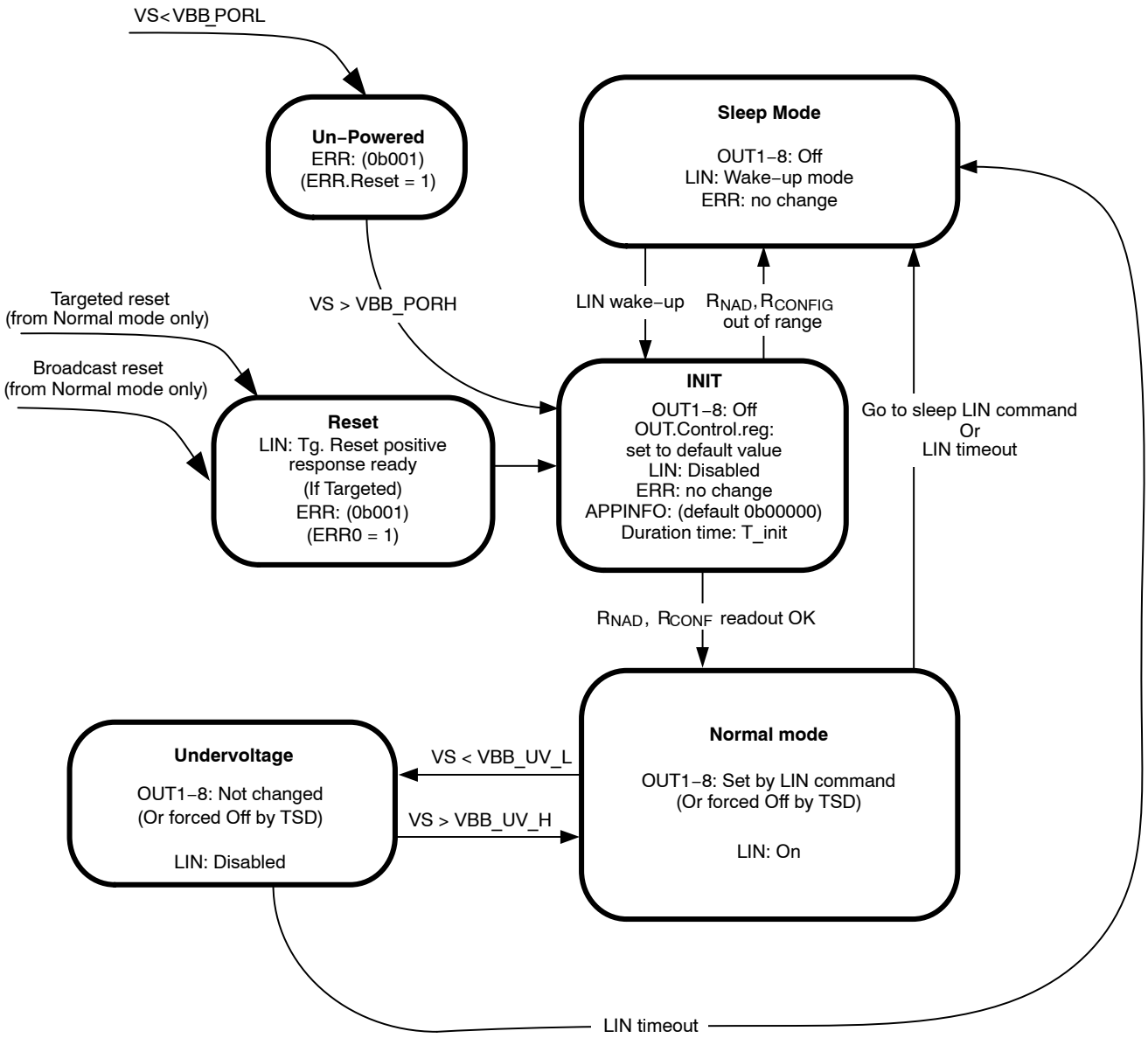


Figure 7. Basic State Diagram

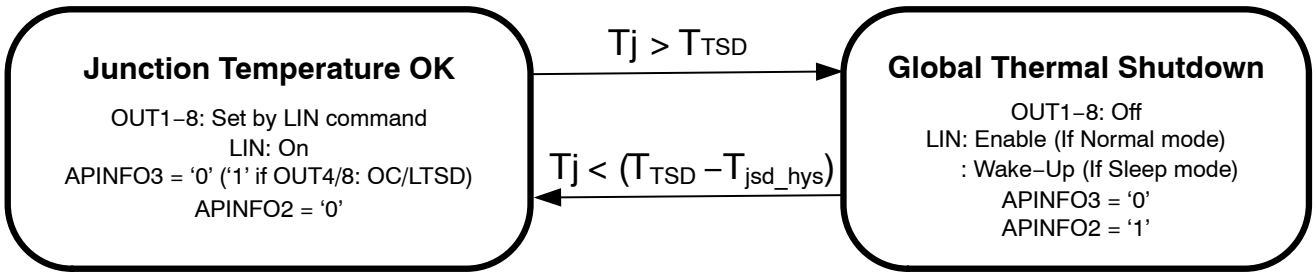


Figure 8. Global Thermal Shutdown State Diagram

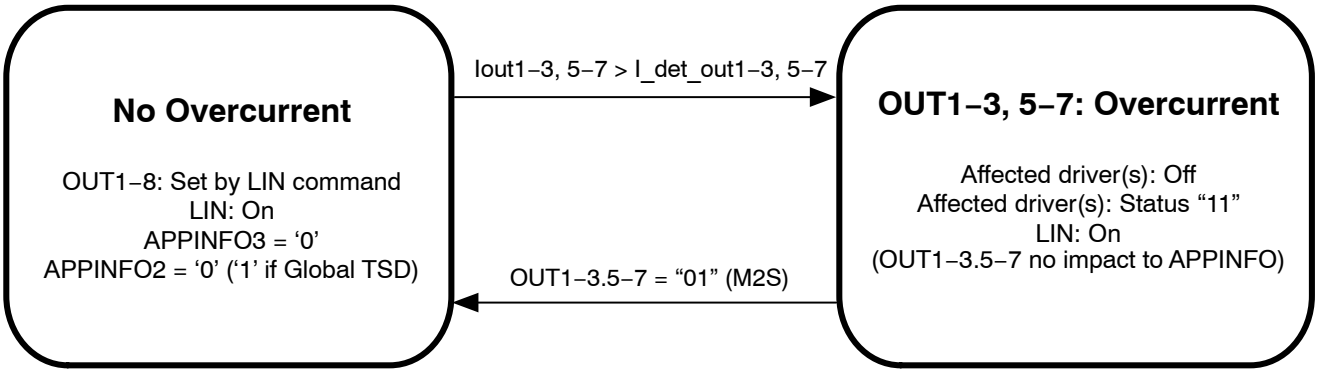


Figure 9. OUT1−3 and OUT5−7 Overcurrent Protection

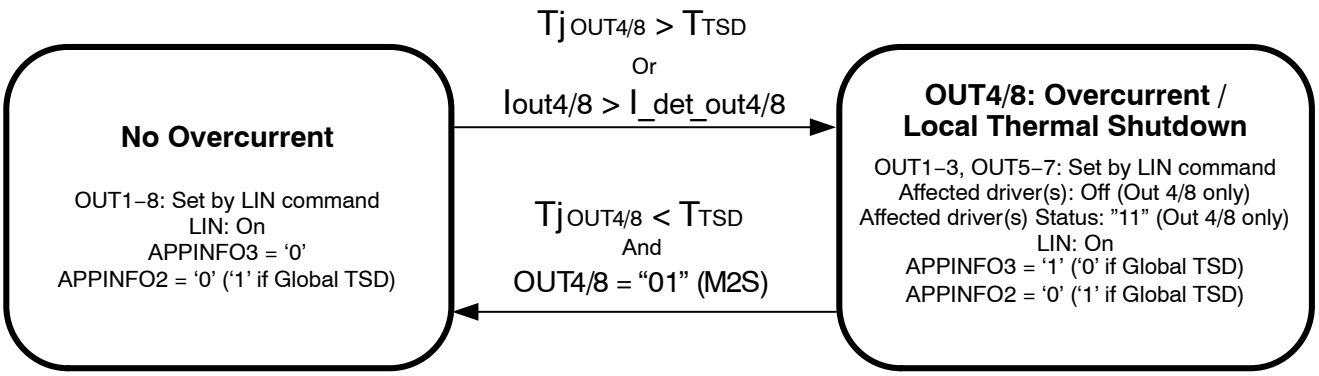


Figure 10. OUT4/8 Overcurrent/local Thermal Shutdown State Diagram

M2S = Master to Slave Output Turn−Off Command

LIN Physical Layer

NCV7748 integrates an on−chip LIN transceiver interface between the physical LIN bus and the integrated LIN protocol controller. (See Supported LIN Commands)

This LIN physical layer is compatible to LIN2.x and J2602 specifications.

The NCV7748 LIN2.2 compliant physical layer can be combined on the network with all the previous LIN physical layers.

The NCV7748 LIN transceiver consists of a transmitter, receiver and wakeup detector.

Automatic Bit Rate Detection

Automatic bit rate synchronization to any LIN master bit rate between 1 kbps and 20 kbps. Re−synchronization is done during the synchronization field of every LIN frame. When synchronized, the NCV7748 LIN Controller maintains bit time accuracy within ±2% of the incoming master bit time. Note: the parameter T_go_to_sleep_i in the MODE TRANSITIONS AND TIMEOUTS table is the only effected parameter for the two mentioned communication speeds.

Supported LIN Commands

A virtual LIN node concept was used to address the NCV7748. (See Figure 11). It allows

- Flexibility to drive up to 32 relays on one node via a LIN bus
- Compliance to SAE J2602 specification
- Provide enough free NAD addresses to other nodes on the LIN bus.

Virtual Slave Node Address

Virtual node means that up to four LIN relay driver chips will share the same NAD. That means up to four devices can be externally addressable as one LIN node.

The NAD of the virtual node is defined by the value of a resistor on the pin NAD according to the Table 6.

The external resistor value is compared to internal references and decoded during the INIT mode.

Table 6. VIRTUAL SLAVE NODE ADDRESS

NAD	0x60	0x62	0x64	0x66	0x68	0x6A	0x6C
R_{NAD}	475Ω	1.00kΩ	2.21kΩ	4.75kΩ	10.0kΩ	22.1kΩ	47.5kΩ

Virtual Slave Node Configuration

The position of the particular device within the virtual node is defined by the value of a resistor on the CONF pin (see Table 7) decoded during the INIT mode.

Table 7. DEVICE IDENTIFICATION WITHIN THE VIRTUAL LIN NODE

Slave	A	B	C	D	A′	B′	C′	D′
R_{CONF}	475Ω	1.00kΩ	2.21kΩ	4.75kΩ	10.0kΩ	22.1kΩ	47.5kΩ	100.0kΩ

Every virtual node must have exactly one prime node (marked with A′, B′, C′ or D′). The prime node will respond to the Targeted Reset and Get Node ID (of the virtual node). Non−prime nodes will not respond to these commands.

Only the prime node has an internal LIN pull−up resistor activated (see *Rslave_LIN* parameter in electrical characteristics section).

Table 9 shows an overview of all the supported LIN commands.

ID to PID Mapping

The relationship between protected identifier (PID) and message ID is explained in Table 8. The PID field consists of two sub−fields; the frame identifier and the parity. Bits 0 to 5 are the frame identifier and bits 6 and 7 (P0, P1) are the parity.

Table 8. ID TO PID MAPPING

PID							
Parity		ID					
P1	P0	5	4	3	2	1	0
1	0	0	0	0	0	0	0

P0 and P1 are used for parity check over <ID0> to <ID5>, (compliant to LIN2.x specification)

P0 = <ID0> ⊕ <ID1> ⊕ <ID2> ⊕ <ID4> (even parity) and P1 = NOT(<ID1> ⊕ <ID3> ⊕ <ID4> ⊕ <ID5>) (odd parity)

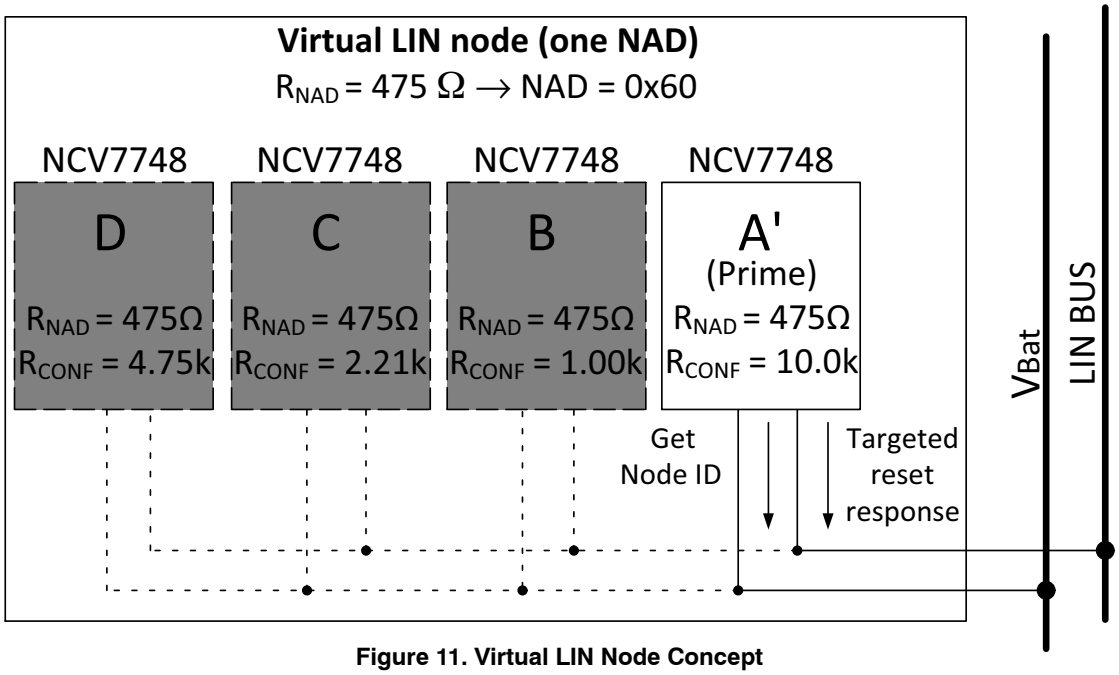


Figure 11. Virtual LIN Node Concept

Table 9. SUMMARY OF SUPPORTED LIN COMMANDS

Frame Type	Description	Data Length	PID[7:0]	Spec
Output Control	Sets all outputs in one virtual node	8	Depends on NAD (See Table 12)	N/A
Get Node ID	Reads identity of prime device in virtual node. (In frame slave Response)	8	Depends on NAD (See Table 23)	N/A
Get Status	Reads diagnostics of one device (LS driver). (In frame slave Response)	8	Depends on CONF (See Table 7) and NAD (See Table 18)	N/A
Targeted Reset master Request	Re−initialization of one virtual node. This includes all devices on the virtual node.	8	0x3C	J2602−1
Targeted Reset slave response	Positive response by prime device	8	0x7D	
Read by identifier master request	Reads identity of device supplier	8	0x3C	LIN2.2
Read by Identifier slave Response	Successfully processed request (Positive Response by prime)	8	0x7D	
	Slave could not process the request (Negative Response by prime)	8		
Broadcast Reset	Re−initialization of all nodes	8	0x3C	J2602−1
Goto Sleep	All devices enter Sleep Mode	8	0x3C	LIN2.2

OUTPUT CONTROL FRAME

Table 10. OUTPUT CONTROL COMMAND

	Byte	Content	Structure							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Master	0	Identifier	PID							
	1	Data 1	OUT4_A/A'		OUT3_A/A'		OUT2_A/A'		OUT1_A/A'	
	2	Data 2	OUT8_A/A'		OUT7_A/A'		OUT6_A/A'		OUT5_A/A'	
	3	Data 3	OUT4_B/B'		OUT3_B/B'		OUT2_B/B'		OUT1_B/B'	
	4	Data 4	OUT8_B/B'		OUT7_B/B'		OUT6_B/B'		OUT5_B/B'	
	5	Data 5	OUT4_C/C'		OUT3_C/C'		OUT2_C/C'		OUT1_C/C'	
	6	Data 6	OUT8_C/C'		OUT7_C/C'		OUT6_C/C'		OUT5_C/C'	
	7	Data 7	OUT4_D/D'		OUT3_D/D'		OUT2_D/D'		OUT1_D/D'	
	8	Data 8	OUT8_D/D'		OUT7_D/D'		OUT6_D/D'		OUT5_D/D'	
	9	Checksum	Enhanced Checksum							

The output Control command is used to control all the connected drivers in the virtual node. Each data byte controls up to four channels where each two bits are assigned to one output channel. (See Table 10) The decoding of the 2−bit output control is shown in the Table 11.

Table 11. OUTPUT ENCODING

OUTx_A[1]	OUTx_A[0]	Output
0	0	No change
0	1	OUTx Off*
1	0	OUTx On
1	1	No change

*Outputs OUT4 and OUT8 have open load diagnostics, which are enabled when the output is off.

The ID of the control frame depends on the chosen NAD of the virtual LIN node. The mapping of the ID to be used based on NAD is shown in Table 12.

Table 12. NAD TO OUTPUT CONTROL COMMAND ID/PID MAPPING

R_{NAD}	NAD	ID	PID
475 Ω	0x60	0x01	0xC1
1.00 kΩ	0x62	0x09	0x49
2.21 kΩ	0x64	0x11	0x11
4.75 kΩ	0x66	0x19	0x99
10.0 kΩ	0x68	0x21	0x61
22.1 kΩ	0x6A	0x29	0xE9
47.5 kΩ	0x6C	0x31	0xB1

Table 13 shows NAD to ID mapping in the context of SAEJ2602 spec.

Table 13. OUTPUT CONTROL COMMAND NAD TO ID MAPPING LINKED TO SAEJ2602 SPEC

NAD	Message ID	PID	NAD	Message ID	PID	NAD	Message ID	PID	NAD	Message ID	PID
$60	$0		$64	$10		$68	$20		$6C	$30	
	$1	0xC1		$11	0x11		$21	0x61		$31	0xB1
	$2			$12			$22			$32	
	$3			$13			$23			$33	
	$4			$14			$24			$34	
	$5			$15			$25			$35	
	$6			$16			$26			$36	
	$7			$17			$27			$37	
$62	$8		$66	$18		$6A	$28		$6E	No Message IDs defined	
	$9	0x49		$19	0x99		$29	0xE9			
	$0A			$1A			$2A				
	$0B			$1B			$2B				
	$0C			$1C			$2C		$6F	No Message IDs defined	
	$0D			$1D			$2D				
	$0E			$1E			$2E				
	$0F			$1F			$2F				

GET STATUS AND DIAGNOSTIC

Table 14. GET STATUS REQUEST

	Byte	Content	Structure							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Master	0	Identifier	PID							
Slave	1	Data 1	ERR2	ERR1	ERR0	APPINFO				
	2	Data 2	OUT4 STATUS		OUT3 STATUS		OUT2 STATUS		OUT1 STATUS	
	3	Data 3	OUT8 STATUS		OUT7 STATUS		OUT6 STATUS		OUT5 STATUS	
	4	Data 4	0x00 (NULL)							
	5	Data 5	0x00 (NULL)							
	6	Data 6	0x00 (NULL)							
	7	Data 7	0x00 (NULL)							
	8	Data 8	0x00 (NULL)							
	9	Checksum	Enhanced Checksum							

GET STATUS COMMAND

The Get Status Request frame (see Table 14) is issued by the master to receive application specific diagnostics.

The error bits decrypted from Data1 of this command are as per SAEJ2602 in Table 15.

The ERR.[2:0] bits are cleared by readout. That means every command response containing ERR.[2:0] clears the error register.

Every driver status (Data 2 and 3) is stored in two bits of information. Only drivers OUT4 and OUT8 allow readout of open load fault (OL) and local TSD. All drivers flag overcurrent info. (See Table 16)

Table 17 describes APPINFO register content.

Table 15. J2602−1 ERROR FIELD

ERR2	ERR1	ERR0	Error States	Priority
0	0	0	No Error	0 (lowest)
0	0	1	Reset	1
0	1	0	Reserved	2
0	1	1	Reserved	3
1	0	0	Data Error	4
1	0	1	Data Checksum	5
1	1	0	Byte Field Framing Error	6
1	1	1	ID Parity Error	7 (highest)

Table 16. OUT STATUS READOUT

STATUS	Output Command	Description	Note
00b	OFF	Open Load Fault (non−latching)	Only OUT4/8
01b	OFF	Per setting or active Global TSD	All OUTx, Default after reset
10b	ON	Per setting	All OUTx
11b	ON	Latched OFF from ON state due to TSD/OC	TSD / OUT4/8; OC on all OUTx

Table 17. APPINFO REGISTER

APPINFO	Error States
00000b	Default − No Failure to Report
00100b	Global Thermal Shutdown
01000b	OUT4 & OUT8 Thermal Shutdown or Overcurrent
1XXXXb	Not Supported (Slave is not requiring configuration / calibration)
X11XXb	Not Supported (No ECU fault reporting)
XXX1Xb	Not Supported (No input fault reporting)
XXXX1b	Not Supported
NOTE: “X” = don’t care	

Table 18 defines the PID depending on NAD and CONF.

Table 18. GET STATUS ID MAPPING

		ID	PID	ID	PID	ID	PID	ID	PID
	Slave	A		B		C		D	
		A′		B′		C′		D′	
R_{NAD}	**NAD**								
475 Ω	0x60	0x02	0x42	0x03	0x03	0x04	0xC4	0x05	0x85
1.00 kΩ	0x62	0x0A	0xCA	0x0B	0x8B	0x0C	0x4C	0x0D	0x0D
2.21 kΩ	0x64	0x12	0x92	0x13	0xD3	0x14	0x14	0x15	0x55
4.75 kΩ	0x66	0x1A	0x1A	0x1B	0x5B	0x1C	0x9C	0x1D	0xDD
10.0 kΩ	0x68	0x22	0xE2	0x23	0xA3	0x24	0x64	0x25	0x25
22.1 kΩ	0x6A	0x2A	0x6A	0x2B	0x2B	0x2C	0xEC	0x2D	0xAD
47.5 kΩ	0x6C	0x32	0x32	0x33	0x73	0x34	0xB4	0x35	0xF5

Table 19 shows get status ID to NAD and node position within a virtual node in context of SAEJ2602 spec.

Table 19. GET STATUS ID MAPPING LINKED TO SAEJ2602 SPEC

NAD	Message ID	PID	NAD	Message ID	PID	NAD	Message ID	PID	NAD	Message ID	PID
$60	$0		$64	$10		$68	$20		$6C	$30	
	$1			$11			$21			$31	
	$2	0x42		$12	0x92		$22	0xE2		$32	0x32
	$3	0x03		$13	0xD3		$23	0xA3		$33	0x73
	$4	0xC4		$14	0x14		$24	0x64		$34	0xB4
	$5	0x85		$15	0x55		$25	0x25		$35	0xF5
	$6			$16			$26			$36	
	$7			$17			$27			$37	
$62	$8		$66	$18		$6A	$28		$6E	No Message IDs defined	
	$9	0xCA		$19			$29				
	$0A	0x8B		$1A	0x1A		$2A	0x6A			
	$0B	0x4C		$1B	0x5B		$2B	0x2B			
	$0C	0x0D		$1C	0x9C		$2C	0xEC	$6F	No Message IDs defined	
	$0D			$1D	0xDD		$2D	0xAD			
	$0E			$1E			$2E				
	$0F			$1F			$2F				

Example of the Get Status command

Reference Figure 12 for bit sequencing.

```
ID = 0x02 [Table ID] => PID = 0x42 [LIN2.2]
(Reference Table 19)

Data1 = 0x08 => OUT4,OUT8 TSD / OC
(0b 000 01000)

Data2 = 0x59 =>  OUT1 : Off (01)
(0b 01 01 10 01) OUT2 : ON  (10)
                 OUT3 : Off (01)
                 OUT4 : Off (01)

Data3 = 0xDA =>  OUT5 : ON  (10)
(0b 11 01 10 10) OUT6 : ON  (10)
                 OUT7 : Off (01)
                 OUT8 : Off (11)Latched Off due to TSD/OC
```

Note the placement of the bits for LSB and MSB!
It is not intuitive. LSB is sent first.

Table 20. GET STATUS EXAMPLE HEX RESPONSE

Status	Hex Response		OUT Number				
			1	2	3	4	
OUT1−4	0x59	LSB	10	01	10	10	MSB
OUT5−8	0xDA	LSB	01	01	10	11	MSB

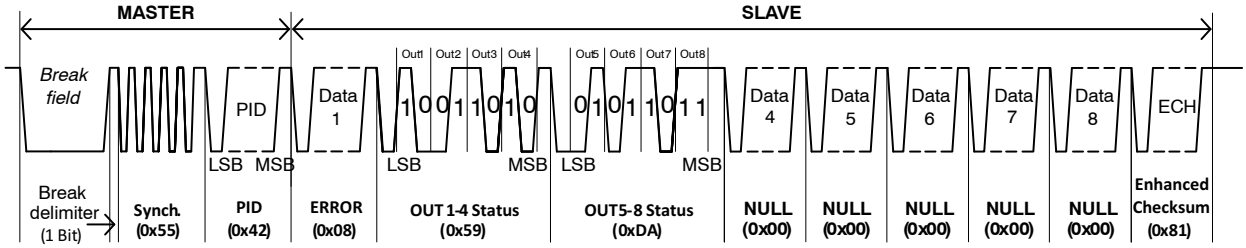


Figure 12. Example of Waveform of Get Status Command

GET NODE ID COMMAND

Table 21. GET NODE ID

	Byte	Content	Structure							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Master	0	Identifier	PID							
Slave	1	Data 1	ERR2	ERR1	ERR0	APPINFO				
	2	Data 2	Index Byte (0x00)							
	3	Data 3	Supplier ID, MSB (0x00)							
	4	Data 4	Supplier ID, LSB (0x24)							
	5	Data 5	Function ID, MSB (0x60)							
	6	Data 6	Function ID, LSB (0x48/0x44)							
	7	Data 7	Silicon Version							
	8	Data 8	0x00 (null)							
	9	Checksum	Enhanced Checksum							

The Get Node ID Request frame (see Table 21) is issued by the master to receive Supplier ID and Function ID information. (Only prime node responds)

Data 1 is the same as in the Get status command. The mapping of the ID to be used based on NAD is shown in Table 23.

The Index byte is fixed to zero as the NCV7748 sends out only six bytes of part number data.

The Supplier ID for ON Semiconductor (Data3, 4) is 0x0024.

Table 22 shows the function ID assignment for the NCV7748.

Table 22. FUNCTION ID ASSIGNMENT

	Function ID, MSB		Function ID, LSB	
	Group	Sub−group	Part Number	
NCV7748	6	0	4	8

Table 23. GET NODE ID / PID MAPPING

R_{NAD}	NAD	ID	PID
475 Ω	0x60	0x00	0x80
1.00 kΩ	0x62	0x08	0x08
2.21 kΩ	0x64	0x10	0x50
4.75 kΩ	0x66	0x18	0xD8
10.0 kΩ	0x68	0x20	0x20
22.1 kΩ	0x6A	0x28	0xA8
47.5 kΩ	0x6C	0x30	0xF0

Table 24 shows get status ID to NAD and node position within virtual node in context of the SAEJ2602 spec.

Table 24. GET NODE ID COMMAND MAPPING LINKED TO SAEJ2602 SPEC

NAD	Message ID	PID	NAD	Message ID	PID	NAD	Message ID	PID	NAD	Message ID	PID
$60	$0	0x80	$64	$10	0x50	$68	$20	0x20	$6C	$30	0xF0
	$1			$11			$21			$31	
	$2			$12			$22			$32	
	$3			$13			$23			$33	
	$4			$14			$24			$34	
	$5			$15			$25			$35	
	$6			$16			$26			$36	
	$7			$17			$27			$37	
$62	$8	0x08	$66	$18	0xD8	$6A	$28	0xA8	$6E	No Message IDs defined	
	$9			$19			$29				
	$0A			$1A			$2A				
	$0B			$1B			$2B				
	$0C			$1C			$2C		$6F	No Message IDs defined	
	$0D			$1D			$2D				
	$0E			$1E			$2E				
	$0F			$1F			$2F				

READ BY IDENTIFIER COMMAND

Table 25. READ BY IDENTIFIER

	Byte	Content	Structure							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Master	0	Identifier	0x00 (Parity)		0x3C (ID)					
	1	Data 1	NAD or 0x7F (Wildcard NAD)							
	2	Data 2	0x06 (PCI)							
	3	Data 3	0xB2 (SID)							
	4	Data 4	Node Identifier (see Node Identification Table 28)							
	5	Data 5	Supplier ID LSB (0x24) or 0xFF (Wildcard Supplier ID)							
	6	Data 6	Supplier ID MSB (0x00) or 0x7F (Wildcard Supplier ID)							
	7	Data 7	Function ID LSB (0x48/0x44) or 0xFF (Wildcard Function ID)							
	8	Data 8	Function ID MSB (0x60) or 0xFF (Wildcard Function ID)							
	9	Checksum	Classic Checksum							

Table 26. POSITIVE RESPONSE FOR READ BY IDENTIFIER

	Byte	Content	Structure							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Master	0	Identifier	0x01 (Parity)		0x3D (ID)					
Slave	1	Data 1	NAD							
	2	Data 2	0x06 (PCI)							
	3	Data 3	0xF2 (RSID)							
	4	Data 4	Supplier ID LSB (0x24)							
	5	Data 5	Supplier ID MSB (0x00)							
	6	Data 6	Function ID LSB (0x48/0x44)							
	7	Data 7	Function ID MSB (0x60)							
	8	Data 8	Silicon Version							
	9	Checksum	Classic Checksum							

Table 27. NEGATIVE RESPONSE FOR READ BY IDENTIFIER

	Byte	Content	Structure							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Master	0	Identifier	0x01 (Parity)		0x3D (ID)					
Slave	1	Data 1	NAD							
	2	Data 2	0x03 (PCI)							
	3	Data 3	0x7F (RSID)							
	4	Data 4	0xB2 (Requested SID)							
	5	Data 5	0x12 (Error Code)							
	6	Data 6	0xFF							
	7	Data 7	0xFF							
	8	Data 8	0xFF							
	9	Checksum	Classic Checksum							

The Read by Identifier Request frame (see Table 25) is issued by the master to receive application specific diagnostics.

Data1 (NAD selection) is explained previously (See Table 6 and Table 7). Data 4 (Node identifier) determines which of the nodes in the virtual LIN node should respond. (See Table 28). The identification of nodes within the virtual node is defined in Table 7.

If the Node identifier is in accordance with Table 28, the addressed slave answers by the Positive response (see Table 26). If the Identifier is out of range in Table 28 (not equal to 0x00, 0x20, 0x21, 0x22 or 0x23), the prime slave answers with the Negative response (see Table 27). A prime device can be addressed by either the 0x00 (′) identifier or the identifier associated with its letter designator (A, B, C, D).

An example of Read by Identifier request / response is shown below.

Table 28. NODE IDENTIFICATION

Identifier	Responding Slave
0x00	Prime (Marked with ′)
0x20	A
0x21	B
0x22	C
0x23	D

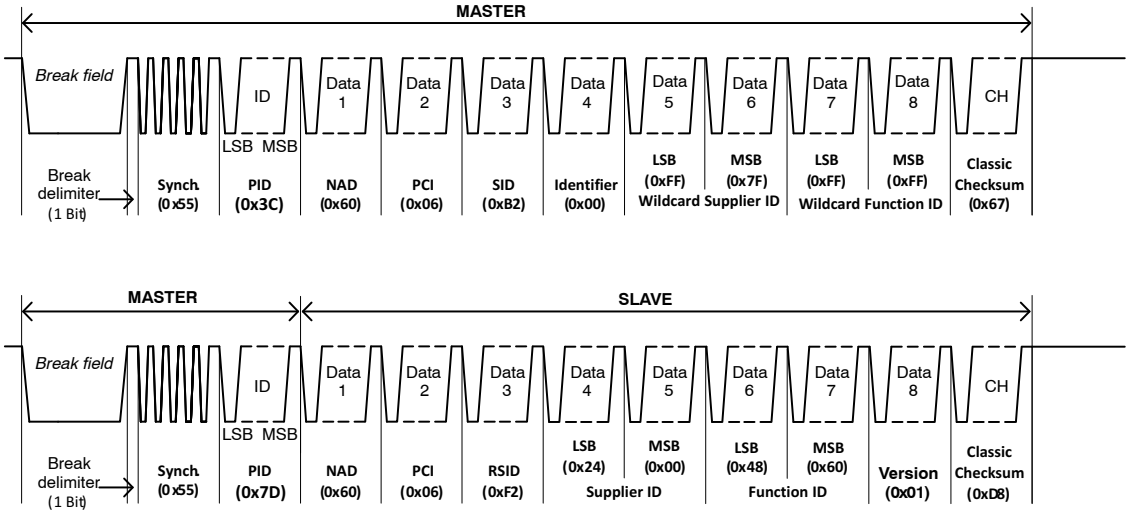


Figure 13. Example of Read by Identifier, NAD = 0x60, Prime Slave Addressed and Positive Responding

BROADCAST RESET COMMAND

Table 29. BROADCAST RESET FRAME

	Byte	Content	Structure							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Master	0	Identifier	0x00 (Parity)		0x3C (ID)					
	1	Data 1	0x7F							
	2	Data 2	0x01							
	3	Data 3	0xB5							
	4	Data 4	0xFF							
	5	Data 5	0xFF							
	6	Data 6	0xFF							
	7	Data 7	0xFF							
	8	Data 8	0xFF							
	9	Checksum	Classic Checksum							

Table 29 describes the command to reset all nodes. No slave response.

TARGETED RESET COMMAND

Table 30. TARGETED RESET REQUEST COMMAND

			Structure							
	Byte	Content	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Master	0	Identifier	0x00 (Parity)		0x3C (ID)					
	1	Data 1	NAD							
	2	Data 2	0x01							
	3	Data 3	0xB5							
	4	Data 4	0xFF							
	5	Data 5	0xFF							
	6	Data 6	0xFF							
	7	Data 7	0xFF							
	8	Data 8	0xFF							
	9	Checksum	Classic Checksum							

Table 31. TARGETED RESET POSITIVE RESPONSE

			Structure							
	Byte	Content	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Master	0	Identifier	0x01 (Parity)		0x3D (ID)					
Slave	1	Data 1	NAD							
	2	Data 2	0x06							
	3	Data 3	0xF5							
	4	Data 4	Supplier ID LSB (0x24)							
	5	Data 5	Supplier ID MSB (0x00)							
	6	Data 6	Function ID LSB (0x48/0x44)							
	7	Data 7	Function ID MSB (0x60)							
	8	Data 8	Silicon Version							
	9	Checksum	Classic Checksum							

Targeted reset (See Table 30) puts all the outputs into the off state (Table 11, OUTx Off), resets the error flags ERR.1,2 and sets the ERR.0 =1 in the ERR status byte (Table 15).

Targeted reset puts all outputs for all devices in a virtual node in the off state.

The node giving positive response (prime node) within the virtual node is defined by Table 31.

GO TO SLEEP COMMAND

Table 32. GO TO SLEEP COMMAND

			Structure							
	Byte	Content	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Master	0	Identifier	0x00 (Parity)		0x3C (ID)					
	1	Data 1	0x00							
	2	Data 2	0xXX							
	3	Data 3	0xXX							
	4	Data 4	0xXX							
	5	Data 5	0xXX							
	6	Data 6	0xXX							
	7	Data 7	0xXX							
	8	Data 8	0xXX							
	9	Checksum	Classic Checksum							

The Go to sleep command (see Table 32) deactivates all the drivers and puts all the slave nodes connected to the LIN bus into the Sleep mode. In 0xXX, XX stands for don’t care.

Output Driver Fault Handling

A summary of output driver device performance under fault conditions is summarized below. This includes reporting to the APPINFO register, the driver condition both during and after fault conditions, and what is required to clear reported faults.

Table 33. FAULT HANDLING

Fault	APPINFO Register	OUTPUT Register	Drivers Condition during Fault	Drivers Condition after Parameters within Specified Limits	Output Register clearing Requirement	APPINFO Register Clearing Requirement
Open load (OUT4 and OUT8)	Not signaled.	Signaled in OFF Mode	Per setting	Driver in Normal operation	Load re−connected	NA
Overcurrent	Latched	latched	Affected driver turns off after T_OC_det time	Affected driver is latched off	Command OFF the affected driver	Command OFF the affected driver (OUT4 and OUT8)
Local Thermal Shutdown (OUT4 and OUT8)	Latched + masked low when Global TSD	latched	All driver turns off	Affected driver is latched off	Exit Local TSD Command OFF the affected driver (OUT4 and OUT8)	Exit Local TSD Command OFF the affected driver (OUT4 and OUT8)
Global Thermal Shutdown (TSD)	Not latched	Signaled	All drivers switched OFF	Returns to the previous programmed state	Exit Global TSD	Exit Global TSD
Undervoltage	NA	Register is not accessible as LIN is disabled	Per Setting (Change of state not possible as LIN is disabled)	Driver in Normal operation	NA	NA

Table 34. FAULT REPORTING

	Drivers	
Fault	OUT1−3, 5−7	OUT4, 8
Open Load (OFF state)	No	Yes
Overcurrent (ON state)	Yes (0.6 A min)	Yes (0.75 A min)
Individual Over Temperature	No	Yes

1S0P Thermal Performance

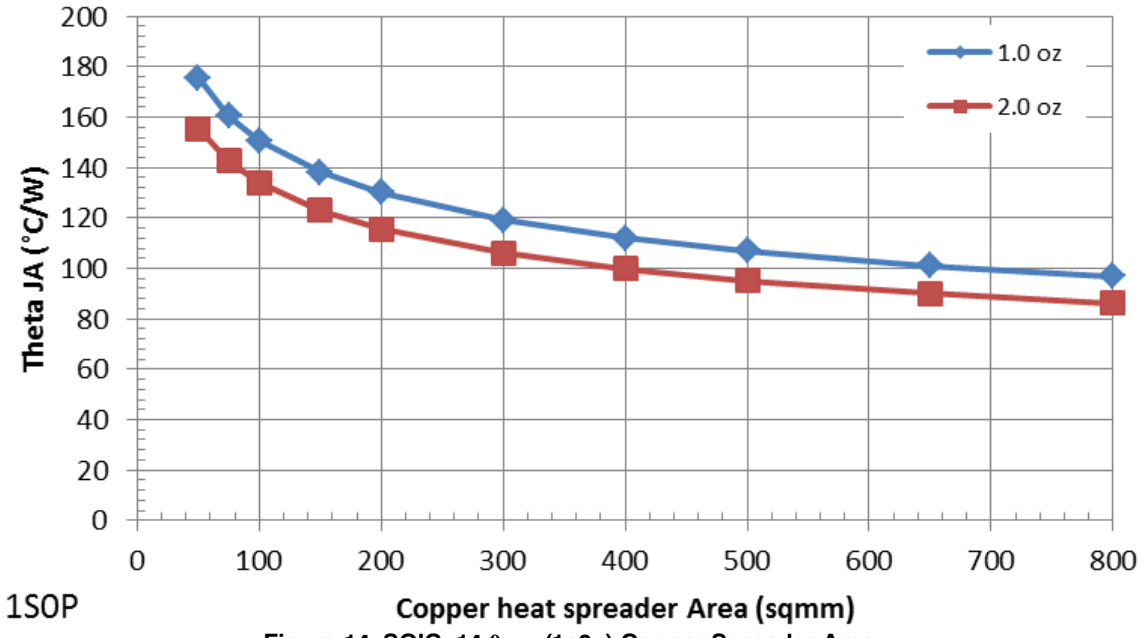


Figure 14. SOIC−14 θ_{J-A} (1s0p) Copper Spreader Area

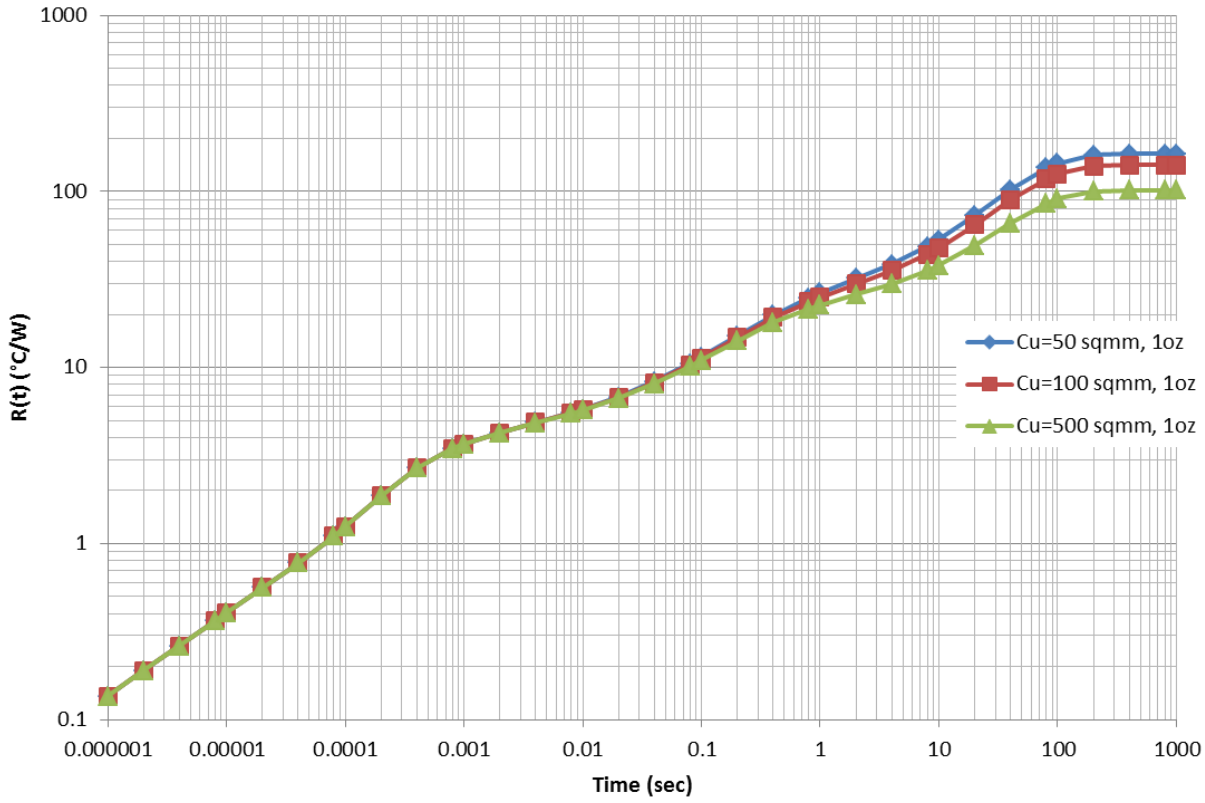


Figure 15. SOIC−14 Single Pulse Heating Curve (1s0p)

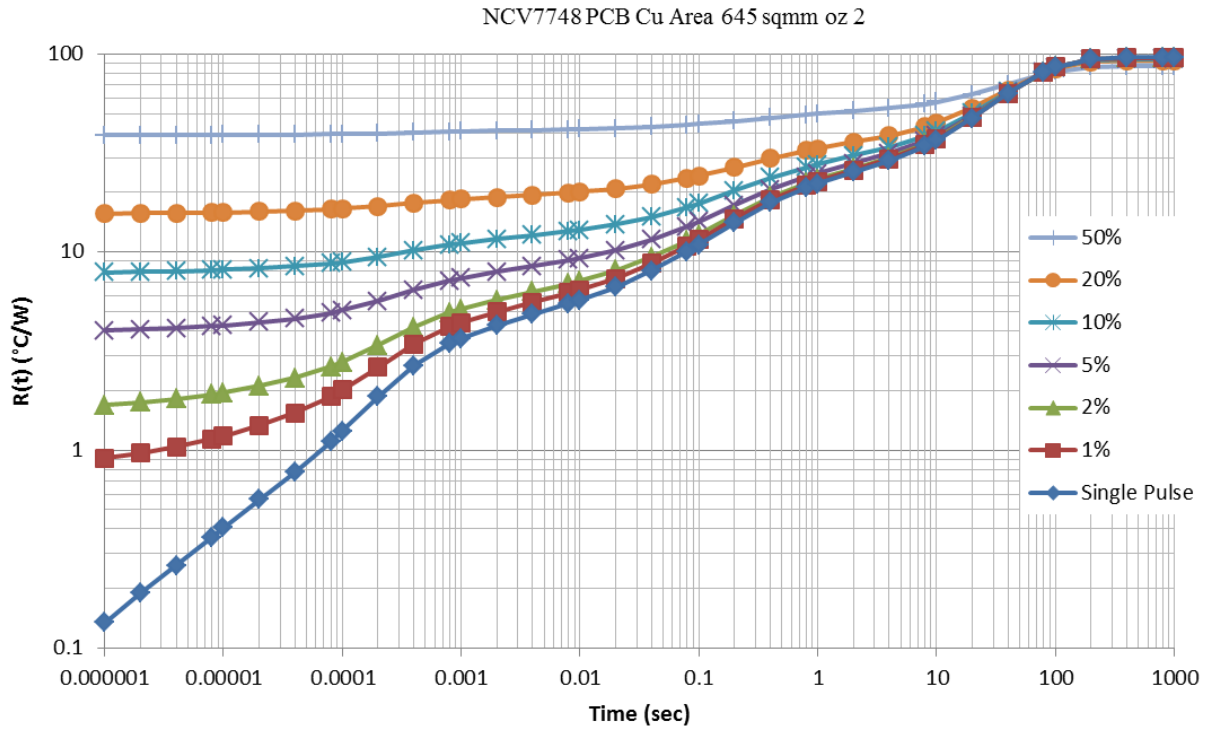
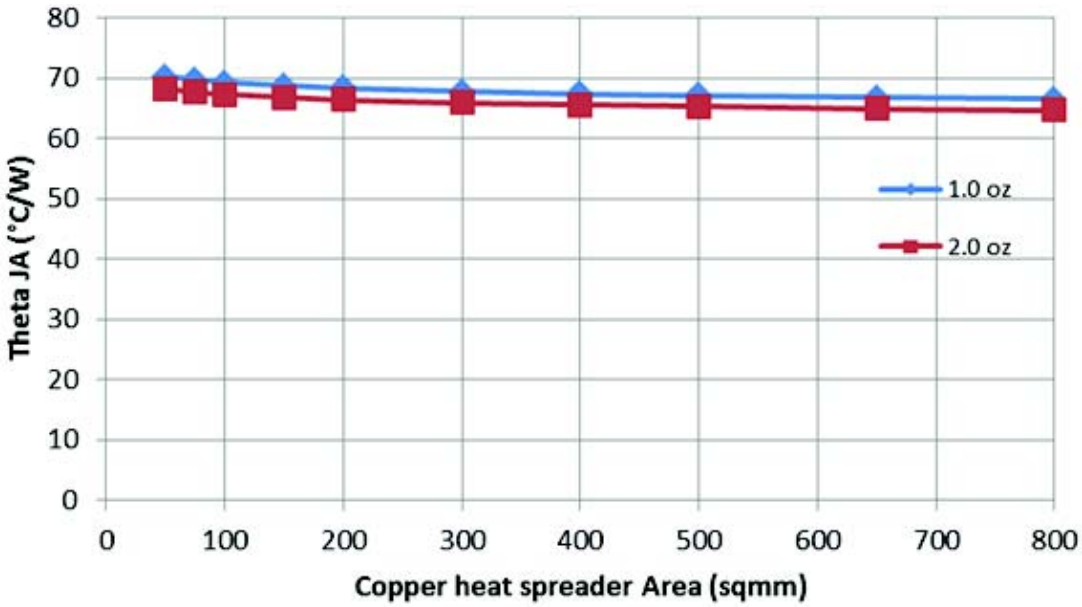


Figure 16. SOIC−14 Thermal Duty Cycle Curve on 645 mm2 Spreader Test Board (1s0p)

2S2P Thermal Performance



2s2p

Figure 17. SOIC−14 θ_{J-A} (2s2p) Copper Spreader Area

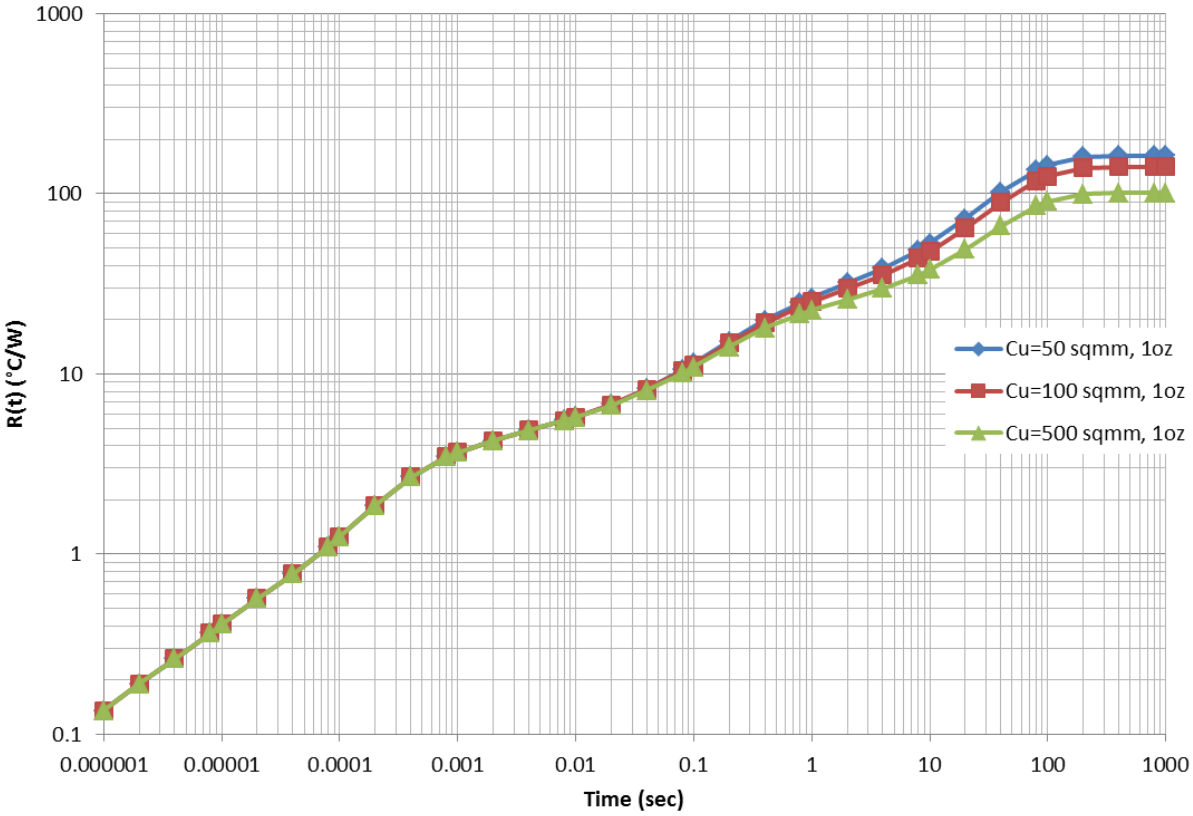


Figure 18. SOIC−14 Single Pulse Heating Curve (2s2p)

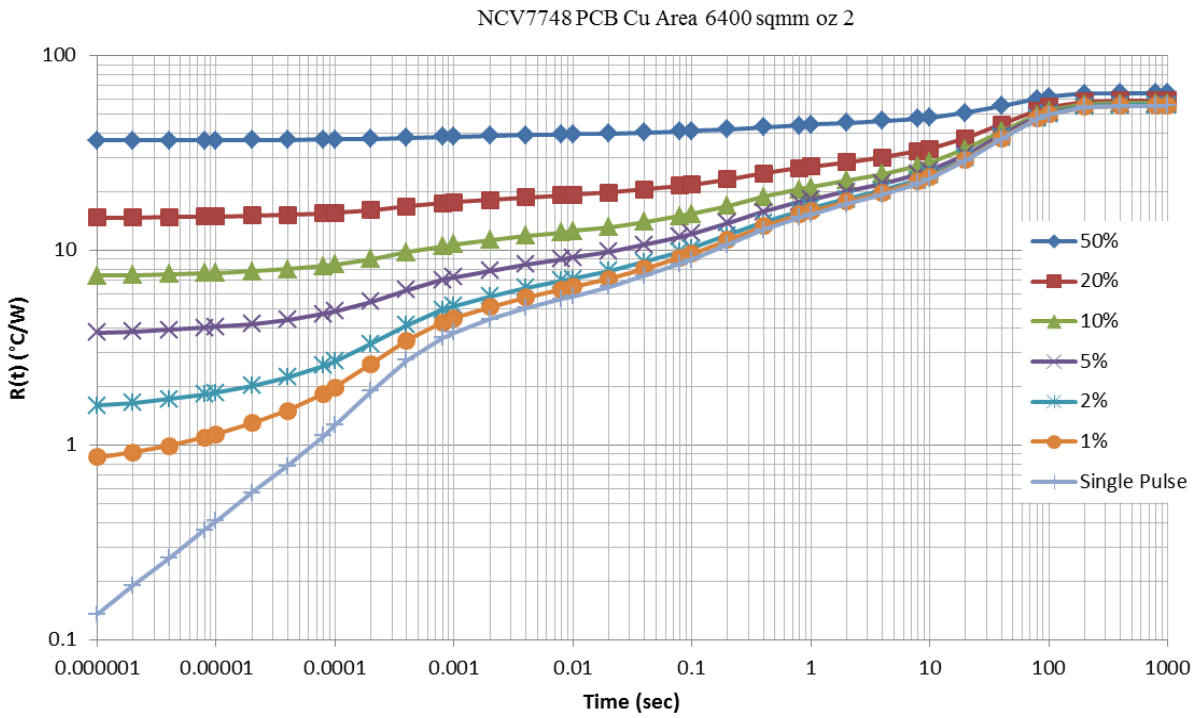


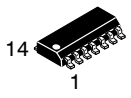
Figure 19. SOIC−14 Thermal Duty Cycle Curve on 645 mm2 Spreader Test Board (2s2p)

ORDERING INFORMATION

Device Order Number	Number of Channels	Package	Shipping†
NCV7748D2R2G	8	SOIC−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

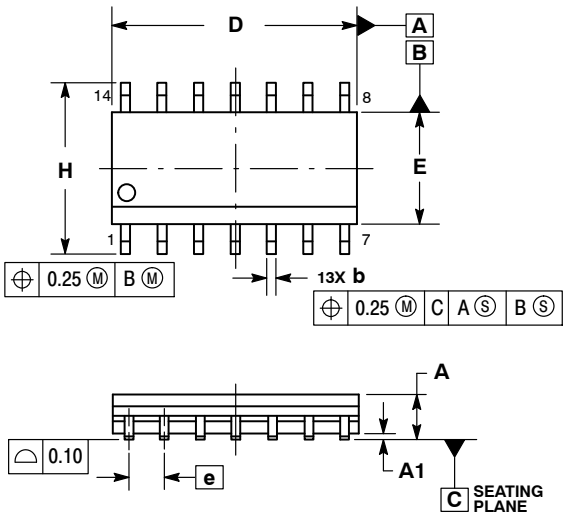
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

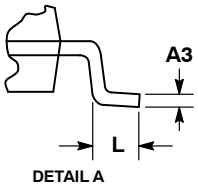


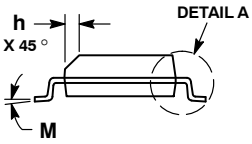
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



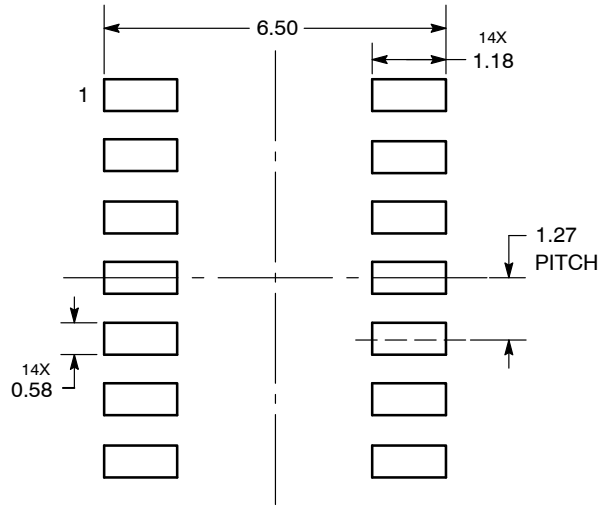




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

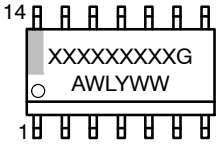
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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